CALIFORNIA STATE UNIVERSITY NORTHRIDGE

DESIGN OF A THREE STAGE MICROWAVE LOW NOISE AMPLIFIER AT 16 GHz

A graduate project submitted in partial fulfillment of the requirements

For the degree of Master of Science

in Electrical Engineering

By

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The graduate project of Pratik Patil is approved

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Acknowledgement

This project is not an individual effort; it's the culmination of all the moral support and encouragement provided by all my teachers, friends, and family who have motivated me to reach to this level. First of all, I would like to thank God for keeping me in good health and well-being, both physically and mentally, without which it would have been impossible to complete the project. I would like to thank my parents for raising me to be the person I am, for creating a spark in me for knowledge, supporting me financially and spiritually and being by my side in all the good times and the bad times.

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A Ku band multistage low noise amplifier also known as LNA was designed to operate at 16 GHz used mostly in radar applications. The LNA is required to provide a gain greater than 20dB and an overall noise figure of less than 2dB. NEC transistor NE321000, a heterojunction FET was selected for this design because it offered excellent gain and noise figure parameters at our required frequency. Simulations showed that the LNA provides a gain of 26 dB over a 10% bandwidth and a noise figure of 1.1dB. Thus, the LNA design met and exceeded our design requirements. It was determined by analysis that the first stage had to be designed as minimum noise and the other two stages as maximum gain to meet our overall noise and gain requirements. The input matching network, the output matching network and inter-stage matching networks were designed afterwards. The circuit schematic, layout and circuit test bench simulations were done using Agilent ADS. Stability, noise figure calculations and gain calculation were done manually as well as using ADS.
CHAPTER 1: INTRODUCTION

As the name suggests a low noise amplifier (LNA) is used as the first stage of the receiver where it amplifies the signal received through an antenna by keeping the noise as low as possible. As shown in figure 1, this generalized block diagram of a receiver the LNA is placed right after the antenna. LNA is a critical component of any receiver/transceiver assembly. The main role of the low noise amplifier is to amplify the signal such that it provides enough gain without any degradation in the signal to noise ratio. As the noise bandwidth is infinite, the LNA is generally placed after a band pass filter. This makes it necessary for perfect matching so as to get the maximum power transfer.

LNA is comparatively less complicated to design as opposed to other transceiver blocks such as mixers, filters, switches etc. Now designing an RF amplifier for both maximum power gain and minimum noise simultaneously is not possible, we use a three stage design to ensure both power gain and the noise figure, are within our required specifications. Designing a three stage amplifier is more complicated and it requires more importance on matching.

Figure 1: LNA block in a typical receiver block diagram [1].
1.1 Design Specifications

Design of a multistage low noise amplifier to meet the following requirements at 16GHz over a range of 10% bandwidth:

Noise figure $< 2$dB

Power Gain $> 20$ dB

Input VSWR $< 3$

Output VSWR $< 2$

Matching Circuit: Lumped element matching with characteristic impedance of 50 ohms

Operating frequency: 15.5-16.5 GHz with amplifier tuned at 16 GHz.

Following tasks will be demonstrated in designing this amplifier:

1. Device selection and characterization.
2. Gain and stability calculations both manually and using Matlab.
3. Matching network design by using smith chart and simulation software.
4. Circuit simulation using Agilent ADS.
5. Circuit Schematic.
CHAPTER 2: DESIGN THEORY

2.1 General Design theory

Microwave amplifiers can be categorized into two types depending on the power requirement.

1- **Small signal Amplifiers**
   
   This type of amplifier is used in small signal analysis. This type of amplifier design is used only when we assume that the signal is fluctuating from the steady bias level by a very small margin. Hence only small part of characteristics is covered in the analysis, so the operation is always in the linear region.

2- **Large signal Amplifiers**

   This type of design is used for active circuits with high amplitude signal level. A large part of operating characteristics is covered in this mode in which the non-linear part of the operating characteristic is also covered along with the linear region of operation. Hence, this type of amplifier design is more complicated to design and implement as compared to small signal amplifiers.

In our design, we will be using the small signal design hence we need not consider the non-linear region of the operating device.

Every type of amplifier design needs optimization of the power gain and noise figure in order to get maximum output and dissipate as little power as possible. To do so, matching networks as well as gain and noise circles are very important aspect of the design [2].

2.2 Classes of Amplifiers

Depending on the mode of operation of the amplifiers can further be classified into following classes:

A) **Class A amplifier**
   
   When all the transistors in the amplifier always operate in the active region it is known as Class A amplifier.

B) **Class B amplifier**

   When the transistors operate in the active region for half the cycle, the type of amplifier is called class B amplifier.
C) **Class AB amplifier**
When the transistors operate in class A mode for the small signal & in class B mode for the large signals it is known as class AB amplifier.

D) **Class C amplifier**
When the transistor is in the active for less than half the signal cycle, the mode of operation is called class C amplifier.

For a small signal amplifier we need to design both AC and DC parts of the circuit.

1) DC bias circuit
2) RF/Microwave circuit.

Both of the above blocks should be designed with proper isolation to prevent any leakage from the RF block into the DC and to prevent power loss.

As the mode of operation is linear in small signal analysis, we should use class A mode, and to achieve this proper biasing of the transistor need to be done so that the Q point is maintained in the midrange of $V_{DS}$-$I_{DS}$.

**2.3 DC Circuit design and Isolation**

![General characteristic transistor curve](image)

Figure 2: General characteristic transistor curve [2].
As shown in the figure 2, the Q point should be maintained properly to ensure good biasing of the transistor. The biasing conditions obtained from the datasheet of the transistor are as shown in the figure 3.

Figure 3: Transistor characteristics of NE321000.

RF circuitry and DC Circuitry isolation can be achieved using three ways [2]. These schemes are as follows:

1) Using and RF choke which is actually an inductor which allows DC but blocks high frequency RF signals.

2) Using a quarter wave transformer of very high impedance such that it would create a high impedance path for RF signals.

3) Using high value capacitors which act as open circuits and block RF signals that might leak into the DC circuitry.

Using more than one or all of these techniques will ensure a high degree of isolation between RF and DC as shown in the figure 4.
2.4 RF/MW circuit Design

Following steps must be followed to design a microwave amplifier at RF and Microwave frequencies:

1) Selecting a transistor depending upon the gain and noise figure requirement by looking at the s-parameters of the transistor at the desired frequency.

2) Biasing the transistor by selecting the Q point as mentioned in the datasheet so as to obtain the desired S-parameters.

3) Obtain the s-parameters from the data sheet or by measuring through simulations from the selected Q-point.

4) Checking for stability of the transistor at the desired frequency by using the s-parameters obtained in previous step using the K-Δ test.

5) If the transistor is not unconditionally stable at the desired frequency, draw the input and output stability circles and find the stable regions on the smith chart.

6) Calculating the gain using the unilateral or bilateral condition depending on the value of \( S_{12} \). For \( S_{12} \) not equal to zero finding the unilateral figure of merit to find the error range if unilateral condition is used. If error range is greater than 5% of the required bandwidth opt for bilateral method.

7) Finding the noise figure of the circuit and drawing the noise figure circles for low noise applications.
8) Designing a matching network using smith chart depending on the design of the amplifier.

Above steps can be summarized as shown in figure 5.

Figure 5: Summary of design steps for RF amplifier design [2].
2.5 Matching Network Design for LNA

In designing an LNA more importance is placed on the noise figure as compared to gain as we need to keep noise as low as possible and get as much gain as we can from the design [6].

The matching circuit can be designed by using the allocated gain values and by plotting the input and the output gain circles as well as the noise circles on the same smith chart. Then by choosing the point of the intersection of the gain and noise circles, we can choose $\Gamma_L$ and $\Gamma_S$ to design our matching network. For designing a minimum noise amplifier we can use the $\Gamma_{opt}$ provided in the datasheet and find $\Gamma_S$ and $\Gamma_L$ and design the matching network which can be summarized as shown in figure 6.

![Figure 6: General matching networks.](image)

2.6 Matching Network Design for an HGA

High gain amplifier has a simpler approach as compared to LNA design. After finding the stable region of operation we need to draw the constant gain circles and choosing any arbitrary point on the constant gain circles in the stable region, the input and the output matching networks can be designed.

For a maximum gain design we, can use $S_{11}^*$ and use it to match the input network and $S_{22}^*$ to design the output network provided both $S_{11}^*$ and $S_{22}^*$ are in the stable region [6].
2.7 Designing multistage amplifiers

Single stage amplifiers usually don’t provide enough gain as required for the design. Also multistage amplifiers can be used to provide both noise immunity and greater gain by cascading LNA and HGA amplifiers. Also with proper matching cascading the amplifiers usually improves the stability as well as VSWR as compared to that of the individual stages. Figure 7 shows the matching networks for a multistage design.

![Multistage Amplifier Diagram](image)

Figure 7: Multistage amplifier design input, output and inter-stage matching networks [3].
CHAPTER 3: DEVICE CHARACTERIZATION AND STABILITY

3.1 Overview

In this section we are going to select the transistor and then study the characteristics of the transistor by using the s-parameters from the data sheet. We are going to simulate our transistor over the desired frequency range and the device characterization will be done using Agilent ADS. Also we are going to check the stability, noise characteristics and VSWR of the transistor.

1. Selecting a Transistor (NE321000) and obtain its S-parameters from the datasheet.
2. Simulate the transistor by carrying out an S-parameter sweep using ADS.
3. Study the noise and VSWR characteristics of the transistor through simulations.
4. Finding the stability of the transistor over our desired frequency range.

3.2 Device selection and characterization

Following an intense investigation and after analyzing several devices for maximum gain, noise figure and stability, we came across a HJ FET from NEC corp. NE321000, which is an ultra-low noise FET. This transistor was selected because it offers very good gain, noise figure and robust stability. Also Agilent ADS has NEC NE321000 transistor in its library.

The operating Q point of this transistor is at $V_{DS} = 2V$ and $I_{DS} = 10mA$. The S-parameters of the device can be obtained from the data sheet. See appendix A for more details. It is necessary to carry out a simulation of the transistor in ADS so that we can see if the transistor performs as per the datasheet.

We do a simple S-parameter sweep of the transistor in ADS to get its specifications.

We put simple 50 ohms terminations across the transistor. Then we simulate the transistor by placing settings like S-parameter, GaCircle, and NsCircle etc. in the work area. The frequency of operation is ranges from 2GHz to 20GHz.

The schematic of the S-parameter sweep is as shown in the figure 8. The simulated noise figure value and s-parameters are shown in tables 1 and table 2, respectively.
Figure 8: Schematic of S-parameter linear frequency sweep of NE321000 using ADS

<table>
<thead>
<tr>
<th>freq</th>
<th>NFmin</th>
<th>Sopt</th>
<th>Rn</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.000 GHz</td>
<td>0.210</td>
<td>0.940 / 3.700</td>
<td>15.500</td>
</tr>
<tr>
<td>3.000 GHz</td>
<td>0.215</td>
<td>0.905 / 5.950</td>
<td>15.500</td>
</tr>
<tr>
<td>4.000 GHz</td>
<td>0.220</td>
<td>0.870 / 8.200</td>
<td>15.500</td>
</tr>
<tr>
<td>5.000 GHz</td>
<td>0.230</td>
<td>0.845 / 10.750</td>
<td>15.750</td>
</tr>
<tr>
<td>6.000 GHz</td>
<td>0.240</td>
<td>0.820 / 13.300</td>
<td>16.000</td>
</tr>
<tr>
<td>7.000 GHz</td>
<td>0.250</td>
<td>0.795 / 16.050</td>
<td>16.000</td>
</tr>
<tr>
<td>8.000 GHz</td>
<td>0.260</td>
<td>0.770 / 18.800</td>
<td>16.000</td>
</tr>
<tr>
<td>9.000 GHz</td>
<td>0.270</td>
<td>0.750 / 21.800</td>
<td>16.000</td>
</tr>
<tr>
<td>10.000 GHz</td>
<td>0.280</td>
<td>0.730 / 24.800</td>
<td>16.000</td>
</tr>
<tr>
<td>11.000 GHz</td>
<td>0.295</td>
<td>0.710 / 28.100</td>
<td>15.750</td>
</tr>
<tr>
<td>12.000 GHz</td>
<td>0.310</td>
<td>0.690 / 31.400</td>
<td>15.500</td>
</tr>
<tr>
<td>13.000 GHz</td>
<td>0.345</td>
<td>0.680 / 34.900</td>
<td>15.500</td>
</tr>
<tr>
<td>14.000 GHz</td>
<td>0.380</td>
<td>0.670 / 38.400</td>
<td>15.500</td>
</tr>
<tr>
<td>15.000 GHz</td>
<td>0.415</td>
<td>0.655 / 42.150</td>
<td>15.250</td>
</tr>
<tr>
<td>16.000 GHz</td>
<td>0.450</td>
<td>0.640 / 45.900</td>
<td>15.000</td>
</tr>
<tr>
<td>17.000 GHz</td>
<td>0.485</td>
<td>0.635 / 49.900</td>
<td>14.750</td>
</tr>
<tr>
<td>18.000 GHz</td>
<td>0.520</td>
<td>0.630 / 53.900</td>
<td>14.500</td>
</tr>
<tr>
<td>19.000 GHz</td>
<td>0.555</td>
<td>0.625 / 58.150</td>
<td>14.250</td>
</tr>
<tr>
<td>20.000 GHz</td>
<td>0.590</td>
<td>0.620 / 62.400</td>
<td>14.000</td>
</tr>
</tbody>
</table>

Table 1: Minimum Noise figure and $\Gamma_{opt}$ vs frequency.

After getting the output we display the S-parameter table and after close observation we see that the transistor behaves exactly the same as given in the datasheet.
Table 2: Results of S-parameter simulation of NE321000

<table>
<thead>
<tr>
<th>freq</th>
<th>S(1,1)</th>
<th>S(1,2)</th>
<th>S(2,1)</th>
<th>S(2,2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.000 GHz</td>
<td>0.979 / -15.880</td>
<td>0.030 / 0.100</td>
<td>4.700 / 161.370</td>
<td>0.631 / -11.440</td>
</tr>
<tr>
<td>3.000 GHz</td>
<td>0.952 / -24.040</td>
<td>0.045 / 75.460</td>
<td>4.658 / 152.380</td>
<td>0.618 / -16.890</td>
</tr>
<tr>
<td>4.000 GHz</td>
<td>0.918 / -32.490</td>
<td>0.059 / 70.710</td>
<td>4.602 / 143.310</td>
<td>0.598 / -22.570</td>
</tr>
<tr>
<td>5.000 GHz</td>
<td>0.876 / -41.180</td>
<td>0.072 / 65.920</td>
<td>4.536 / 134.130</td>
<td>0.574 / -28.450</td>
</tr>
<tr>
<td>6.000 GHz</td>
<td>0.826 / -53.050</td>
<td>0.087 / 59.370</td>
<td>4.557 / 123.190</td>
<td>0.517 / -37.470</td>
</tr>
<tr>
<td>7.000 GHz</td>
<td>0.756 / -62.140</td>
<td>0.097 / 55.240</td>
<td>4.400 / 114.520</td>
<td>0.492 / -42.710</td>
</tr>
<tr>
<td>8.000 GHz</td>
<td>0.704 / -71.410</td>
<td>0.107 / 51.140</td>
<td>4.241 / 105.890</td>
<td>0.463 / -47.930</td>
</tr>
<tr>
<td>9.000 GHz</td>
<td>0.652 / -81.350</td>
<td>0.116 / 47.150</td>
<td>4.086 / 97.180</td>
<td>0.428 / -53.460</td>
</tr>
<tr>
<td>10.00 GHz</td>
<td>0.599 / -91.600</td>
<td>0.125 / 43.280</td>
<td>3.925 / 88.590</td>
<td>0.390 / -59.620</td>
</tr>
<tr>
<td>11.00 GHz</td>
<td>0.547 / -102.520</td>
<td>0.132 / 39.420</td>
<td>3.757 / 80.010</td>
<td>0.351 / -66.370</td>
</tr>
<tr>
<td>12.00 GHz</td>
<td>0.500 / -113.970</td>
<td>0.140 / 36.010</td>
<td>3.591 / 71.670</td>
<td>0.313 / -74.060</td>
</tr>
<tr>
<td>13.00 GHz</td>
<td>0.459 / -126.080</td>
<td>0.146 / 32.770</td>
<td>3.418 / 63.450</td>
<td>0.279 / -82.240</td>
</tr>
<tr>
<td>14.00 GHz</td>
<td>0.425 / -138.720</td>
<td>0.153 / 29.590</td>
<td>3.241 / 55.380</td>
<td>0.247 / -93.600</td>
</tr>
<tr>
<td>15.00 GHz</td>
<td>0.398 / -151.460</td>
<td>0.160 / 26.770</td>
<td>3.069 / 47.700</td>
<td>0.221 / -105.600</td>
</tr>
<tr>
<td>16.00 GHz</td>
<td>0.380 / -164.210</td>
<td>0.166 / 24.330</td>
<td>2.904 / 40.360</td>
<td>0.206 / -118.230</td>
</tr>
<tr>
<td>17.00 GHz</td>
<td>0.370 / -176.460</td>
<td>0.174 / 22.070</td>
<td>2.750 / 33.250</td>
<td>0.195 / -131.110</td>
</tr>
<tr>
<td>18.00 GHz</td>
<td>0.365 / -171.420</td>
<td>0.183 / 19.950</td>
<td>2.606 / 26.430</td>
<td>0.188 / -144.120</td>
</tr>
<tr>
<td>19.00 GHz</td>
<td>0.365 / -159.530</td>
<td>0.194 / 17.750</td>
<td>2.476 / 19.760</td>
<td>0.187 / -156.140</td>
</tr>
<tr>
<td>20.00 GHz</td>
<td>0.373 / 147.720</td>
<td>0.206 / 15.550</td>
<td>2.358 / 13.260</td>
<td>0.193 / -168.030</td>
</tr>
</tbody>
</table>

Figure 9: S-parameter plot of the transistor NE321000.
Noise figure, S-parameter and VSWR measurements are very important when we design an amplifier. From figure 9 we see that $S_{11}$ also known as input return loss is equal to -8.404 dB, $S_{12}$ i.e. isolation is equal to -15.598 dB, $S_{21}$ also called as the forward gain is equal to 9.260 dB and $S_{22}$ output return loss equal to -13.723 dB.

Active directivity i.e. “the measure of how much the source match gets affected by the load impedance or vice versa”, can be measured from above-mentioned parameters. Active directivity can be defined as the difference between the forward gain and the isolation [4]. In our case, active directivity is equal to 25.218 dB.

![Figure 10: VSWR of transistor NE 321000.](image)

![Figure 11: Noise figure of the transistor NE 321000.](image)
From the figure 10 we can see that the input and the output VSWR of the transistor are measured to be around 2.226 and 1.519 respectively. By adding appropriate matching networks these VSWR values can be improved.

The noise figure from figure 11 is equal to around 1.215 dB and our specification is about 2 dB which means for each stage we need to have a noise figure no more than 0.7 dB. By selecting the optimum value of \( \Gamma \) we can optimize our design for minimum noise and the actual noise figure would be much smaller than 2 dB.

### 3.3 Stability checks using manual calculations and Matlab

S-parameters at 16GHz are as follows:

\[
S_{11} = 0.38 \angle -164.21^\circ \\
S_{12} = 0.166 \angle 24.33^\circ \\
S_{21} = 2.904 \angle 40.360^\circ \\
S_{22} = 0.206 \angle -118.23^\circ
\]

Using these S-parameters, the stability of the transistor can be determined. The stability parameters \( K \), \( \Delta \) and \( \mu \) are now calculated using the above-mentioned S-parameters [5].

\[
K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|}
\]

\[
= 1 - |0.38|^2 - |0.206|^2 + |0.405|^2 \\
= \frac{2|0.4814|}{2|0.4814|}
\]

\[
= 1.014
\]

\[
\Delta = S_{11}S_{22} - S_{12}S_{21}
\]
\[
= (0.38 \angle -164.21^\circ)(0.206 \angle -118.23^\circ) - (0.166 \angle 24.33^\circ)(2.904 \angle 40.360^\circ)
\]

\[= 0.405 \angle -117.7^\circ\]

The values of K and Δ were calculated using Matlab and it yielded same results. See Appendix (B) for Matlab.

Hence, the transistor is unconditionally stable as, |Δ|<1, K<1.

The three stage design is as shown in figure 12.

![Block diagram for the three stage amplifier](image)

Figure 12: Block diagram for the three stage amplifier
CHAPTER 4: DESIGNING OF THE AMPLIFIER USING LUMPED ELEMENTS

4.1 Overview

The design we are trying to implement will provide gain greater than 20 dB and a noise figure of no more than 2 dB over a 10% bandwidth with center frequency at 16 GHz. A systematic approach will be used to try and get the desired output from our LNA. First we will design single stages and then try and design a three stage amplifier. The general design flow which was used is as follows:

1. Designing a single stage minimum noise amplifier using lumped elements.
2. Designing a single stage maximum gain amplifier using lumped elements.
3. Designing a three stage amplifier using cascading.

4.2 Single stage minimum noise amplifier design using lumped elements

As our transistor is unconditionally stable at 16 GHz we can now proceed with our design.

To find gain associated with the MNA design and the matching networks we first need to calculate $\Gamma_S$ and $\Gamma_L$. From the data sheet at 16 GHz we see that

$\Gamma_{opt} = 0.64\angle 45.9^\circ$

$F_{min} = 0.45$ dB.

Now the noise figure can be calculated by,

$$F = F_{min} + \frac{4R_n |\Gamma_s - \Gamma_{opt}|^2}{(1 - |\Gamma_s|^2)(1 + |\Gamma_{opt}|^2)}$$

By choosing $\Gamma_S = \Gamma_{opt}$ we get

$$F = F_{min}$$

Therefore $\Gamma_S = 0.64\angle 45.9^\circ$.

And the value of $\Gamma_L$ can be found using the equation,
\[ \Gamma_L^* = \Gamma_{out} = S_{22} + \frac{S_{21}S_{12}\Gamma_S}{1 - S_{11}\Gamma_S} \]

\[ \Gamma_L^* = 0.206\angle -118.23^\circ + \frac{(0.166\angle 24.33^\circ)(2.904\angle 40.360^\circ)(0.64\angle 45.9^\circ)}{1 - (0.38\angle -164.21^\circ)(0.64\angle 45.9^\circ)} \]

\[ \Gamma_L^* = 0.167\angle 149.01^\circ \]

Therefore \( \Gamma_L = 0.167 \angle -149.01^\circ \)

Using \( \Gamma_S \) and \( \Gamma_L \) the gain of the amplifier can be calculated by using the formula.

\[ G_T = \frac{1 - |\Gamma_S|^2}{|1 - S_{11}\Gamma_S|^2} \cdot |S_{21}|^2 \cdot \frac{1}{1 - |\Gamma_L|^2} \]

\[ = \frac{1 - |0.64|^2}{|1 - (0.38\angle -164.21^\circ)(0.64\angle 45.9^\circ)|^2} \cdot |2.9|^2 \cdot \frac{1}{1 - |(0.167\angle -149.01^\circ)|^2} \]

\[ = 3.922 \]

\( G_T = 5.936 \, dB \).

Therefore from each LNA stage we can obtain 5.936 dB gain.

To design the matching networks reflection coefficient of the source \( \Gamma_S \) and reflection coefficient of the load \( \Gamma_L \) can be used. By moving from the center of the smith chart, i.e. from \( Z_0 \) to \( \Gamma_S \) we can find the following input matching network lumped element values.
Series C:

\[ jX_s = \frac{-j}{\omega C Z_0} \]

\[ -j1.7 = \frac{-j}{(2\pi \times 16E9 \times 50 \times C)} \]

\[ C = 0.117\text{pF} \]

Shunt L:

\[ jB_p = \frac{-j}{\omega L Y_0} \]

\[ -j0.87 = \frac{-j \times 50}{(2\pi \times 16E9 \times L)} \]

\[ L = 0.571\text{nH} \]

These results were verified using the smith tool of the ADS and we got the same values as shown in the figure 12. Similarly by moving from the center of the smith chart towards \( \Gamma_L \) we can find the following output matching network lumped element values for the MNA.

Shunt \( C = 0.123 \text{ pF} \)

Series \( L = 0.153 \text{ nH} \).

The results can be verified using ADS smith tool utility as shown in figure 13.

After the matching networks were designed the circuit was simulated in ADS between 15.5GHz to 16.5GHz and the schematic is shown in figure 14.
<table>
<thead>
<tr>
<th>Network</th>
<th>Component</th>
<th>Simulated using ADS</th>
<th>Simulated using Matlab</th>
<th>Calculated</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input matching network</td>
<td>Series C</td>
<td>0.117 pF</td>
<td>0.11703 pF</td>
<td>0.117 pF</td>
</tr>
<tr>
<td></td>
<td>Shunt L</td>
<td>0.571 nH</td>
<td>0.57168 nH</td>
<td>0.571 nH</td>
</tr>
<tr>
<td>Output matching network</td>
<td>Shunt C</td>
<td>0.123 pF</td>
<td>0.12335 pF</td>
<td>0.1229 pF</td>
</tr>
<tr>
<td></td>
<td>Series L</td>
<td>0.153 nH</td>
<td>0.15148 nH</td>
<td>0.154 nH</td>
</tr>
</tbody>
</table>

Table 3: Lumped elements matching network components for MNA
Figure 13: Input and Output matching networks for MNA calculated using smith tool of ADS.
Figure 14: MNA schematic in ADS

Figure 15: Noise figure simulation of MNA
The simulation results yield a gain of 6.017 dB and a noise figure of 0.455 dB. The input and output VSWR is equal to 1.991 and 1.368. There is an improvement in the input and the output VSWR of the transistor after optimizing it for minimum noise design and after adding the matching networks.
4.3 Single stage maximum gain amplifier design using lumped elements

Designing a single stage maximum gain amplifier is less complicated as far as calculations are concerned as compared to a minimum noise amplifier. The maximum gain occurs when

$$\Gamma_{in} = S_{11}^* \quad \text{and} \quad \Gamma_{out} = S_{22}^* \quad \text{if} \quad S_{12} = 0$$

To find our gain first we need to find the unilateral figure of merit $U$, as our $S_{12}$ i.e. the isolation from the source to the load is not equal to zero [6].

Where $U$ is given by

$$U = \frac{|S_{11}| |S_{12}| |S_{21}| |S_{22}|}{(1 - |S_{11}|^2)(1 - |S_{22}|^2)}$$

$$= \frac{(0.38)(0.166)(2.904)(0.206)}{(1 - |0.38|^2)(1 - |0.206|^2)}$$

$$= 0.0459$$

From $U$, we can find the error which will arise if we use unilateral assumption.

$$\frac{1}{1 + U^2} < \frac{G_T}{G_{TU, max}} < \frac{1}{1 - U^2}$$

$$0.914 < \frac{G_T}{G_{TU, max}} < 1.098$$

$$-0.39 \text{ dB} < \frac{G_T}{G_{TU, max}} < 0.406 \text{ dB}$$

The gain for MGA design for unilateral assumption is given by

$$G_{TU, max} = G_{S, max} \times G_o \times G_{L, max}$$

$$G_{S, max} = \frac{1}{1 - |S_{11}|^2} = 1.168$$

$$G_o = |S_{21}|^2 = 8.597$$

23
\[ G_{L,\text{max}} = \frac{1}{1 - |S_{22}|^2} = 1.249 \]

\[ G_{T_u,\text{max}} = 11.26 = 10.53\,dB \]

As we can see that the error associated with using unilateral assumption is almost less than 5% of the required gain, we can proceed with our unilateral assumption.

<table>
<thead>
<tr>
<th></th>
<th>Simulated using ADS</th>
<th>Simulated using Matlab</th>
<th>Calculated</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input matching</td>
<td>Shunt C</td>
<td>0.217 pF</td>
<td>0.218 pF</td>
</tr>
<tr>
<td>network</td>
<td>Series L</td>
<td>0.306 nH</td>
<td>0.3058 nH</td>
</tr>
<tr>
<td>Output matching</td>
<td>Series L</td>
<td>0.356 nH</td>
<td>0.3581 nH</td>
</tr>
<tr>
<td>network</td>
<td>Shunt C</td>
<td>0.103 pF</td>
<td>0.10345 pF</td>
</tr>
</tbody>
</table>

Table 4: Lumped elements matching network components for MGA

The source and the load matching networks can be designed using \( S_{11}^* \) and \( S_{22}^* \) respectively.

Input matching network can be found by moving from the center of the smith chart i.e. from \( Z_0 \) towards \( S_{11}^* \). For input network, manual calculations on smith chart yield

Shunt C = 0.215 pF

Series L = 0.303 nH

Similarly output matching network can be found by moving from \( S_{22}^* \) towards the center of the smith chart. Manual calculations yield

Series L = 0.35 nH and
Shunt C = 0.104 pF.
Figure 18: Input matching network and output matching networks for MGA design.
The matching network results were verified using ADS smith tool, and it yielded same results. As shown in the figure 18.

Figure 19 : MGA schematic using ADS.
After the matching networks were designed the circuit was simulated in ADS between 15.5GHz to 16.5GHz and the schematic is shown in the figure 19.

Figure 20: Power gain of MGA

Figure 21: Input and Output VSWR of MGA design.

The simulation results yielded a total power gain of 10.502dB which is consistent with our calculated and Matlab results. Input and output VSWR of 1.293 and 1.630 was obtained which is very good.
4.4 Final three stage design using cascading

We will use the cascaded design where the three stages of the amplifier are just cascaded with no further modifications to the circuit. We are using the first stage as the minimum noise and other two stages as maximum gain to maximize gain. The equivalent noise figure of the three stage cascaded design is given by

\[ F_{\text{cascaded}} = F_1 + \frac{F_2 - 1}{G_{A1}} + \frac{F_3 - 1}{G_{A1}G_{A2}} \]

Where \( F_1 \) is the noise figure of first stage and \( F_2 \) and \( F_3 \) are the noise figures of stage 2 and 3 respectively. Similarly, \( G_{A1} \) and \( G_{A2} \) are the gains of stage 1 and 2 respectively.

First stage is minimum noise amplifier so \( F_1 = F_{\text{min}} \).

As the second and the third stages are maximum gain amplifiers, \( \Gamma_s = S_{11} \), \( \Gamma_{\text{opt}} = 0.64 \angle 45.9^\circ \), \( r_n = 0.3 \), and \( F_{\text{min}} = 0.45 \text{dB} = 1.1104 \)

\[ F_2 = F_3 = F_{\text{min}} + \frac{4r_n|\Gamma_s - \Gamma_{\text{opt}}|^2}{(1 - |\Gamma_s|^2)(|1 + \Gamma_{\text{opt}}|^2)} \]

\[ F_2 = F_3 = 1.69 \]

Substituting the values in for \( F_{\text{cascaded}} \) we get,

\[ F_{\text{cascaded}} = 1.11 + \frac{1.69 - 1}{3.923} + \frac{1.69 - 1}{3.923 \times 11.27} \]

\[ F_{\text{cascaded}} = 1.284 = 1.08 \text{ dB} \]

After cascading the three stages we get the final schematic as shown in the figure 22

Here we can see that both the inter-stage matching networks have capacitors in parallel which can be combined to reduce the number of components and hence reduce the complexity of the design. The final simplified circuit is shown in figure 23.
Figure 22: Three stage cascaded design schematic using ADS.
Figure 23: The final three stage design with less number of components.
After running the simulations we can see that the simulated power gain and noise figure values are in line with the calculated values.

Figure 24: Noise figure of the three stage design.

Figure 25: Power gain of the three stage design
The cascaded design yields a better result with an overall gain of 26.817 dB at 16 GHz and noise figure of 1.006 dB which are well within our specified limits and in line with our calculated values. Also the cascaded design gives a very good VSWR that is measured to be 2.178 at the input and 1.544 at the output.
CHAPTER 5: CONCLUSION

We have successfully designed a three stage Low Noise amplifier using an inexpensive NE321000, a heterojunction field effect transistor. Simulation results showed that the LNA met the design goal and has a gain of more than 25dB, a noise figure less than 1.5dB, input VSWR of less than 3 and output VSWR less than 2, for 15.5GHz to 16.5GHz frequency range. The matching networks were designed using lumped elements. The performance of the LNA is listed in the table below.

<table>
<thead>
<tr>
<th></th>
<th>Specified</th>
<th>Calculated by hand</th>
<th>Simulated using Matlab</th>
<th>Simulated using ADS</th>
</tr>
</thead>
<tbody>
<tr>
<td>MNA Gain</td>
<td>N/A</td>
<td>5.936 dB</td>
<td>5.989 dB</td>
<td>6.017 dB</td>
</tr>
<tr>
<td>MGA Gain</td>
<td>N/A</td>
<td>10.53 dB</td>
<td>10.1255 dB</td>
<td>10.502 dB</td>
</tr>
<tr>
<td>Total Gain</td>
<td>&gt;20 dB</td>
<td>26.996 dB</td>
<td>26.229 dB</td>
<td>26.817dB</td>
</tr>
<tr>
<td>Input VSWR</td>
<td>&lt; 3</td>
<td>N/A</td>
<td>N/A</td>
<td>2.178</td>
</tr>
<tr>
<td>Output VSWR</td>
<td>&lt; 2</td>
<td>N/A</td>
<td>N/A</td>
<td>1.544</td>
</tr>
<tr>
<td>Noise Figure</td>
<td>&lt; 2dB</td>
<td>1.08 dB</td>
<td>1.0432</td>
<td>1.006 dB</td>
</tr>
</tbody>
</table>

Table 5: Final Gain, VSWR and Noise figure calculations
REFERENCES


APPENDIX (A)

ULTRA LOW NOISE PSEUDOMORPHIC HJ FET

FEATURES
- SUPER LOW NOISE FIGURE:
  0.35 dB Typ at f = 12 GHz
- HIGH ASSOCIATED GAIN:
  13.0 dB Typ at f = 12 GHz
- GATE LENGTH: ≤0.2 μm
- GATE WIDTH: 160 μm

DESCRIPTION
NEC's NE321000 is a Hetero-Junction FET chip that utilizes
the junction between Si-doped AlGaAs and undoped InGaAs
to create high electron mobility. Its excellent low noise figure
and high associated gain make it suitable for commercial,
industrial and space applications.

NEC’s stringent quality assurance and test procedures assure
the highest reliability and performance.

ELECTRICAL CHARACTERISTICS (Ta = 25°C)

<table>
<thead>
<tr>
<th>PART NUMBER PACKAGE OUTLINE</th>
<th>NE321000 CHIP</th>
</tr>
</thead>
<tbody>
<tr>
<td>SYMBOLS</td>
<td>PARAMETERS AND CONDITIONS</td>
</tr>
<tr>
<td>NF</td>
<td>Noise Figure, Vds = 2 V, ib = 10 mA, f = 12 GHz</td>
</tr>
<tr>
<td>GM</td>
<td>Associated Gain, Vds = 2 V, ib = 10 mA, f = 12 GHz</td>
</tr>
<tr>
<td>IS</td>
<td>Saturated Drain Current, Vds = 2 V, Vgs = 0 V</td>
</tr>
<tr>
<td>VP</td>
<td>Pinch-off Voltage, Vds = 2 V, ib = 100 μA</td>
</tr>
<tr>
<td>gm</td>
<td>Transconductance, Vds = 2 V, ib = 10 μA</td>
</tr>
<tr>
<td>iAcc</td>
<td>Gate to Source Leakage Current, Vgs = -3 V</td>
</tr>
</tbody>
</table>

Note:
1. RF performance is determined by packaging and testing 10 samples per wafer. Wafer rejection criteria for standard devices is 2 rejects per 10 samples.
NE321000

**ABSOLUTE MAXIMUM RATINGS** (T<sub>a</sub> = 25°C)

<table>
<thead>
<tr>
<th>SYMBOLS</th>
<th>PARAMETERS</th>
<th>UNITS</th>
<th>RATING(S)</th>
</tr>
</thead>
<tbody>
<tr>
<td>V&lt;sub&gt;DS&lt;/sub&gt;</td>
<td>Drain to Source Voltage</td>
<td>V</td>
<td>4.0</td>
</tr>
<tr>
<td>V&lt;sub&gt;GS&lt;/sub&gt;</td>
<td>Gate to Source Voltage</td>
<td>V</td>
<td>-3.0</td>
</tr>
<tr>
<td>I&lt;sub&gt;DS&lt;/sub&gt;</td>
<td>Drain Current</td>
<td>mA</td>
<td>I&lt;sub&gt;ds&lt;/sub&gt;</td>
</tr>
<tr>
<td>I&lt;sub&gt;G&lt;/sub&gt;</td>
<td>Gate Current</td>
<td>mA</td>
<td>100</td>
</tr>
<tr>
<td>P&lt;sub&gt;DI&lt;/sub&gt;</td>
<td>Total Power Dissipation</td>
<td>mW</td>
<td>200</td>
</tr>
<tr>
<td>T&lt;sub&gt;CH&lt;/sub&gt;</td>
<td>Channel Temperature</td>
<td>°C</td>
<td>175</td>
</tr>
<tr>
<td>T&lt;sub&gt;ST&lt;/sub&gt;</td>
<td>Storage Temperature</td>
<td>°C</td>
<td>-45 to +175</td>
</tr>
</tbody>
</table>

**NOTES:**
1. Operation in excess of any one of these parameters may result in permanent damage.
2. Chip mounted on Alumina heat sink.

**RECOMMENDED OPERATING CONDITIONS** (T<sub>a</sub> = 25°C)

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>NE321000</th>
</tr>
</thead>
</table>

**TYPICAL PERFORMANCE CURVES** (T<sub>a</sub> = 25°C)

1. Total Power Dissipation vs. Ambient Temperature
2. Drain Current vs. Drain to Source Voltage
3. Drain Current vs. Gate to Source Voltage
APPENDIX (B)

% Matlab Program to calculate the stability, gain and noise figure of the transistor.
clear all; clc;
% Getting the S-parameter values from the user.
s11_mag=input('Enter the magnitude of s11 ');
s11_phase=input('Enter the phase of s11 in degrees ');

s12_mag=input('Enter the magnitude of s12 ');
s12_phase=input('Enter the phase of s12 in degrees ');

s21_mag=input('Enter the magnitude of s21 ');
s21_phase=input('Enter the phase of s21 in degrees ');

s22_mag=input('Enter the magnitude of s22 ');
s22_phase=input('Enter the phase of s22 in degrees ');

% S-parameter matrix
s = [s11_mag*exp(j*deg2rad(s11_phase))
     s12_mag*exp(j*deg2rad(s12_phase)); ...
     s21_mag*exp(j*deg2rad(s21_phase))
     s22_mag*exp(j*deg2rad(s22_phase))];

% Calculating delta
delta = s(1,1)*s(2,2) - s(1,2)*s(2,1);

% Calculating rollet stability factor K
K = (1 - abs(s(1,1))^2 - abs(s(2,2))^2 +
    abs(delta)^2)/abs(2*s(1,2)*s(2,1));

display(K);
X1 = ['magnitude of delta = ' num2str(abs(delta))];
X2 = ['phase of delta = ' num2str(rad2deg(angle(delta)))];
disp(X1);
disp(X2);

% Checking for stability
if (K>1) && (abs(delta)<1);
    display('Transistor is unconditionally stable, we can proceed
    further with our calculation');

    gamma_opt_mag=input('Enter the magnitude of gamma_opt ');
    gamma_opt_phase=input('Enter the phase of gamma_opt in degrees ');

    F_min=input('Enter the value of Fmin in dB ');

    rn=input('Enter Rn/50 ');

    % Calculating gamma_s and gamma_l
    gamma_s=gamma_opt_mag*exp(j*deg2rad(gamma_opt_phase));
    gamma_opt=gamma_s;
    gamma_l=conj(s(2,2)+(s(2,1)*s(1,2)*gamma_s)/(1-
                   (s(1,1)*gamma_s))));
% Calculating the gain of Minimum noise amplifier
G_T_MNA = (((1-(abs(gamma_s))^2)/((abs(1-s(1,1)*gamma_s))^2))*(abs(s(2,1)))^2)/(1-(abs(gamma_l))^2));
G_T_MNA_dB=10*log10(G_T_MNA);

X1 = ['G_T for minimum noise amplifier is equal to ' num2str(G_T_MNA_dB) 'dB '];
disp(X1);

% Calculating the gain of Maximum gain amplifier
G_T_MGA = ((1/(1-(s11_mag)^2))*(s21_mag)^2)/(1-(s22_mag)^2));
G_T_MGA_dB=10*log10(G_T_MGA);

X2 = ['G_T for maximum gain amplifier is equal to ' num2str(G_T_MGA_dB) 'dB '];
disp(X2);

% Calculating the noise figure of the cascaded amplifier
F1 = 10^(F_min/10);
gamma_s1=conj(s(1,1));
N=((abs(gamma_s1-gamma_opt))^2)/(1-(abs(gamma_s1))^2);
F2 = F1 + (((4*rn*N)/(abs(1+gamma_opt)^2)));
F_cascade=10*log10( F1 + (F2-1)/(G_T_MNA) + (F2-1)/(G_T_MNA*G_T_MGA));

X3 = ['The total noise figure of the final cascaded amplifier is equal to ' num2str(F_cascade) 'dB '];
disp(X3);
else
display('Transistor is conditionally stable')
end

Output:
Enter the magnitude of s11 0.38
Enter the phase of s11 in degrees -164.21
Enter the magnitude of s12 0.166
Enter the phase of s12 in degrees 24.33
Enter the magnitude of s21 2.904
Enter the phase of s21 in degrees 40.360
Enter the magnitude of s22 0.206
Enter the phase of s22 in degrees -118.23
K =

1.0145

magnitude of delta = 0.40613
phase of delta = -117.7706
Transistor is unconditionally stable, we can proceed further with our calculation
Enter the magnitude of gamma_opt 0.64
Enter the phase of gamma_opt in degrees 45.9
Enter the value of Fmin in dB 0.45
Enter Rn/50 0.3
G_T for minimum noise amplifier is equal to 5.9894dB
G_T for maximum gain amplifier is equal to 10.1255dB
The total noise figure of the final cascaded amplifier is equal to 1.0432dB
% Program to calculate the component values of the matching network
clear all; clc;
Z= input('Enter the value of characteristic impedance Zo \n');
f= input('Enter the frequency in GHz \n');
w= 2*pi*f;
disp('1 for series L');
disp('2 for shunt L');
disp('3 for series C');
disp('4 for shunt C');
I = input('Enter the component from the above list \n');

if (I==1)
    Xs = input('Enter the value Xs = '); 
    L = Xs*Z/(w);
    X1 = ['L = ' num2str(L) 'nH '];
    disp(X1);
elseif (I==2)
    Bp = input('Enter the value Bp = '); 
    L = Z/(w*Bp);
    X1 = ['L = ' num2str(L) 'nH '];
    disp(X1);
elseif (I==3)
    Xs = input('Enter the value of Xs = '); 
    C = 1000/(w*Z*Xs);
    X1 = ['C = ' num2str(C) 'pF '];
    disp(X1);
elseif (I==4)
    Bp = input('Enter the value of Bp = '); 
    C = 1000*Bp/(w*Z);
    X1 = ['C = ' num2str(C) 'pF '];
    disp(X1);
end