FULL CHIP MODELING FOR PREDICTIVE SIMULATION OF CHARGED DEVICE MODEL ELECTROSTATIC DISCHARGE EVENTS

BY

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THESIS

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ABSTRACT

With downscaling of device dimensions in integrated circuits (ICs), the risk of circuit failure due to electrostatic discharge (ESD) is increasing. In particular, the increased usage of automated handlers is causing charged device model (CDM) ESD induced failures to become more prominent. Gate oxide failure is the primary signature of CDM ESD. During CDM, the IC is the source as well as the path for the static charge. Therefore, it is important to include the circuit elements representing the package, ESD circuits and the silicon substrate of the packaged ICs. Power domain crossing circuits, also known as internal I/Os, are susceptible to gate oxide damage during CDM events. In this thesis, circuit-level simulations of internal I/O circuits are used to elucidate the roles of the package, power clamp placement, anti-parallel diode placement and decoupling capacitors in determining the amount of stress at the internal I/O circuits. This thesis will also provide design recommendations for preventing CDM failures in the internal I/O circuits.

To My Parents

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Chapter 1. INTRODUCTION

Electrostatic discharge (ESD) is the transfer of static charges between objects at different electric potentials [1]. Static charges are generated due to tribo-electric charging, ionic charging, direct charging or field-induced charging [2]. Discharge of static charges into or out of integrated circuits (ICs) can damage the internal circuits and render them unusable or degrade their performance. As the physical dimensions of the devices in the ICs are scaled down to increase the operating speed and decrease the area, the devices are becoming increasingly susceptible to the damage due to ESD events. Therefore, a few samples of the ICs are tested in the laboratory for ESD robustness before delivering the ICs to the customers. These tests are called ESD tests. Various models are used simulate the ESD events that the IC may experience in the real environment. The human body model (HBM) [3], machine model (MM) [4] and charged device model (CDM) [5] are the three component level ESD test models that are used by the IC vendors. As the automated handling of ICs increases, CDM is becoming the most relevant of these three tests today. Two types of CDM tests are used in the industry: socketed CDM (SCDM) and field-induced CDM (FICDM). The work presented in this thesis is related to FICDM. This model is used since it is a better representation of CDM events in the real environment [6].

1.1. Charged Device Model

During a FICDM test, a packaged chip, called a device under test (DUT), is placed upside-down on a charge plate as shown in Figure 1.1. The charge plate potential is raised to a predetermined pre-charge voltage and then a pogo pin, which is attached to a ground plate, is lowered until it makes contact with a pin of the DUT. Charge flows through the pogo pin to the

DUT in order to support the potential difference between the grounded component and the field charge plate. The charge flows through the lowest impedance paths that lie between the "zapped pin" and the charge storage sites throughout the component. This results in a high current stress as shown in Figure 1.2.

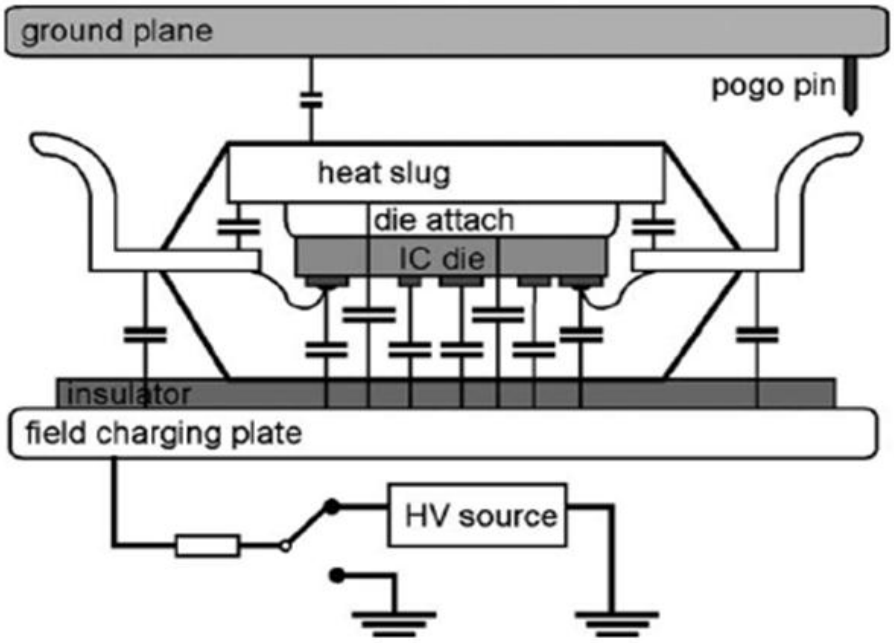

Figure 1.1 Packaged component placed upside down between the charge plate and ground plate of an FICDM tester is shown. (Drawing taken from M. Etherton et al., "Study of CDM Specific Effects for a Smart Power Input Protection Structure," EOS/ESD Symposium, 2004.)

The pogo pin is then raised, and the pre-charge voltage is reduced to 0 V. A stress of negative polarity can then be applied by bringing the pogo pin down to make contact with the device pin. The peak current depends upon the amount of charge stored in the IC and the impedance of the discharge path. The amount of charge is determined by the total capacitance formed between the metallic parts of the IC and the charge plate. The pogo pin inductance, the resistance of the spark between the pogo pin and DUT, and the impedance of the discharge path on the chip determine the peak current for a given amount of charge storage. The DUT is

characterized before and after the CDM stress. The CDM robustness of the DUT is defined as the highest pre-charge voltage that can be used to stress all the pins of the DUT without causing a failure.

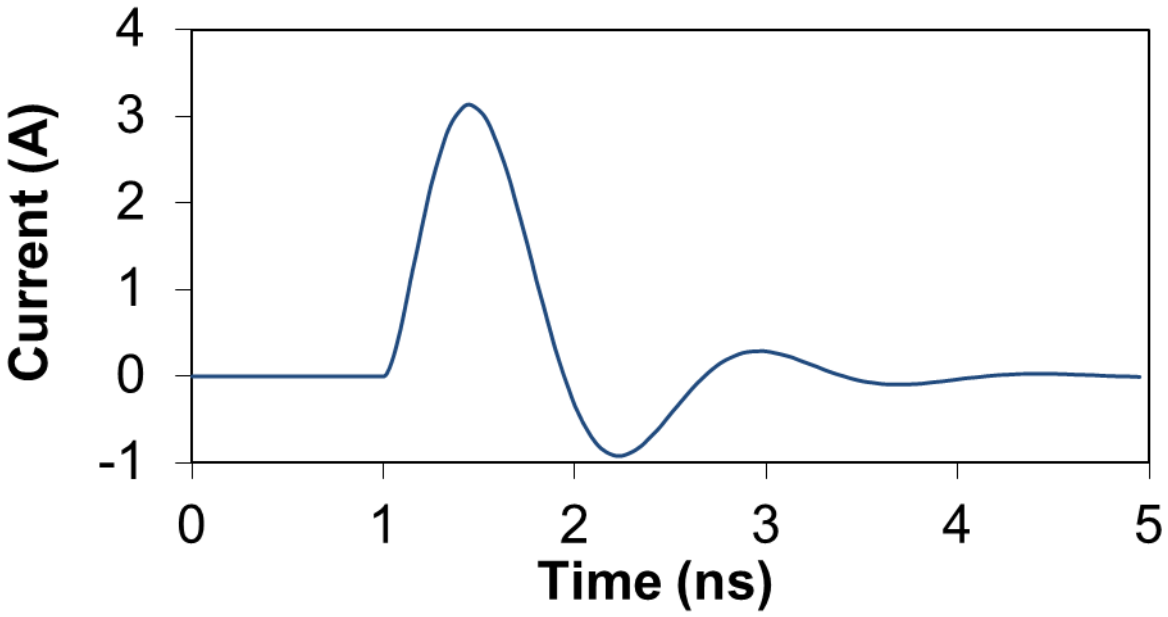

Figure 1.2 Typical simulated waveform of the CDM discharge current through the pogo pin; CDM simulation of 500 V was carried out on a quad flat package IC test case.

1.2. Motivation for CDM Simulation of Circuits

The CDM test is carried out on a packaged IC. Finding the ESD related failures after fabricating and packaging an IC costs much more than finding the same issues earlier in the design cycle, and fixing them before fabrication. Hence, it is desirable to detect the ESD weakness in the ICs and fix them before fabricating the ICs. In the HBM and the MM test, the peak current for a given pre-charge voltage is known beforehand. Designers can design and place the ESD protection circuits to minimize the stress on the circuits for each stress mode. In contrast, in the CDM test, the peak current varies from design to design, depending on the size of the die and of the package. Also, unlike in the other component level tests, during the CDM test, the path

of discharge is not well understood. The CDM discharge current has fast rise time, of the order of a few hundreds of pico seconds. The rise time dictates that the transient effects have to be included while analyzing the circuit reliability. Thus, transient circuit simulations are needed to study the robustness of circuits. Circuit simulations also allow designers to measure voltages and currents at the internal nodes, a method which is not easy to implement while testing packaged ICs.

1.3. Thesis Overview and Organization

This work presents a simulation model that can be used to predict full chip CDM failures . Simulation of CDM events in integrated circuits requires modeling the plural charge storage locations and discharge paths. The charge is stored in various metallic parts of the IC, such as the conducting parts of the package and on-chip interconnect. The discharge path for each storage site may be different. In order to simulate the discharge current waveform, the netlist must include elements representing the package, ESD circuits and substrate [7],[8]. If full-chip modeling is undertaken, one can also simulate the CDM waveforms at power domain crossing circuits, known as internal I/Os. These circuits may be susceptible to gate oxide damage during CDM events [9],[10]. Previous work on full-chip CDM simulation to study the power domain crossing circuits did not include the substrate model [11]. This thesis shows that the substrate resistivity plays an important role in determining the stress at the power domain crossing circuits.

Worley [10] introduced the concept of a structured cross-domain signal interface in which anti-parallel diodes (APDs, i.e. back-to-back diodes) and power clamps are placed near the driver and the receiver of the internal I/O. In practice, this requires the internal I/O to be placed close to the pad ring because this is the preferred location for placing a power clamp due to its large size. This impacts the chip’s floorplan and limits the blocks between which signals may be passed.

This work uses circuit simulation to explore whether an internal I/O may safely be located far from the pad ring and the primary ESD protection, if the primary protection is augmented by small APDs and decoupling capacitors placed near the internal I/O. In [10], APDs are also used between power rails, a strategy not preferred by designers due to a power sequencing problem. In this work, protection devices are therefore not placed directly between different power busses. Simulation results compare favorably with measurements obtained on a CDM testchip; this provides confidence in the results of the predictive simulations.

Chapter 2 provides an overview of the simulation model for CDM and its individual components: the package, substrate and on-chip circuit models. Chapter 3 presents the test cases used for the research and the simulation results. Chapter 4 provides the comparison between the simulation results and the measurement data for one of the test cases. Last, a summary of the conclusions and some ideas for future work are presented in Chapter 5.

Chapter 2. MODELING METHODOLOGY

Circuit simulations are only as good as the models used in the simulations. The presence of an accurate charge storage model is an important factor in determining the accuracy of the CDM simulation results. Once the charge storage locations are known for an IC, one can proceed to model all the relevant paths of discharge. A capacitive model is used to model the charge storage locations. Chapter 2.1 presents the charge storage model and an overview of the schematic model used in the simulations.

2.1. Package Model

2.1.1. Capacitive Model of Charge Storage

The amount of charge transferred during a CDM event depends on the capacitors formed by the metallic parts of the DUT with the plates of the CDM tester. The capacitance between the plates of the tester also contributes to the amount of charge storage. A lumped three-capacitor model [12] is sufficient to calculate the total amount of charge; subsequently, the peak current may be found by roughly estimating the series impedance of the discharge paths [13]. Although this method for estimating the peak current is sufficient to predict the reliability of I/O circuits, distributed modeling of charge storage is needed to estimate the stress on the internal circuitry, particularly the power domain crossing circuits. Therefore, a distributed capacitance model of the part is needed.

In this study, the various capacitances between the DUT and the tester plates were calculated using CSURF, a 3-D capacitance modeling tool [14]. The actual dimensions of the package and the die were drawn using the graphical user interface of CSURF. The package dielectric constant was entered and capacitances were extracted. The capacitance between the on-

chip power/ground interconnect metal and the charge plate was estimated by extracting the area of the interconnect metal using a layout extraction tool. At each metal level, the area of the metal exposed to the charge plate was extracted. A customized layout extraction rule set was written to perform the extraction.

This thesis presents the model of a cavity-up quad flat package (QFP). The QFP is placed in a dead-bug position on an FICDM charge plate as shown in Figure 2.1.

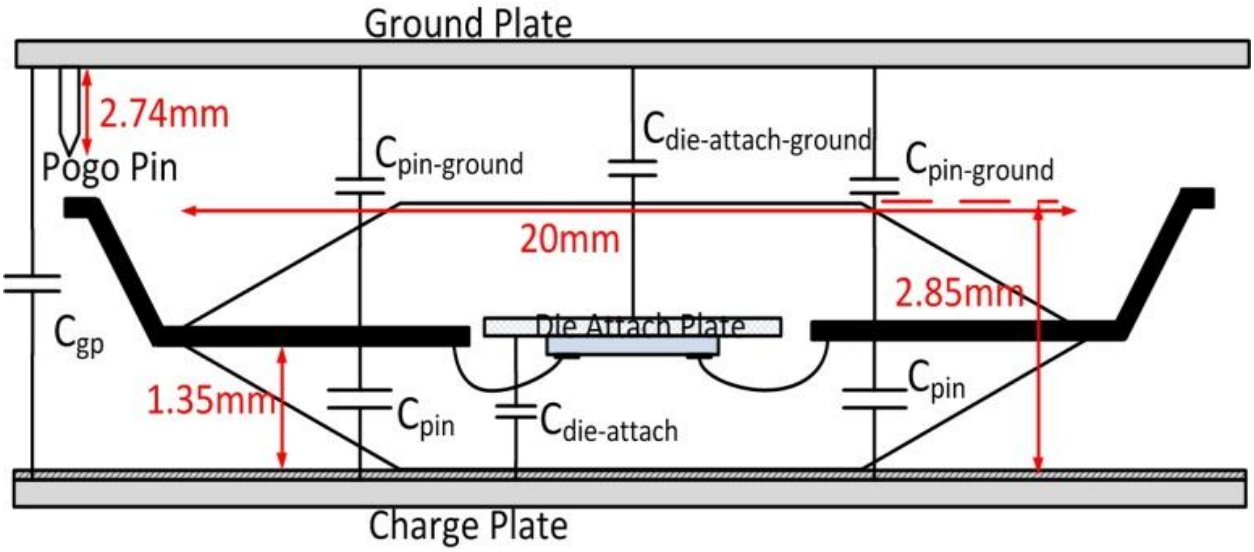

Figure 2.1 QFP package that was modeled in this work. Important capacitances formed by the parts of the components with the charge plate and ground plate of the FICDM tester are shown.

In a QFP with a large number of pins or long pin leads, package pins are the primary charge storage locations. Packages that have a small die attach plate in comparison to the package size can have long pin leads. This can lead to a large pin capacitance. For very thin packages, the bondpads and the on-die interconnect will be closer to the charge plate and the capacitance formed by them with the charge plate may become significant. However, for a small die in a thicker package, the capacitances formed by the interconnect metal and the bondpads can be negligibly small. For packages with a metal heat sink, the capacitance between the heat sink and the charge plate will be significant, and the connection of the heat sink to the rest of the on-die

elements will decide the path of discharge for the charges stored in the heat sink. For example, the heat sink could be down-bonded to a ground pin of a particular power domain. In that case, zapping a pin belonging to another power domain will lead to a higher current flowing from the power domain connected to the heat sink to the zapped power domain, compared to that in the case of zapping a pin down-bonded to the heat sink.

2.1.2. Full Chip Schematic Model

Once a capacitive model is obtained, a schematic representation of the CDM simulation model for a QFP package can be drawn as shown in Figure 2.2. Only one package pin is shown in the figure. Parasitic resistance, inductance and mutual capacitance of the package pins can be obtained from the package data sheets. The parasitic resistance and the inductance of the bondwires can be calculated once the die is packaged and bondwire lengths are known. Alternatively, these values may be estimated with reasonable accuracy before packaging, if the die size and the package size are known.

The charge stored in the $C_{die\text{-}attach}$ has to flow through the substrate, into the on-chip ground bus through the substrate contacts. A substrate model is necessary to understand the flow of charges through the substrate and its impact on the on-chip circuits. The substrate model used in this study is presented in Chapter 2.2. Charge stored in all the pins other than the zapped pin has to flow through the on-chip ESD protection circuit and the power and the ground busses. This necessitates that the on-chip ESD protection network and the power and the ground interconnect be modeled for the simulation. Chapter 2.3 presents the on-chip circuit model used in this work.

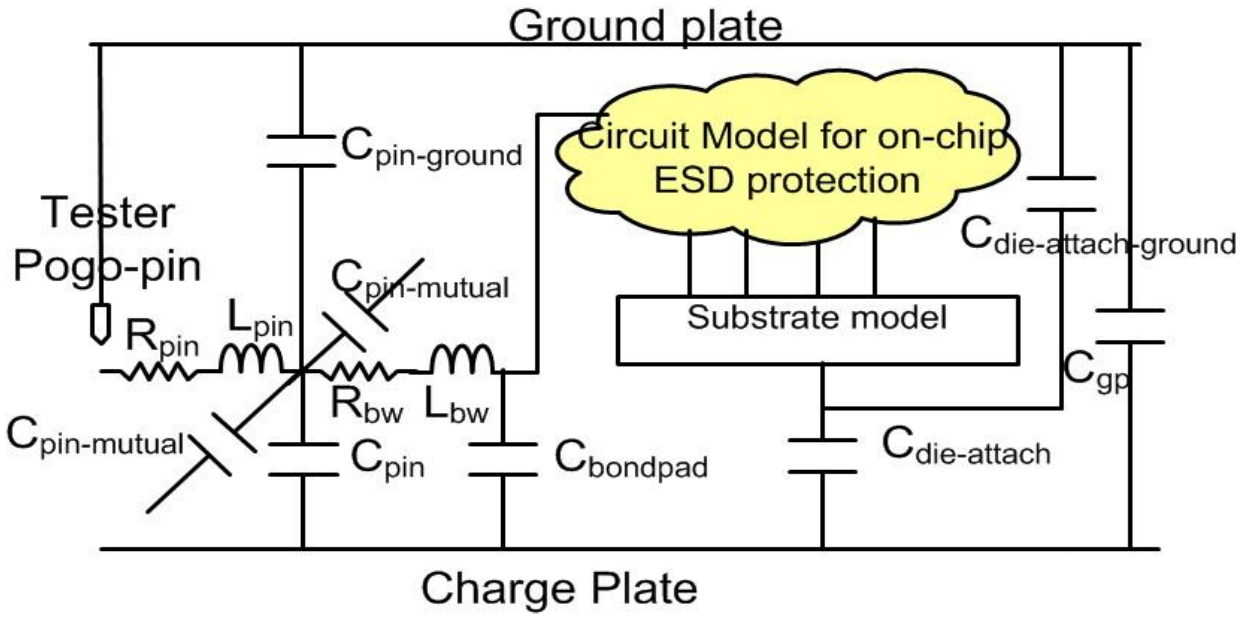

Figure 2.2 High-level representation of CDM simulation model showing interconnection of substrate, package and on-chip models.

2.2. Substrate Model

The charge stored on $C_{die\text{-}attach}$ flows through the substrate, into the on-chip ground bus through the substrate contacts. To understand the flow of charge through the substrate and its impact on the on-chip circuitry, it is important to model the substrate. The chip substrate was divided into a 3-D grid of boxes, each represented by six resistors, as suggested in [7]. A script was written to create the substrate resistor network, given the substrate size and the grid size. The grid size and the chip size determine the number of nodes in the substrate model. The backside of the substrate is connected to $C_{die\text{-}attach}$, and the top side of the substrate is connected to the substrate contacts of VSS busses as shown in Figure 2.3.

Figure 2.3 corresponds to the particular case in which the die attach plate is connected to the die substrate using conductive glue (silver filled epoxy). If, instead, the die is attached using an insulating glue, the $C_{die\text{-}attach}$ should be distributed across the bottom-most grid boxes of the substrate in the x-y plane.

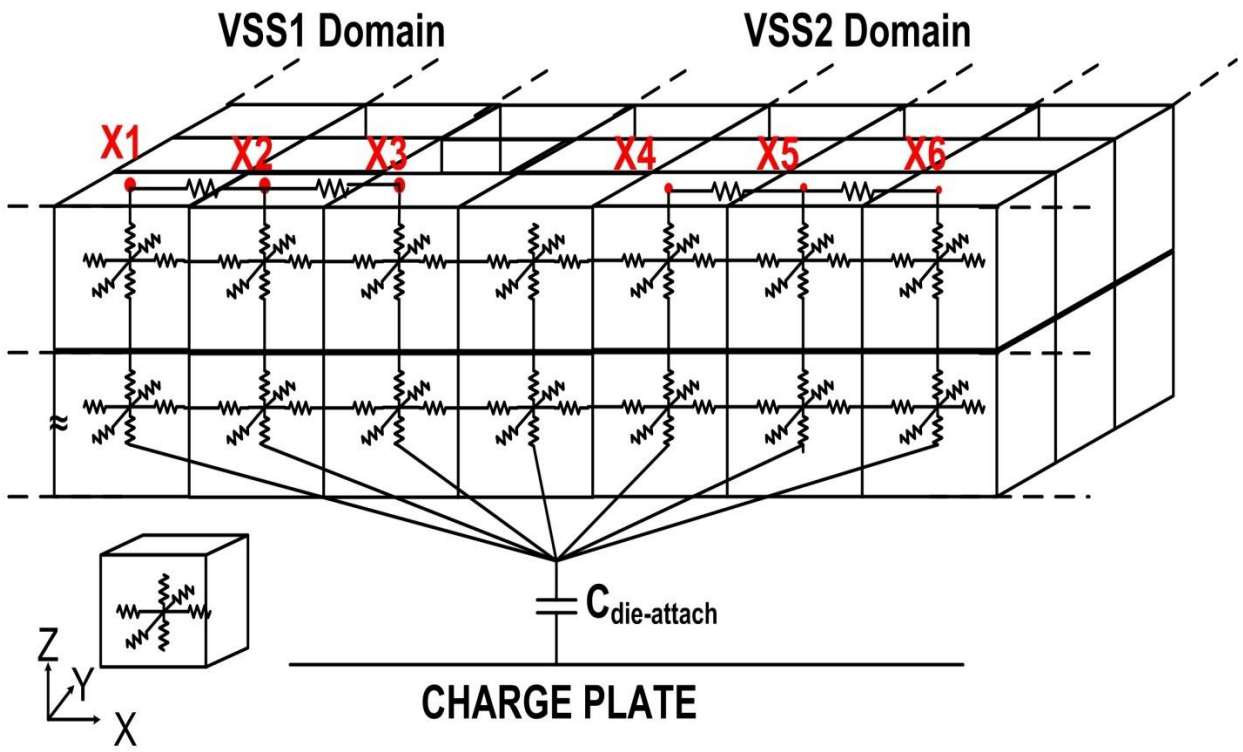

Figure 2.3 3-D substrate resistor grid. X1, X2 … Xn are the substrate contacts. The resistors in the top row model the Vss busses. A sample grid-box with 6 resistors is shown on the lower left corner.

Capacitive coupling is stronger along the periphery of the substrate than in the center due to fringing fields, and thus the capacitors connected to the outermost grid boxes would be larger than those in the interior. The top-side of the substrate is connected to the substrate contacts. In this work, substrate contacts were automatically extracted from the layout and a reduction algorithm was used to merge the substrate contacts that were in the same grid box of the substrate model. The locations of the substrate contacts were extracted using a customized layout extraction rule set. A layout extraction tool called Calibre [15] was used as the extraction engine. The rule set was written in Calibre's native extraction language. The locations of the substrate contacts were written into a text file. A pattern extraction and report language (PERL) [16] script was written to read the locations of the layout extracted substrate contacts from the file. The script then identified the top-most grid box of the substrate model that contained each of the substrate

contacts. Multiple substrate contacts contained within the same grid box were connected together. The output of the script is a netlist that connects the substrate contacts to the resistors in the Z-direction of the top-most grid boxes of the substrate model.

2.3. On-Chip Circuit Model

The circuit-level model is connected to the package and the substrate models. The substrate contacts provide connection to the ground busses. The bondpads provide connection to the package model. The circuit-level model contains ESD protection devices at each pad, parasitic resistance of power and the ground busses, and decoupling capacitors between the power and the ground busses. In this work, ESD protection includes dual diodes at the signal pads and active clamps as the power clamps [17]. The circuit-level model should also contain any core circuitry of interest, e.g. internal I/O. The capacitance between the interconnect metal and the charge plate, if significant, should be included in the netlist.

Figure 2.4 illustrates an internal I/O studied in this work. One can observe the connections between the circuit-level model, the package model and the substrate model. The driver is in the VDD1 domain and the receiver is in the VDD2 domain. Note that the respective grounds, VSS1 and VSS2, are connected by anti-parallel diodes (APDs) in the pad ring. The transistors in the internal I/O circuits have thin gate oxides which can conduct significant current under CDM conditions; therefore, Fowler-Nordheim gate tunneling current models [18] were used in the simulations.

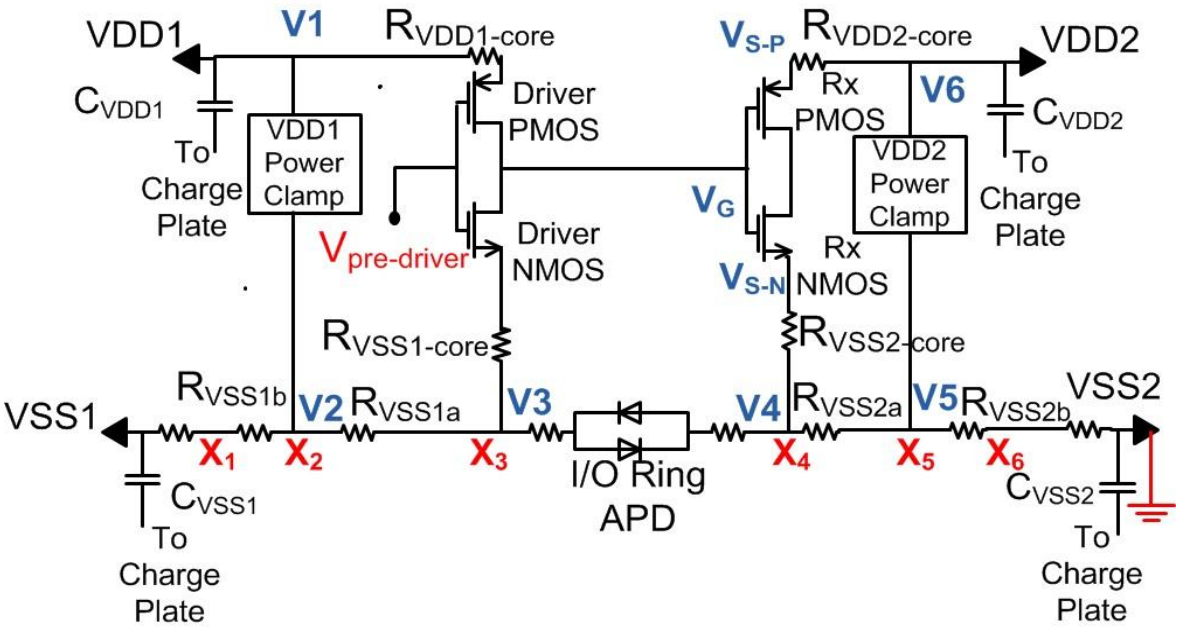

Figure 2.4 Internal I/O circuit. Driver in VDD1 domain; receiver in VDD2 domain. The substrate contacts (X1, X2, etc.) are shown. Refer to Figure 2.3 for substrate connections. C_{VDD1}, etc., are pin capacitors.

To accurately model the gate tunneling current, a voltage controlled current source was connected in parallel with the gate-source of the receiver transistors, Rx NMOS and Rx PMOS. The gate current can be modeled as

$$J_G = Ae^{-BT_{ox}/V_G} \tag{2.1}$$

J_G is the gate tunneling current density. A and B are the model fitting parameters. The gate leakage currents for the NMOS and the PMOS thin oxide devices were measured under the transmission line pulsing (TLP) [19] stress, and the mathematical model in Eq. 2.1 was fitted using MATLAB [20]. After obtaining the appropriate parameters for the measured data, the equation was implemented in verilog-A [21] script and the resulting verilog-A model was included in the Spectre [22] netlist used for the simulations.

During any CDM event in which the rail clamps turn on, the digital logic will be activated. The input to the driver may be pulled low or high depending upon the logic state of the pre-driver or the coupling of the signal line with the power or the ground bus. When the driver PMOS is ON, the potential at the gate of the receiver is approximately equal to V1, whereas, when the driver NMOS is ON, the potential at the gate of the receiver is approximately equal to V3. Since V1 is greater than V3, the stress at the receiver gates will be higher when the driver PMOS is ON. Thus, to simulate the worst case stress for the receiver, it was assumed that the input to the driver is pulled low. To reduce the simulation runtime, other functional circuits were not included in the netlist.

Using the methodology described so far, a complete simulation netlist was created for two testcases in 90 nm technology. The testcases and the simulation results are described in Chapter 3.

Chapter 3. PREDICTIVE CDM SIMULATION OF POWER DOMAIN CROSSING CIRCUITS

3.1. Description of Test Cases

Simulation studies were conducted on two 90 nm test cases: Test Case A and Test Case B. Test Case A is a small chip that is used only for predictive (i.e., "what if") simulations. In Test Case A, a 500 µm x 500 µm die is modeled as being inside a 34-pin QFP package. The package height is 2.85 mm and its other dimensions are 20 mm x 16 mm. Its die attach plate is 6 mm x 6 mm. A capacitance model was extracted as described in Section 2.1, and the values are tabulated in Table 3.1. For the 34-pin package, the total pin capacitance amounts to 3.74 pF, which is much larger than the next largest capacitor, $C_{die\text{-}attach}$. The bondpad and the interconnect capacitance were found to be very small and were not included in the simulation netlist. Test Case A uses a high resistivity substrate (ρ = 15 Ω-cm), unless otherwise noted.

Table 3.1 Values of capacitors extracted for the QFP package using 3-D capacitance extraction tool. Refer to Figure 2.1 for component names.

Component Name	Value	Component Name	Value
C_{pin}	0.11pF	$C_{die\text{-}attach}$	1.33pF
$C_{pin\text{-}ground}$	60fF	$C_{die\text{-}attach\text{-}ground}$	160fF
C_{gp}	20pF	$C_{bondpad}$	0.08fF

The pad assignments for Test Case A are illustrated in Figure 3.1. The power and ground busses for each domain run along the periphery of the chip. The VSS1 bus is continuous while the VSS2 bus runs only in the VDD2 domain section of the I/O ring. The parasitic resistance grid

of the core power bus and that of the core ground bus were created using a script and are shown in Figure 3.1. The substrate contacts were created with a regular grid and are shown as red dots in the figure. Note that the VDD1 domain is larger than the VDD2 domain. The contents of each pad cell are shown in Figure 3.2. A decoupling capacitance of 10 pF was placed in each pad cell. The bus resistance of each power/ground bus is 0.25 Ω per pad cell. In the CDM simulations of Test Case A, the charge plate was brought to 300 V and then a VSS2 pin was grounded by the pogo pin. This study focuses on the stress induced at the internal I/O illustrated in Figure 2.4.

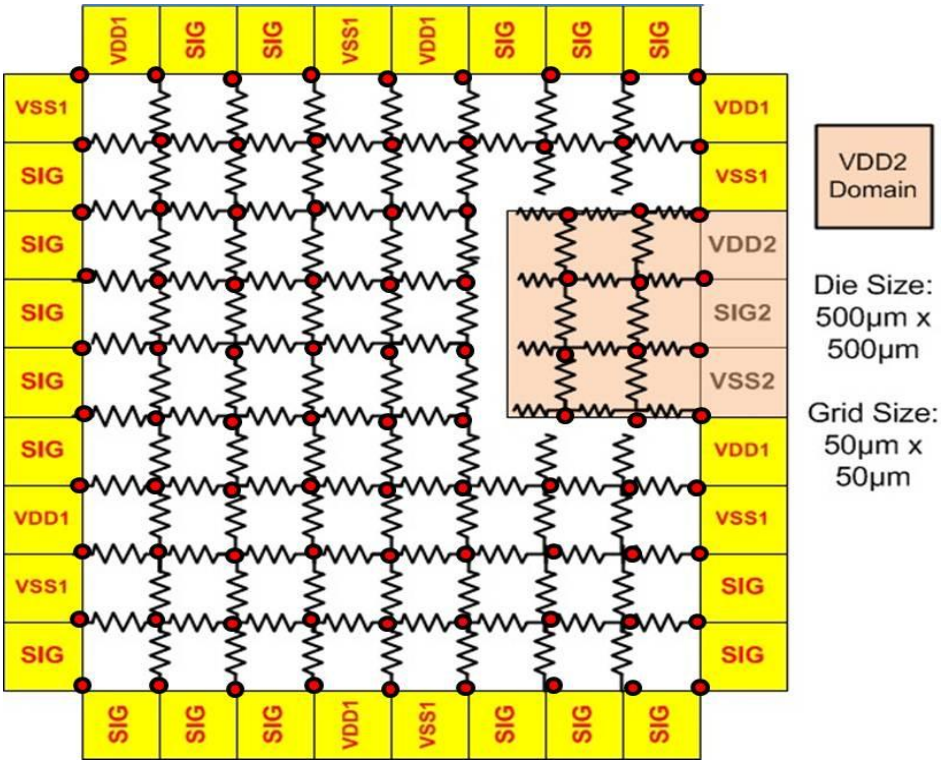

Figure 3.1 Pad arrangement for Test Case A. VDD1/VSS1 domain is larger with higher pin count and larger number of substrate contacts. Ground bus model for the core is also shown.

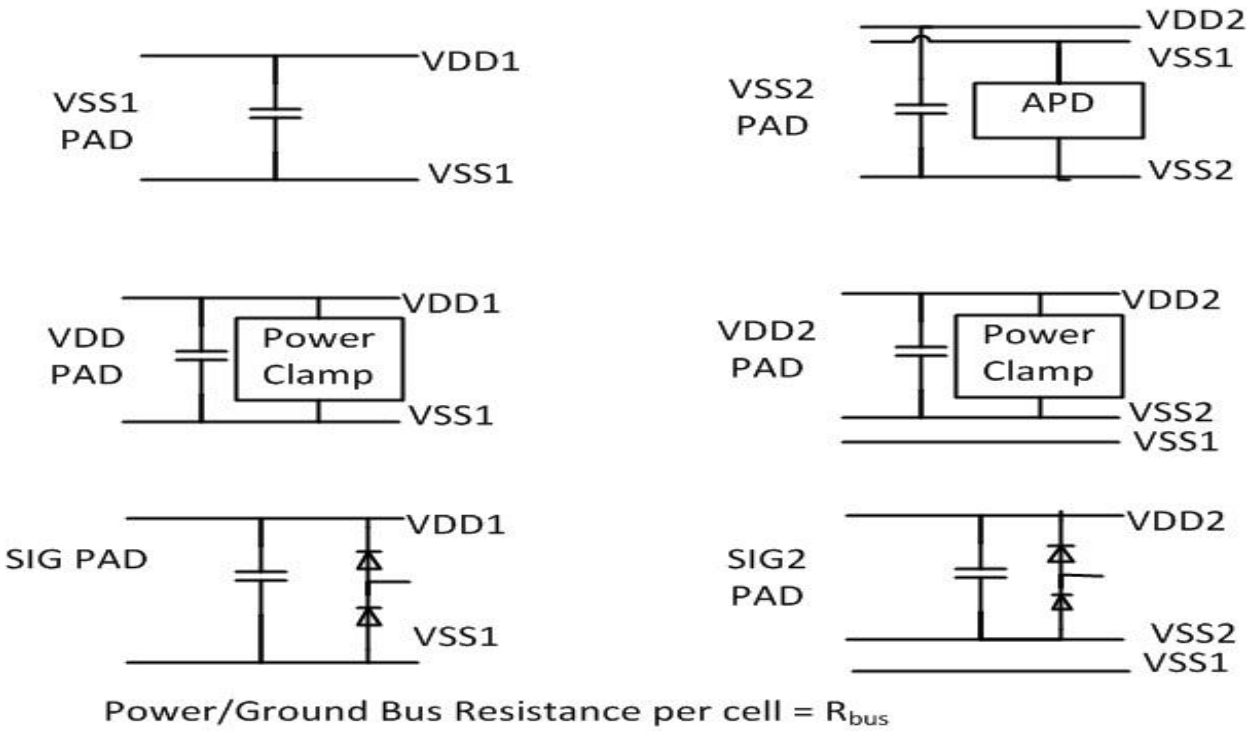

Figure 3.2 Block diagram of each pad cell used in the pad ring described in Figure 3.1.

Test Case B is a CDM test chip that was fabricated and tested. This chip was packaged in the 100-pin QFP package described in Chapter 2. The total pin capacitance for this package is large (11 pF). The die size is 2 mm x 4 mm. The test chip was built on a high resistivity substrate (ρ = 15 Ω-cm). The test chip has 64 pads and contains multiple internal I/Os that are similar to the one illustrated in Figure 2.4. The two domains, VDD1 and VDD2, are of the same size. In Chapter 4 of this thesis, the simulation results for Test Case B are compared with data obtained using capacitively coupled TLP (cc-TLP) [23] and very fast TLP (VFTLP) [24] testers.

3.2. Simulation Results and Discussions

The simulation results for Test Case A will be presented in this section. Cadence's Spectre [22] was used as the simulation engine. As previously stated, the simulations are for a 300 V CDM event with respect to a VSS2 pin. The currents through the APD and the grounded pin are

plotted in Figure 3.3. A large fraction of the total current flows through the APD from VSS1 to VSS2. This is because most of the charge is stored in the pin capacitors and most of the pins are in the VDD1 domain. The primary path for ESD current from the VDD1 to the VDD2 domain is through the VSS busses and the APD.

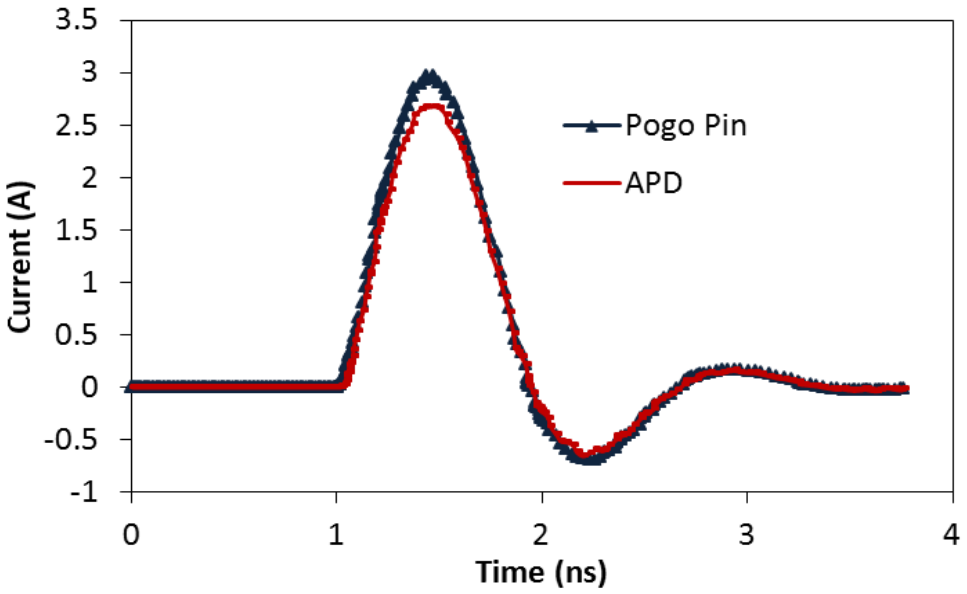

Figure 3.3 Simulated current waveforms at the grounded pin and at the APD. Current flows through the APD from VSS1 to VSS2.

3.2.1. Effect of Substrate Resistivity

Simulations were performed for two cases: ρ_{sub} = 15 Ω-cm (default case) and ρ_{sub} = 0.02 Ω-cm. In Figure 3.4, the peak V_{gs} of the receiver NMOS and that of PMOS are plotted as a function of the per cell power/ground bus resistance in the pad ring. Despite the internal I/O being off-path for the ESD current, large potential differences appear across the gate oxides of the receiver transistors, especially when a high-resistivity substrate is used. During this CDM event, the NMOS is biased in inversion and the PMOS is biased in accumulation. The stress can be measured in terms of the voltage drop across the oxide, which is V_{gs} in inversion and V_{gb} in

accumulation. However, since the source and body nodes of these transistors are tied together, there is no need to distinguish between V_{gs} and V_{gb}.

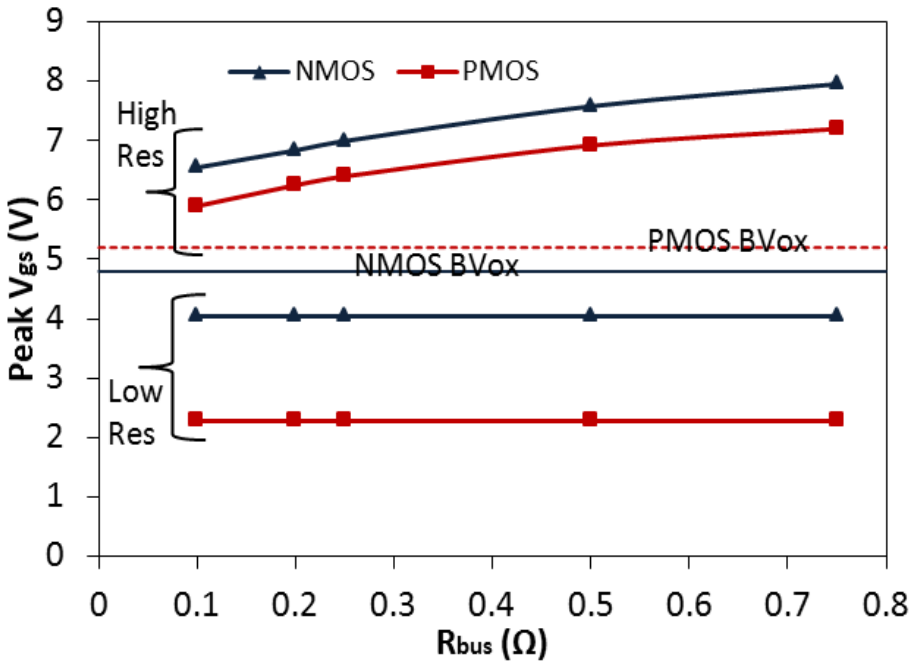

Figure 3.4 V_{gs} of the receiver transistors for low and high resistivity substrates.

Using the node voltages previously introduced in Figure 2.4, the voltage stress across the receiver NMOS can be written as

$$V_{gs-nmos} = V_G - V_{S-N} \cong V1 - V4 \tag{3.1}$$

$$V1 - V4 = (V1 - V2) + (V2 - V3) + (V3 - V4) \tag{3.2}$$

The right-most quantity in Eq. (3.1) is approximately equal to $V_{gs\text{-}nmos}$ since the ESD current primarily flows through the pad ring and there is little voltage drop in the core busses, e.g. there was a negligible potential drop through $R_{VSS2\text{-}core}$ or $R_{VDD1\text{-}core}$. In Eq. (3.2), the quantity (V1-V2) is the voltage drop across the power clamp. V2-V3 is the voltage drop in the VSS1 bus between the power clamp and the APD. V3-V4 is the voltage drop across the APD.

Similarly the stress across the receiver PMOS can be written as

$$V_{gs-pmos} = V_G - V_{S-P} \cong V1 - V6 \tag{3.3}$$

$$V1 - V6 = V_{gs-nmos} + (V4 - V5) - (V6 - V5) \tag{3.4}$$

The quantity (V4-V5) is the voltage drop in the VSS2 bus between the point at which the receiver source is connected to the VSS2 bus in the I/O ring and the VDD2 power clamp. V6-V5 is the voltage drop between VDD2 and VSS2; this quantity is positive because current flows from VDD2 to VSS2 when a VSS2 pin is zapped.

Equation (3.4) explains why the receiver PMOS, not just the NMOS, is stressed when VSS2 pin is zapped. $V_{gs\text{-}pmos}$ may be higher or lower than $V_{gs\text{-}nmos}$ depending upon the relative values of (V4-V5) and (V6-V5). If the quantity (V6-V5) is larger, the voltage stress on the receiver PMOS oxide will be smaller than the stress on the NMOS oxide. However, in this test case, the VDD2 domain is small and the current flowing from VDD2 to VSS2 is small, leading to a very small voltage drop between VDD2 and VSS2. This leads to a significant voltage stress across the PMOS.

The oxide breakdown voltage of 90 nm thin oxide transistors was measured using a very fast transmission line pulsing (VFTLP) system with a pulse width of 10 ns. The oxide breakdown voltage for an NMOS in inversion was about 4.8 V, and the PMOS oxide breakdown voltage in accumulation region was about 5.2 V. The simulation results of Figure 3.4 indicate that oxide breakdown at the internal I/O is far more likely to occur when a high resistivity substrate is used rather than using a low resistivity substrate.

In order to simulate the case of a chip built on a low resistivity substrate (0.02 Ω-cm), the substrate model was replaced with a new resistance grid, appropriate for the lower resistivity

material. When a low resistivity substrate is used, the charge from $C_{die\text{-}attach}$ flows through the substrate directly to the grounded VSS2 bus. Although the charge stored on the pins in the VDD1 domain will enter the VSS1 bus, a large amount is diverted to the low resistivity substrate that is in parallel, thus bypassing the APD and the bus resistances; the reduced voltage drop across the VSS1 bus resistance and the APD yields a greatly reduced receiver V_{gs}. Therefore, CDM failures at internal I/O's are not expected to occur in ICs built on low-resistivity substrates.

3.2.2. Effect of Decoupling Capacitance

Increasing the amount of decoupling capacitance placed between the power and the ground busses reduces the stress on the internal I/O receiver gates, as shown in Figure 3.5. Increasing the decoupling capacitance reduces the voltage drop between VDD1 and VSS1, which is the quantity (V1-V2) in Eq. (3.1). The displacement current through the decoupling capacitors (I=C*dv/dt) is not negligible in the CDM timescale. The beneficial properties of decoupling capacitors were noted in [10]; this work highlights the quantitative importance of including them in CDM simulation models. Even though decoupling capacitance reduces the stress across the receiver gates, it may not be sufficient to protect the receiver gates from oxide breakdown. Therefore, additional protection strategies are considered in the following sections.

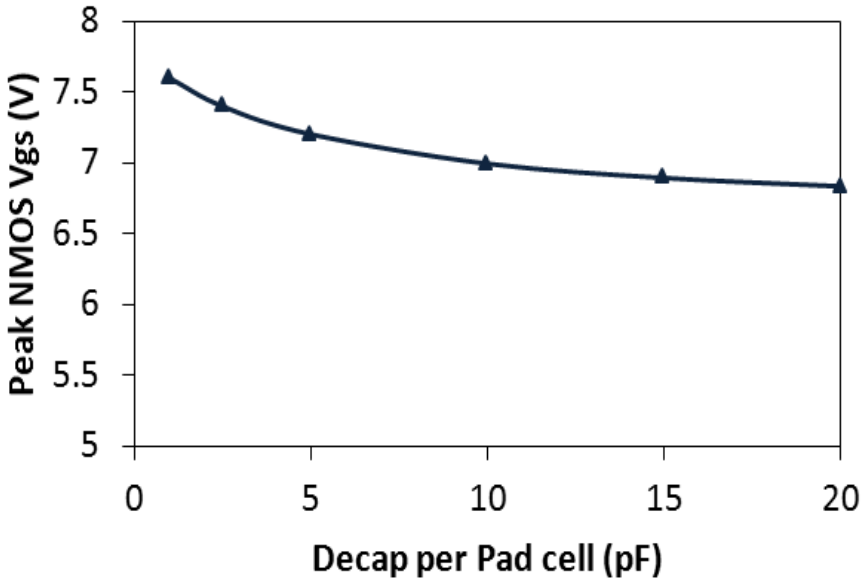

Figure 3.5 Effect of decoupling capacitance on the receiver NMOS V_{gs}.

3.2.3. Effect of Cross-Domain Power Clamp

A cross-domain power clamp may be used to reduce the stress at the internal I/Os, as shown in Figure 3.6. However, the cross-domain clamp is beneficial only if the VDD12 clamp shown in Figure 3.6 is placed near the VSS2 pad, such that R_{VDD12} and R_{VSS12} are minimized. A plot of PMOS and NMOS V_{gs} as a function of the sum of R_{VDD12} and R_{VSS12} is shown in Figure 3.7. Although the cross-domain clamps reduce the voltage stress across the receiver gate oxides, the voltage stress may not be low enough to protect the gate oxide. This depends upon the parasitic resistance of the power and the ground bus and the placement of the clamp. Designers who are concerned with noise isolation between the domains may not wish to use cross-domain power clamps.

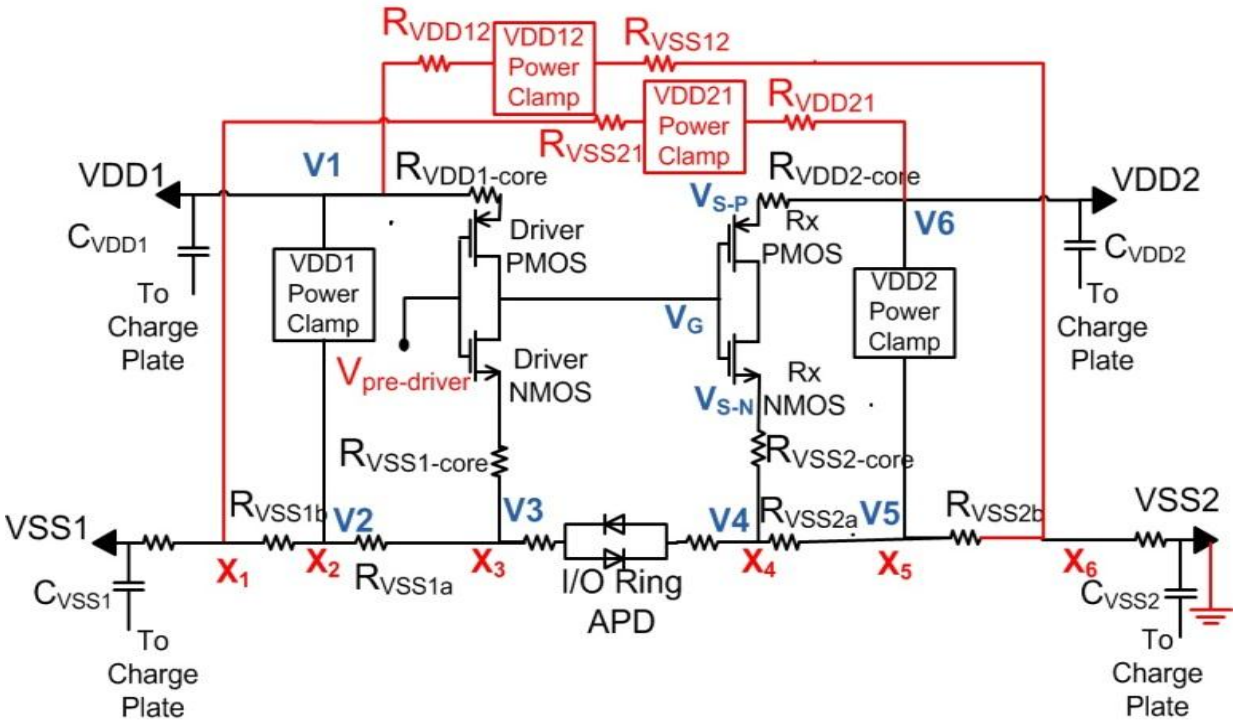

Figure 3.6 Internal I/O circuit with cross-domain power clamps between VDD1 and VSS2 and between VDD2 and VSS1.

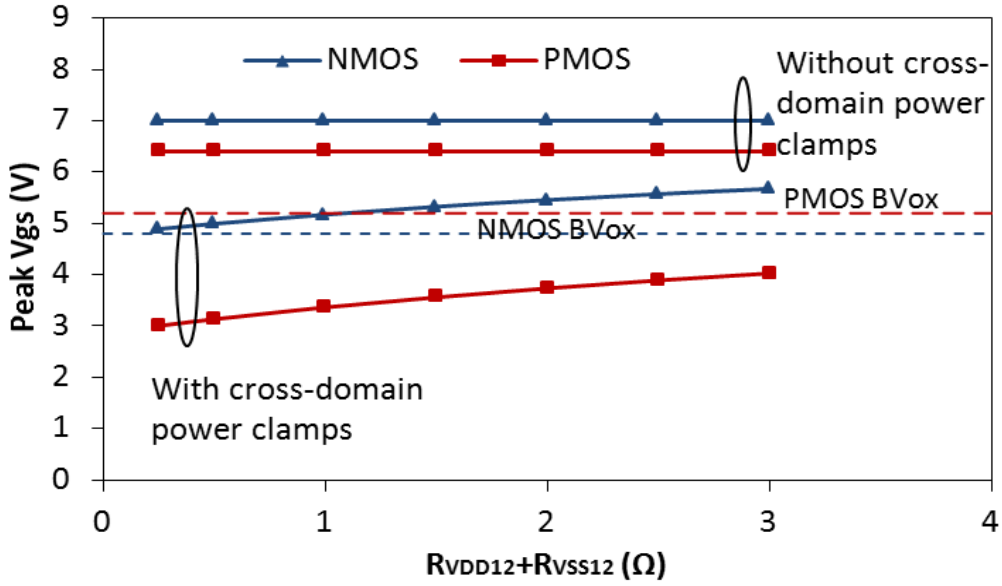

Figure 3.7 The cross-domain power clamps (VDD1-VSS2 and VDD2-VSS1) reduce V_{gs} of the receiver transistors. Resistance from the clamp to the respective pads is important.

3.2.4. Local APD

As shown in Figure 3.8, a small APD is placed between VSS1 and VSS2 in close proximity to the internal IO circuit in order to augment the APD in the I/O ring. R_{con} is the parasitic resistance of the ground bus connecting the local APD to the source of the driver NMOS or to the source of the receiver NMOS.

The local APD reduces the voltage drop between the VSS busses local to the driver and the receiver. The local APD carries very little current compared to the APDs in the I/O ring. As shown in Figure 3.9, the receiver V_{gs} is reduced significantly when using a local APD. R_{con} was set to 0.5 Ω in the simulations.

The data in Figure 3.9 show that the voltage stress can be further reduced by increasing the amount of decoupling capacitance in the vicinity of the driver and the receiver in addition to adding the local APD. Decoupling capacitors placed near the driver reduce the receiver NMOS V_{gs}. C_{local} placed near the driver reduces the local potential difference V1'–V3', while the local APD reduces the potential difference V3'–$V_{S\text{-}N}$, thus the two reduce the potential difference V1'–$V_{S\text{-}N}$. Decoupling capacitors placed near the receiver reduce the receiver PMOS V_{gs}. Specifically, C_{local} in the receiver domain (i.e. VDD2 domain) reduces the potential difference $V_{S\text{-}P} - V_{S\text{-}N}$, which reduces the potential difference V1–$V_{S\text{-}P}$.

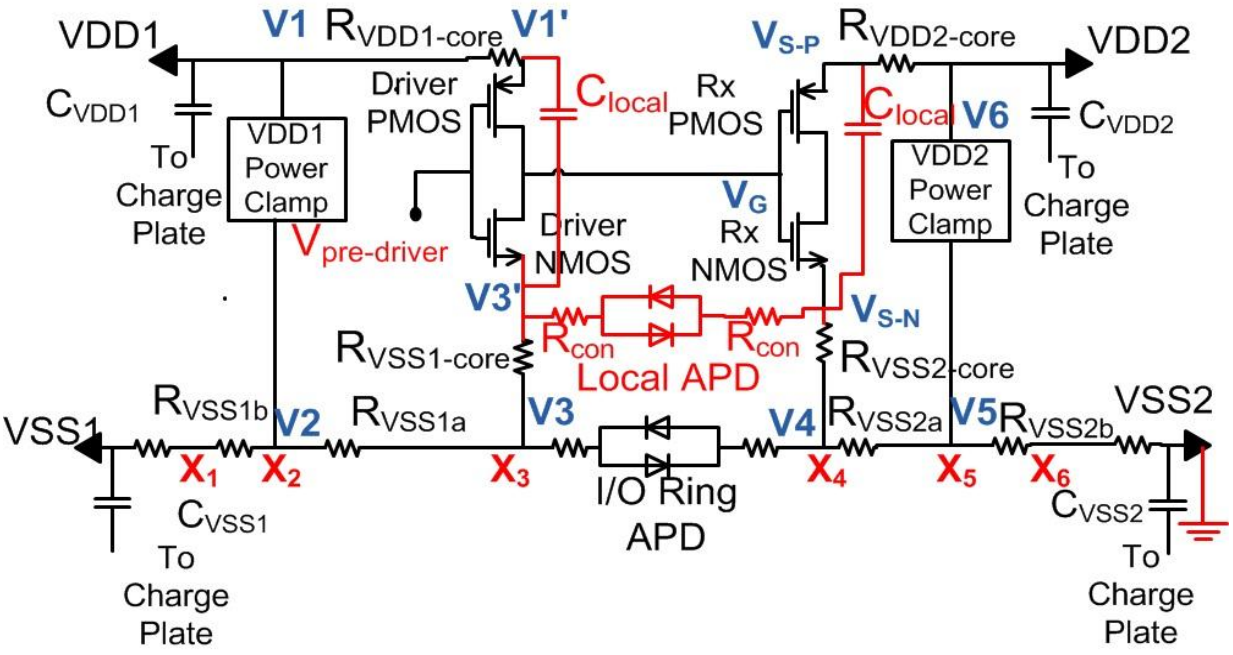

Figure 3.8 Internal I/O circuit with a local APD added close to the driver and the receiver, in addition to the APD in the I/O ring.

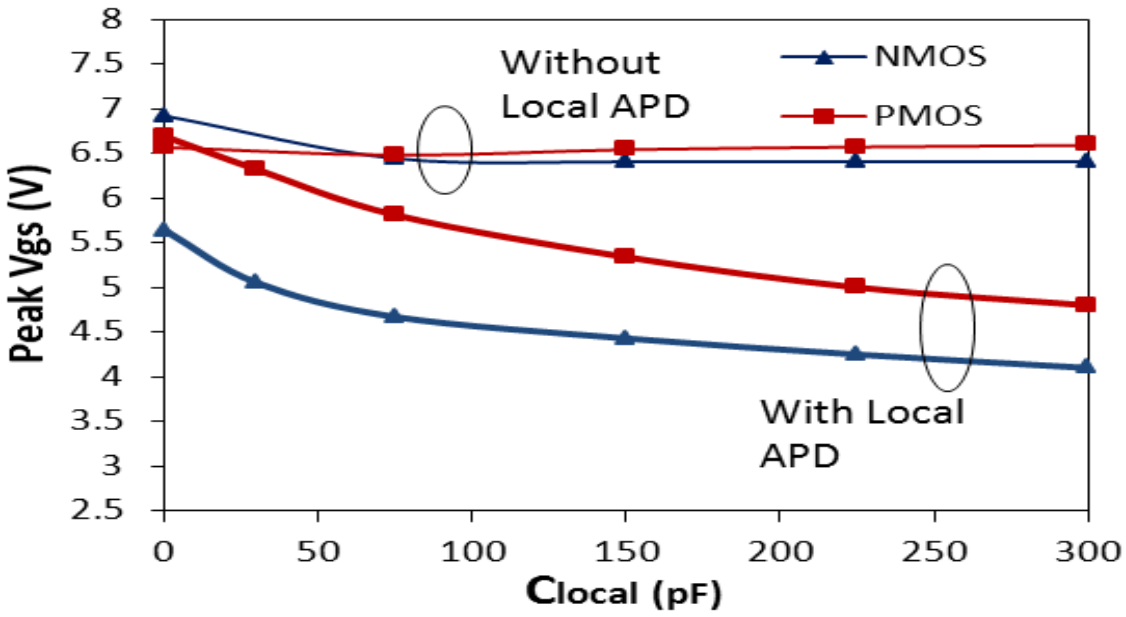

Figure 3.9 A local APD along with local decoupling capacitance greatly reduces V_{gs} of the receiver transistors. Local APD perimeter = 42 µm. Perimeter of the APD in the I/O ring is 210 µm.

Increasing the size of the APD devices in the pad ring does not provide the same benefit as does adding a local APD, as evidenced by the data shown in Figure 3.10. In these simulations, the

parasitic resistance from the core VSS1 and VSS2 busses to the APD in the I/O ring ($R_{vss1\text{-}core}$ and $R_{vss2\text{-}core}$ in Figure 3.6) is 6 Ω each, and the parasitic resistance to the local APD (R_{con}) is 0.5 Ω.

Figure 3.11 is a plot of the peak V_{gs} of the receiver NMOS as a function of both the amount of local decoupling capacitance and the local APD perimeter. V_{gs} decreases as either the amount of decoupling capacitance is increased and/or the perimeter of the local APD is increased. To clamp the V_{gs} to a particular value at a given CDM stress level, one adjusts the diode perimeter or the value of C_{local}. For example, a local APD with a perimeter of 84 µm needs 40 pF of C_{local} to clamp the NMOS V_{gs} to about 4.5 V. In order to get a further reduction of 0.3 V, either the local APD perimeter can be increased by about 150%, to 210 µm, or the value of C_{local} can be increased by about 50%, to 60 pF.

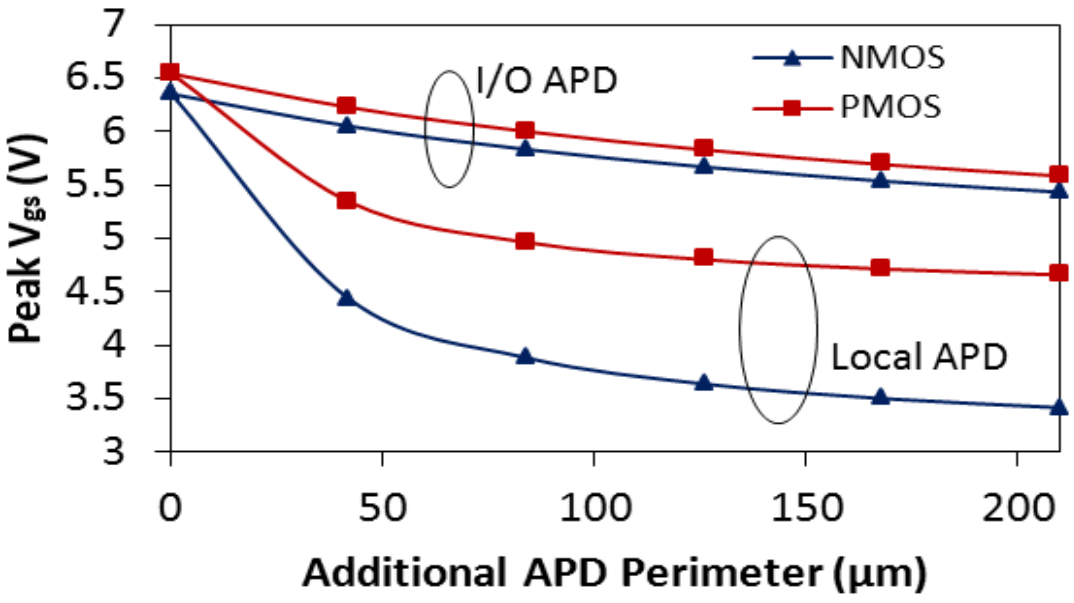

Figure 3.10 The effect of adding a local APD close to the internal I/O is compared with the effect of increasing the perimeter of the APD in the I/O ring. C_{local} = 150 pF in both cases, APD perimeter in the I/O ring = 210 µm. The local APD is not present initially.

It might appear that adjusting C_{local} is the more favorable approach; however, the absolute silicon area required to increase the amount of decoupling capacitance is 12 times higher than that required to increase the local APD perimeter. This analysis suggests that in light of the silicon area constraint, improved voltage clamping is best achieved by increasing the local APD perimeter, rather than increasing the amount of local decoupling capacitance. However, in designs with a large amount of core decoupling capacitance, a small local APD may be sufficient to clamp the V_{gs} to a safe level.

The efficacy of the local APD also depends on the parasitic resistance between the APD terminals and the source terminals of the driver and receiver NMOS transistors, R_{con}. If R_{con} is comparable to the parasitic resistance from the internal I/O to the APD in the I/O ring ($R_{vss1\text{-}core}$ and $R_{vss2\text{-}core}$ in Figure 3.8), the local APD provides little benefit, as shown in Figure 3.12. The

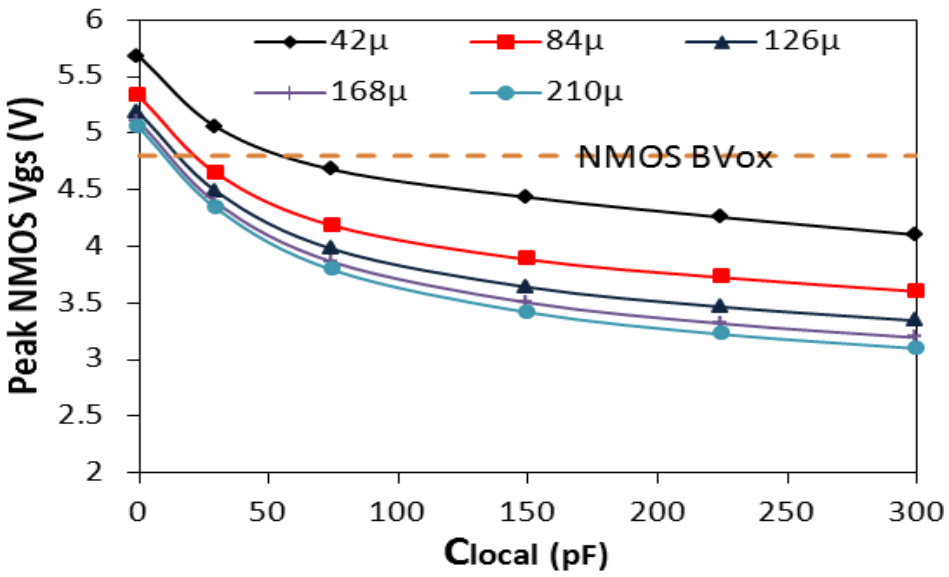

Figure 3.11 Peak V_{gs} across receiver NMOS as function of local decoupling capacitance for various perimeters of local APD.

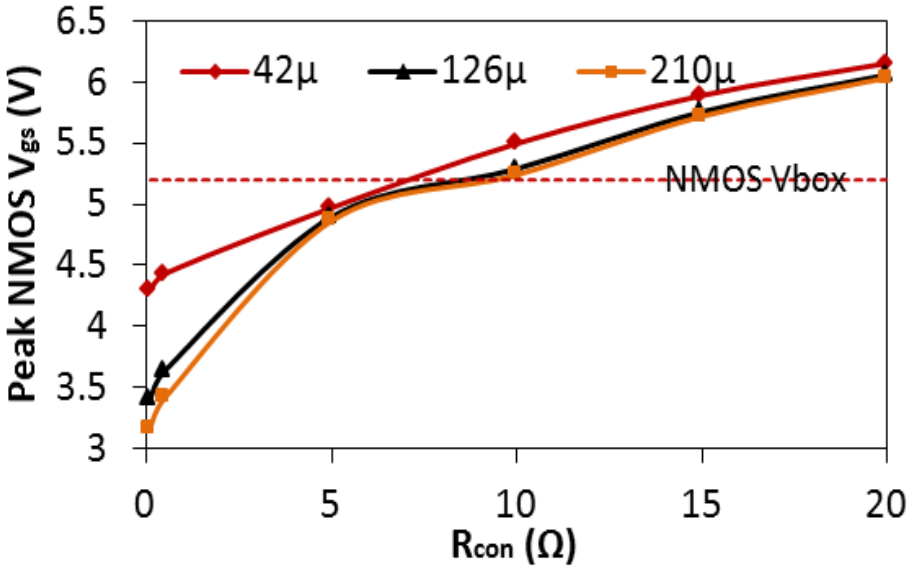

Figure 3.12 The effect of parasitic resistance connecting the driver and receiver transistors to the local APD terminals. The perimeter of APD in the I/O ring is 210 µm. $R_{vss1\text{-}core}$ and $R_{vss2\text{-}core}$ are each 6 Ω, this is the parasitic resistance to the APD in the I/O ring. C_{local}=150 pF.

local APD is intended for use when the internal I/O is located far from the pad ring, in which case R_{con} will be smaller than the resistance out to the ring, e.g., $R_{vss1\text{-}core}$. In flip-chip designs with the power and ground bumps over the core region, the APDs in the I/O ring may behave as local APDs if $R_{vss1\text{-}core}$ is very small.

If placing an APD in the core region between the analog and the digital grounds is a noise concern, the APD could be replaced by a circuit which is off during normal circuit operation and conducts current between the domains only during an ESD event [25].

3.2.5. Local Clamps

A local clamp may be placed at the receiver input [2], but this will increase the path delay unless the designer considers the capacitive loading due to the ESD clamp when sizing the driver. Simulation results show, however, that the CDM benefits of local clamps are significant. A

receiver with a diode based local clamp is shown in Figure 3.13. The peak stress voltage across the receiver gate oxides is plotted in Figure 3.14 as a function of the series resistance R_{series}.

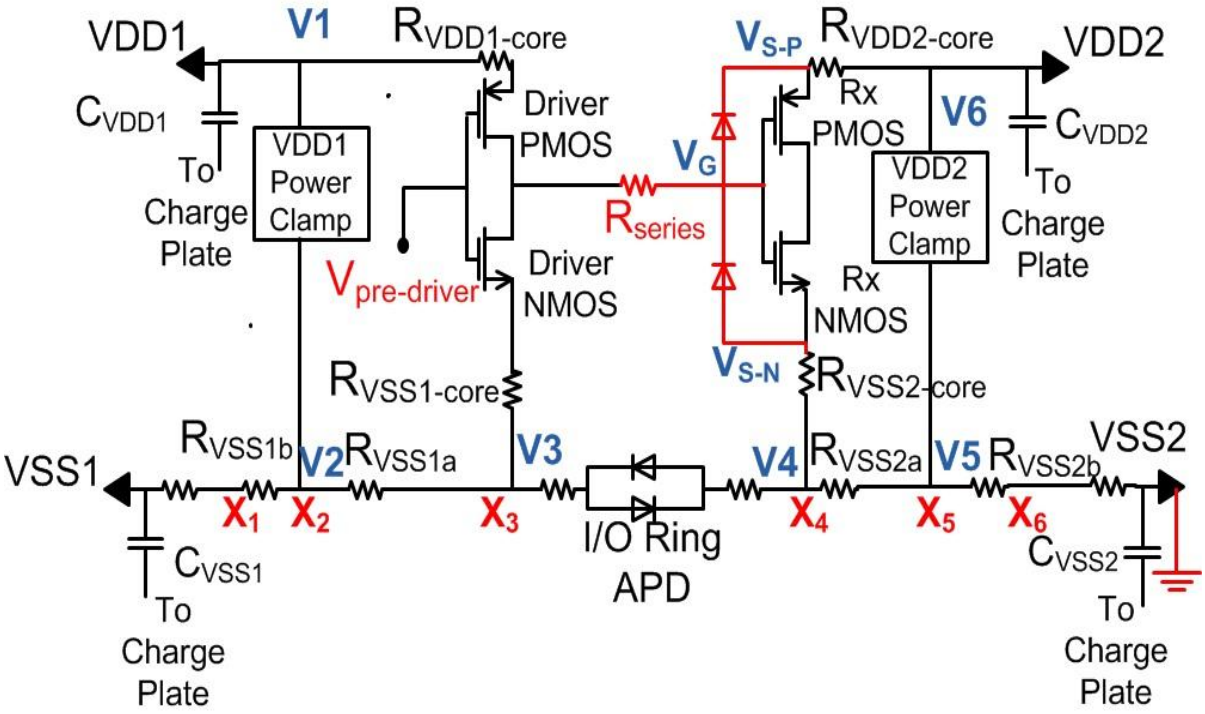

Figure 3.13 The internal I/O protected by a local clamp consisting of diodes across the gate-source terminals of the receiver transistors and a series resistor.

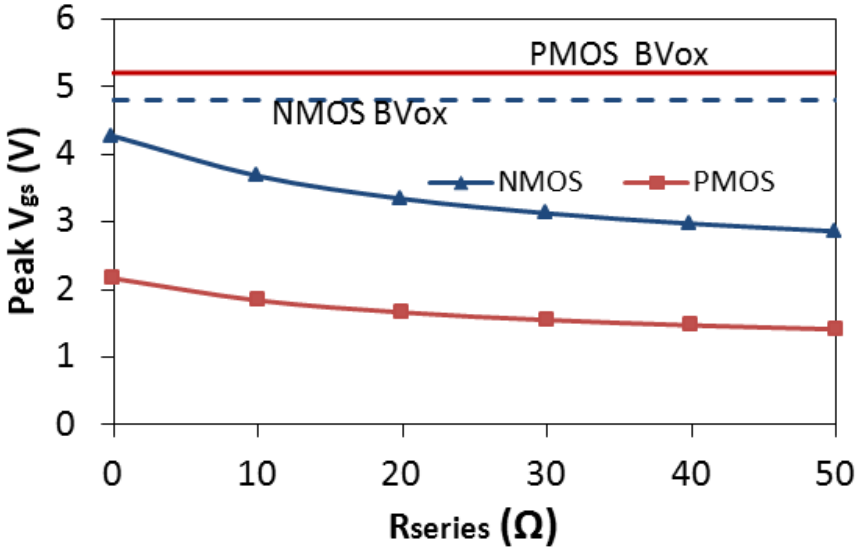

Figure 3.14 There is voltage stress at the receiver transistors when there is a diode based clamp at the receiver input. The perimeter of each diode in the dual diode clamp is 42 µm.

The stress voltage is clamped to a lower value when R_{series} is increased. However, increasing R_{series} provides diminishing returns. The simulation results indicate that an R_{series} of 20 Ω provides a sufficient margin to protect the receiver gate oxides against a 300 V CDM event.

Table 3.2 compares the peak V_{gs} of the receiver transistors for all of the investigated protection strategies. From Table 3.2, one can see that the local APD with local decoupling capacitance can clamp the voltage across the gate oxides below the gate oxide breakdown voltage (BV_{ox}). A local clamp at the receiver input will clamp the voltage to an even lower value, but there is a performance penalty due to an additional series resistor and the capacitance of the diodes. The driver transistors may need to be resized to meet the initial performance goals.

Table 3.2 Comparison of peak voltage stress across the receiver transistors for different protection strategies. Simulation results.

ESD Protection Methods	**Receiver Voltage Stress**	
	RX NMOS V_{gs} (V)	**RX PMOS V_{gs} (V)**
Diode based Clamp at the gate(Diode perimeter=42µm, R_{series}=20Ω)	3.3	1.7
Local APD of 120µm perimeter with C_{local}=150pF,	3.64	4.8
Cross domain power clamp (VDD1-VSS2) with $R_{VDD12}+R_{VSS12}$=0.5Ω	5	3.11

Chapter 4. COMPARISON OF SIMULATION RESULTS WITH MEASUREMENT DATA

In this section, the simulation results for Test Case B will be compared with the actual measurement data to establish the validity of the simulation model and the methodology. A simulation model was created for the 64-pad CDM testchip embedded in the 100-pin QFP package. The measurement method used on the test chip was developed by my colleague Nathan Jack [23].

The simulation model was created for the die on the VFTLP tester. A VF-TLP stress of 80 V was applied between the VDD1 and VSS2 pads of the design. The measurement data for the testchip were reused from the previous work [26]. Waveforms at the internal nodes of the CDM testchip were obtained using real-time probing at the die level, and the voltage monitor circuits recorded peak voltages at the internal nodes [23]. Table 4.1 compares the measured and simulated values of peak NMOS V_{gs} at two internal receivers, one with and one without a local clamp at the input. This local clamp was a grounded-gate NMOS. The simulation results match well with the measurement data.

Table 4.1 Comparison of measured and simulated voltage stress across the receiver NMOS gate oxide under VF-TLP stress.

	Voltage Monitor Reading (V)	**Simulated voltage (V)**
No clamp at the gate	3.4	3
Local clamp at the gate	1.89	1.86

Table 4.2 quantifies the effect of a local APD, without local decoupling capacitors, using both measurement and simulation. The measurement data was reused from the previous work [26]. Here, the potential difference was measured between the sources of the driver and the receiver NMOS devices. A cc-TLP stress was applied to the VSS2 pad near the receiver in the core. The peak discharge current was 1 A. The potential difference was measured between the VSS1 and VSS2 probe pads placed near the driver and the receiver, respectively. The agreement between the measurement and the simulation results is reasonably good. The data in Table 4.1 and Table 4.2 provide confidence in the simulation results presented in Chapter 3.

Table 4.2 Comparison of cc-TLP measurement results with the simulation results.

	cc-TLP Measurement (V)	**Simulation Results (V)**
Control Case	5.58	6.15
Internal I/O with local APD	5.05	5.45

The minor differences between the measurement and the simulation results stem from known inaccuracies in the model for the core power/ground bus mesh and in the models of the ESD protection devices. The extracted core power and the ground bus parasitic resistance networks were very large. To reduce the simulation runtime, a simple lumped model was used for the core power and ground bus in the simulation netlist. The model consisted of a resistor representing the point-to-point resistance between each of the internal I/O transistor terminals and the I/O ring power and the ground bus. The test chip consisted of a snapback based ESD device [2] in parallel with the active power clamp [17]. The snapback based ESD device was not modeled in the simulation netlist due to the absence of stand-alone test structure for the

measurement and modeling. Thus, only the active power clamps were modeled in the simulation netlist. Also, the diode models used in the simulation did not include the conductivity modulation effect prevalent during high current conduction [27]. However, both the measurement and the simulation results indicate that the stress at the receiver gate is lower in the case of the local APD placed near the internal I/O circuit.

Chapter 5. CONCLUSIONS AND FUTURE WORK

A simulation model for the CDM simulation of internal I/O circuits was presented in this work. Simulation results indicating the importance of modeling the package, the substrate and the on-chip ESD network were discussed. A summary of conclusions based on the simulation results will be presented in this chapter.

5.1. Conclusions

On chips that have been built on high resistivity substrates, internal I/O receivers may experience significant voltage stress unless an ESD protection circuit is appropriately placed near the internal I/O circuit. At an internal I/O, if the driver output is high, then not only the receiver NMOS but also the receiver PMOS can experience significant voltage stress when the receiver ground is zapped. This is especially the case if the charge storage capacitance of the receiver power domain is small. A local APD along with some local decoupling capacitance reduces the gate voltage stress at internal I/Os significantly with no performance penalty. However, the interconnect resistance between the local APD and the source terminals of the driver and receiver NMOS transistors has to be small in order for the local APD to effectively reduce the voltage stress at the receiver. Cross-domain clamps provide another approach to reduce the stress at the internal I/O; they are effective if placed close to the receiver ground pad.

This work also illustrated that when using a local clamp at the gate of the internal I/O, a small series resistor is sufficient to clamp the voltage below the gate oxide breakdown voltage. The simulation results also showed that the internal I/O failures are less likely to occur with a low resistivity substrate.

5.2. Future Work

The substrate model used in this study did not account for p-well and n-well regions above the uniformly doped substrate region. P-well is a thin sheet of highly doped region compared to the lowly doped, thicker substrate region. Similarly, the substrate to n-well diode provides another discharge path for the charge stored on the substrate backside ($C_{die\text{-}attach}$). Modeling these regions will increase the accuracy of the simulation results. The substrate model used in this study also does not account for the dielectric property of the silicon substrate. To account for this, a purely resistive model for the substrate is not sufficient. Each grid box has to be modeled by a parallel combination of a resistor and a capacitor. In the future, the impact of these factors should be studied.

In this study, it was assumed that the receiver sees the worst case stress when the driver output is high. It will be interesting to study the case in which the driver output is low. It will also be interesting to understand the conditions that lead to a particular state of the driver output under the CDM conditions.

Finally, the reliability risk from a CDM discharge to an integrated circuit in a stacked die package is largely unknown. Charge storage and CDM circuit simulation models for SiP ICs have not appeared in the current literature. In the future, the simulation model needs to be extended to stacked die designs.

REFERENCES

[1] Electrostatic Discharge Association, Rome, NY, "Fundamentals of ESD," June 2001. [Online]. Available: http://www.esda.org/basics/part1.cfm.

[2] A. Amarasekera and C. Duvvury, *ESD in Silicon Integrated Circuits*, 2nd ed. New York, NY: John Wiley and Sons, 2002.

[3] *Electrostatic Discharge Sensitivity Testing, Human Body Model, Component Level*, Standard Test Method ANSI/ESD STM 5.1-2007, 2007

[4] *Electrostatic Discharge Sensitivity Testing, Machine Model, Component Level*, Standard Test Method ANSI/ESD STM 5.2-1999, 1999.

[5] *Electrostatic Discharge Sensitivity Testing, Charged Device Model, Component Level*, Standard Test Method ANSI/ESD STM 5.3.1-1999, 1999

[6] Industry Council on ESD Target Levels, "White Paper 2: A Case for Lowering Component Level CDM ESD Specifications and Requirements," Mar. 2009. [Online]. Available: http://www.esda.org/documents/ /IndustryCouncilWhitePaper2.pdf

[7] M.S.B. Sowariraj, T. Smedes, C. Salm, A.J. Mouthaan, and F.G. Kuper, "Role of package parasitics and substrate resistance on the CDM failure levels," *Microelectronics Reliability*, vol. 43, pp. 1569-1575, 2003.

[8] M. Etherton, "Charged device model (CDM) ESD in ICs," PhD dissertation, Eidgenössische Technische Hochschule Zurich, 2006.

[9] K. Watanabe, T. Hiraoka, K. Sato, T. Sei and K. Numata, "New protection techniques and testchip design for achieving high CDM robustness," in *Proceedings of the EOS/ESD Symposium*, 2008, pp. 332-338.

[10] E. R. Worley, “Distributed gate ESD network architecture for inter-power domain signals,” in *Proceedings of the EOS/ESD Symposium*, 2004, pp. 238-247.

[11] J. Lee, Y. Huh, J. Chen, P. Bendix and S. M. Kang, “Chip level simulation for CDM failures in multi-power ICs,” in *Proceedings of the EOS/ESD Symposium*, 2000, pp. 456-464.

[12] R. Renninger, M-C. Jon, D. L. Lin, T. Diep and T. L. Welsher, “A field induced charged device model simulator,” in *Proceedings of the EOS/ESD Symposium*, 1989, pp. 59-71.

[13] B. C. Chou, T. J. Maloney and T. W. Chen, “Wafer-level charged device model testing,” in *Proceedings of the EOS/ESD Symposium*, 2008, pp. 115-124.

[14] T.T. Lu, Z.Y. Wang, and W. J. Wu, “Hierarchical Block Boundary-Element Method (HBBEM): a fast field solver for 3-D capacitance extraction,” *IEEE Transactions on Microwave Theory Tech*., vol. 52, no. 1, pp. 10 - 19, 2004.

[15] *Calibre Verification User’s Manual, Product Version 2009.2,* Mentor Graphics, 2009.

[16] L. Wall, T. Christiansen and J. Orwant, *Programming Perl*, 3rd ed. Cambridge, MA: O'Reilly, 2000.

[17] C. Torres, J. Miller, M. Stockinger, M. Akers, M. Khazhinsky and J. Weldon, “Modular, portable and easily simulated ESD protection networks for advanced CMOS technologies,” in *Proceedings of the EOS/ESD Symposium*, 2001, pp. 82-95.

[18] M. Lenzinger and E.H. Snow, “Fowler-Nordheim tunneling into thermally grown SiO_2,” in *Journal of Applied Physics,* vol. 40, pp. 278-83, 1969.

[19] A. Gerdemann, K. Bhatia, E. Rosenbaum, "A Kelvin transmission line pulsing system with optimized oscilloscope ranging," in *Proceedings of the EOS/ESD Symposium*, 2007, pp. 80-88.

[20] *MATLAB 7 Getting started Guide Release 2008a*, The Mathworks, Mar. 2008.

[21] *Verilog-AMS Language Reference Manual Version 2.2*, Accellera, Nov. 2004.

[22] *Virtuoso Spectre Simulator User Guide Product Version 5.1.41*, Cadence, July 2004.

[23] N. Jack, "Measurement and test methods for charged device model electrostatic discharge," M. S Thesis, University of Illinois at Urbana Champaign, Urbana, IL, 2009.

[24] J. Li, S. Hyvonen, and E. Rosenbaum, "Improved wafer-level VFTLP system and investigation of device turn-on effects," in *Proceedings of the EOS/ESD Symposium,* 2004, pp. 331-337.

[25] C. Duvvury, private communication, Feb. 2005.

[26] N. Jack, V. Shukla and E. Rosenbaum, "Investigation of Current Flow During Wafer-Level CDM Using Real-Time Probing," in press.

[27] J. Willemen et al., "Characterization and modeling of transient device behavior under CDM ESD stress," in *Proceedings of the EOS/ESD Symposium,* 2003, pp. 88-97.