THESIS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

Modular Battery Systems for Electric Vehicles based on Multilevel Inverter Topologies - Opportunities and Challenges

ANTON KERSTEN

Department of Electrical Engineering
Division of Electric Power Engineering
CHALMERS UNIVERSITY OF TECHNOLOGY
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ANTON KERSTEN
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Department of Electrical Engineering
Division of Electric Power Engineering
Chalmers University of Technology
SE–412 96 Göteborg
Sweden
Telephone +46(0)31-772 1000

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"A person with a new idea is a crank until the idea succeeds."

Mark Twain

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Abstract

Modular battery systems based on multilevel inverter (MLI) topologies can possibly overcome some shortcomings of two-level inverters when used for vehicle propulsion. The results presented in this thesis aim to point out the advantages and disadvantages, as well as the technical challenges, of modular vehicle battery systems based on MLIs in comparison to a conventional, two-level IGBT inverter drivetrain. The considered key aspects for this comparative investigation are the drive cycle efficiency, the inverter cost, the fault tolerance capability of the drivetrain and the conducted electromagnetic emissions. Extensive experiments have been performed to support the results and conclusions.

In this work, it is shown that the simulated drive cycle efficiency of different low-voltage-MOSFET-based, cascaded seven-level inverter types is improved in comparison to a similarly rated, two-level IGBT inverter drivetrain. For example, the simulated WLTP drive cycle efficiency of a cascaded double-H-bridge (CDHB) inverter drivetrain in comparison to a two-level IGBT inverter, when used in a small passenger car, is increased from 94.24 % to 95.04 %, considering the inverter and the ohmic battery losses. In contrast, the obtained efficiency of a similar rated seven-level cascaded H-bridge (CHB) drivetrain is almost equal to that of the two-level inverter drivetrain, but with the help of a hybrid modulation technique, utilizing fundamental selective harmonic elimination at lower speeds, it could be improved to 94.85 %. In addition, the CDHB and CHB inverters' cost, in comparison to the two-level inverter, is reduced from 342 € to 202 € and 121 €, respectively.

Furthermore, based on a simple three-level inverter with a dual battery pack, it is shown that MLIs inherently allow for a fault tolerant operation. It is explained how the drivetrain of a neutral point clamped (NPC) inverter can be operated under a fault condition, so that the vehicle can drive with a limited maximum power to the next service station, referred to as limp home mode. Especially, the detection and localization of open circuit faults has been investigated and verified

through simulations and experiments.

Moreover, it is explained how to measure the conducted emissions of an NPC inverter with a dual battery pack according to the governing standard, CISPR 25, because the additional neutral point connection forms a peculiar three-wire DC source. To separate the measured noise spectra into CM, line-DM and phase-DM quantities, two hardware separators based on HF transformers are developed and utilized. It is shown that the CM noise is dominant. Furthermore, the CM noise is reduced by 3 dB to 6 dB when operating the inverter with three-level instead of two-level modulation.

Index Terms: Batteries, Battery modeling, Battery system performance, BMS, Cascaded converters, Common mode noise, Conduction losses, DC-AC power converters, Drive cycle efficiency, Dual battery pack, Dynamic reconfiguration, Electric vehicles, Electromagnetic compatibility, Energy efficiency, Energy storage, H-bridge, Modular battery systems, Modular multilevel converters, Multilevel systems, Power MOSFET, vehicle electrification, vehicles.

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Anton Kersten
Gothenburg, Sweden
December, 2021

Contents

List of Abbreviations

The following list presents abbreviations that are used throughout this thesis:

AMN	Artificial mains network
ANPC	Active neutral point clamped
BEV	Battery electric vehicle
BMS	Battery management system
CDHB	Cascaded double-H-bridge
CHB	Cascaded H-bridge
CISPR	Comité international spécial des perturbations radioélectriques (English: international special committee on radio interference)
CM	Common mode
CSHB	Cascaded semi-H-bridge
DM	Differential mode
EIS	Electrochemical impdance spectroscopy
EUT	Equipment under test
EV	Electric vehicle
FSHE	Fundamental selective harmonic elimination
HVDC	High-voltage direct current
IGBT	Insulated-gate bipolar transistor
LISN	Line impedance stabilization network

MLI	Multilevel inverter
MOSFET	Metal oxide semiconductor field-effect transistor
NPC	Neutral point clamped
OP	Operating point
PHEV	Plug-in hybrid electric vehicle
PWM	Pulse-width modulation
RBS	Reconfigurable battery system
Rx	Receiver
SOC	State of charge
SOH	State of health
SVM	Space vector modulation
Tx	Transmitter
WLTP	Worldwide Harmonized Light Vehicles Test Procedure

Introduction

The number of deployed EVs has significantly increased during the past years [1, 2] and vehicle battery capacities are becoming larger [3]. This trend is presumably going to continue in the future [3, 4], driven largely by the need to sustainably reduce the emission of green house gases and nitrogen oxides [5]. For example, as described in [6], the particle pollution of EVs in comparison to diesel and gasoline vehicles is reduced by a factor of about eight and two, respectively. Moreover, the greenhouse gas emissions from EVs in comparison to modern Euro 6 diesel cars are significantly reduced (>>25 %; up to 85 %), even when charged by the most carbon-intensively produced electricity in Europe (Poland; 650 g of CO_2 per kWh) [7, 8].

In comparison to liquid fossil fuels, such as diesel and gasoline, the energy density of vehicle batteries is typically lower, by an order of magnitude [9–12], although the efficiency of an electric motor is typically higher than 90 % and, furthermore, it can be utilized for regenerative braking [9]. In contrast, hydrogen can be characterized by a specific energy which is about three times as high as the specific energy of diesel [12]. Nonetheless, the production of hydrogen, using electrolysis, and the additional transportation are typically very energy intensive. Thus, the energy efficiency from the production to the fueling at a hydrogen station is about 50 % [13]. As described in [14], the price for green hydrogen (3.5 - 6 € kg^{-1}) is about two to four times as high as that of commercially available grey hydrogen. Moreover, the consumption efficiency of a fuel cell EV is about 50 %, which is much lower than that of BEVs [13]. Therefore, as concluded in [13], batteries are the favored technology for the electrification of light vehicles when considering the overall energy efficiency, especially if clean electricity is regionally available throughout the year.

1.1 Technical Background and Motivation

As described in [15], the battery system is the most expensive component of a BEV. Typically, EV battery systems are formed by the parallel and series connection of individual battery cells to fulfill vehicles' voltage, energy and power requirements [16]. This system suffers from aging in terms of capacity fading [17] and increase of battery's impedance [18], which in turn reduces the power capability. As summarized in [19], the first life end-of-life for BEVs' batteries is typically reached when the remaining battery capacity has dropped below a threshold of 70 % to 80 % of the initial battery capacity. Nevertheless, as described in [20], EVs' batteries theoretically continue to satisfy the majority of daily travel needs below this threshold. However, an increased battery impedance leads not only to a reduced power capability but also to increased battery losses, which in turn leads to a reduced energy efficiency or may even cause thermal runaways, for example during fast charging [21,22]. Moreover, as described and illustrated in [23], individually faster degraded battery cells/modules can significantly reduce the battery packs' usable capacity when using passive balancing.

For these reasons, it seems reasonable to develop and exploit novel battery topologies for EVs to fully utilize and thermally balance individual battery cell or battery pack capacities and temperatures [24]. Due to its technical maturity, the two-level inverter topology is commonly used for variable speed drives, such as today's EVs [25, 26]. In contrast, multilevel inverters are typically used and suggested for high voltage applications, such as HVDC [27]. In the late 1990s, the authors of [28–30] were the first to suggest multilevel inverters for electric drives. For example, in [29, 30], a cascaded H-bridge inverter with integrated battery packs, forming a modular battery system, was suggested. As described in [31], the integrated battery packs can be drained according to their individual capacity and, further, as shown in [32], output waveforms of multilevel inverters' typically contain a reduced amount of harmonic components in comparison to two-level inverters. Based on simplified simulations models, the authors of [33–35] compare the drive cycle efficiency of a small PHEV when using a two-level and a multilevel inverter, showing an overall drive cycle efficiency improvement when using a multilevel inverter. Comparisons for BEVs in [36, 37], show a similar efficiency enhancement. However, the results presented in [33–37] contain only the total drive cycle losses, without distinguishing between the battery and inverter losses, and in [37] the battery losses are not even taken into account. Thus, the conclusions in [33–37]

might not be well grounded, because an oversized battery system and the use of a simplified battery or inverter model affect the loss estimation. Moreover, additional advantages of modular battery systems for vehicle propulsion, such as fault-tolerant operation, reduced inverter cost and increased battery life time were implied in [34]. However, up to today, these have not been fully explored in academia or industry yet.

1.2 Purpose and Main Contributions

The purpose of this thesis is to provide a comprehensive study about the advantages and disadvantages, as well as the technical challenges, of modular battery systems based on different multilevel inverter topologies in comparison to a classical, two-level IGBT inverter drivetrain for vehicle propulsion applications. The key aspects considered for this comparative investigation are the drive cycle efficiency of both the inverter and the battery system, the electromagnetic emission levels, the system's fault tolerance capability and the inverter cost. Furthermore, advantages of different output voltage modulation techniques, reducing the inverter's switching losses and the motor's current THD, are compared as well. In addition, advanced online or on-board capable battery diagnostics are derived.

To the best of the author's knowledge, the main contributions of this thesis can be categorized and summarized as follows:

- An analytical expression to evaluate the conduction losses of a three-phase, two-level MOSFET inverter considering the effect of the reverse conduction (third quadrant characteristic) and the blanking time has been derived and verified using experiments. It is pointed out that the neglect of MOSFET's reverse conduction capability typically leads to an overestimation of the conduction losses of any kind of MOSFET inverter, especially at partial load operation.
- It has been shown and experimentally verified that a pure resistive battery model overestimates the ohmic battery losses of modular battery systems by up to 20 % due to the additional low order current harmonics drawn from the individual battery modules. Furthermore, it is shown that in comparison to a two-level inverter, a dynamic battery model with two or three RC-pairs should be preferably used when estimating and comparing the ohmic battery losses of modular battery systems used for vehicle propulsion or variable speed drives.

- In comparison to a two-level IGBT inverter propulsion system, the drive cycle losses of modular battery systems based on different multilevel inverters have been quantified using simulations, considering a dynamic battery model with three *RC*-pairs and MOSFET's reverse conduction capability. Using cheap, low-voltage MOSFETs, multilevel inverters' drive cycle efficiency is typically increased, whereas the battery system efficiency is reduced, in comparison to the two-level IGBT inverter propulsion system. Nonetheless, it is shown that modular battery systems improve the overall drive cycle efficiency, even when used for small passenger vehicles.
- Electrolytic capacitors, as well as supercapacitors, have been considered to reduce the stress and the ohmic losses that low and medium-frequency current pulsations cause in a vehicle's modular battery system based on a seven-level cascaded H-bridge inverter. For this purpose, the reduction of the current harmonics with respect to capacitor type and capacitance and the ohmic battery loss reduction with respect to the added weight and system costs have been quantified using simulations and experiments. The obtained results indicate that additional filter capacitors improve the drive cycle efficiency relative to the added weight or system costs to a greater extent than increasing the battery system's capacity.
- A hybrid modulation technique for cascaded H-bridge seven-level propulsion inverters, utilizing multilevel PWM at lower speeds and FSHE at higher speeds, has been derived. The suggested hybrid technique improves both the output current quality and the drive cycle efficiency in comparison when using only multilevel PWM. For example, the WLTP drive cycle efficiency for the simulated small passenger car can be improved from 94.43 % to 94.85 %.
- Based on a three-level NPC inverter with a simple dual battery system, it has been shown how all types of single inverter faults, as well as nondestructive battery faults, can be handled and how the vehicle can be brought over to a reduced performance mode, referred to as limp home mode. In detail, a new, simple open circuit fault detection algorithm, using a current estimator, and its performance have been analyzed. Furthermore, two new fault localization algorithms, using a pulse pattern injection principle and an online adaption of the SVM, have been investigated and verified through simulations and experiments.

- A method is explained for measuring the conducted emissions of a fault-tolerant, three-level NPC inverter according to the governing standard, CISPR 25, using three LISNs, and the noise separation of the three-wire CM/DM is explained. Additionally, two compact hardware CM/DM separators, based on small-circuit HF transformers, for the CM, line-DM and phase-DM noise levels have been developed and characterized. An experimental test setup with an artificial machine load and an NPC prototype inverter has been used for measurements, operating the inverter with three-level and two-level modulation. Thereby, it is shown that the conducted emissions of a three-level in comparison to a two-level inverter are presumably reduced by 30 % to 50 %, corresponding to about 3 dB to 6 dB.
- It has been shown that an arbitrary number of semi-full bridge modules can be directly cascaded to form a novel multilevel inverter type that can bypass and positively insert the individual energy storages of a phase strand. Moreover, the energy storages of adjacent converter modules can be connected in parallel, reducing the phase strand's equivalent battery impedance. This novel multilevel converter topology can be applied at battery cell voltage level to form a modular battery system, simultaneously acting as an inverter and battery balancing circuitry. Therefore, the suggested topology is referred to as battery modular multilevel management (BM3) converter system.
- In general, the advantages of modular and reconfigurable battery systems, such as their fault tolerance capability and the possibility to combine different battery chemistries, have been extensively reviewed and advanced online and on-board capable battery impedance estimation techniques for modular battery systems and reconfigurable batteries have been developed. In addition, the controlled mitigation/elimination of the output voltage harmonics of multilevel inverters when using fundamental frequency switching has been analyzed for an arbitrary number of output voltage levels.

1.3 Thesis Outline

This thesis primarily consists of a collection of research publications, which are listed in the following Section 1.4 and can be found in the end of this thesis. Hence, the main work and research contributions of this thesis are contained in the research papers themselves.

The following chapters provide a context for the thesis's work. Furthermore, these summarize and briefly highlight the key results and research contributions

of the publications.

Chapter 2 gives an overview about the two-level inverter drivetrain topology, since it is currently the most common in BEVs. The topology's advantages and shortcomings are shortly discussed.

Chapter 3 shortly reviews the possible advantages and disadvantages of modular battery systems for vehicle propulsion in comparison to classical two-level inverter drivetrains. Additionally, the multilevel inverter topologies considered and developed in this thesis are described in detail and their working principles are explained and illustrated.

Chapter 4 deals with the quantification of the drive cycle efficiency improvement that modular battery systems can achieve in comparison to a classical two-level IGBT inverter drivetrain. Furthermore, the applied modeling approaches and their importance for the ohmic battery losses, using a dynamic battery model, and the MOSFET inverter conduction losses, considering MOSFET's reverse conduction capability, are described.

Chapter 5 deals with the fault tolerance capability of an NPC inverter with a simple dual battery, allowing for a reduced power or limp home mode under a fault condition. Furthermore, it is shown how inverter faults can be detected and localized without requiring any additional hardware.

Chapter 6 deals with the measurement of the conducted emissions of the fault-tolerant, three-level NPC inverter according to the international standard CISPR 25. Moreover, a brief comparison about the quantified conducted emissions of the three-level NPC inverter when operated with two-level and three-level modulation is given to verify the performance of the separators.

The last chapter, Chapter 7, briefly summarizes the thesis's key contributions and, based on these, draws some conclusions on the potential application of power electronics based battery propulsion systems in the future.

The remaining claimed research contributions can be directly found in the research publications.

1.4 List of Publications

This thesis is mainly based on the work contained in the following publications:

I. **A. Kersten**, E. Grunditz, and T. Thiringer - *Efficiency of Active Three-Level and Five-Level NPC Inverters Compared to a Two-Level Inverter in a Vehicle.* Published in 20th European Conference on Power Electronics and Applications (EPE'18 ECCE Europe), Riga, Latvia, pp. P.1-P.9, Sept. 2018.

II. **A. Kersten**, K. Oberdieck, A. Bubert, M. Neubert, E. Grunditz, T. Thiringer, and R.W. De Doncker - *Fault Detection and Localization for Limp Home Functionality of Three-Level NPC Inverters With Connected Neutral Point for Electric Vehicles.* Published in IEEE Transactions on Transportation Electrification, vol. 5, no. 2, pp. 416-432, June 2019.

III. **A. Kersten**, K. Oberdieck, J. Gossmann, A. Bubert, R. Loewenherz, M. Neubert, E. Grunditz, T. Thiringer, and R.W. De Doncker - *CM & Line-DM Noise Separation for Three-Level NPC Inverter with Connected Neutral Point for Vehicle Traction Applications.* Published in IEEE Transportation Electrification Conference and Expo (ITEC), Detroit, MI, USA, pp. 1-6, June 2019.

IV. O. Theliander, **A. Kersten**, M. Kuder, E. Grunditz, T. Thiringer - *$LiFePO_4$ Battery Modeling and Drive Cycle Loss Evaluation in Cascaded H-Bridge Inverters for Vehicles.* Published in IEEE Transportation Electrification Conference and Expo (ITEC), Detroit, MI, USA, pp. 1-7, June 2019.

V. **A. Kersten**, O. Theliander, E. Grunditz, T. Thiringer, and M. Bongiorno - *Battery Loss and Stress Mitigation in a Cascaded H-Bridge Multilevel Inverter for Vehicle Traction Applications by Filter Capacitors.* Published in IEEE Transactions on Transportation Electrification, vol. 5, no. 3, pp. 659-671, Sept. 2019.

VI. M. Kuder, **A. Kersten**, L. Bergmann, R. Eckerle, F. Helling, and T. Weyh - *Exponential Modular Multilevel Converter for Low Voltage Applications.* Published in 21st European Conference on Power Electronics and Applications (EPE '19 ECCE Europe), Genova, Italy, pp. P.1-P.11, Sept. 2019.

VII. **A. Kersten**, M. Kuder, E. Grunditz, Z. Geng, E. Wikner, T. Thiringer, and T. Weyh - *Inverter and Battery Drive Cycle Efficiency Comparisons of CHB and MMSP Traction Inverters for Electric Vehicles.* Published in 21st European Conference on Power Electronics and Applications (EPE '19 ECCE Europe), Genova, Italy, pp. P.1-P.12, Sept. 2019.

VIII. **A. Kersten**, L. Baum, W. Han, T. Thiringer, and M. Bongiorno - *Output Voltage Synthesis of a Modular Battery System based on a Cascaded H-Bridge Multilevel Inverter Topology for Vehicle Propulsion: Multilevel Pulse Width Modulation vs. Fundamental Selective Harmonic Elimination.* Published in IEEE Transportation Electrification Conference & Expo (ITEC), Chicago, IL, USA, pp. 296-302, June 2020.

IX. W. Han, and **A. Kersten** - *Analysis and Estimation of the Maximum Circulating Current during the Parallel Operation of Reconfigurable Battery Systems.* Published in IEEE Transportation Electrification Conference & Expo (ITEC), Chicago, IL, USA, pp. 229-234, June 2020.

X. M. Kuder, J. Schneider, **A. Kersten**, T. Thiringer, R. Eckerle, and T. Weyh - *Battery Modular Multilevel Management (BM3) Converter applied at Battery Cell Level for Electric Vehicles and Energy Storages.* Published in PCIM Europe digital days 2020; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nuremberg, Germany, pp. 1-8, July 2020.

XI. **A. Kersten**, M. Kuder, A. Singer, W. Han, T. Thiringer, T. Weyh, and R. Eckerle - *Elimination/Mitigation of Output Voltage Harmonics for Multilevel Converters Operated at Fundamental Switching Frequency using Matlab's Genetic Algorithm Optimization.* Published in 22nd European Conference on Power Electronics and Applications (EPE'20 ECCE Europe), Lyon, France, pp. 1-12, Sept. 2020.

XII. **A. Kersten**, M. Kuder, W. Han, T. Thiringer, A. Lesnicar, T. Weyh, and R. Eckerle - *Online and On-Board Battery Impedance Estimation of Battery Cells, Modules or Packs in a Reconfigurable Battery System or Multilevel Inverter.* Published in IECON 2020 - 46th Annual Conference of the IEEE Industrial Electronics Society, Singapore, pp. 1884-1891, Oct. 2020.

XIII. **A. Kersten**, M. Kuder, J.L. Marques-Lopez, F. Schwitzgebel, T. Thiringer, R. Marquardt, T. Weyh, and R. Eckerle - *Sensorless Capacitor Voltage Balancing of a Grid-Tied, Single-Phase Hybrid Multilevel Converter with Asymmetric Capacitor Voltages using Dynamic Programming.* Published in IECON 2020 - 46th Annual Conference of the IEEE Industrial Electronics Society, Singapore, pp. 4288-4293, Oct. 2020.

XIV. O. Theliander, **A. Kersten**, M. Kuder, W. Han, E. Grunditz, and T. Thiringer - *Battery Modeling and Parameter Extraction for Drive Cycle Loss Evaluation of a Modular Battery System for Vehicles based on a Cascaded H-Bridge Multilevel Inverter.* Published in IEEE Transactions on Industry Applications, vol. 56, no. 6, pp. 6968-6977, Nov.-Dec. 2020.

XV. W. Han, T. Wik, **A. Kersten**, G. Dong, and C. Zou - *Next-Generation Battery Management Systems: Dynamic Reconfiguration.* Published in IEEE Industrial Electronics Magazine, vol. 14, no. 4, pp. 20-31, Dec. 2020.

XVI. **A. Kersten**, K. Oberdieck, J. Gossmann, A. Bubert, R. Loewenherz, M. Neubert, T. Thiringer, and R.W. De Doncker - *Measuring and Separating Conducted Three-Wire Emissions From a Fault-Tolerant, NPC Propulsion Inverter With a Split-Battery Using Hardware Separators Based on HF Transformers.* Published in IEEE Transactions on Power Electronics, vol. 36, no. 1, pp. 378-390, Jan. 2021.

XVII. A. Acquaviva, A. Rodionov, **A. Kersten**, T. Thiringer and Y. Liu - *Analytical Conduction Loss Calculation of a MOSFET Three-Phase Inverter Accounting for the Reverse Conduction and the Blanking Time.* Published in IEEE Transactions on Industrial Electronics, vol. 68, no. 8, pp. 6682-6691, Aug. 2021.

XVIII. **A. Kersten**, M. Kuder, and T. Thiringer - *Hybrid Output Voltage Modulation (PWM-FSHE) for a Modular Battery System Based on a Cascaded H-Bridge Inverter for Electric Vehicles Reducing Drivetrain Losses and Current Ripple.* Published in MDPI Energies, vol. 14, no. 5, pp. 1424, March 2021.

XIX. W. Han, **A. Kersten**, C. Zou, T. Wik, X. Huang, and G. Dong - *Analysis and Estimation of the Maximum Switch Current during Battery System Reconfiguration.* Published in IEEE Transactions on Industrial Electronics, doi: 10.1109/TIE.2021.3091923, June 2021.

Furthermore, the author contributed to the following publications:

A. **A. Kersten**, Y. Liu and D. Pehrman - *Rotor Design of a Line-Start Synchronous Reluctance Machine with Respect to Induction Machine for Industrial Applications.* Published in 2018 XIII International Conference on Electrical Machines (ICEM), Alexandroupoli, Greece, pp. 393-399, Oct. 2018.

B. **A. Kersten**, Y. Liu, D. Pehrman and T. Thiringer - *Rotor Design of Line-Start Synchronous Reluctance Machine With Round Bars.* Published in IEEE Transactions on Industry Applications, vol. 55, no. 4, pp. 3685-3696, July-Aug. 2019.

C. **A. Kersten**, M. Kuder, and T. Thiringer - *Review of Technical Design and Safety Requirements for Vehicle Chargers and Their Infrastructure According to National Swedish and Harmonized European Standards.* Published in MDPI Energies, vol. 14, no. 11, pp. 3301, June 2021.

D. F. Schwitzgebel, M. Kuder, **A. Kersten**, C. Meisl and T. Weyh - *Design and Testing of a Novel Transcranial Magnetic Stimulator with Adjustable Pulse Dynamics and High Current Capability (>2 kA) based on a Modular Cascaded H-Bridge Inverter Topology.* Published in PCIM Europe digital days 2021; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nuremberg, Germany, pp. 1-8, May 2021.

E. J. Buberger, **A. Kersten**, M. Kuder, A. Singer, A. Mashayekh, J. Estaller, T. Thiringer, R. Eckerle and T. Weyh - *Charging Strategy for Battery Electric Vehicles with a Battery Modular Multilevel Management (BM3) Converter System using a PR controller.* Published in 23rd European Conference on Power Electronics and Applications (EPE'21 ECCE Europe), Ghent, Belgium, pp. P.1-P.10, Sept. 2021.

F. A. Mashayekh, **A. Kersten**, M. Kuder, J. Estaller, M. Khorasani, J. Buberger, R. Eckerle and T. Weyh - *Proactive SoC Balancing Strategy for Battery Modular Multilevel Management (BM3) Converter Systems and Reconfigurable Batteries.* Published in 23rd European Conference on Power Electronics and Applications (EPE'21 ECCE Europe), Ghent, Belgium, pp. P.1-P.10, Sept. 2021.

G. F. Neukirchinger, **A. Kersten**, M. Kuder, B. Lohse, F. Schwitzgebel and T. Weyh - *Where Transcranial Magnetic Stimulation is headed to: The Modular Extended Magnetic Stimulator.* Published in 2021 IEEE International Conference on Environment and Electrical Engineering and 2021 IEEE Industrial and Commercial Power Systems Europe (EEEIC / I&CPS Europe), Bari, Italy, pp. 1-6, Sept. 2021.

H. N. Sorokina, J. Estaller, **A. Kersten**, J. Buberger, M. Kuder, T. Thiringer, R. Eckerle and T. Weyh - *Inverter and Battery Drive Cycle Efficiency Comparisons of Multilevel and Two-Level Traction Inverters for Battery Electric Vehicles.* Published in 2021 IEEE International Conference on Environment and Electrical Engineering and 2021 IEEE Industrial and Commercial Power Systems Europe (EEEIC / I&CPS Europe), Bari, Italy, pp. 1-8, Sept. 2021.

I. T. Högerl, J. Buberger, F. Schwitzgebel, L. Obkircher, J. Estaller, M. Hohenegger, **A. Kersten**, M. Kuder, R. Eckerle and T. Weyh - *Battery Emulation for Battery Modular Multilevel Management (BM3) Converters and Reconfigurable Batteries with Series, Parallel and Bypass Function.* Published in 2021 IEEE International Conference on Environment and Electrical Engineering and 2021 IEEE Industrial and Commercial Power Systems Europe (EEEIC / I&CPS Europe), Bari, Italy, pp. 1-8, Sept. 2021.

J. J. Estaller, **A. Kersten**, M. Kuder, A. Mashayekh, J. Buberger, T. Thiringer, R. Eckerle and T. Weyh - *Battery Impedance Modeling and Comprehensive Comparisons of State-Of-The-Art Cylindrical 18650 Battery Cells considering Cells' Price, Impedance, Specific Energy and C-Rate.* Published in 2021 IEEE International Conference on Environment and Electrical Engineering and 2021 IEEE Industrial and Commercial Power Systems Europe (EEEIC / I&CPS Europe), Bari, Italy, pp. 1-8, Sept. 2021.

Two-Level Inverter Drivetrain

The two-level inverter drivetrain topology is most common in today's EVs [25, 26]. It typically comprises a 400 V battery system (at rated SOC), a three-phase, two-level IGBT inverter and a three-phase electric machine, as schematically depicted in Fig. 2.1. The entire traction system is usually insulated and is, thus, on a floating potential relative to the vehicle's chassis (depicted as ground). In comparison to three-phase multilevel inverters, the two-level inverter topology utilizes only six semiconductor switches.

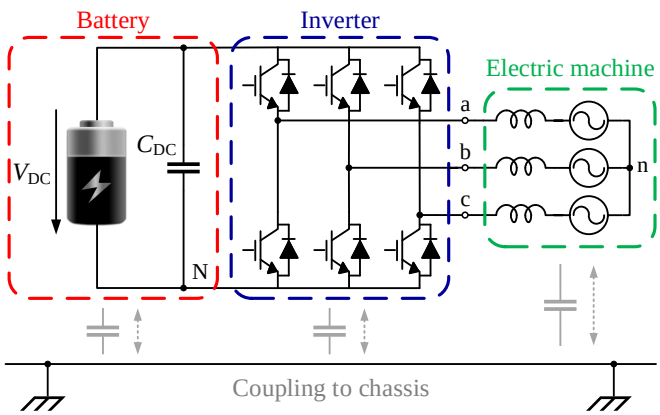


Figure 2.1: Three-phase, two-level inverter drivetrain of an EV.

2.1 Battery Architecture using Passive Balancing

The battery pack of a two-level inverter drivetrain is schematically depicted in Fig. 2.2. It typically consists of a large number of series and parallel connected

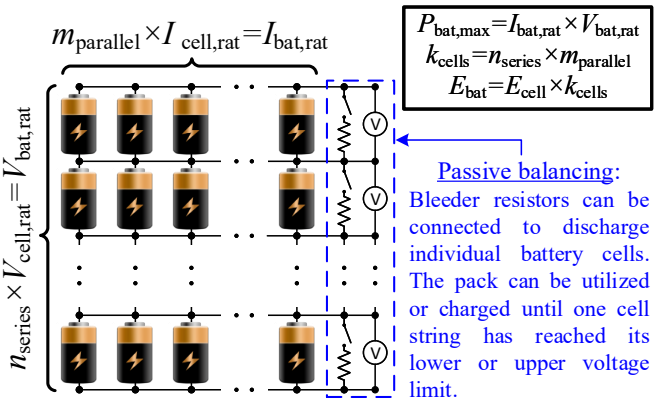


Figure 2.2: Structure of a battery pack with passive balancing utilizing bleeder resistors (shunt transistor method).

battery cells to satisfy the vehicle's energy and power requirements and, thus, the electric machine's voltage and current ratings. The battery cells are commonly interconnected using welding or soldering techniques [38, 39]. Therefore, individual battery cells cannot be replaced throughout the lifetime of the battery pack. To operate each battery cell within its SOC limits, passive balancing [40, 41] is most commonly used. Hence, at least each parallel battery string/strand is equipped with a voltage sensor and a transistor controlled bleeder resistor, which can dynamically dissipate excessive charge during the charging or the operation of the battery pack. This approach is referred to as shunt transistor method. It achieves a cost-effective and compact balancing solution in comparison to active balancing methods [42]. Nonetheless, since the weakest cell of each parallel battery strand dictates the utilizable capacity of each parallel strand and the weakest parallel strand constrains the utilizable capacity of the entire battery pack, it can be stated that only one faulty battery cell can lead to a severe reduction of the utilizable total battery capacity. Throughout the battery's life, individual battery cells can degrade faster than others due to thermal gradients during operation and, thus, resulting not only in capacity fading [43], but also reducing the available power capability. As a consequence, the ohmic battery losses and the heat dissipation in the passive balancing circuitry increases as well throughout the battery lifetime,

which are a major concern in terms of the system's cooling capabilities. Therefore, if the SOH of the battery pack has dropped below 80 %, it is recommended to replace the entire battery pack [44]. Nonetheless, replaced vehicle batteries can be further used in second-life applications with a reduced power requirement such as stationary energy storage applications for better utilization of renewable energy sources [45, 46].

2.2 Output Voltage Modulation

The two-level inverter of the drivetrain, emphasized in blue in Fig. 2.1, is used to control the three-phase, sinusoidal currents feeding the electric machine. For BEVs, it typically consists of six IGBT switches with six antiparallel diodes. Each phase, such as phase a, consists of a high-side switch S_{a1} and low-side switch S_{a2}. The switches of each phase can be activated or deactivated ($S_{\mathrm{a1}} = \{1, 0\}$ and $S_{\mathrm{a2}} = \{1, 0\}$), whereas these must be inversely operated to avoid a shoot-through fault. With the help of the phase's switching state expression

$$S_{\mathrm{a,2L}} = \{1, 0\} = S_{\mathrm{a1}} = -S_{\mathrm{a2}} \tag{2.1}$$

the instantaneous pole voltage of phase a v_{aN} can be described as

$$v_{\mathrm{aN}} = S_{\mathrm{a,2L}} V_{\mathrm{DC}} \quad . \tag{2.2}$$

The desired output voltage can be synthesized using pulse width modulation (PWM) or space vector modulation (SVM) [32]. Using PWM, a high frequency, triangular carrier is compared with the desired sinusoidal reference voltage to determine the instantaneous switching state of each phase. The frequency of the carrier f_{c} corresponds to the switching frequency f_{sw}. Fig. 2.3 depicts the output voltage modulation of the reference voltage $v'_{\mathrm{aN,ref}}$ for a modulation index of

$$M = \frac{2V_{\mathrm{aN,ref}}}{V_{\mathrm{DC}}} = 0.9 \tag{2.3}$$

and a carrier ratio of

$$m_{\mathrm{f}} = \frac{f_{\mathrm{c}}}{f_1} = \frac{f_{\mathrm{sw}}}{f_1} = 14 \tag{2.4}$$

with f_1 being the fundamental frequency. The triangular carrier waveform v_{carrier} is depicted in red. Usually, to increase the amplitude of the reference voltage $v'_{\mathrm{aN,ref}}$ by about up to 15 %, optimal zero sequence injection is used [32], shown as the adapted reference waveform $v_{\mathrm{aN,ref}}$. The resulting PW modulated pole voltage v_{aN} is depicted in blue in Fig. 2.3. Using discrete-time synchronous PWM, the

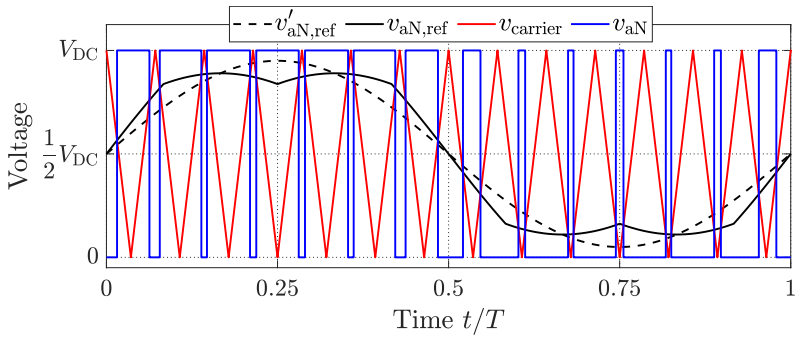


Figure 2.3: Naturally sampled voltage synthesis of the pole voltage $v'_{\mathrm{aN,ref}}$ using PWM with optimal zero sequence injection, resulting in $v_{\mathrm{aN,ref}}$, and $m_{\mathrm{f}} = 14$.

switching frequency f_{sw} typically corresponds to the sampling frequency f_{s}. To properly modulate the desired reference voltage and, thus, to satisfy the estimation

$$v'_{\mathrm{aN,ref}} \approx v_{\mathrm{aN},1} \tag{2.5}$$

the switching frequency should be selected according to

$$\frac{f_{\mathrm{sw}}}{f_1} \geq 10 \tag{2.6}$$

for the entire operating range of the vehicle [32, 47]. As described in [47], if $\frac{f_{\mathrm{sw}}}{f_1}$ equals 10, the phase shift is 18° and the amplitude error is about 2 %.

SVM can be similarly used instead of PWM, whereas the selection of the redundant zero vector ($V_{\alpha\beta} = 0$ can be achieved using $[S_{\mathrm{a,2L}}\ S_{\mathrm{b,2L}}\ S_{\mathrm{c,2L}}]$=[0 0 0] and $[S_{\mathrm{a,2L}}\ S_{\mathrm{b,2L}}\ S_{\mathrm{c,2L}}]$=[1 1 1]) could result in a different harmonic content and, thus, the current quality could be affected [32].

2.2.1 Common Mode Voltage Problem

The harmonic components of the pole voltage v_{aN} for a modulation index $M = 1.15$ and a carrier ratio $m_{\mathrm{f}} = 40$ are depicted in Fig. 2.4. The red emphasized harmonics are differential mode (DM) harmonics of the pole voltage v_{aN}, rotating in the forward and backward directions. These cause three-phase currents and, thus, distort the current quality. The common mode (CM) harmonics of the pole voltage v_{aN} are emphasized in blue ($V_{\mathrm{aN},h} = V_{\mathrm{nN},h}$). Ideally, the common mode harmonics do not cause any currents in a floating three-phase system. However, due to parasitic couplings, these can result in unwanted, capacitive currents, such as bearing currents [48, 49], and these can cause unwanted electromagnetic

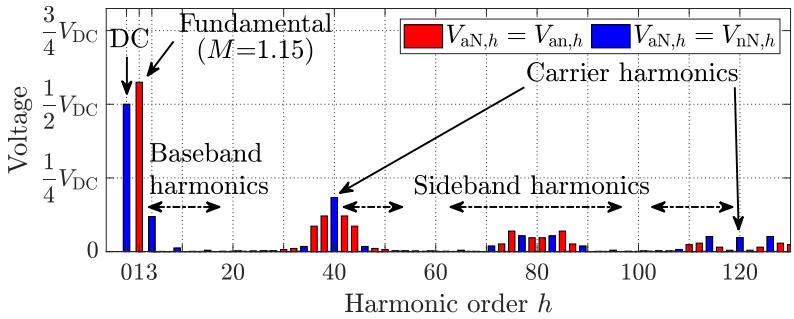


Figure 2.4: Harmonic content of v_{aN} when using PWM with optimal zero sequence injection and $m_f = 40$.

inferences with on-board equipment or surrounding devices [50, 51]. Probable consequences could be insulation failure [52], reduced bearing lifetime [53–55] or even the malfunctioning of on-board equipment or on-board devices. Since the propulsion inverter is the most powerful component (in terms of the kVA rating) in an EV, it is of utmost importance to mitigate the electromagnetic emissions of the inverter using for example proper shielding or the application of an EMI-filter [56]. Though, the design of an EMI-filter or the effective application of shielding can be quite challenging for fast switching inverters with a high voltage (>400 V) DC link [56]. Furthermore, these measures introduce additional costs and losses [56]. Standards, for example CISPR 25 [57], MIL-STD-461 [58] or SAE J1113/41 [59], are often used to classify electric drivetrains by the noise levels on dc-power cables. These typically cover a frequency range from 150 kHz to 30 MHz (CISPR band B), sometimes even up to 108 MHz, for conducted emissions. However, this range is often not sufficient [51, 60]. Due to the rapid roll-off in magnitude relative to the frequency, the dominant common mode harmonic with the highest energy content can be observed at the switching frequency f_{sw}, which lies within the supraharmonic band (2 kHz to 150 kHz) [32, 61].

2.2.2 Fault Intolerance

To protect the two-level inverter, as depicted in Fig. 2.1, from overcurrents or short circuits, additional gate driver circuitry, such as described in [62–64], can be employed to automatically turn off the inverter's gate signals. If the fault cannot be cleared after restarting the inverter, this kind of fault is referred to as permanent fault [65]. Permanent inverter faults can be caused by various reasons, such as the malfunction of the gate drive circuitry or the breakdown of a semiconductor switch

due to an unwanted overvoltage [66]. Consequently, the two-level inverter cannot be further operated under a permanent fault [67], which would lead to a total shutdown of the vehicle drivetrain. In this case, roadside assistance is required and the vehicle must be towed to the nearest repair shop.

To illustrate the ceased functioning of the inverter after a single short or open circuit fault of a semiconductor switch, the space vector diagram in the αβ-plane, first introduced in [68], can be used. As described in (2.1), each phase of the inverter has two valid output voltage states and, thus, with the help of the switching state vector

$$S_{2\mathrm{L}} = \begin{bmatrix} S_{\mathrm{a,2L}} \\ S_{\mathrm{b,2L}} \\ S_{\mathrm{c,2L}} \end{bmatrix} \tag{2.7}$$

it can be seen that there are eight valid switching state combinations. Using the Clark transformation matrix, the three-phase output voltage of each switching state can be transformed according to

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \cdot \begin{bmatrix} S_{\mathrm{a,2L}} V_{\mathrm{DC}} \\ S_{\mathrm{b,2L}} V_{\mathrm{DC}} \\ S_{\mathrm{b,2L}} V_{\mathrm{DC}} \end{bmatrix} \tag{2.8}$$

and the space vector diagram in the αβ-plan, as shown in Fig. 2.5, can be obtained. The reference voltage $\underline{V}_{\mathrm{ref}}$, depicted in the first sector, can be synthesized by the three nearest vectors [68]. In case of a permanent fault, such as a single

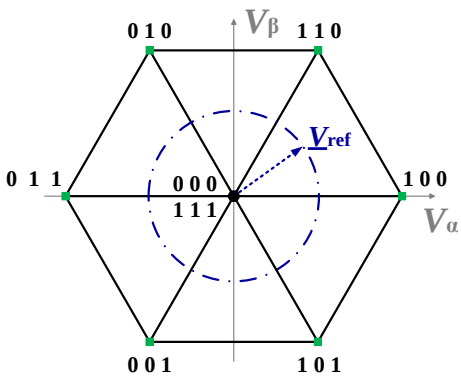


Figure 2.5: Space vector diagram in the αβ-plane with $\underline{V}_{\mathrm{ref}}$ lying in the first sector.

short or open circuit fault of a semiconductor switch, the valid switching state combinations reduce from eight to four. This is due to the reason that only one

valid switching state remains for the faulty phase when considering both positive and negative phase current values. Consequently, the space vector diagram changes, as exemplified in Figs. 2.6(a) and 2.6(b), for a permanent open or a short circuit fault of the high side switch of phase a S_{a1}, respectively. As can be seen for both fault cases, the rotating reference voltage $\underline{V}_{ref}$ can only be properly synthesized in two of the six sectors. Thus, the inverter cannot create a rotating three-phase voltage any longer and, consequently, the three-phase currents cannot be properly controlled any longer, either.

As described above, the consideration of the the remaining valid switching states and, thus, the remaining voltage vectors in the αβ-plane can be easily used to conclude the fault intolerance of the two-level inverter.

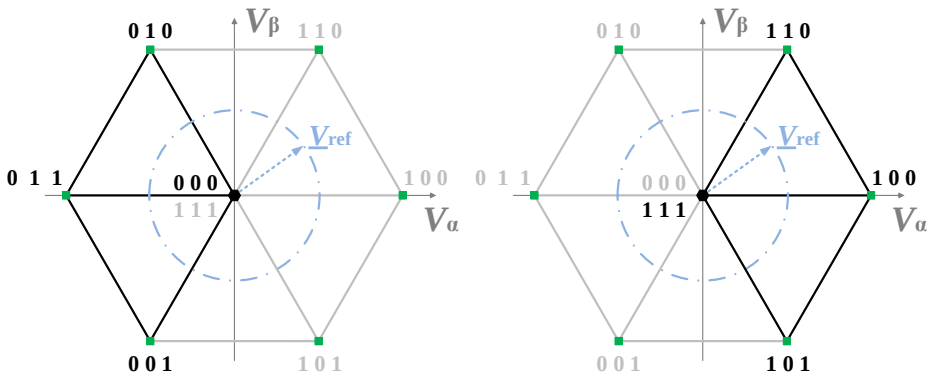


Figure 2.6: Adaption of the space vector diagram in the αβ-plane in case of a permanent (a) open circuit fault and (b) short circuit fault of the high side switch of phase a.

Modular Battery Architectures based on Multilevel Inverters

To fully utilize a vehicle's entire battery capacity and to create a scalable battery architecture, it seems reasonable to employ a modular battery structure instead of a single battery pack architecture, as illustrated in Fig. 3.1. When having a modular battery architecture, each small, individual battery pack must be attached to a power electronics converter to dynamically control and optimize its energy flow. Such kinds of modular battery systems are often referred to as reconfigurable battery systems (RBS) [69], which can be even applied at battery cell level. An RBS typically requires an additional, designated propulsion

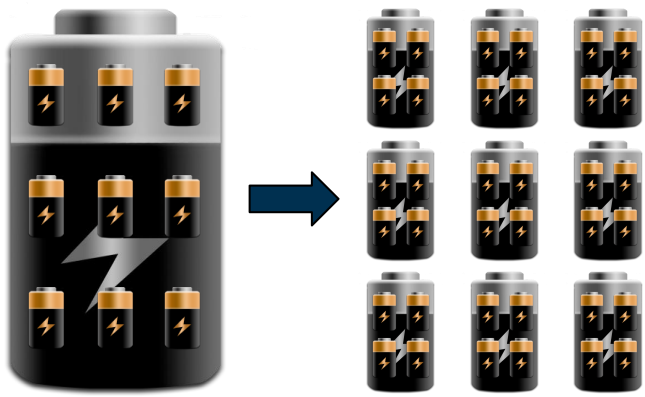


Figure 3.1: Rearrangement of the high voltage battery pack into a modular battery system consisting of small, generic battery packs.

inverter. In contrast to RBSs, different multilevel inverter topologies can act as modular battery systems at battery pack level and, in addition, these can simultaneously function as a propulsion inverter. Usually, modular or cascaded multilevel inverters/converters are used for power system applications, such as high voltage DC transmission systems or reactive power compensators [70–72], coping with high system voltages and typically employing IGBT switches. For low-voltage battery packs (<100 V), low-priced Si MOSFETs instead of IGBTs can be used to achieve a cost-effective inverter design [37, 73]. The available literature [32, 72] and [31, 74, 75] extensively describes how to modulate the output voltage using multilevel pulse-width modulation (PWM) or space vector modulation (SVM) and, further, how to balance the batteries' SOC or SOH.

The possible advantages of MLIs employing a modular battery system in comparison to a two-level inverter for EV drivetrains can be shortly summarized as follows:

- **Increased inverter efficiency:** The usage of low-voltage Si MOSFETs in comparison to IGBTs improves the inverter efficiency at low speeds and partial load operation and, thereby, the overall drive cycle efficiency is improved as well [37].
- **Reduced electromagnetic emissions:** The decreased voltage swing of the output voltage results in reduced voltage harmonics [32, 76, 77]. Therefore, the conducted emissions are significantly reduced, which lowers the risk of unwanted electromagnetic inferences and, inherently, reduces the required EMI filter size or the required shielding efforts.
- **Fault tolerance:** Due to the modular battery and converter structure, the drivetrain can cope with certain inverter or battery faults. Thus, in case of a permanent fault, the drivetrain can be further operated with a reduced current quality or a constrained output power without requiring road side assistance [74, 78].
- **Extended battery life time:** The battery packs can be drained by their individual capacity and, thus, the charge of the battery system can be fully utilized [79]. Individually, faster degraded battery packs (SOH < 80 %) do not act as bottlenecks and these can be easily replaced or bypassed during operation.
- **Advanced battery balancing techniques:** Through the proper selection of redundant voltage vectors or the injection of zero sequence currents, the battery packs can be efficiently balanced without wasting any charge [31, 79,

80]. Moreover, different battery chemistries or types can be combined in one battery system [69].

- **Reduced life cycle costs:** The application of low-voltage Si MOSFETs in comparison to IGBTs significantly reduces the inverter cost and the modular structure allows the inverter to fulfill functions of the BMS [37, 81]. Furthermore, individual battery packs can be safely (due the low voltage levels) replaced or maintained throughout the entire life time.
- **Safety extra-low voltage and protection:** The individual battery modules can satisfy existing protective low voltage requirements (DC; $<60\,\mathrm{V}$) and, therefore, pose a low risk for dangerous electric shock [81]. With the help of only one additional battery relay (semiconductor switch) per battery module, the inverter can all-pole disconnect/bypass individual battery modules and standard, low-voltage fuses can be utilized for the protection against external short-circuit and overcurrent faults [82].

The disadvantages of MLIs employing a modular battery system in comparison to two-level inverter drivetrains can be shortly summarized as follows:

- **Increased system complexity:** Due to the increased number of semiconductor switches, the number of the required gate signals is increased as well. Consequently, it becomes quite challenging to properly implement a synchronous current control approach [83].
- **Increased ohmic battery losses:** The battery packs in a modular battery system are subject to low-order current harmonics. These cause increased ohmic losses in the battery system in comparison to a two-level inverter drive [84–86].

The following sections of this chapter give an overview about the MLI topologies, and their basic switching configurations, considered in this thesis. Primarily, the active three-level neutral point clamped (ANPC) inverter and different variants of cascaded MLIs are considered.

3.1 Three-Level Neutral Point Clamped Inverter

The three-level NPC inverter was first introduced in 1981 [87], which is nowadays referred to as I-type NPC inverter. Since the number of required semiconductor switches exponentially increases with the number of output voltage levels, NPC inverters with more than three output voltage levels are rarely found [88, 89].

The neutral point potential of the three-level NPC inverter is usually formed by a capacitive voltage divider, as schematically shown in Fig. 3.2(a). An unbalance between the dc-link voltages, caused by the drawn low-order harmonics including the dominant third harmonic [90], should be mitigated [91, 92], especially at low speeds. For example, a high torque demand at low-speed operation (e.g., climbing

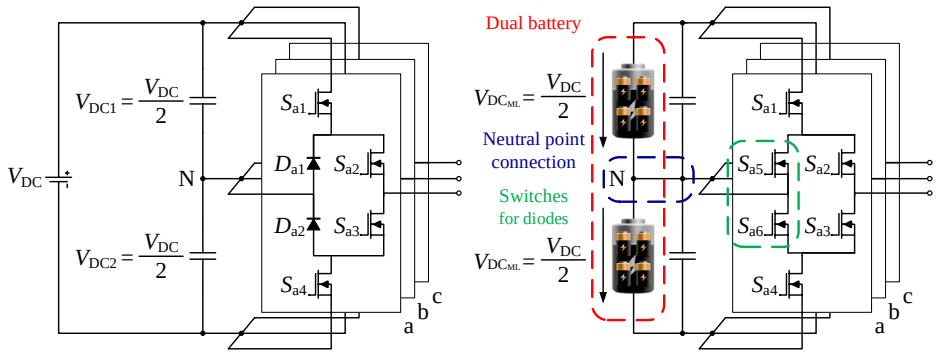


Figure 3.2: Three-level NPC inverter with (a) capacitive voltage divider and (b) dual battery pack with additional neutral point connection, including MOSFETs in the clamping paths (active).

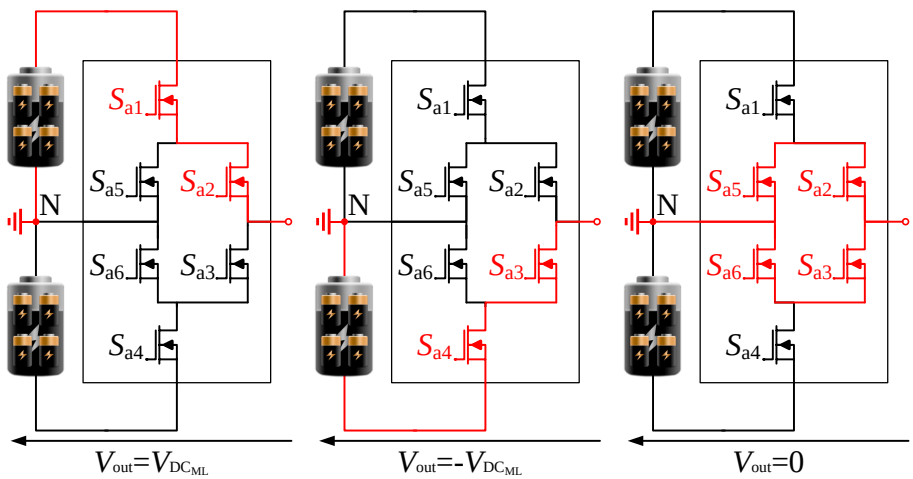


Figure 3.3: Valid switching state combinations for each phase of the NPC inverter, achieving (a) positive, (b) negative and (c) zero output voltage level.

a curb) can quickly drain one capacitor while charging the other capacitor to the full DC link voltage V_{DC}. In contrast, the fault-tolerant three-level NPC inverter [78], as shown in Fig. 3.2(b), utilizes a dual battery system with an additional neutral point connection. Thus, the capacitor voltages are clamped to the batteries' potentials and the low order harmonic currents at low speed are conducted through the battery packs, resulting in slightly increased ohmic battery losses. This NPC variant would be a favorable choice for a vehicle application. Fig. 3.3 depicts the valid switching states of the active neutral point clamped inverter. Similar to the normal NPC inverter, the switches are operated in pairs, but for the active NPC inverter the additional switches/MOSFETs in the clamping path should be activated during the zero state. If three switches in series, such as S_{a1}, S_{a2} and S_{a3}, or an outer switch and a series connected clamping switch, such as S_{a1} and S_{a5}, are simultaneously activated, a shoot-trough fault is caused. With the help of the phase's switching state expression

$$S_{\mathrm{a,NPC}} = \{1, 0, -1\} = S_{\mathrm{a1}} S_{\mathrm{a2}} - S_{\mathrm{a3}} S_{\mathrm{a4}} \tag{3.1}$$

the instantaneous phase voltage of phase a v_{aN} can be described as

$$v_{\mathrm{aN}} = S_{\mathrm{a,NPC}} V_{\mathrm{DC_{ML}}} \quad . \tag{3.2}$$

Correspondingly, Fig. 3.4 depicts the possible output voltage levels of the three-level NPC inverter considering the configuration of the individual battery packs.

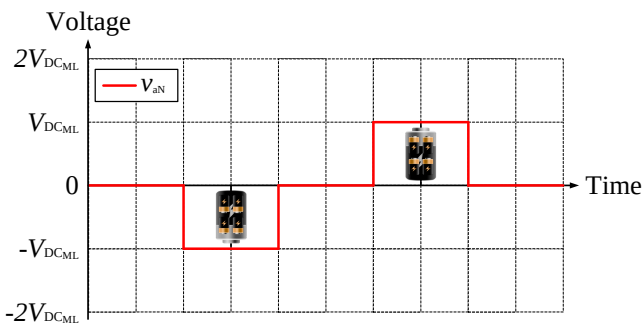


Figure 3.4: Possible phase output voltage levels and battery module configurations for a three-level NPC inverter.

3.2 Cascaded Multilevel Inverter Types

Another type of multilevel inverters utilizes a cascaded three-phase structure with a single star arrangement, as schematically depicted in Fig. 3.5. Cascaded inverters

consist of series connected sub-modules (SM) containing an energy storage element equipped with an individual power electronics converter. Depending on the used converter type, a single pole (black solid lines) or a double pole connection (red dotted lines) between adjacent modules is utilized, as illustrated in Fig. 3.5. Using a single pole connection type structure, the individual energy storages can be inserted in the corresponding phase strand or these can be bypassed. In addition, the double pole connection in comparison to the single pole connection allows to parallel adjacent energy storages to reduce the equivalent Thevenin impedance of the phase strand's energy storages. It should be noted that the parallel operation can lead to circulating currents between the energy storages, which should be taken into account when selecting the semiconductor switches [93, 94]. Nonetheless, the circulating currents can possibly be utilized for advanced battery diagnostics [95] or for the SOC balancing of the individual energy storages [69]. The phase voltage $v_{\mathrm{ph,x}} = v_{x\mathrm{N}}$ with $x = \{\mathrm{a}, \mathrm{b}, \mathrm{c}\}$ of an arbitrary number of n SMs can be described as the sum of the SMs' output voltages according to

$$v_{\mathrm{ph},x} = v_{x\mathrm{N}} = \sum_{j=1}^{n} V_{\mathrm{out},j} \quad . \tag{3.3}$$

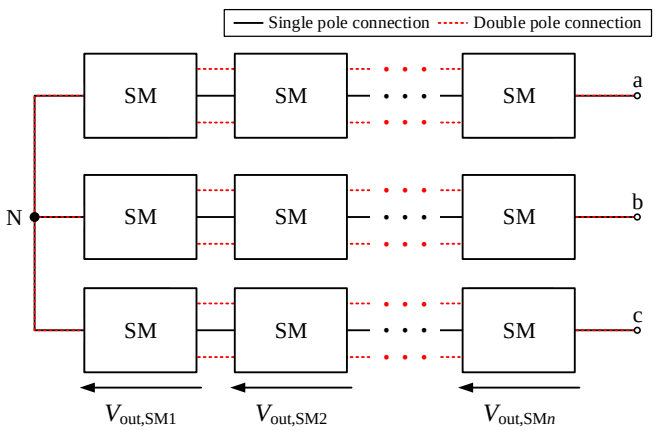


Figure 3.5: Schematic structure of three-phase cascaded multilevel inverters with single or double pole connection type between adjacent sub-modules.

In the following subsections, the basic switching combinations of various cascaded converter types with different SM converters are described and illustrated.

3.2.1 Cascaded H-bridge Inverter

The cascaded H-bridge (CHB) converter was probably first introduced in 1992 [96]. When used for a modular vehicle battery system, it utilizes an H-bridge converter for each individual battery module, achieving a simple single pole connection between adjacent modules [34]. The switches are operated in pairs, whereas only one switch per half-bridge should be activated. Therefore, there are four valid switching state combinations, as illustrated in Fig. 3.6. As can be seen, the energy storage can be inserted in forward or reverse direction into the phase strand or, alternatively, it can be bypassed. Consequently, the output voltage V_{out} of the j-th H-bridge module can be expressed in terms of the module's switching state combination according to

$$V_{\text{out},j} = \{+V_{\text{DC}_{\text{ML}}}, 0, -V_{\text{DC}_{\text{ML}}}\} = S_{\text{HB}j} V_{\text{DC}_{\text{ML}}} \tag{3.4}$$

with the H-bridge's switching state combination $S_{\text{HB}j}$ expressed as

$$S_{\text{HB}j} = \{+1, 0, -1\} = S_{2,\text{HB}j} S_{3,\text{HB}j} - S_{1,\text{HB}j} S_{4,\text{HB}j} \quad . \tag{3.5}$$

A CHB inverter with n SMs per phase can achieve L output levels according to

$$L = 2n + 1 \quad . \tag{3.6}$$

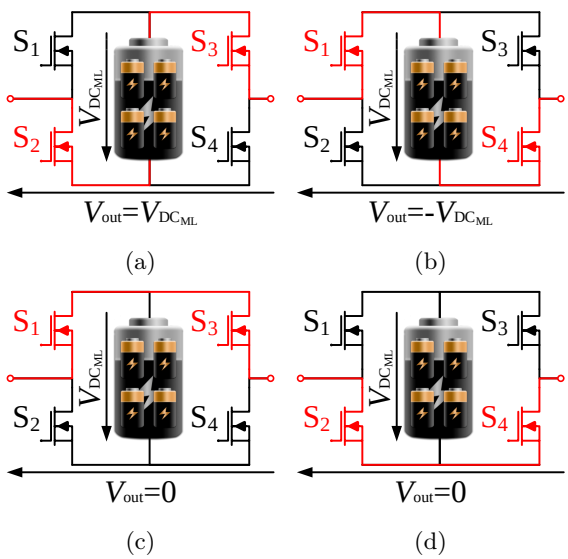


Figure 3.6: Valid switching state combinations of each individual H-bridge converter. In (a) and (b) the battery module is inserted in forward and reverse direction, respectively. In (c) and (d) the battery module is bypassed.

The possible phase output voltage levels, including the configurations of the battery modules, for two SMs per phase ($n = 2$) are depicted in Fig. 3.7. As can be seen, the phase voltage can attain positive and negative output voltage levels.

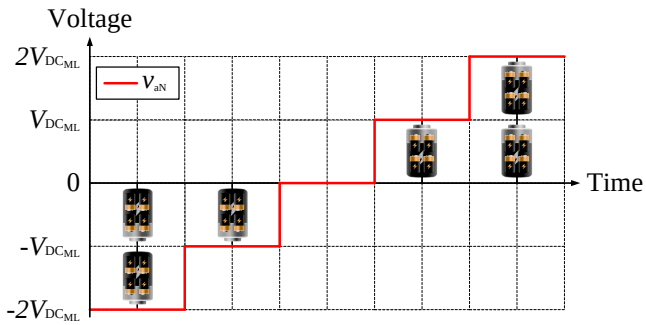


Figure 3.7: Possible phase output voltage levels and battery module configurations for a CHB inverter with two SMs per phase, $n = 2$.

3.2.2 Cascaded Semi-H-Bridge Inverter

In [97], the authors have introduced a reconfigurable battery storage system based on a three-switch converter module that allows to dynamically connecting adjacent battery modules in series or in parallel. Additionally, individual battery modules can be bypassed. As described in [97], this topology is referred to as a battery modular multilevel management system (BM3), which is intended to balance the battery cells' charges and to adjust the battery pack's DC voltage level. Nonetheless, as described in [97], the BM3 topology requires an additional, designated inverter when used for variable speed drive or grid-tied applications. In [98] the authors have used the same three-switch module, referred to as semi-full-bridge module in [98], for the converter arms' sub-modules of a classical modular multilevel converter. In contrast to [97], the authors of [99] were the first who described how to employ the semi-full-bridge/BM3 (three-switch) module to form a cascaded inverter with two-pole connections between adjacent SMs. Using this approach, the inverter modules can be used to balance the individual battery packs and to generate a sinusoidal phase output voltage. Hereinafter, this inverter topology is referred to as cascaded semi-H-bridge (CSHB) converter. As before mentioned, each SHB module can be operated with three valid switching state combinations, as illustrated in Fig. 3.8. The output voltage V_{out} of the j-th semi-H-bridge module can be expressed in terms of the module's switching state

combination according to

$$V_{\text{out},j} = \{+V_{\text{DC}_{\text{ML}}}, 0\} = S_{\text{SHB}j} V_{\text{DC}_{\text{ML}}} \tag{3.7}$$

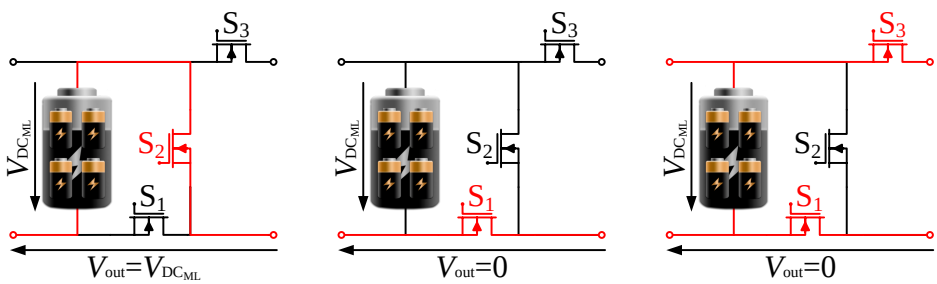
with the semi-H-bridge's switching state combination $S_{\text{SHB}j}$ expressed as

$$S_{\text{SHB}j} = \{1, 0\} = S_{2,\text{SHB}j} \quad . \tag{3.8}$$

When connecting n CSHB SMs per phase strand to form a cascaded inverter topology, the upper pole of the first and the last SM should be left unconnected, as schematically shown in Fig. 3.5. A detailed illustration of the strand connections of the SMs can also be found in [99]. A CSHB inverter with n SMs per phase can achieve L output levels according to

$$L = n + 1 \quad . \tag{3.9}$$

As earlier described, paralleling adjacent battery modules result in the same zero output voltage as with the bypass operation. However, when parallel connecting adjacent battery modules, the phase strand's battery impedance is reduced and, thus, the ohmic battery losses are reduced as well. In particular, the ohmic battery losses when operated at low modulation indices can be significantly reduced. The possible phase output voltage levels, including the configurations of the battery modules, for two SMs per phase strand ($n = 2$) are depicted in Fig. 3.9. As can be seen, the phase voltage levels can only be positive. Therefore, as described in [99], a zero sequence voltage must be injected into each phase to create a rotating three-phase voltage.



(a) (b) (c)

Figure 3.8: Valid switching state combinations of each individual semi-H-bridge converter module. In (a) the battery module is inserted in forward direction. In (b) the battery module is bypassed and in (c) the battery module is connected in parallel to the adjacent battery module.

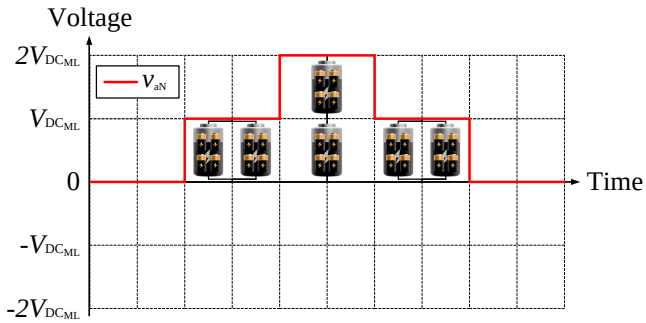


Figure 3.9: Possible phase output voltage levels and battery module configurations for a CSHB inverter with two SMs per phase, $n = 2$.

3.2.3 Cascaded Double-H-Bridge Inverter

In addition to the before mentioned CHB and CSHB inverter topologies, the authors of [100] were the first to suggest a more advanced, cascaded multilevel inverter topology with bypass, parallel and series connectivity, including positive and negative output voltage polarity. In [100], this topology is referred to as modular multilevel series/parallel converter (M2SPC). However, in contrast, the authors of [36,84] abbreviated this converter name as MMSPC, modular multilevel series parallel converter. In extension to the CHB converter topology, the M2SPC topology utilizes two H-bridge converters per SM. Hence, in accordance with Fig. 3.5, the individual SMs form two-pole connections between adjacent SMs, which is similar to the CSHB inverter topology. Hereinafter, the M2SPC topology is referred to as cascaded double-H-bridge (CDHB) converter, which is in accordance with the terminology of the before described CHB and CSHB inverter topology. Each SM of the CDHB inverter can be operated with six valid switching state combinations, as illustrated in Fig. 3.10. The output voltage V_{out} of the j-th double-H-bridge module can be expressed in terms of the module's switching state combination according to

$$V_{\mathrm{out},j} = \{+V_{\mathrm{DC_{ML}}}, 0, -V_{\mathrm{DC_{ML}}}\} = S_{\mathrm{DHB}j} V_{\mathrm{DC_{ML}}} \tag{3.10}$$

with the double-H-bridge's switching state combination $S_{\mathrm{DHB}j}$ expressed as

$$S_{\mathrm{DHB}j} = \{1, 0, -1\} \tag{3.11}$$

which corresponds to

$$S_{\mathrm{DHB}j} = S_{2,\mathrm{DHB}j} S_{4,\mathrm{DHB}j} S_{5,\mathrm{DHB}j} S_{7,\mathrm{DHB}j} - S_{1,\mathrm{DHB}j} S_{3,\mathrm{DHB}j} S_{6,\mathrm{DHB}j} S_{8,\mathrm{DHB}j} \quad . \tag{3.12}$$

When connecting n CDHB SMs per phase strand to form a cascaded inverter topology, one half-bridge of the first and the last SMs' poles should be left unconnected, as schematically shown in Fig. 3.5. A detailed illustration of the strand connection of SMs can also be found in [84]. A CDHB inverter with n SMs per phase can achieve L output levels according to

$$L = 2n + 1 \quad . \tag{3.13}$$

The possible phase output voltage levels, including the configurations of the battery modules, for two SMs per phase strand ($n = 2$) are depicted in Fig. 3.11. As can

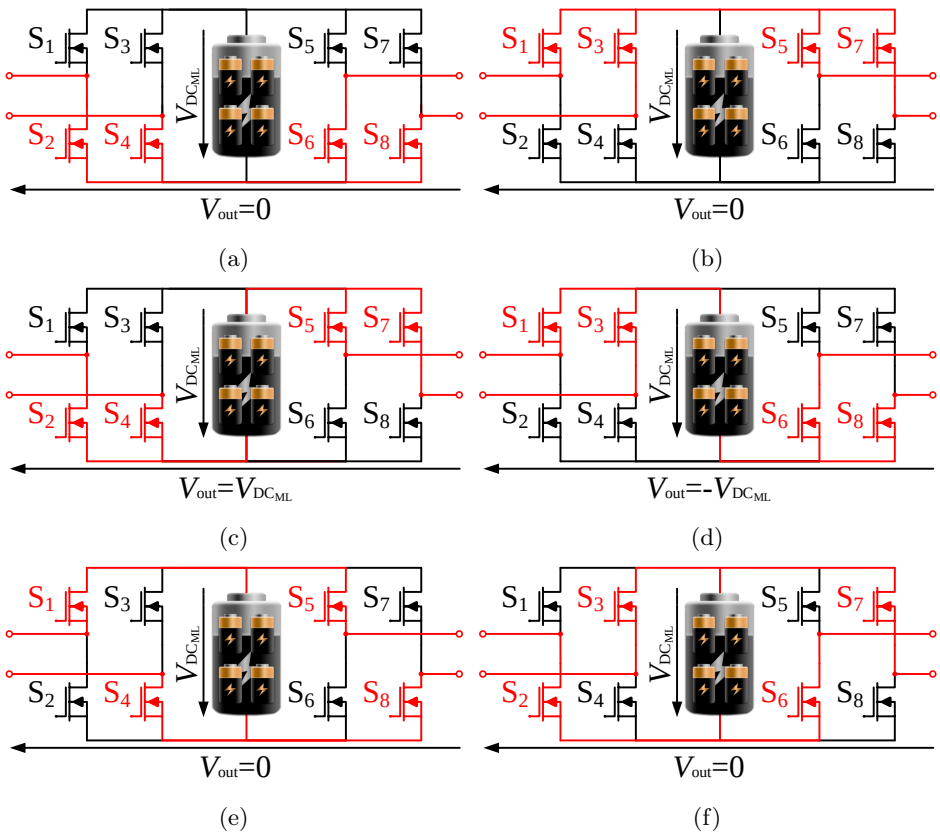


Figure 3.10: Valid switching state combinations of each individual double-H-bridge converter module. In (a) and (b) the battery module is bypassed. In (c) and (d) the battery module is inserted in forward and reverse direction, respectively. In (e) and (f) the battery module is connected in parallel to the adjacent battery module.

be seen, the phase voltage can be of positive and negative polarity and the battery packs can be connected in parallel for both output voltage polarities $V_{\text{out}} = V_{\text{DC}_{\text{ML}}}$ and $V_{\text{out}} = -V_{\text{DC}_{\text{ML}}}$.

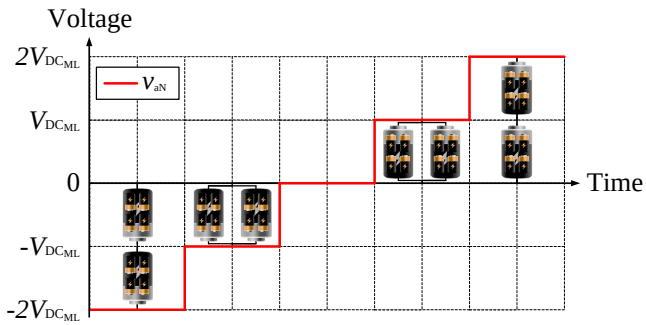


Figure 3.11: Possible phase output voltage levels and battery module configurations for a CDHB inverter with two SMs per phase, $n = 2$.

Drive Cycle Efficiency

As claimed in [37], multilevel inverters based on cheap, low-voltage MOSFETs can increase the overall drive cycle efficiency in comparison to similar apparent-power-rated two-level IGBT or SiC inverters for vehicle propulsion. However, in [37], the ohmic battery losses are totally neglected. Thus, the question arises: is the claim in [37] about the efficiency enhancement still valid when taking the ohmic battery losses into account?

This chapter shows a fair comparison of the drive cycle efficiencies between a two-level, a seven-level CHB and a seven-level CDHB inverter when used in a small passenger car with a nominal battery capacity of about 45 kWh. Additionally, a hybrid modulation technique, reducing the drive cycle losses and the inverter-induced current ripple, for a seven-level CHB is suggested.

Both the battery and the inverter losses are considered and a detailed description about their modeling is given. For MOSFET inverters with low switching frequencies ($f_{\mathrm{sw}} < 20\,\mathrm{kHz}$), the conduction losses are typically dominant. Thus, the conduction losses must be properly modeled considering the third quadrant characteristic of the used MOSFETs. Furthermore, since the battery packs are subject to a large number of low order harmonics, a dynamic battery model is required to comparatively model the ohmic battery losses.

The results and scientific contributions presented in this chapter are based on Paper I [101], Paper IV [102], Paper V [86], Paper VII [84], Paper VIII [103], Paper XI [104], Paper XIV [85], Paper XVII [105] and Paper XVIII [106].

4.1 Conduction Loss Modeling of MOSFETs

To calculate or simulate the conduction losses of a three-phase, two-level inverter, different analytical models can be found in [107–110] or in suppliers' application manuals [111, 112]. These can be typically used for IGBT inverters, but are not suitable for MOSFET inverters. This is due to the fact that the mentioned literature [107–112] does not properly consider the conduction losses in the third quadrant of MOSFET's voltage-current characteristic. As described in [105], Fig. 4.1 depicts the forward voltage drop V_{DS} of a silicon carbide MOSFET (SiC module 1.2 kV/ 50 A CCS050M12CM2 from Cree Wolfspeed [113]) relative the drain current I_{DS}. As can be seen, in the first quadrant (I), the forward voltage drop follows a restive behavior according to the MOSFET's on-state resistance R_{on}. Considering the depicted part of the third quadrant (III) characteristic, the forward voltage follows either a restive or a diode voltage drop depending on the gate voltage V_{GS}. This is due to the fact that the MOSFET is a majority carrier device, which can conduct in the reverse direction when being turned on. Furthermore, as described in [105], if the voltage drop across the MOSEFT's

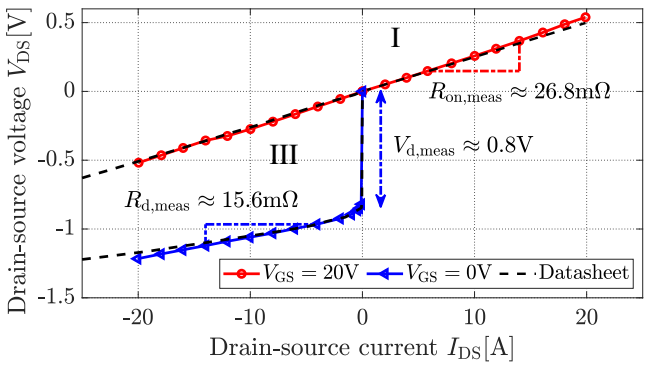


Figure 4.1: Measured MOSFET and diode characteristic of the chosen SiC MOSFET inverter [113], including the reverse conduction of the MOSFET channel.

channel exceeds the diode voltage drop according to

$$|I_{\mathrm{DS}} R_{\mathrm{on}}| \geq |V_{\mathrm{d}}| \rightarrow I_{\mathrm{DS}} \leq -\frac{V_{\mathrm{d}}}{R_{\mathrm{on}}} \tag{4.1}$$

both the antiparallel diode and the MOSFET channel conduct in parallel. Since both the reverse conduction and the parallel conduction of the antiparallel diode and the MOSFET's channel are inherently utilized for all types of MOSFET converters, the forward voltage drop and, thus, the conduction losses ($P_{\mathrm{cond}} = V_{\mathrm{DS}} I_{\mathrm{DS}}$)

can be described for three different intervals depending on the drain-source current I_{DS}. In the first quadrant (I), the MOSFET's current I_{T} and the diode's current I_{D} can be described relative to the drain-source current I_{DS} according to

$$I_{\mathrm{T}} = I_{\mathrm{DS}} \quad \text{for} \quad I_{\mathrm{DS}} \geq 0 \tag{4.2}$$

and

$$I_{\mathrm{D}} = 0 \quad \text{for} \quad I_{\mathrm{DS}} \geq 0 \quad . \tag{4.3}$$

Therefore, the device's forward voltage drop becomes

$$V_{\mathrm{DS}} = I_{\mathrm{DS}} R_{\mathrm{on}} \quad \text{for} \quad I_{\mathrm{DS}} \geq 0 \quad . \tag{4.4}$$

Considering only the reverse conduction interval of the MOSFET in the third quadrant (III), the MOSFET's current I_{T} and the diode's current I_{D} can be described relative to the drain-source current I_{DS} according to

$$I_{\mathrm{T}} = I_{\mathrm{DS}} \quad \text{for} \quad -\frac{V_{\mathrm{D}}}{R_{\mathrm{on}}} \geq I_{\mathrm{DS}} < 0 \tag{4.5}$$

and

$$I_{\mathrm{D}} = 0 \quad \text{for} \quad -\frac{V_{\mathrm{D}}}{R_{\mathrm{on}}} \geq I_{\mathrm{DS}} < 0 \quad . \tag{4.6}$$

Thus, the device's forward voltage drop becomes

$$V_{\mathrm{DS}} = I_{\mathrm{DS}} R_{\mathrm{on}} \quad \text{for} \quad -\frac{V_{\mathrm{D}}}{R_{\mathrm{on}}} \geq I_{\mathrm{DS}} < 0 \quad . \tag{4.7}$$

Considering the parallel conduction interval of the MOSFET and the diode in the third quadrant (III) according to [105], the MOSFET's current I_{T} and the diode's current I_{D} can be described relative to the drain-source current I_{DS} according to

$$I_{\mathrm{T}} = \frac{R_{\mathrm{d}} I_{\mathrm{DS}} - V_{\mathrm{d}}}{R_{\mathrm{d}} + R_{\mathrm{on}}} \quad \text{for} \quad I_{\mathrm{DS}} < -\frac{V_{\mathrm{D}}}{R_{\mathrm{on}}} \tag{4.8}$$

and

$$I_{\mathrm{D}} = -\frac{R_{\mathrm{on}} I_{\mathrm{DS}} + V_{\mathrm{d}}}{R_{\mathrm{d}} + R_{\mathrm{on}}} \quad \text{for} \quad I_{\mathrm{DS}} < -\frac{V_{\mathrm{D}}}{R_{\mathrm{on}}} \tag{4.9}$$

with

$$I_{\mathrm{T}} - I_{\mathrm{D}} = I_{\mathrm{DS}} \quad . \tag{4.10}$$

Therefore, during the parallel conduction interval, the device's voltage drop becomes

$$V_{\mathrm{DS}} = \frac{R_{\mathrm{d}} I_{\mathrm{DS}} - V_{\mathrm{d}}}{R_{\mathrm{d}} + R_{\mathrm{on}}} R_{\mathrm{on}} \quad \text{for} \quad I_{\mathrm{DS}} < -\frac{V_{\mathrm{D}}}{R_{\mathrm{on}}} \quad . \tag{4.11}$$

With the help of (4.2) to (4.11), the instantaneous conduction loss can be calculated according to

$$P_{\text{cond}} = I_{\text{DS}} V_{\text{DS}} \quad . \tag{4.12}$$

Using a lookup table approach, as for example used by Plexim's PLECS software, the conduction losses for different MOSFET inverters can be easily simulated.

Fig. 4.2 depicts the overestimation of the conduction losses when using the proposed method in [111] in comparison to when considering the reverse conduction of the MOSFET and the parallel conduction of the MOSFET and the antiparallel diode for a three-phase, two-level inverter [113]. The relative overestimation of the conduction losses is depicted relative to the modulation index M and the displacement power factor (DPF) angle φ for different output current amplitudes. As can be seen, the relative differences become smaller for

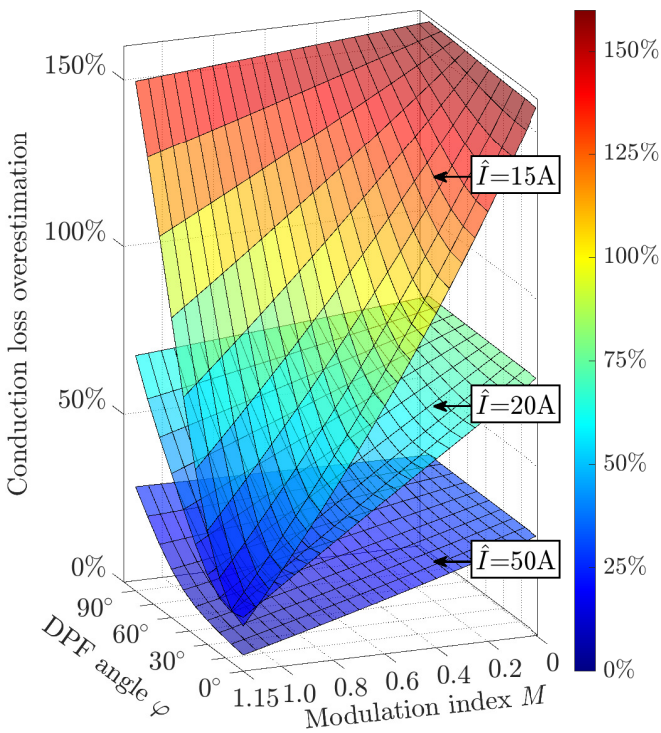


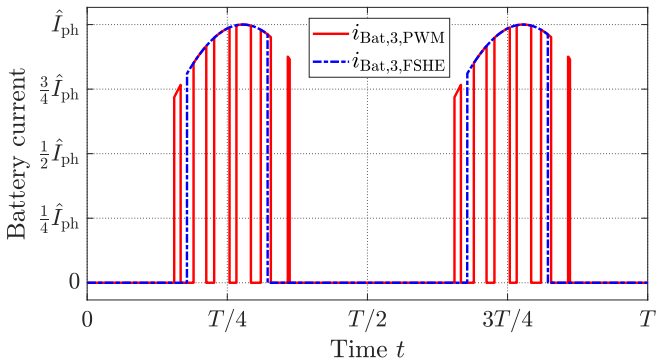
Figure 4.2: Overestimation of the conduction losses when using the method described in Semikron's application manual [111] in comparison to the presented method in [105] for the three-phase, two-level SiC MOSFET inverter of Cree Wolfspeed [113].

larger current amplitudes. For a certain current amplitude, the overestimation becomes the highest at low modulation index and pure inductive DPF and the lowest at a high modulation index and unity DPF. For the depicted current amplitudes of 15 A and 50 A, the relative overestimation varies from 13.5 % to 159.3 % and 4.9 % to 29.8 %, respectively. Consequently, this indicates that the method in [111], which is suitable for IGBT inverters, significantly overestimates the losses of a MOSFET inverter operated at partial load.

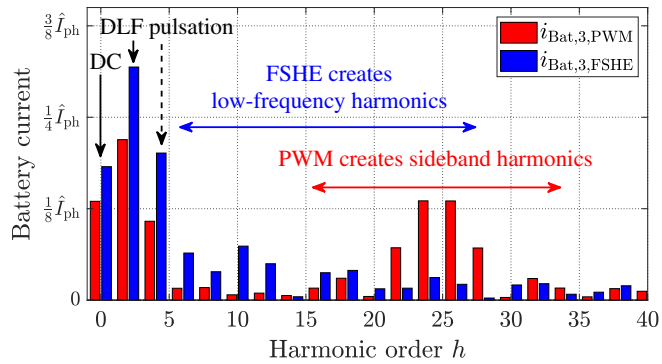
4.2 Dynamic Modeling of Ohmic Battery Losses

The battery packs in an MLI are stressed with strong current pulses ranging from DC up to a couple of kHz. For example, Fig. 4.3(a) shows the current drawn from one of the battery packs (3 → shortest insertion time) of a seven-level CHB inverter when operating the inverter with multilevel PWM and with fundamental selective harmonic elimination (FSHE). The chosen modulation index is about $M = 0.9$ and the carrier ratio is $m_\mathrm{f} = 40$ (PWM). The corresponding harmonic components of the drawn battery current using multilevel PWM and FSHE are depicted in Fig. 4.3(b). As can be seen, the second harmonic component, for single phase converters referred to as double line frequency (DLF) pulsation [114], is dominant for both multilevel PWM and FSHE. Due to the intermittent rectification of the phase current, the fourth harmonic is notably pronounced as well. Comparing the distinct harmonics, multilevel PWM typically creates side band harmonics around multiples of the switching frequency f_sw, whereas FSHE creates a series of low-frequency harmonics. It has been controversially discussed whether these current harmonics cause an additional rapid aging of the battery cells, but this controversy has been proven wrong, except for the increased RMS current [115–117]. Nonetheless, the question arises how to properly model the battery losses of an MLI with respect to a similar dimensioned two-level inverter?

In a BEV, independent of the inverter topology, the battery cells are subjected to a DC component, which slowly varies while driving. On the one hand, the switching events of a two-level inverter additionally generate a high-frequency current ripple ($\geq 10\,\mathrm{kHz}$), which is easily filtered out by the DC-link capacitor [118, 119]. Hence, for energy calculations, the battery is often just modeled as a simple resistor [120–123]. On the other hand, as described in [86], the low order battery current harmonics of an MLI cannot be filtered out that easily. Thus, a dynamic battery model is required to allow for accurate energy calculations. Several battery equivalent circuit models can be found in literature [124–127]. The general conclusion is that the simplified Randles model, as shown in Fig. 4.4 with



(a)



(b)

Figure 4.3: (a) Drained battery currents for one battery pack of a seven-level CHB inverter when using multilevel PWM and FSHE for a modulation index $M = 0.9$ and a carrier ratio of $m_{\mathrm{f}} = 40$ (PWM). (b) Corresponding harmonic components.

three RC-pairs and without a Warburg impedance element, adequately describes the battery dynamics and the ohmic battery losses. The battery cell is modeled by an RC-network. One to three time constants, represented by R_1 to R_3 and C_1 to C_3, are used to describe the transient battery behavior. The resistance R_0 represents the internal battery resistance. The open circuit voltage V_{OCV} is dependent on the State of Charge (SOC). Considering the high frequency behavior, the modeled series inductance L is required. As illustrated in Fig. 4.4, the DC, low-frequency (LF) and high-frequency (HF) components are conducted through different paths. For example, when using simulations, the ohmic battery losses

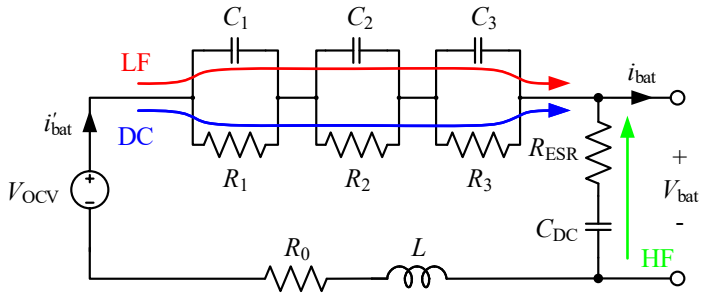


Figure 4.4: Simplified Randles model of a battery pack, using three time constants, including the DC-link capacitor.

using three time constants can be estimated according to

$$P_{\text{bat,loss}} = \sum_{j=0}^{3} R_j i_{R_j}^2 + R_{\text{ESR}} i_{R_{\text{ESR}}}^2 \quad . \tag{4.13}$$

In [85], the measured ohmic battery losses of a small-scale, laboratory CHB inverter, representing a seven-level CHB propulsion inverter used in a small passenger vehicle, are compared with simulations. For the simulations, varied specification detail of the simplified Randles model, with up to three *RC*-pairs, and a pure restive are used. Fig. 4.5 depicts the obtained loss comparison from [85] for six characteristic operating points (OP) of the small passenger vehicle. A detailed description of the OPs can be found in [85]. On the one hand, it can be seen that the dynamic models with two to three RC-pairs show a very good agreement with the measurements. On the other hand, it can be seen that the dynamic model with one *RC*-link and the resistive model overestimate the losses by about 10 % and 20 %, respectively. Considering the EIS-extracted model (using three *RC*-pairs), the losses are generally underestimated, while the operating points at higher frequencies (OP4 to OP6) agree better with the measurements than the ones at low frequency (OP1 to OP3). From the loss results it can be seen that the dynamic model is the most accurate one for five of the six operating points, whereas the EIS model is the most suitable for OP6 at the highest chosen frequency.

Consequently, it can be stated that the selection of a simple battery model, for example a pure resistive model, might be suitable for energy calculations concerning a two-level inverter system. However, based on the shown loss comparison, it can be seen that a simple resistive model overestimates the ohmic battery losses in a CHB multilevel inverter by up to 20 %. Thus, when quantifying the

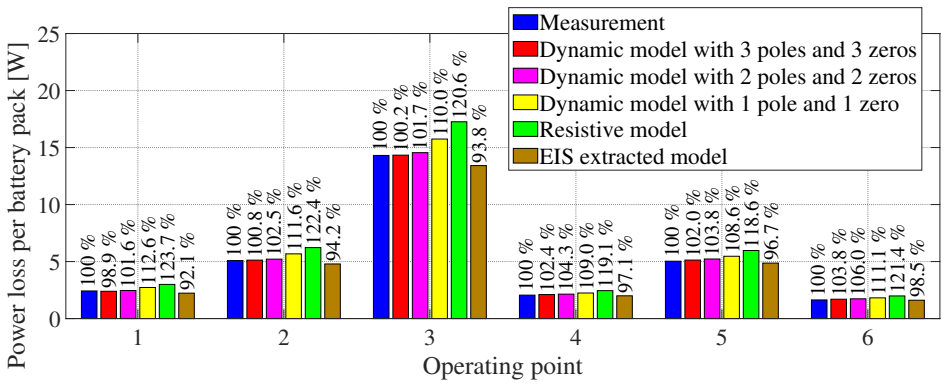


Figure 4.5: Loss comparison between measurements, different dynamic models and a pure resistive model of a small-scale CHB multilevel propulsion inverter. The six characteristic OPs can be described as follows: OP1: low speed and low torque; OP2: low speed and medium torque; OP3: low speed and high torque; OP4: medium speed and low torque; OP5: medium speed and medium torque; OP6: high speed and low torque.

ohmic battery losses of a multilevel inverter or when performing energy efficiency comparisons between two-level and multilevel inverters, a dynamic battery model with two or, preferably, three *RC*-pairs should be chosen.

4.3 Drive Cycle Efficiency of Seven-Level CHB and CDHB in Comparison to a Two-Level Inverter

The drive cycle losses of a seven-level CHB and CDHB inverter in comparison to a two-level IGBT inverter, when used in a small passenger car, are estimated using two main steps. At first, the losses of the inverter and the battery system are obtained for the broad speed-torque range of the small passenger car using simulations. Next, using a quasi steady state assumption, the losses corresponding to each operating point of the vehicle are determined, using the previously obtained loss matrices, by a lookup table approach.

The chosen reference car has a curb weight of $m_{\mathrm{veh}} = 1500\,\mathrm{kg}$ and is driven by an 84 kW rated interior permanent magnet machine. The vehicle's and the motor's parameters can be found in Table A.1 in the Appendix. The battery system has a nominal capacity of 45 kWh, which is scaled based on the impedance of a cylindrical 18650 high energy cell, given in Table A.2, manufactured by

LG Chem. This battery cell has a nominal voltage of 3.72 V and a rated capacity of 2800 mAh, which corresponds to about 10.42 Wh [128]. Assuming a DC link voltage of $V_{\mathrm{DC}} = 400\,\mathrm{V}$ for the two-level inverter drivetrain results in a battery pack voltage of about $V_{\mathrm{DC_{ML}}} = 66.6\,\mathrm{V}$ for the seven-level CHB and CDHB inverters. Furthermore, each battery pack is equipped with a DC link capacitor. A more detailed description about the drivetrain and the sizing of the battery packs can be found in [84, 101].

The inverter losses are mainly modeled according to Infineon's application manuals [112, 129], whereas the MOSFET conduction losses are modeled according to the description found in Section 4.1. The inverters are operated with a switching frequency of $f_{\mathrm{sw}} = 10\,\mathrm{kHz}$ using space vector modulation. For the seven-level inverter, the multilevel space vector modulation approach implemented in [130] is used. For the determination of the battery losses a dynamic battery model with three *RC*-pairs is chosen. For the simulations, it is assumed that all battery packs are ideally balanced and, thus, no circulating currents [93, 94] are triggered during the parallel operation of the CDHB inverter's battery modules.

The chosen semiconductor switches for the two-level IGBT and the seven-level CHB and CDHB multilevel inverter drivetrains are presented in Table 4.1. The current rating of the chosen IGBT module ($I_{\mathrm{nom}} = 400\,\mathrm{A}$) is slightly higher in comparison to the chosen MOSFET ($I_{\mathrm{nom}} = 300\,\mathrm{A}$). Further, as can be seen, the cost for the MLI's semiconductor switches in comparison to the two-level IGBT inverter with a similar apparent power rating is significantly reduced from 341.54 € to 202.20 € and 121.32 € for the seven-level CHB and CDHB inverter, respectively. The costs for the additional gate drivers are presumably increased in comparison to a two-level inverter, but a modular battery system based on an MLI inherently acts as a part of the battery management system and individual modules can be used as low-voltage auxiliary supplies [73, 99]. Therefore, the MLIs are cost-effective solutions in comparison to a two-level IGBT inverter with a 400 V battery system.

Table 4.1: Chosen inverter semiconductor switches

Inverter	Switch	V_{blocking}	I_{nom}	N	PPU	Cost
2-level	FS400R07A3E3 [131]	700 V	400 A	6	341.54 €[1]	341.54 €
CHB	IPT015N10N5 [132]	100 V	300 A	36	3.37 €[2]	121.32 €
MMSP	IPT015N10N5 [132]	100 V	300 A	60	3.37 €[2]	202.20 €

[1] price for entire IGBT power module for purchase of at least 5 units
[2] price for purchase of at least 1000 units

4.3.1 Simulated Inverter and Battery Efficiency

The obtained inverter efficiency values for the two-level IGBT and the seven-level CHB and CDHB inverter can be seen in Fig. 4.6 for the vehicle's entire torque-speed range. For the obtained efficiency values, the junction temperatures of the semiconductor switches and the antiparallel diodes of the IGBTs were set to $T_\mathrm{J} = 70\,^\circ\mathrm{C}$. At standstill and very low speeds, the vehicle cannot beneficially

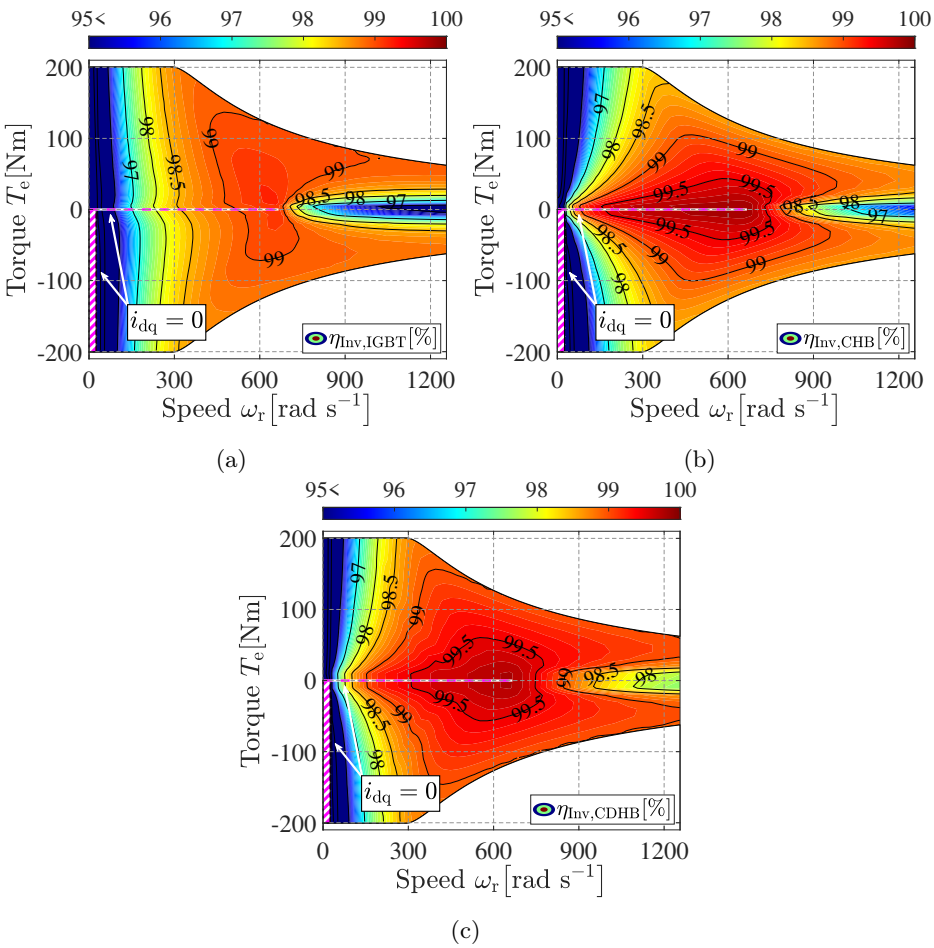


Figure 4.6: Simulated inverter efficiency for the entire torque-speed range of the vehicle's motor for (a) the two-level IGBT, (b) the seven-level CHB and (c) the seven-level CDHB inverter drivetrain for a constant junction temperature of $T_\mathrm{J} = 70^\circ$.

utilize regenerative braking and, thus, the inverter is inactive, emphasized by the vertical bar with magenta-colored hatching and the indication of the zero dq-currents $i_{\mathrm{dq}} = 0$. Further, when operating at low to medium speeds and zero torque, the dq-currents are zero as well, emphasized by the magenta dashed line. For both of these emphasized regions, no efficiency value can be obtained for the inverter and the battery system. As can be seen, both MOSFET multilevel inverters show a high efficiency at partial loading and low speed. Furthermore, their peak efficiency is increased in comparison to the IGBT two-level inverter

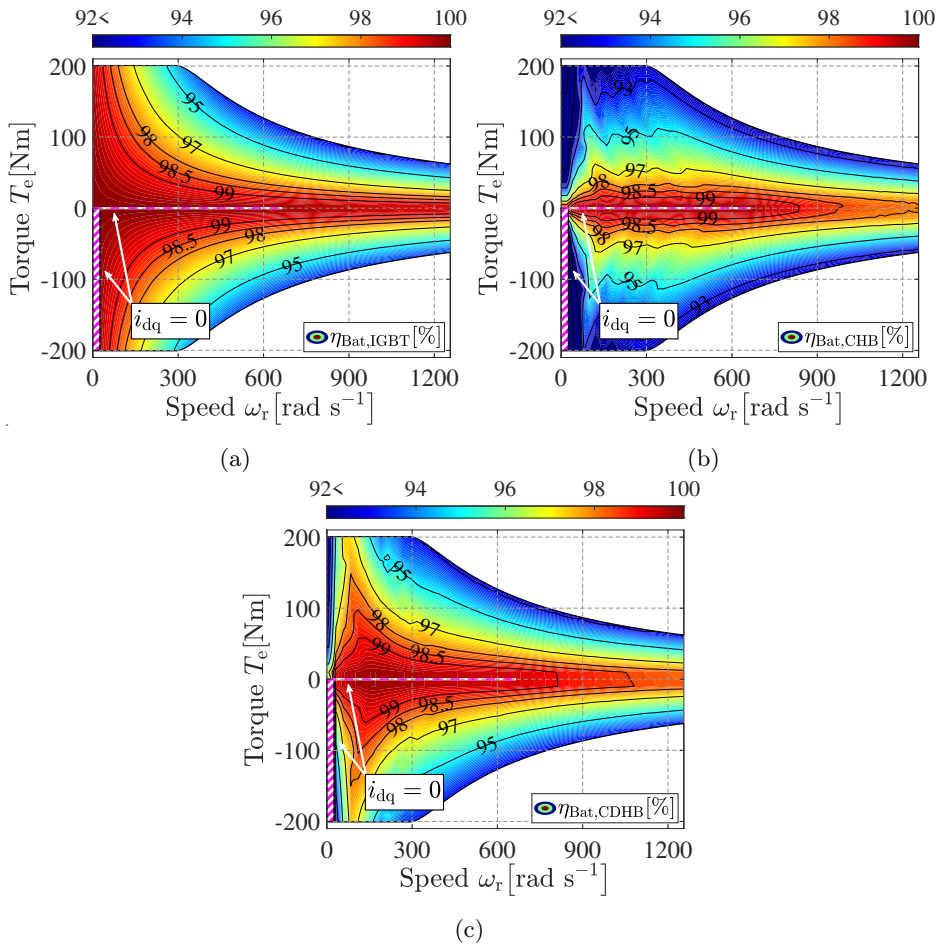


Figure 4.7: Simulated battery efficiency for the entire torque-speed range of the vehicle's motor for (a) the two-level IGBT, (b) the seven-level CHB and (c) the seven-level CDHB inverter drivetrain.

system.

The battery efficiency values for the three different drivetrains can be seen in Figure 4.7. Due to the large thermal time constant of the battery system and the short driving distance of each driving cycle, the influence of the battery's SOC and temperature is neglected. Similar to the inverter efficiency, no battery efficiency value can be obtained for the regions emphasized by the vertical bar with magenta-colored hatching and the magenta dashed line. As can be seen in Figure 4.7, the CHB inverter's battery system shows a decreased efficiency, especially below rated speed. Due to the fact that the motor currents are intermittently conducted through the battery packs, the battery packs are subject to a large amount of low order harmonic currents, which create additional ohmic losses. In comparison to the CHB inverter, the CDHB inverter reduces the battery losses, especially below rated speed. By paralleling adjacent battery modules in each phase strand for low output voltage levels, the CDHB inverter reduces the active battery impedance per phase strand in comparison the CHB inverter. Nonetheless, the CDHB inverter's battery losses at high speed are just marginally reduced in comparison to the CHB inverter. Since the active battery impedance per phase strand of the CHB and the CDHB inverter is varying with the modulation index M or the number of utilized output voltage levels, the isopotential lines of the efficiency values of the multilevel inverters are not as smooth as for the two-level inverter system. From the obtained efficiency values of the two-level inverter drive system, it can be seen that the two-level inverter shows the lowest battery losses at any operating point in comparison to the MOSFET multilevel inverters.

4.3.2 WLTP Drive Cycle Efficiency

Within this subsection, the obtained drive cycle results of the two-level IGBT and the seven-level CHB and CDHB inverter for the worldwide harmonized light vehicles test procedure (WLTP) are shown. The WLTP is a global standard for determining vehicles' emission values and fuel or energy consumption. Therefore, the operating points of the WLTP for the small passenger car, parameterized according to Table A.2 in the Appendix, are a good measure to compare the energy efficiency of the three different drivetrains.

The obtained inverter and battery losses for the two-level IGBT and the seven-level multilevel inverters can be seen in Figs. 4.8(a) and 4.8(b), simulated throughout the WLTP. For the inverter losses the feedback of the junction temperatures T_J, using a lumped parameter model as described in [84, 101], is considered. On the one hand, the two-level IGBT inverter shows the highest inverter losses, as

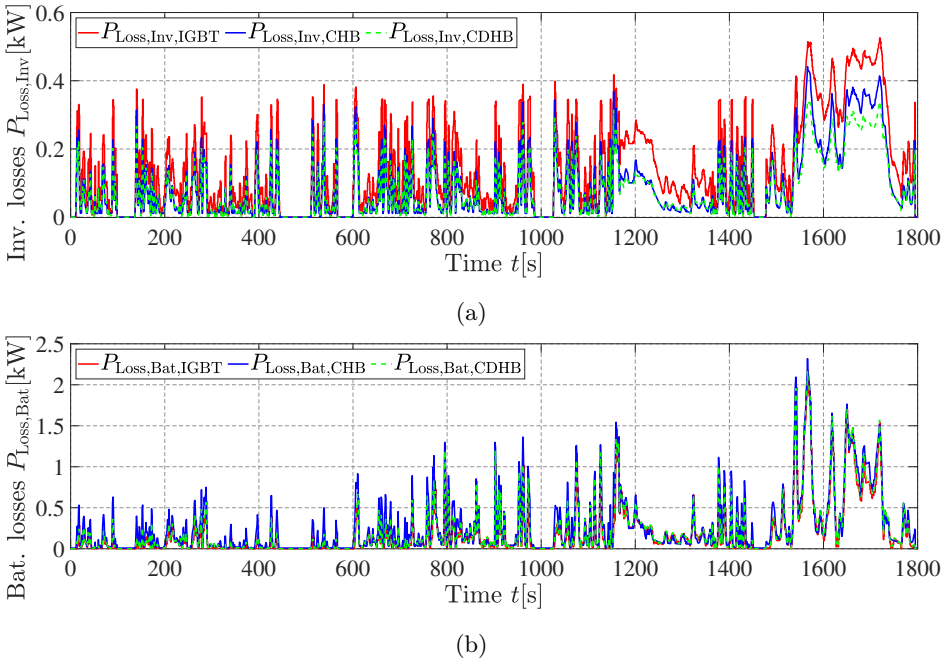


Figure 4.8: Simulated (a) inverter and (b) ohmic battery losses throughout the WLTP driving cycle for the three drivetrains.

can be seen in Fig. 4.8(a). The MOSFET multilevel inverters reduce the inverter losses, especially at partial load operation, which is similar to [133]. Furthermore, the CDHB inverter shows the lowest inverter losses. On the other hand, the two-level IGBT inverter system shows the lowest battery losses, as can be seen in Fig. 4.8(b). In comparison to the CHB inverter system, the CDHB inverter topology reduces the battery losses. However, the battery losses of both MOSFET multilevel inverter systems are increased in comparison to the two-level inverter topology.

The estimated junction temperatures of the semiconductor switches can be seen in Fig. 4.9. For the two-level IGBT inverter, the junction temperatures of the IGBTs and the antiparallel diodes are separately considered. As can be seen, the MOSFET junction temperatures of the CHB and the CDHB multilevel inverters are significantly reduced in comparison to the two-level IGBT inverter. Consequently, the junction temperatures' swings are reduced as well, which presumably result in a prolonged inverter life-time [134, 135].

The total energy losses, considering the inverter and the battery losses, of

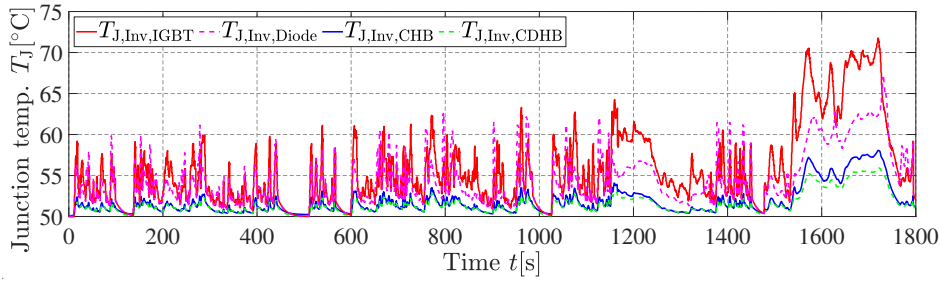


Figure 4.9: Estimated junction temperatures T_J of the semiconductor switches throughout the WLTP driving cycle .

Table 4.2: WLTP ($E_{Load} = 2.761\,kWh$) drive cycle evaluation of the two-level (IGBT), seven-level CHB and CDHB inverter

	Two-level (IGBT)	CHB	CDHB
Conduction losses E_{Cond}[kWh]	0.050	0.036	0.025
Switching losses E_{Sw}[kWh]	0.021	0.005	0.012
Inverter losses $E_{Loss,Inv}$[kWh]	0.071	0.041	0.037
Inverter efficiency η_{Inv}[%]	97.49	98.54	98.68
Battery losses $E_{Loss,Bat}$[kWh]	0.098	0.128	0.107
Battery efficiency η_{Bat}[%]	96.66	95.63	96.32
Overall losses $E_{Loss,Tot}$[kWh]	0.169	0.169	0.144
Overall efficiency η_{Tot}[%]	94.23	94.23	95.04

the three different drivetrains throughout the entire WLTP are given in Table 4.2. The simulated road load, including the gear box efficiency ($\approx 95\,\%$), of the WLTP for the small reference vehicle is about $E_{Load} = 2.761\,kWh$. The seven-level CDHB and CHB inverter show an improved inverter efficiency in comparison to the two-level IGBT inverter. As listed in Table 4.2, the inverters' conduction losses are dominant, especially for the MOSFET multilevel inverters. The CDHB inverter shows the highest inverter efficiency. However, as listed in Table 4.1, the CDHB inverter inherently employs more discrete semiconductor switches, for a similar inverter current rating, than the CHB inverter. Furthermore, as listed in Table 4.1, the CDHB inverter utilizes $N_{CDHB} = 60$ discrete MOSFETs, whereas the CHB inverter utilizes only $N_{CHB} = 36$ discrete MOSFETs. Therefore, when using a similar chip size area for the CHB inverter as for the CDHB inverter, the conduction losses of the CHB inverter would be presumably reduced by a factor according

$N_{\mathrm{CHB}}/N_{\mathrm{CDHB}}$, which corresponds to 0.6. Thus, using the similar chip size area as the CDHB inverter, the CHB inverter's conduction losses would be reduced to about 0.022 kWh. Assuming equal switching losses ($E_{\mathrm{Sw,CHB}} = E_{\mathrm{Sw,CDHB}}$) and using a similar chip size area, the CHB inverter's efficiency would be increased to about $\eta_{\mathrm{Inc,CHB}} = 98.78\,\%$. Consequently, the inverter efficiency of the CHB inverter would be marginally improved in comparison to the CDHB when using the same chip size area for both inverters. Considering the battery losses, it can be seen that the two-level inverter topology achieves the highest battery efficiency. The CDHB inverter reduces the battery losses in comparison to the CHB inverter, but the battery losses of the multilevel inverters are increased in comparison to the two-level inverter. Using a larger battery capacity or a battery cell type with a smaller impedance, the absolute energy loss difference between the three different drivetrains would be decreased [86]. Considering the combined/total drive cycle efficiency for the WLTP, it can be seen that the CDHB inverter achieves the best efficiency result. Furthermore, the CHB and the two-level inverter show the same total energy efficiency. Thus the CHB inverter is competitive with the chosen two-level IGBT inverter system.

In [84], a more detailed inverter comparison between the three drivetrains can be found, including three more driving cycles (NEDC, Artemis 130 and FTP-75). Nonetheless, the additional drive cycle results in [84] show a similar relation between the inverters as is presented here for the WLTP.

4.4 Hybrid Modulation of CHB Inverter

Besides multilevel PWM or space vector modulation (SVM) [32], fundamental frequency switching techniques as nearest-level control [72] or fundamental selective harmonic elimination (FSHE) [136] can be used to synthesize the desired output voltage. These reduce the switching losses, but induce low-order voltage harmonics. Thus, fundamental switching techniques do not seem suitable for low modulation indices, for example when operating at low speeds. Consequently, it might be beneficial to combine both SHE and PWM for EVs' broad torque-speed range. The authors of [31] were the first to suggest to use FSHE at higher speeds ($M >= 0.5$) and PWM at lower speeds ($M < 0.5$) to achieve an improved output current quality with reduced switching losses in comparison to using only PWM. Since the method in [31] describes how to balance the charges of the individual DC sources and the FSHE optimization problem (seven levels require three switching angles) can be easily solved, it seems very suitable for a CHB drivetrain with individual battery packs. However, no quantification/analysis of the reduced energy losses or

the improved current THD in comparison when using only PWM for the broad torque-speed range of a vehicle has been provided in [31] and, further, the optimal boundary between PWM and FSHE was not verified.

Thus, the objective of this subsection is to show a quantification of the possible energy efficiency and current quality enhancement of an EV with a modular battery system based on a seven-level CHB inverter when using PWM at lower speeds and FSHE at higher speeds. For this purpose, the boundary between FSHE and PWM is determined relative to the modulation index and the vehicle speed. The energy efficiency and the inverter-induced current THD of the drivetrain are determined using simulations. To verify FSHE's dominance at high speed, a simple, small-scale laboratory setup with an inductive load is used and the current THD and the output voltage's supraharmonics are measured.

Within the scope of this section, phase-disposition PWM (PD-PWM) is considered. This means, that the individual carrier waves of all half-bridges are just level-shifted, but their phase angles are constant. In comparison to other PWM methods (phase opposition disposition (POD) or alternative phase opposition disposition (APOD)), PD-PWM introduces the lowest current harmonic distortion, while shifting the harmonic energy content into the common mode carrier harmonics [32].

4.4.1 Simulated Output Current Quality

The obtained current THD_I for the entire torque-speed range of the vehicle's drivetrain is depicted in Figs. 4.10(a) and 4.10(b) for multilevel PWM and FSHE, respectively. As expected, at lower speeds, for example at low modulation indices ($M < 0.3$), the current THD_I is significantly increased ($>> 5\,\%$) when using FSHE, since none of the low-order harmonic components can be eliminated. Calculating the absolute difference of the THD_I between multilevel PWM and FSHE, as shown in Fig. 4.11, it can be seen that FSHE achieves a slightly worse current quality around medium speeds. Nonetheless, it becomes obvious, that FSHE becomes superior at higher speeds in comparison to multilevel PWM. The boundary is emphasized in Fig. 4.11 by the black dashed line.

Hence, the simulated boundary between multilevel PWM and FSHE with respect to the current THD_I at a modulation index of $M = 1$ can be roughly expressed in terms of the relative fundamental frequency (f_1/f_sw) as:

$$\begin{aligned} \frac{f_1}{f_\mathrm{sw}} &\geq 0.048 \;\rightarrow \text{FSHE} \\ \frac{f_1}{f_\mathrm{sw}} &< 0.048 \;\rightarrow \text{multilevel PWM} \end{aligned} \tag{4.14}$$

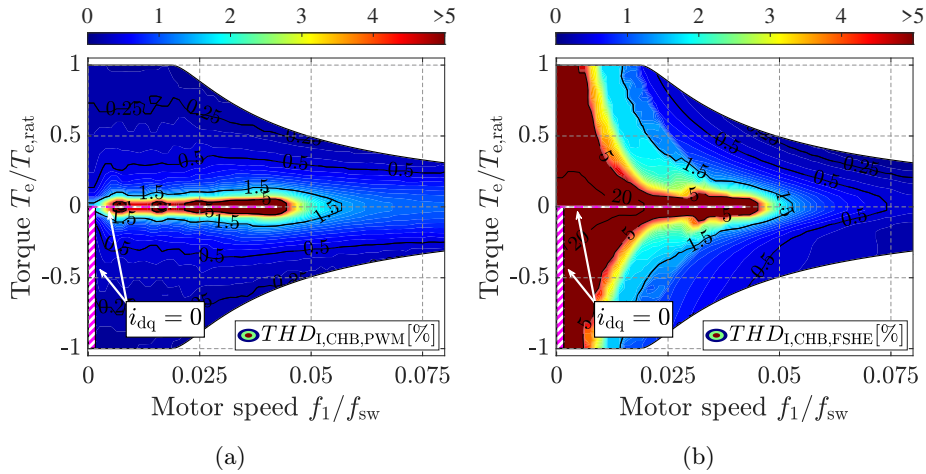


Figure 4.10: Simulated current THD_I for the entire drivetrain operating range for (a) multilevel PWM and (b) FSHE.

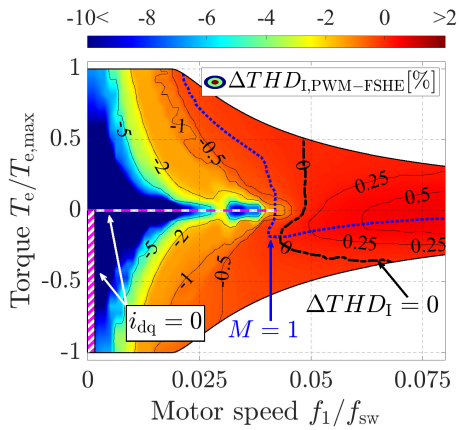


Figure 4.11: Obtained simulated, absolute difference in current THD_I between multilevel PWM and FSHE, $\Delta THD_{I,PWM-FSHE}$.

4.4.2 Simulated Inverter and Battery Efficiency

The simulated inverter efficiency for the entire torque-speed range of the drivetrain is depicted in Figs. 4.12(a) and 4.12(b) for multilevel PWM and FSHE, respectively. At standstill and low speed, PWM is more efficient than FSHE, since the low-order current harmonics using FSHE significantly increases the conduction losses. Exceeding lower speeds, FSHE, eliminating a selection of low-order harmonics,

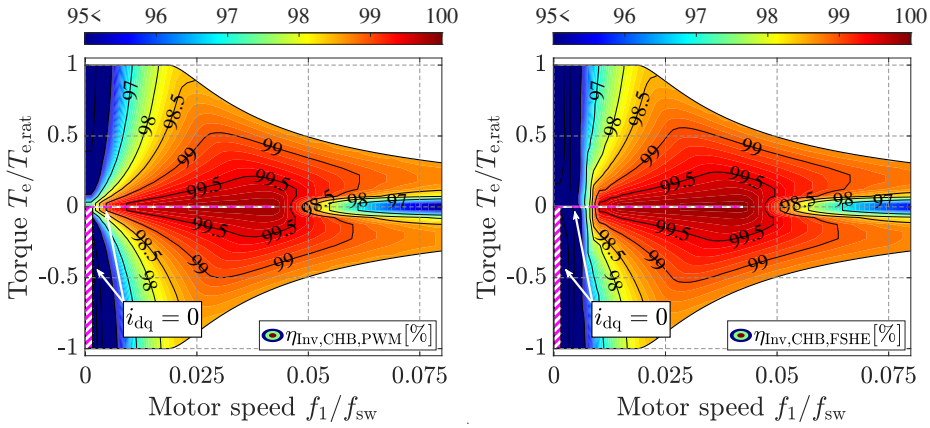


Figure 4.12: Simulated inverter efficiency η_{Inv} for the entire drivetrain operating range for (a) multilevel PWM and (b) FSHE.

becomes more efficient, since the conduction losses become fairly equal, while the switching losses are reduced. As can be seen, the inverter efficiency improvement using FSHE is not that obvious, since the conduction losses of the MOSFETs are dominant in comparison to the switching losses for the chosen switching frequency of 10 kHz.

The simulated battery system's efficiency for the entire torque-speed range of the drivetrain is depicted in Figs. 4.13(a) and 4.13(b) for multilevel PWM and FSHE, respectively. It can be seen that the battery efficiency is improved for a wide operating range, especially at low speed. However, since FSHE cannot be applied at low speeds due to the significantly increased current THD, only the medium and high speed range should be considered, showing an absolute efficiency improvement of up to 1 %. Taking a look at the absolute difference of the combined battery and inverter efficiency $\eta_{\text{Inv}}\eta_{\text{Bat}}$, as shown in Fig. 4.14, it can be seen that FSHE achieves an improvement almost throughout the entire operating range. The zero boundary is emphasized with the black dashed line. Throughout the medium speed range, the absolute improvement of the drivetrain efficiency is up to about 1.5 %. At low speed, FSHE cannot be applied due to the high current THD. Hence, the drivetrain efficiency boundary between multilevel PWM and FSHE can be roughly described as:

$$\begin{aligned} M &\geq 0.3 \;\rightarrow \text{FSHE} \\ M &< 0.3 \;\rightarrow \text{multilevel PWM} \end{aligned} \tag{4.15}$$

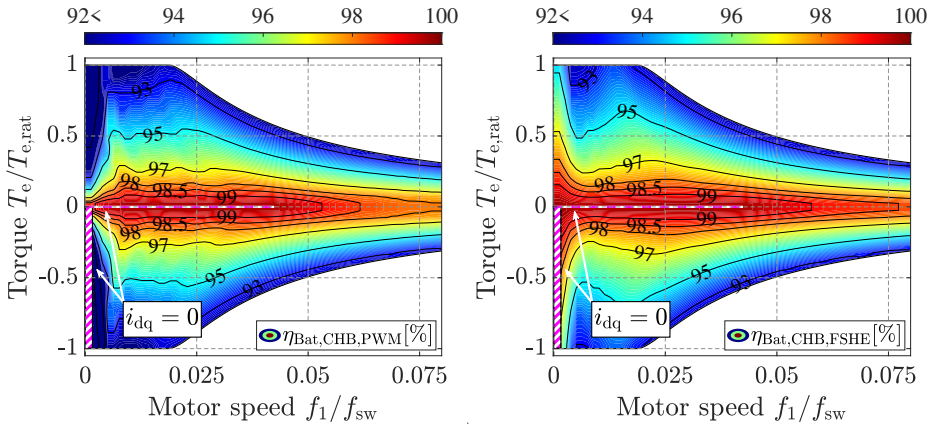


Figure 4.13: Simulated battery efficiency η_{Bat} for the entire drivetrain operating range for (a) multilevel PWM and (b) FSHE.

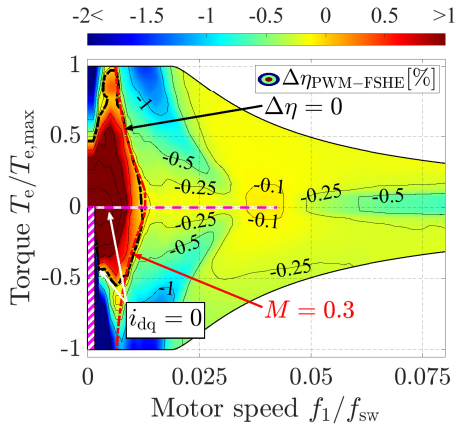


Figure 4.14: Obtained simulated, absolute difference in combined inverter and battery efficiency $\eta_{\mathrm{Inv}}\eta_{\mathrm{Bat}}$ between multilevel PWM and FSHE, $\Delta\eta_{\mathrm{PWM-FSHE}}$.

4.4.3 Simple Optimal Hybrid Modulation - PWM-FSHE

Fig. 4.15 depicts the beneficial operating regions using FSHE in comparison to multilevel PWM. Additionally, the operating points of the small passenger car, as described in Table A.1 in the Appendix, are calculated according to [101] for three different driving cycles. As seen from (4.14) and (4.15), depicted in Fig. 4.15, it seems reasonable to operate the CHB inverter with a hybrid modulation technique,

using multilevel PWM at low and FSHE at medium and high speeds. The boundary between multilevel PWM and FSHE should be selected in a manner to meet a simple optimization relative to the individual current THD_{I} and the drivetrain efficiency $\eta_{\mathrm{Inv}}\eta_{\mathrm{Bat}}$ requirements according to

$$\begin{aligned} &\underset{\frac{T_{\mathrm{e}}}{T_{\max}},\frac{f_1}{f_{\mathrm{sw}}}}{\text{minimize}} && K_\eta \cdot \eta_{\mathrm{Inv}}\eta_{\mathrm{Bat}} + K_{\mathrm{THD}} \cdot THD_{\mathrm{I}} \\ &\text{subject to} && M \geq 0.3 \end{aligned} \tag{4.16}$$

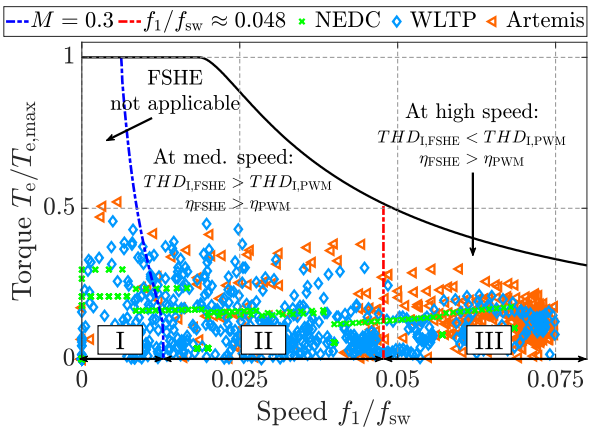


Figure 4.15: Obtained beneficial operating regions for multilevel PWM and FSHE relative to the normalized torque and relative fundamental frequency considering the current THD_{I} and the drivetrain efficiency $\eta = \eta_{\mathrm{Inv}}\eta_{\mathrm{Bat}}$, along with operating points of three driving cycles; NEDC; WLTP; Artemis.

To quantify the effectiveness of the suggested hybrid technique, the energy consumption of the reference vehicle in [84] is simulated using only multilevel PWM and the suggested hybrid technique in (4.16) with $K_{\mathrm{THD}} = 0$ (if $M \geq 0.3$, FSHE is applied). The obtained results can be seen in Table 4.3, which are compared with the results of the two-level IGBT converter in [84] (given in Table 4.2), utilizing the FS400R07A3E3 HybridPACK$^{\mathrm{TM}}$ module [137] from Infineon Technologies AG with a blocking capability of $BV_{\mathrm{CES}} = 700\,\mathrm{V}$ and a nominal collector current of $I_{\mathrm{C,nom}} = 400\,\mathrm{A}$. As can be seen from the obtained results, the two-level inverter (2-L IGBT) achieves a better battery efficiency, whereas the MOSFET multilevel inverter, operated with PWM (CHB-PWM) and the suggested hybrid technique (CHB-Opt), yields a better inverter efficiency. Considering the total WLTP drive cycle efficiency, the MOSFET multilevel inverter operated with only PW-PWM

achieves an absolute efficiency enhancement of 0.2 % in comparison to the IGBT inverter drivetrain. Using the suggested optimized hybrid modulation technique, the efficiency enhancement is improved even further by 0.62 %, achieving an efficiency of about 94.85 %.

Table 4.3: WLTP ($E_{\mathrm{Load}} = 2.761\,\mathrm{kWh}$) drive cycle evaluation using the optimal hybrid modulation technique for the seven-level CHB inverter

	Two-level (IGBT)	CHB-PWM	CHB-Opt
Inverter losses [kWh]	0.071	0.044	0.040
Inverter efficiency [%]	97.49	98.43	98.57
Battery losses [kWh]	0.098	0.119	0.110
Battery efficiency [%]	96.66	95.93	96.22
Overall losses [kWh]	0.169	0.163	0.150
Overall efficiency [%]	94.23	94.43	94.85

4.4.4 Experimental Results

To validate the effectiveness of FSHE in comparison to multilevel PWM at higher speeds, a small-scale laboratory setup with an *RL*-load is used. Since any efficiency measurements are quite intricate and would result only in a small difference, which is typically prone to large errors, only the current THD is measured. Fig. 4.16(a) shows one of the used IGBT H-bridge modules including one 48 V battery pack. The H-bridge modules utilize the sixpack IGBT power modules PSS15S92F6-AG/PSS15S92E6-AG ($BV_{\mathrm{CES}} = 400\,\mathrm{V}$ and $I_{\mathrm{C,nom}} = 15\,\mathrm{A}$) from Mitsubishi Electronics [138]. One phase leg of the power modules is not used. Additionally, each H-bridge is equipped with a capacitor bank of 4 mF. The converter modules were originally used in a STATCOM demonstrator [139]. The battery packs consists of 13 series and 4 parallel connected battery cells, resulting in a nominal voltage of about 48 V. The complete inverter setup, consisting of 6 H-bridge modules, can be seen in Fig. 4.16(b). Just two phases, comprising 3 converter modules each, are operated with a phase shift of 120°. The used *RL*-load has an inductance and a resistance value of about 52 mH and 2.4 Ω, respectively. The load is connected between both phases representing a motor-load in delta connection. A dSPACE system is used to operate the gate signals of the inverter. Fig. 4.17 depicts the measured line voltage, including its FFT, and the line current when operating the inverter with multilevel PWM and FSHE. The

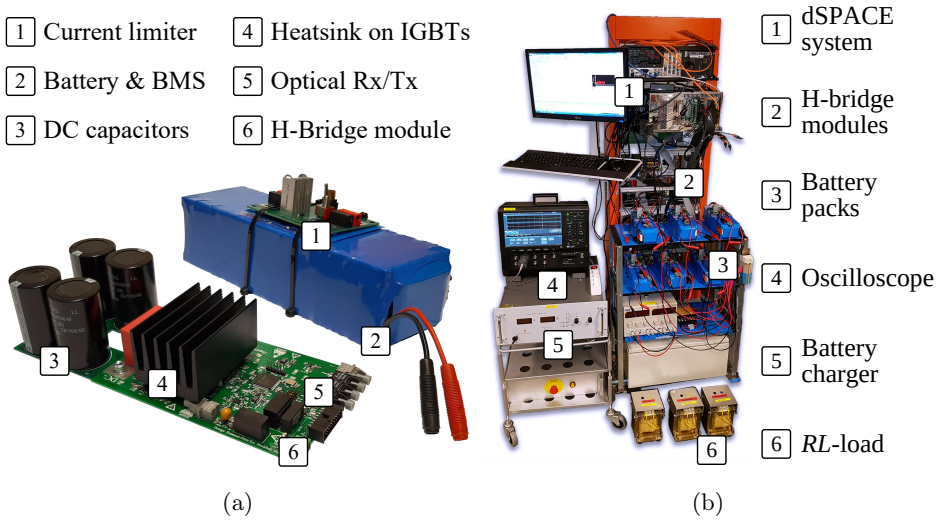


Figure 4.16: Small-scale laboratory setup of seven-level CHB inverter: (a) H-bridge module with 48 V battery pack and (b) entire setup with control and measurement equipment.

battery packs are charged to about 50 V and the modulation index M is about 1. The fundamental frequency f_1 and the switching frequency f_{sw} are chosen to be 500 Hz and 10 kHz, respectively, to emphasize the effectiveness of FSHE at high speed. As can be seen, the voltage drop across the IGBTs and the antiparallel diodes, depending on the current direction, distorts the voltage waveform. This effect would be significantly reduced when using MOSFETs, as intended for a real application, instead of IGBTs. The FFT of the line voltage, displayed up to 150 kHz (supraharmonic band [140]), indicates a reduction of possible conducted emissions. Using FSHE, the highest occurring line voltage harmonic, the 17^{th}, is reduced by a factor of four in comparison to the highest sideband harmonic when using multilevel PWM. Further, Fig. 4.17(c) shows the measured load current. Despite the reduced number of switching events, the current THD using FSHE in comparison to multilevel PWM, is reduced from 1.59 % to 1.13 %.

Furthermore, Fig. 4.18 depicts the measured current THD relative to the modulation index M when operating the CHB inverter with multilevel PWM and FSHE ($f_1 = 500\,\mathrm{Hz}$ and $f_{\mathrm{sw}} = 10\,\mathrm{kHz}$). Additionally, the simulated $WTHD_3$ is shown. Both measurement series follow the trend of each simulation.

Moreover, the measured current THD difference, using FSHE in comparison to multilevel, seems enhanced. As can be seen from Fig. 4.17(c), at each switching

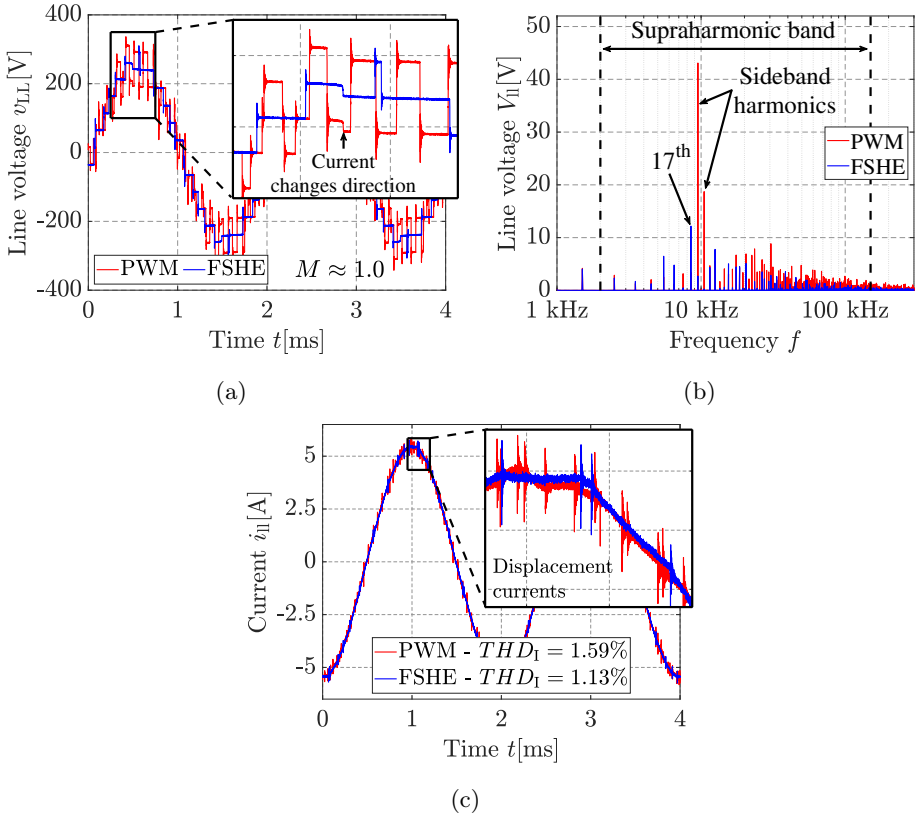


Figure 4.17: Measured (a) output voltage waveforms, including their (b) harmonic components, and (c) line current when operating the CHB inverter with multilevel PWM and FSHE for a modulation index of $M \approx 1$ ($f_1 = 500\,\text{Hz}$ and $f_{sw} = 10\,\text{kHz}$).

event a displacement current [141] is triggered, which distorts the current waveform. Since multilevel PWM inherently utilizes more switching events than FSHE, the difference between the simulation and the measurements is larger. Thus, FSHE actually shows a better current quality over a wider modulation index range in comparison to multilevel PWM.

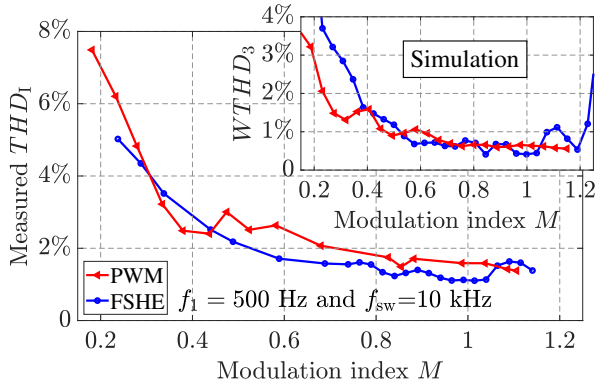


Figure 4.18: Measured current THD relative to the modulation index M and simulated $WTHD_3$ when operating the CHB inverter with multilevel PWM and FSHE ($f_1 = 500\,\text{Hz}$ and $f_{\text{sw}} = 10\,\text{kHz}$).

Fault Tolerance of a Three-Level NPC Inverter

Modular battery systems based on MLIs inherently provide a certain fault tolerance capability due to the availability of redundant switching states, creating the same voltage space vector and, thus, achieving the same three-phase output voltage. This means that the drivetrain can cope with a variety of battery or inverter faults, such as the malfunctioning of an individual battery module, an open circuit switch fault or a short circuit switch fault.

Within this chapter, the fault tolerance capability of a common (I-type) and a MOSFET based active three-level NPC inverter with a connected neutral point for vehicle propulsion is investigated for different permanent fault cases. A three-level NPC inverter with a connected neutral point is one of the simplest types of modular battery systems, since it comprises a simple dual battery pack. Nonetheless, the theory and approaches presented here can be easily adapted and extended to different MLI topologies facilitating a modular battery system.

Therefore, the contribution of this chapter is to present how all types of single, permanent inverter faults, as well as non-destructive battery faults, can be handled and how the vehicle can be brought over to a reduced performance mode, referred to as limp home mode. A new, simple open circuit fault detection algorithm, using a current estimator, and the algorithm's performance are analyzed. Furthermore, two new fault localization algorithms, using a pulse pattern injection principle and an online adaption of the space vector modulation, are investigated.

The results and scientific contributions presented in this chapter are based on Paper II [78].

5.1 SVM for Three-Level NPC Inverters

As described in (3.1), each phase leg of the three-level NPC inverter has three-valid switching states (e.g., for phase a: $S_{\mathrm{a,NPC}} = \{-1, 0, 1\}$). Considering all three phase legs, the three-level NPC inverter comprises in total 27 valid switching states ($S_{\mathrm{NPC}} = [S_{\mathrm{a,NPC}}\ S_{\mathrm{b,NPC}}\ S_{\mathrm{c,NPC}}]$). Transforming the three-phase voltages corresponding to the individual switching states onto the αβ-plane, the SVM scheme as depicted in Fig. 5.1(a) is obtained. As can be seen, the zero vector and each small vector can be created by three or two valid switching states, respectively. Only the medium and large vectors do not have any redundancy.

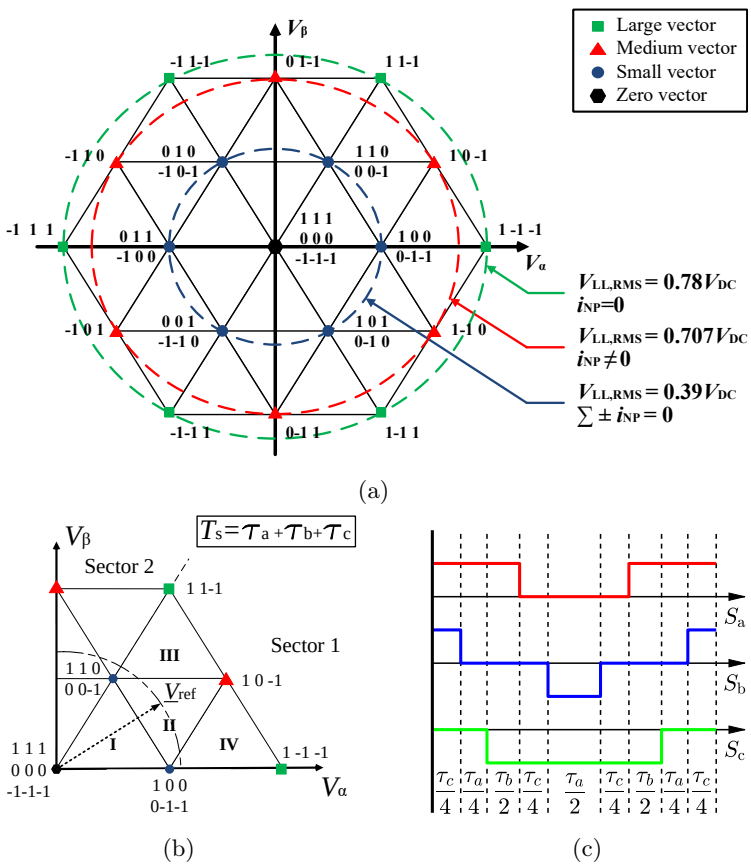


Figure 5.1: (a) Three-level SVM diagram in the αβ-plane and (b) output voltage synthesis in Region II with (c) equal usage of redundant small vectors to reduce the neutral point current.

Using a three-level SVM, Figures 5.1(b) and 5.1(c) depict, for instance, the output voltage synthesis in Region II of Sector 1, equally sharing the medium vector time intervals, as implemented in Plexim's software tool PLECS [142]. In this manner, the neutral point current can be significantly reduced when operating at low modulation indices.

Based on the remaining valid switching state combinations in the state vector diagram, it can be easily assessed whether the NPC inverter can be operated further under a fault condition or not, which is utilized for the analyses in the following sections.

5.2 Battery Faults

Battery faults or charge imbalances are assumed to result either in single battery operation (small vectors) [92] or asymmetric voltage operation [143]. The root of the fault can be for instance an external single battery short circuit [144] or different SOC/SOH of the battery packs [145–147].

External short circuit faults in either of the battery packs, should be detected by the BMS, triggering the corresponding battery relay to trip. Consequently, the powertrain can be operated with half of the rated power, since the possible output voltage is limited to the inner hexagon (small vectors) of the space vector scheme. The torque boundaries of the motor, supplied by a complete and half DC-link for the small passenger vehicle are shown in Fig. 5.2 as Motor limit I and Motor limit II, respectively. Different drive cycle operating points, according

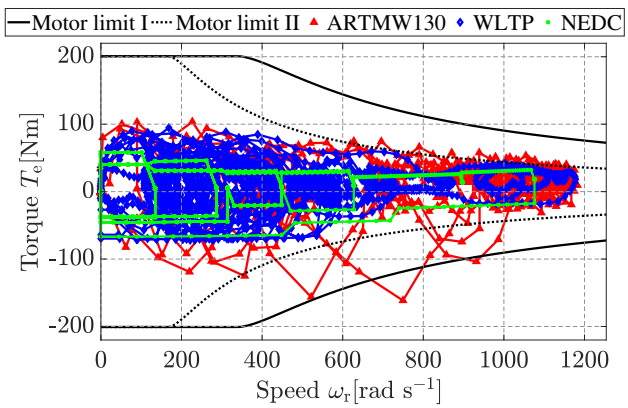
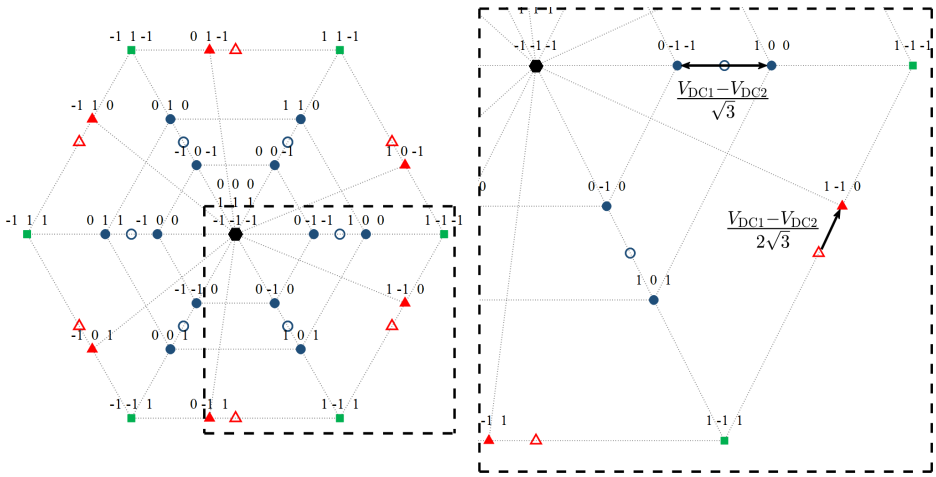


Figure 5.2: Motor limits I and II with full DC-link and half DC-link voltage (small vectors), respectively.

to [101], are also depicted. It can be seen, that the drivetrain can easily cope with the operating points at low speeds, whereas the high speed region is slightly compromised. For instance, the required time to reach 100 km/h from standstill would be increased from initial 10.1 s to 20.1 s for Motor limit I and II, respectively. In case of unequal battery voltages, the SVM scheme can be adapted, without a significant reduction of the output power [143, 148, 149]. Unequal battery voltages can be caused by different SOHs and unsymmetrical load conditions. Fig. 5.3 depicts the distortion of the space vector diagram. It can be seen, that a rotating field can still be created, but the SOCs or DC link voltages of the battery packs should be balanced to fully utilize the battery packs' capacity.



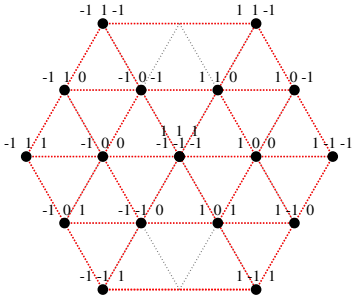
(a) (b)

Figure 5.3: (a) Asymmetric space vector modulation scheme and (b) relation of space vector distortion, which does not significantly affect the drivetrain's performance.

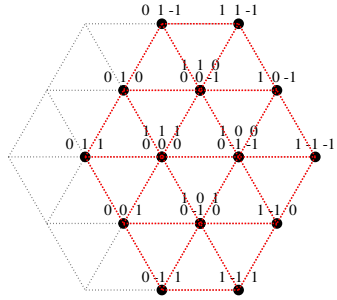
5.3 Inverter Faults

5.3.1 Single Short Circuit Faults

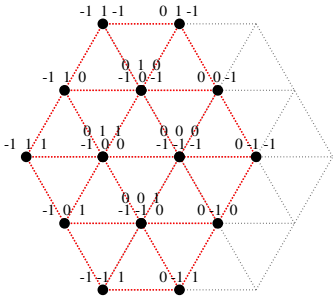
In general, inverter short circuit faults can be detected, and the inverter protected, by additional gate driver circuitry, as for example described in [62–64]. Such short circuit protection mechanism are indispensable for modern EVs. Since the switches are operated in pairs, a shoot-through is usually caused when three switches in



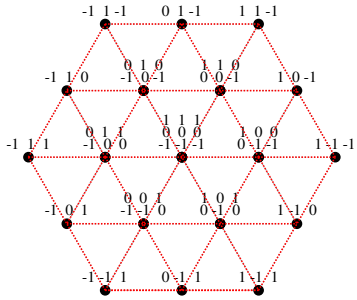
(a) NPC S_{a1} - short



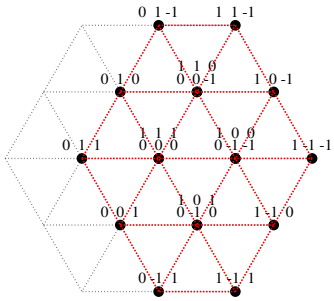
(b) NPC S_{a2} - short



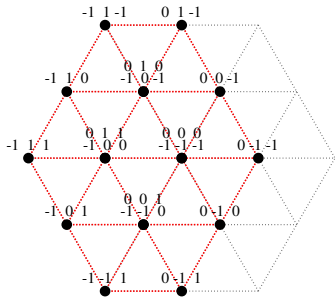
(c) NPC D_{a1} - short



(d) ANPC S_{a1} - short



(e) ANPC S_{a2} - short



(f) ANPC S_{a5} - short

Figure 5.4: Space vector diagram for the corresponding short circuit fault of the three-level NPC and ANPC inverter. Short circuit fault location: (a) NPC S_{a1}−short; (b) NPC S_{a2}−short; (c) NPC D_{a1}−short; (d) ANPC S_{a1}−short; (e) ANPC S_{a2}−short and (f) ANPC S_{a5}−short.

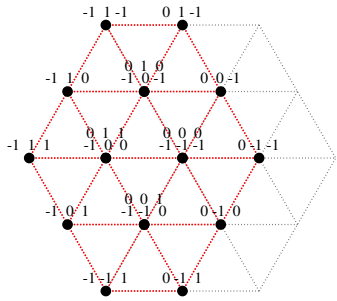
series are unintentionally conducting. If the NPC inverter's short circuit protection is triggered at one or multiple switches, the localization of the fault (for example in a diode or a switch) can be determined by the switching states before and during the event of the short circuit [63]. If the location of the short-circuited switch is known, the space vector modulation can be adapted to single source operation (small vectors) or the faulty leg can be run in two-level operation (large vectors), as illustrated in Fig. 5.4. Because of the NPC topology's symmetry, it is enough to consider just one half leg of the inverter, such as the chosen high-side half-leg of phase a.

It can be seen that a single short circuit fault does not lead to a stall of the drivetrain, which is a great advantage compared to a classical two-level inverter.

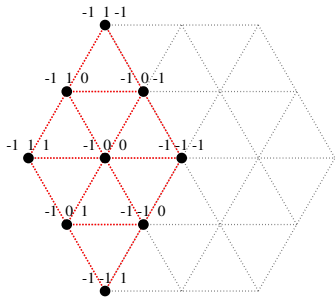
5.3.2 Single Open Circuit Faults

In contrast to short circuit faults, open circuit faults of the inverter are difficult to detect and to localize. Further, there is a need to distinguish between an open circuit fault due to a switch breakdown or to a control circuit fault [150]. Here, it has to be mentioned that a pure open circuit fault (package diode and switch are in open circuit condition) due to breakdown at the switch, would cause an over-voltage, which most likely destroys the circuit. Nevertheless, the most common open circuit faults originate from the drive circuit side. For these reasons, open circuit faults of the clamping diodes/MOSFETs, semiconductor switches and control circuits can be safely detected. If the fault type and location is known, the space vector diagram changes its valid states according to Fig. 5.5. In the case of an open circuit fault at an inner switch, the NPC inverter loses controllability of the current in four complete sectors, which in turn results in a high torque ripple, forcing the powertrain to stall. For the other two open circuit fault cases the space vector modulation can be adapted to single source operation or the faulty leg can be operated in two-level operation. If an ANPC inverter is used, the remaining valid states change according to Figs. 5.5(d) to 5.5(f). For an open circuit at S_{a5} a complete open circuit was considered, because an open circuit of the switch would not affect the functionality of the inverter, since the body or package diode would still work.

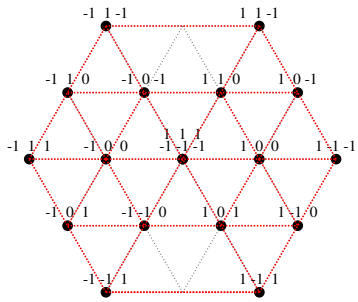
A current estimator, used for current controlled motor or grid feeding inverter applications, can be utilized to detect open circuit faults. When designing the current controller in direct and quadrature quantities for an interior permanent magnet machine, loop shaping is commonly used. This measure has the objective to shape the response of the system like a first order system with a bandwidth 10



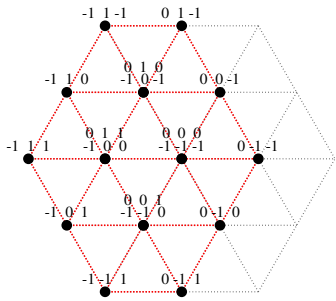
(a) NPC S_{a1} - open



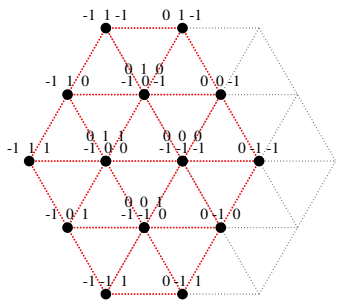
(b) NPC S_{a2} - open



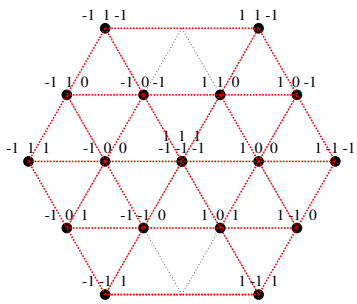
(c) NPC D_{a1} - open



(d) ANPC S_{a1} - open



(e) ANPC S_{a2} - open



(f) ANPC S_{a5} - open

Figure 5.5: Space vector diagram for the corresponding open circuit fault of the three-level NPC and ANPC inverter. Open circuit fault location: (a) NPC S_{a1}_open; (b) NPC S_{a2}_open; (c) NPC D_{a1}−open; (d) ANPC S_{a1}−open; (e) ANPC S_{a2}−open and (f) ANPC S_{a5}−open.

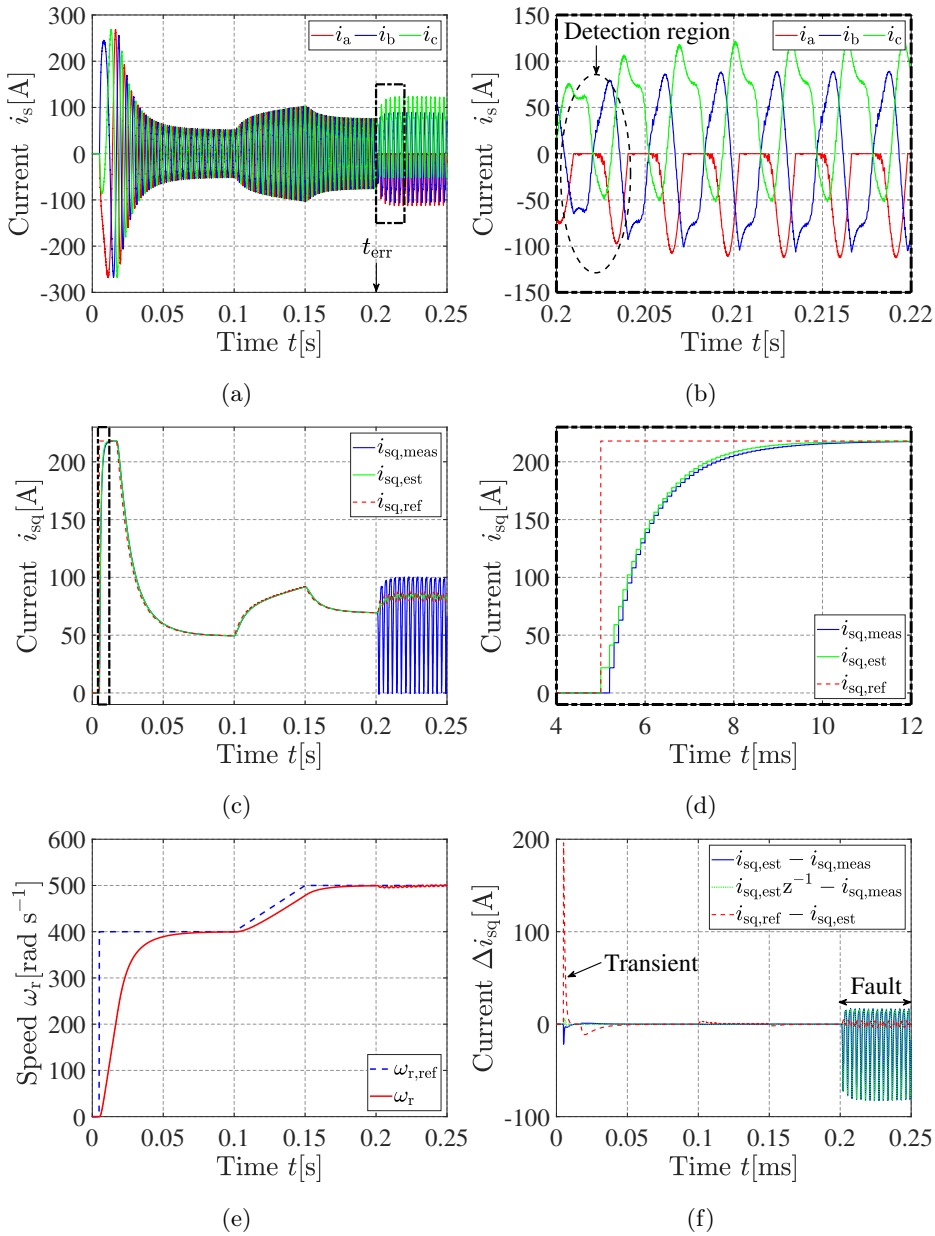


Figure 5.6: (a)(b) Three-phase motor currents, (c)(d) quadrature current, (e) motor speed and (f) fault detection signal based on the quadrature current in case of an open circuit fault at the inner switch S_{a2} of the NPC inverter.

times slower than the PWM converter. Assuming a good knowledge of the plant, the stator currents in dq-quantities $\underline{i}_{\mathrm{sdq}}$ can thus be estimated by a discrete first order system model as

$$\underline{i}_{\mathrm{sdq}}(k) = \underline{i}_{\mathrm{sdq}}(k-1) + \alpha_{\mathrm{c}}(\underline{i}_{\mathrm{sdq,ref}}(k) - \underline{i}_{\mathrm{sdq}}(k-1)) \tag{5.1}$$

where the bandwidth α_{c} typically equals 0.1 [47]. This estimation is accurate as long as $\frac{f_1}{f_{\mathrm{sw}}} \leq 0.1$. If $\frac{f_1}{f_{\mathrm{sw}}}$ equals 0.1, the phase shift is 18° and the amplitude error is about 2 % [47]. This in turn results in an inaccurate current estimation during high transient changes of the current reference.

Figs. 5.6(a) to 5.6(f) describe the simulated detection of an open circuit fault of switch S_{a2}, occurring at t_{err} =0.2 s, if a speed reference is applied as depicted in Fig. 5.6(e). The mechanical dynamics are modeled as a rotating single mass with a low inertia to speed up the simulation time. In the beginning of the fault, the current of the faulty phase is negative, meaning that the fault cannot be detected until the current becomes positive, which is the worst-case scenario. To detect a fault condition, the reference, estimated and measured current values in quadrature quantities, as can be seen in Figs. 5.6(c) and 5.6(d), are processed as illustrated in Fig. 5.7. If the difference of the measured and the estimated

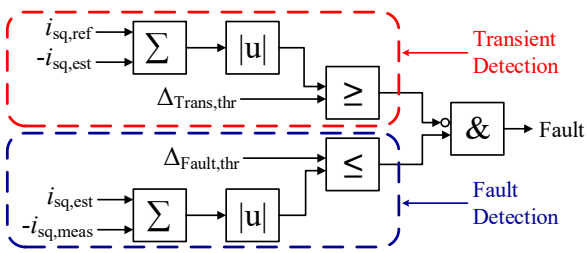


Figure 5.7: Fault triggering algorithm considering fault and transient detection conditions.

quadrature current exceeds a certain threshold ($\Delta_{\mathrm{Fault,thr}}$), a fault detection signal is activated. However, during high current transients, a current difference occurs as well, as shown in Fig. 5.6(f), which could be misinterpreted as an error. Therefore, a transient detection condition can be added, so that the actual fault signal is just triggered during small transient or steady state conditions. From Fig. 5.6(f), it can be seen, that the estimated and the measured current substantially differ when applying a step in the reference, due to the sample delay of the discrete control and the bandwidth of the controller. An additional delay of the estimated current reduces the difference, but during a high transient a detection is not instantly

possible. However, during small transients and steady state, the error detection time lies within a few switching cycles (samples) from the time instant when the faulty device/semiconductor would normally start to conduct the phase current.

5.4 Open Circuit Fault Localization at Stand Still

As stated above, the source of an open circuit must be localized to properly adapt the space vector modulation scheme. In this section a fault localization technique in form of a pulse pattern injection at standstill is introduced. It thus requires, the vehicle to stop after the detection of a fault. Table 5.1(a) shows the six pulses that need to be applied for the duration of a single or multiple switching intervals. Also listed are the average phase currents of the response during the zero state, that must be observed. If a response complies with the condition of the average phase currents, all conducting switches are properly functioning and the case response can be assessed as "TRUE", otherwise "FALSE"(¬). Depending on the result of the responses, the error can be localized by a combination of the six different

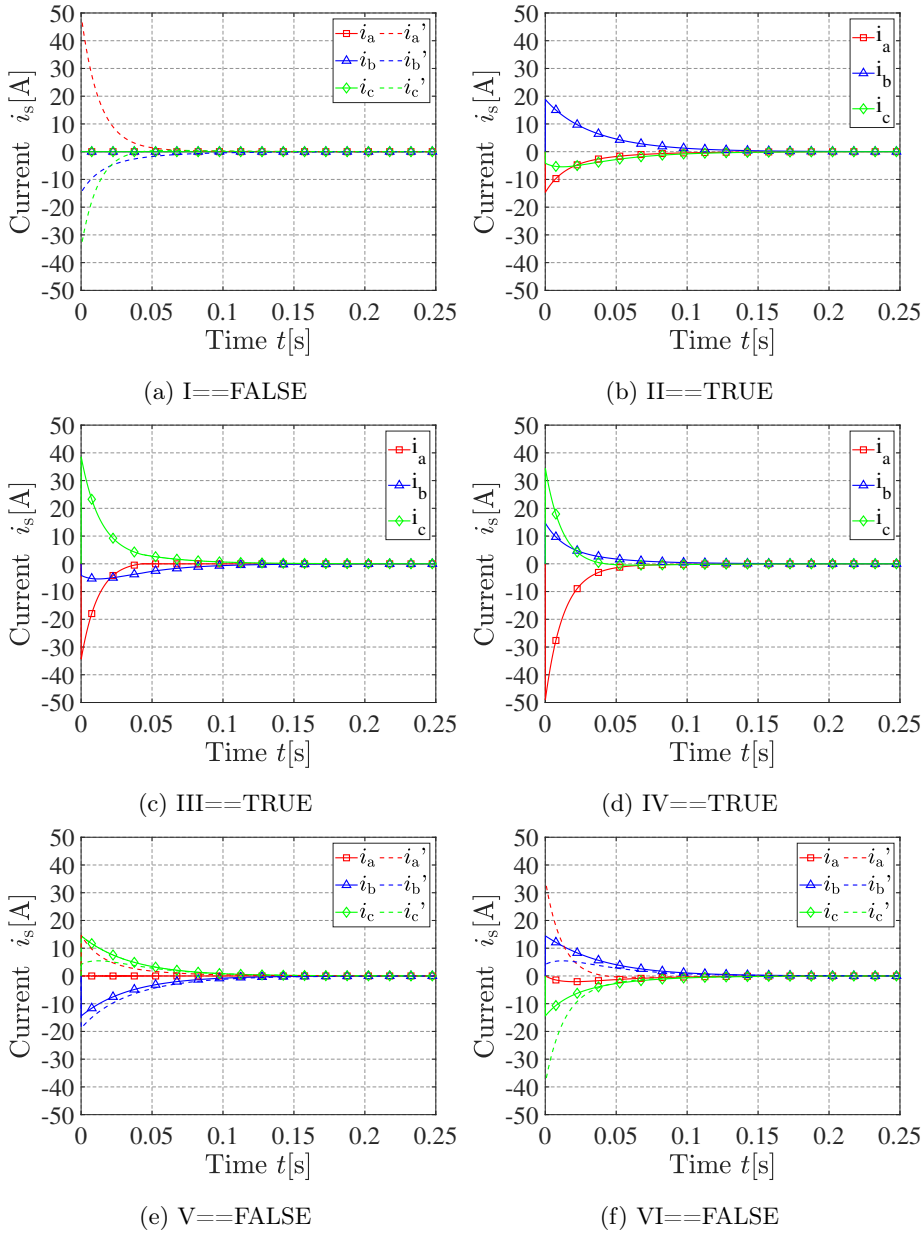
Table 5.1: Open circuit fault localization

(a) Pulse pattern

Case	Pulse	I_a	I_b	I_c	Conducting switches
I	(1, 0, 0) → (0, 0, 0)	> 0	< 0	< 0	S_{a1}, S_{a2}, D_{b2}, S_{b3}, D_{c2}, S_{c3}
II	(0, 1, 0) → (0, 0, 0)	< 0	> 0	< 0	D_{a2}, S_{a3}, S_{b1}, S_{b2}, D_{c2}, S_{c3}
III	(0, 0, 1) → (0, 0, 0)	< 0	< 0	> 0	D_{a2}, S_{a3}, D_{b2}, S_{b3}, S_{c1}, S_{c2}
IV	(-1, 0, 0) → (0, 0, 0)	< 0	> 0	> 0	S_{a3}, S_{a4}, D_{b1}, S_{b2}, D_{c1}, S_{c2}
V	(0,-1, 0) → (0, 0, 0)	> 0	< 0	> 0	D_{a1}, S_{a2}, S_{b3}, S_{b4}, D_{c1}, S_{c2}
VI	(0, 0,-1) → (0, 0, 0)	> 0	> 0	< 0	D_{a1}, S_{a2}, D_{b1}, S_{b2}, S_{c3}, S_{c4}

(b) Diagnosis for phase leg a

Case combination	Broken switch
¬ I & II & III & IV & V & VI	S_{a1}
¬ I & II & III & IV & ¬V & ¬VI	S_{a2}
I & ¬II & ¬III & ¬IV & V & VI	S_{a3}
I & II & III & ¬IV & V & VI	S_{a4}
I & II & III & IV & ¬V & ¬VI	D_{a1}
I & ¬II & ¬III & IV & V & VI	D_{a2}



(a) I==FALSE

(b) II==TRUE

(c) III==TRUE

(d) IV==TRUE

(e) V==FALSE

(f) VI==FALSE

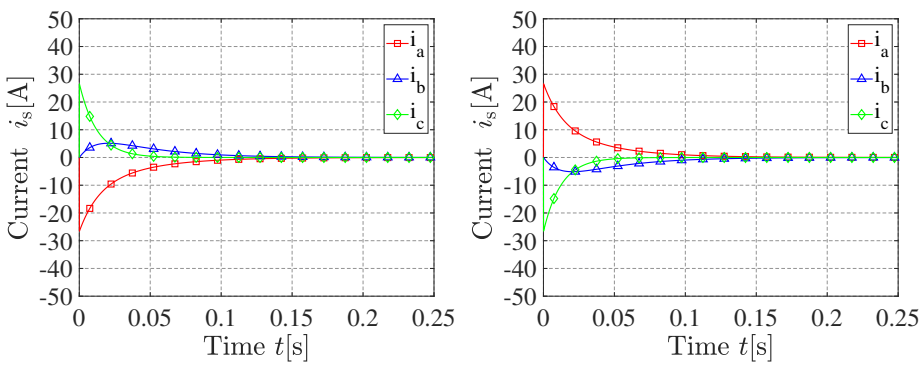
Figure 5.8: Simulated pulse responses for a localization of an open circuit fault at S_{a2} for the NPC and ANPC inverters. The dashed lines illustrate the pulse responses under normal conditions for the with FALSE marked cases. Cases from Table 5.1: (a) I==FALSE; (b) II==TRUE; (c) III==TRUE; (d) IV==TRUE; (e) V==FALSE and (f) VI==FALSE.

responses as described in Table 5.1(b).

For example, Fig. 5.8 shows the simulated pulse responses for an open circuit fault at S_{a2} of an NPC and an ANPC inverter. The dashed lines mark the expected responses for the Cases I, V and VI, where the observed average currents do not comply with the conditions in Table 5.1(b), while all other cases are yielding a "TRUE" value. Therefore, switch S_{a2} can be localized as the faulty switch. The approach can be similarly applied to an ANPC inverter, to check the main switches and the body/package diodes of the clamping MOSFETs. As long as the body/package diodes of the clamping MOSFETS and the main switches S_{x1} to S_{x4} are working, the inverter can be properly operated and the phase currents do not yield any fault indications. Nevertheless, the main difference of the ANPC in comparison the NPC inverter lies in the possibility to overcome a fault at an inner switch, for example S_{a2}. Therefore, the channels of the MOSFETs should be

Table 5.2: Open circuit fault localization at clamping MOSFETs

Pulse	I_a	I_b	I_c	Broken switch (if FALSE)
(0^p, 1 , 1) → (0^p, 0 , 0)	< 0	–	–	S_{a5}
(0^n,-1 ,-1) → (0^n, 0 , 0)	> 0	–	–	S_{a6}
(1 , 0^p, 1) → (0 , 0^p, 0)	–	< 0	–	S_{b5}
(-1 , 0^n,-1) → (0 , 0^n, 0)	–	> 0	–	S_{b6}
(1 , 1 , 0^p) → (0 , 0 , 0^p)	–	–	< 0	S_{c5}
(-1 ,-1 , 0^n) → (0 , 0 , 0^n)	–	–	> 0	S_{c6}



(a) TRUE (b) TRUE

Figure 5.9: Pulse response to test the MOSFETs (a) S_{a5} and (b) S_{a6} in reverse direction for the ANPC inverter.

tested in the reverse current direction of the corresponding clamping path diode. For this purpose, a test pulse for each switch can be applied and the responses according to Table 5.2 must be observed. Here, just one switch of the tested leg must be switched on during the zero state, which is depicted in the table with a positive (0^{p}) or negative (0^{n}) marked exponent, representing clamping switch of the upper and lower half leg, respectively. Fig. 5.9 depicts the pulse response of the clamping switches of phase leg a. Both are working properly, since they are able to conduct in reverse direction.

5.5 Online Open Circuit Fault Localization

To localize the open circuit fault during online operation, the faulty half leg needs to be first determined and subsequently two different space vector modulation patterns are used (two-level operation of the corresponding half leg and single battery operation) until current control is regained. A schematic overview of the fault detection and localization for the NPC inverter can be seen in Fig. 5.10. To determine the faulty half leg, the average Park vector method is often used as described in [151]. It is based on the Clark transformation of the average values of the phase currents, yielding a nonzero value at fault condition. The method, however, cannot be used to accurately determine the faulty switch of the half leg. The average value of the phase currents can be written as

$$I_{x,\mathrm{avg}} = \frac{1}{t_1 - t_0} \int_{t_0}^{t_0+t_1} i_x \mathrm{dt} \tag{5.2}$$

where the integral part along the time interval from t_0 to t_1 represents a charge, which can be divided into a positive charge as

$$Q_{x,\mathrm{p}} = \int +i_{x,\mathrm{p}} \mathrm{dt} \tag{5.3}$$

and a negative charge as

$$Q_{x,\mathrm{n}} = \int -i_{x,\mathrm{n}} \mathrm{dt} \quad . \tag{5.4}$$

The direction of the phase current yields the consideration of a positive and negative charge, described as

$$i_{x,\mathrm{n}} = \begin{cases} 0; & i_x > 0 \\ i_x; & i_x <= 0 \end{cases} \tag{5.5}$$

and

$$i_{x,\mathrm{p}} = \begin{cases} i_x; & i_x > 0 \\ 0; & i_x <= 0 \end{cases} \quad . \tag{5.6}$$

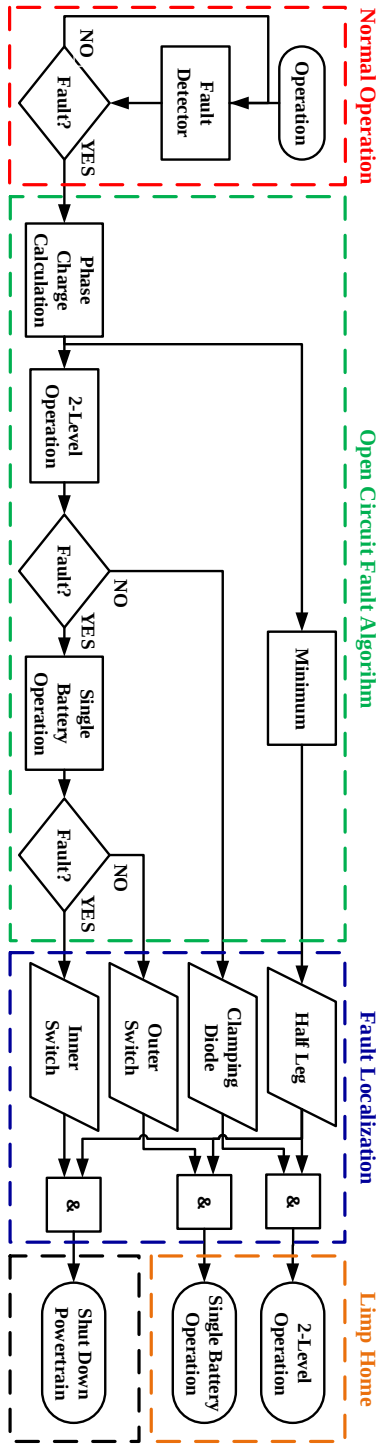


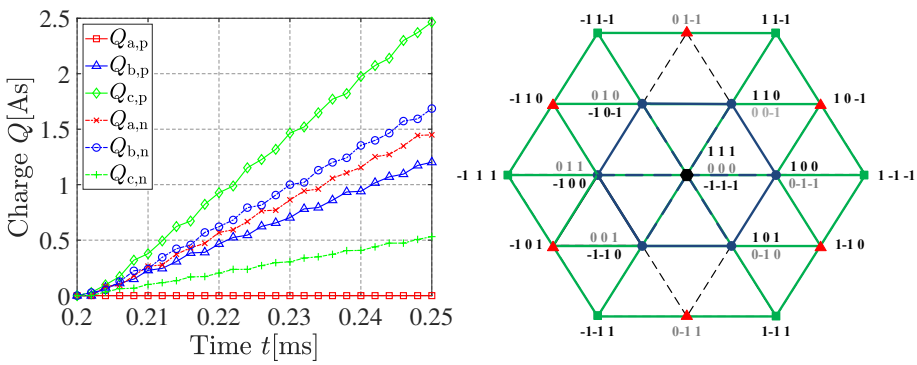
Figure 5.10: Schematic overview of the online fault localization of an open circuit fault of the NPC inverter.

Immediately after the detection of the fault, as can be seen in the scheme, the positive and negative phase charge values should be calculated according to (5.3) and (5.4) for a certain time duration, since the minimum yields the faulty half leg according to Table 5.3.

Fig. 5.11(a) shows an example, when an open circuit fault occurs at $t_{\mathrm{err}} = 0.2\mathrm{s}$ at S_{a2}, as depicted in Fig. 5.6. Depending on the accuracy of the charges, an acceptable result is already achieved after about 3 ms to 10 ms, which corresponds to 1 to 3 electrical periods. It can be seen, that $Q_{\mathrm{a,p}}$ remains zero, which indicates a fault at the positive half leg of phase a. Next, the space vector modulator should be adapted to 2-level operation, meaning the avoidance of the zero state for phase a, as emphasized in green in Fig. 5.11(b). If the control of the current is regained, the clamping diode is broken. Otherwise, the space vector modulator is subsequently adapted only to small vectors. This causes the available torque to

Table 5.3: Open circuit fault localization

Minimum	Broken half leg
$Q_{\mathrm{a,p}}$	S_{a1} & S_{a2} & $D_{\mathrm{a1}}/S_{\mathrm{a5}}$
$Q_{\mathrm{a,n}}$	S_{a3} & S_{a4} & $D_{\mathrm{a2}}/S_{\mathrm{a6}}$
$Q_{\mathrm{b,p}}$	S_{b1} & S_{b2} & $D_{\mathrm{b1}}/S_{\mathrm{b5}}$
$Q_{\mathrm{b,n}}$	S_{b3} & S_{b4} & $D_{\mathrm{b2}}/S_{\mathrm{b6}}$
$Q_{\mathrm{c,p}}$	S_{c1} & S_{c2} & $D_{\mathrm{c1}}/S_{\mathrm{c5}}$
$Q_{\mathrm{c,n}}$	S_{c3} & S_{c4} & $D_{\mathrm{c2}}/S_{\mathrm{c6}}$



(a) (b)

Figure 5.11: (a) Phase charge values in case of an open circuit fault at S_{a2} and (b) corresponding single battery and two-level space vector modulation of phase a.

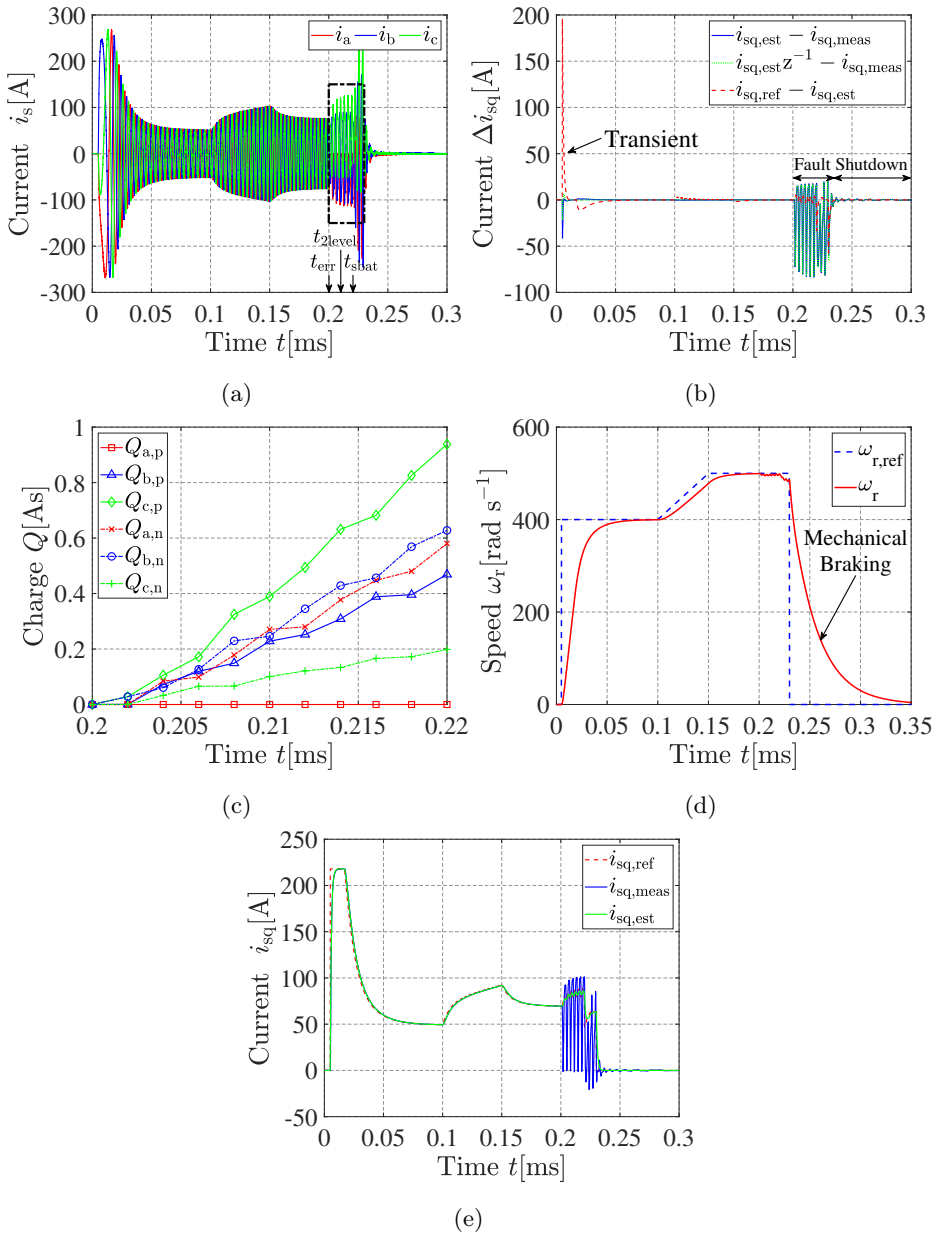


Figure 5.12: Online localization of an open circuit fault at S_{a2} for the NPC inverter. (a) Three-phase motor currents. (b) fault detection signal based on the quadrature current. (c) Phase charges. (d) Motor speed. (e) Quadrature current.

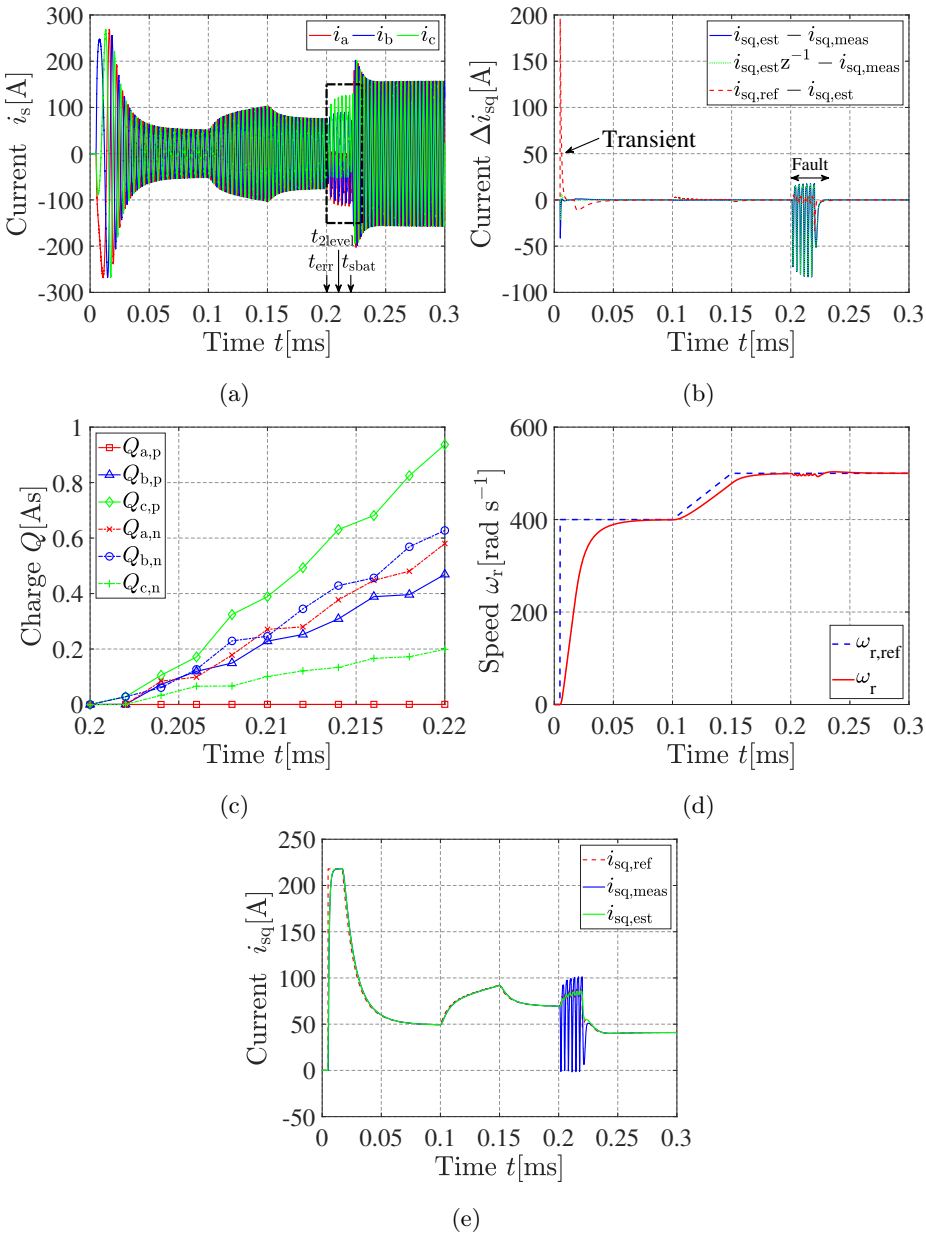


Figure 5.13: Online localization of an open circuit fault at S_{a2} for the ANPC inverter. (a) Three-phase motor currents. (b) fault detection signal based on the quadrature current. (c) Phase charges. (d) Motor speed. (e) Quadrature current.

be compromised and may cause a braking torque to be applied to the drivetrain.

As seen from Fig. 3.2, the differentiation between an active and common NPC inverter is essential since the active NPC inverter, containing MOSFETs in the clamping path, is able to be operated in single battery operation in the case of an open circuit fault at an inner switch. Therefore, the last fault case shows an open circuit fault at S_{a2}, occurring at $t_{\mathrm{err}} = 0.2\mathrm{s}$, as shown in Figs. 5.12 and 5.13 for the NPC and the ANPC inverter, respectively. The same procedure as before is followed and both inverters show the same behavior until single battery operation is applied. As can be seen in Figs. 5.12(b) and 5.13(b), an instantaneous fault detection is easily achieved due to the high three-phase current distortion. Next, the phase charges are calculated as can be seen in Figs. 5.12(c) and 5.13(c). Already after 3 ms to 10 ms, the phase charges yield a minimum of $Q_{\mathrm{a,p}}$, as expected, which indicates a fault at the positive half leg of phase a. Afterwards, two level operation and single battery operation are applied at $t_{\mathrm{2level}} = 0.21\,\mathrm{s}$ and $t_{\mathrm{sbat}} = 0.22\mathrm{s}$, respectively. Regarding the NPC inverter, neither in two-level nor in single battery operation is current control regained, which indicates an open circuit fault of S_{a2}. Consequently, the NPC inverter will shut down, as seen in Fig. 5.12(a), and the powertrain will stall, braking mechanically, shown in Fig. 5.12(d). On the contrary, if an ANPC inverter is used, two-level operation does not show an effect either, but the fault can be overcome and current control is regained by single battery operation, as can be seen from the current and speed plots in Fig. 5.13. This is due to the fact, that the clamping switch S_{a6} in addition to the diode enables bidirectional current. This is one of the major advantages of an ANPC inverter compared to an NPC inverter, in particular for an automotive application.

5.6 Experimental Results

To verify the theoretical assumptions and simulation results above, a simple, open circuit fault test procedure was conducted on a motor test bench, which can be seen in Fig. 5.14(a). The testbed comprises a common three-level NPC inverter with a connected neutral point, as shown in Fig. 5.14(b), which operates a two-pole induction machine. A field oriented control approach is implemented to control the motor's currents. It should be noted that the observer theorem, given in (5.1), is not affected by the motor type (e.g., induction machine, synchronous reluctance machine, etc.) as long as the current controller is designed using loop shaping [47]. For safety reasons and simplicity, all measurements are conducted with a nominal DC link voltage of only 60 V, which is sufficient to prove the concept's validity.

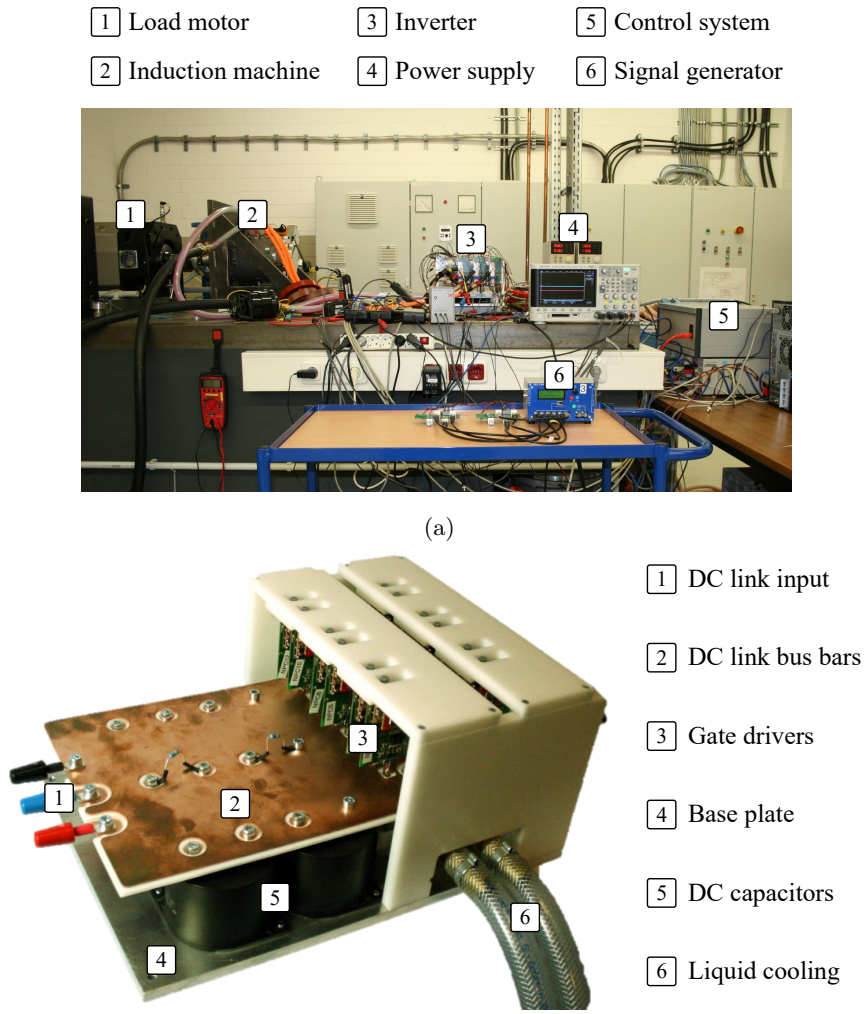


Figure 5.14: (a) Motor test bench and (b) three-level NPC inverter with accessible neutral point.

For the implementation of the pulse pattern injection and an adapted space vector modulation, a PWM signal generator is used. An introduced open circuit fault at S_{a1} should be handled. The test procedure is divided into three parts: the fault detection, the fault localization and the fault mitigation.

5.6.1 Fault Detection

At first, the machine's three-phase currents are controlled to have a peak value of about 10 A and a fundamental frequency of 17 Hz, as shown in Fig. 5.15(a). Since the machine is unloaded, the direct-axis current i_{sd} equals the phase currents' peak value (amplitude-invariant) at steady state, whereas the quadrature-axis current i_{sq} is roughly zero, as can be seen in Fig. 5.15(b). The rotational speed reaches about 505 to 510 rpm, which approximately equals the synchronous speed of 510 rpm. At steady state, an open circuit fault at switch S_{a1} is introduced at t_{err} =0.2 s by disconnecting the corresponding fibre optic cable that transmits the gate signal. From the three-phase current and dq-current plots, it can be seen that the motor currents are distorted during fault operation. Similar as in

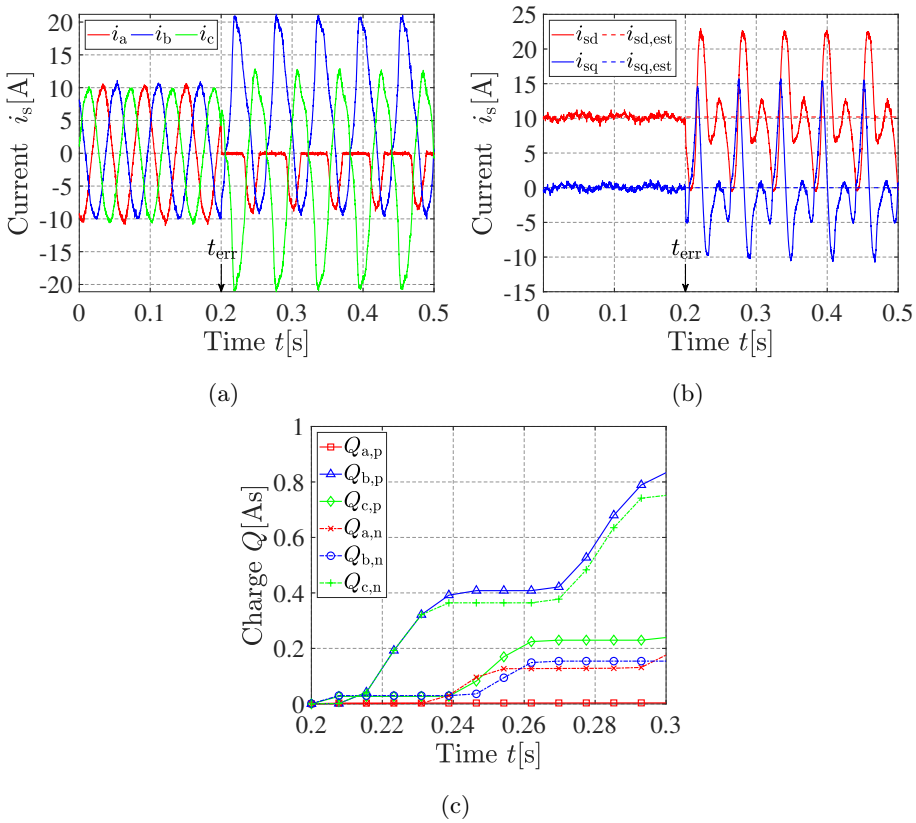
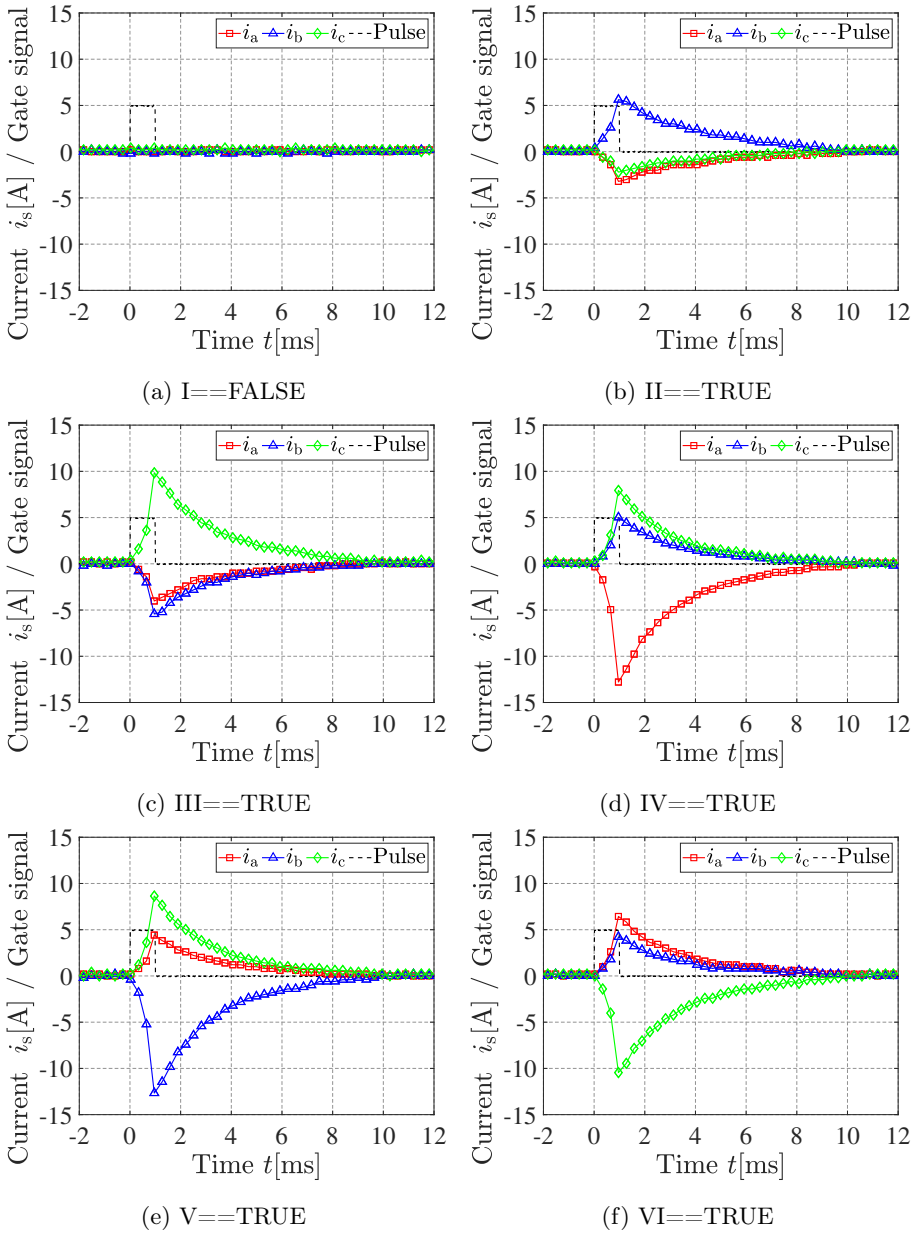


Figure 5.15: Measured detection of an open circuit fault at S_{a1} for the NPC inverter.

the simulations, the faulty phase leg does not conduct the current in forward direction, which in turn distorts and increases the peak current of the remaining phases. Comparing the faulty phase's current with the simulation results seen in Fig. 5.6(b), a similar characteristic can be observed, but the phase shift of the currents is altered, since the machine type differs and the operating point is shifted from the field weakening to the constant torque region, though these differences do not change the effectiveness of the detection algorithm. Depending on the threshold for triggering a fault signal, the fault detection time could be within a few µs up to 20 ms (a third of an electrical period). However, since the peak-to-peak ripple of the q-current at steady state is within a band of 1 A, which should not be misinterpreted as a fault, an almost instantaneous detection within a few µs can be easily achieved, if setting a threshold criteria $\Delta_{\mathrm{Fault,thr}}$ of 2 A as $|i_{\mathrm{sq,est}} - i_{\mathrm{sq,meas}}| \leq 2A$. If the online localization method would be applied, the phase charges according to (5.2)-(5.6) are calculated, as can be seen in Fig. 5.15(c). The minimum of charge $Q_{\mathrm{a,p}}$ indicates a fault at the positive half leg of phase a. It can be seen, that the algorithm converges to a reliable result after one electrical period, similar as in the simulations, of about 60 ms.

5.6.2 Pulse Pattern Injection

After successfully detecting a fault condition, the motor should be stopped and, then, the open circuit fault can be localized by the responses of the injected pulse pattern, as can be seen in Fig 5.16. Since the DC link voltage is limited to 60 Volt, the current derivative is low. Therefore, a pulse duration of 1 ms is chosen to achieve an acceptable magnitude of the current responses so that these can be post-processed. In the simulations, a pulse duration of 100 µs was used, which was sufficient since the DC link voltage was chosen to be 400 V and the motor inductance value was less than that of the chosen induction machine. Regarding the responses, it can be seen that the three-phase response currents for Case I are zero, whereas all remaining cases show nonzero current responses with the expected polarity. Therefore, according to Table 5.1, an open circuit fault at switch S_{a1} can be identified.



(a) I==FALSE (b) II==TRUE

(c) III==TRUE (d) IV==TRUE

(e) V==TRUE (f) VI==TRUE

Figure 5.16: Measured pulse responses for a localization of an open circuit fault at S_{a1} for the NPC inverter. Cases from Table 5.1: (a) I==FALSE; (b) II==TRUE; (c) III==TRUE; (d) IV==TRUE; (e) V==TRUE and (f) VI==TRUE.

5.6.3 Single Source Operation

An open circuit fault at switch S_{a1} means that the inverter can still be operated in single battery operation. Therefore, the inverter is restarted, utilizing just the negative DC link voltage, as can be seen in Fig 5.17. The magnitude of the phase currents can still be controlled to 10 A as shown in Fig. 5.17(a). Fig. 5.17(b) shows a short time interval of 1 ms, so that the output voltage of one phase can be seen. As expected, the output voltage is just switched between the neutral point and the negative DC link.

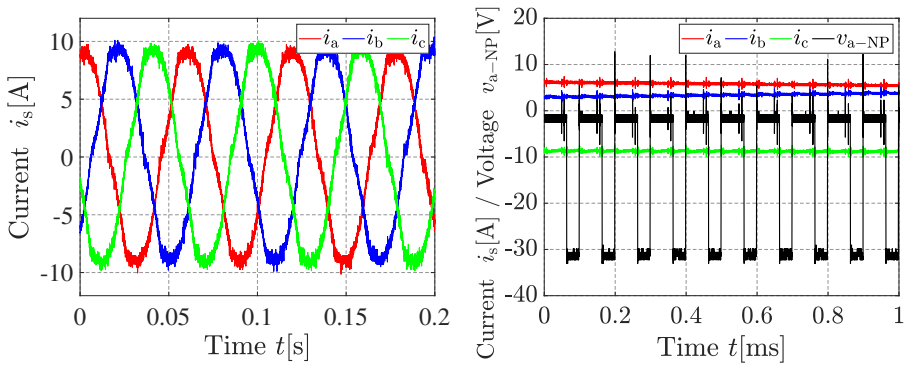


Figure 5.17: Single source operation of the NPC inverter with utilization of the negative DC link in case of an open circuit fault at S_{a1}: (a) three-phase motor currents and (b) zoomed time interval with switched phase voltage waveform.

Conducted Emissions of a Fault-Tolerant NPC Inverter

In modern EVs, the proper functioning of all electronic devices must be ensured to guarantee an adequate and safe operation of the entire vehicle. The propulsion inverter, as the most powerful component, bears a high risk of unwanted electromagnetic interference with other onboard or surrounding devices. Therefore, potential sources of electromagnetic emissions should be identified and mitigated during an early stage of the inverter's and the system's design process to reduce radiated and conducted emissions before applying shielding and filters.

However, the additional neutral point connection of the fault-tolerant three-level NPC, as shown in Fig. 3.2(b), forms a unique three-wire DC source, whereas the test procedures and limitations, stated in CISPR 25 [57], are usually applied to single DC sources (two-wire), requiring only two LISNs for the measurement of conducted emissions [152, 153]. Furthermore, the classical two-wire CM and DM consideration, as described in [154], cannot be applied to localize CM/DM resonances. Hence, the question arises: How to measure and separate the noise levels of the three-wire DC side of the fault-tolerant NPC inverter in accordance to CISPR 25?

Therefore, this chapter shows how to measure the conducted emissions of the fault-tolerant NPC inverter according to CISPR 25 [57], using three LISNs, and the noise separation of the three-wire CM/DM is explained. Additionally, two compact hardware CM/DM separators, based on small circuit HF transformers, for the CM, line-DM and phase-DM noise levels were developed and are characterized. A test setup with an artificial machine load and an NPC prototype inverter are used for measurements. The inverter is operated with three-level and two-level

modulation, resembling normal operation and operation under an open circuit fault of a clamping-diode, respectively.

The results and scientific contributions presented in this chapter are based on Paper III [155] and Paper XVI [76].

6.1 Three-Wire Noise and CM & DM Separation

Since the three-level NPC inverter, as shown in Fig. 3.2(b), is supplied by a dual battery pack with a connected neutral point, the DC side cannot be considered as a classical two-wire inverter system. Thus, it must be dealt with as a three-wire or three-phase CM/DM system, depicted in Fig. 6.1 as the EUT. The definition and separation of three-phase DM/CM quantities are already known from classical three-phase AC systems (load side), as for example described in [156–159]. The corresponding standard CISPR 14-1 [160] regulates the conducted emission levels within the frequency range from 150 kHz to 30 MHz. Hence, for the noise measurement according to CISPR 25 [57], three LISNs, often referred to as a special type of AMNs, must be inserted between the split battery system and the DC link capacitors' terminals of the NPC inverter to have a defined network impedance. Furthermore, these are required to couple the high frequency noise into the measurement equipment, whereas the low frequency components are still conducted via the DC-link rails. When measuring the noise levels, each output of the LISNs must be terminated by 50 Ω, either by the spectrum analyzer's input or by external terminations, to provide a symmetric measurement condition. As seen from the measurement scheme, shown in Fig. 6.1, the CM noise of the three-wire system is defined as the mean of the three LISN measurement outputs as

$$V_{\mathrm{CM}} = \frac{V_{\mathrm{a}'} + V_{\mathrm{b}'} + V_{\mathrm{c}'}}{3} \tag{6.1}$$

whereas each of the three phase-DM noise spectra can be determined by the corresponding LISN measurement output and the CM noise as

$$V_{\mathrm{DM},x} = V_{x'} - V_{\mathrm{CM}} \quad \text{with} \quad x = \{\mathrm{a}, \mathrm{b}, \mathrm{c}\} \quad . \tag{6.2}$$

Consequently, the line-DM noise spectra can be obtained by the subtraction of two phase-measurement outputs as

$$V_{\mathrm{DM},xy} = V_{x'} - V_{y'} \quad \text{with} \quad xy = \{\mathrm{ab}, \mathrm{bc}, \mathrm{ca}\} \quad . \tag{6.3}$$

Equations (6.1) to (6.3) are referred to as noise separation. Typically, swept-tuned spectrum analyzers acquire only the magnitude information over a broad

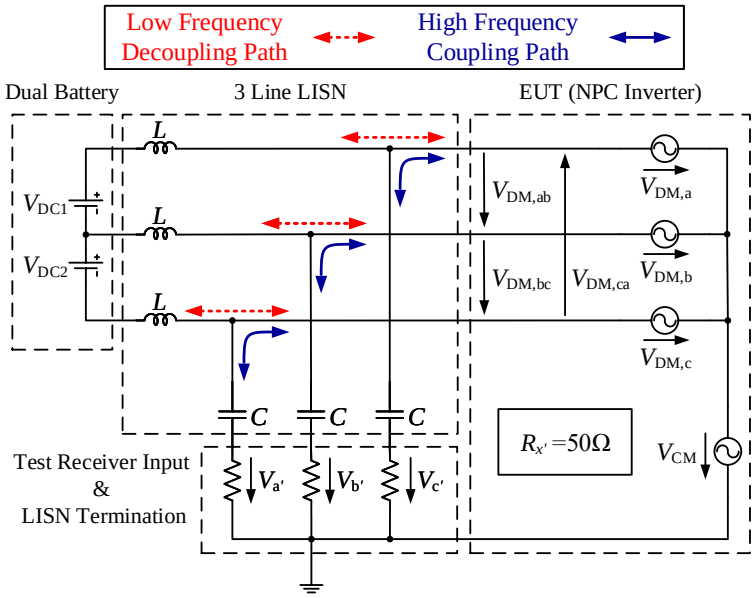
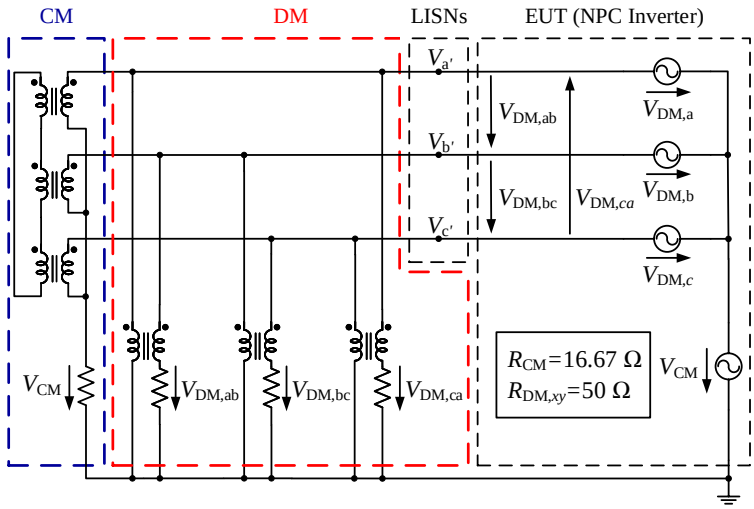


Figure 6.1: Schematic of the noise measurement for the NPC inverter, including three LISNs. The *LC*-filter couples the high frequency noise of the EUT into the measurement receiver.

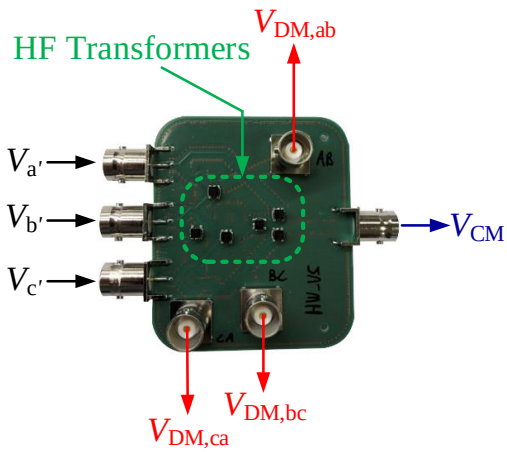
frequency range, so that these cannot distinguish between DM and CM quantities. On the other hand, real-time spectrum analyzers, such as a fast fourier transform analyzer, can acquire both magnitude and phase information, but the frequency range is limited to low frequency signals up to 150 kHz. Therefore, the noise separation is quite challenging, since the phase angle of the noise components must be taken into account over a broad frequency up to several MHz (CISPR 25: 150 kHz $\leq f \leq$ 108 MHz). In order to overcome the limited frequency range, an additional hardware separator, which is inserted between the three LISNs' outputs and the spectrum analyzer, can be used.

6.1.1 Noise Separation Based on HF Transformers

Two compact hardware separators based on small circuit HF transformers were developed for the DC side of the fault-tolerant NPC inverter, including its additional neutral point connection. Both separator topologies are based on [156, 157], which were originally intended to be used for power electronic systems connected to the three-phase mains (AC-side). Similar analyses regarding the design and characterization of hardware separators using small circuit transformers can be



(a)

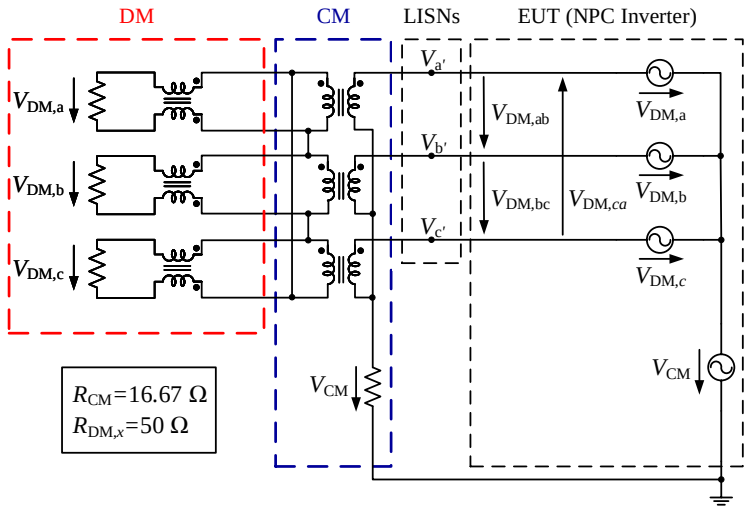


(b)

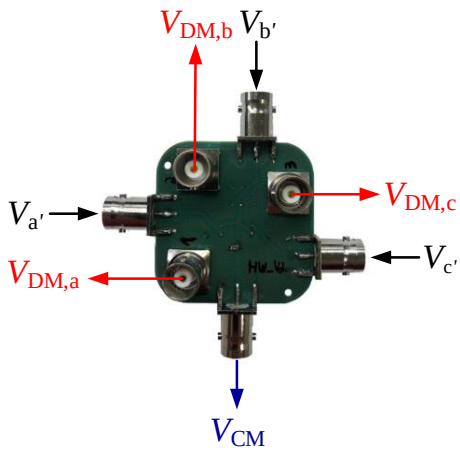
Figure 6.2: **CM and line-DM separation** using HF transformers. (a) Schematic separation of the high frequency noise coupled into the LISN. (b) PCB of the corresponding separator.

found in [158, 159]. Figs. 6.2 and 6.3 show the equivalent circuit diagrams and the PCB designs of the separators.

Both separators utilize the same CM separation technique, whereas the DM measurement differs. The first separator, shown in Fig. 6.2, measures the line-DM quantities. Here, the DM separation is placed directly at the terminals



(a)



(b)

Figure 6.3: **CM and phase-DM separation** using HF transformers. (a) Schematic separation of the high frequency noise coupled into the LISN. (b) PCB of the corresponding separator.

of the LISNs with an adjacent connection of the DM mode separation part. The second separator, shown in Fig. 6.3, measures the phase-DM quantities. Here, the CM separation is placed directly at the terminals of the LISNs with an adjacent connection of the CM mode separation part. It should be noted that, when using either of the separators, the output terminations (50 Ω) of the LISNs should not

be affected. Thus, all DM outputs must be terminated by 50 Ω and the CM output must be terminated by 50/3 Ω, as described in [156, 157]. Since the CM output of the separators has an internal 25 Ω resistor mounted on the PCB, the required termination resistances are achieved by using external 50 Ω terminators or the input impedance of the spectrum analyzer. For the PCB realization, the TC1-42x+ [161] small circuit HF-transformers from Minicircuits were selected, achieving a very compact and cost effective separator design in comparison to [156–159]. The chosen HF transformers have an operational frequency range from 250 kHz up to 400 MHz with a typical insertion loss of 0.3 dB. In Fig. 6.3 the HF transformers are not visible, since these are placed on the backside of the PCB. In the following pages, separator one and two are referred to as CM/line-DM and CM/phase-DM separator, respectively. The consideration of line or phase DM noise should be chosen in accordance with possible mitigation techniques. For example, if the traction system is on a floating potential, it might be more suitable to consider line-DM noise levels and, thus, to apply X instead of Y-capacitors [162].

6.1.2 Characterization of the CM/line-DM Separator

The performance of the three-phase CM/line-DM noise separator can be characterized by the following quantities:

1. CM Transmission Ratio ($CMTR$):

$$CMTR(f) = 20\ \mathrm{dB} \cdot \log\left(\left| \frac{V_{\mathrm{CM,out}}}{V_{\mathrm{CM,in}}} \right| \right) \Bigg|_{\substack{V_{\mathrm{DM,a}}=0 \\ V_{\mathrm{DM,b}}=0 \\ V_{\mathrm{DM,c}}=0}} \tag{6.4}$$

2. Line-DM Transmission Ratios ($DMTR_{xy}$):

$$DMTR_{xy}(f) = 20\,\mathrm{dB} \cdot \log\left(\left| \frac{V_{\mathrm{DM},xy,\mathrm{out}}}{V_{\mathrm{DM},xy,\mathrm{in}}} \right| \right) \Bigg|_{\substack{V_{\mathrm{DM},y}=-V_{\mathrm{DM},x} \\ V_{\mathrm{DM},z}=V_{\mathrm{CM}}=0}} \tag{6.5}$$

$$\text{with } xyz = \{\mathrm{abc}, \mathrm{bca}, \mathrm{cab}\}$$

3. CM Rejection Ratios ($CMRR_{xy}$):

$$CMRR_{xy}(f) = 20\,\mathrm{dB} \cdot \log\left(\left| \frac{V_{\mathrm{DM},xy,\mathrm{out}}}{V_{\mathrm{CM,in}}} \right| \right) \Bigg|_{\substack{V_{\mathrm{DM,a}}=0 \\ V_{\mathrm{DM,b}}=0 \\ V_{\mathrm{DM,c}}=0}} \tag{6.6}$$

$$\text{with } xy = \{\mathrm{ab}, \mathrm{bc}, \mathrm{ca}\}$$

4. Line-DM Rejection Ratios ($DMRR_{xy}$):

$$DMRR_{xy}(f) = 20\,\mathrm{dB} \cdot \log\left(\left| \frac{V_{\mathrm{CM,out}}}{V_{\mathrm{DM},xy,\mathrm{in}}} \right| \right) \Bigg|_{\substack{V_{\mathrm{DM},y}=-V_{\mathrm{DM},x} \\ V_{\mathrm{DM},z}=V_{\mathrm{CM}}=0}} \tag{6.7}$$

$$\text{with } xyz = \{\mathrm{abc}, \mathrm{bca}, \mathrm{cab}\}$$

The measured CM and line-DM characteristics of the separator are shown in Figs. 6.4(a) and 6.4(b), respectively. The Common Mode Transmission Ratio (CMTR) and the Differential Mode Transmission Ratios (DMRR) are essentially 0 dB for the considered frequency range, so that the CM and DM noises are transmitted undiminished to the corresponding outputs. The CMRRs of the three DM outputs are at least −42 dB, which corresponds to an attenuation of 0.79 % relative to the input signal. The DMRR characteristics show an attenuation lower than −32 dB for up to 30 MHz and −21 dB for up to 110 MHz, which corresponds to an attenuation relative to the input signal of 2.5 % and 8.91 %, respectively. It can be seen that both CMRRs and DMRRs show a slight asymmetric behavior. This, however, is not crucial due to the high attenuation factors.

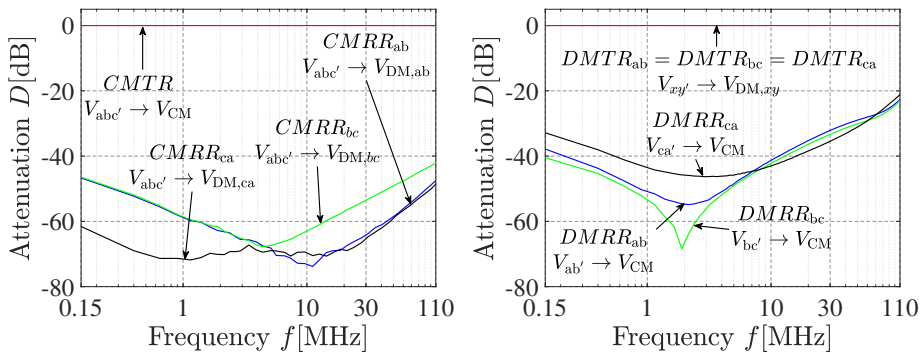


Figure 6.4: (a) Common mode and (b) differential mode characteristic of the **CM/line-DM separator**.

6.1.3 Characterization of the CM/phase-DM Separator

The performance of the three-phase CM/phase-DM noise separator can be characterized by the following quantities:

1. CM Transmission Ratio ($CMTR$):

$$CMTR(f) = 20\,\mathrm{dB} \cdot \log\left(\left| \frac{V_{\mathrm{CM,out}}}{V_{\mathrm{CM,in}}} \right| \right) \Bigg|_{\substack{V_{\mathrm{DM,a}}=0 \\ V_{\mathrm{DM,b}}=0 \\ V_{\mathrm{DM,c}}=0}} \tag{6.8}$$

2. Phase-DM Transmission Ratios ($DMTR_x$):

$$DMTR_x(f) = 20\,\mathrm{dB} \cdot \log\left(\left| \frac{V_{\mathrm{DM},x,\mathrm{out}}}{V_{\mathrm{DM},x,\mathrm{in}}} \right| \right) \Bigg|_{\substack{V_{\mathrm{DM},y}=-V_{\mathrm{DM},x} \\ V_{\mathrm{DM},z}=-V_{\mathrm{DM},x} \\ V_{\mathrm{CM}}=0}} \tag{6.9}$$

$$\text{with } xyz = \{\text{abc}, \text{bca}, \text{cab}\}$$

3. CM Rejection Ratios ($CMRR_x$):

$$CMRR_x(f) = 20\,\text{dB} \cdot \log\left(\left| \frac{V_{\text{DM},x,\text{out}}}{V_{\text{CM,in}}} \right| \right) \Bigg|_{\substack{V_{\text{DM,a}}=0 \\ V_{\text{DM,b}}=0 \\ V_{\text{DM,c}}=0}} \tag{6.10}$$

$$\text{with } x = \{\text{a}, \text{b}, \text{c}\}$$

4. Phase-DM Rejection Ratios ($DMRR_x$):

$$DMRR_x(f) = 20\,\text{dB} \cdot \log\left(\left| \frac{V_{\text{CM,out}}}{V_{\text{DM},x,\text{in}}} \right| \right) \Bigg|_{\substack{V_{\text{DM},y}=-V_{\text{DM},x} \\ V_{\text{DM},z}=-V_{\text{DM},x} \\ V_{\text{CM}}=0}} \tag{6.11}$$

$$\text{with } xyz = \{\text{abc}, \text{bca}, \text{cab}\}$$

The measured CM and phase-DM characteristics of the separator are shown in Figs. 6.5(a) and 6.5(b), respectively. Again, the Common Mode Transmission Ratio (CMTR) and the Differential Mode Transmission Ratios (DMRR) are close to 0 dB for the considered frequency range, so that the CM and DM noises are transmitted undiminished to the corresponding outputs. The CMRRs of the three DM outputs are at least −33 dB, whereas the attenuation at low frequencies is up to about −78 dB. The DMRR characteristics show an attenuation of at least −33 dB, which corresponds to an attenuation of 1.6 % relative to the input signal. It can be seen that the DMRRs are symmetrical, whereas the DMRRs show a slightly asymmetric behavior, however, less pronounced than for the CM/line-DM separator.

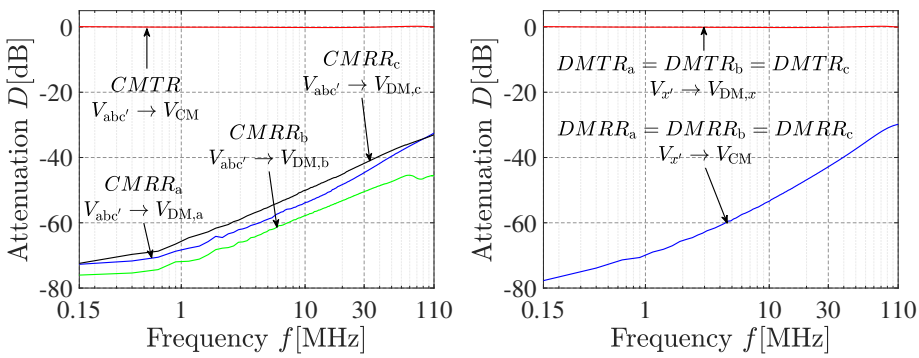
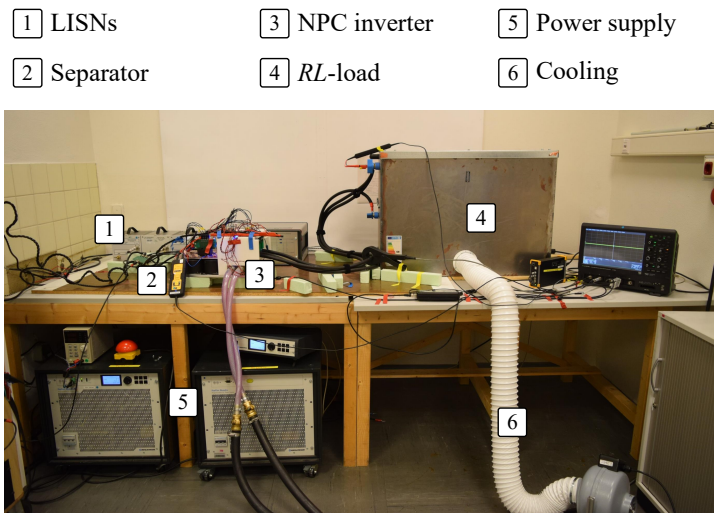


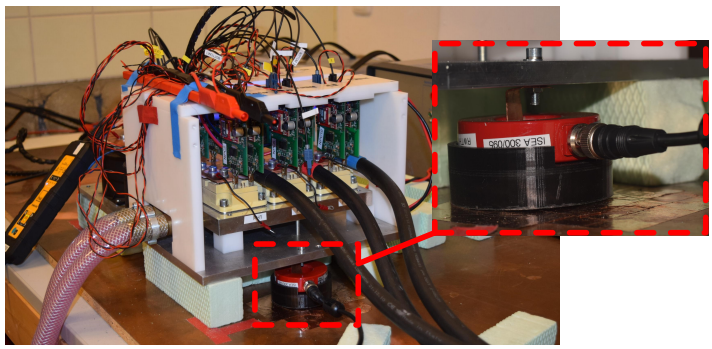
Figure 6.5: (a) Common mode and (b) differential mode characteristic of the **CM/phase-DM separator**.

6.2 Experimental Results

The previously described hardware separators are used to quantify the DM and CM noise levels of an NPC inverter with a connected neutral point, so that their performance can be validated. The used prototype of the IGBT-based three-level NPC inverter can be seen in the previous chapter in Fig. 5.14(b). It utilizes the SKM300MLI066TAT [163] three-level half-bridge modules from Semikron, with



(a)



(b)

Figure 6.6: (a) EMI measurement testbench for the three-level NPC inverter and (b) current sensor mounting to measure the parasitic current through the ground plate.

a nominal blocking capability of 600 V and a current rating of 300 A. For safety reasons, a nominal DC-link voltage of $V_{\mathrm{DC}} = 400\,\mathrm{V}$ is chosen, so that each DC-link capacitor is supplied by about 200 V. In a real application, a DC link voltage of 800 V would be an appropriate choice for the chosen IGBT blocking voltage capability. A custom-made three-phase *RL*-load, utilizing an air-core coil, is used as an artificial machine load. The load is suggested to mimic an induction machine at standstill. Due to the absence of a back emf, the derivative of the current ripple (di/dt) is theoretically the highest [164, 165]. Thus, for an actual application, when using an electric machine, the measurement results could be different. Each phase of the artificial machine load has a nominal inductance of 220 µH and a resistance of about 50 mΩ, resulting in a power factor $\cos\phi$ close to zero. The current rating is about $125\,\mathrm{A_{RMS}}$ when using forced air cooling. The complete laboratory test bench can be seen in Fig. 6.6(a), built according to the standard CISPR series 16 [166]. The surface of the test bench is covered by a copper sheet (ground plate). Spacers were used to have a defined distance of 5 cm between the test equipment and the ground plate. A current sensor is mounted on a flat copper bar between the inverter's heatsink and the ground sheet, as can be seen in Fig. 6.6(b), to measure the parasitic current through the ground plate. The power modules are electrically insulated from the heatsink by the internal ceramic substrate and the star point of the RL-load is floating.

During the investigation, the inverter is operated either with three-level space vector modulation, as described in [142], or with classical two-level space vector modulation (avoidance of small and medium vectors shown), changing the instantaneous output voltage in (3.2) to

$$v_{\mathrm{abcN}} = \frac{V_{\mathrm{DC}}}{2} S_{\mathrm{abc,NPC}} \quad \text{with} \quad S_{\mathrm{abc,NPC}} = \{1, -1\} \quad . \tag{6.12}$$

The two-level modulation resembles an operation under an inverter fault condition, as for example an open circuit fault of a diode in the clamping path [78]. A switching frequency of 10 kHz is chosen and an open-loop control approach, using a fixed modulation index, is selected. The blanking time and the voltage drop across the semiconductor switches are not taken into account. It should be noted that the switching frequency of a multilevel inverter is referred to as the average frequency at which a phase leg is operated and should not be misinterpreted as the average switching frequency of individual semiconductor switches [72]. The fundamental frequency f_1 is set to 500 Hz and the modulation indices are chosen to be 3.75 % and 7.5 % for the two-level and the three-level modulation, respectively. Due to absence of a back-emf, the maximum possible modulation index is about 23 % and, furthermore, the derivative of the current ripple is unaffected by the

modulation index. Thus, the noise levels are unaffected by the modulation index as well. Fig. 6.7 shows the load current in phase a when using two-level and three-level operation. It can be observed that a displacement current is triggered at each switching event. As shown in Fig. 6.7, the three-level modulation reduces the peak of the displacement current by about 50 %. It should be noted that no EMI filter is applied.

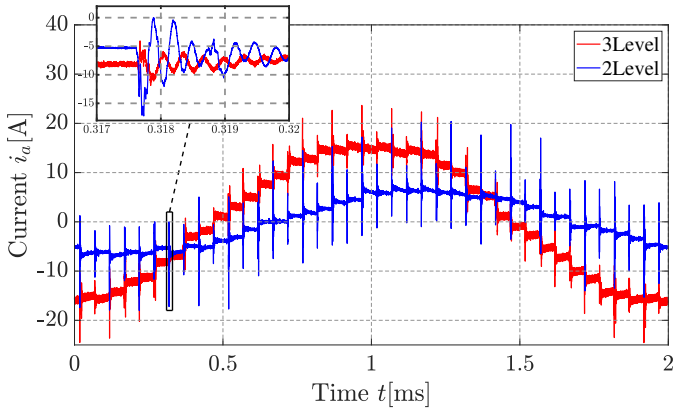


Figure 6.7: Single-phase load currents for three-level and two-level operation of the three-level NPC inverter.

6.2.1 Emission Levels at LISNs' Outputs

When operating the inverter, the outputs of the three LISNs are at first individually connected to the spectrum analyzer. Later these are connected to the noise-separator and the measured noise signal is fed from the testbed to the spectrum analyzer. Fig. 6.8 shows the spectra obtained at the outputs of the three LISNs measured with a peak detector. A Gaussian filter is selected. The spectrum analyzer's resolution bandwidth is set to 3 kHz. Since the CISPR 25 recommends a video bandwidth of at least three times the resolution bandwidth [57], the spectrum analyzer automatically adjusted the video bandwidth to 30 kHz, which resulted in a sweep time of about 16.5 s. Three typical resonances can be observed in Fig. 6.8. One resonance valley occurs around 225 kHz, while a second dominant resonance peak is present at about 1 MHz. A smaller resonance peak is also located around 25 MHz. These three resonance points can be associated with the in [56, 76, 155] described and modeled LISN, artificial machine load and power module oscillations, respectively. As can be seen from the three LISNs' outputs, the module resonance

is not symmetrical. The highest noise level is observed at the negative DC-link rail ($V_{c'}$). Furthermore, it can be seen that the three-level in comparison to the two-level modulation does not only reduce the noise level by 3 dB to 6 dB, it affects also the module resonance frequency.

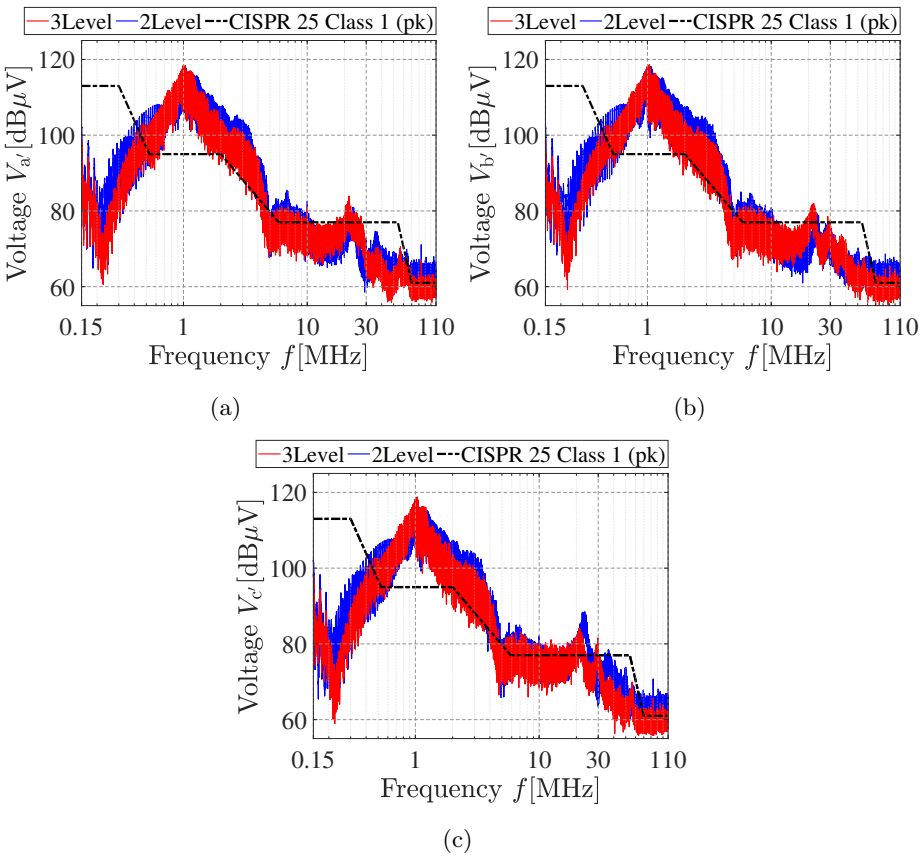


Figure 6.8: Three and two-level noise spectra at (a) positive, (b) neutral and (c) negative DC link rail.

6.2.2 Separated Noise Spectra

To validate the performance of the separators, the measured noise levels are separated into CM, line-DM and phase-DM quantities with the previously described hardware separators.

CM & Line-DM Noise Levels

Figs. 6.9(a) and 6.9(b) show the separated CM and one line-DM ($V_{\mathrm{DM,ab}}$) spectrum, respectively, measured with the CM/line-DM separator. Since the three line-DM spectra show similar noise levels, just $V_{\mathrm{DM,ab}}$ is shown here. Similar to the two-level inverter investigation in [154], the CM is also predominant for the three-level NPC inverter with connected neutral point. It can be seen that the noise levels using two-level operation are slightly increased by 3 dB up to 6 dB for both CM and DM. Furthermore, as modeled in [76], it is observed that the LISN and artificial machine load resonances are driven by the CM, whereas the module resonance is driven by the DM. Regarding the power module resonance, the two-level in comparison to the three-level modulation shifts the resonance frequency from about 25 MHz to 21 MHz and the noise level is reduced by about 3 dB.

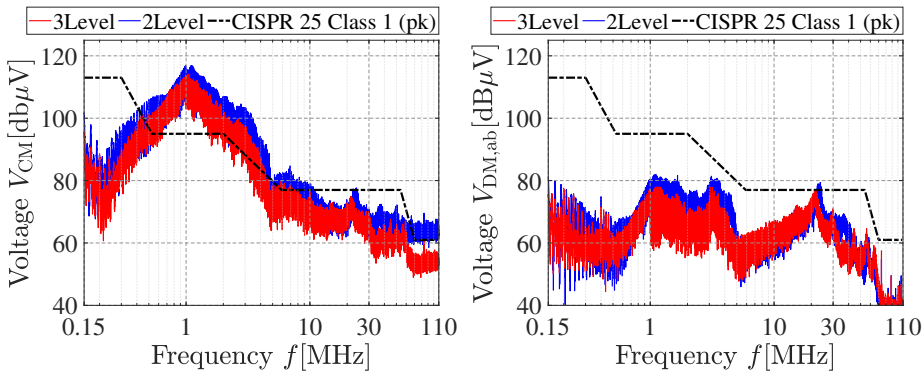


Figure 6.9: Measured (a) **CM** and (b) **line-DM** ($V_{\mathrm{DM,ab}}$) noise, when operating the three-level NPC inverter with two-level and three-level modulation.

CM & Phase-DM Noise Levels

The obtained results of the CM/phase-DM separator can be seen in Fig. 6.10. Regarding the CM, a similar noise spectrum as for the CM/line-DM separator is obtained, as shown in Fig. 6.10(a). Figs. 6.10(b) and 6.10(c) show the phase-DM spectra $V_{\mathrm{DM,a}}$ and $V_{\mathrm{DM,b}}$, respectively. The third phase-DM spectrum $V_{\mathrm{DM,c}}$ is not displayed, since it does not qualitatively differ from $V_{\mathrm{DM,a}}$. $V_{\mathrm{DM,a}}$ shows a similar spectrum as $V_{\mathrm{DM,ab}}$, while the phase quantities seem slightly increased compared to the line quantities. When in two-level operation, $V_{\mathrm{DM,b}}$ shows a significant noise reduction in the range above 4 MHz, since the zero switching state

of each phase leg is not used and the power module oscillation is not triggered. The spectrum at lower frequencies is not effected.

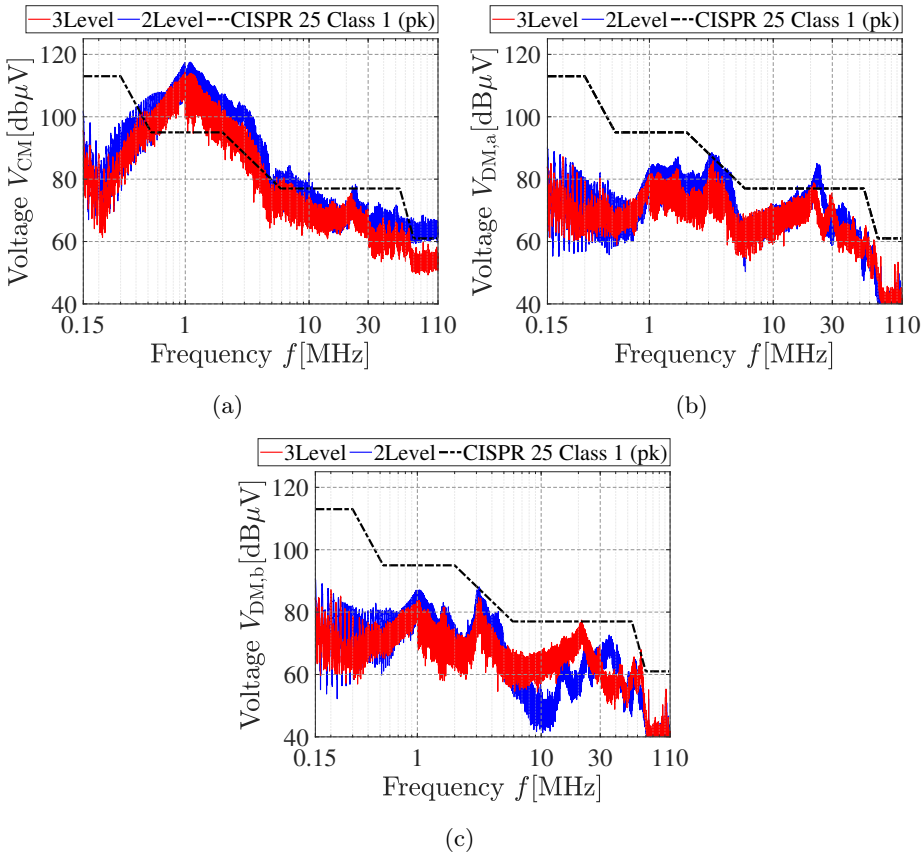
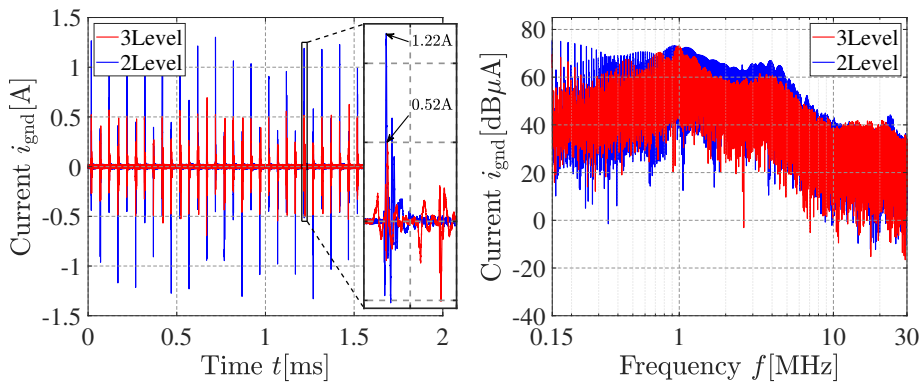


Figure 6.10: Measured (a) **CM** and (b) **phase-DM** at positive ($V_{DM,a}$) and (c) neutral DC-link rail ($V_{DM,b}$), when operating the three-level NPC inverter with two-level and three-level modulation.

6.2.3 Parasitic CM Current over the Ground Plate

Typically, the high voltage traction system in an EV is isolated. Although, the unwanted parasitic currents, capacitively or inductively coupled, in the motor bearings [48] or the vehicle's chassis are other criteria to assess the electromagnetic emissions of the traction inverter and can be used to verify the measured CM noise reduction. For this purpose, a current sensor was mounted on a flat copper bar between the inverter's heatsink and the ground plate, as can be seen in Fig. 6.6(b).

The power modules are electrically insulated from the heatsink by the internal ceramic substrate and the star point of the *RL*-load is floating. The measured waveforms of the parasitic currents through the ground plate can be seen in the time and frequency domain in Fig. 6.11(a) and Fig. 6.11(b), respectively. At each switching event, a displacement current is triggered, generating broadband emissions. It can be seen that the three-level modulation reduces the peak of the current spikes/oscillations by about 50 %, which is consistent with the previously measured noise reduction of about 6 dB. In the logarithmic plot shown in Fig. 6.11, the characteristic of the artificial machine load at 1 MHz, as described in [56,76,155], can be recognized and it can be seen that the emissions at the sidebands are reduced by about 3 dB to 6 dB. This in turn confirms the acquired CM results of the separators.



(a) (b)

Figure 6.11: Measured parasitic current through the ground plate (a) in time and (b) in frequency domain, when operating the three-level NPC inverter with two-level and three-level modulation.

Conclusions

In this thesis, the potential of modular battery systems based on multilevel inverter topologies for vehicle propulsion applications in comparison to classical, two-level IGBT inverter drivetrains is investigated. The key aspects considered for this comparative investigation are the drive cycle efficiency of the inverter as well as the battery system, the electromagnetic emission levels, the system's fault tolerance capability and the inverter cost. Advantages of different output voltage modulation techniques, reducing the inverter's switching losses and the motor's current THD, are compared as well. In addition, advanced online and on-board battery diagnostics are derived.

When estimating and comparing the drive cycle efficiency of modular battery systems with low-voltage MOSFETs, it is of utmost importance to consider MOSFET's reverse conduction capability (third-quadrant characteristic) and, furthermore, a dynamic battery model with two or three *RC*-pairs should preferably be used. Otherwise, the inverter conduction losses and the ohmic battery losses would be significantly overestimated. For example, it is shown and experimentally verified for a three-phase, two-level SiC MOSFET inverter that the neglect of MOSFET's reverse conduction capability can lead to a relative overestimation of the inverter conduction losses of 13.5 % to 159.3 % when operated at partial load. Furthermore, it is experimentally verified that a simple resistive battery model overestimates the ohmic battery losses of modular battery systems based on MLIs by about 20 %.

Based on the suggested loss-modeling approaches, the drive cycle efficiency of a seven-level CHB and a seven-level CDHB inverter with MOSFETs are estimated and compared to a two-level IGBT inverter when used in a small passenger car. The chosen reference two-level inverter drivetrain has a nominal voltage of about

400 V and a battery capacity of about 45 kWh. Typically, the partial load efficiency of the MOSFET-based MLIs is increased in comparison to the two-level IGBT inverter and, thus, the inverter drive cycle efficiency of the MLIs is increased as well. For instance, the seven-level CHB inverter's WLTP drive cycle efficiency in comparison to the IGBT two-level inverter is increased from 97.49 % to 98.54 %. In contrast, it is seen that the ohmic battery losses of the modular battery systems are increased due to the additional low and medium frequency current harmonics that are drawn from the individual battery packs. The seven-level CDHB inverter reduces the ohmic battery losses in comparison to the seven-level CHB inverter and achieves a battery efficiency of about 96.32 %, but the obtained battery efficiency of the two-level inverter drivetrain is 96.66 %. Nonetheless, when considering the combined efficiency, the drive cycle efficiency of the seven-level CDHB in comparison to the two-level inverter is increased from 94.23 % to 95.04 %. The total efficiency of the seven-level CHB inverter is similar to that of the two-level inverter system. Here, it is worth noting that the CHB inverter utilizes only 36 of the OptiMOS MOSFETs from Infineon, whereas the CDHB utilizes 60. Nevertheless, with the help of a derived hybrid modulation technique, using PWM at lower and FSHE at higher speeds, it is shown that the total WLTP drive cycle efficiency of the seven-level CHB inverter can be improved to about 94.85 %. If the battery capacity would be increased further, the ohmic battery losses would be reduced as well and, thereby, the increased battery losses of the MLIs would constitute a smaller part of the total drive cycle efficiency.

Furthermore, it is shown that the inverter cost of the two-level IGBT in comparison to a similar rated seven-level CHB and CDHB inverter is reduced from 342 € to 121 € and 202 €, respectively. The costs for the additional gate drivers are presumably increased. Nonetheless, modular battery systems inherently act as a part of the battery management system and individual modules can be used as low-voltage auxiliary supplies. Therefore, the suggested seven-level MLIs are cost-effective solutions in comparison to the two-level IGBT inverter system.

Based on a simple three-level NPC inverter with a dual battery pack, which is one of the simplest types of modular battery systems, it is shown that modular battery system based on multilevel inverters inherently provide a certain fault tolerance capability. With the help of the three-level space vector diagram it is illustrated that an active NPC inverter can cope with permanent single type faults, such as an open or short-circuit fault of an individual semiconductor switch or the malfunctioning of an individual battery pack. Still, the fault location must be properly localized so that the remaining valid space vectors can be properly utilized and the vehicle can be brought to reduced performance mode, referred

to as limp home mode. Especially, open circuit faults are difficult to detect and localize. Therefore, a current estimator solution to recognize fault conditions and two localization techniques, a pulse pattern injection principle and an online adaption of the space vector modulation, are suggested. It is experimentally demonstrated that an open circuit fault of an outer switch of the NPC inverter can be easily detected and localized with the help of the pulse pattern principle. Subsequently, the inverter can be operated further in single-source operation, but its possible output power rating is halved due to the open circuit fault.

Moreover, the conducted emission levels of a three-level NPC with a dual battery supply are experimentally investigated. Due to the additional neutral point connection, the three-level NPC inverter's DC side forms a special three-wire CM/DM system. This fact has brought up the question how to actually measure the conducted emission levels according to the governing standard, CISPR 25, and this aspect has also shown that it is quite intricate to measure the conducted emissions levels of modular battery systems, because these comprise multiple DC sources. It is shown that three instead of two LISNs are actually required for the measurement of the NPC inverter's conducted emissions and, thus, it must be dealt with a three-wire CM and DM system. Therefore, two very compact CM/DM separator prototypes, one for the line-DM and for the phase-DM quantities, have been built and their CM/DM frequency characteristics are measured, showing reasonable noise transmission and rejection ratios. An EMI testbed with three LISNs is used to measure the conducted noise of the fault-tolerant three-level NPC inverter, which is operated with two-level and three-level modulation. Based on the measurements, it is seen that the CM noise levels are dominant. Furthermore, the three-level in comparison to the two-level modulation decreases the CM noise levels by about 3 dB to 6 dB.

So far, the drive cycle losses of the electric machine have not been taken into account. It is only shown that MLIs reduce the inverter-induced current ripple in comparison to a two-level inverter, which should presumably decrease the iron losses of the electric machine. Not been covered and fully explored yet either have been the aging process of MLI battery systems and the cost-effective utilization of an automotive data bus, such as CAN, to achieve a synchronous PWM control for MLI based battery systems. Hence, in a future work, the drive cycle efficiency of the entire powertrain, including the electric machine, should be quantified. Moreover, the aging of MLI battery systems should be assessed and the influence of the output voltage modulation technique, such as multilevel PWM or FSHE, should be determined. Additionally, it should be investigated how and to which extent a data bus, such as CAN or SPI, could be utilized to transmit

the individual gate signals of the converter modules, so that a synchronous PWM control can be cost-effectively achieved.

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Appendix

A.1 Vehicle and Motor parameters

Table A.1: Small passenger car and motor model parameters

(a) Vehicle

	Value	Unit
Vehicle mass m_{veh}	1500	kg
Occupant weight m_{occ}	75	kg
Frontal area A	2.2	m^2
Drag cofficient C_{d}	0.30	
Rolling resistance C_{r}	0.012	
Wheel radius r_{wheel}	0.316	m
Gear box ratio G_{r}	10.2	
Gearbox efficiency η_{G}	95	%
Top speed v_{max}	140	km/h

(b) Motor

	Value	Unit
Stator resistance R_{s}	20	mΩ
D-axis inductance L_{d}	250	µH
Q-axis inductance L_{q}	700	µH
Flux constant ψ_{m}	75	mWb
Pole pairs n_{p}	4	
Max torque T_{max}	200	Nm
Max phase current I_{RMS}	190	A
Max phase voltage V_{RMS}	200	V
Max speed n	12000	rpm

A.2 Battery Cell Impedance

Table A.2: Battery cell parameters of LG Chem CR18650 C2 2800 mAh

R_0[mΩ]	R_1[mΩ]	R_2[mΩ]	R_3[mΩ]	C_1[mF]	C_2[mF]	C_3[F]	L[nH]
41.53	5.02	7.32	3.23	75.44	339.5	3.625	590.8