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FPGA IMPLEMENTATION OF MOVING OBJECT AND FACE DETECTION USING ADAPTIVE THRESHOLD

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ABSTRACT

The real time moving object and face detections are used for various security applications. In this paper, we propose FPGA implementation of moving object and face detection with adaptive threshold. The input images are passed through Gaussian filter. The 2D-DWT is applied on Gaussian filter output and considered only LL band for further processing to detect object/face. The modified background subtraction technique is applied on LL bands of input images. The adaptive threshold is computed using LL-band of reference image and object is detected through modified background subtraction. The detected object is passed through Gaussian filter to get final good quality object. The face detection is also identified using matching unit along with object detection unit. The reference image is replaced by face database images in the face detection. It is observed that the performance parameters such as TSR, FRR, FAR and hardware related results are improved compared to existing techniques.

KEYWORDS

Discrete Wavelet Transform, Gaussian Filter, Adaptive Threshold, Object Detection, Face Recognition.

1. INTRODUCTION

Biometrics are used to identify and verify persons based on their physical and behavioural characteristic parameters. The physical characteristic traits are fingerprint, Iris, Palm print, DNA etc., of a person and are constant throughout life span. The recognition using physiological traits are easy and require less number of samples to build high speed real-time biometric system efficiently with less complexity. The recognition using behavioural traits are not very accurate and require more number of samples to build real time biometric system. The behavioural

biometric traits are signature, voice keystroke gait etc., and are time variant parameters. The general biometric system has three sections to recognise a person viz., pre-processing, feature extraction and matching section. In pre-processing section, the images are resized, colour conversion, noise removal etc., are performed to enhance quality of images. The features like mean, variance, standard deviation and principal component analysis are extracted in spatial domain by directly manipulating enhanced image. The features are extracted from enhanced image using spatial domain features are parameters corresponding direct manipulation on images directly such as mean, variance and standard deviations and also principal component analysis (PCA).The transform domain features are extracted from Fast Fourier Transform (FFT), Discrete Cosine Transform (DCT), Discrete Wavelet Transform (DWT), Dual Tree Complex Wavelet Transform (DTCWT) etc., Features are also extracted by fusing spatial and transform domain features for better identification. The Euclidian distance (ED), Hamming Distance, Neural Network, Support vector machine etc., are used in matching section to compute similarities and distance and differences among images.The microcontrollers, DSP Processors, FPGA etc., are used to build real time biometric systems. The biometric systems are used in application like authentication of a person, access to computers, entry in to vehicles, Cloud computing, Bank transactions, Intellectual property access etc.

In this paper we propose FPGA Implementation of Moving Object and Face Detection using Adaptive Threshold. The Gaussian filter, DWT, modified background subtraction and adaptive threshold techniques are used to detect moving object and recognize face effectively. One of the major advantages of proposed technique is that, the adaptive threshold approach is used to compute variable reference values for different object and face image of different persons.

The contribution and novel aspects of the proposed techniques are listed as follows

i. The computed threshold values are varied based on characteristics of images i.e., the threshold values are computed adaptively based on characteristics of the images.

ii. The modified background subtraction technique is used on filtered LL coefficients of background image/Face database and actual image/Test face image to compute absolute difference between LL coefficients of two sets of images. The absolute difference is compared with adaptive threshold values to detect object.

iii. The object detection architecture is extended to face detection by using global threshold and matching unit blocks.

iv. The performance parameters are improved since adaptive threshold, modified background subtraction and filters used in the architecture.

2. LITERATURE SURVEY

Surveillance plays important role in-terms of providing security and many security issues can be solved by surveillance of video sequences by only considering the changes in the scene of video sequences. The detected foreground moving object will reduce the bandwidth for transmission. B. Ugur et al., [1] proposed moving object detection in transform domain. The Dubechies wavelet transform used to convert the spatial domain and applied to background subtraction to obtain foreground. Shih-Wei Sun et al., [2] proposed object detection based on SIFT trajectory. This

method does not require any training data or interaction by user. Based on the SIFT correspondence frame SIFT trajectories are calculated for foreground features. Chang Liu et al., [3] proposed the uses of visual saliency for moving object detection via direct analysis of video which is represented by information saliency map. In this method both spatial and temporal saliencies are calculated and constructed information saliency map which is further used for detecting foreground information.

The Discrete Wavelet Transform (DWT) is a transform domain technique [4] which having time-frequency resolution and multilevel decomposition. The DWT mainly uses two sets of FIR filters i.e., low pass filter and high pass filter where the output of each filter is a sub-band. The low pass filter output to generate approximation coefficients which have significant information of an image and high pass filter output generate detailed coefficients which have no significant information of an image. The lifting scheme of DWT computation has become more popular compared with convolution based technique for its lower computational complexity [5]. Andra et al., [6] proposed four-processor architecture for 2D-DWT which is used for block based implementation for 2D-DWT, which requires large memory. Liao et al., [7] proposed 2D-DWT dual scan architecture, which requires two lines of data samples simultaneously for forward 2DDWT and also proposed another 2D-DWT architecture, which accomplished decomposition of all stages resulting in inefficient hardware utilization and more sophisticated control circuitry. Barua et al., [8] proposed folded based architecture for 2D-DWT by using hybrid level at each stage.

A number of defence, security and commercial applications demand real time face recognition system [9]. The algorithm proposed by Fei Wang et al., [10] uses spectral features for face recognition which is a nonlinear method for face feature extraction. The algorithm can detect nonlinear structure present in the face image and this structure is then used for recognition purpose. Ben Niu et al., [11] proposed two dimensional Laplacian face method for face detection. The algorithm based on locality preserved embedding and image based projection techniques which preserve geometric structure locality of sample space to extract face feature. The performance of the algorithm is checked by using FERET and AR database. Sajid et al., [12] proposed FPGA implementation of face recognition system. The system uses Eigen values for recognition purpose. To eliminate floating point Eigen value software-hardware co-design is used with partial re-configurability. Guo and Lu [13] proposed face detection based on Haar classifier which is implemented on FPGA. The uses of pipelined architecture decrease the recognition time. Chen and Lin [14] proposed minimal facial based face detection algorithm. The algorithm first check for skin and hair colored region and then it decide the face area. Veeramanikundan et al., [15] proposed FPGA implementation of face detection and recognition system under light intensity variation. The proposed algorithm based on the Adapting Boosting Machine learning algorithm with Haar transform which increase the accuracy of face recognition.

3. PROPOSED ARCHITECTURES

The architectures for Moving Object Detection and Face Detection are shown in Fig.1 and 2 respectively. The Gaussian filters are used to remove high frequency edges and some amounts of light variations present in the images. The filtered images are then fed to 2D-DWT block, where only LL band is considered because most of the valuable information of an image is available. The LL1 is the approximation band coefficients of image_in/test image and LL2 is the approximation band coefficients of image_ref/database. The adaptive threshold block is used to

compute the threshold by Modified Background Subtraction simultaneously along with 2DDWT block. The Modified Background Subtraction block is used to remove the background from LL band of actual image and then image is fed to Gaussian filter to remove any small light variations present in the image.

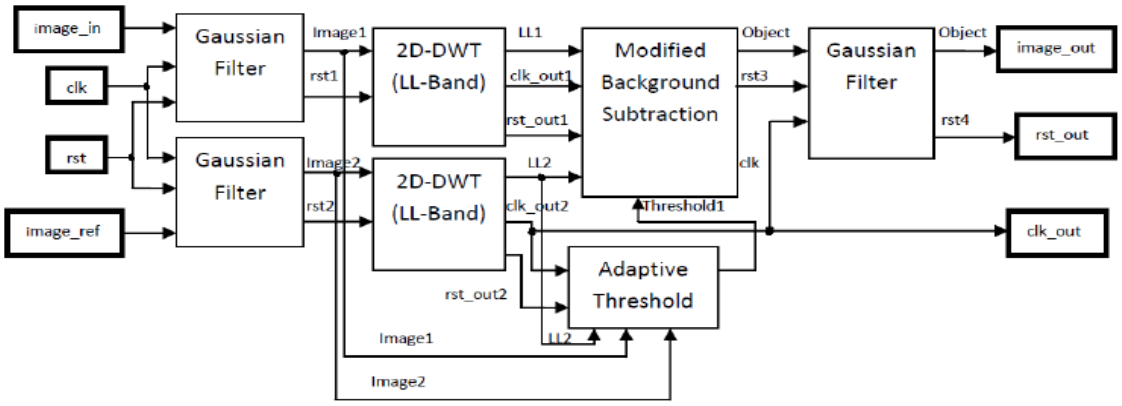

Figure 1. Proposed Architecture for Moving Object Detection

The Moving Object Detection block diagram is also used to detect face images by using Matching Unit at the end of Fig. 1. The ORL face database [16] is used to test the performance of the proposed face detection architecture.

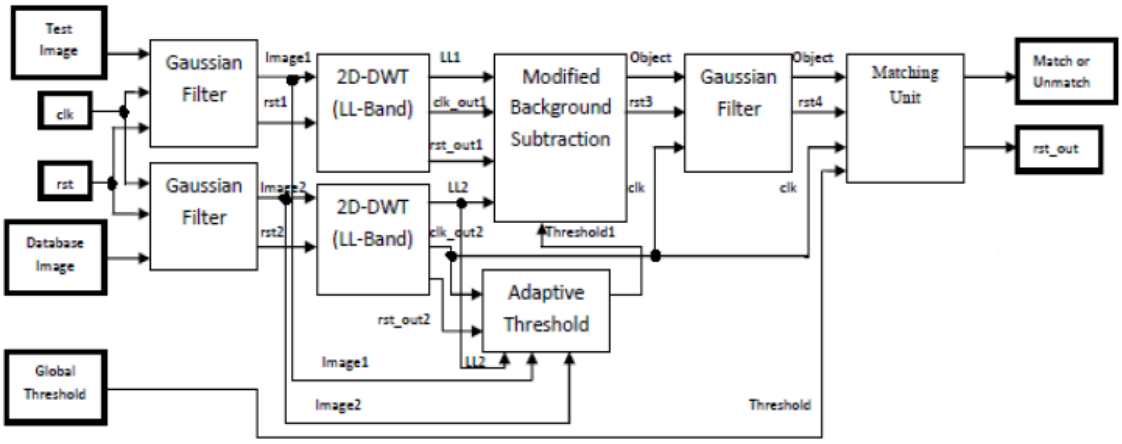

Figure 2. Proposed Architecture for Face Detection

3.1. Face Database

The ORL (Olivetti Research Laboratory) database [16] is used to test the performance of the system and it has 40 persons with 10 images per person i.e., it has 400 images in total. All images were captured at different times, varying the lighting, facial expressions and facial details. The images were taken against a dark homogeneous background with the subjects in an upright, frontal position with tolerance for some side movements. The face image samples of a single person is shown in figure 3. The original size of each image is 92x112 and is resized to 256x256, in the proposed architecture to implement on FPGA.

Figure 3. Ten Sample Images of a Person in ORL Database

3.2. Gaussian Filter

The filter is used to transform the image to smoothened image by removing high frequency edges. The basic equation for two dimensional Gaussian filter [17] is given in equation (1).

$$g(x,y) = \frac{1}{2\pi\sigma^2} e^{-\frac{x^2+y^2}{2\sigma^2}} \quad (1)$$

Where, x is the distance from the origin in the horizontal axis
y is the distance from the origin in the vertical axis
σ is the standard deviation of the Gaussian distribution.

The Gaussian mask filter of 3x3 is derived from equation (1) to obtain mask [17] given in equation (2).

$$Gaussian\ Mask = \frac{1}{16}\begin{bmatrix} 1 & 2 & 1 \\ 2 & 4 & 2 \\ 1 & 2 & 1 \end{bmatrix} \quad (2)$$

Then the Gaussian filter is given in equation (3) by multiplying Gaussian mask with 3x3 sub-matrix of an image.

$$Gaussian\ Filter = \frac{1}{16}\begin{bmatrix} 1 & 2 & 1 \\ 2 & 4 & 2 \\ 1 & 2 & 1 \end{bmatrix} * \begin{bmatrix} a_{33} & a_{32} & a_{31} \\ a_{23} & a_{22} & a_{21} \\ a_{13} & a_{12} & a_{11} \end{bmatrix} \quad (3)$$

Where, a_{11} to a_{33} are 3x3 sub-matrix pixel values of an image.

$$Gaussian\ Filter = \frac{1}{16}[(a_{33} + 2a_{32} + a_{31}) + (2a_{23} + 4a_{22} + 2a_{21}) + (a_{13} + 2a_{12} + a_{11})]$$

$$Gaussian\ Filter = \frac{1}{16}[(a_{33} + a_{31} + a_{13} + a_{11}) + 2(a_{32} + a_{23} + a_{21} + a_{12}) + 4a_{22}]$$

$$Gaussian\ Filter = \frac{1}{2^4}[(a_{33} + a_{31} + a_{13} + a_{11}) + 2^1(a_{32} + a_{23} + a_{21} + a_{12}) + 2^2 a_{22}]$$

$$Gaussian\ Filter = \frac{1}{(\gg 4)}[(a_{33} + a_{31} + a_{13} + a_{11}) + (\ll 1)(a_{32} + a_{23} + a_{21} + a_{12}) + (\ll 2)a_{22}] \quad (4)$$

The proposed hardware structure for Gaussian filter using equation (4) is shown in Fig.4.

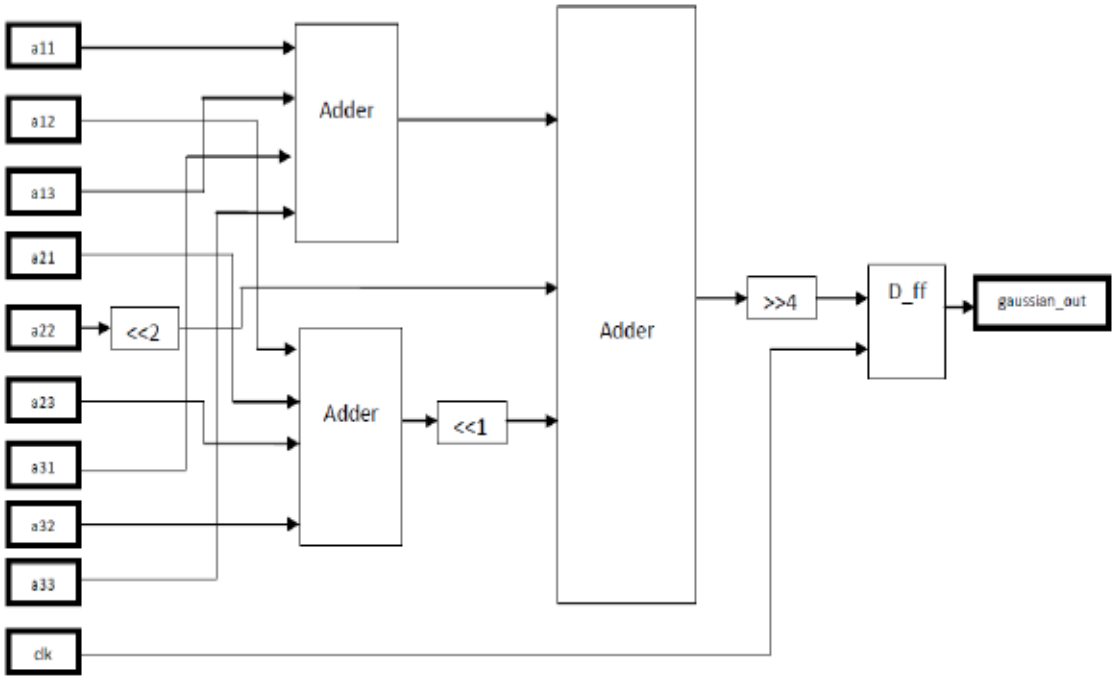

Figure 4. Hardware Structure for Gaussian Filter

The Gaussian mask of 3x3 matrix is convolved with 3x3 overlapping matrices of an image to obtain filtered output image. The proposed architecture uses only 3 shifters as compared to six shifters in the existing architecture. The hardware structure used to read 3x3 overlapping matrix is given in Fig. 5.

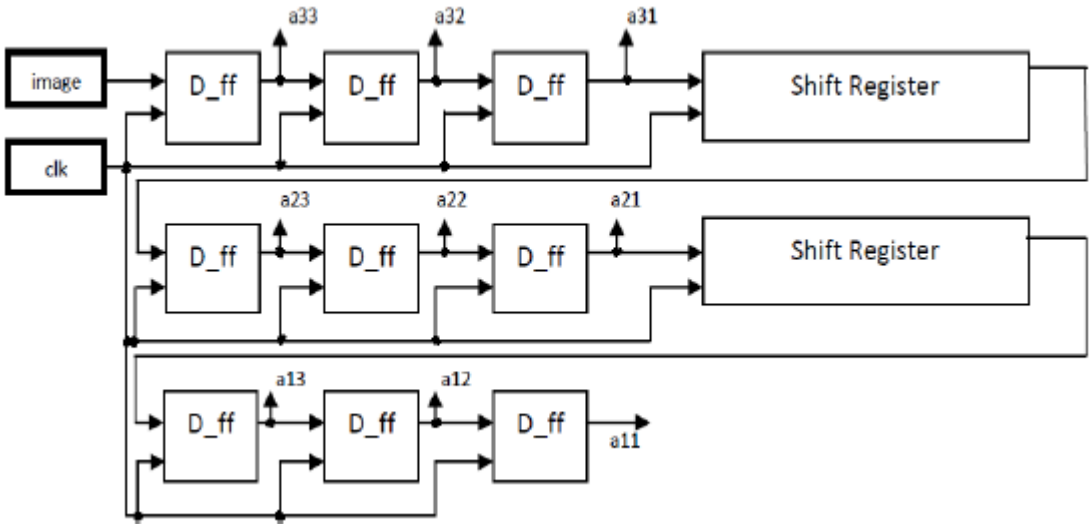

Figure. 5. Hardware Structure for 3x3 Overlapping Matrix

3.3. Discrete Wavelet Transform

The one level DWT is used to compress image to reduce the memory size and decrease computation time. The low pass and high pass FIR filters [18] are designed by using only shift and add operations required for optimization with respect to area and speed are given in equations (5) and (6).

$$y_{2i+1} = -0.5(x_{2i} + x_{2+2i}) + x_{2i+1} \quad (5)$$

$$y_{2i} = 0.25(y_{2i+1} + y_{2i+3}) + x_{2i} \quad (6)$$

Where x is the input signal value and y is the output transformed signal values. The odd output samples are calculated from even input and even outputs are calculated from updated odd output samples along with even input samples.

Equations (5) and (6) shows the lifting step for 5/3 LeGall integer wavelet transform [19]. The rational coefficients allow the transforms to be invertible with finite precision analysis presented by Andra et al., [6]. The equations (5) and (6) are simplified to derive low pass and high pass filter coefficients. The 2D-DWT is designed by considering 1DDWT, memory and controller units.

3.3.1. 1D-DWT

The low pass filter of CDF-5/3 [18] used to implement 1D-DWT architecture is given in equation (7) and (8).

$$y_{LPF}(n) = -\frac{1}{8}x[n] + \frac{1}{4}x[n-1] + \frac{3}{4}x[n-2] + \frac{1}{4}x[n-3] - \frac{1}{8}x[n-4] \quad (7)$$

$$y_{LPF}(n) = \frac{1}{8}\{-x[n] + 2x[n-1] + 6x[n-2] + 2x[n-3] - x[n-4]\}$$

$$y_{LPF}(n) = \frac{1}{8}\{-x[n] + 2x[n-1] + (4+2)x[n-2] + 2x[n-3] - x[n-4]\}$$

$$y_{LPF}(n) = \frac{1}{2^3}\{-x[n] + 2^1x[n-1] + (2^2 + 2^1)x[n-2] + 2^1x[n-3] - x[n-4]\}$$

$$y_{LPF}(n) = (\gg 3)\{-x[n] + (\ll 1)x[n-1] + ((\ll 2) + (\ll 1))x[n-2] + (\ll 1)x[n-3] - x[n-4]\} \quad (8)$$

Where (<<) and (>>) indicates Left shift and Right shift respectively.

The adders, shifters and D-FF's are used to implement 1D-DWT to generate L-Band as shown in Fig 6. The D-FF's are used to implement delay and down-sampling. The shifters are used to replace multiplications and divisions.

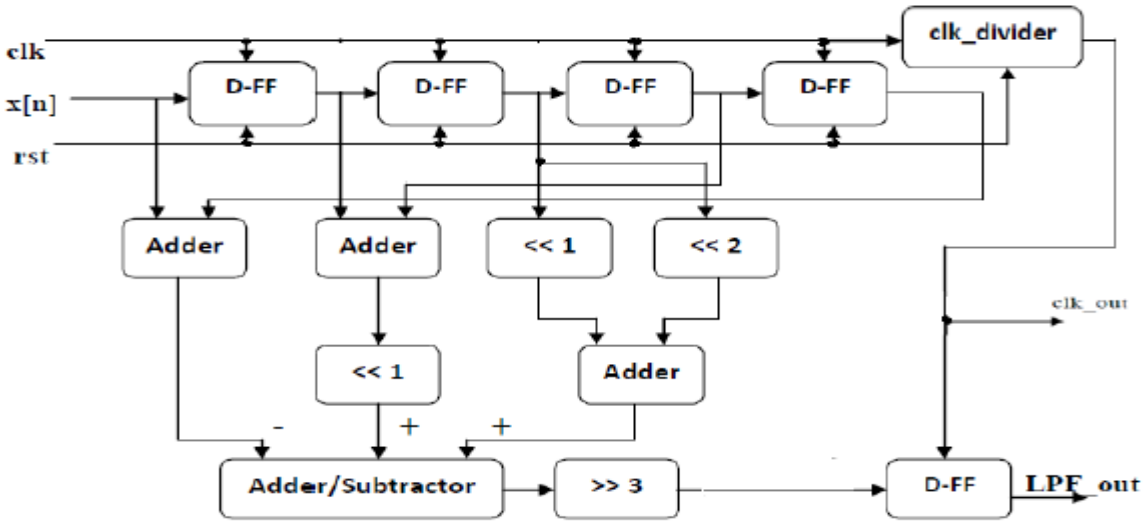

Figure 6. Hardware Structure for L-band of 1D-DWT

3.3.2. 2D-DWT

The 1D-DWT architecture is used to get 2D-DWT architecture by using memory and controller units as shown in Fig. 7 which is known as flipping architecture [5]. The LPF coefficients from 1D-DWT are stored in the memory unit block of 2D-DWT architecture. The stored L-band coefficients in memory unit are further processed by using same 1D-DWT unit with the help of MUX and DEMUX.

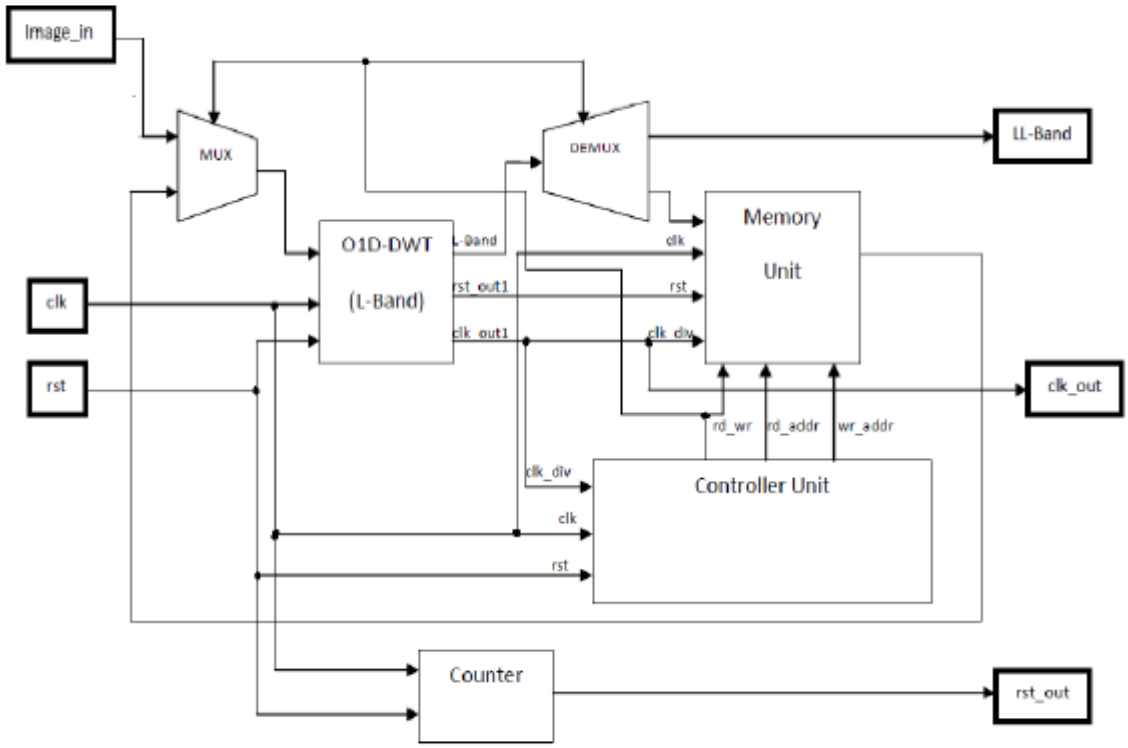

Figure 7. Hardware Structure for 2D-DWT (LL Band only)

3.3.2.1. Memory Unit

The L-Band coefficients generated by1D-DWT are stored in memory units as shown in Fig. 8 which is used to obtain transposition of input image. The clock signals clk1 and clk2 are used to read and write the coefficients from both memory units simultaneously. The clk_out of 1DDWT block is used as input to clk2 signal for memory unit. The control signals like rd_addr, wr_addr, rd_wr, clk and clk_div are selected by Proposed Control Unit. When rd_wr is logic-0 then the memory is in writing mode and it uses the wr_addr address. As a result input data is stored into the memory at location specified by wr_addr. Similarly when rd_wr is logic-1 then the memory is in reading mode and it uses the rd_addr address. As a result stored data is read from the memory at location specified by rd_addr. The memory unit is used to convert 1DDWT into 2D-DWT with the help of control unit.

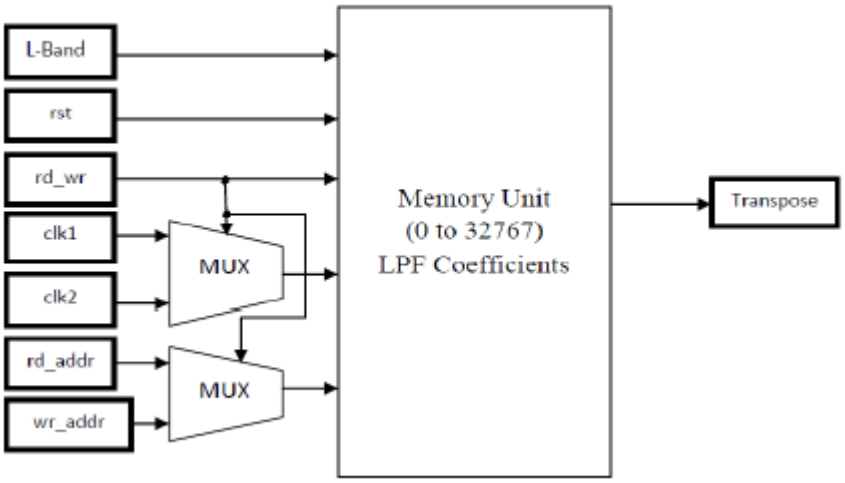

Figure 8: Memory Unit

3.3.2.2. Controller Unit

The controller unit is used to generate the address used by the memory to perform transpose of L-Band coefficients. When rst is logic-1 then it produces write address (wr_addr) at the clock rate defined by clk2 and make rd_wr to logic-0. When all L-Band coefficients are stored into the memory the signal rd_wr becomes logic-1and produces read address (rd_addr) at the clock rate define by clk1 in such way that, transpose address of input coefficients are available.

3.4. Adaptive Threshold

The adaptive threshold block is used to calculate the threshold used to detect object/image efficiently. If the input pixel value is greater than the threshold value then the respective values are passed to the output else the output will be zero. The pixel value difference (S) between background and actual image is given in equation (9) and (10).

$$S = \frac{[A_1 - B_1]^2 + [A_2 - B_2]^2 + \cdots + [A_N - B_N]^2}{8N} \quad (9)$$

$$S = \sum_{i=1}^{N} \frac{[A_i - B_i]^2}{8N} \quad (10)$$

Where, N is the dimension of input image (N=256x256).

A1, A2…AN are the actual image pixel intensity values after filtering.

B1, B2...BN are the background image pixel intensity values after filtering.

The Adaptive Threshold (ATi) is calculated using S and LL coefficient values of background image (LL2) are given in equation (11) and (12).

$$AT_i = S + (LL\ Coefficients\ of\ Background\ Image)_i \quad (11)$$

$$AT_i = S + (LL2)_i \quad (12)$$

Where, i=1 to (128x128).

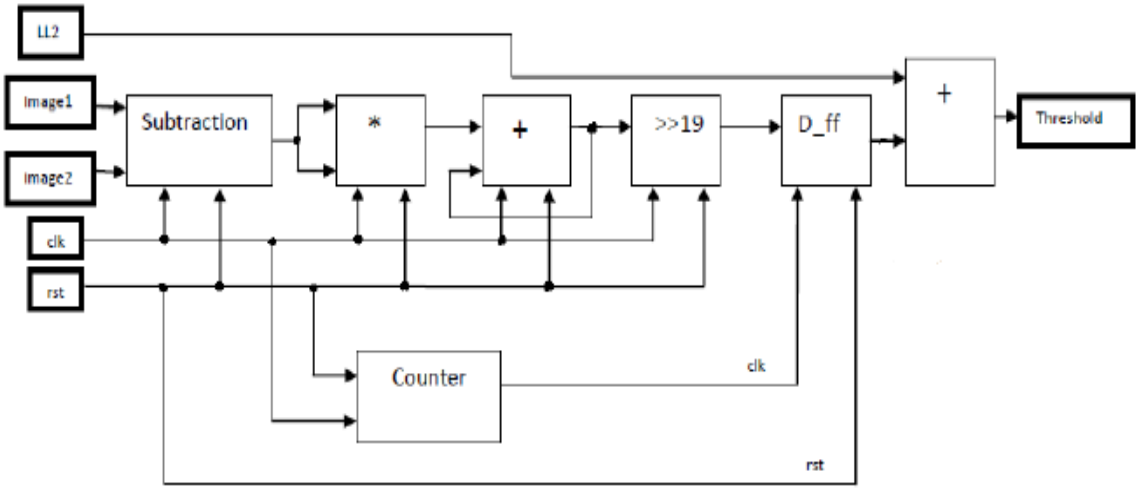

Figure 9. Hardware Structure for Adaptive Threshold

The hardware architecture is used to build adaptive threshold block is given in Fig. 9 where the image size is N=256x256. The presence of feedback in addition block in the architecture, the output value changes at every clock pulse, hence D-FF and counter is used to obtain S value for an image at 65536 clock pulse. The right shift by 19 (i.e. >>19) is used to implement 8x256x256. The LL coefficients of background image/database face images are added with the value of S to compute final threshold values of each LL coefficients. The threshold value is adaptive since each LL coefficient has different threshold values.

3.5. Modified Background Subtraction

In Object Detection, the background information is removed to obtain foreground information. In Background subtraction [19], the LL band coefficients of two images obtained from DWT block are subtracted and compared with proposed Adaptive Threshold to obtain segmented foreground

image. The background image LL2 coefficients are subtracted and considered absolute values as given in equation (13) and (14).

$$LL_j = mod\left((LL2)_j - (LL1)_j\right) \tag{13}$$

Where, j=1 to (128x128).

LL2= LL band coefficients of Background Image/Database.

LL1= LL band coefficients of Actual Image/Test.

$$Background\ Subtraction = \begin{cases} LL_j & ; \quad if\ LL_j \geq AT_i \\ 0 & ; \quad Otherwise \end{cases} \tag{14}$$

The hardware architecture of Modified Background Subtraction block is shown in Fig. 10. The two images (i.e. background and foreground) are fed to max. and min. calculations block to find minimum and maximum values of two LL band coefficients. Then use subtraction block to get subtracted values of both LL coefficient values. Now this value is compared with adaptive threshold value. If the adaptive threshold value is less than subtracted LL coefficient value then send the subtracted value (object) to the output else send zero to the output.

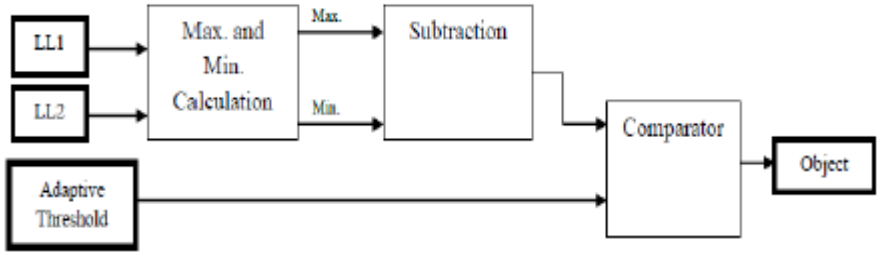

Figure 10. Hardware Architecture of Background Subtraction

3.6. Matching Unit

The similarities between test and database face images are computed and the block diagram is shown in Fig 11. The Background Subtraction block subtract two images and as a result similar portions of two images are cancelled at the output. But sometime due to large amount of light intensity variations similar portions of both images produce some small pixel intensity value after background subtraction. To eliminate this problem, a small value (say10) is fixed as tolerance threshold. If input to this block is in between 0 to 10 then the counter will be incremented by amount of oneelse the counter value stays on the previous value. Now this counter value is compared with the database global threshold value. If the counter value is greater than global threshold value, then person is matched else not matched. Pseudo code for Matching Unit is given below.

```
initilize counter value = 0;
if(rising edge clock)
    if(input ≤ 10)
        increment counter value by 1.
    else
        stay on the previous counter value.
    end if;
    if(counter value ≥ global threshold value)
        the person is matched.
    else
        the person is not matched.
    end if;
end if;
```

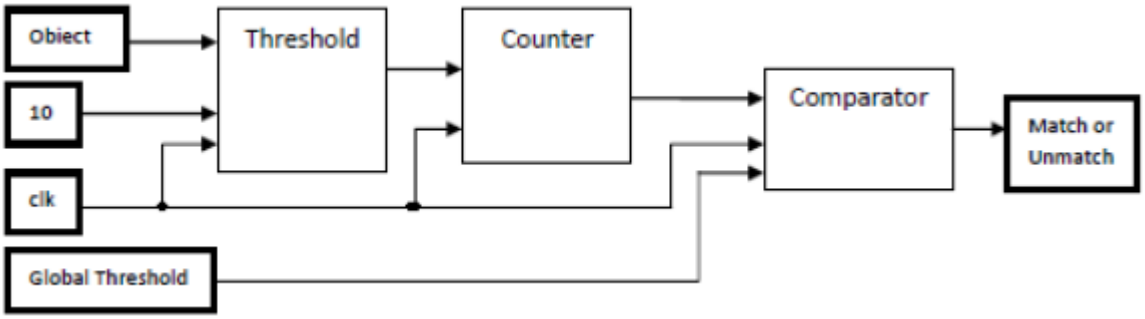

Figure 11. Hardware Architecture of Matching Unit

4. PERFORMANCE ANALYSIS OF PROPOSED OBJECT DETECTION ARCHITECTURE

In this section, the performance parameters are evaluated using PSNR, number of slices, number of slice flip flops, number of 4 input LUT's and DSP48E's. The performance parameters of proposed method are compared with existing methods of different block levels.

4.1. Performance Parameters for Gaussian Filter

4.1.1. PSNR Comparison of Gaussian Filter

The Noise in image is reduced using Gaussian filter. For experimentation, the different noise levels from 0.01 db to 0.20 are introduced into images to generate noisy images. The parameter peak signal to noise ratio (PSNR) [20] is used to measure the quality of images and is given in equation (15).

$$PSNR = 10\log_{10}\frac{255^2}{MSE} \quad (15)$$

Where, MSE = Mean Square Error=$\frac{1}{MN}\sum_{i=0}^{M-1}\sum_{j=0}^{N-1}[P_I(i,j) - P_O(i,j)]^2$

$P_I(i,j)$ is input image pixel values.

$P_O(i,j)$ is input image pixel values.

MN is the image dimensions=256x256.

The noisy image with 0.01 noise level is considered and passed through Gaussian filter to eliminate noise in image. The noisy and derived images are as shown in figure 12. It is observed that the output image of Gaussian filter has less noise compare to input image.

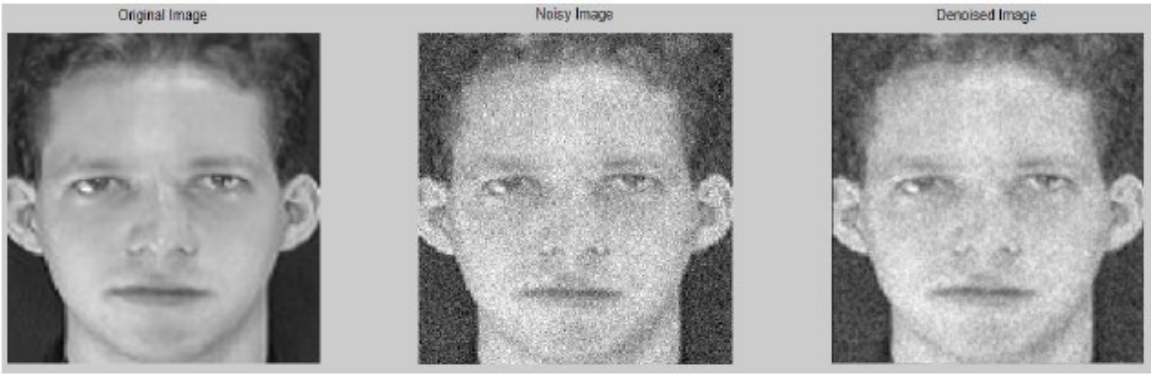

Figure 12. Input and output images of Gaussian filter

The values of PSNR with different noise levels are given in table 1. The PSNR values are computed by considering original and de noised images. The PSNR values are high with less noise levels compare to low PSNR values with high noise levels.

Table 1: PSNR values for different noise levels

Noise Level	PSNR in dB
0.01	90.2750
0.05	86.7532
0.10	73.2302
0.15	64.2544
0.20	61.0270

4.1.2. Hardware Performance Parameters Comparisons

The proposed method hardware parameters such as number of slices, number of slice flip flops, number of 4 input LUT's and DSP48E'sare compared with existing Gaussian filter architecture presented by Barbole and Shah [21], Mehra and Ginne [22], Hanumantharaju and Goplakrishna [23]. It is observed from the table 2 that, the performance parameters are better in the case of proposed architecture compare to existing architectures.The proposed architecture uses only DFF, shifters and adders, hence hardware requirement is less compared existing Gaussian filter architectures.

Table 2: Hardware Comparison of Proposed and Existing Gaussian Filter

Parameters	Barbole and Shah [21]	Mehra and Ginne [22]	Hanumantharaju and Gapalakrishna [23]	Proposed Method
Number of Slices	521	220	725	116
Number of Slice Flip Flops	225	169	1224	28
Number of 4 input LUTs	459	480	825	208
Number of DSP48Es	17	0	0	0

4.2. Performance Parameters for 2D-DWT

The de noised image of size 256*256 from Gaussian filer is passed through 2D-DWT block. The LL band of size 128*128 from DWT block is considered for further processing and corresponding images are shown in figure 13.

(a) Input Image (256x256) (b) LL-Band (128x128)

Figure 13. 2D-DWT images

The hardware performance parameters of proposed 2D-DWT architecture are compared with existing architectures presented by Sowmya et al., [24], Rajashekar and Srikanth [25] and AnandDarji et al., [26]. The performance parameters are better in the case of proposed 2D-DWT architecture compared to existing 2D-DWT architectures and corresponding values are given in table 3. In proposed 2D-DWT architecture, only add and shift operations are used hence results are improved

Table 3: Hardware Comparison of Proposed and Existing 2D-DWT

Parameters	Sowmya et al., [24]	Rajashekar and Srikanth[25]	AnandDarji et al., [26]	Proposed Method
Number of Slice Registers	832	2649	633	301
Number of Fully used FF pairs	643	3343	----	229
Number of MULT18x18SIOs	2	3	6	0

4.3. Performance Parameters of Proposed Object Detection

The proposed object detection architecture to detect an object from an image effectively as adaptive threshold concept is used. The object detected using proposed architecture is compared with existing architectures presented by Lee and Park [27] and Chu et al., [28] are shown in the figure 14. It is observed that, the minute part in the object is also detected effectively in the proposed architecture compare to existing architectures.

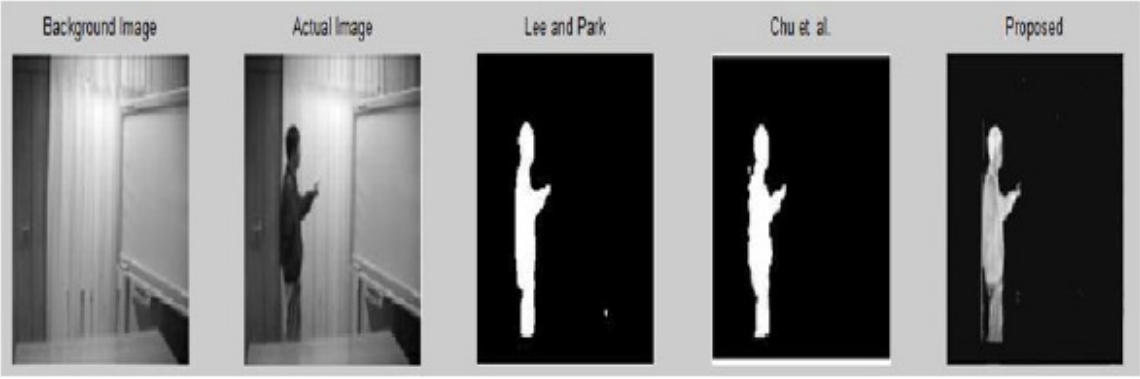

Figure 14. Output Image Comparison for existing and proposed Moving Object Detection

The hardware requirements of proposed and existing object detection architecture are given in Table 4. The architecture presented by Chodwary et al., [29] requires 1180 slice registers and 2118 fully used flip-flop pairs. This architecture is implemented by using Microblaze processor and the scripting is done by using C-language. The architecture presented by Mahamuni and Patil [30] requires 961 slice registers and 339 fully used flip-flop pairs. This architecture is implemented by using inbuilt system generator HDL blocksets. Similarly the architecture presented by SusruthaBabu et al., [31] uses 409 slice registers and 269 fully used flip-flop pairs. The proposed object detection architecture requires only 365 slice registers and 98 fully used flip-flop pairs. Hence the proposed architecture is better compared to existing architecture.

Table 4: Hardware Comparison of Proposed and Existing Object Detection Architectures

Logic Utilization	Chodwary et al., [29]	Mahamuni and Patil [30]	SusruthaBabu et al., [31]	Proposed
Number of Slice Registers	1180	961	409	365
Number of Fully Used FF-Pairs	2118	339	269	98

The performance parameters are better in the proposed object detection architecture for the following reasons

(i) The adaptive threshold values are computed based on different kinds of images.
(ii) The 2D-DWT architecture is implemented using only adders, shifters and D-FF's.

5. PERFORMANCE ANALYSIS OF PROPOSED FACE DETECTION ARCHITECTURE

In this section, the definition of performance parameters viz., Total success Rate (TSR), False Rates (FRR), False Acceptance Rates (FAR) and Equal Error Rate (ERR) are discussed to evaluate proposed architecture using face database. The performance parameters are computed by varying threshold values and the TSR values are compared with existing methods. The hardware parameters such as number of slice registers and maximum clock frequency (MHz) of proposed face detection architecture is compared with existing architecture.

5.1. Definition of Performance Parameters

(i) False Rejection Rate (FRR) is the measure of the number of authorized persons rejected. It is computed using an equation (16).

$$FRR = \frac{\text{No of authorized persons rejected X100}}{\text{Total No of persons in database}} \tag{16}$$

(ii) False Acceptance Rate (FAR) is the measure of the number of unauthorized persons accepted and is computed using equation (17).

$$\%FAR = \frac{\text{No. of unauthorized persons acceptedX100}}{\text{Total No.of persons outside the database}} \tag{17}$$

(iii) Total Success Rate (TSR) is the numbers of authorized persons successfully matched in the database and is computed using the equation (18).

$$\%TSR = \frac{\text{No.of authorized persons correctly matchedX100}}{\text{Total No.of persons in the database}} \tag{18}$$

(iv) Equal Error Rate (EER) is the point of intersection of FRR and FAR values at particular threshold value. The EER is the trade-off between FRR and FAR. The value of EER must be low for better performance of an algorithm.

$$EER = FAR = FRR \tag{19}$$

5.2. Performance Analysis using Simulation Results

5.2.1. Analysis using FAR, FRR, EER and TSR

The performance parameters are computed by running computer simulation using MATLAB R2012a(7.14.0.739) version. The values of FRR, FAR and TSR are computed by comparing features of test images with features of image in database using a counter for varying threshold shown in Table 5.

Table 5: Variations of FRR, FAR and TSR

Threshold	% TSR	% FRR	% FAR
1	0	100	0
1.1	0	100	0
1.2	0	100	0
1.3	10	80	0
1.4	20	60	0
1.5	40	40	0
1.6	60	20	0
1.7	68	10	0
1.8	75	0	8
1.9	75	0	13
2.0	89	0	25
2.1	93	0	45
2.2	99	0	60
2.3	99	0	100

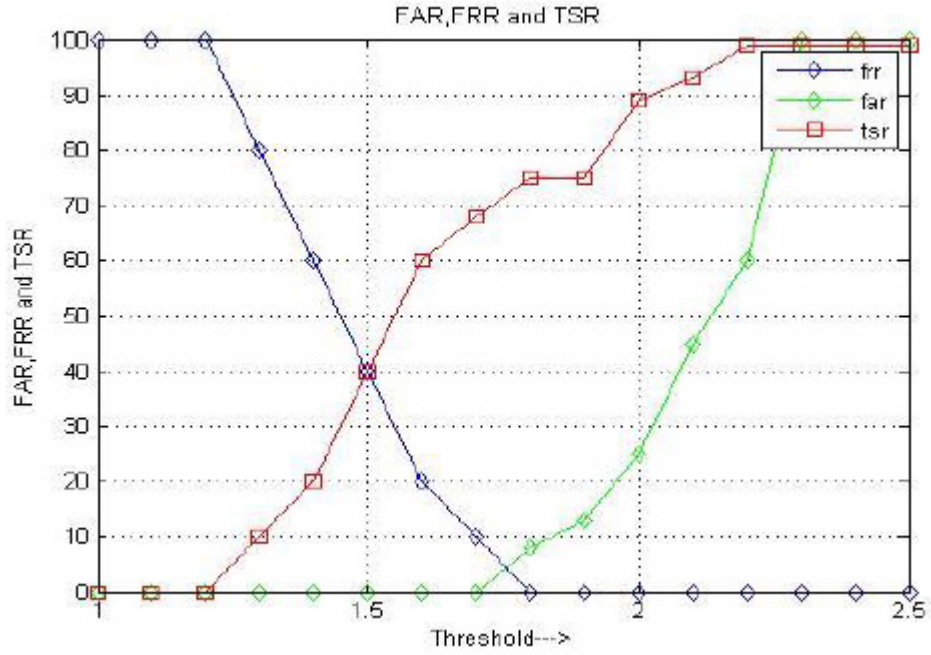

Figure15: Plots of FAR, FRR and TSR against Threshold

5.2.2. Performance Comparisons of Proposed Techniques and Existing Techniques

The percentage values of TSR of proposed method is compared with existing methods presented by Ben Niu et al., [11], Sardar and Babu [32], Junjie Yan et al., [33], Thiago H.H. Zavaschi et al., [34], Manchula and Arumugam [35] and Wang and Yin [36]. It is observed that the value of TSR is high in the case of proposed method compared to existing methods as shown in table 6. The

performance parameters are improved since; the proposed method uses adaptive threshold and background subtraction techniques.

Table 6. Comparison of percentage TSR values of proposed method with existing methods

Authors	Techniques	% TSR
Ben Niu et al., [11]	Two Dimensional Laplacian Face	97.8
Sardar and Babu [32]	DWT, PCA and Neural Networks	93
Junjie Yan et al., [33]	Hierarchical Part	96.5
Thiago H.H. Zavaschi et al., [34]	Gabor and Local Binary Pattern	96.2
Manchula and Arumugam [35]	PCA and Eigen Vector	96
Wang and Yin [36]	Topographic Context	82.68
Proposed method	DWT, Background Subtraction and Adaptive Threshold	99

5.2.3. Performance Analysis using Hardware Comparison results

The logic utilizations comparison of proposed method with existing method is given in table 7. The existing technique presented by Sardar and Babu [32] uses 39432 slice registers and the maximum operating frequency is 80MHz. i.e., this architecture uses a large amount of hardware and low operating frequency because the architecture is implemented on microblaze embedded processor. The proposed architecture uses only 861 slice register and maximum operating frequency is 118.60 MHz i.e., low amount of hardware and high operating frequency because the architecture uses only adders, shifters and D-FF's for implementation and also the adaptive threshold concept.

Table 7: Hardware Comparison of Proposed and Existing Face Detection Techniques

Logic Utilizations	Sardar and Babu [32]	Proposed method
Number of Slice Registers	39432	861
Maximum Clock Frequency (MHz)	80	118.60

6. CONCLUSION

The object and face detection is essential to detect a person in real time applications. In this paper, we propose FPGA implementation of object and face detection using adaptive threshold. Input image and reference images are passed through Gaussian filters to remove noise and DWT is applied to generate LL band coefficients. The modified background subtraction is used along with adaptive threshold on two LL bands to detect an object. The final object is obtained after passing output of modified background subtraction through Gaussian filter. The face detection can also be performed with the same architecture with and additional matching unit and global threshold unit. In face detection architecture the reference image and input image of object detection architectures are replaced by face database and test face image respectively. The performance parameters are better in the proposed architecture compared to existing architectures in-terms of software and hardware results.

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