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I, Purva Bhatnagar , hereby submit this original work as part of the requirements for the degree of Master of Science in Electrical Engineering.

It is entitled:

A microcontroller-based Electrochemical Impedance Spectroscopy Platform for Health Monitoring Systems

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UNIVERSITY OF Cincinnati

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A microcontroller-based Electrochemical Impedance Spectroscopy Platform for Health Monitoring Devices

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Abstract

Electrochemical Impedance Spectroscopy (EIS) is an experimental procedure and important technique to evaluate the underlying characteristics of biosensors, body fluids, electrochemical fuel cells, and electronic circuits. Existing EIS systems are expensive, bulky, and difficult to integrate with other systems such as wearable medical devices. This thesis presents a prototype of a low-cost, portable, microcontroller-based EIS platform for integration with health monitoring systems. A major challenge is to eliminate the use of sophisticated and expensive hardware and provide an alternative low-cost solution that can maintain the ability of measuring over an acceptable range of frequencies and impedance values.

The prototype of the portable EIS system is developed using an off-the-shelf, fast and, powerful digital signal controller that serves as the main control unit of the system. The in-built modules like Pulse Width Modulation, Analog-to-Digital Converter, Direct Memory Access and Universal Asynchronous Receiver Transmitter along with low pass-filters are used for signal generation, sampling as well as signal processing. The system also employs a low-cost and effective analog interface module for conditioning digital signals generated from the controller, which are as analog inputs in electrical cell impedance models as well as commercial electrochemical cell in the form of interdigitated electrodes with Phosphate Buffer Saline(PBS) and vice versa. With an operating sampling frequency in the range of 2 Hz – 2 KHz, the overall cost of the system is estimated to be less than $100.

The overall efficiency of the system is fair for complex impedance amplitude and phase computation with error in computation calculated to be less than 10%. These results demonstrate the feasibility of a portable EIS system for electrochemical as well as bioelectrical impedance analysis.

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Thank you Mom, Dad, Garvit and Pulkit for always believing in me and my abilities. Without your constant encouragement and motivation, I could not have done any of this. I feel blessed to have had an opportunity to study at the University of Cincinnati. The work and professional lessons that I have learnt here would guide me throughout my life.

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List of Abbreviations

EIS	**E**lectrochemical **I**mpedance **S**pectroscopy
DSC	**D**igital **S**ignal **C**ontroller
BIA	**B**io-electrical **I**mpedance **A**nalysis
ADC	**A**nalog-to-**D**igital **C**onverter
DAC	**D**igital-to-**A**nalog **C**onverter
PLL	**P**hase **L**ocked **L**oop
PWM	**P**ulse **W**idth **M**odulation
LPF	**L**ow **P**ass **F**ilter
AAF	**A**nti-**A**liasing **F**ilter
DMA	**D**irect **M**emory **A**ccess
IDE	**I**nter**D**igitated **E**lectrodes
IVT	**I**nterrupt **V**ector **T**able
UART	**U**niversal **A**synchronous **R**eceiver **T**ransmitter
ICD	**I**n **C**ircuit **D**ebugger
FFT	**F**ast **F**ourier **T**ransform

1. Introduction

1.1 Electrochemical Impedance Spectroscopy (EIS)

EIS is an excellent technique that has been used over the years to understand electrochemical reactions occurring in a cell. The technique is also used widely to explore the dielectric and transport properties of porous electrodes and also to investigate passive surfaces. It is known to be a powerful technique as it is a linear system and thus easy to interpret using Linear Systems Theory. Another reason that adds to the importance of EIS is that if the technique is performed over a broad frequency range, only one experimental procedure can isolate all the information concerning the influence of the governing physical and chemical phenomena at a given applied potential. It holds the potential to isolate various processes such as conduction, charge transfer, mass transfer etc. with remarkably high experimental efficiency makes it an elegant technique for electrochemical systems. The validity of the EIS data is readily determined using techniques that are independent of the physical processes involved.

The fundamental approach of all impedance methods is to apply a small excitation signal to the system under investigation and measure the response signal, i.e., current or voltage. The system under investigation is usually a three-electrode electrochemical cell containing a solution that allows the measurement system to establish electrical connection with the surface of electrode. EIS is analyzed by determining the amplitude and phase of the impedance response obtained from the reactions that occur in the electrochemical cell on application of the small excitation signal.

1.2 Applications of EIS

Over the years, EIS has found widespread applications in the field of characterization of materials. Well known applications of EIS include simulation of coatings, fuel cell, batteries and characterization of corrosion phenomena which include corrosion inhibition, evaluation of corrosion rates and corrosion protection by polymer coatings. It has also been used extensively as a tool for investigating mechanisms such as electron deposition, electron dissolution, and passivity and corrosion studies. Over the years, the methods of performing EIS have evolved and researchers have explored its usage in wide range of systems and processes, ranging from conduction in solid states, ionic and electronic conduction in polymers and important phenomenon of passivity.

Interestingly EIS finds applications in the medical field where the technique is applied to the body surface and is often referred to as bioelectrical impedance analysis (BIA). BIA is used to measure extracellular, intracellular, and total body water, as well as to monitor the changes in the amount of free fat mass in the body [25]. It has also been used for characterizing biological materials, which include lipid bilayers and many membrane proteins [7]. The most recent and perhaps most attractive medical application of EIS is its use in the monitoring and detection of biomarkers in biosensors as a function of frequency [2]. The technique reveals the frequency response of the system over a wide range of frequencies and therefore evaluates the impedance of the system. EIS finds wide range of applications in health monitoring systems utilizing sensors for specific analyte detection. For diagnostic purposes, it is necessary to characterize changes at a surface under specific parameters while, for application purposes, it is essential to tailor system parameters in order to obtain desirable effect on the surface. EIS is a tool that bridges both purposes of diagnosis and characterization.

1.3 Point of Care System Device Motivation

While EIS is widely used in health monitoring systems for detection of specific analytes, the full potential of EIS is yet to be realized [5], partly because it is regarded as a specialty technique requiring expensive equipment. Furthermore, the large size of existing EIS equipment makes it difficult to integrate such techniques into small form factor systems that are hand-held, wearable and intended for use in point-of-care testing. Thus, miniaturized and low cost EIS modules are needed in order to render effective point-of-care testing of biomarkers from electrochemical sensors. A functional block diagram of the proposed microcontroller based system device is shown in Figure 1.1.

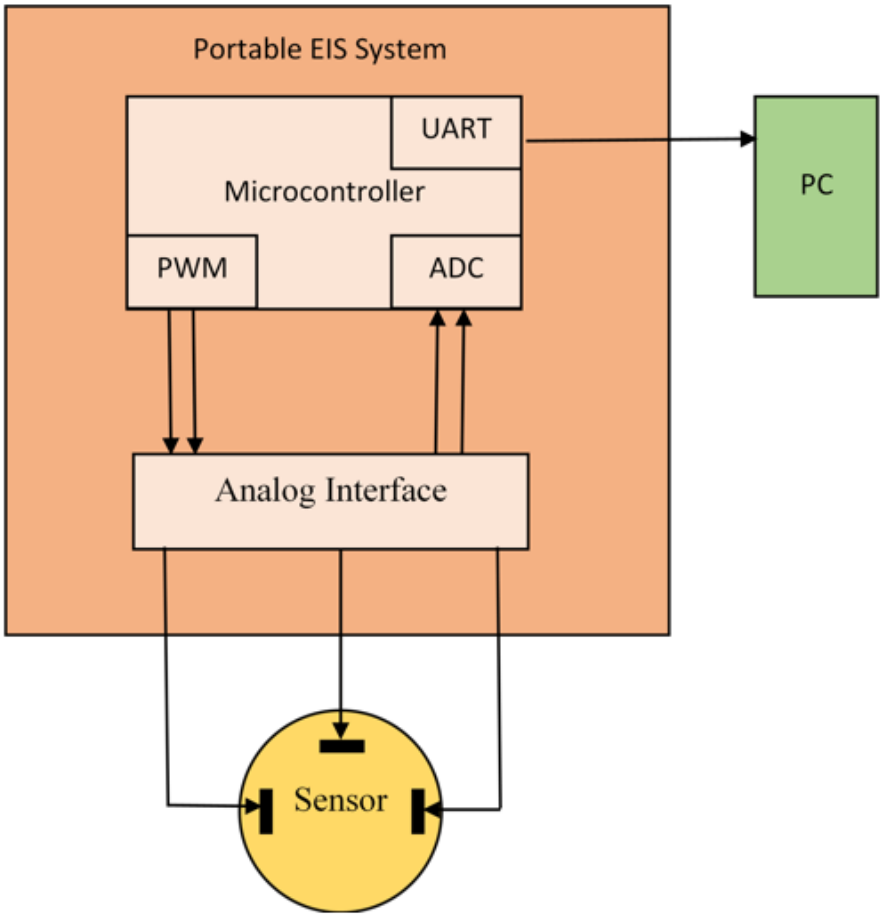


Figure 1.1 Block diagram of microcontroller based portable EIS system

These portable devices must have small valuation time for results along with being compact and portable enough to be used outside of a laboratory bench setting. Additionally, the devices should also be intuitive and easy to use for the professionals, technicians, researchers or students working on the experiments.

1.4 Research Objectives

The objective of this research is the development of a microcontroller based Point-of-Care Electrochemical Impedance Spectroscopy platform for health monitoring devices. The main aim of the proposed system is make it compact and minimize the use of external hardware circuitry. The device should be able to generate a small sinusoidal wave excitation signal over a variable frequency range up to 200 kHz and apply that signal to an electrochemical cell where electrical response of the material under test can also be measured. The device is aimed to be able to calculate the magnitude and phase of the impedance response collected from the electrochemical cell. Along with this, the device includes an analog interface circuitry with potentiostat for interfacing the device with the electrochemical cell and filters for signal conditioning of the stimulus and responses procured by the electrochemical cell. The device is also proposed to include a wired connection to a personal display device that is proposed to display the parameters to indicate the results. Design methods are proposed to be followed to the maximum capacity and error minimization due to external interferences is also proposed. In order to keep the cost of the device at the minimum, the device is proposed to be constructed using commercially available and economic embedded systems components including microcontrollers that provide low cost custom programmability.

1.5 Thesis Outline

In this thesis, we present a compact microcontroller-based EIS system that allows measurement of impedance at frequencies up to 200 kHz. This frequency range is an acceptable range to extract information about body fluids and analytes.

Chapter 1 gives a brief introduction to the EIS technique and the application of the technique to the field of medical sciences. It also discusses in brief the motivation for a point-of-care platform and points out the main goals of the research work carried out.

Chapter 2 gives a brief history of the EIS process and its development through the last two or three decades. It also discusses the various applications that have benefitted from the technique of EIS and its applications in the field of medical devices.

Chapter 3 describes in detail the design of the proposed system that generates signal for stimulus, calculates the magnitude and phase of impedance of a cell using software based control over the microcontroller and peripherals thus reducing the system size. It also discusses the integration of the hardware and describes its functioning.

Chapter 4 discusses the experimental setup used to perform the experiments and the results obtained on the portable platform.

Chapter 5 summarizes the research, methods and integration work described in the thesis and discusses the opportunities for future work.

2. Literature Review

2.1 EIS History

The foundations of EIS began as early as 1880 through the extraordinary work of Oliver Heaviside who by his application of Laplace transforms to the transient response of electrical circuits became the father of impedance spectroscopy [26]. He coined the terms of inductance, capacitance and impedance and introduced these concepts to the treatment of electrical circuits. Nernst, Finkelstein and Warburg applied this technique using reactive bridges and dielectrics with Warburg becoming the first to extend the concept of impedance to electrochemical systems, when he derived the impedance function for diffusion process that still bears his name [27]. In the 1920s impedance was applied to biological systems, including the resistance and capacitance of cells of vegetables and the dielectric response of blood suspensions. The technique was also applied to muscle fibers, skin tissues and other biological membranes and thus introducing bioelectrical impedance analysis [8].

By 1970s, there had been significant inventions in the field of electrical engineering with potentiostats and frequency response analyzers becoming readily available [5]. EIS was then applied to corrosion mechanisms with the help of potentiostats and remarkable success with characterization of materials was achieved. These inventions have led to a wide range of applications, systems and processes that can use EIS for their characterizations. In the recent past, EIS has also been applied to studies of semiconductor electrodes [5], medical imaging [16], DNA hybridization [28] and many more fields in the medical industry. During the past few years,

impedance measurements have become increasingly popular as a label-free detection tool for many different types of biosensors [29].

2.2. Review of EIS and its process

2.2.1 Process of EIS

A basic EIS technique consists of triggering an electrochemical cell with AC potential, and then measuring the current flowing across the cell. The impedance of the cell is computed as Z = V/I, where V is the voltage and I is the current flowing through the cell. Since, impedance is a complex value, it can be broken down as Z= R + jX, and

$$|Z| = \sqrt{(R^2 + X^2)} \quad (1)$$

$$\theta = \tan^{-1}(\frac{X}{R}) \quad (2)$$

Impedance is used to characterize electrochemical systems in place of resistance because the use of resistor is bound to only a single passive circuit element. However, the electrochemical processes exhibit much more complex behavior that has to be represented by complex impedance that is the ability to resist the flow of electric current without the limitations of Ohm's law [17]. Impedance takes the phase difference between input voltage and output current into account and is composed of various resistors, capacitors and inductors.

Electrochemical impedance is usually evaluated using a low amplitude trigger potential. It is known that electrochemical systems are non-linear, however at small AC signals, electrochemical

signals become pseudo-linear and do not produce any harmonics at the excitation frequency as illustrated in Figure 2.1.

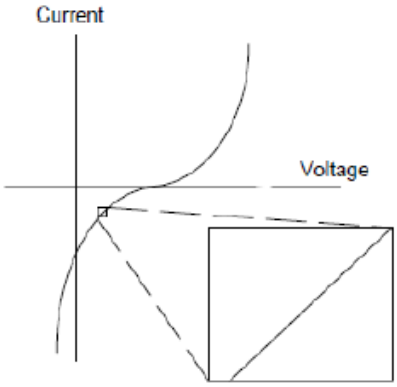


Figure 2.1 Illustration of pseudo-linearity of electrochemical cells

Linear systems show the characteristics that is a varying amplitude potential is applied then the response is also a varying amplitude signal with visible phase shift as shown in Figure 2.2.

The excitation signal can be expressed as a function of time and is given by

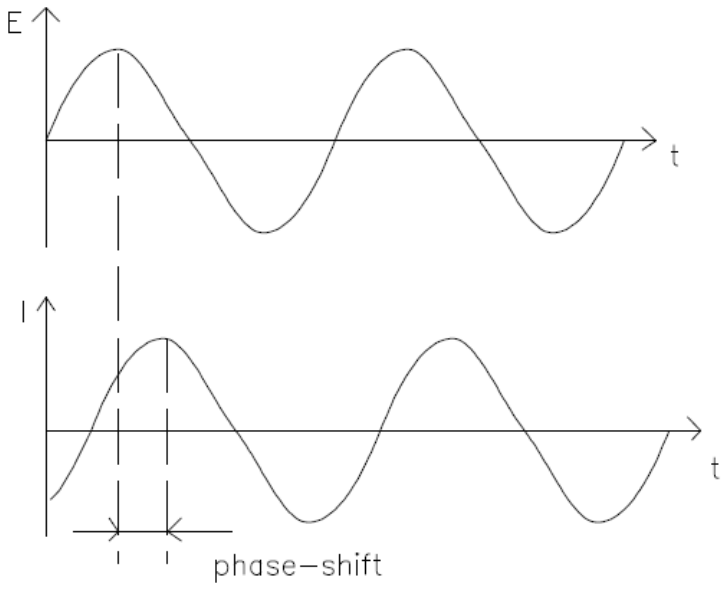


Figure 2.2 Sinusoidal Current Response in a Linear System [17]

$$E_t = E_0 \sin(\omega t) \tag{3}$$

where E0 is the amplitude of the signal, Et is the voltage and ω is the frequency. In the linear system, the response signal It, depicts a phase shift and a different amplitude, I0.

$$I_t = I_0 \sin(\omega t + \emptyset) \tag{4}$$

The impedance of the system can be calculated analogous to Ohms law as given below in the equation where the impedance is given by a magnitude Z_0, and a phase shift, Ø.

$$Z = \frac{E_t}{I_t} = \frac{E_0 \sin(\omega t)}{I_0 \sin(\omega t + \emptyset)} = Z_0 \frac{\sin(\omega t)}{\sin(\omega t + \emptyset)} \tag{5}$$

If the applied sinusoidal signal is plotted against the received sinusoidal response signal, the result is an oval called the Lissajous Figure which is shown in Figure 2.3 below and is one way of viewing data on the oscilloscope screens before the modern EIS instrumentation was available and the impedance is then given by the equation (4).

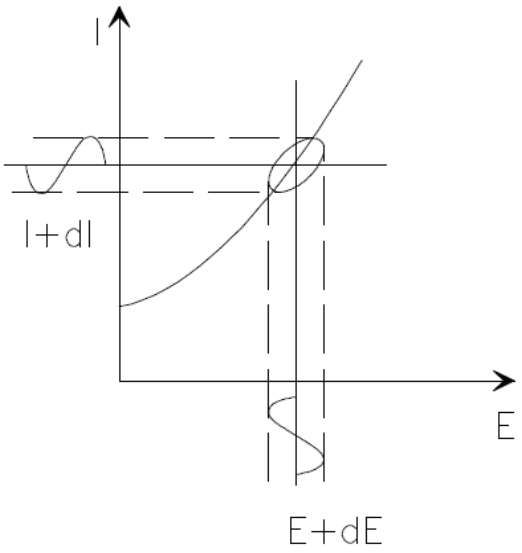


Figure 2.3 Illustration of the Lissajous Curve [17]

$$Z(\omega) = Z_0(cos\emptyset + j \sin \emptyset) \quad (6)$$

The EIS measurements can be performed in a frequency range that can extend seven orders of magnitude or more from 10 mHz to 10 MHz [2]. A wide frequency range helps to obtain a good resolution of processes between the surfaces of electrode and provides with all the information needed to collect the bulk response of the material under measurement. The impedance measurement is usually carried out by using an electrochemical cell containing a solution that allows the measurement system to establish electrical connection with the coating [23].

2.2.2 Experimental Setup for EIS

EIS experimental setup typically consists of an electrochemical cell, a potentiostat/galvanostat and a signal processing module, preferably a response analyzer, the function of which is to apply the sine wave and analyze the response of the system to determine the impedance of the system [22]. The electrochemical cell can be configured to have two, three or four electrodes. Generally the electrode containing the substance to be investigated is called the working electrode and the electrode necessary to balance the cell is identified as the counter electrode. For liquid state analysis, these electrodes are immersed in a liquid electrolyte and for solid-state systems, there are solid electrolytes or no electrolytes.

Two electrode cell:

A two-electrode cell is used when exact control of the potential across the electrochemical cell is not critical and also when the counter electrode potential is expected not to drift over the course of experiment. This configuration is mostly used to study conductivity properties of the electrolyte and for characterization of solid state systems. Two-electrode experiments measure the whole cell,

that is, measure the complete voltage dropped by the current across the whole electrochemical cell: working electrode, electrolyte and the counter electrode. According to the Figure 2.4, the impedance is measured between R and S.

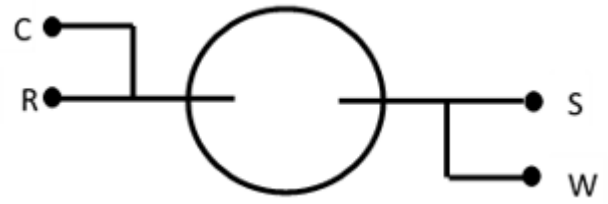


Figure 2.4 Illustration of a two electrode cell

Three electrode cell:

A three-electrode configuration for an electrochemical cell (shown in Figure 2.5) is the most common for general electrochemical applications. In this mode, a third electrode, Reference electrode is used to accurately determine the potential within the electrochemical cell. This electrode is positioned at a point close to the working electrode and all potential measurements in the electrochemical cell are measured with respect to the reference electrode. Impedance is measured between Rand S and this shows a distinct experimental advantage over the two-electrode setup as this allows potential changes of the working electrode to be measured independent of the changes that occur at the counter electrode.

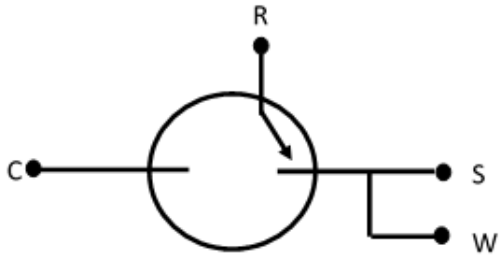


Figure 2.5 Illustration of a three-electrode cell

Four electrode cell:

This setup is uncommon in electrochemistry but it finds its application in the study of ion transport through a membrane or measurements on low impedance solids where the influence of contact and wire resistance is deemed minimal. As shown in Figure 2.6, in this configuration, there is an addition of a Working Sense electrode and the potential is measured in between R and S. This leads to the understanding that the voltage difference between these two electrodes that is working and counter is not measured. Instead, what is measured is the effect of an applied current on the solution itself or on some barrier in the solution.

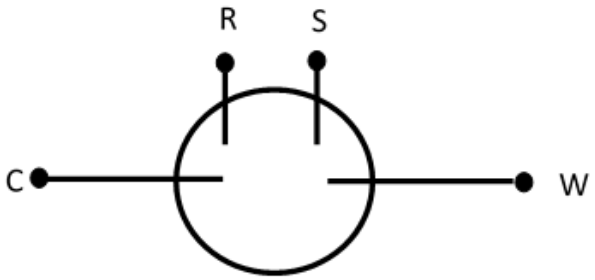


Figure 2.6 Illustration of a four-electrode cell

2.2.3 Measurement techniques

The earliest measurement techniques after the invention of potentiostat relied on the use of A.C. bridges also called Wheatstone bridges that are now rarely used. The bridge is based on a nulling technique that requires manipulation of an adjustable resistor and capacitor at each frequency to obtain an effective frequency-dependent resistance and capacitance of the cell, from which can be derived an impedance. Another technique, called Lissajous technique, [17] is also obsolete but very useful to visualize impedance, where the applied sinusoidal signal is plotted against the

sinusoidal response current and this results in an oval called the Lisaajous Figure, as shown in Figure 2.3. The technique that is most useful at high frequencies, is inexpensive and accurate is the use of phase-sensitive detection with a lock-in amplifier. This helps to determine the change in magnitude and phase of the response sinusoidal with respect to a reference signal. Other techniques that are also used for EIS are Fourier analysis techniques which are also accurate. The experiment parameters and the settings of the potentiostats in the systems can be configured to obtain different electrochemical impedance spectroscopy techniques.

Potentiostatic EIS: In this mode the experiment is performed by applying a sinusoidal voltage which is superimposed on a fixed DC potential to the sample. The resulting current is measured to evaluate impedance of the system. Potentiostatic EIS is the most popular technique and is favored by corrosion scientist and sensor developers.

Galvanostatic EIS: In this mode the experiment is performed by applying a sinusoidal current which is superimposed on a fixed DC potential to the sample. The resulting voltage is measured to construct impedance of the system. This mode is commonly used in battery and fuel cell studies.

Single Frequency EIS: In this mode the impedance is measured at a frequency versus time. The experiment is then repeated for the whole frequency band which is separated by decades of interval is called the multi frequency EIS.

2.2.4 Data Presentation

The data for EIS measurements are often represented in Nyquist and Bode plots. Bode plot refers to the representation of the impedance magnitude and phase angle as a function of frequency. A Nyquist plot depicts the imaginary impedance corresponding to the capacitive and inductive nature

of the cell versus the real impedance of the cell. The advantage of Nyquist plot is that it gives a quick overview of the data and one can make some qualitative interpretations. While plotting the data in the Nyquist format the real axis must be equal to the imaginary axis so as not to distort the shape of the curve. The shape of the curve is important in making qualitative interpretations of the data. An example of Nyquist plot of a simple electrical RC in parallel circuit is shown in Figure 2.7.

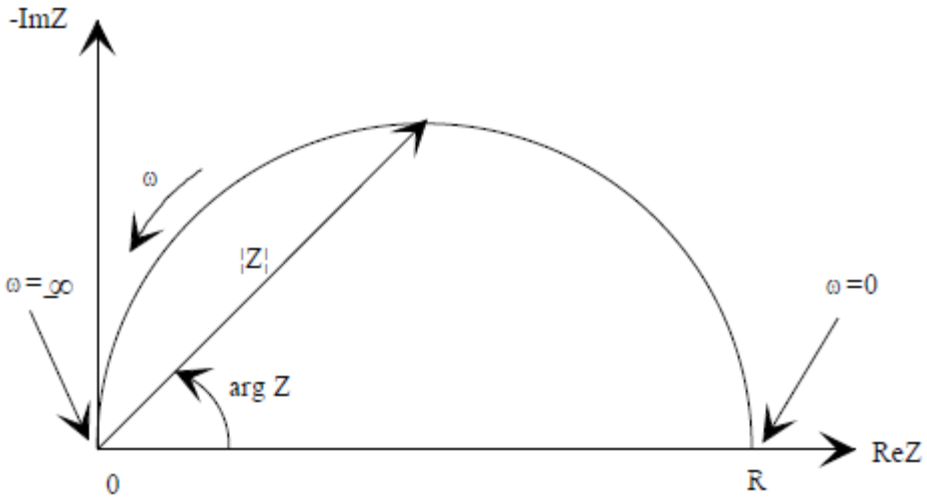


Figure 2.7 Illustration example of a Nyquist Plot with Impedance Vector [17]

The disadvantage of the Nyquist representation is that one loses the frequency dimension of the data. It can be overcome by simply labeling the frequencies on the curve but this is not a good solution. Bode plot represents the absolute value of impedance and the phase shifts as a function of frequency in two different plots as shown in Figure 2.8. Because both data formats have their own disadvantages, it is usually best to present both.

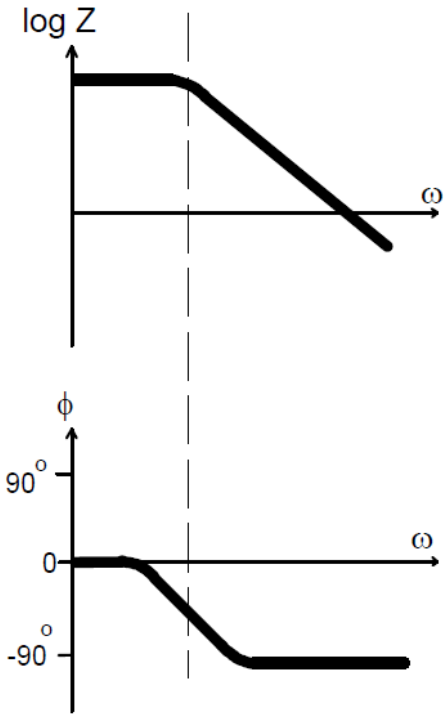


Figure 2.8 Illustration example of a Bode Plot with 1 time constant [17]

2.2.5 Data Analysis

The EIS data that is obtained after characterization of EIS is analyzed to interpret the underlying characteristics. Electrochemical cells can be modeled as a network of passive electrical circuit elements. This network is called an equivalent circuit. The EIS response of an equivalent circuit can be calculated and compared to the actual EIS response of the cell. These models are applied to data obtained from the experiments and can be used to understand the system under various conditions. Capacitors, resistors and inductors generally known as passive elements are used to model the cells. Sometimes use of distributed elements takes place with the help of elements like

constant phase element and Warburg impedance. The connections between these elements can be in series or in parallel.

The physical meaning of a few elements of equivalent circuit models are explained below.

Resistance (R):

The element R can be expressed in terms of impedance by

$$Z_R = R \tag{7}$$

The impedance of the resistor does not contain any imaginary part. The current through a resistor is always in phase with applied voltage. The resistance can be used in the models in different ways. One as Ohmic resistance, R Ω which is defined as the potential drop between the reference electrode and the working electrode. It depends on the conductivity of the electrolyte and the physical characteristics of the electrode. The other is polarization resistance which is defined as the transition resistance between the electrode and the electrolyte in an electrochemical cell.

Capacitance (C):

The circuit element C, capacitor can be expressed in terms of impedance as,

$$Z_c = \frac{1}{jwC} \tag{8}$$

Capacitors only exhibit impedance which is the imaginary part as a function of frequency. A capacitor's impedance increases directly with increase in frequency. The current in the capacitor is phase shifted -90° with respect to voltage. The capacitance is also used in different ways to describe the electrochemical phenomena. One is double layer capacitance, is created due to the

existence of an electrical double layer at the electrode/electrolyte surface. Double layer capacitance is directly proportional to types of ions, roughness of electrodes, electrode potential and layers of oxide. The other is coating capacitance, C_c which is used to measure the substrate absorbed by the coating.

Constant Phase Element (CPE):

CPE which is used to model the lack of homogeneity in electrochemical reactions. The modelling of electrochemical phenomenon with a capacitor assumes that the surface being investigated is homogenous which the case is not normally.

It is represented as

$$Z_Q = \frac{1}{Y_0(jw)^n} \tag{9}$$

where, Y_0 is the admittance of an ideal capacitor and *n* is an empirical constant ranging from 0 to 1. The two terms described above, double layer capacitance and coating capacitance are usually modelled with constant phase element.

Warburg Impedance (W):

It has been developed to model the process of diffusion at the interface. For a semi-infinite diffusion layer, the impedance is:

$$Z_W = \frac{1}{Y_0\sqrt{jw}} \tag{10}$$

where, Y_0 is the diffusion admittance. A Warburg impedance is known to have identical real and imaginary parts. Therefore, the phase angle of the element is 45°.

Inductance (L):

The impedance of which is given by:

$$Z_L = jwL \tag{11}$$

The impedance of an inductor is also a function of frequency. Inductors also exhibit an imaginary impedance as a function of frequency. The current passing in an inductor is shifted in phase by 90° with respect to the voltage. Inductance behavior in an electrochemical cell can result from adsorption of reactants on the surface or from uneven current distribution, slow response of reference electrodes etc. In rare cases, when an inductance result is obtained, it indicates error in EIS measurement.

2.2.6 Equivalent Circuit Analogs

Equivalent Circuit models represent the real world electrochemical cells in terms of resistances, impedances and capacitances [12, 23, 25]. Equivalent circuit modelling is a useful way to understand the mechanisms or processes involved in an electrochemical cell. Because a system's impedance at any particular frequency will often be dependent on more than one element of the cell, equivalent circuit modelling can help to separate out the contributions from each of the elements. This can help to understand the various things happening inside the cell in mechanistic terms. In equivalent circuit analogs, the resistors represent conductive pathways for ions and electron transfer. The capacitors and inductors represent the space charge polarization regions such as the electrochemical double layer, and adsorption/desorption processes at an electrode respectively [24].

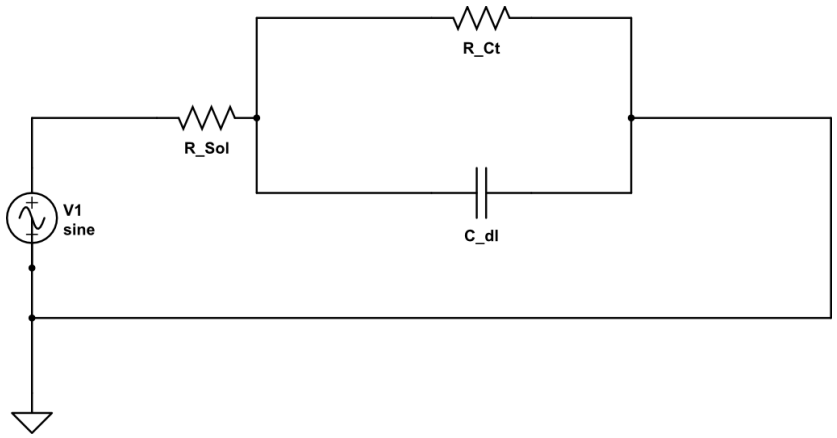


Figure 2.9 A circuit representing Randles Cell

The cell model called the Randles cell, as shown in Figure 2.9 is one of the most well-known cell models. It is composed of a solution resistance (R_{sol}), a double layer capacitor (C_{dl}) and a charge transfer (R_{ct}) (or polarization resistance). The double layer capacitance is often in parallel to the charge transfer resistance.

2.3 Previous work on applications of EIS in medical field

In the recent years, EIS has found many applications in the field of material sciences and metal studies. It is often used in the study of coatings, batteries, fuel cells, and corrosion phenomena [14]. It has also been used extensively as a tool for investigating mechanisms in electro-deposition and corrosion studies [6].It is gaining popularity in the investigation of diffusion of ions across membranes and in the study of semiconductor surfaces. With this existing popularity of and wide range of applications in material science and chemistry fields, the medical applications do not shy away from taking advantage of EIS.

The medical industry has benefitted the society with the development of biosensors that are used to monitor and detect biomarkers in the body fluids. One of the first applications of EIS in medical field was the analysis and detection of biomarkers with biosensors in body fluids as a function of frequency. However, traditional EIS methods are inefficient at low frequencies, where these materials are used as biosensor applications. In efforts to reduce times of measurement, researchers have proposed methods in which no frequency scanning is required. They used the Fast Fourier transform method on the current response obtained from the electrochemical cell and then deconvoluted the ac voltages and currents to calculate the impedance. This method was termed as Fourier Transform Electrochemical Impedance Spectroscopy (FTEIS) and sharply decreased the impedance measurements time at low frequencies thereby leading to significant developments in biomarker detections [6]. In one application the neurotransmitter serotonin was effectively captured on gold electrodes [25]. Medical researchers worked in collaboration with chemists and EIS experts and created capacitive biosensors for antibodies, antigens, proteins and heavy metal ions by modifying electrode surfaces with self-assembles monolayer (SAM) adducts causing dielectric properties to change and their detection by impedance measurement techniques[6]. With these developments, EIS became an increasingly popular label-free detection tool for many types of biosensors.

EIS is capable of more sensitive detection than either voltametric or amperometric methods. With the development of second generation FTEIS and its fast measurement range, EIS is used as a detection tool for an array of hundreds of electrodes on DNA or biochips. The work in [21] presents an application of CMOS EIS biosensor 10 x 10 array to detect various biological analytes, such as

DNA and proteins, in real time without the need for molecular labels. EIS has found applications in DNA hybridization, single-neucleotide mismatches and DNA's interactions with other molecules with the development of electrochemical DNA hybridization sensors [29]. Through the use of appropriate strategies, a target DNA having single mismatch with the probe DNA can be distinguished from its fully complementary target DNA.

EIS has also been proposed as a simple non-invasive technique to monitor the amount of fat and liquids contained inside the human body. This technique is also being called bioelectrical impedance analysis (BIA) [8, 30]. This non-invasive frequency screening technique with the use of Multi-frequency EIS is relatively simple and research has demonstrated application in breast cancer screening [16]. The most common form of breast examination system available is mammography that by its use of x-ray is an expensive and health hazardous breast screening procedure. EIS has been the subject of intensive research in this area for about 20 years. EIS is also being viewed as a medical imaging technique in which an image of the conductivity or permittivity's of part of the body is inferred from surface electrical measurements. The advantages of EIS over other medical imaging techniques is that it is comparatively cheap and has no health hazards attached to it. The data can be collected very rapidly and long term monitoring physical function is possible in EIS as compared to other techniques.

EIS has also been exploited for low-invasive diagnosis of metallic prosthesis osseointegration by characterizing the quality of the tissue at the interface between the bone and the prosthesis [4, 8]. Preliminary clinical experimental results show EIS as a valid alternative, no-destructive and low-invasive technique, to the diagnosis of osseointegration level [4].

2.4 Previous work on portable EIS devices

In the previous section, it is seen that EIS is widely used for health monitoring systems and medical device applications. But EIS is a technique that requires expensive equipment which runs on high end software and has a sophisticated interface to connect the electrochemical cell to the hardware and software [5]. Many times EIS tests are performed on objects located directly in the field. An example of one such use of impedance spectroscopy is the testing of anticorrosion coatings on bridges, pipeline and other steel structures [13]. For health monitoring applications as well, the tests are all performed in the laboratories as the large size of existing EIS equipment [17, 23] makes it difficult to integrate such techniques into small form factor systems that are hand-held, wearable and intended for use in point-of-care testing. One of the many commercial EIS systems available is manufactured by Gamry Instruments, USA and is called the Reference 3000 potentiostat [31] which is equipped to perform EIS from high impedance coatings to low impedance supercapacitors. The product can also operate as a potentiostat, glavanostat, Impedance response analyzer and frequency response analyzer. It handles 2, 3, and 4 electrode measurements with ease, interfaces with lab computer and weighs about 7 kg. Another commercially available EIS system is marketed by Metrohm Autolab B.V. [23, 32] which are capable of both single frequency and multi frequency EIS measurements. Recently Metrohm Autolab has also been working on portable potentiostats called the mini-series [33] for simple and entry level electro-analytical techniques, fuel cells, solar cells etc. There are no commercially available EIS systems that are miniaturized enough and enable wireless communication between the measuring device installed in the field and a personal computer. Due to these facts, developments have been performed on realization of a portable analyzer AD5933 from Analog Devices, USA which resulted in the prototype presented in [34] and also the main aim of the thesis presented.

The idea of portable multi frequency device for measurement of electrical bio-impedance was first discussed as early as 1995 in [15]. A multi frequency device for measurement of the modulus and phase shift of complex electrical impedance of the biological tissue was shown. The device had a phase and peak detector circuit and its first application was the measurement of the transthoracic impedance which was based on tetrapolar current method. The device was interfaced to a personal computer and measured impedance in the range of 2Hz – 200 kHz. The instrument described in [2] tried to increase the portability by embedding all the components into a single fully independent device that provided both portability and low-cost requirements. The system used a signal generator built with two pulse width modulation (PWM) oscillators and an autocalibration system. It included a Digital Signal Processor (DSP) with an Analog to Digital Converter (ADC) and communication to the PC, where the impedance was calculated by fitting data from all measurements. The above and currently available commercial EIS platforms commonly use off chip signal generation techniques that make the system bulky [1-3, 11, 13, 21,]. These systems of EIS also suffer from long measurement times at the interface stage to sensor [1]. An on-chip EIS system that introduces a methodology and circuit that can rapidly perform EIS in the 1 mHz to 100kHz range has been shown in [7]. The circuit has been realized with CMOS technology and has found applications on detection of lipid bilayers in biosensor arrays. Another CMOS-based EIS system extract magnitude and phase information using in-phase and quadrature mixtures that increases the measurement times due to time required for low pass filters to settle [21].

In [3], a microcontroller based EIS system for prostheses osseointegration has been prototyped. The impedance measurement of the device is based on the classical EIS method where a sinusoidal stimulus is injected into the tissue which is controlled by a software running on PC and measurements are carried out in the 50Hz to 1 kHz range. This system extracts magnitude and

phase information using a seven-parameter sine fitting algorithm which is faster, but requires a lot of processing at the signal processing end [3]. Other EIS prototypes, implement external phase detector circuits to extract the phase information and heavily reduce the measuring range and adds hardware overhead [3, 9].

In the reference [11], a feedback system calculates the impedance of a circuit under test using a peak detector external circuit which limits the measurement times to milliseconds for each iteration. Here, a trans-impedance amplifier (TIA) based architecture is used to calculate the magnitude of the signal that limits high frequency ranges due to comparator delays. Another time domain EIS integration method has been discussed in [10] where the sinusoid stimulus is again generated by using external DAC without the need for analog filter. Compared with traditional structure, the proposed system does not require clean quadrature sinusoid stimulus and therefore eliminates the need for power and area hungry analog filters. This microsystem was also implemented in a CMOS technology and can work well in low frequency 0.1 Hz – 10 kHz applications.

Very recent developments in the portable EIS systems include the Arduino-based portable system for bioelectrical impedance measurement [8]. The circuit takes advantage of the ADC and DAC made available by the board and employs a logarithmic amplifier to extend the impedance measuring range to 6 decades without using complex programmable gain amplifiers. The EIS can be measured in the frequency range of 1 Hz – 100 kHz and can be stored on a PC with a wireless link.

This similar work with the use of logarithmic amplifier at the front end has been repeated in [9] for the measurement of impedance in the frequency range of 1 mHz – 100kHz. The system also employs a commercially available Arduino Due board for the signal generation/acquisitions and for the processing and a simple front-end based on a logarithmic amplifier thus avoiding complex programmable gain amplifiers. Both these prototypes claim to be low cost and portable EIS systems ranging in the price of $50- $150 with overall uncertainty of below 5% of amplitude and a few degrees of phase.

2.5 Square wave EIS

As mentioned in Section 2.1, the process of EIS includes passing a frequency varying sinusoidal stimulus through an electrochemical cell and determining the response current. The magnitude and phase difference of the measure response current with respect to the input voltage then determines the charge transfer resistance which is one of the characteristics determined by EIS. This approach is also known as the traditional approach of performing spectroscopy. It is found in literature that the same EIS characteristics can be achieved by using variable frequency square wave stimulus instead of sine wave stimulus [1]. These small form factor EIS platforms mentioned in Section 1.3 use different methods to generate the sine wave stimulus. Some use the DDS technique [8, 9], PWM sine wave generation or DAC sine wave generation [10, 21].

3.System Design

3.1 System Level Block Diagram

The hardware design for the proposed microcontroller based prototype is as shown in Figure 3.1. The system design consists of a signal generator block that generates the sinusoidal voltage stimulus, the electrochemical cell, the analog interface circuit that interfaces the cell to the system and signal processing block. The main components of the system are (1) DSC (Digital Signal Controller) with peripherals, (2) Equivalent Circuit and Sensor, and (3) Analog Interface.

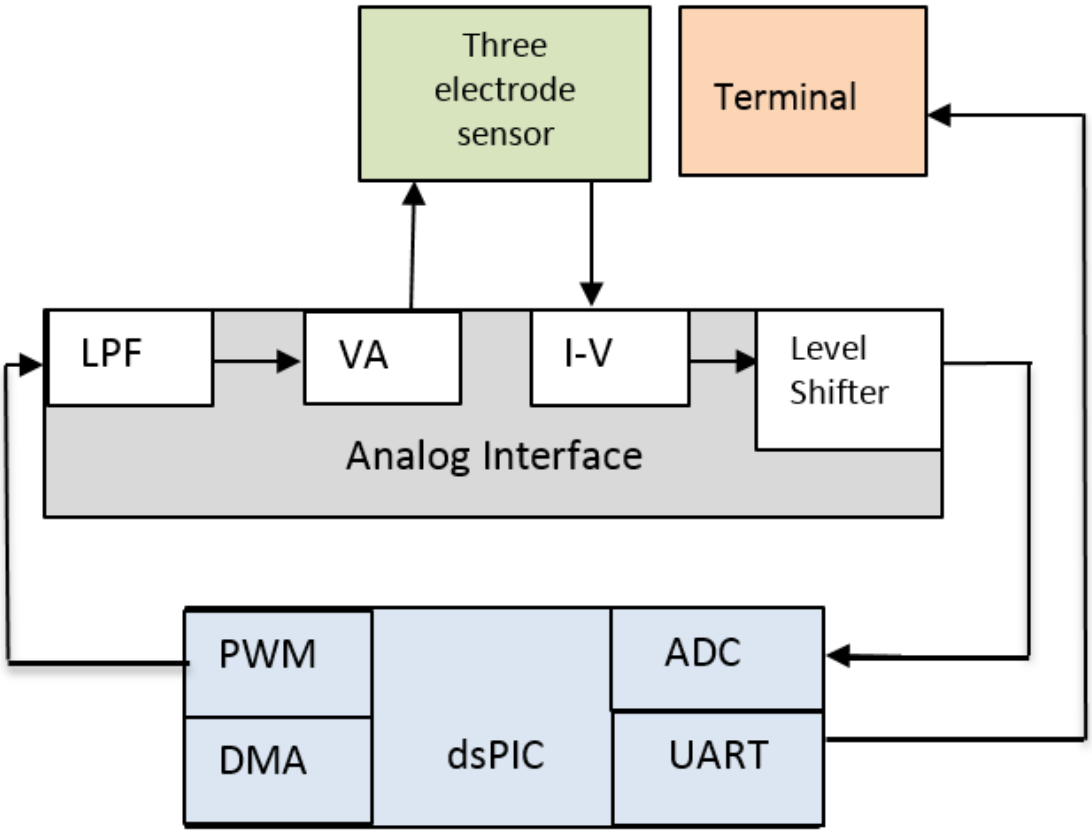


Figure 3.1 Block Diagram of the proposed EIS system

3.2 Digital Signal Processor (DSP):

The Digital Signal Processor (DSP) is a core functioning hardware of the EIS platform. Microcontrollers are used as control devices and are well suited for interfacing sensors, communication devices and other forms of support hardware. The control unit for the EIS platform is chosen from the dsPIC33F device family manufactured by Microchip Inc. that integrates the control features of a Microcontroller (MCU) with the computational capabilities of a Digital Signal Processor. This processor is ideal for applications like EIS that require high-speed, repetitive computations as well as control. The main attraction of the EIS platform is that it performs most of the functionalities with the support of different modules on the microcontroller and eliminates extra hardware. All PIC microcontrollers are programmed using the MPLABX Integrated Development Environment (IDE) that supports program downloaded into the microcontroller along with debugging options using the ICD3 programmer and debugger. The development environment supports the programming of the microcontroller using the high level language C with the support of XC16 compiler.

The DSP (Microchip Inc.) is a 16-bit Microcontroller Unit (MCU) that controls major blocks of the hardware. The controller with its DSP engine, 40-bit accumulators, hardware support for performing operations like divisions, barrel shifter, with 17 x 17 multiplier, large array of 16-bit working registers and a wide variety of data addressing modes, together provide the Central Processing Unit (CPU) with extensive mathematical processing capability. The DSP has flexible and deterministic interrupt handling, along with a powerful array of peripherals that renders the device suitable for applications requiring control. The process of EIS requires large amounts of data to be transferred between the peripherals and control unit. The Direct Memory Access (DMA)

enables overhead-free transfer of data between several peripherals and a dedicated DMA RAM. It also has a reliable, field programmable Flash program memory that ensures scalability of applications.

The dsPIC33FJ256GP710 is a 100-pin, 40 MIPS, 16-bit high performance DSC CPU. It is based on modified Harvard architecture. The Digital Signal Processor (DSP) has several features that contributed to its selection as a part of the design and requirements mentioned in the Section 1.4.

- Low power consumption mode
- A 10-bit, 1.1 Msps or 12-bit, 500 Ksps conversion Analog to Digital Converter (ADC) with 2,4 or 8 simultaneous sampling and 32 input channels with conversion in Sleep mode
- 8 16-bit Timer/Counters/Compare/PWM modules and 1 timer runs as Real-Time Clock with external 32.768 kHz oscillator
- Up to 85 programmable digital I/O pins that can work from 3.0 V to 3.6 V
- 64 Kb of Data Memory and 256 KB of programmable flash memory
- 3-wire SPI modules, I2C and Enhanced High Speed Baud mode UART modules.
- 118 interrupt vectors with 7 programmable priority levels
- Flexible clock options ranging from external, crystal, internal RC to fully integrated PLL
- On-chip 2.5 V voltage regulator with real time switching between idle, sleep and doze modes with fast wake-up
- 8-channel hardware DMA that allows data transfer between RAM and a peripheral while CPU is executing code

3.2.1 Pin Description

The DSP/dsPIC has 100 pins. Figure 3.2 illustrates the pin diagram of the microcontroller. Colored highlighting is used to indicate which pins are being used in for connections to the

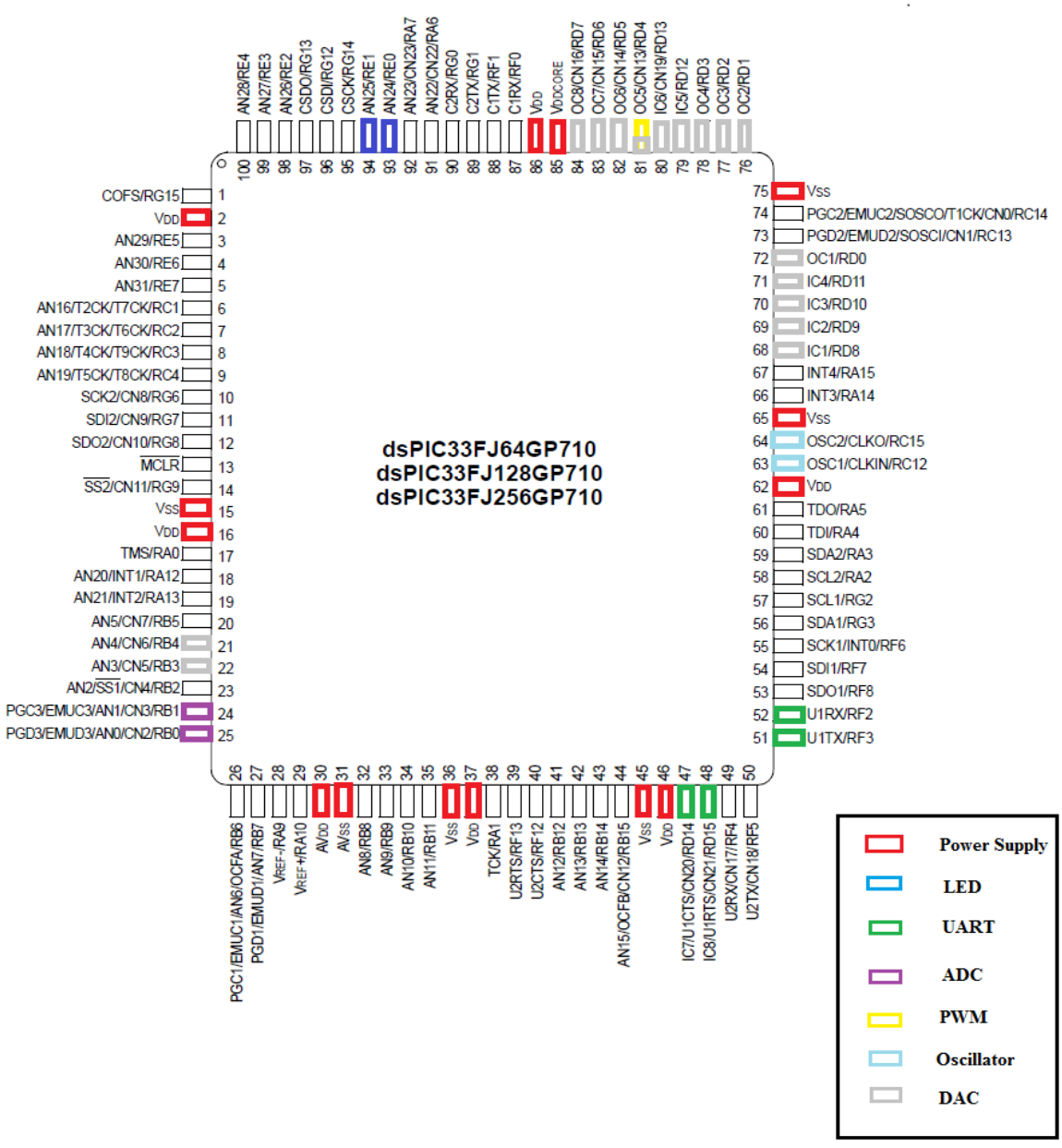


Figure 3.2 Pin Diagram of dsPIC33FJ256GP710 where color coding indicated the connections to various peripherals

corresponding peripherals. Table 1 lists the pins that are being used and provides a brief description of the pin function.

Table 1: Pin Description table for the dsPIC33FJ256GP710

Pin Name	Pin No	Function	I/O	Description
OSC1/RC15/CLKIN	64	OSC1	I	Oscillator clock input
OSC2/RC12/CLKO	63	OSC2	I	Oscillator clock input
U1TX/RF3	51	U1TX	O	UART Data Transmit Pin
U1RX/RF2	52	U1RX	I	UART Data Receive Pin
IC7/U1CTS/RD14	47	U1CTS	I	UART Clear to Send Pin
IC8/U1RTS/RD15	48	U1TRS	O	UART Request to Send Pin
OC5/CN13/RD4	81	OC5	O	PWM signal generation Pin
PGEC3/AN1/RB1	24	AN1	I	ADC input for output response of electrochemical cell
PGED3/AN0/RB0	25	AN0	I	ADC input for reference given to electrochemical cell
RD0-RD13	68-72, 76-84	RD0-RD13	O	Connected when DAC used, Parallel Data Pins for 14-bit data
RB3, RB4	22,21	CS, WR	O	Connected with DAC only, Chip select and Write Pins
MCLR	13	MCLR	I	Memory clear input Pin

3.2.2 I/O Ports

There are 85 digital I/O pins on the dsPIC that are shared between peripherals and parallel I/O ports with improved noise immunity. The I/O ports are divided as nine general purpose ports – A, B, C, D, E, F, G, H and J. When a peripheral is enabled, the pin associated with it is also enabled and the use of the pin as a general purpose output pin is disabled. Each of the ports are bidirectional and 8-bit wide and only PORT G which is 6-bit wide.

To program each port, there are registers associated with them

1. **PORT** register – Used to read the levels in the associated pins.

2. **TRIS** register – Used to specify the direction of data on the pin. A pin can be set as an input or output pin by setting it as 1 or 0 respectively.
3. **LAT** register – Register used to read/modify/write the values of the port. This is the only register that is used to write any value on the port.

In addition to the PORT, LAT and TRIS registers for control of data, each port pin can also be individually configured for either digital or open-drain output. With the use of special registers, some pins can also be configured as analog port pins for the ADC.

3.2.3 Oscillator Configuration

There are three different ways of clocking the dsPIC microcontroller: the Primary Oscillator, the Secondary Oscillator and the Internal Oscillator that is embedded into the chip circuitry. An on-chip PLL system provides the internal operating frequency to the required system frequency. The system can also switch between various clock sources and has programmable clock postscaler for system power savings. A Fail-Safe Clock Monitor (FSCM) detects clock fail and takes fail-safe measures.

1. Primary Oscillator from external crystal connected between OSC1 and OSC1 pins. For the EIS platform we have an 8MHz crystal oscillator connected between these pins.
2. Secondary Oscillator is also an external oscillator source and is most often a 32.768 KHz crystal. This oscillator is sometimes used with Timer 1 as a time base for real time clock.
3. Internal Oscillator runs at a nominal 7.37 MHz frequency and can be used with the PLL thereby allowing full-speed operation without any external clock generation hardware.

There are seven system clock options provided by the dsPIC33F:

- FRC Oscillator and FRC Oscillator with PLL

- Primary (XT, HS or EC) Oscillator
- Primary Oscillator with PLL
- Secondary (LP) Oscillator
- LPRC Oscillator
- FRC Oscillator
- FRC with postscaler

Figure 3.3 shows the different clock sources for dsPIC33F and the modules that are used are marked in red. In the platform, the external primary oscillator is used with the PLL to generate a

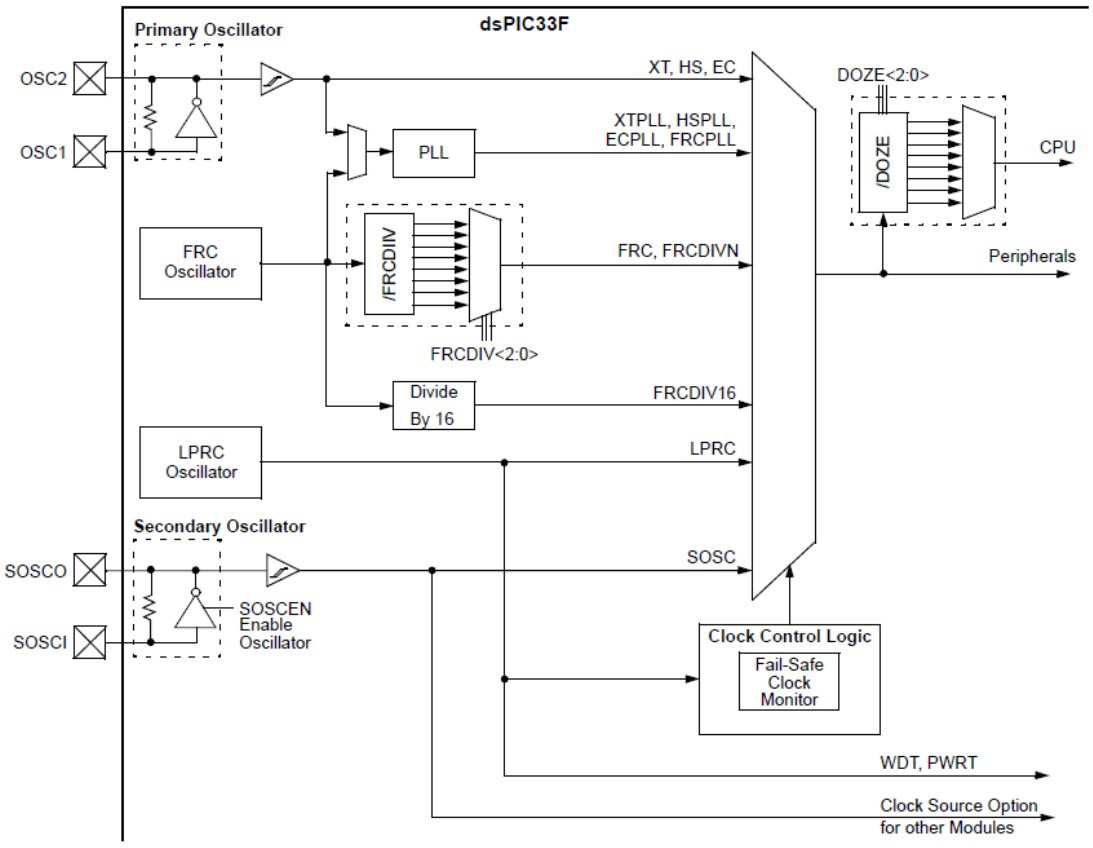


Figure 3.3 Illustration of Oscillator Configuration [37]

frequency of 40 MHz for the system. This is because the instruction execution speed or device operating frequency (F_{CY}) up to 40MHz are supported by the dsPIC33F.

Instruction execution speed or device operating frequency, F_{CY}, is given by

$$FCY = FOSC/2 \tag{12}$$

For the primary oscillator with PLL mode, the PLL output F_{OSC} is given by

$$FOSC = FIN * (\frac{M}{N1 * N2}) \tag{13}$$

where FIN is the frequency of the crystal oscillator = 8MHz in this case. M is a factor by which the input frequency to the VCO is multiplied to achieve PLL. N1 and N2 are prescale and postscale factors and can be selected using special registers to achieve the desired frequency. Therefore, the device operating frequency can thus be calculated as

$$FCY = \frac{FOSC}{2} = \frac{1}{2}\left(\frac{FIN * M}{N1 * N2}\right) MIPS \tag{14}$$

The design of oscillator is parallel cut crystal. The device uses 8 MHz 20 pF crystal. Figure 3.3 shows the connections. Capacitors C1 and C1 are 22pF ceramic capacitors.

3.2.4 Timers

The dsPIC has 9 16-bit timers with selectable timing modes and a combination of two timer modules can be configured as one 32-bit timers. They support the features of timer gate operation with selectable prescaler settings. They also function during Idle and Sleep modes. A few selectable timers can be configured for use as a time base for Input Capture and Output Compare Modules and also for ADC Event Triggering and DMA data transfer.

In this research, the timers are used in 16-bit configuration mode with the prescaler disabled. Timers are used for signal generation with the PWM module, signal acquisition with the ADC interrupts for ADC event triggering.

3.2.5 Interrupts

The dsPIC33F has several internal and external interrupt sources, a few exceptions and software traps. It also consists of an interrupt controller that reduces work of the controller by using only one interrupt request signal to the CPU for all the numerous peripheral interrupt request. The controller does so by using the Interrupt Vector Table (IVT) that has a unique vector for each of the 126 interrupts or exception sources. Interrupt vectors have priorities and are organized in terms of their natural priority and this organization is linked to their position in the vector table. The user can select up to 7 priority levels and lower addresses in the vector table have higher priority.
In general, the interrupt vectors can be selected and priorities assigned with the help of interrupt control registers. Three bits are assigned to control the operation of interrupts.

1. **Priority** bit: This is used to set priority levels on the interrupt source.
2. **Enable** bit: The program branches to the interrupt vector only when the corresponding enable bit for the interrupt source is set.
3. **Flag** bit: This bit is set when the interrupt occurs.

In this thesis, the device uses Timer 2 Interrupt for the Output Compare match for the generation of sine wave. Timer 3 and Timer 5 ADC interrupt are used for ADC sampling for the input voltage and output response current of the electrochemical cell and circuit in use.

3.2.6 Pulse Width Modulation (PWM) Module

The Output Compare (OC) module is used in this application to generate the Pulse Width (PWM) signal. It does so by comparing the value of an associated timer with a comparison register and an operation mode. Whenever, there is a match between the comparison register and the timer output, the pin is toggled. The Output Compare module has many operating modes, one of which is the PWM mode. The PWM hardware block diagram is shown in Figure 3.4.

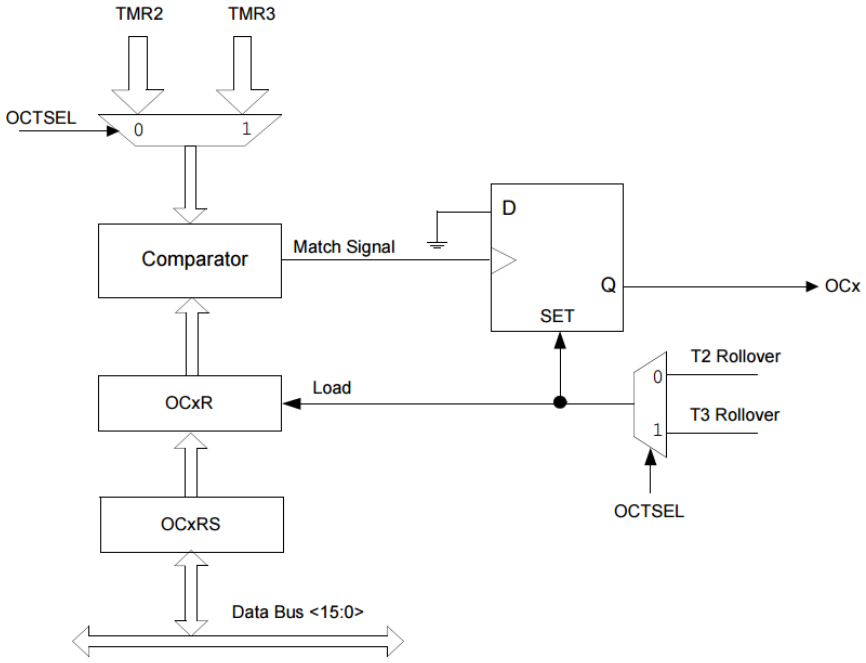
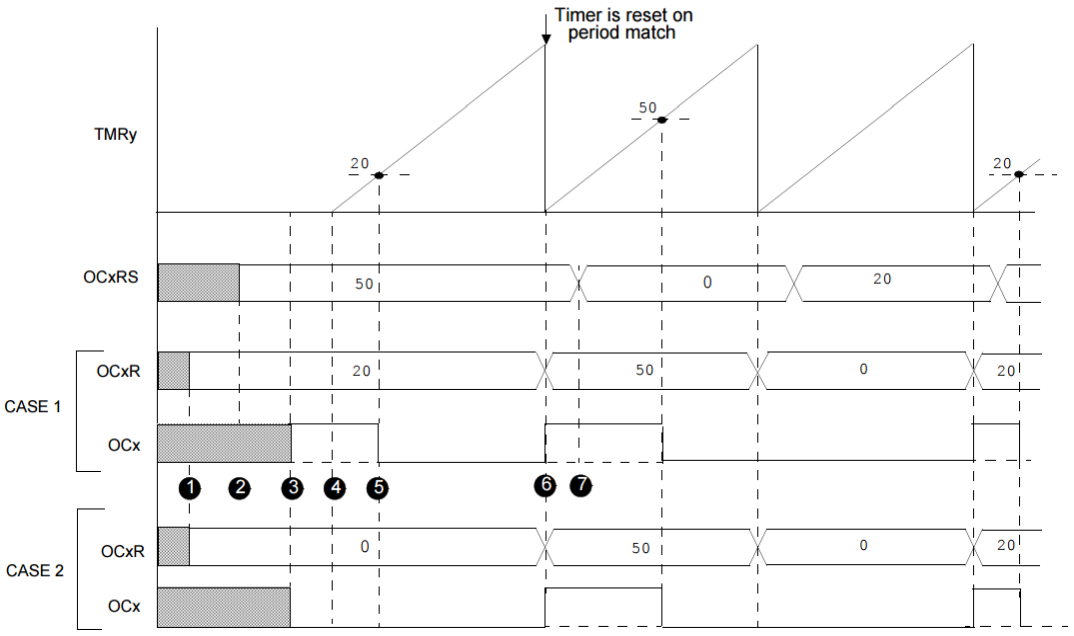


Figure 3.4 PWM hardware block diagram [37]

The PWM mode is used to generate variable duty cycle count. This module is used to generate the sine wave stimulus to be applied to the electrochemical cell. The PWM duty cycle is specified through Secondary Output Compare (OCxRS) register. A timer is used with this module which when enabled, starts incrementing until it reaches the value in the period register. The Compare Register (OCxR) value is constantly compared with the timer value. When a match occurs, the OCx goes low. For the generation of sine wave, it is required to have variable duty cycle which is entered in the OCxRS register. The duty cycle is written at any time, but it is only latched when there is a Reset on a period match. This is important because it offers an extra space for PWM duty cycle that is a buffer and is important for smooth PWM operation.



1. The duty cycle for first PWM cycle is written to OCxR register before enabling the PWM mode.
2. The duty cycle for second PWM cycle is written to OCxRS register.
3. PWM mode is enabled, OCx pin is driven low if OCxR is zero. OCx pin is driven high if OCxR is non-zero.
4. Timer is enabled and starts incrementing.
5. On a compare match, the OCx pin is driven low.
6. On timer rollover, OCxRS value is loaded into OCxR register. OCx pin is driven high if OCxR is zero. OCx pin is driven low if OCxR is non-zero.
7. The duty cycle for third PWM cycle is written to the OCxRS register.

Figure 3.5 PWM Mode Operation [37]

The PWM period is written in to the PRy, the TMRy period register and is calculated using the following equation

$$PWM\ Period = \frac{1}{PWM\ Frequency} = [(PRy) + 1] * TCY * (TMRy\ Prescale\ Value) \quad (15)$$

- If the duty cycle register has value of 0h, it is zero percent duty cycle (0% duty cycle)
- If thevalue is greater than PRy (Timer Period register), the OCx is high (100% duty cycle)

The PWM resolution depends on PWM frequency and the timer clock frequency and is given by the following equation

$$PWM\ Resolution(bits) = log_2\left(\frac{PWM\ Frequency}{Timer\ Clock\ Frequency}\right) bits \quad (16)$$

3.2.7 Analog-to-Digital Converter (ADC)

The dsPIC33F includes a Successive Approximation (SAR) Analog-to-Digital Converter (ADC) that can be configured to function as a 10-bit, 4-channel, 500 ksps ADC or a 12-bit, single channel, 1.1 Msps ADC.

The useful features of ADC that have been used in the development of the platform are:

- Four Sample and Hold (S&H) amplifiers that are unipolar and differential
- Simultaneous sampling of up to four analog input pins
- Automatic Channel Scan availability
- Conversion trigger source selection
- Buffer Filling Selection availability
- Dynamic Memory Access (DMA) support

- Operation support during Sleep and Idle modes of CPU
- Up to 32 analog input pins

The analog-to-digital conversion process is converted in three steps. In the first step, the input voltage signal is connected to the sample capacitor. The sample capacitor is then disconnected from the input in the second step. Finally, the stored voltage is converted to their equivalent digital bits. The sampling time (T_{SAMP}) and conversion time (T_{AD}) can be calculated and the phases can be set to start manually or automatically. The 32 analog input pins are connected to four S&H amplifiers called CH0- CH3. However, as can be seen from Figure 3.6, the ADC module has only

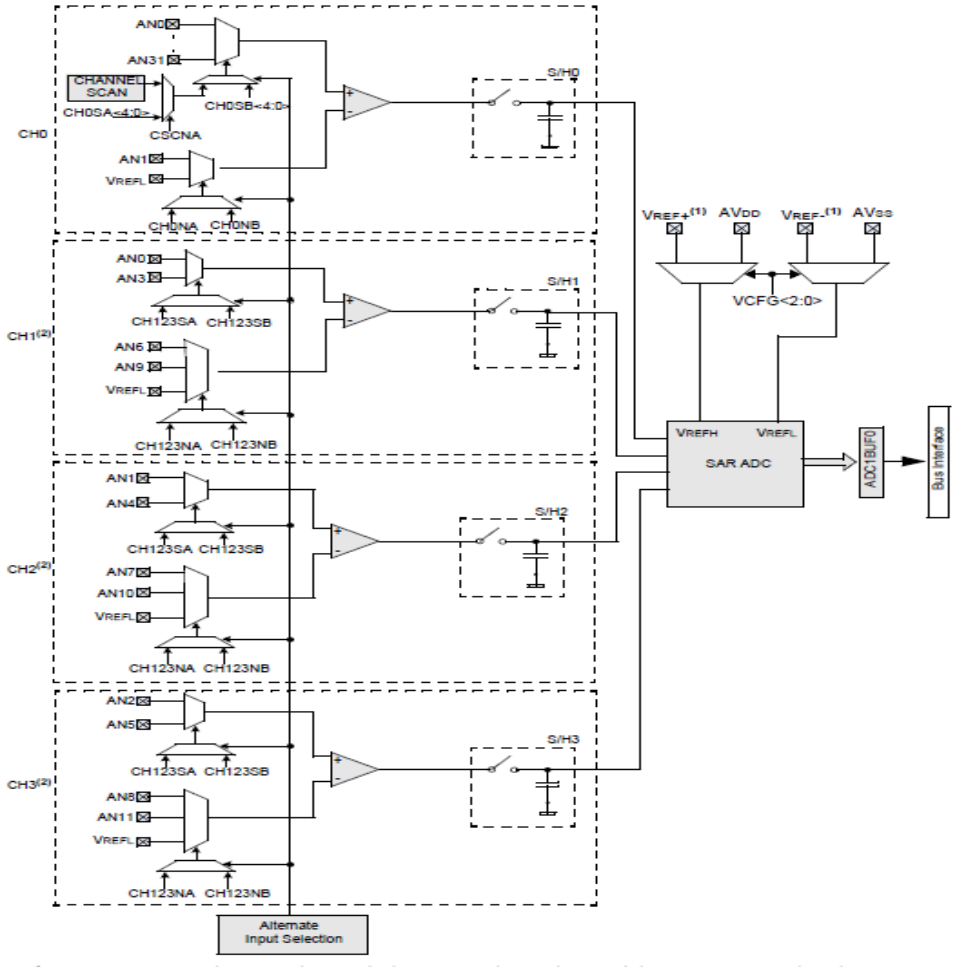


Figure 3.6 ADC Block Diagram for Devices with DMA [35]

one conversion unit. The multi-channel ADC typically converts each input channel one after the other using an input multiplexer.

For the EIS application, it is required to sample and convert the input signal voltage given to the electrochemical cell and the output current response converted into voltage. This means the application requires simultaneous sampling of channels since the phase information exists between these two channels. The simultaneous mode is selected by setting the simultaneous sampling bit in the ADC register. Figure 3.7 shows the timing sequence for 2-channel simultaneous sampling.

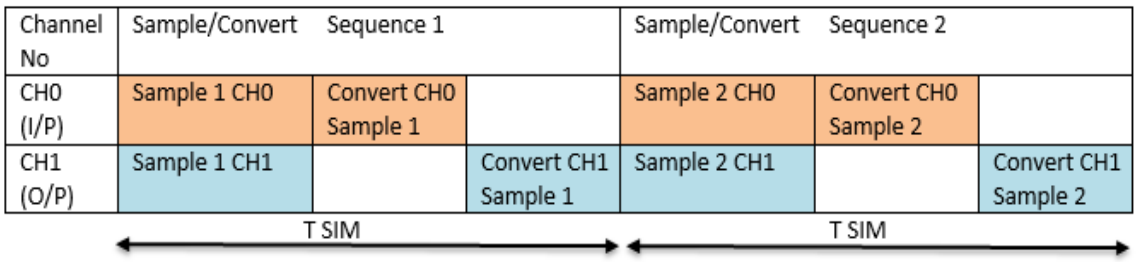


Figure 3.7 2-Channel Simultaneous Sampling

Calculation of Effective Conversion Time (TAD) for 2-Channel Simultaneous Sampling

According to the electrical characteristics of dsPIC33FJ256G710 [Ref NO], the minimum effective TAD is 70 ns and the minimum effective TSAMP is 1 TAD. At 40MIPS, TCY= 25ns. Since the minimum TAD time is 70ns, 3 TCY would be 75ns, which is as close as possible to the minimum effective conversion time. Since, this is simultaneous sampling, all channels are sampled at the same time then converted sequentially as there is only one conversion hardware. While a channel is converting no new samples on that channel are permitted. In the case of simultaneous

sampling, since all the channels are sampled together, it is imperative to wait for all channels to be converted before sampling again. This total conversion time calculation is shown below

$$Min\ TAD = 70\ ns \tag{17}$$

$$Min\ Sample\ Time\ (TSAMP) = 1\ TAD \tag{18}$$

And it is already known that,

$$TCY = \frac{1}{40} MIPS = 25\ ns \tag{19}$$

$$Min\ effective\ TAD\ in\ TCY\ (TADtcy) = \frac{70ns}{25ns} = 3 \tag{20}$$

$$Min\ eff\ TAD\ in\ ns = 3 * 25ns = 75\ ns \tag{21}$$

Now, for the platform, two channel CH0 and CH1 are being used for input and output respectively. Therefore, maximum effective sample rate per channel is,

$$\begin{aligned} Maxm\ Eff\ \frac{Sample\ Rate}{Channel} &= \frac{1}{Sample\ Time + Conversion\ time} \\ &= \frac{1}{1TAD + (\#channels + 12TAD)} \\ &= \frac{1}{1TAD + 24TAD} = \frac{1}{25TAD} = \frac{1}{25 * 75ns} \\ &= 533.33kHZ \end{aligned} \tag{22}$$

Finally, the value of conversion trigger source through Timer 3 is

$$PR3 = \frac{FCY}{533.33kHZ} = 75 \tag{23}$$

ADC Reference Voltage settings:

The voltage reference for ADC conversions is selected in the software either internally or externally. The voltage reference high (VREFH) and voltage reference low (VREFL) in the ADC module is supplied internally by AVDD and AVSS pins while the external VREF+ and VREF- require certain specifications. For the EIS platform, internal voltage references of AVDD and AVSS are used. Since two channels are being sampled simultaneously, 10-bit ADC is used and the conversion voltage appearing in the buffer is calculated as

$$ADC\ Voltage\ in\ mV = \left(\frac{Reference\ in\ mV}{1023}\right) * ADC\ Value \tag{24}$$

In the system, reference value used is 3.3V. Given the 10-bit value it can be converted back to the analog input voltage as follows

$$ADC\ Voltage\ in\ mV = \left(\frac{3300}{1023}\right) * ADC\ Value \tag{25}$$

3.2.8 Direct Memory Access (DMA):

The Direct Memory Access (DMA) is a very efficient mechanism of moving data between Special Function Registers and buffers and variables stored in RAM, with minimum CPU intervention. The DMA is equipped with a controller that can automatically copy entire blocks of data without the user software requiring to read or write registers every time a peripheral interrupt occurs. It works with a dedicated bus for data transfers and therefore, does not use the cycles of the CPU from the code execution.

The peripherals on dsPIC33F with DMA support are Input Capture, Output Capture, Timers, ADCs, UART, SPI and ECAN transmission and reception. Some more features are

- Word or byte sized data transfers

- Transfers from any microcontroller peripheral to DMA RAM and vice versa
- One shot or Continuous Block Transfers
- Block transfers that are selectable to be manual or automatic
- Ping-pong mode-switching between two DMA RAM start addresses between the block transfers

After a block has been transferred completely, a DMA interrupt request is generated for each DMA channel. The block diagram of the DMA in action is shown below in Figure 3.8.

The following steps are to be followed closely to configure each DMA channel and peripheral, for each DMA data transfer to operate properly:

1. The first step is to associate the DMA channel to a Peripheral which is a target address to the controller such that it can read from and write to the peripheral. Each peripheral has a dedicated register value to read from and write to.
2. The second step in the DMA set-up process is to properly configure DMA-ready peripherals for DMA operation. For example, when using the peripheral ADC with DMA and selecting the Peripheral Indirect Mode, the two bits that need to be set appropriately are the Increment Rate for the DMA Addresses bits and the number of DMA Buffer locations per analog input. Also, the DMA Buffer Build mode bit in the ADC control register must be properly set for address generation.

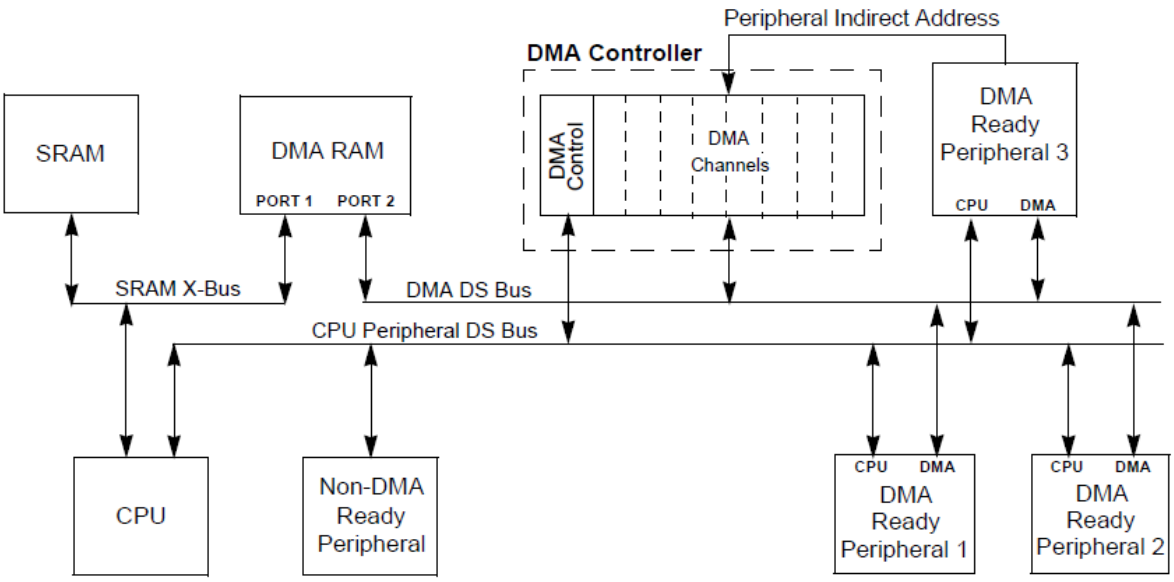


Figure 3.8 Top Level System Architecture using a dedicated transaction bus [36]

3. Within a specific area of memory the buffers are allocated in the next step. The device being used as the peripheral gets the authority to decide the location and size of the memory. For proper operation, the DMA should be provided with the DSPSRAM address that functions as the needs to know the DSPSRAM address to read from or write to as an offset from the beginning of the DMA memory.
4. In the fourth step of DMA set up process, a single DMA channel is to be programmed to understand N+1 number of requests before the transfer of data clock is finished. The DMA Channel Transfer Count Register is responsible for providing the value of 'N'.
5. In the final step of the DMA setup, the DMA Channel Control register is used to write the mode of operation. The DMA channel supports many modes of operation; a few of which are mentioned below:
    - Word of Byte Data transfer
    - Transfer direction

- Full or Half transfer interrupts to CPU
- Peripheral Indirect Addressing
- One-Shot or continuous block transfers
- Auto-switch between two start addresses offsets
- Null Data Write mode

For the ADC operation, the DMA is used in Peripheral Indirect Addressing mode. In the specified mode the peripheral, not the DMA channel, provides the changeable part of the DPSRAM address. The DMA request from the peripheral is accompanied by an address that is presented to the DMA channel. The buffer base address is then logically OR with the zero extended incoming Peripheral Indirect Address and the actual DPSRAM address is created as shown in Figure 3.9.

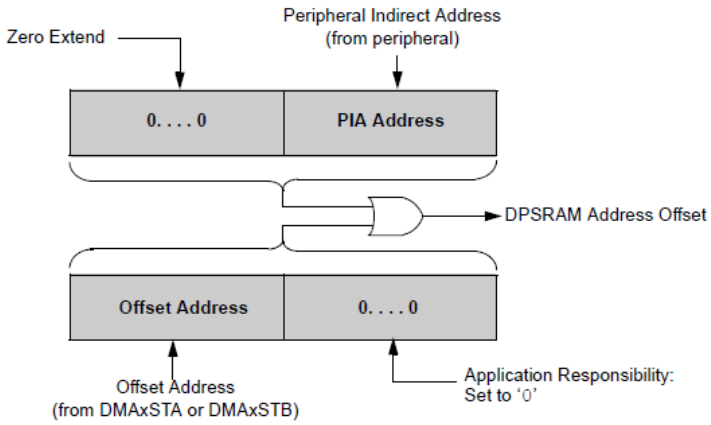


Figure 3.9 Address Offset Generation in Peripheral Indirect Addressing Mode [36]

The example in Figure 3.10 shows how the DMA transfer moves ADC data into separate buffers when the DMA channel is configured in Peripheral Indirect Addressing Mode.

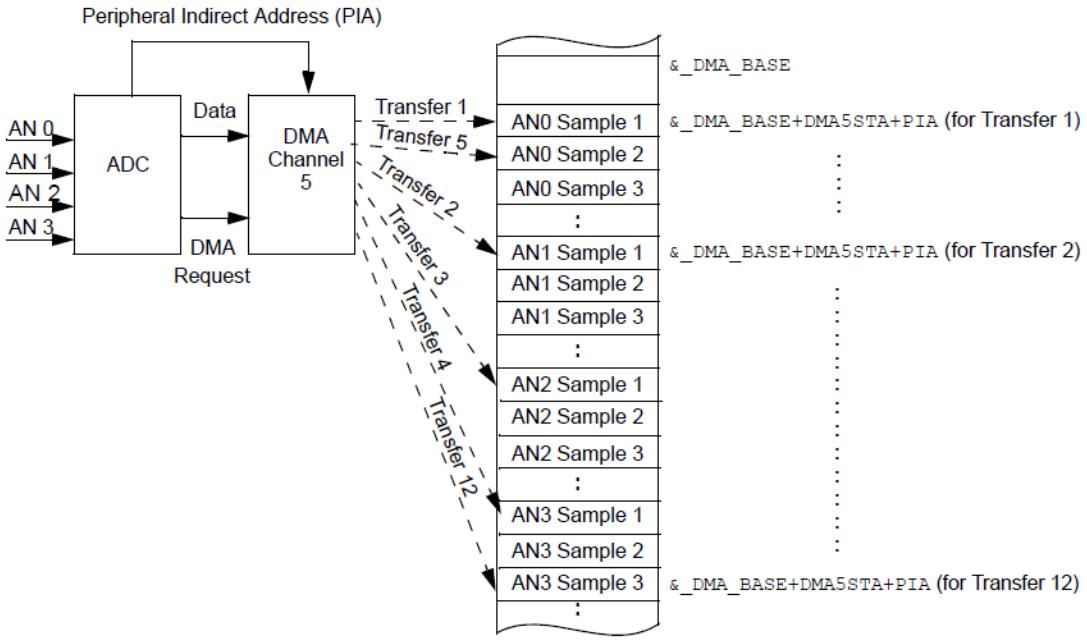


Figure 3.10 Data Transfer from ADC with Peripheral Indirect Addressing [36]

3.2.9 UART Module

Of the many serial I/O modules available in the dsPIC33F device, the Universal Asynchronous Receiver Transmitter (UART) module is used in this application. The UART is a full duplex asynchronous system that can communicate with the peripheral, in this case, a personal computer interface. The module is equipped with a hardware flow control option with the UxCTS and UxRTS pins and also includes an IrDA encoder and decoder. A simplified block diagram of the UART module is shown in the Figure 3.11 below.

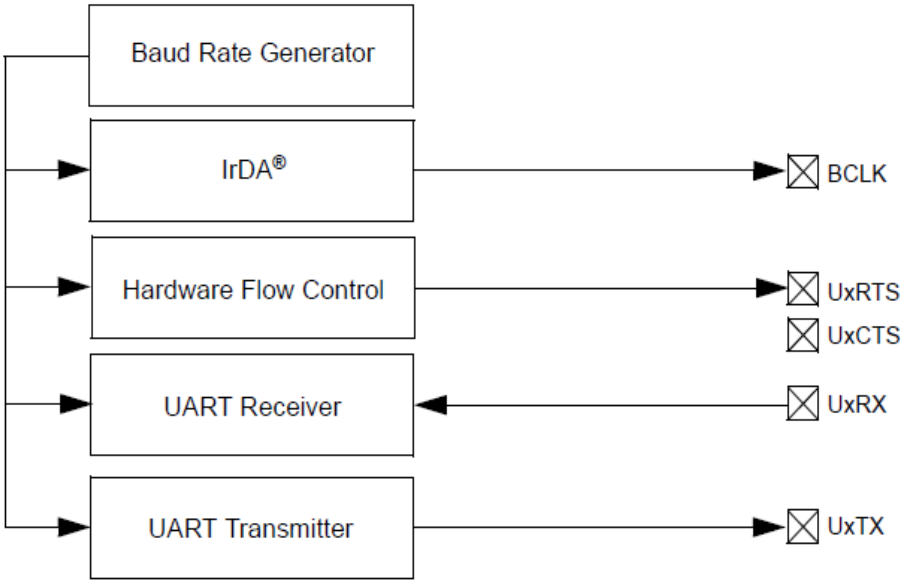


Figure 3.11 UART Simplified Block Diagram [37]

The UART module includes a fully integrated Baud Rate Generator with 16-bit prescaler. Baud rates ranging from 1 Mbps to 12 bps at 16 MIPS can be achieved. A register BRGx is dedicated to UART module which controls the period of a free running 16-bit timer. The following equation shows the formula for computation of Baud Rate and the corresponding value that is to be written in the BRGx register for the desired Baud Rate. For this application, a Baud Rate of 9600 bps is desired and the corresponding value for the period register is calculated using the equation.

$$Baud\ Rate = \frac{FCY}{16 * (BRGx + 1)} \tag{26}$$

$$BRGx = \frac{FCY}{16 * Baud\ Rate} - 1 \tag{27}$$

Where F_{CY} denotes the instruction clock cycle frequency ($F_{OSC}/2$)

3.2.10 Programming the dsPIC

The requisites for programming a dsPIC are listed below. These resources must be ready and installed/connected before starting code development.

- MPLAB X IDE, free Integrated Development Environment available for download from Microchip's website.
- MPLAB XC16 Compiler
- An MPLAB X compatible programmer/debugger, for example, PICkit3 or ICD3(In-Circuit Debugger 3)
- The Explorer 16 board, or any demonstration board

The sequence of getting the board programmed is as follows

- The first step is to write the **source** code, which is written in either C or assembly language in the MPLABX IDE. The source code is saved as a .c file.
- The next step, Compiling, is initiated by the IDE upon execution of the Build command. For this step, the XC16 **compiler** is used to create an object code file (.o) which is not a completely executable file because all addresses of functions and variables remain undefined in this step.
- The third step begins when the MPLAB C **linker** is used and a home is found for each function and variable in the memory space. In this step, all the pre-complier object code files and standard library functions are also added. Among the several output files produced by the linker, the actual binary executable file is (.hex).

- Lastly, the **programmer**, in this project the ICD3 (programmer/debugger), is invoked that uses the .hex file to program the dsPIC over the modular (six conductor) cable using the RJ-11 connector. Figure 3.12 shows the connections between ICD3 and the target microcontroller. The ICD3 can also be used as a debugger by invoking the Debug command in the IDE. The ICD3 is USB powered and provides a programmable voltage power supply of 3-5V. All debug features are turned off or removed when the debugger is used as a programmer.

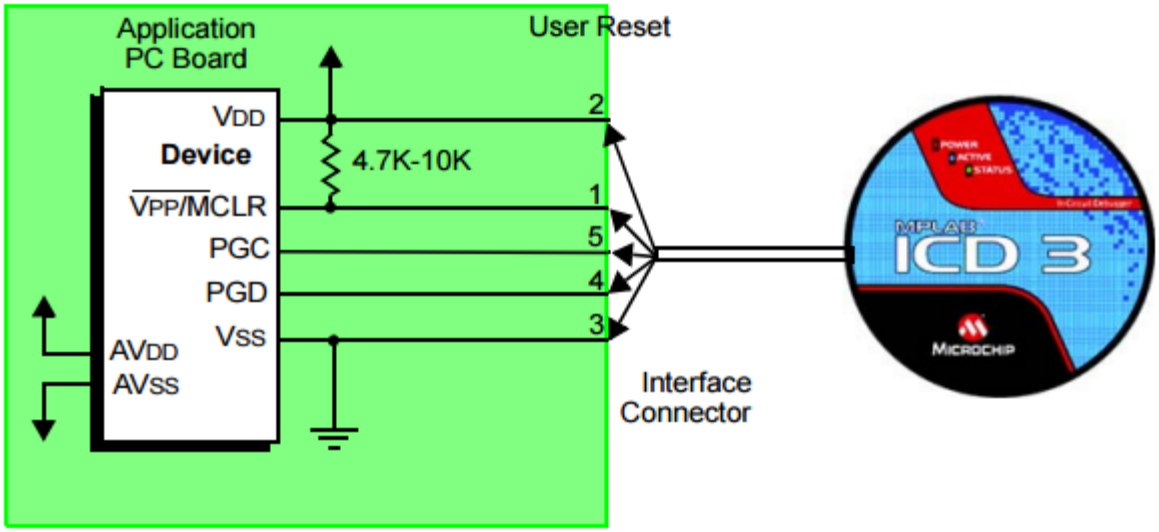


Figure 3.12 ICD3 Standard Connection Target Circuitry [37]

3.3 Sensor and Equivalent Circuit Analog

As mentioned in Section 2.2.6 Equivalent Circuit Analogs are the representations of the real world electrochemical cells. The choice of the equivalent circuit model is critical to understand the characteristics of the electrochemical cells under investigation. Based on the literature survey, the most common choice of equivalent circuit model is dependent on the type of material to be

characterized and also the type of process being used. It is difficult to model an equivalent circuit for a particular electrochemical cell as it is likely to be unique to the sample under test. Computer algorithms are now available that can assign an electrical equivalent circuit to almost any impedance data given to the computer. For this research work, the Randles Cell shown in Figure 2.9 is used with different values of resistors and capacitors to validate the system design and performance analysis.

3.4 Signal Generation Module

As mentioned earlier in section 2.2.1, EIS is usually measured by applying a sinusoidal potential to an electrochemical cell and measuring the current response. The impedance spectrum is obtained by sweeping the input signal frequency within a designated range. It can be established that the sweeping sine wave synthesizer is one of the key blocks in the process of EIS. There are many sine wave generators found in instruments and chips. Some of the more comment are listed below.

- Non-linear circuit based sine wave generators that generate the sine waves by using the nonlinear characteristics of transistors. However, the accuracy of these sine wave generators is poor and the signals generated may have many harmonics.
- Gm-C oscillator based signal generator that works by tuning a gm-C circuit. Drawbacks for this approach included, limited output frequency and inaccuracy of frequency control. Additionally, the output frequency range is typically too high for biomedical and electrochemical applications.
- Square wave filtering sine wave generator
- Digital-to-Analog Converter based sine wave generation

- Pulse Width Modulation based sine wave generation or Digital Design Synthesis (DDS)

In this research, the main aim is to develop a small form factor EIS system. This requires the elimination of extra hardware on the platform. Since, the main device for control is a powerful dsPIC that is a digital signal processor with operating frequency of 40MIPS, attempts are made to achieve the best possible sine wave synthesizer with sweep using just the dsPIC and filters. Three approaches have been tried as mentioned below and the one with which the maximum frequency range is achieved is used for conducting all experiments. The three approaches are:

3.4.1 Square Wave Filtering

One of the many ways to generate sine wave is to pass a square wave through a low-pass filter. This causes the high-order harmonics to get filtered, leaving only the fundamental. This is done by using the MAX292 from MAXIM, an 8th-order Bessel low-pass switched capacitor filter. As per the datasheet, a sine wave can be generated by passing a square wave and a 1:64 input-signal/clock ratio. The dsPIC is used to generate the square wave and clock signals. The frequency

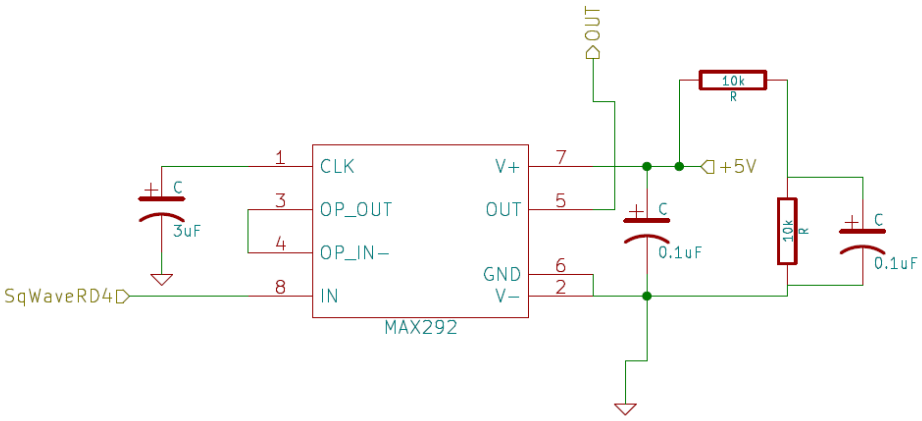


Figure 3.13 MAX292 Filters connections with the dsPIC

of the square wave is controlled in software by the microcontroller and it changes from one frequency to another frequency with delay. This operation continues for a frequency sweep and the square waves are then passed through the MAX292 filter which eliminates the higher order harmonics and leaves the sine wave at the fundamental frequency. The connections of the microcontroller with the MAX292 8^{th}-order filter are shown in Figure 3.13. The dsPIC has an 8 MHz oscillator that gives 80MHz oscillator frequency in PLL and the useful frequency range that can be easily generated by this circuit is between 25 Hz and 25 kHz.

3.4.2 Pulse Width Modulation (PWM)

This technique is also called Direct Digital Synthesis (DDS) and is simply a PWM signal generated over a whole sine period passed through a low pass filter. The dsPIC33F has an Output Compare module discussed in section 3.2.4 that is used to generate PWM signals. A corresponding low pass filter is then used and an analog voltage is obtained at the output that is proportional to the duty cycle and is given by the following equation

$$Vout = Vhigh * Dutycycle \tag{28}$$

where Vhigh is voltage for logic HIGH for PWM pulse; in this case it is 3.3V.

When the duty cycle is changed i.e., the TON time of PWM signal in sine fashion, a sine wave is obtained at the filter output. This is done by dividing the waveform into certain number of divisions. The PWM cycle time is then set up for all the divisions and the timer for which the PWM is set up, called the TON time or the duty cycle time is used to understand the amplitude of the waveform. This amplitude is determined in this application using an open source software that generates sine amplitude tables.

For example, if the sinewave is divided into divisions, a PWM pulse with 0% duty cycle will obtain the minimum amplitude and the on with 100% duty cycle will obtain the maximum amplitude (3.3V). Since the minimum voltage on the dsPIC33F is 0V and the maximum is 3.3V, the sine wave will also vary between 0V and 3.3V. It is known that s sine wave completes one cycle in 360 degrees, therefore it is required to increase the number of steps of sine wave with respect to the angle. This is called the Angle Step Rate or Angle Resolution. For the generation of sine waves in the software, 512 divisions are used to get a better resolution. Resolution is defined as the minimum increment that is required to increase or decrease the PWM TON time, i.e., Duty Cycle. The maximum number of PWM counter ticks is given by the following equation-

$$MAX\ Number\ of\ PWM\ counter\ Ticks = \frac{PWM\ period}{Resolution} \tag{29}$$

In the dsPIC the OC compare module using a timer interrupt is used to generate the PWM signals. The interrupt service routine is executed each time the Timer overflows and in the routine, the sine look up table generated earlier is read. The PWM period is specified by writing to the PR, period register of the timer and can be calculated using the following equation-

$$PWM\ period = [(PRy) + 1] * TCY * Time\ Prescame\ Value \tag{30}$$

and the maximum PWM resolution bits can be calculated using

$$Max\ PWM\ Resolution(bits) = \frac{\log_{10}(\frac{FCY}{FPWM})}{\log_{10} 2} bits \tag{31}$$

A low pass filter (LPF) is needed which is used as a Digital to Analog Converter for converting PWM into sine wave. This LPF blocks the high frequency PWM signal and lets the encoded low

frequency sinusoidal waves to pass. In order to design this filter, the Cut-Off frequency or the corner frequency is to be decided. Two simple low pass RC filter with a cut off frequency of 200Hz and 2kHz is designed using the following equation

$$Fc = \frac{1}{2 * \pi * R * C} Hz \quad (32)$$

Here the Time Constant T_C = R*C

The design tradeoff for this method is that the filter frequency must be chosen high enough to not alter the analog signal of interest. The step-size difference between the analog levels is dependent on the resolution of the PWM.

3.4.3 Digital-to-Analog Converter (DAC)

One of the other simple ways to generate a sine wave is to use a sine table with discrete values and pass it to a DAC to generate a waveform. The disadvantage of this technique is that it uses more storage memory than other sine wave generation techniques, but is far simpler more efficient as compared to the time and processing that other techniques employ. This technique also requires the use of very simple filtering as the unwanted harmonics are many times the sine frequency and need to be eliminated. A two pole or a single pole filter is high enough to generating clean sine waves. Since the dsPIC33F does not have an onboard DAC, a 14-bit DAC AD7840 that is commercially available from Analog Devices has been used. It has the following features:

- Bipolar analog output of ±3V
- Parallel and serial interface capabilities
- Fast interface in parallel mode with a data setup time of 21ns
- Low signal to noise ratio

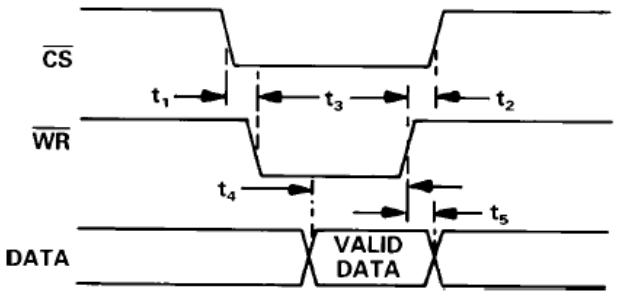


Figure 3.14 DAC Parallel Mode Timing Diagram [42]

- Double buffering interface. It has a 14-bit input latch and a 14-bit DAC latch. Data is first loaded onto the input latch and then transferred to DAC latch under the control of $\overline{LDAC}$ signal.

For the generation of sine wave the DAC is operated in parallel mode as it has a faster interface as compared to serial mode. In parallel mode the 14-bit input data appears on the data lines RD13 to RD0. Two signal CS and WR control the loading of the data on the input latch as it appears. These signals are triggered to level when both the signals are low and the input latches i.e., the input data is loaded onto the input latch. The DAC is triggered at the level and also controlled by LDAC [42].

To avoid the problem of both latches becoming transparent at the same time, LDAC is hardwired to ground. When LDAC is hardwired to ground DAC latches when CS and WR are high and input latch is transparent when CS and WR are low. Figure 3.14, shows the timing diagram for the procedure discussed above. The circuit connections for AD7840 DAC are shown in Figure 3.15. The output voltage in terms of the 14-bit input can be calculated using the given equation

$$Vout = \frac{2 * N * REFIN}{16384};\ -8192 \leq N \leq +8191 \tag{33}$$

where N is the 14-bit value.

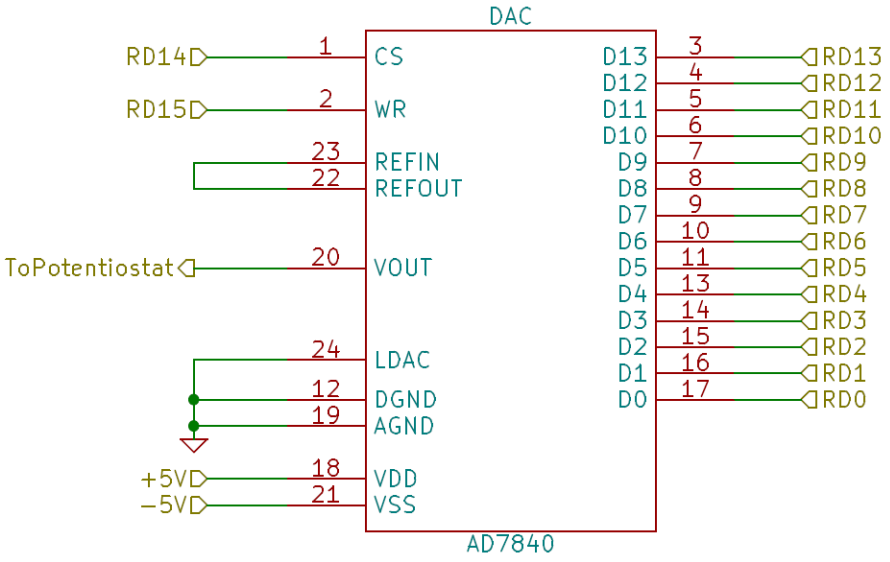


Figure 3.15 Figure showing DAC connections to the microcontroller

3.4.2 Low Pass Filter

Two passive low pass filter is used to reject the high frequency harmonics of the PWM signal. It is a first order filter and the characteristics are as shown in the table. The continuos-time domain transfer function for a first order filter is given by the equation

$$\frac{Vout(s)}{Vin(s)} = \frac{1}{\tau s + 1} \tag{34}$$

Where the time constant τ is in units of seconds. The filter bandwidth is then given by the equation

$$BW = \frac{1}{\tau}({}^{rad}/_{s}) \tag{35}$$

A passive first order low pass filter is construed using a single resistor and capacitor and is shown in Figure 3.16.

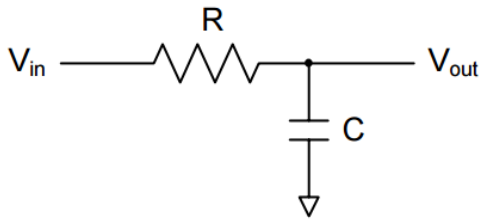


Figure 3.16 First Order Active Low Pass Filter circuit

The time constant τ is given as equal to RC and the filter bandwidth is BW = 1/RC (rad/s). The passive RC filter offers the advantages of simplicity and cost. However, the stop-band roll off rate is a sluggish 20dB/decade, giving the first order filters less than desirable performance in the PWM/DAC application. The other solution is to use active filters as they avoid the impedance loading issues suffered by passive filters. However, with active filters, one must also consider the gain bandwidth of the op-amps used. The input signal components with frequencies above the gain bandwidth will be attenuated since the op-amp will not have the ability to handle such frequencies. Keeping all this in mind, the simple and easy solution to obtaining a sine wave is chosen which is the passive low pass filter and the results obtained are favorably suitable for the application.

Table 2 Low Pass Filter Component Values Used

Filter	Component Values	Cut-Off frequency
Low Frequency Band Filter	R = 110Ω, C = 10µF	144 Hz
High Frequency Band Filter	R = 620Ω, C = 0.1µF	2567 Hz

3.5 Analog Interface Module

The analog interface circuit holds all circuitry that is required to interface the three-electrode sensor or equivalent circuit with the rest of the hardware. It mainly consists of a potentiometer, the main function of which is to maintain a constant voltage difference between the reference electrode and working electrode. A basic potentiometer consists of a voltage divider and differential amplifier circuits that impose the sinusoidal signal generated from the microcontroller on to the cell. The analog interface circuit also provides circuitry to measure the anodic current at the working electrode.

The basic requirement of the cell is that the input voltage should be applied in such a way that it does not change the potential at the reference electrode. An operational amplifier connected with large impedance is used to accomplish this. The amplifier is connected to a virtual ground to collect the current from the working electrode. A transimpedance amplifier then converts the current into a voltage. The output voltage is then fed into a level shifter that shifts the output of the current-to-voltage converter by a certain voltage. This is necessary to insure that the output voltage is compatible with the ADC on the microcontroller that can measure only positive voltages. The output of the level shifter is then filtered through an anti-aliasing filter before sending it to the ADC for digitization and processing.

3.5.1 Building blocks of Analog Interface Module

The analog interface module performs the tasks described above and in order to achieve these goals, the module is divided into smaller blocks

1. Voltage divider circuit which is responsible to control the potential of the sinusoidal input to be in the order of 50-100mV.

2. A control amplifier, for a three electrode system which is responsible to control the difference between the two electrodes of the cell
3. Transimpedance amplifier that is responsible to measure the current from the working electrode while maintaining the working electrode at virtual ground.
4. Level Shifter that shifts the voltage above zero volts compatible for ADC input.

3.5.2 Voltage divider

The voltage divider is a very simple resistor divider network that is used to divide the voltage to milli volts range before it is applied to the electrochemical cell. For biological applications, the amplitude of the sinusoidal wave is in the range of 5-100 mV.

3.5.3 Control Amplifier

This amplifier is used only for a three electrode set-up. Its purpose is to ensure that the cell potential V_{cell} tracks the applied sinusoidal potential without allowing any current to flow through the reference electrode (RE).

$$Vcell = -V_{RE} \tag{36}$$

Due to the electrochemical reactions taking place in the cell, the voltage is subject to change.

The operational amplifier forms a feedback system that controls the potential of the electrochemical cell. In general, operational amplifiers maintain both their terminals at the same voltage. The voltage has to be equal, if it is not, the output of op-amp changes until potential becomes equal.

3.5.4 Transimpedance Amplifier (TIA)

The process of EIS requires the application of a small signal voltage to the electrochemical cell and the collection of the current response which when divided gives the impedance of the cell. A transimpedance amplifier is used to measure the current flow generated by the electrochemical activity in the cell when a low amplitude voltage is applied to the cell. The basic circuit of a transimpedance amplifier is shown in Figure 3.17.

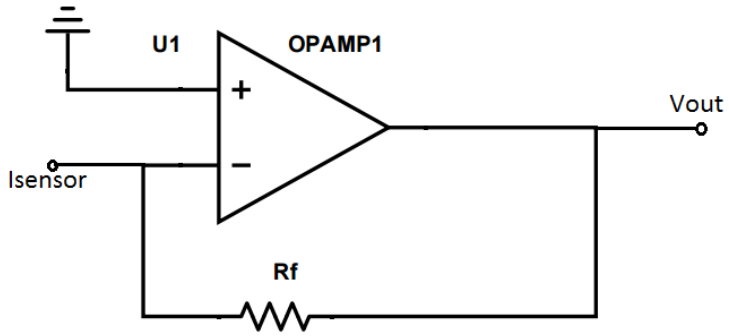


Figure 3.17 Basic circuit of transimpedance amplifier

The transimpedance amplifier is also known as a current-to-voltage converter and is implemented using an operational amplifier. The transimpedance is chosen to convert the current response to voltage input for the microcontroller because it can also be used to amplify the very small current signal that is in the order of uA obtained from the cell. The electrochemical cell and the equivalent circuits are assumed to have linear behavior when very small potential is applied to it and transimpedance amplifiers are mostly used to convert current responses that are more linear. For the application, the simplest form of amplifier is used which just has a feedback resistor, Rf. The gain of the amplifier is set by the feedback resistor and this is connected to the inverting input of

the operational amplifier which changes the value to –Rf. The voltage at the output of the operational amplifier is given by the equation

$$Vout = -Isensor * Rf \tag{37}$$

where, I_{sensor} is the current flow from the working electrode and V_{out} is the output voltage of the operational amplifier.

3.5.5 Level Shifter

The voltage that corresponds to the current from the working electrode needs to be digitized and processed to calculate the impedance. This is done in the ADC module of the dsPIC as discussed in section 3.2.9. The 10-bit ADC on the dsPIC33F can measure only positive voltages between 0V and 3.3V. A level shifter has been incorporated using an operational amplifier that shifts up the output of the transimpedance amplifier by 1.5V. The output of the level shifter is then connected to the ADC for digitization. The software then converts the measured voltage back to its current and the corresponding value is divided by input voltage to calculate impedance. Figure 3.18, shows the level shifter configuration.

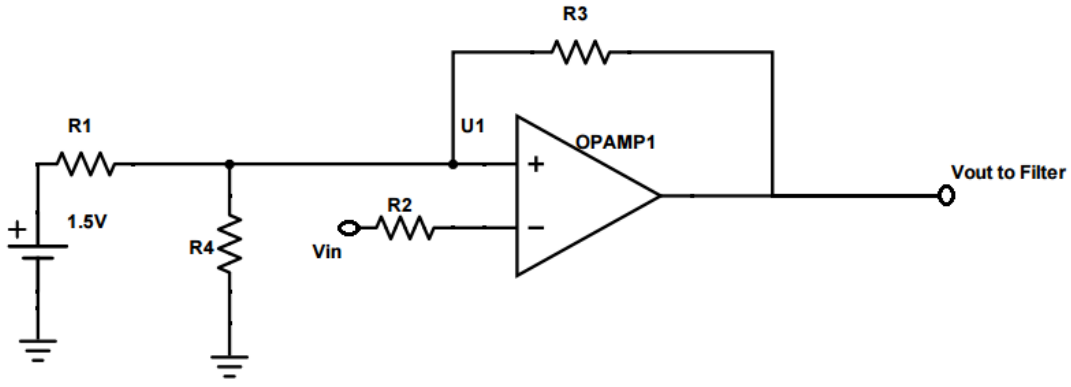


Figure 3.18 Level Shifter

3.5.6 Operational Amplifier TLE2064

The TLE2064 low power- JFET-input operational amplifier from Texas Instruments is used to build the analog interface circuitry. The chip has four operational amplifiers and features a high-output-drive circuit capable of driving 100-Ω loads at supplies as low as ±5V. Because of extremely high input impedance and resulting low bias current requirements, the TLE2064 is well suited for low-level signal processing. One operational amplifier is used to build the transimpedance amplifier that converts the current response to voltage. Since this voltage response is negative for some frequencies and out of phase, a level shifter using the second operational amplifier is built to shift the voltage to above 0V to be able to be read by the ADC and to bring the

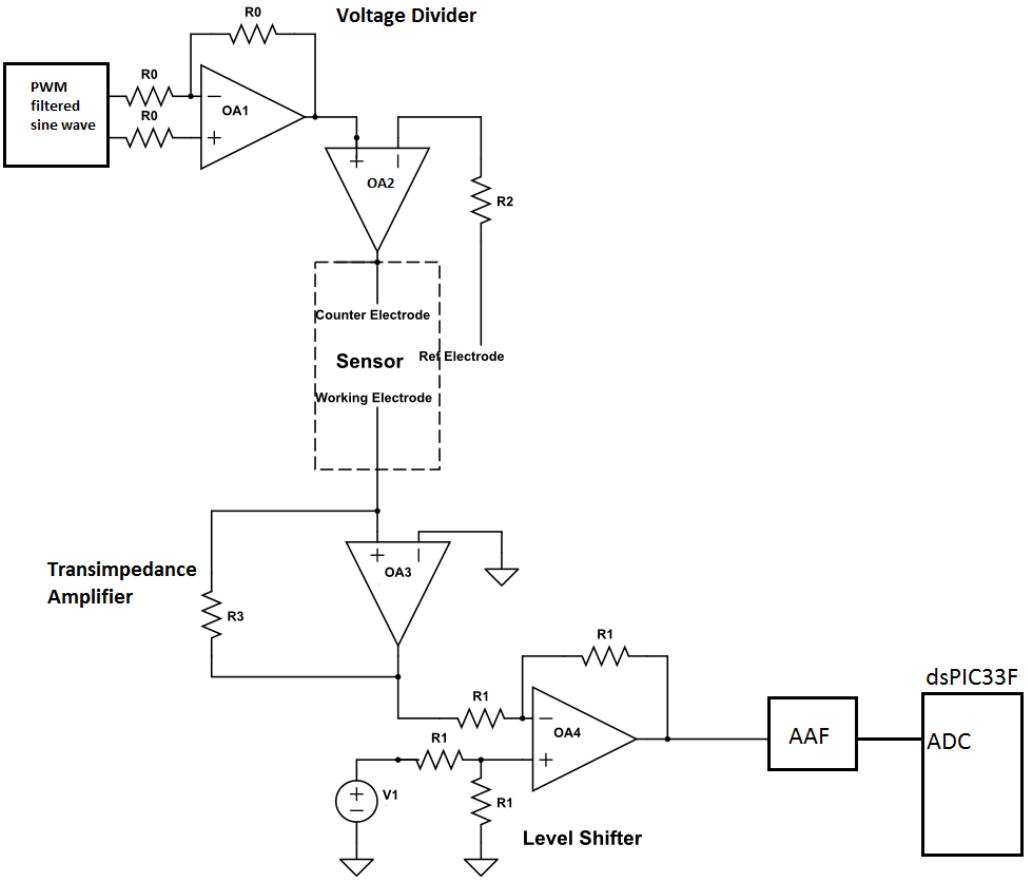


Figure 3.19 Analog Interface Circuit

voltage response in phase with respect to the input. The third operational amplifier on the chip is used to build an active anti-aliasing first order filter to which the voltage output from the level shifter is given as input. This output of this filter is then applied to the analog input of the microcontroller for digitization. A block diagram of the analog impedance circuit shown in Figure 3.19. Figure 3.20 provides package level circuit diagram showing the usage of the four amplifiers on the chip to build the different blocks of analog interface circuitry.

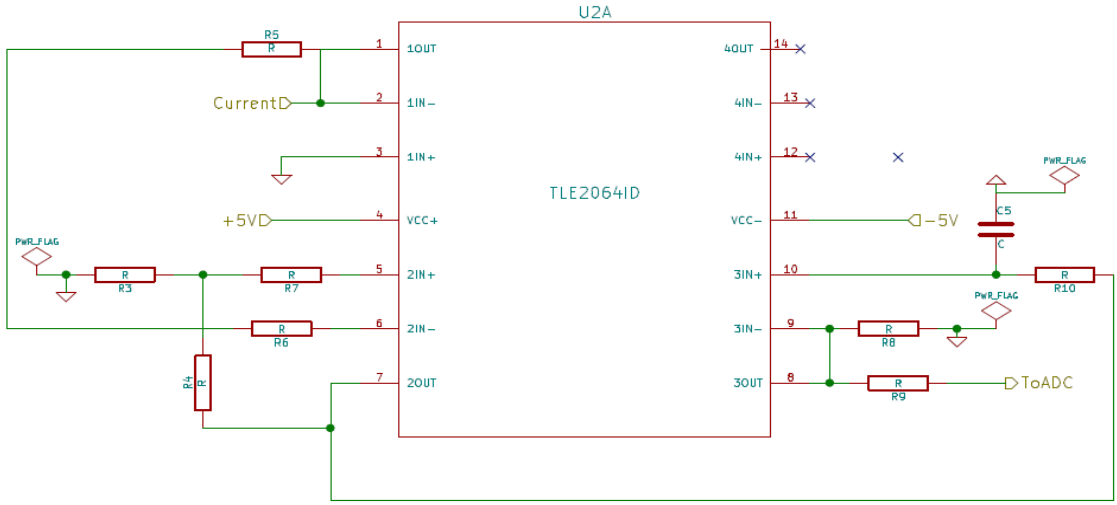


Figure 3.20 Analog Interface built using the operational amplifier

3.6 Signal Processing Module

3.6.1 Anti-Aliasing Filter (AAF)

In order to eliminate noise and high frequency interference from the sampled signal, an anti-aliasing filter (AAF) is implemented as shown in Figure 3.21,

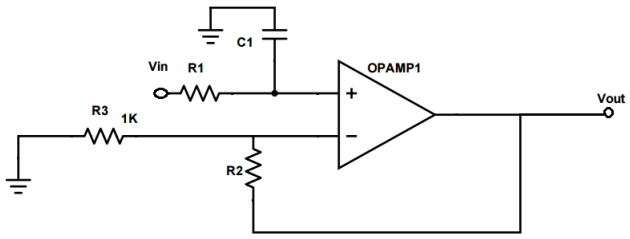


Figure 3.21 Anti-aliasing filter circuit

According to the Nyquist sampling theorem the sampling rate is required to be set to at least twice the maximum frequency component of the signal that is being sampled. Interference, noise, stray signals may have frequencies higher than the Nyquist frequency and can be picked up by the ADC. These frequencies can then interfere or alias with the required frequency range and sample data wrongly. In order to avoid this, a low pass filter is added before the ADC and the sampler. This filter is recognized as an anti-alias filter because it attenuates the higher frequencies and prevents the interfered or aliasing components from being sampled by the ADC. At this stage, the anti-aliasing filter is an analog filter because the signal is still analog.

An ideal anti-pass filter allows all the good input frequencies to pass and cuts off all the underside frequencies. However, such a filter is not totally realizable. An illustration of the filters is shown below in Figure 3.22.

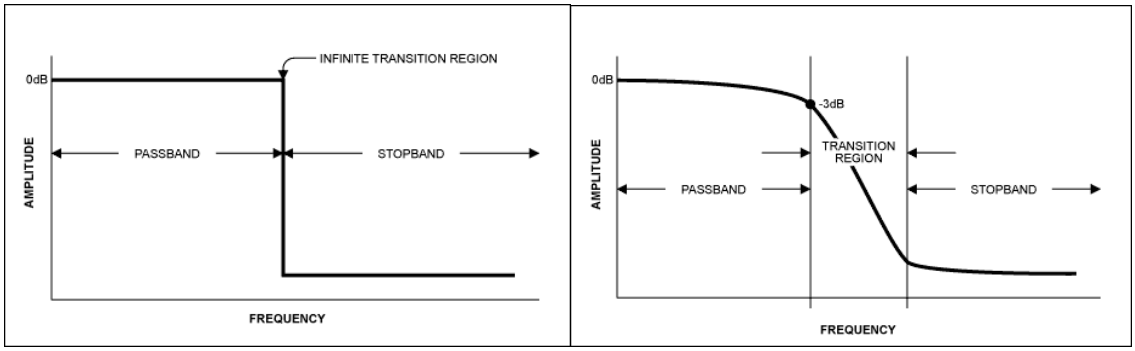


Figure 3.22 Ideal and Practical Anti-alias Filter [43]

One is an ideal filter that passes all frequencies below the frequency of interest and cut-off all frequencies above it. The region where the signal is allowed to pass is known as transition band. Although, it is assumed that passing of signals with frequencies less that frequency of interest is required, some signals in the transition band can also cause interference. Therefore, it is a rule when sampling that the sampling frequency should be greater than two times the highest frequency in the allowable band.

For example, it is required to sample a component of 20 kHz. The Nyquist theorem states a required sampling frequency of 40 kHz. The anti-aliasing has a cut-off frequency of 20 kHz, but since this is not an ideal filter usually the sampling frequency selected goes from 44 kHz to 96 kHz, which allows a transition band of at least 2 kHz. For this application, the highest frequency that is sampled is 20 kHz, therefore, the cut off frequency of the anti-aliasing filter is 20 kHz while, the sampling frequency is never less than 44 kHz.

3.6.2 Peak Detection

The system is required to detect the peak of the response from the electrochemical cell. This is easily done in the microcontroller. The requirements to be able to calculate the peak of a sine wave easily is that the sine wave should be sampled properly and at least a complete period is to be sampled in the ADC. Since, the sampling frequency of the ADC is quite high, there are enough sine wave samples to be able to calculate the peak of the sine waves. Also, since the sine wave is offset to above 0V with the use of a potentiometer, there is no need to bother about the negative detection. Therefore, only the maximum and minimum voltages (in this case 0V) is to be subtracted to determine the peak-to-peak voltage of the sine waves. Two variables are used to perform this

```
Function peakDetection( )
      max ← 0
      min ← 0
      peakValue ← 0

      for each ADCBufferValue in ADC_DMABuffer
            if waveAmplitudeValue > max then
            max ← waveAmplitudeValue
            end

            if waveAmplitudeValue < min then
                  min ← waveAmplitudeValue
            end

      end

      peakValue ← max – min
      return peakValue

      end
```

Table 3 Pseudo-code for peak detection using which the peak-to-peak voltage of input reference and output response is calculated

calculation. Each sample in the ADC DMA buffer is compared with the last sample. If it is higher than the last sample, its value is stored in a variable that holds the highest variable till now and the same is done to determine the smallest sample that is stored in a second variable. Finally, the two samples are subtracted to determine the peak-to-peak voltage.

3.6.3 Phase Detection

As it has been shown in section 2.2.1, the excitation signal is given by $E_t = E_0 \sin(\omega t)$ and the response current is given by the equation $I = I_0 \sin(\omega t + \emptyset)$. Therefore, the complex impedance can be calculated as

$$Z = \frac{E_t}{I_t} = \frac{E_0 \sin(\omega t)}{I_0 \sin(\omega t + \emptyset)} = Z_0 \frac{\sin(\omega t)}{\sin(\omega t + \emptyset)} \quad (385)$$

There are a few ways to calculate the phase difference between two sinusoidal signals using a microcontroller. The phase difference between two sinusoidal waves is usually calculated by evaluating the time when the signals cross zeros to get the time delay, also known as zero crossing evaluation. Most microcontrollers have hardware that allows a timer to run based on some internal or external trigger. If the timer is allowed to turn on when the first signal crosses the zero and to stop when the second signal crosses the zero time, the difference between the timer's on and off

time gives the time between the zero crossings. The difference between the zero crossings of the signals gives the period. The phase shift in units of time is then just the time difference between the two signals divided by the period of the signa. The dsPIC has an Input Capture module based on timers that can be used to capture the signal's zero crossings. However, since in this research work, an ADC is already employed in order to calculate the amplitude and the data is transmitted to the terminal via UART, the phase difference is calculated without using capture timers.

In this work, the sine wave has been generated between 0V-3.3V by adding the other half of the wave as offset. This helps in the response being captured by the ADC since it accepts only values about 0V. Therefore, the above mentioned method has been applied and time difference between the two peaks of the waves or the two smallest samples between the waves is calculated. This can be done both off the chip and on the chip. The off-chip processing is done after the data has been captured by the UART. If the sampling frequency of the ADC is known, the samples can be converted into time and the difference between the two zeros be calculated. If the time delay is t, and the period of the sine wave is T, then

$$\frac{t}{T} = \frac{\emptyset}{360} \tag{39}$$

The phase 'Ø' is in degrees. The way to determine the lag and lead in the phase, if 't' is negative, the output lags the input and if it is positive, the output leads the input. This program is repeated for every frequency and algorithmically, this method is tougher.

Other methods to calculate the phase difference are

- By using Fast Fourier Transform (FFT): This method is based on the same concept of finding the zero crossings and calculating the time delay. But in this method, the time delay between the input and the output can be calculated by using a cross correlation of the input and output signal. An auto-correlation between the signals can yield the frequency that in turn can output the time period, T. These values can be plugged in the same Equation 35 to determine the phase difference.
- If the sine waves are of equal size, voltage and intensity, then this method can be used. The input and the output sine wave can be summed up together and the amplitude of the

resulting wave can be calculated. If the phase shift is 0 degrees then the result will be a sine wave twice the original amplitude. If the phase shift is 180 degrees then the result will be zero amplitude. The phase differences in between can be mapped to a look up table stored in the memory of the microcontroller. If the sine waves are not of equal amplitude, then this method is not the best to be used. For the EIS process, in this work, the amplitude of the input and the output of the waves change due to the modulus of the impedance and therefore, this method was not chosen.

```
Function calculatePhaseDifference (timePeriod)
      inputMinIndex ← 0  outputMinIndex ← 0
      outputStartIndex ← 0 outputEndIndex ← outputWaveValueslength-1
      outputMinValue  ← MAX_VALUE  index ← 0   j←0

      for each ADCInputValue in ADCInBuffer
            if inputWaveValues[inputMinIndex]>inputWaveValues[index]
      then
                  index ← index+1
      end
      if inputMinIndex-timePeriod>0 then
            outputStartIndex = inputMinIndex-timePeriod;
      end
      if inputMinIndex+timePeriod<outputEndIndex then
            outputEndIndex = inputMinIndex+timePeriod
      end
      for each ADCOutputValue in ADCOutuffer
            if outputMinValue>outputWaveValues[j] then
                  inputMinIndex ← i
                  outputMinValue ← outputWaveValues[j];
                  outputMinIndex ← j;
      end
      j←j+1
      end
      end
```

Table 4 Pseudocode for Phase Calculation using which the phase difference between the input signal and the output response is calculated

3.7 Power Supply

All the peripheral devices require a positive +5V and a negative -5V supply. The positive supply is derived from the regulators LM117 with +5V and +3.3V outputs as shown in Figure 3.23.

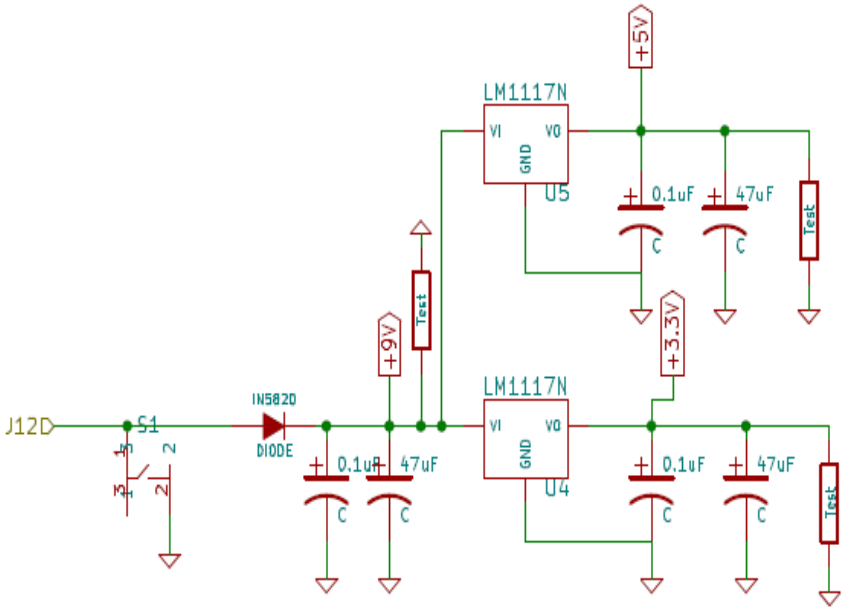


Figure 3.23 Power Supply Schematic

The negative -5V supply is devised using the positive +5V power supply and the LM7660 voltage converter from Texas Instruments. The LMC7660 is a CMOS voltage converter capable of converting a positive voltage in the range of +1.5V to +10V to the corresponding -1.5V to -10V. It uses its built-in oscillator to switch 4 power MOS switches and charge two inexpensive electrolyte capacitors. The drive circuitry consumes little power and the power switches are matched and have low resistance. The output is connected to a common power rail which supplies

negative 5V supply to other devices. Figure 3.24, shows the schematic of the LMC7660 taking positive 5V from the voltage rails as converting it to negative 5V.

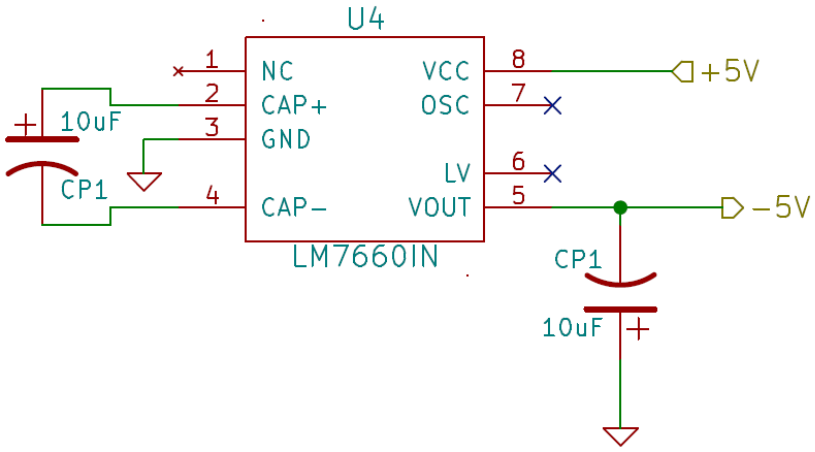


Figure 3.24 Schematic showing connections for LMC7660IN

3.8 Schematic of Circuit Board

Figure 3.25 shows a schematic circuit diagram for the board that has been designed for mounting all of the peripherals including the filters, operational amplifiers and the dsPIC. The schematic circuit of the board is shown in Appendix I. The design of a two metal layer board layout was completed using KiCAD board layout software. The dimensions of the board are 86 mm * 87 mm.

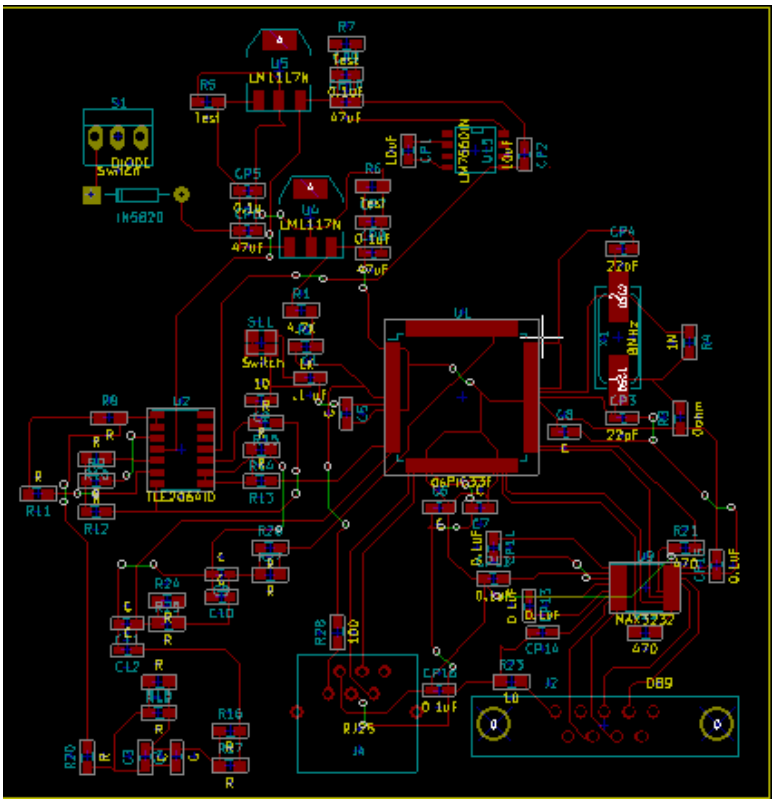


Figure 3.25 Design of the PCB layout

3.9 Integration and Working of System

The circuit schematic and and image of the fabricated board of are shown in Figure 3.25. As shown, the individual blocks are integrated to form a complete EIS system. The electrochemical cell can be placed with two electrodes as well as three electrodes. When a two electrode cell is attached, the reference electrode is tied to the counter electrode and current is measured across the circuit. The process starts with calculation of the solution resistance (R_{sol}) of the cell. This is done by passing a DC voltage across the cell and measuring the current across it. When using an equivalent circuit, the current is measured across the whole circuit.

The second step is then to measure the current across the cell by sending an analog sine wave stimulus over the specified range of frequency. This current is then converted to voltage by using a current to voltage converter (I-V). The output voltage is compared against the input voltage that is used as the reference. An algorithm in software calculates the magnitude of the impedance with respect to the reference by calculating the peak to peak voltage (V_{p-p}) of the output wave. The algorithm is able to calculate the peak-to-peak voltage over the frequency range and transfers the data via UART to a terminal. The second algorithm calculates the phase difference between the reference and the output wave. This is done by calculating the time difference between the zero crossings of the wave over an average of wave cycles. A timer is used to calculate the timer ticks of the zero crossings that are converted into time. The data is then transferred to a terminal for plotting the Nyquist and Bode plots.

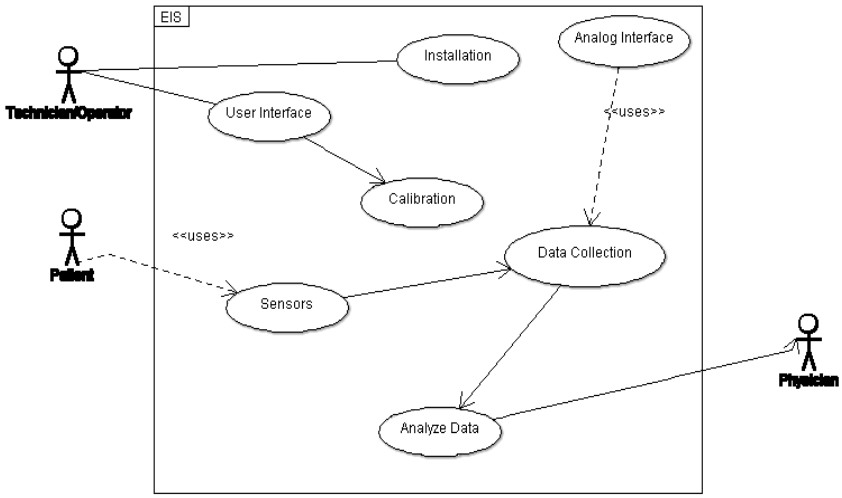


Figure 3.26 Use case diagram of the EIS system

A Use Case diagram of the system is shown in Figure 3.26. Since, the system is aimed to be used for health monitoring applications, a patient-physician setting is considered for understanding the system better. The system requires an operator who gets the system started and ready for use before the testing begins. A calibration function is included in the system design that enables calibration using a resistive circuit. Another important feature is the user interface that helps in collection of data samples into a file on the terminal.

4. Results

4.1 Experimental Setup

The experimental setup for performing EIS using the point-of-care device is shown in Figure 4.1. An electrochemical cell (Micrux Technologies) is tested with the system and the amplitude of sinusoidal stimulus is reduced to the order of millivolts for experimental purposes. The device is connected to the electrochemical cell using an EIS electrochemical cell interface and alligator clips as shown in Figure 4.1.

The performance of the circuit has been evaluated experimentally using four electrical circuits, both for low impedance and high impedance measurements. The circuit elements used in these evaluation circuits are provided in Table 5.

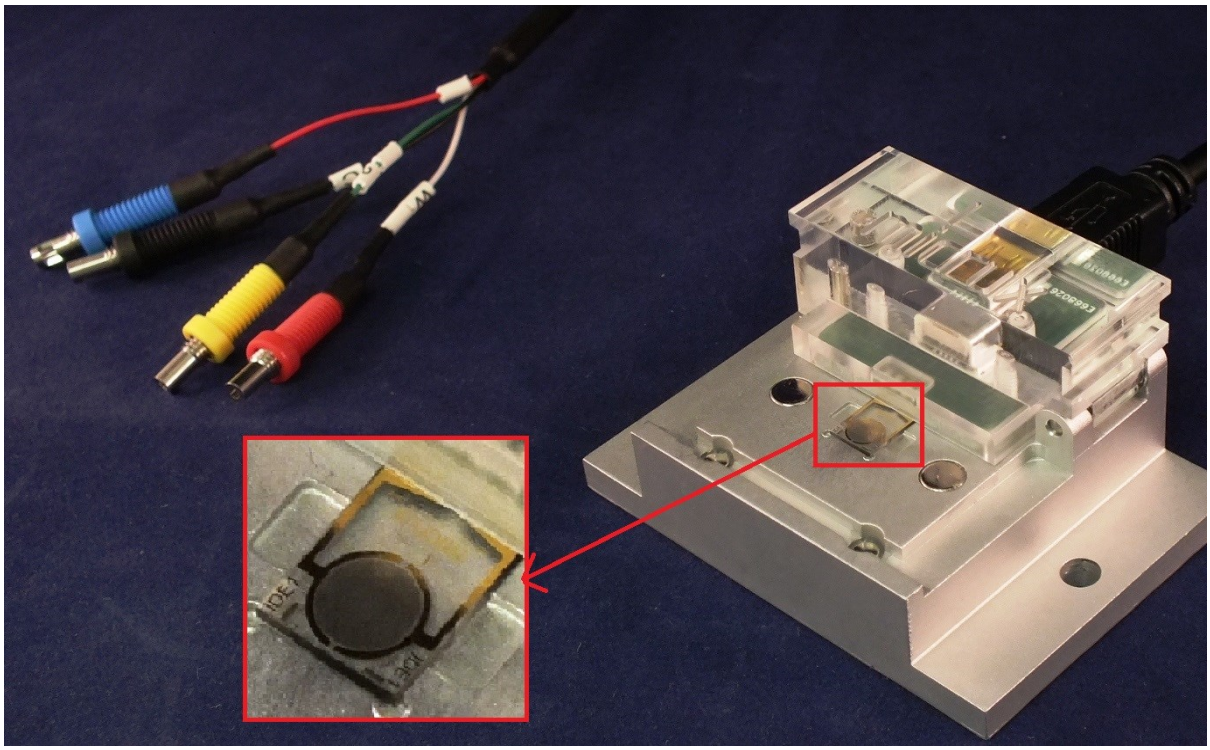


Figure 4.1 Cell Interface from Micrux holding the Interdigitated Electrodes for EIS testing

Table 5 Preliminary equivalent circuits

Rsol	Rct	Cdl
10Ω	100Ω	-
1Ω	1Ω	1 µF
10Ω	100Ω	2.2µF
100Ω	300kΩ	100 nF

The device is validated by using the Universal Dummy Cell 2 from Gamry Instruments, which includes a printed circuit board having two test cells equipped with terminals, arranged on the edges of the printed circuit board. One of the test cells is a Randle's cell, the circuit diagram of which is shown below in Figure 4.2.

Finally, the device is tested on electrochemical sensor from micrux Technologies, which is a metal-based InterDigitated Electrodes (IDE) and are fabricated by thick-film technologies on a glass substrate. The interdigitated electrodes provide a suitable tool for impedance, capacitance and conductivity measurements as well as fuel cells.

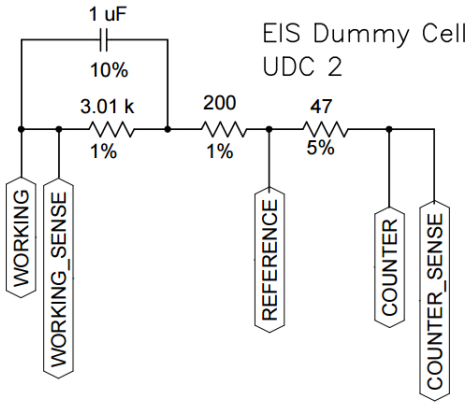


Figure 4.2 EIS Dummy Cell Schematic Diagram [39]

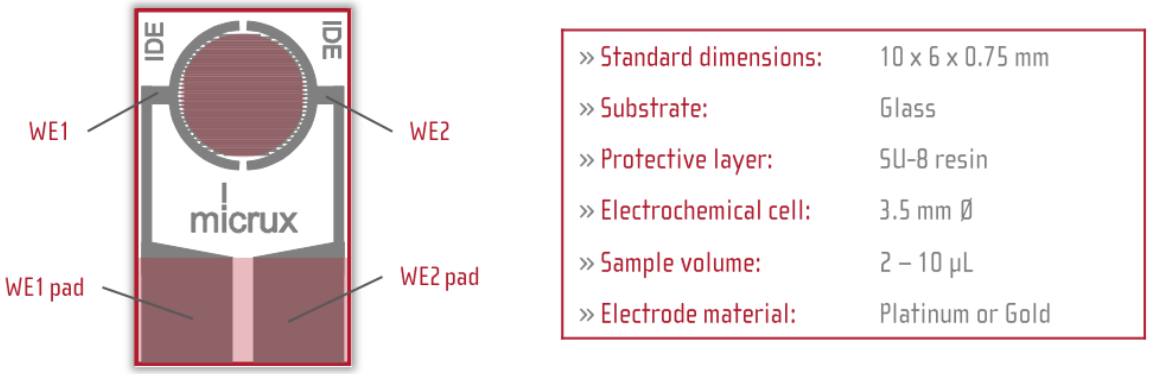


Figure 4.3 Electrochemical cell and its features [40]

A cell with the standard dimensions is shown in the Figure 4.3. For experimental testing, the cell is connected to the experimental setup shown in Figure 4.1.The above four circuits, the dummy cell and the electrochemical cell are all tested with sine and square waves. All possible environmental conditions and kept same for both the sine and square wave experiments. The results are shown in the section below.

4.2 Sine Wave Testing

4.2.1 Procedure and Observations

For the testing, two methods have been employed. One is to calculate the impedance of the system under test with individual frequencies and at each frequency calculating, the magnitude and phase of the system. When a voltage signal is applied to the system and the output current is converted into voltage, the raw data collected at the terminal by the UART and stored in a file. An example wave of 434.4 Hz is shown in the Figure 4.4. The input and output captured simultaneously is successfully converted in ADC and transmitted by UART to evaluate magnitude and phase difference.

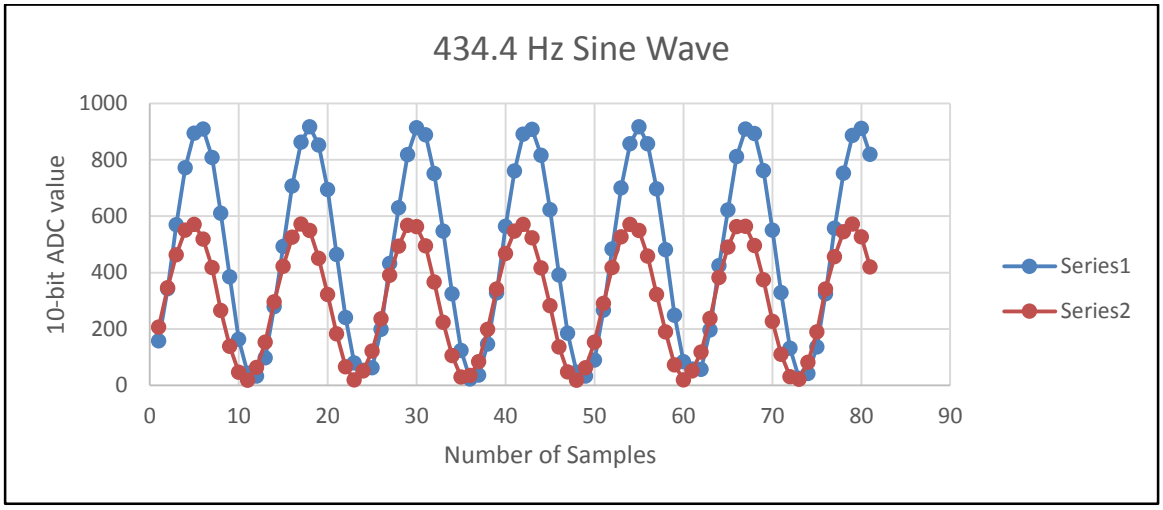


Figure 4.4 Sample of data at 434.4 Hz Sine wave in terminal

4.2.2 Results

The Figure 4.5 above shows the system being tested on a 1kΩ resistor with ±5% tolerance. The resistance measured on multimeter is 990kΩ and the graph shows the output resistance captured at different frequencies.

The results for the circuit in table 3 are shown in Figure 4.6.

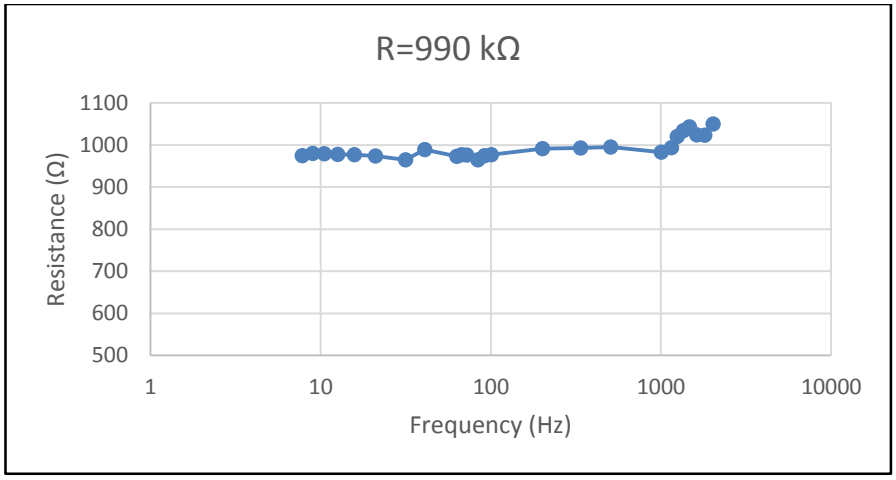


Figure 4.5 Experimental results for purely resistive circuit

The results for the EIS dummy cell are shown in Figure 4.7.

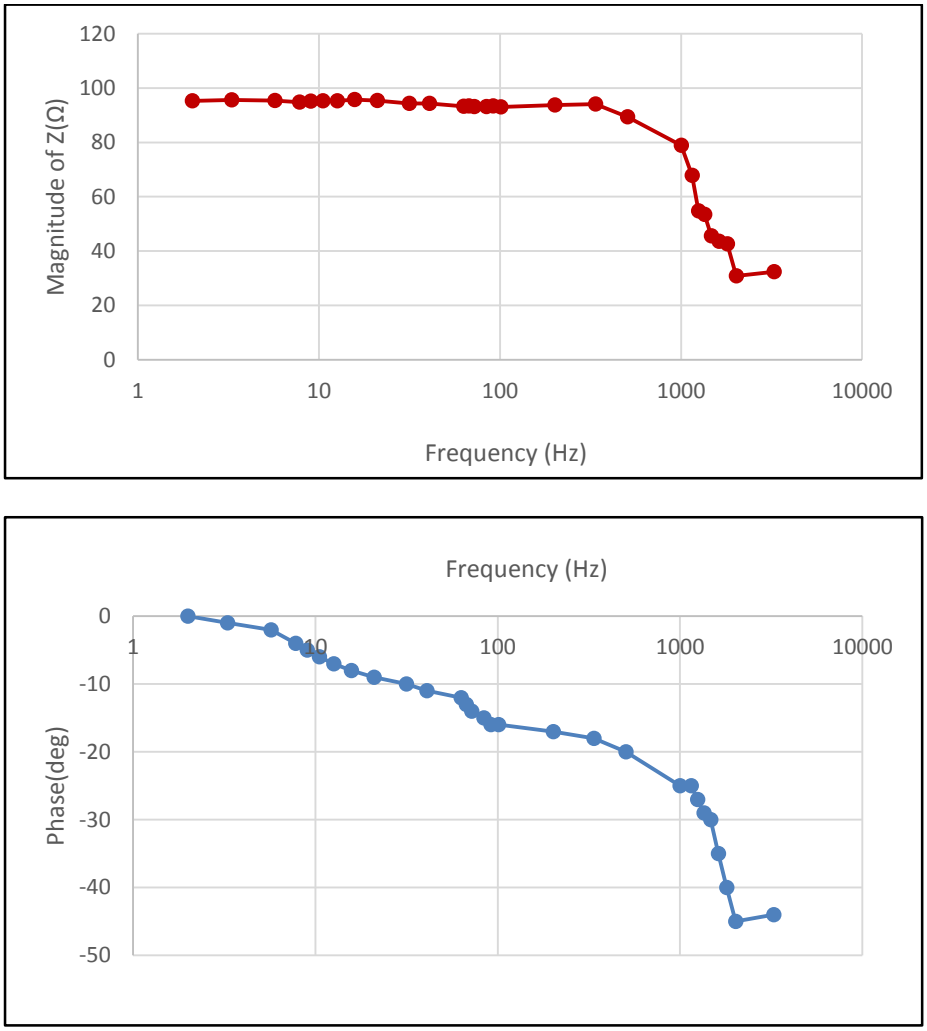


Figure 4.6 Experimental results using equivalent circuit 3 showing modulus of impedance vs frequency and phase vs frequency

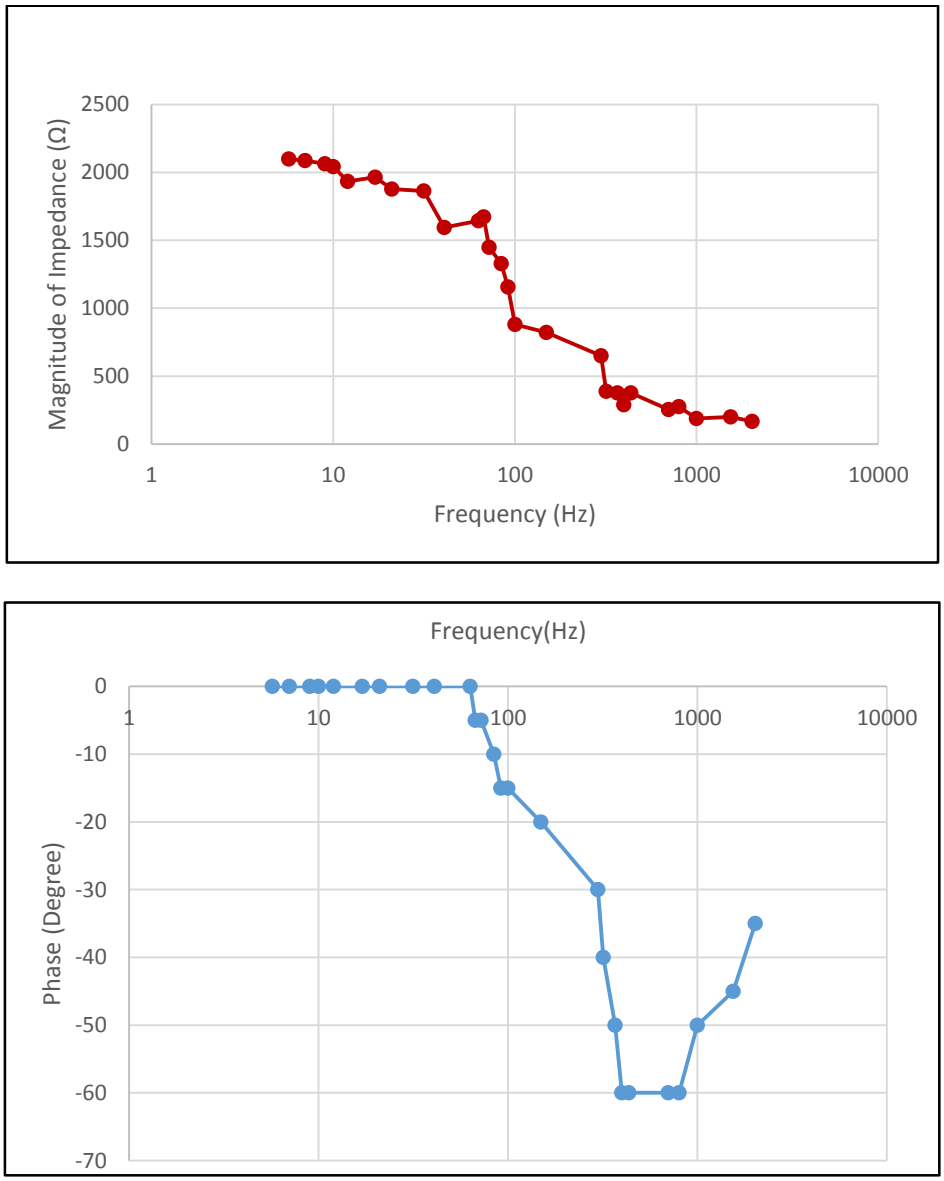


Figure 4.7 Experimental results using the EIS Dummy Cell 3 showing modulus and phase of impedance

The system is also tested using the IDE as shown in the Figure 4.3 and a buffer solution Phosphate-buffered saline (PBS) is used to cover the entire area of the IDE. PBS is a water-based salt solution containing sodium phosphate, sodium chloride and in some formulations potassium chloride and potassium phosphate. This solution is used because the osmolarity and ion concentrations of the solutions match those if the human body. The pH of the solution prepared is 7.4 and it is isotonic and non-toxic to most cells. Covering the cell with a dampened tissue reduces the evaporation process of the solution from the surface of the cell. This allows the solution to stay on the surface for more than an hour. The equivalent circuit for this cell can be estimated to a resistance and capacitance in series. This suggests that at low frequencies, the capacitor allows the current to flow across the circuit and therefore it is expected to observe a phase difference where the voltage lags the current response obtained. At very high frequencies, the capacitor does not allow any current to pass as the capacitive reactance goes to zero, i.e., the capacitor does not have time to charge up so the impedance is only the resistance R in the cell. The results for the cell are as shown in the Figure 4.8.

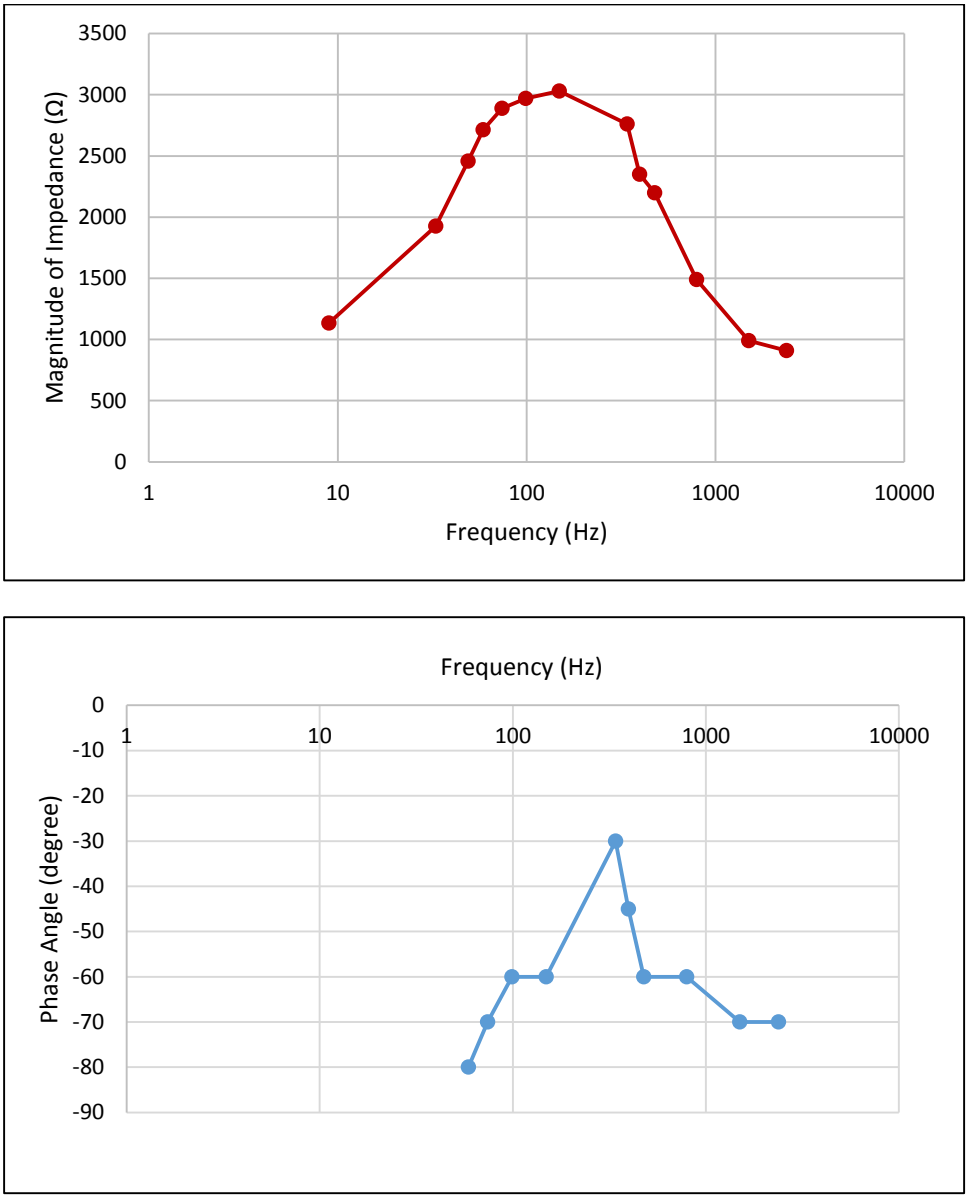


Figure 4.8 Experimental results using the Micrux Interdigitated Electrodes showing modulus and phase of impedance

4.3 Square Wave Testing

The testing of a frequency sweep of square wave yields interesting and appalling observations. A frequency sweep of square waves from 2Hz to 200 kHz is passed through the 1kΩ resistor and the EIS dummy cell. Figure 4.9 shows pictures taken from the oscilloscope as both the input and output

waveforms were being recorded at the same time. The input has been scaled to visualize the readings clearly.

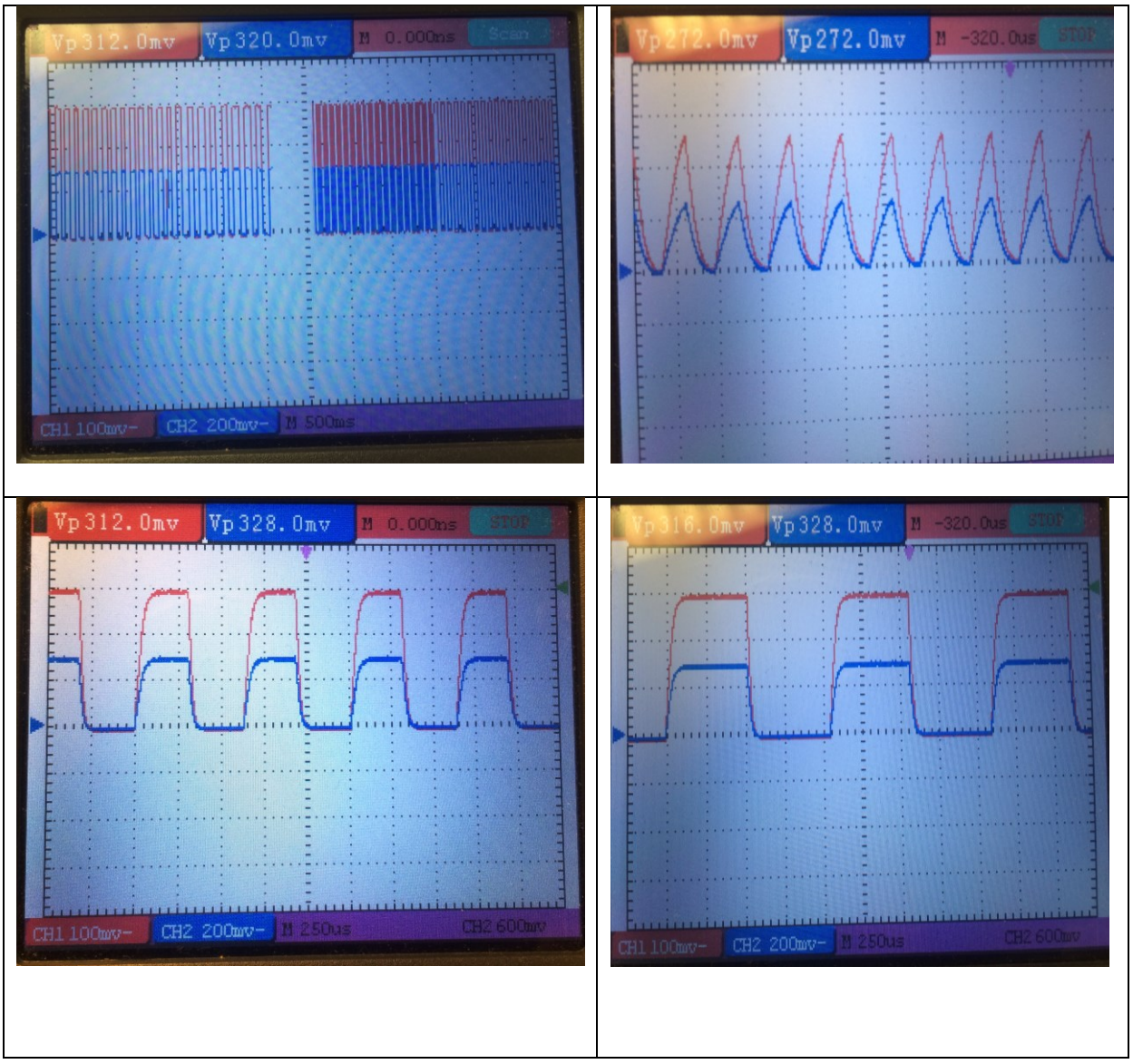


Figure 4.9: EIS technique Square Wave Observations Figure 4.9(a): Experimental Square wave input and output data at ~200 kHz Figure 4.9(b) Data at ~20 kHz Figure4.9(c) Data at ~400 Hz, Figure 4.9 (d) Data at ~100 Hz

From the observations in Figure 4.9, it can be understood that there is certain amplitude change between the input voltage and output current which is converted to voltage and then back to current in the software. The division of these quantities yield the magnitude of the impedance which is a similar procedure as that of sinusoidal EIS experimentation. However, the capacitance in the circuit is seen to be charging and discharging at the application of different frequencies. At high frequencies, the capacitor charges but due to the small time period, discharges fast. At smaller frequencies, the capacitor charges and discharges slowly and this can be attributed to the large time period. Now, it is known that the phase angle between the two components is known by

$$\emptyset = \tan^{-1}(\frac{1}{\omega RC}) \tag{40}$$

where the time constant is given by

$$\tau = \frac{1}{RC} \tag{41}$$

If the value of time constant, τ is plugged in the equation, the phase angle can be calculated at each frequency by

$$\emptyset = \tan^{-1}(\frac{1}{2\pi fRC}) \tag{42}$$

It can therefore be interpreted that when a square wave is passed through an electrochemical cell that contains both resistive and capacitive components, the phase change between the input voltage and output current is not visible to the eye and the calculation is not deemed straightforward. Therefore, it is interpreted that the information of phase change can be calculated using a different approach which is an open area of research on this sub-topic.

5. Conclusion and Future Work

5.1 Summary

This section summarizes the research work presented in the thesis on development of a micro-controller based Electrochemical Impedance Spectroscopy platform for wearable health monitoring devices. The research considers two different approaches of performing EIS and puts forward solutions to develop a small form factor based EIS device. The first approach is to use the classical way of performing an EIS on an electrochemical cell which is by applying a small amplitude sinusoidal signal sweep generated by the dsPIC and tracking the current response from the working electrode using an analog interface circuitry; the processing of which yields the characteristics of the electrochemical cell. The second approach is to use a different and easily producible square waves in place of sine waves and compare the results with respect to the classical EIS method.

In Chapter 2, the previous work on small form factor based EIS devices is discussed and the technique of EIS is explained in brief. Different approaches tried by various researchers over the period of last twenty years is brought under light and existing issues and challenges related to the development of portable EIS devices in the above scenarios are explained. Chapter 3 puts forward an EIS development system based on the dsPIC33F. It explains the salient features of the proposed system design such as signal generation using the PWM and filter thereby reducing hardware and cost, analog interface to the electrochemical cell and the signal processing module. In order to reduce the size of the system, signal generation is done using the PWM module available on the

dsPIC chip and a low pass filter. Software in the IDE allows sweep of the frequency and at each frequency the magnitude and phase is calculated in the software additionally.

Chapter 4 presents the results obtained from the application of the developed EIS system design described in Chapter 3. The results signify the reliability and efficiently of the proposed system design as it is successful in determining the characteristics of the electrochemical cell with the requirements laid down in Chapter 2.

5.2 Conclusions

This section elucidates upon the conclusions that were derived from the research work presented in the thesis. An analysis was carried out to understand the performance of the system using a sinusoidal voltage input and a square voltage input.

The proposed system design has been tested using the equivalent circuits and the electrochemical cells mentioned in Section 4.1. The results of the pure resistive circuit show that the system is able to calculate the amplitude of the sinusoidal waves to a commendable extent. This experiment can also serve as a calibration experiment for the system. The dummy cell is used next to evaluate the performance of the device and the results are pitted against the results in the manual of the dummy cell.

For square wave systems, the observations reported present a very interesting scenario. It is already known that to calculate the impedance, one needs to evaluate the magnitude and phase change of the system current in response to the input system voltage. For experimentation, square waves of

low magnitude are applied to the dummy cell in a sweep ranging from 200 kHz to 2Hz in a decreasing fashion. The time constant has to be plugged in the equation for phase angle detection, which is not a convincing method of determining the phase angle. Not much literature has been found in the way of doing EIS using square waves as input.

5.3 Discussion and future work

From the literature review of EIS and its process, it is evident that the technique is popular and powerful and efficient in predicting the behavior of electrolytes in electrochemical cells. In addition to its popularity, it has a wide range of applications from corrosion behavior to health monitoring. This system has been developed to be able to serve as an on-chip EIS device and has been designed keeping in mind the requirements and constraints. Of the many requirements, the main is to be able to reduce the size of the system yet make it reliable and efficient. It is already noted that the device is able to generate sinusoidal inputs on the chip and change the frequencies to produce the sweep. The device is also able to calculate the magnitude of the impedance correctly with less than 5% error both when the inputs are given as individual and in sweep. The system can detect phase changes between the input signal and output response and transmit it to a terminal via UART. The processing is done off chip and the results obtained are reliable as shown in Section 4.2. It is believed that the proposed algorithm for phase detection can be extended to perform on-chip processing where at each frequency there is a time delay that allows the microcontroller to calculate the magnitude and phase and transmit the output values via UART. However, in such a scenario it would be important to take care of conflicting time delays between generation of signal and the processing of signal sampled on the ADC. The proposed system design can also be

extended to a wireless system with the broadcast peripheral connected to a Bluetooth device via the UART.

In case of square wave EIS approach, an extensive research in the sub-area is to be undertaken and the phase angle determination concept is to be realized. If this is possible, with all the constraints available, this could take a lot of load off the microcontroller chip as square waves is very easy to produce using a PWM module and the sweep is easier to generate as compared to the sinusoidal sweep generation. With the use of square waves as input signals to a cell, the frequency band also increases two folds thereby extending the range of EIS. Research can also be undertaken to identify how electrochemical cells behave when supplied with a digital square wave input as opposed to analog sinusoidal input waves.

In summary, the research carried out in this thesis is, however, is a proof-of-concept of a low cost, reliable, compact Electrochemical Impedance Spectroscopy system that can be used for point-of-care applications paving a way for better, safer and reliable health care and monitoring systems to be developed in the future. Moving forward, the challenge is to innovate on this work in a manner that could greatly impact point-of-care health monitoring.

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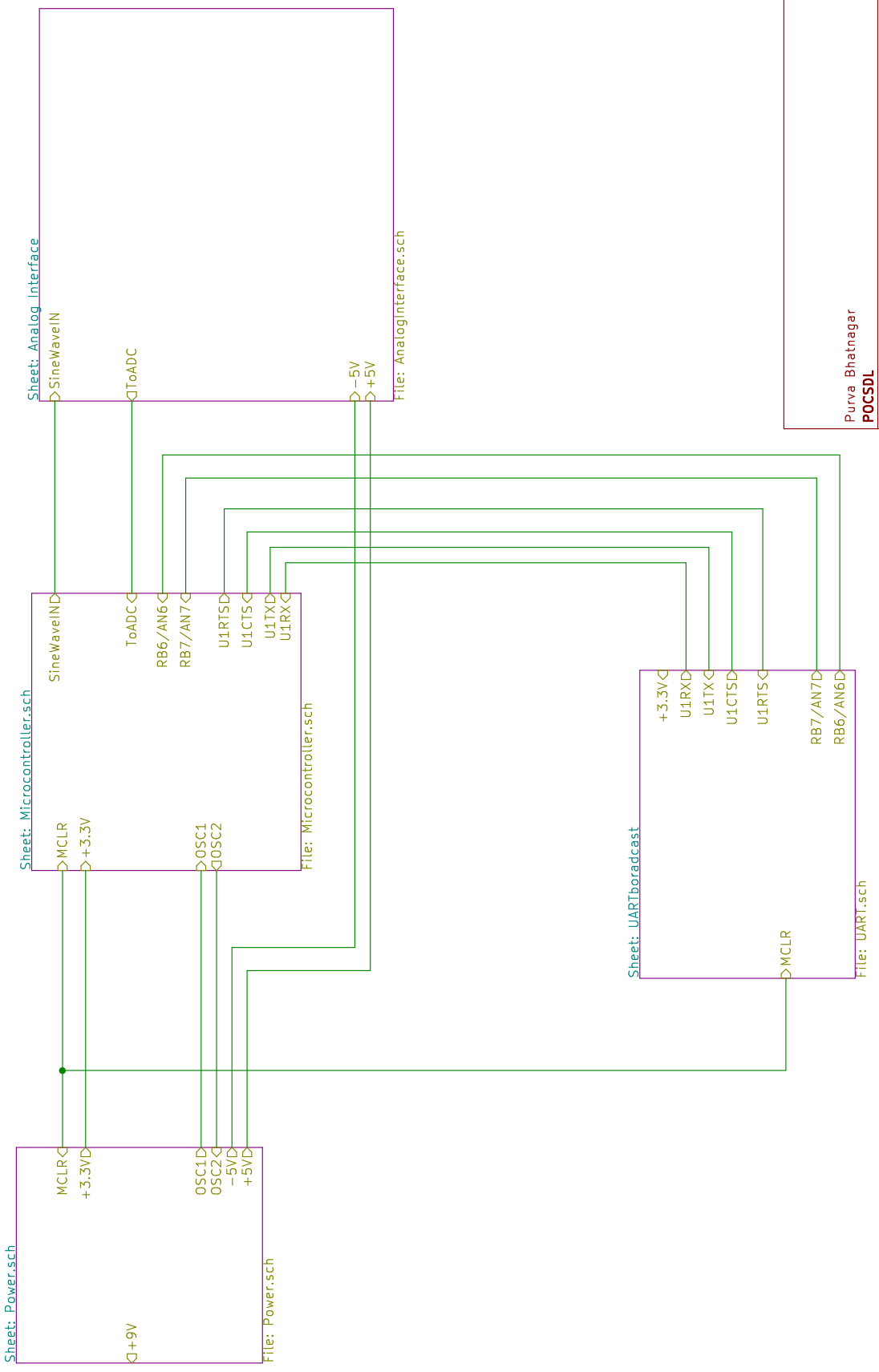
Appendix I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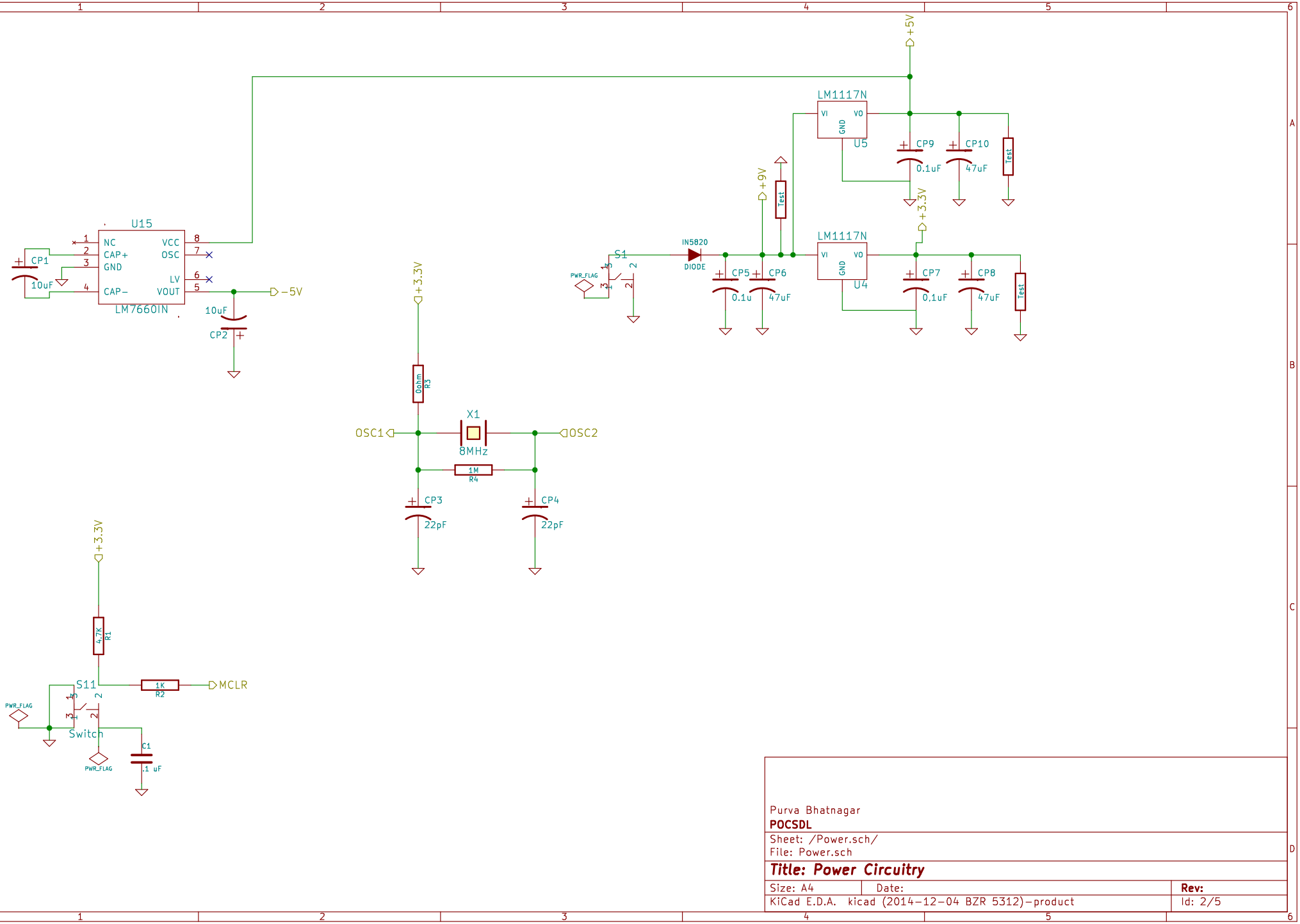

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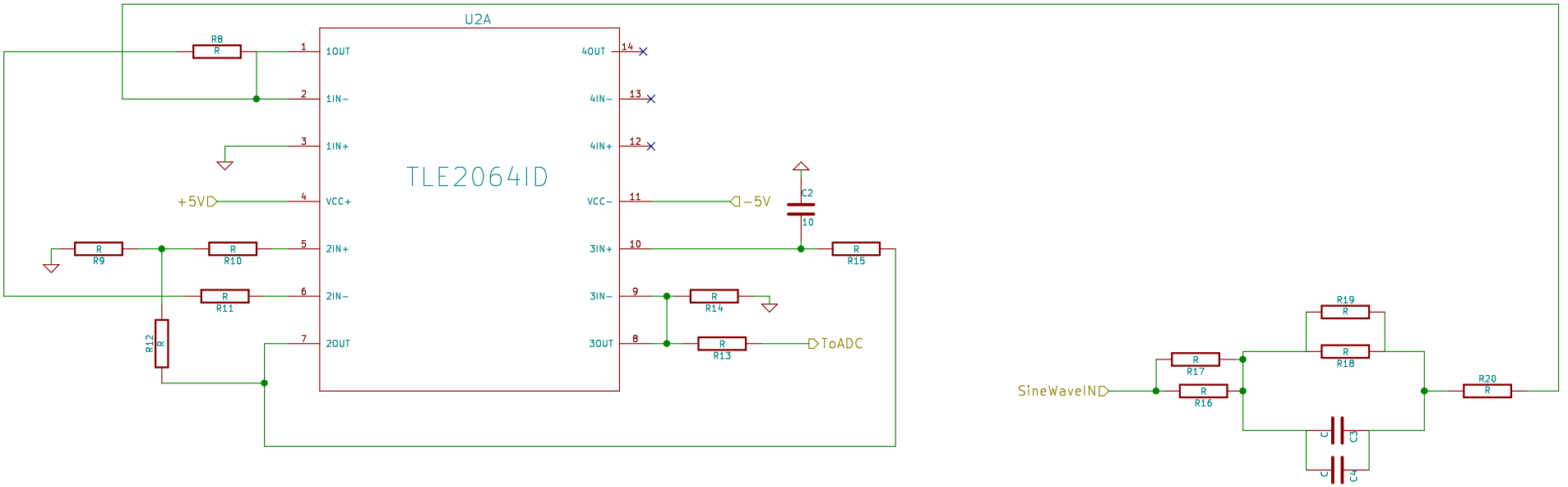

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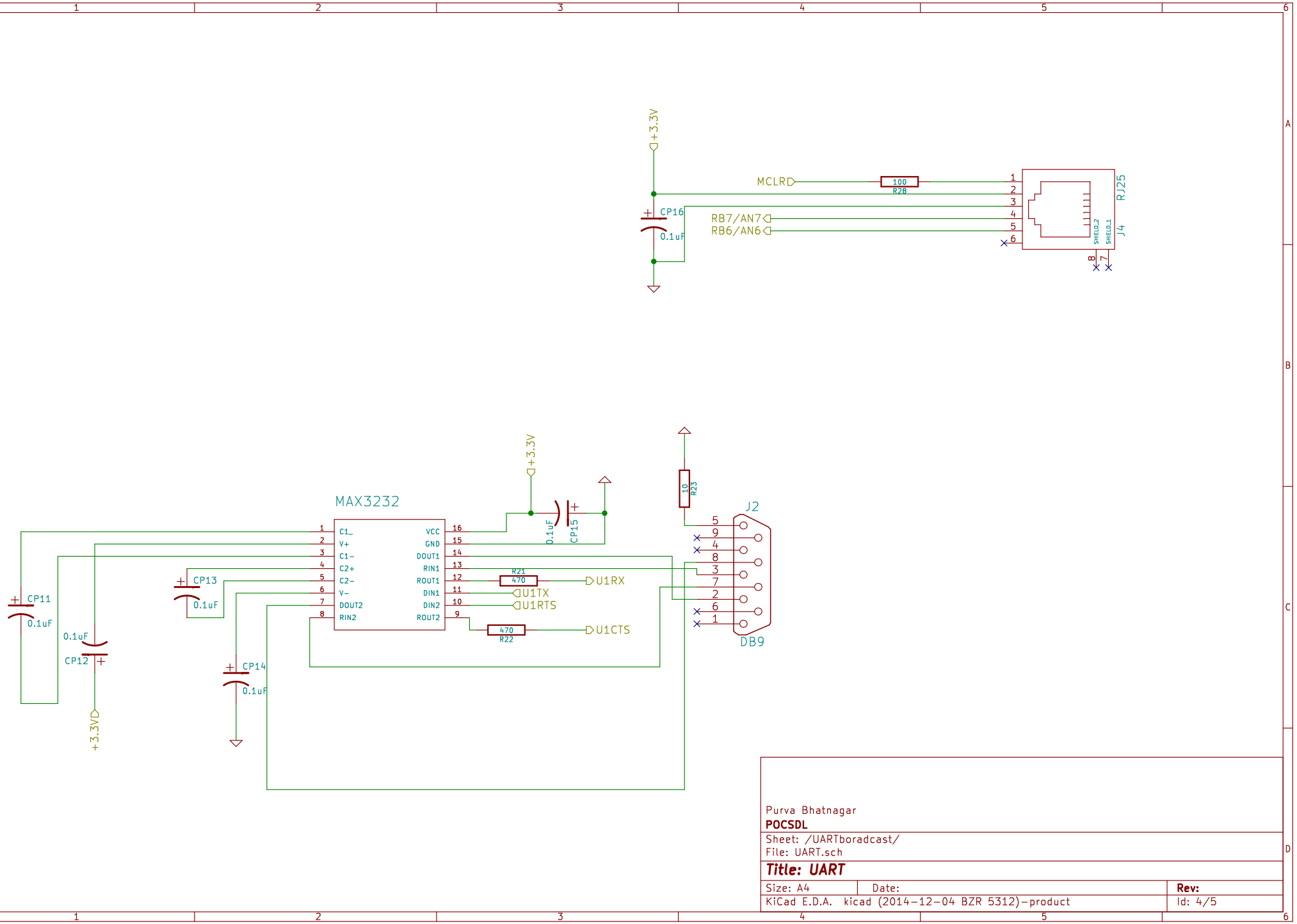
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MAX3232
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V+
C1-
C2+
C2-
V-
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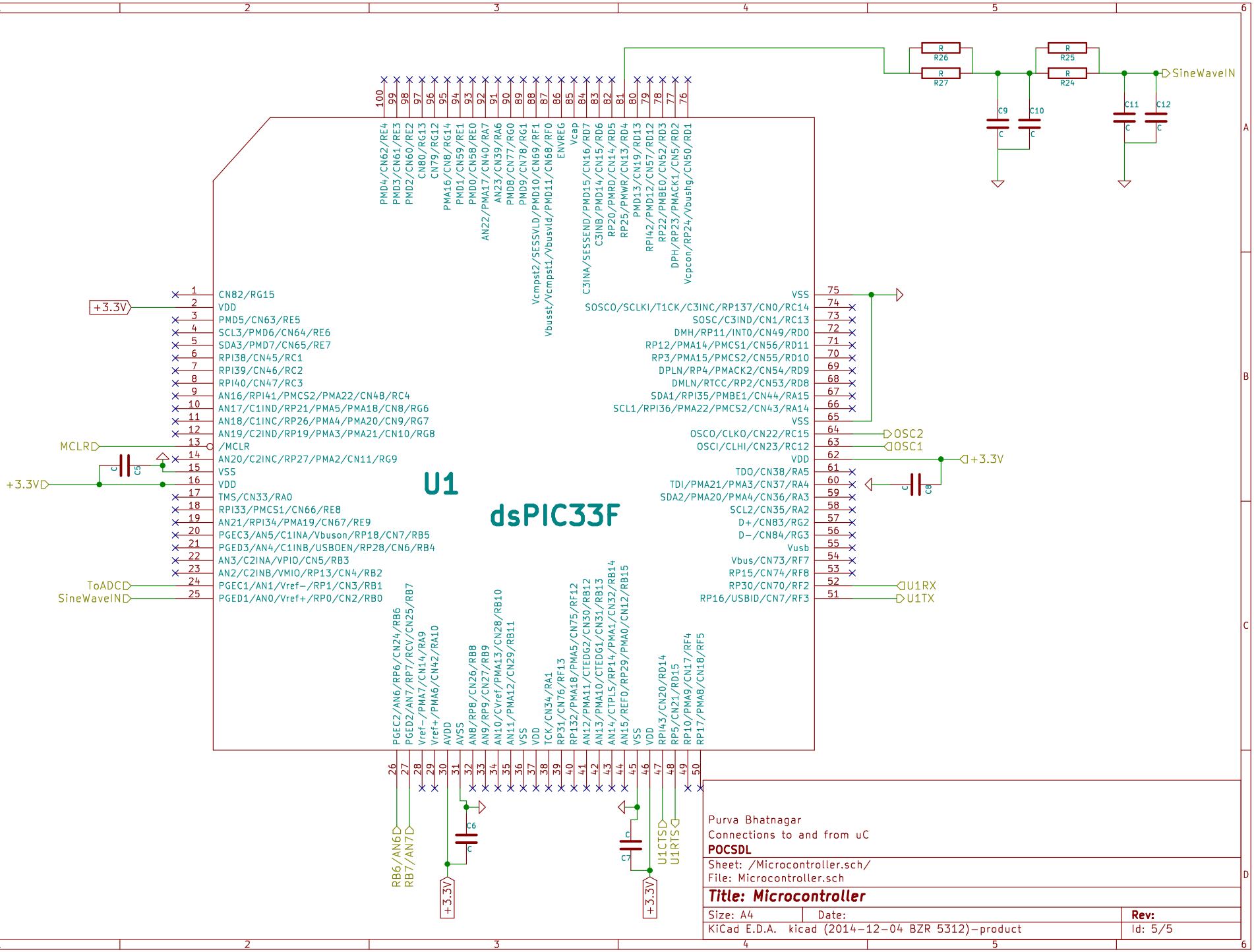

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