CHARACTERIZATION OF SINGLE EVENT UPSETS IN 32 NM SOI TECHNOLOGY USING ALPHA PARTICLE AND HEAVY-ION RADIATION SOURCES

By

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Thesis

Submitted to the Faculty of the

Graduate School of Vanderbilt University

In partial fulfilment of the requirements

for the degree of

MASTER OF SCIENCE

in

Electrical Engineering

August 2014

Nashville, Tennessee

Approved:

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ACKNOWLEDGMENT

I would first like to thank my advisor, Dr. Massengill, for his guidance and encouragement throughout this project. Next, I would like to thank Dr. Loveless and Jeff Kauppila for their work in designing the test chips and their insight and help throughout the work. To Drs. Alles and Reed, thank you for the many contributions and enlightening discussions. I am also greatly appreciative to Dr. Enxia Zhang for her work in packaging the test chips.

I would like to thank many of the RER students for their help and support, most importantly those without whom the work would not be done: Jeff Maharrey, Srikanth Jagannathan, and Nelson Gaspard. I would also like to thank my loving parents and friends who have encouraged and supported me throughout my work. Lastly, I am grateful to the Defense Threat Reduction Agency Rad-Hard Microelectronics Program as well as Robust Chip Inc. for their sponsorship of this work.

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CHAPTER I

INTRODUCTION

The response of electronic devices to ionizing radiation is a reliability concern for commercial and space applications. An ionizing particle can cause charge to be generated and collected at the node of a circuit. If the charge is collected in the memory element, a single event upset (SEU) can occur where a logic state is flipped from '0' to '1' or '1' to '0'. Since the discovery of single event effects, circuit designers have faced the challenge of creating radiation hardened by design (RHBD) flip-flops that decrease the memory element's susceptibility to SEUs [1]. Test structures of unhardened and hardened flip-flop designs are fabricated and irradiated in order to understand the relative error rates due to single event upsets. Each test structure is irradiated using heavy-ion particle accelerators to simulate the radiation in a space environment. In the past only particles with a relatively high linear energy transfer (LET) were capable of generating enough charge to flip the state of a memory element. However, as technology has scaled, the critical charge necessary to cause an SEU has decreased. Radiation effects must now be considered in calculating the error rate for commercial applications as well [2]. Irradiating circuits using isotropic button sources simulates terrestrial radiation such as alpha particles emitted from packaging material [3]. The continued improvement of RHBD techniques relies on the ability to thoroughly test circuits at each new technology node over all radiation environments and understand how the cells upset.

In this thesis, SEU data for hardened and unhardened flip-flop designs from a variety of radiation sources are presented. The combination of data from heavy-ion beam,

alpha particle beam, and isotropic alpha particle sources provides the critical parameters for calculating error rate for a given flip-flop design in a specific environment. Heavy-ion data also reveals the robust design of DICE, DICE Guard Gate, and Stacked flip-flops in comparison with unhardened DFF NAND and Transmission Gate flip-flops in 32 nm SOI technology. The stacked flip-flop designs fabricated in this technology show the least sensitivity to ionizing particles compared to the implementation of other hardening techniques.

CHAPTER II

BACKGROUND

Single Event Effects Overview

When an ionizing particle traverses silicon it loses energy, creating electron-hole pairs, which deposit charge in the device. The linear energy transfer (LET) of the particle depends on the particle type and energy. The deposition of charge in a device or circuit can result in a variety of effects depending on the LET and location of the strike. Some effects of radiation are destructive and are called hard errors. Examples of hard errors include single event gate rupture (SEGR) or single event burnout (SEB). Single events can also produce soft errors, which are non-destructive and lead to data corruption rather than device failure. A single event particle strike will cause a transient signal to appear on a node, which can then change the logic state of a circuit element. The amount of deposited charge from a particle strike to change the logic state is called the critical charge. When this transient causes an incorrect state to be latched in a memory device such as a flip-flop, the error is called a single event upset (SEU).

Radiation Environments Overview

The majority of particles interacting with silicon in space environments are high-energy particles trapped in belts, transient protons, and heavy ions from galactic cosmic rays [4]. Therefore, circuits evaluated for use in space applications require characterization of response to high Linear Energy Transfer (LET) particles such as heavy ions. Experiments are often conducted for these environments using heavy-ion accelerators.

Single event effects have also been discovered due to particle interactions in terrestrial environments. The first terrestrial single event upset in a memory device was seen by May and Woods. The error was linked to the interaction between the semiconductor device and alpha particles emitted from packaging material [4]. Therefore, the error rate of circuits due to terrestrial radiation is a key concern for commercial applications. The particles in this environment are primarily alpha particles from decaying packaging materials interacting with silicon. Experiments are often run using isotropic button sources to simulate alpha particles emitted from packaging materials.

Error Rate

In order to calculate the error rate of a circuit for a given radiation environment, experiments are performed to find the radiation response to a variety of particles. Two important parameters exist in understanding a circuit's response to radiation. These two parameters are used to find the error rate of a particular circuit in a given environment. The parameters are the limiting cross-section found using high LET particles, and LET threshold found using low LET particles. The LET threshold is related to the smallest amount of deposited energy that can cause an upset. The limiting cross-section describes the amount of deposited energy at which the addition of more energy will not cause any more upsets. The device has already been saturated with charge and the amount of damage a single particle can cause has been found at this value. It is important for each new technology node that the limiting cross-section and LET threshold are found to calculate the error rate. Figure 1 shows the critical parameters.

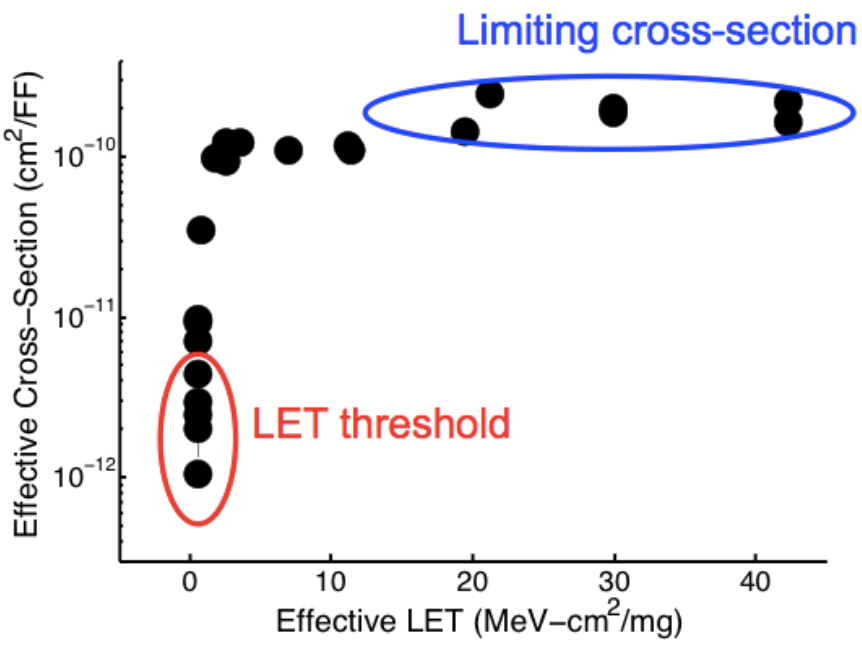

Figure 1: Example of two parameters necessary in calculating error rate: LET threshold and limiting cross-section.

Single Event Upset Hardening

As technology scales, the amount of deposited charge necessary to cause an SEU decreases, increasing the vulnerability of electronic devices [2]. However, a variety of radiation hardened by design (RHBD) techniques have been developed over the years to decrease circuit sensitivity to radiation. While effective at decreasing error rate, trade offs in area, speed, and power exist when choosing a RHBD circuit over an unhardened design. Several of these designs are discussed: DICE, DICE Guard Gate, and Stacked flip-flops. Radiation hardness is also affected by advancement in the fabrication of devices. One such example is the Silicon on Insulator (SOI) technology. It is important that with each new technology node, RHBD techniques are implemented and tested to ensure their continued improvement in radiation hardness over unhardened designs.

Silicon on Insulator

Silicon on Insulator technology was first introduced for its reduced sensitivity to latchup due to the isolation of individual transistors [5]. Figure 2 shows the charge generation and collection in a SOI device. The SOI technology offers the potential for an increase in radiation hardness over bulk technology because the buried oxide limits the amount of charge that can be collected from a single event strike. Despite the limited charge collection, SOI devices do not always provide an increase and robust design. Gain from the parasitic bipolar in SOI technology can increase the effect of single event current, resulting in comparable single event sensitivity to bulk technology [6],[7].

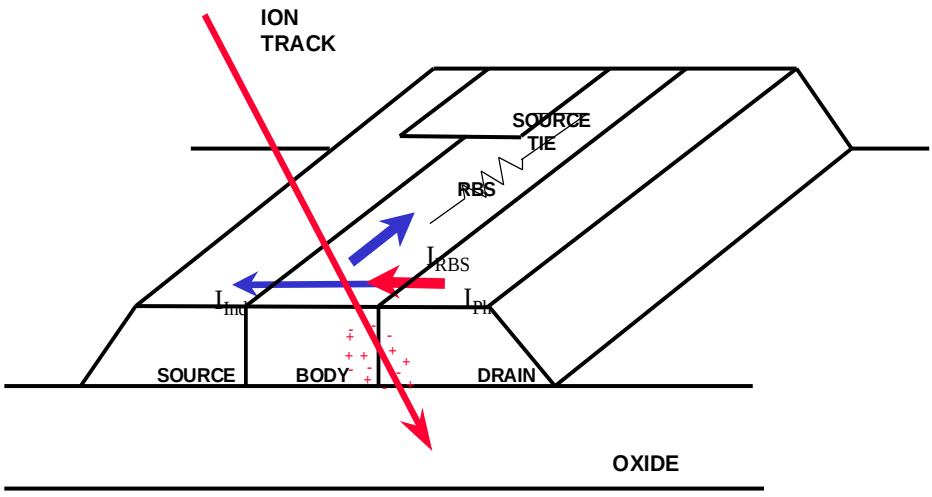

Figure 2. Charge generation and collection in an SOI device [6].

DICE

The first Dual Interlocked storage Cell (DICE) design was implemented in 1996 by Calin [8]. Figure 3 shows the schematic for the DICE design. The DICE memory latch stores data by using the value and its complement, stored in four different latches. All of the latches are read and written to at the same time through transmission gates. The

latches that are spatially close in proximity do not depend on one another. X0 and X2 store the data and X1 and X3 store the complement. Therefore, a single event would have to affect two of the nodes diagonal from each other in order to upset. The DICE latch has been widely adapted and used for radiation-hardened circuits in many technologies [9],[1],[10],[11].

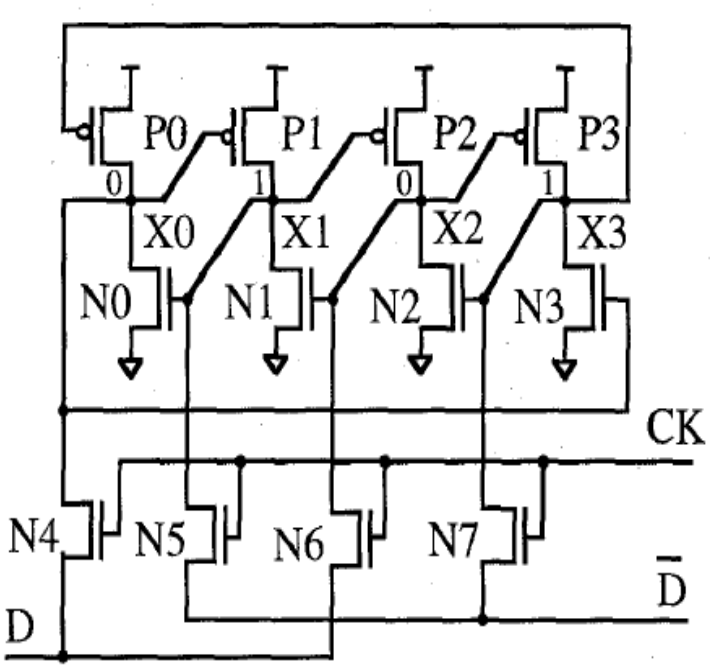

Figure 3. Schematic of the original DICE latch [8].

DICE Guard Gate

As technology size and consequently node spacing have decreased, single particle strikes are now able to cause charge collection on multiple nodes, and DICE designs are increasing in vulnerability. Guard bands have been shown to decrease the single event sensitivity of single devices [12] as well as implementation in flip-flop designs. DICE Guard Gate latch designs have been shown to have a radiation response better than the classic DICE configuration [13]. The DICE Guard Gate design is shown in Figure 4. In a

DICE latch, charge collection on two nodes can easily cause the latch to change state. The Guard Gate design prevents the latch from changing state unless both inputs to the same node are identical. If the inputs differ, the latch output will float to the previously held value and will not be upset.

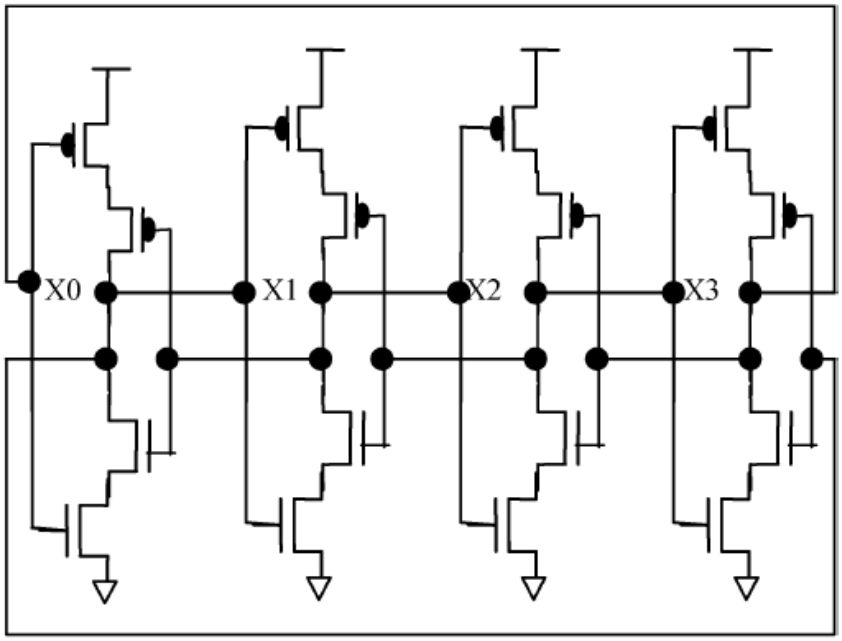

Figure 4. A DICE latch implemented with Guard Gates [13].

Stacked

Another recently discovered hardening technique is device stacking [14], [15]. The technique is simple to implement, where every individual transistor is replaced with two transistors that share a gate and one other common node. A schematic of a stacked inverter is shown in Figure 5. Both transistors must collect enough charge simultaneously to cause an upset. Variations of stacked devices have been irradiated and have shown increased radiation hardness over standard unhardened designs [14]. The two transistors

in the stack can also be fabricated on separate silicon islands, which provide increased hardness over stacked transistors that share a silicon island [1].

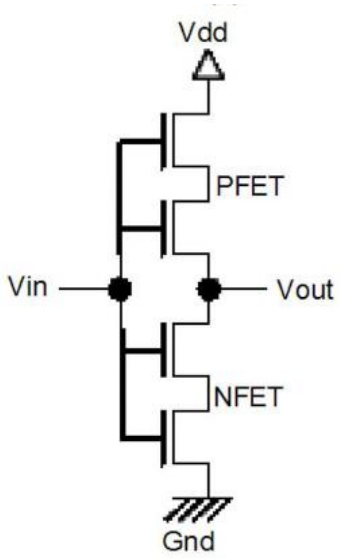

Figure 5. A stacked inverter [1].

DICE, DICE Guard Gate, and Stacked devices are three of the most commonly used RHBD techniques. The importance of understanding the radiation response of these designs cannot be overstated. With each new technology node, the impact of ionizing particles on hardened and unhardened designs must be characterized in order for progress in RHBD circuitry to continue.

CHAPTER III

TEST CHIP DESIGN

To observe the radiation response of various hardened flip-flop designs versus unhardened flip-flop designs, test chips are constructed to count SEUs from each type of flip-flop. The basic structure of the SEU test chip from this work is shown in Figure 6. Each topology of flip-flop is represented in a chain. Each chain contains thousands of flip-flops with the output of each flip-flop connected to the input of the following flip-flop. Thousands of flip-flops are included per chain to increase the area for radiation testing. A common input is tied to the input of the first flip-flop in each chain. During irradiation, an input is applied and clocked through the chains. At the output of each chain is an XOR gate, which effectively compares the input pattern to the output of the last flip-flop in the chain. The output of the XOR gate is then run to an asynchronous counter. If a single event causes a bit to flip in any of the flip-flops in the chain, the incorrect bit will be clocked through the chains until it reaches the last flip-flop. At that time the XOR gate will output a '1' and the asynchronous counter will count the error.

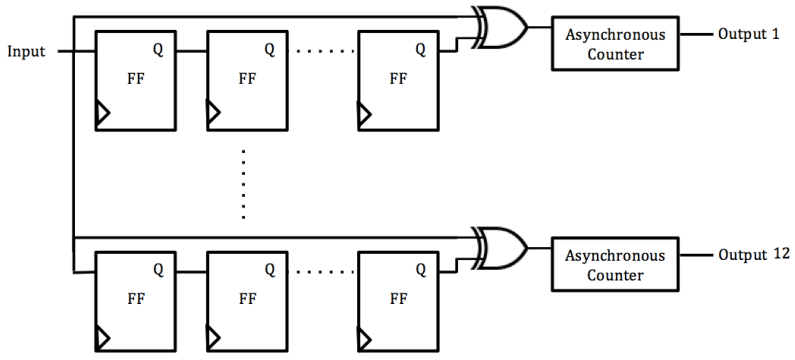

Figure 6. Schematic of the test chip design for SEU testing.

The test chip was designed in a 32 nm PDSOI technology and includes 7 chains of flip-flops designed by Vanderbilt ISDE engineers. All 7 chains of flip-flops are tested simultaneously during irradiation. Table 1 shows some of the relevant information for each flip-flop chain. The NAND and TG designs are both 4.07 um in length. The increase in length of the hardened designs is shown in Table 1 as a ratio. The difference in the flip-flop design areas is also shown through layout pictures in Figure 7 [15].

Name	Length (um)	Normalized Length	Description
NAND DFF	4.07	1	Unhardened NAND DFF
Stacked NAND DFF	8.75	2.15	NAND DFF using stacked transistors
TG DFF	4.07	1	Unhardened Transmission Gate DFF
Stacked TG DFF	6.8 (5.5 w/o buffer)	1.67 (1.35)	TG DFF using stacked transistors
DICE	7.58	1.86	DICE from [8]
DICEGG1	9.79	2.41	DICE Guard Gate with single output
DICEGG2	9.79	2.41	DICE Guard Gate with two outputs

Table 1. Information about the 7 flip-flop designs on the 32 nm SOI SEU test chip.

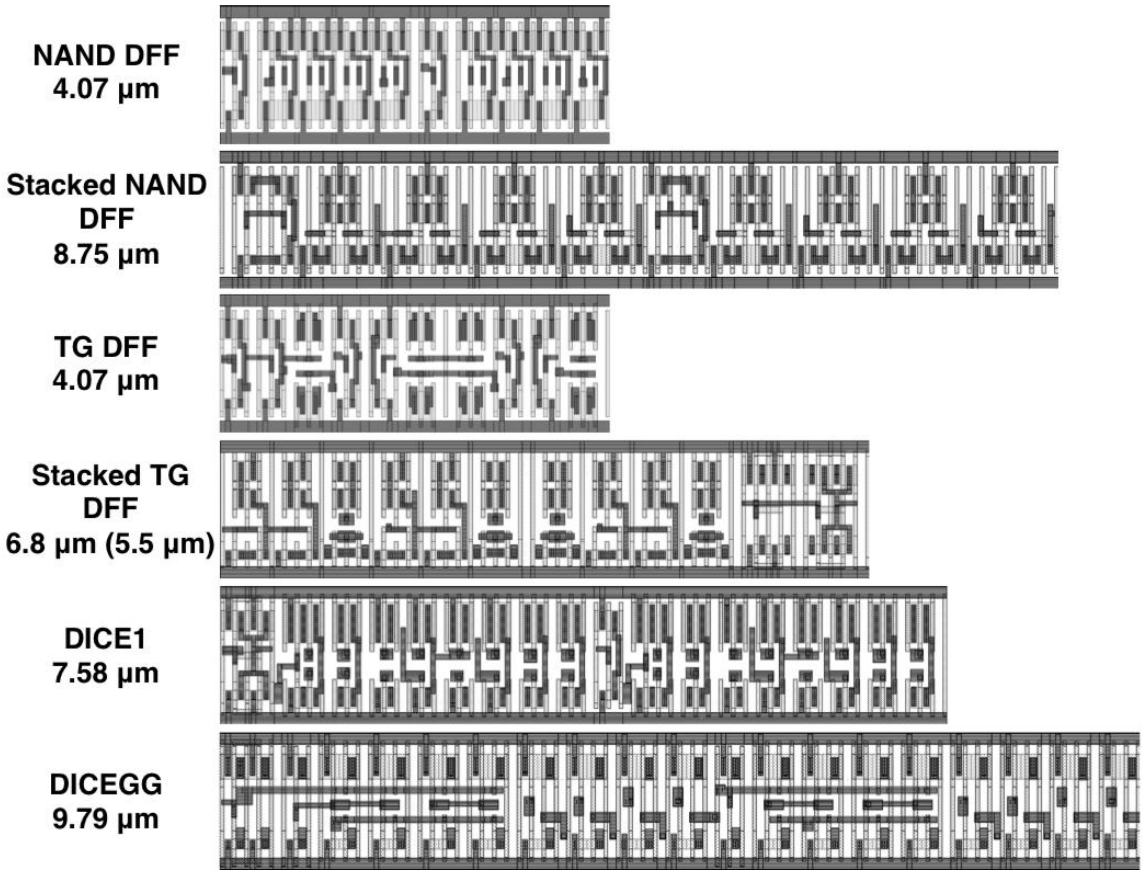

Figure 7. Pictures of the layout of each of the SEU test chip flip-flop designs [15].

The standard DFF NAND and Transmission Gate flip-flops are unhardened designs that are used as a baseline in comparison with the radiation hardened designs shown in Figure 8 [15]. It is important to include baseline designs to understand the relative hardness of RHBD designs compared to unhardened designs in the same technology.

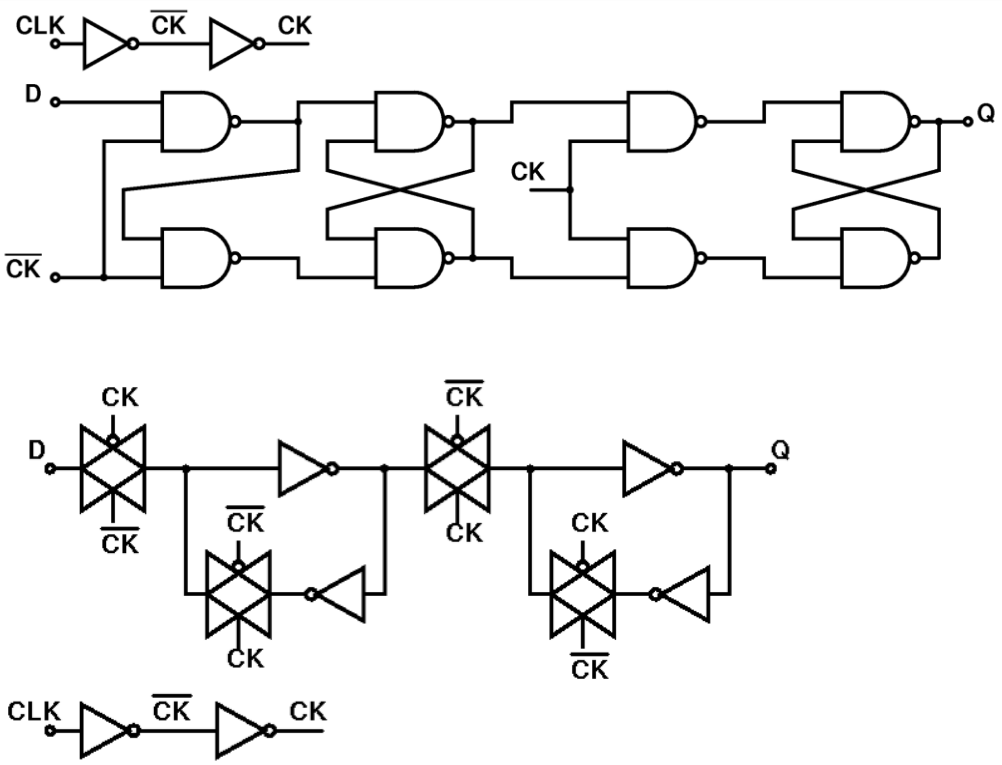

Figure 8. Schematic of the NAND (top) Transmission Gate (bottom) flip-flop design [15].

The DICE design is identical to that used in [8]. Two DICE Guard Gate designs are included on the test chip. The Guard Gate design is identical to that used in [13]. Guard Gate design 1 passes the output to the next flip-flop in the chain. Guard Gate design 2 passes the output and its complement to the next flip-flop chain.

The stacked NAND and TG designs are identical to the DFF NAND and TG designs, replacing every single transistor with a stacked transistor. The designs are similar in concept to the stacked devices used in [1] and explained in a previous chapter. The NMOS devices were fabricated in the side-by-side configuration, while the PMOS devices were fabricated in the inline configuration. Figure 9 shows the layout of an inverter implemented in the stacked design for the Stacked NAND and TG flip-flops.

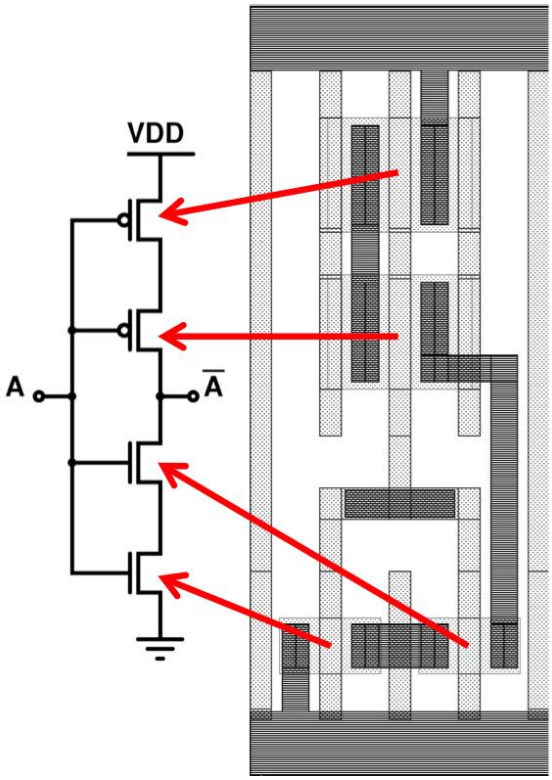

Figure 9. Stacked inverter layout [15].

By stacking devices, the angular range at which an incident particle strike can cause an upset is reduced. Strikes must deposit charge in more than one transistor to produce an upset. Therefore, the stacked flip-flops are theoretically immune to upsets at normal incidence where a particle strike will only deposit charge in a single transistor. Figure 10 shows the PMOS and NMOS device minimum spacing and distance between sensitive regions. P_A and P_B are the highest sensitivity regions and were found using TCAD.

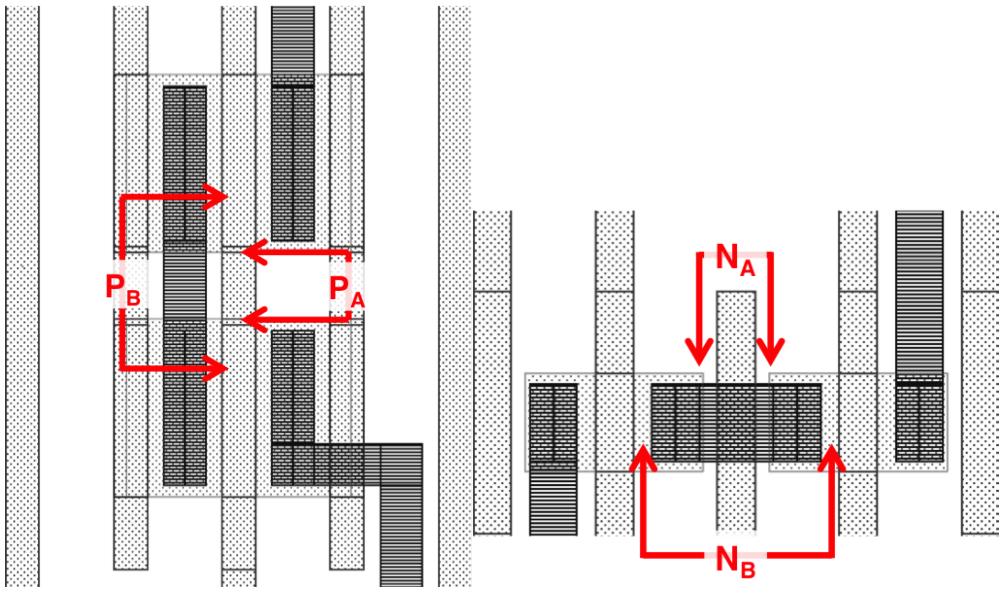

Figure 10. The stacked PMOS (left) and NMOS (right) devices from the inverter in Figure 9. The 'A' spacings represent the minimum spacing between devices and the 'B' spacings represent the distances between sensitive device regions [15].

Based on these diagrams, only an ion with tilt angle of 45° or greater can traverse the silicon and interact with both points on P_A and N_A. In order for an upset to occur due to a strike on P_B or N_B, a tilt angle of 65° or greater must be achieved by the ionizing particle.

CHAPTER III

EXPERIMENTAL SETUP

Three types of irradiation experiments were performed on the SEU test chip: heavy-ion beam, alpha particle beam, and alpha particle button source. This chapter will describe the details of each experiment as well as the experimental setup used consistently in each experiment.

The standard Vanderbilt test coupon was used to interface the SEU test chip with experimental equipment. The test coupon uses a backplane and GPIO PCB to interface a custom PCB created for each test chip with test equipment. The custom PCB for this test chip is shown in Figure 12. The DUTs were bonded on-site in PGA packages, as shown in Figure 11, and fit into the board using a socket. Power was supplied to the board using banana jacks and signals were routed to SMA connectors on the board to check the functionality of the test chips. Signals such as the input pattern and clock signal were routed to SMA connectors to ensure test code functionality before every test was run.

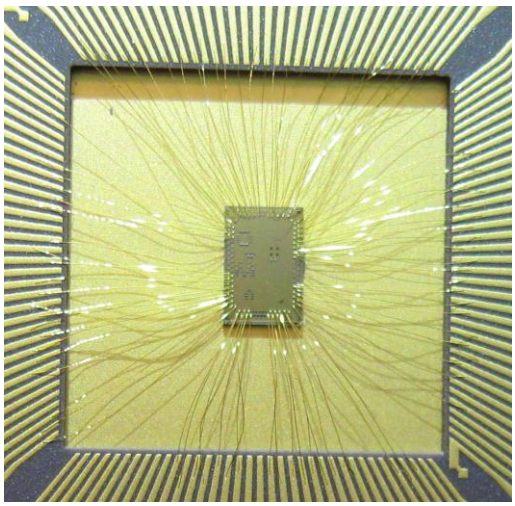

Figure 11. A picture of the test chip bonded in a PGA package.

The input and clock signals were applied to the chip using Quartus code written for an Altera DE2-115 FPGA. The FPGA would read the 4-bit asynchronous counters about every 3 seconds and send a reset signal to clear the counters. This ensures that the counters do not overflow with upsets before being read. Before testing at each beam facility, a counter test was conducted by collecting data at a high flux and a low flux. The results of each of these tests were comparable results with both flux levels. This test gave confidence that the on-chip counters were not overflowing with upsets before being read out to the FPGA. Experiments were performed using all '0' and all '1' input patterns and all experiments were run at a clock speed of 30 kHz.

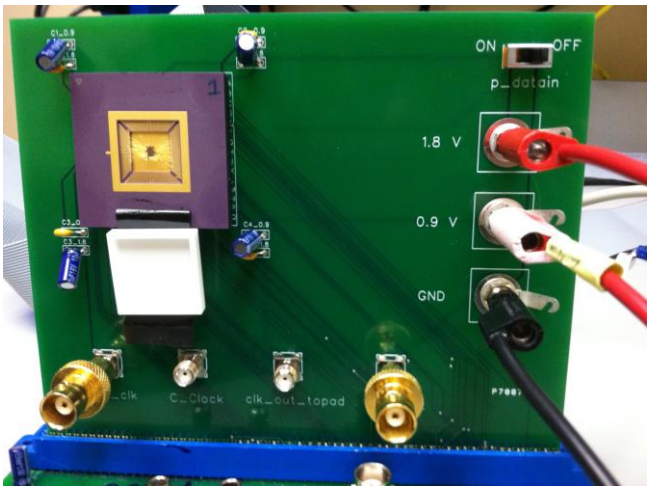

Figure 12. The PCB created for the radiation testing of the SEU test chip.

From August 2013-March 2014 radiation experiments were performed on test chip 32-VuRC-2 using heavy-ion beams at Lawrence Berkeley National Lab (LBNL) and Texas A&M University (TAMU) and alpha particle button sources and beam (Pelletron) at Vanderbilt University. The experimental setup described above was used for all of the experiments. An overview of the experiments performed is given in Table 2.

Type of irradiation	Facility	Experiment Type	Radiation Source	Source Energy
Heavy-ion	Lawrence Berkeley National Laboratory	88’ Cyclotron	O, Ne, Ar, Cu, Xe	10 MeV/amu
Heavy-ion	Texas A&M University	Cyclotron	Ne, Ar	25 MeV/amu
Alpha (broad beam)	Vanderbilt University	Pelletron	He^{2+} (α particle)	6 MeV
Alpha (isotropic)	Vanderbilt University	Button source	^{252}Cf	5.9 MeV
Alpha (isotropic)	Vanderbilt University	Button source	^{241}Am	5.5 MeV

Table 2. An overview of all of the types of experiments performed on the SEU test chip.

Heavy-ion broad beam

Heavy-ion experiments were performed in vacuum at LBNL using the 10 MeV/amu cocktail and in air at TAMU using the 25 MeV/amu beam. A picture of the experimental setup in the vacuum chamber at LBNL is shown in Figure 13. The Vanderbilt test setup is placed inside the vacuum chamber and BNC connections are used to connect signal lines to power supplies outside of the chamber.

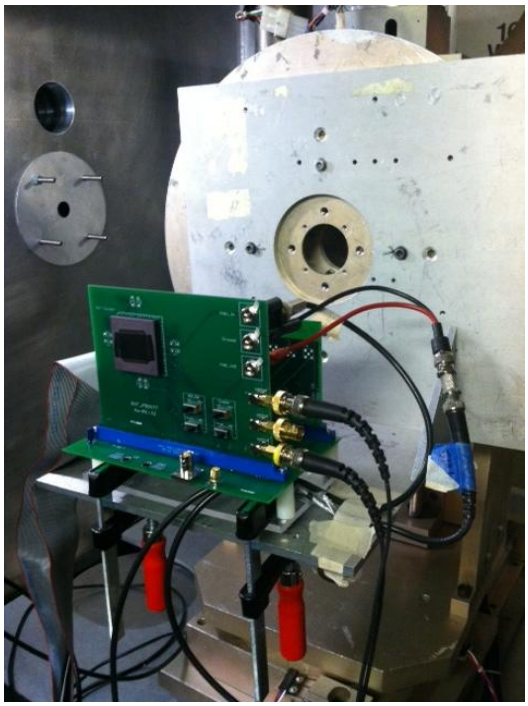

Figure 13. The Vanderbilt test setup in the vacuum chamber at LBNL.

High Current State

Upon heavy-ion irradiation, a high current state was encountered in the I/O pad ring of the 32 nm SOI test chip. High current states above ~750 mA caused bond wires to melt. After these conditions, resetting the DUT supply caused the DUT to operate normally, and the high current state could not be achieved. A temporary solution which allowed for the completion of the heavy-ion test was to use thick copper foil as shielding to cover the I/O pad ring, as shown in Figure 14. This approach allowed for normal incident irradiation up to an LET of 59 MeV-cm^2/mg. In a subsequent test, the I/O was operated at the lowest voltage possible while still maintaining functionality. The I/O could be lowered from 1.8 V to 1 V. Using this method the DUT could be irradiated up to an LET of 20 MeV-cm^2/mg before exhibiting any abnormal effects. Irradiating slightly above 20 MeV-cm^2/mg caused transient high current states to appear on the I/O.

Irradiating significantly above 20 MeV-cm^2/mg caused the sustained high current state as seen previously.

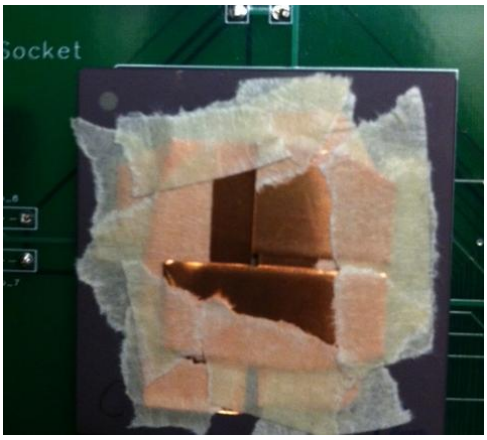

Figure 14. Test chip covered in copper foil, used to gather data without triggering the high current state in the I/O pad ring.

The Xenon data obtained at LBNL was the result of melted bond wires or a shielded I/O pad ring. Copper data from LBNL used a lowered I/O voltage and was therefore taken in a noisy environment. Data from TAMU was only taken for two particles, Argon and Neon, not exceeding an LET of 6 MeV-cm^2/mg to avoid any issues surrounding the I/O high current state. No effects were seen during irradiation using alpha particle button sources or broad beam.

Elevated Bonding

One of the goals in testing this chip for radiation response was to understand the sensitivity of hardened designs in comparison with unhardened designs. After observing no upsets on these designs on the first test trip using Xe (LET~59 MeV-cm^2/mg), several test chips were bonded for high angle testing. Gold plates were placed in the bottom of the PGA package to raise the die to a level above the edge of the package as shown in Figure 15.

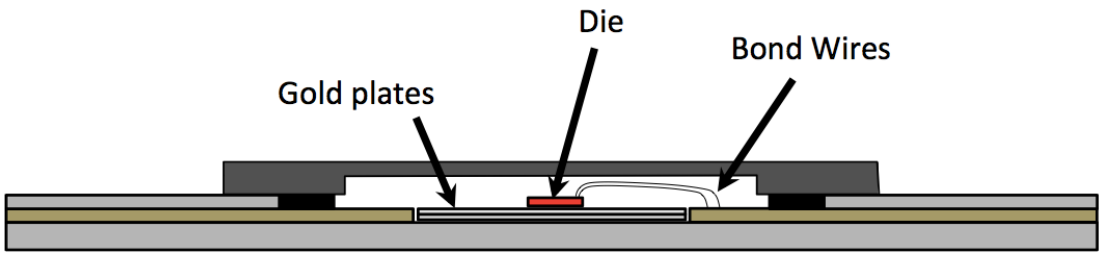

Figure 15. Die raised by gold plates in the PGA package for high angle testing.

Bonding only one side of the chip allowed future tests at high tilt angles without the concern of bond wires or bumps causing shadowing on a portion of the chip. For this reason, some of the data show results only for the even or odd chains. The bonding diagrams for high angle testing are shown in Figure 16. Bonding the right hand side of the chip allows for unobstructed irradiation of the even flip-flop chains: Stacked NAND, Stacked TG, DICE Guard Gate 1, and 3 DICE variations. Bonding the left hand side exposes the odd flip-flop chains: DFF NAND, DICE, DFF TG, and DICE Guard Gate 2. Data was obtained up to a tilt angle of 75°, revealing increased sensitivity of hardened flip-flop chains.

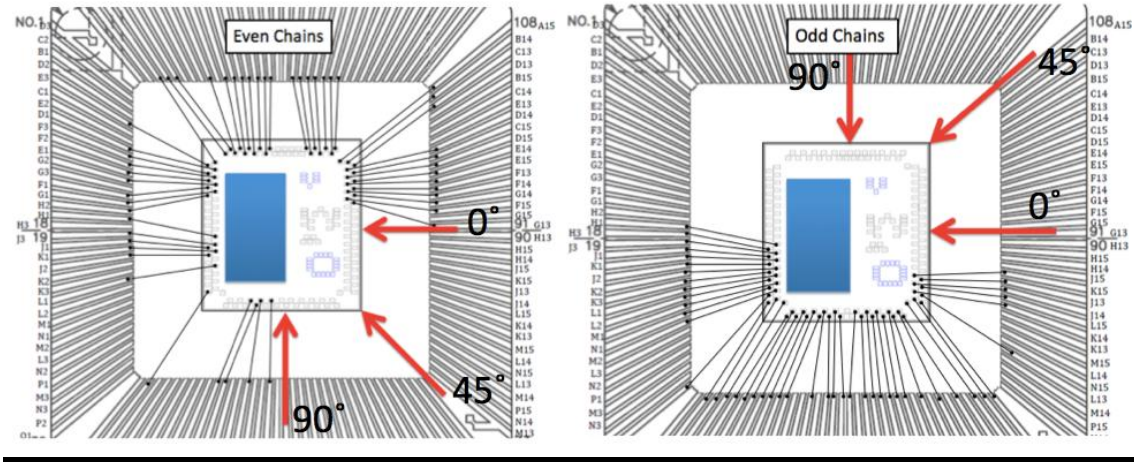

Figure 16. Bonding diagrams for high angle testing.

Alpha particle broad beam

Alpha particle beam experiments were performed in the Pelletron at Vanderbilt University using 6 MeV alpha particles. The test setup was similar to that at LBNL and TAMU, where the experiments were performed in a vacuum chamber and power and signal connections were made using SMA cables and ribbon cables through the chamber. The majority of the alpha particle Pelletron tests were performed at normal incidence and few tests were performed at a 45° tilt angle and 0° face angle. Experiments were run to a minimum fluence of 5E8 alphas/cm^2, comparable to the fluence from previous heavy-ion testing.

Alpha particle button source

Alpha particle button source experiments were performed at Vanderbilt University using ^{252}Cf and ^{241}Am button sources. The sources were placed directly on top of the DUT about 1 mm away. The tests were run for 2-5 days to achieve a fluence of ~1E10 alphas/cm^2. The emission is in 4π space therefore, the fluence was calculated taking the Californium and Americium as point sources and calculating the solid angle containing the chip. Californium emits 97% alpha particles and 3% fission fragments. The fission fragments produced are the heavy ions Neodymium (80 MeV) and Cadmium (106 MeV) both of which have an LET~ 40 MeV-cm^2/mg [16]. The alpha particles have energy of 5.9 MeV. The Americium source emits 5.5 MeV alpha particles in 4π space.

CHAPTER IV

EXPERIMENTAL RESULTS: COMPARING RADIATION SOURCES

Because of the wide variety of radiation sources used in these experiments, results not only showed the relative hardness of various types of flip-flop chains, but also gave insight into the comparison of the different sources. Data from each of the radiation sources used has provided an essential piece of the data necessary to fully understand the radiation response of the unhardened flip-flop designs on the 32 nm SOI SEU test chip.

The results from heavy-ion irradiation are shown in Figure 17 for the NAND based flip-flop. The Ne and Ar data are from irradiation at TAMU and the Cu data is from irradiation at LBNL. As expected, the limiting cross-section can be found from these results to be ~2E-10 cm^2/FF. The TG data shows a similar curve with a lower limiting cross-section of ~6E-11 cm^2/FF. Although the designs are the same size, the NAND design is shown to be more sensitive to single event upsets. Heavy-ion data also reveals that the LET threshold is lower than 1.8 MeV-cm^2/mg for both unhardened designs.

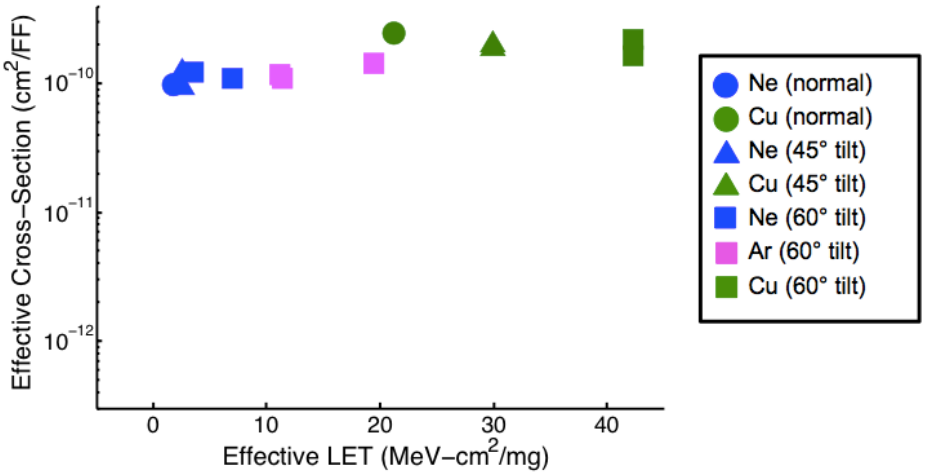

Figure 17. Heavy-ion data plotted as Effective Cross-Section vs. Effective LET for the NAND flip-flop design. These data reveal the limiting cross-section for this design. Error bars representing the standard error are within the symbols.

A comparison between Pelletron alpha beam data and isotropic button source data for both unhardened flip-flop designs is shown in Figure 18. The difference in button source and alpha beam data at normal incidence can be explained by angled strikes from the isotropic sources. The majority of emitted particles from the button sources strike the silicon at normal incidence or at an angle slightly off of normal incidence. Therefore, button source cross-section data falls between the Pelletron data at normal incidence and the data at a 45° tilt angle. These data reveal that the angled strikes from the isotropic sources contribute to the error rate by increasing the cross-section. However, alpha particle irradiation data for the TG flip-flop of Figure 4 shows that this design is no more sensitive to angled strikes from button sources compared to normal incidence strikes because both cases reveal the same cross-section. The 45° tilt angle Pelletron data shows an increase in cross-section from button source data for both unhardened flip-flop designs. Most terrestrial radiation testing is performed using these isotropic button

sources. Alpha beam results suggest that the cross-section in an alpha particle environment can be underestimated using button sources.

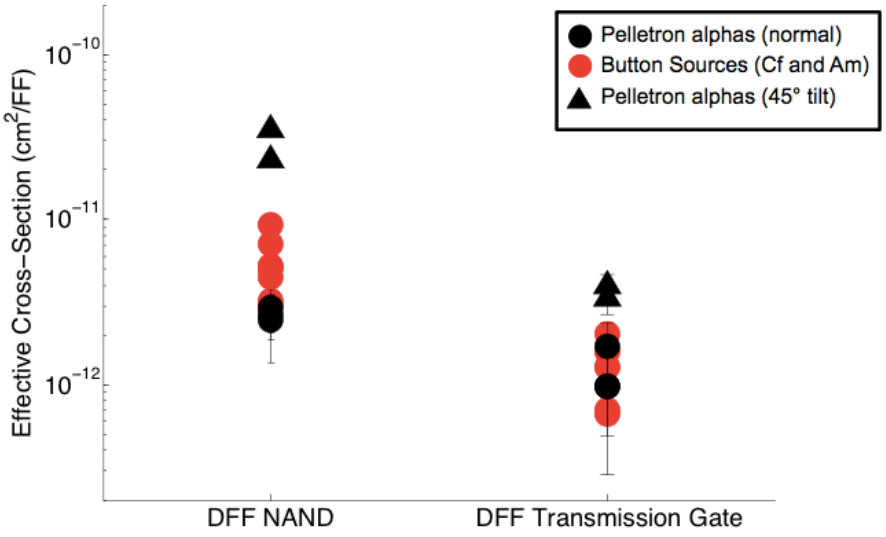

Figure 18. Pelletron alpha beam and isotropic button source data for both NAND and TG flip-flops.

This difference is most obviously shown by the order of magnitude increase in cross-section from button source alpha irradiation to 45° tilt angle Pelletron alpha irradiation for the NAND flip-flop. The effective LET of a 45° tilt angle strike is given by:

$$Normal\ incidence\ LET\ (0.6\ ) * \frac{1}{\cos(45°)} = 0.84\ MeV - cm^2/mg$$

Therefore, from Pelletron alpha irradiation data, the LET threshold of the DFF NAND flip-flop in 32 nm SOI technology is found to be between 0.6 and 0.84 MeV-cm^2/mg. Figure 19 displays data from all 3 types of irradiation in an Effective Cross-Section vs. Effective LET plot for the NAND flip-flop design.

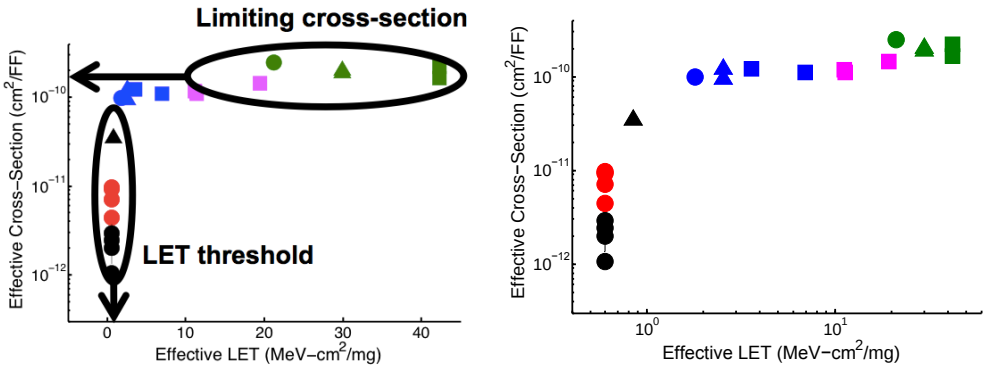

Figure 19. Effective Cross-Section vs. Effective LET curves for the NAND flip-flop design. The semi-log plot on the left highlights the limiting cross-section and LET threshold that have been found using a combination of heavy-ion and alpha particle accelerators. The log-log plot on the right emphasizes the importance of using a variety of sources to well characterize the low LET radiation response of the flip-flop. The data symbols correspond to those described in Figures 17 and 18.

The addition of alpha beam data uncovers the full shape of the curve. The critical parameters for finding error rate, limiting cross-section and LET threshold, are clearly marked. The use of alpha particle and heavy-ion accelerators in comparison with isotropic button sources has revealed the error rate parameters as well as given a better understanding of the angular dependence of strikes to the devices. These results are important for comparison with and the development of new RHBD designs.

CHAPTER IV

EXPERIMENTAL RESULTS: HARDENING TECHNIQUES

Data from both heavy-ion and alpha particle irradiation illustrate the effective use of the hardening techniques implemented on the 32 nm SOI SEU test chip. The Stacked NAND and Stacked TG flip-flops were proven to be the most radiation hardened by design flip-flops on the test chip. Tests using a variety of heavy ions over a wide range of tilt angle have revealed the predicted sensitivity of hardened designs.

Alpha Particle Irradiation Results

Figure 20 shows the results of Americium and Californium testing performed on 3 different test chips. The flip-flops are ordered from softest to hardest in the plot. The error bars shown represent the standard error. Only one upset was recorded on the Stacked NAND flip-flop design. The other hardened flip-flop designs saw less than 5 upsets, while the NAND and TG flip-flop cross-sections represent thousands of upsets.

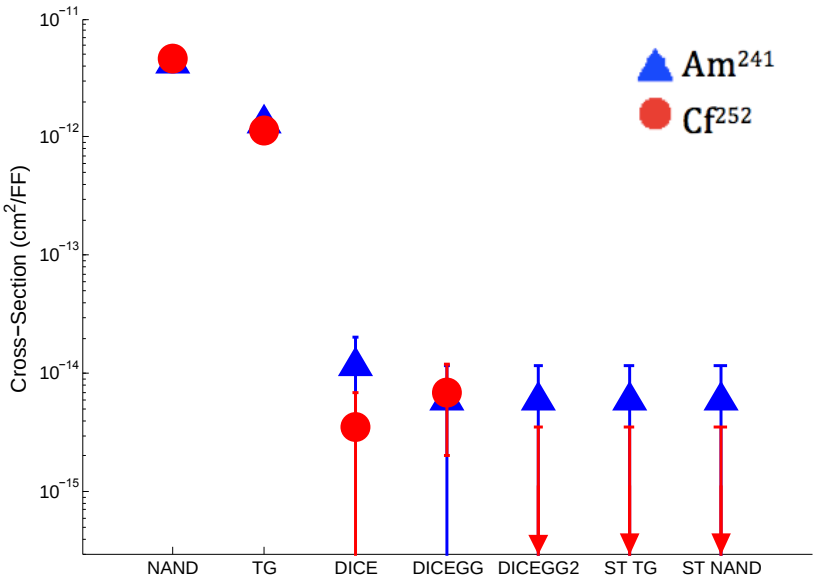

Figure 20. Results from Americium and Californium button source testing. Unhardened flip-flop design cross-sections represent ~1000 upsets while hardened designs saw no more than 5 upsets each.

The only upsets recorded on hardened flip-flop designs in the Pelletron experiments were on the DICE Guard Gate 2 design. Many upsets were recorded at one time and these results were shown on two different test chips. However, no explanation for these upsets can be made from the design. For both normal incidence and 45° tilt angle, no upsets were seen on the Stacked NAND, Stacked TG, DICE, or DICE Guard Gate 1 designs. These results are consistent with heavy-ion data which show the LET threshold of these hardened designs is higher than the LET of an alpha particle at normal incidence or a 45° tilt angle.

Heavy-ion Irradiation Results

The comparison of radiation hardness of the RHBD designs was found through heavy-ion testing over varying LET and tilt angle. Shown in Figure 21 is a comparison of the NAND, DICE, and Stacked NAND flip-flop cross-sections for heavy-ion copper and argon irradiations over a variety of tilt angles. These data further illustrate the

effectiveness of the DICE and stacked NAND RHBD techniques. The full cross-section curve from which limiting cross-section and LET threshold can be drawn is shown for the DICE design. The radiation response of the DICE design is better than that of the DFF NAND design, whose LET threshold is less than 3.5 MeV-cm^2/mg. The Stacked NAND point that approaches the DICE cross-section is from a 75° tilt angle irradiation and is further explained in Figure 22.

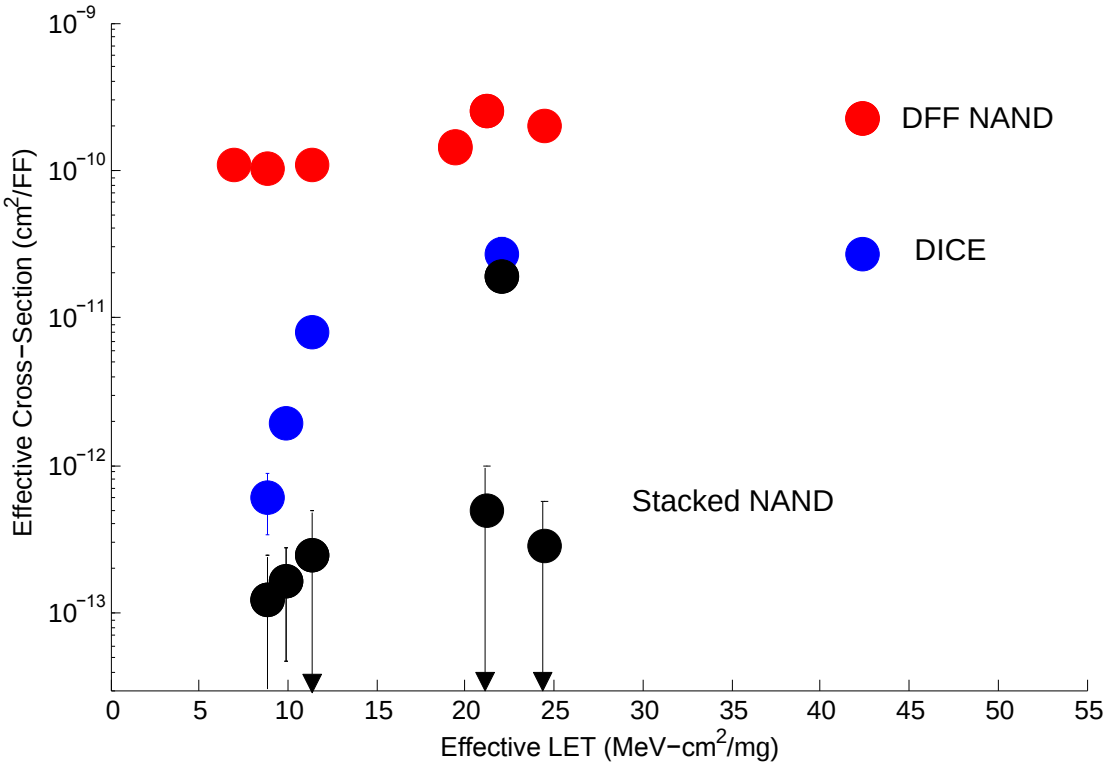

Figure 21. Cross-section vs. Effective LET curve using data from TAMU and LBNL (Cu and Ar over a variety of tilt angles). Data show the effective use of stacking devices to lower cross-section and a comparison of the technique with a classic DICE hardened flip-flop.

The hardened flip-flop designs showed a significant decrease in cross-section from the unhardened designs. Only at very high tilt angles did the hardened flip-flop designs approach the cross-section of the NAND and TG designs. Figure 22 shows the

sensitivity of 5 different flip-flop designs over varying tilt angle using Ar (LET~6 MeV-cm^2/mg), an 'all-0' data pattern, and a 90° roll angle (perpendicular to the gate).

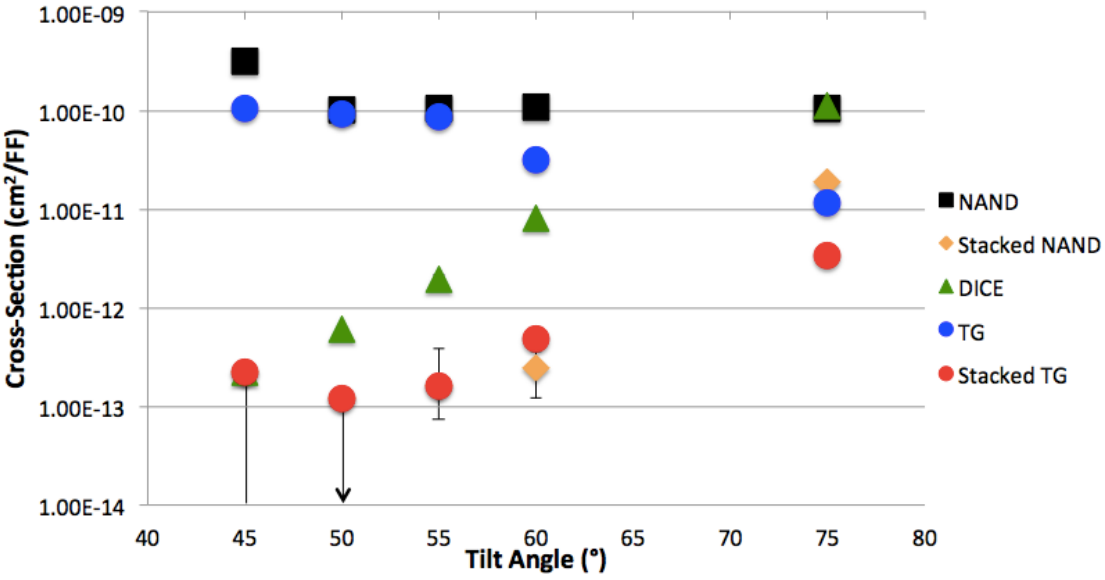

Figure 22. Data from TAMU using the heavy-ion Ar at a 90 degree roll angle. Cross-section is shown for a variety of tilt angles. Increasing the tilt angle above 45 degrees shows the sensitivity of the hardened NAND and TG stacked transistor flip-flop designs.

Stacked NAND and Stacked TG designs show increased sensitivity with increasing tilt angle, as speculated by the stacked devices flip-flop layout. The results displayed in Figure 22 are in agreement with the angular sensitivity deduced from the layout of the designs, further explained in Chapter 3. The Stacked flip-flops were designed with theoretical immunity to particle strikes up to 45° for spacing between devices and 60° for spacing between sensitive regions as shown in Figure 10 and further discussed in [15]. The Stacked flip-flops continue to show an increase in radiation hardness compared to their unhardened baseline versions up to and at a 75° tilt angle. Unlike the other designs, the unhardened Transmission Gate flip-flop shows a decrease in cross-section with increasing tilt angle. This behavior of the cross-section curve over tilt angle indicates the influence of a geometric effect on the TG flip-flop radiation response.

This plot also shows the performance of Stacked designs in comparison with a classic DICE hardened design. The DICE design shows a linear increase in cross-section with increasing tilt angle and equal to the unhardened designs over 75° tilt. These data gathered on all of the RHBD designs for a wide range of LET and tilt angle further enlighten circuit designers of the ways to design flip-flops for robust circuitry at future technology nodes.

CHAPTER V

CONCULSIONS

The variety of experiments performed on the 32 nm SOI SEU test chip has given unique insight into the radiation response of unhardened NAND and TG flip-flop designs. Two important factors in calculating error rate, LET threshold and limiting cross section, have been found using alpha particles and heavy-ions. Heavy-ion irradiation revealed the limiting cross-section of both designs. Normal incidence and 45° tilt angle alpha beam irradiation data provided confidence in the LET threshold by adding needed points to the cross-section vs. LET curve. Alpha beam data bounded isotropic button source irradiation data and allowed further insight into the angular dependence of alpha particle strikes. These data have shown that using particle accelerators for irradiation experiments over isotropic button sources gives further insight into a circuit's response to radiation for a subset of angles and particle energies.

Heavy-ion irradiation of hardened designs has shown the relative hardness of RHBD design techniques. The technique of stacking devices provides increased hardness over DICE and DICE Guard Gate designs. The angular sensitivity of the hardened devices was found up to a tilt angle of 75 degrees. All of the information presented in this thesis is valuable in gaining a comprehensive understanding of a circuit's radiation response and continuing improvement of radiation hardened by design circuits.

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