TOTAL DOSE IRRADIATION EFFECTS ON SILICON AND GERMANIUM MOS CAPACITORS WITH ALTERNATIVE GATE DIELECTRICS

By

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To my grandfather, who recently passed away, for his forever love and support

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CHAPTER I

INTRODUCTION

Microelectronic components are essential elements in space exploration systems. While in space the electronics are exposed to various types of radiation that can detrimentally affect device operations. Radiation such as photons, neutrons, protons, and electrons, interact with the semiconductor material to cause atomic displacement, ionization, and/or internal energy changes. Total-dose irradiation is especially a concern for the long-term reliability of Metal-Oxide-Semiconductor (MOS) devices. Understanding radiation effects on semiconductor devices remains critical to the application of advanced technologies in space and terrestrial environments. Furthermore, radiation effects can become increasingly complex to understand as newer technologies and materials are introduced.

The number of transistors on an integrated circuit approximately doubles every two years, as described by Moore's Law. In response to the demands for faster microelectronic components, the semiconductor manufacturers seek to enhance performance and cut costs by reducing device dimensions. The aggressive scaling of device dimensions has driven SiO_2 MOS technology close to the end of its era of continual improvement. The gate leakage current is the primary limitation for SiO_2. For gate oxides < 2 nm, the gate leakage current due to quantum mechanical tunneling becomes unmanageable (> 1 A/cm^2) [1]. Alternative high dielectric constant (high-k)

gate oxides will most likely be the future for MOS technology.

Table 1. Dielectric constant, band gap, and band offsets for high-k dielectric materials (After[2]).

Materials	Diele. Constant (K)	Band Gap (eV)	CB Offset (eV)	VB Offset (eV)
SiO_2	3.9	8.9	3.5	4.4
Si_3N_4	7	5.1	2.4	4.4
Al_2O_3	9	8.7	2.8	4.9
Y_2O_3	15	5.6	2.3	2.6
La_2O_3	30	4.3	2.3	2.6
TiO_2	80	3.5		
Ta_2O_5	26	4.5	0.3	3.0
$ZrSiO_4$/ $HfSiO_4$	13-26		1.5	3.4
HfO_2	25	1.5	1.5	3.4
ZrO_2	25	3.4	1.4	3.3

High-k devices, due to larger charge storage capacity relative to SiO_2, allow for a physically thicker gate oxide while maintaining a low electrical oxide thickness. Among the likely candidate high-k materials that are currently being investigated include ZrO_2, Al_2O_3, Ta_2O_5, La_2O_3, and HfO_2 [2-5]. Table 1 lists several alternative dielectric materials and their respective relative dielectric constant values, energy band gaps, and band offsets [2, 5]. The larger band gap and band offsets in SiO_2 discourage electron tunneling. On the other hand, high-k dielectrics have significantly reduced band gap and band offsets, which increase the gate leakage current via electron tunneling. As shown in Fig. 1, the dielectric constant and band gap values for various gate oxide materials are inversely related. A higher dielectric constant ordinarily comes at the cost of a reduced energy band gap. Another critical issue in the development of high-k devices is the gate

oxide/substrate interface quality. Being a native oxide of Si, SiO_2 can be processed to form an almost perfect interface with the Si substrate. The interface between a high-k dielectric and Si contains many structural defects due to lattice mismatch, which results in a much higher density of process-induced interface traps in high-k MOS systems [6]. In addition, an interfacial layer always forms between the high-k dielectric and the Si substrate. The interfacial layer, usually in the form of SiO_x, has a much lower dielectric constant relative to the high-k layer, so the effective gate oxide capacitance is reduced. A number of variables to be considered in selecting the right material include thermodynamic/chemical stability, dielectric constant, band gap, and band offsets.

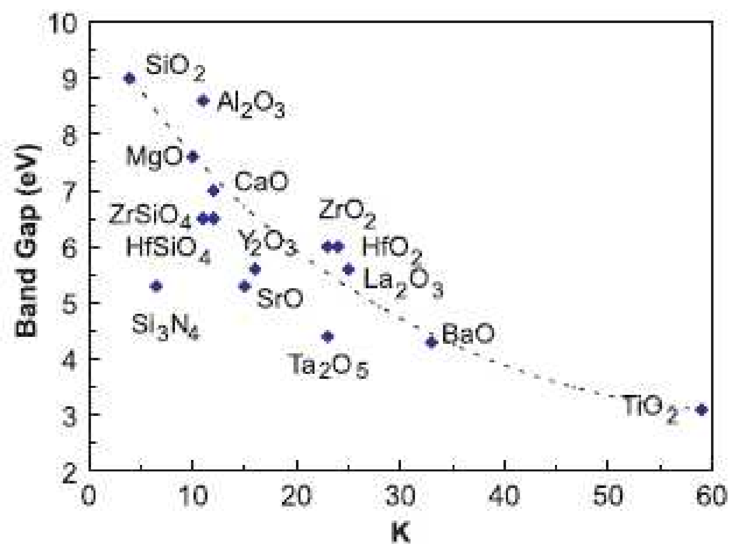

Fig. 1. Energy band gap vs. dielectric constant (K) of various gate oxide materials (After[2]).

HfO_2 (k ~ 25) is a particularly strong candidate due to its thermal stability and high dielectric constant value relative to the other high-k materials [2, 5, 7]. However, it

remains a challenge to form a chemically stable interface between HfO_2 and Si. Hf alloys with lower dielectric constants, e.g., Hf silicates and Hf Si oxynitrides, offer improved interface qualities at the expense of lower dielectric constants, but in the case of the silicates display a chemical phase separation that limits processing temperatures [8]. Phase separation is undesirable because it introduces nano-crystalline HfO_2, which contains grain boundaries that are favorable trap sites for radiation-induced electrons and/or holes [9]. The incorporation of nitrogen in Hf silicate films increases the thermal budget. Thus, the Hf silicate remains homogeneous even after high temperature processes [10]. We will discuss in more detail the charge trapping properties of a homogeneous HfSiON film and one which contains crystalline HfO_2. In addition to improved thermal stability, nitrided surfaces also inhibit dopant diffusion from the substrate [11]. However, metallic Hf-N bonding at the interface can decrease the band gap by reducing band offsets, in turn increasing gate leakage current [11,12]. There are many trade-offs in choosing dielectric materials and fabrication processes. The impacts of these variables on the device electrical characteristics must be analyzed before making the appropriate selection for a high-k MOS system.

While the Si MOS system dominates mainstream microelectronics, it has several limitations. For example, the maximum current drive, as limited by the saturated drain current, is one of the key restricting factors for scaling Si devices. Germanium offers higher electron (4×) and hole mobility (2×) than Si. The higher symmetry of electron and hole mobility in Ge also allows for smaller pMOS area. Therefore, more logic gates can

be implemented in integrated circuits. These characteristics make Ge devices suitable for high speed MOS technologies. In spite of these advantages, there are many challenges for Ge MOS devices. The small band gap of germanium (0.67 eV relative to 1.12 eV for Si) makes Ge MOSFETs vulnerable to band-to-band-tunneling and junction leakage [13]. The much lower melting point of Ge (934°C compared with 1,400°C for Si) also limits processing temperatures [13]. Dopant diffusion is an additional concern, due to the enhanced diffusivity of n-type dopant atoms (P, As, and Sb) in Ge. Another significant issue concerning Ge MOS fabrication is forming a stable interface between the gate dielectric and Ge substrate. GeO_2 is very unstable on Ge, due to its water solubility. GeO_xN_y, on the other hand, forms a much more chemically and thermally stable interface with Ge. The incorporation of nitrogen can also prevent dopant diffusion and reduce hysteresis [14]. Therefore a thin GeO_xN_y interfacial layer may be especially beneficial to Ge MOSFETs with high-k gate dielectrics. However the nitridation process has some drawbacks. For example, insufficiently nitrided or oxidized GeO_xN_y can easily dissolve during deposition, leading to the diffusion of Ge species into the HfO_2 gate oxide [15]. Also, excessive nitridation can increase interface traps and negative fixed charge generation [14]. Dysprosium oxide (Dy_2O_3) is a possible interfacial layer candidate. Dy_2O_3 can eliminate Ge diffusion from the substrate or interlayer. The inclusion of a GeO_xN_y interlayer, which has a relative dielectric constant value of ~ 5-6, lowers the overall capacitance of the gate insulator stack. The capacitance reduction is minimized by using Dy_2O_3 (k ~ 14) as the interlayer. Studies also reported that Si MOS devices with

a gate stack that consisted of laminated Dy_2O_3 on HfO_2 exhibited less bias temperature instability relative to HfO_2/Si devices [16]. These prospects indicate that Dy_2O_3 may be used as an interfacial layer with HfO_2 for Ge MOS applications.

Another important element to consider for the high-k MOS system is the gate material. Polycrystalline silicon (poly-Si) has been the conventional gate material for most Si MOS devices. However, a switch to metal gates is necessary for high-k technology. IBM and Intel announced earlier this year that high-k transistors with metal gates are in the plan for the 45 nm node technology [17]. The deficiencies of the poly-Si gate electrode are amplified as device dimensions become smaller. The poly-Si gate forms an undesirable depletion layer at the gate electrode/gate oxide interface during inversion bias. Therefore additional n^+ or p^+ doping is necessary to offset the depletion effects. The subsequent high temperature dopant activation process steps are unsuitable for high-k dielectric materials. Metals and metallic compounds are much more appropriate as the gate electrodes for high-k MOS applications. Some popular choices include Al, W, Pt, TiN, TaN, and Ta_2O_5 [2, 5, 13]. The crucial consideration in choosing a metal gate material is how well the work function aligns with the Fermi level of the substrate. The metal work function should be within reasonable range from the conduction or valence band of the semiconductor substrate [5].

Total-dose irradiation data on MOS devices with high-k dielectrics are still very limited. Therefore further research on the radiation effects is necessary to evaluate their electrical quality and reliability for potential commercial and space-exploration

applications. In this thesis, the radiation response and bias-temperature effects on MOS devices with Hf-based dielectrics are explored. Chapter II reviews the basic total-dose effects in MOS systems. Chapter III examines the X-ray radiation effects on Ge MOS devices with HfO_2/Dy_2O_3 gate dielectrics. The radiation response of HfSiON on Si MOS devices are presented in chapter IV. Bias-temperature reliability results for the HfSiON devices are discussed in chapter V. Finally chapter VI provides a summary of this work.

CHAPTER II

TOTAL IONIZING DOSE AND ITS EFFECTS ON MOS DEVICES

Total dose irradiation is a fundamental reliability concern for microelectronic devices in space. Radiation-induced charge build-up can degrade device performance and long term reliability. With the advent of new technologies and materials, it is necessary to understand the basic mechanisms of ionizing radiation-induced degradation in MOS devices. This chapter discusses the basic effects of radiation-induced charge buildup in MOS systems, including oxide, interface, and border trapped charges.

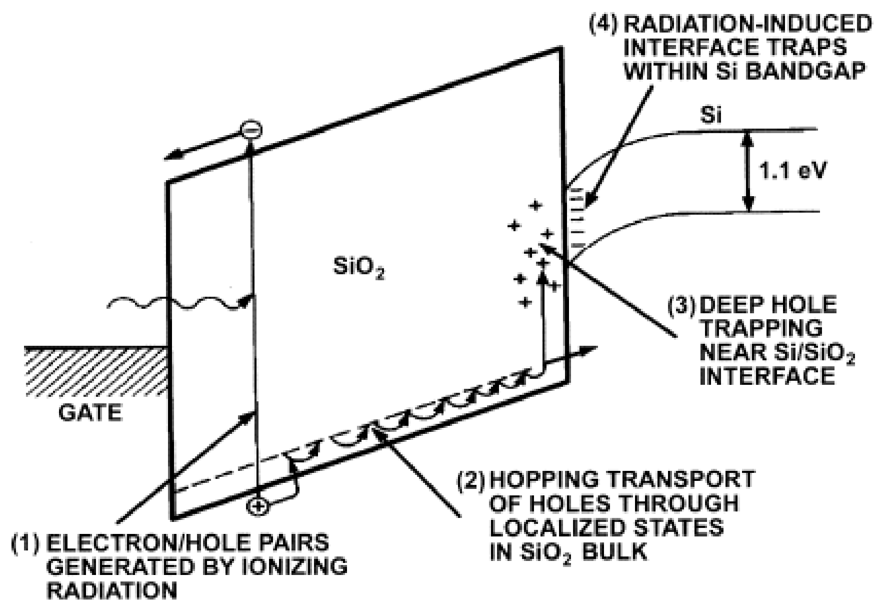

Fig. 2. Schematic energy band diagram of a MOS capacitor under positive gate bias, with physical processes related to radiation-induced electron/hole hairs (After [18]).

Figure 2 shows the schematic energy band diagram of a MOS system under positive bias, and the four main physical processes caused by ionizing radiation. The first process of the radiation response is the generation of electron-hole pairs (EHPs). The positive applied electric field pulls electrons towards the gate and pushes holes to the oxide/Si interface. The majority of electrons are swept out of the oxide due to their high mobilities. Some EHPs recombine in less than ~ 1 picosecond. The larger and less mobile holes that avoid initial recombination remain in the oxide. The ensuing trapped holes determine the initial negative shift of the threshold voltage. Then the trapped holes start to move toward the interface. This process typically takes less than a second, but may continue for several decades of seconds at lower temperatures. Some holes become trapped in deep energy levels in the oxide near the interface – deep hole traps. The final process is the generation of interface traps, which are localized states in the Si bandgap with occupancy that depends on the Fermi level.

Oxide, Interface, and Border Traps

Oxygen vacancies or E' centers are electrically active states in SiO_2 that are primarily responsible for oxide-trapped charges in SiO_2 [19]. The E' centers can be generated by x-rays, γ-rays, electrons, α-particles, holes, high electric fields and ion implantations. Intrinsic E' sites can be activated into the paramagnetic state by irradiation, the application of large electric fields, and/or hole injection. Figure 3 schematically illustrates the precursor and the active state of the E' center in amorphous SiO_2. Studies

have shown that the E'_γ center is the most probable precursor to the formation of the oxide-trapped charge in SiO_2 [20-21].

The most widely accepted model for interface trap formation involves the release and subsequent migration of a hydrogen species toward the SiO_2/Si interface, where reaction occurs with the trivalent Si dangling bond (P_b center) [19-21]. The energy level of interface traps exists within the Si bandgap. The charge of the interface trap depends on the surface potential of the MOS device. Most traps that lie above midgap are acceptorlike; they become negatively charged when filled. Most traps that lie below midgap are donorlike; they become positively charged when filled. Thus radiation-induced interface traps are approximately neutral at midgap.

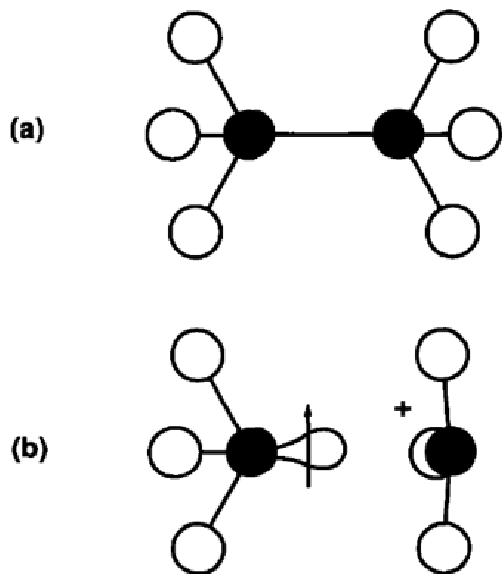

Fig. 3. Schematic diagram of an E'_γ center, showing the characteristic strained Si-Si bond precursor state and the charged EPR active state (After [18]).

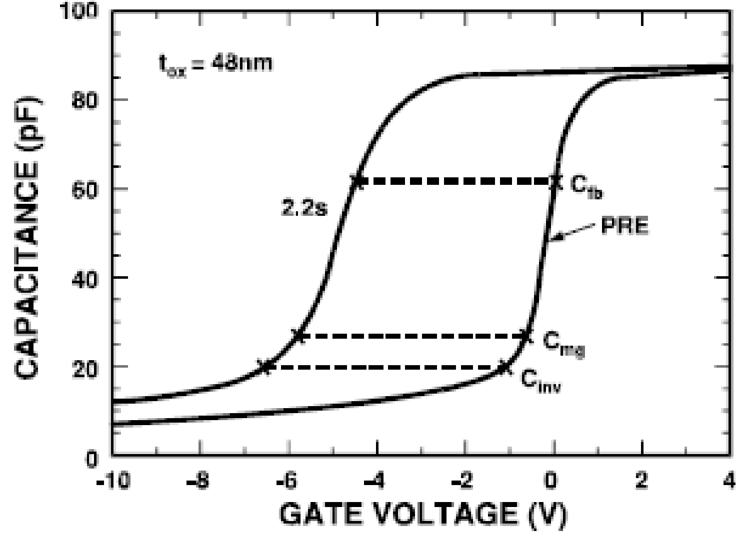

Fig. 4. The Capacitance-Voltage characteristics for a n-substrate capacitor irradiated to 1 Mrad(SiO_2) with V_g = 10 V (After[23]).

The midgap charge separation method is a widely accepted calculation technique for estimating the radiation-induced oxide and interface trap charge buildup. The radiation-induced net oxide-trapped charge density can be estimated by the shifts in the midgap voltages before and after irradiation [22]. The radiation-induced interface trap charge density can be estimated from the stretchout of the Capacitance-Voltage (*C*-*V*) curve [23].

$$\Delta N_{ot} = -\frac{C_{ox}\Delta V_{mg}}{qA} \tag{1}$$

$$\Delta N_{it} = \frac{C_{ox}\Delta(V_{fb} - V_{mg})}{qA} \tag{2}$$

Here ΔN_{ot} and ΔN_{it} are the change in oxide-trapped and interface-trapped charge densities, respectively, C_{ox} is the oxide capacitance, –q is the electron charge, and A is the

capacitor area. The midgap and flatband voltages (V_{mg} and V_{fb}) can be determined from high frequency *C-V* measurements, as illustrated in Fig. 4. This method can also be used to estimate the radiation-induced charge buildup in high-k devices.

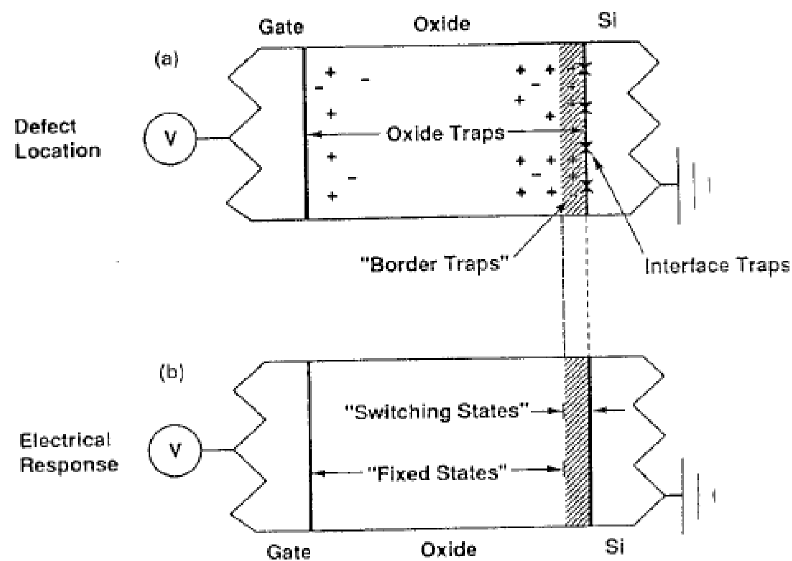

Fig. 5. Schematic diagram showing border traps in a MOS system (After [25]).

In addition to oxide and interface traps, trapped charges located close to the interface have distinct electrical properties that require differentiation. These trapped charges are called border traps since they are located in the bulk oxide region (close to the Si/SiO_2 interface) but remain in communication with the Si substrate, similar to the “border states” in the American Civil War [24]. Oxide-trapped charges are fixed states that do not communicate with the Si substrate. Border traps can easily communicate electrically with the Si substrate by exchanging charge, similar to interface traps. However unlike

interface traps, border traps typically reside within ~ 2.5 nm in the oxide from the Si/SiO_2 interface, as illustrated in Fig. 5. Border traps can significantly impact the radiation response and reliability of MOS devices. The effects include *C-V* hysteresis, enhanced 1/f noise, compensation of trapped holes, and increased thermally stimulated current [24-26]. The role of border traps becomes more significant as devices become smaller. The gate oxides in highly scaled devices are thin enough that any trapped oxide charges can be considered as border traps.

Our understanding of the mechanisms of radiation-induced charge generation/trapping is based on SiO_2 gate dielectrics. These basic mechanisms are similar in many types of high-k materials. For example, oxygen vacancies are most likely responsible for radiation-induced hole trapping in Hf-based MOS devices [9]. Studies have also observed the generation of silicon dangling-bond type defects (P_b) at the Si/HfO_2 interface from stress [27, 28]. Nonetheless, there are differences in the dominant mechanisms for charge trapping in high-k dielectrics that require further investigation. The radiation response of high-k dielectrics is significantly influenced by the material properties and processing techniques. For example, HfO_2 dielectrics have exhibited a tendency to trap more electrons relative to SiO_2 [29]. The charge trapping properties of amorphous and phase-separated Hf silicate films are also significantly different, due to the much higher density of precursor defects in the grain boundaries of nano-crystalline HfO_2 [9]. Spectroscopy tests have estimated defect densities ~ 1×10^{13} cm^{-2} in nano-crystalline HfO_2 [9]. The high pre-irradiation defect density can greatly influence

the radiation response. Since the high-k MOS system is still in its developmental stage, the differences in fabrication processes, like the annealing temperature and ambient, can greatly alter the charge trapping properties. The application of new exotic dielectric materials, such as dysprosium oxide (Dy_2O_3), in HfO_2 on Ge-substrate MOS devices is investigated in this thesis. Results show that the radiation response is significantly influenced by the poor interface quality between the HfO_2/Dy_2O_3 gate dielectric and the Ge substrate. The radiation and bias-temperature effects of HfSiON on Si devices are also discussed. The results show that slight differences in the chemical compositions can result in drastically different charge trapping characteristics in the HfSiON films. The results also reveal that processing techniques can significantly affect the bias-temperature stability of the HfSiON devices.

CHAPTER III

HAFNIUM DIOXIDE ON GERMANIUM

In this chapter, the radiation response of HfO_2/Dy_2O_3 on Ge MOS devices is examined. Germanium devices are attractive for high speed MOS applications, due to the enhanced carrier mobility of Ge relative to Si. Recent developments in high-k dielectrics show that HfO_2 on Ge devices are promising for future highly-scaled MOS technology. Sub-1 nm EOT gate dielectric p-channel HfO_2/Ge MOSFETs that exhibit 2× hole mobility compared with HfO_2/Si control samples have already been reported [30]. However interfacial stability remains an issue for Ge devices. HfO_2 on Ge capacitors with an ultrathin GeO_xN_y interfacial layer fabricated via atomic oxygen beam deposition have shown reasonably good characteristics [31]. However dopant diffusion may still occur if the interlayer is insufficiently nitrided [32]. Dysprosium oxide may be an alternative interfacial layer material as it can eliminate many disadvantages of the nitridation process.

Devices were fabricated at NCSR DEMOKRITOS in Greece using the atomic oxygen beam deposition method. For sample preparation, n-type germanium substrates were annealed at 360°C for 15 min to desorb the native oxide. Dy_2O_3 was deposited at 225 ^{o}C in an O plasma. HfO_2 was then deposited also at 225 ^{o}C, in the O plasma. The gate material is Pt and the backside contact is InGa. The MOS capacitors consist of 10

nm or 5 nm layers of HfO_2 and a 1 nm interfacial layer of Dy_2O_3, on an n-type germanium substrate. The device structure and the energy band diagram for the structure are shown schematically in Fig. 6. The relatively small conduction band offset (1.5 eV, as compared to 3.1 eV for Si/SiO_2) between the Ge and the high-k dielectric layers makes the high-k Ge system exhibit more leakage current. The relative dielectric constants for HfO_2 and Dy_2O_3 are approximately 25 and 12, respectively [33]. The equivalent oxide thicknesses are approximately 1.9 nm and 1.1 nm for the 10 nm and 5 nm HfO_2 devices, respectively.

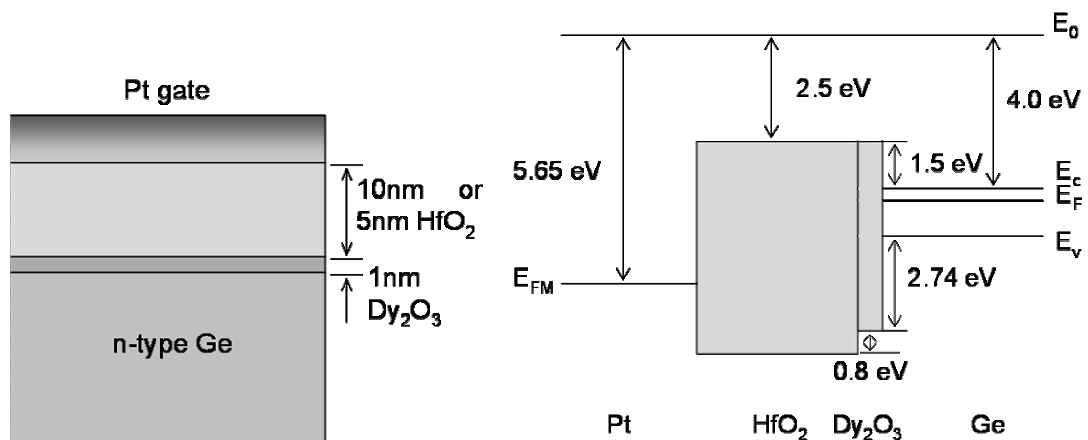

Fig. 6. Device structure and energy band diagram for $Pt/HfO_2/Dy_2O_3$/n-Ge capacitors.

Border Traps

Before irradiation, the hysteresis in the *C-V* curves was significant in the 10 nm HfO_2 sample, with a value of ~ 800 mV at midgap. For the 5 nm HfO_2 capacitors, the hysteresis was considerably less, with a value of ~ 150 mV. These values are

significantly larger than typically found in high quality SiO_2/Si devices. Large hysteresis in HfO_2 during its early development as a dielectric on Ge has been observed in other work. For example, studies on Al/HfO_2/Ge capacitors found hysteresis of ~ 500 mV [34]. More recent studies have shown that an ultrathin GeO_xN_y interfacial layer (approximately 0.3 nm) between HfO_2 and Ge minimized *C-V* hysteresis [14].

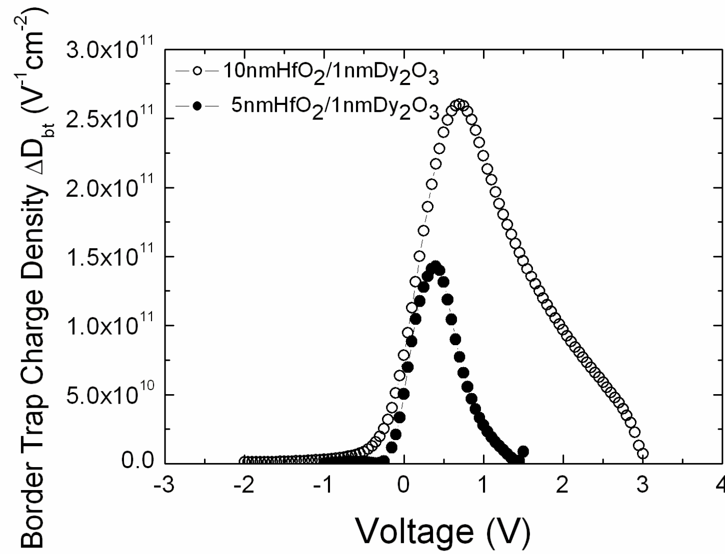

Fig. 7. Border trap densities per unit energy vs. gate voltage for 10 nm HfO_2 and 5 nm HfO_2 devices; the maximum values of ΔD_{bt} are ~ 2.6×10^{11} $V^{-1}cm^{-2}$ and 1.4×10^{11} $V^{-1}cm^{-2}$, respectively.

The large hysteresis values before irradiation likely reflect the relatively easy exchange of electrons with border traps in the HfO_2/Dy_2O_3 gate stack [26]. The large hysteresis also indicates high densities of border traps near the interface. The effective border trap density, ΔN_{bt}, can be calculated by integrating the difference in forward and reverse C-V curves [35]:

$$\Delta N_{bt} \sim (1/qA) \int |C_r - C_f|\, dV. \quad (3)$$

Here –q is the electron charge, A is the capacitor area, and C_r and C_f are the reverse and forward capacitance values. The estimated ΔN_{bt} values are ~ 4.36×10^{11} and 1.05×10^{11} cm^{-2} for the 10 nm and 5 nm HfO_2 devices. Figure 7 plots the border trap densities per unit energy as a function of gate voltage. The border trap density is significantly larger in the 10 nm HfO_2 sample. This indicates that a majority amount of trapped charges reside in the HfO_2 film near the Dy_2O_3/Ge interface. Therefore while Dy_2O_3 may inhibit reactions between the HfO_2 gate oxide and Ge species, the HfO_2/Dy_2O_3 interface is relatively poor, as represented by the high border trap densities.

X-ray Irradiation

The devices were irradiated with an ARACOR 10 keV X-ray source at a dose rate of 31.5 krad(SiO_2)/min. During irradiation the capacitor gates were biased at 1 MV/cm; V_g = 0.7 V for the 10 nm HfO_2 capacitors and V_g = 0.3 V for the 5 nm HfO_2 devices.

Figures 8 and 9 show the irradiation effects on these devices. We observed no measurable change in the *C-V* characteristics after exposure to 10 Mrad(SiO_2) for the 5 nm HfO_2 and 30 Mrad(SiO_2) for the 10 nm HfO_2 samples. The lack of change in net oxide-trap charge with irradiation may reflect a balance of electron and hole trapping in the gate dielectric, similar to what has been reported for HfO_2 based gate stacks on Si [29]. However, it seems more probable that charge neutralization via the relatively higher gate leakage currents is the dominant cause for the lack of change in net oxide-trap

charge for such thin gate dielectrics.

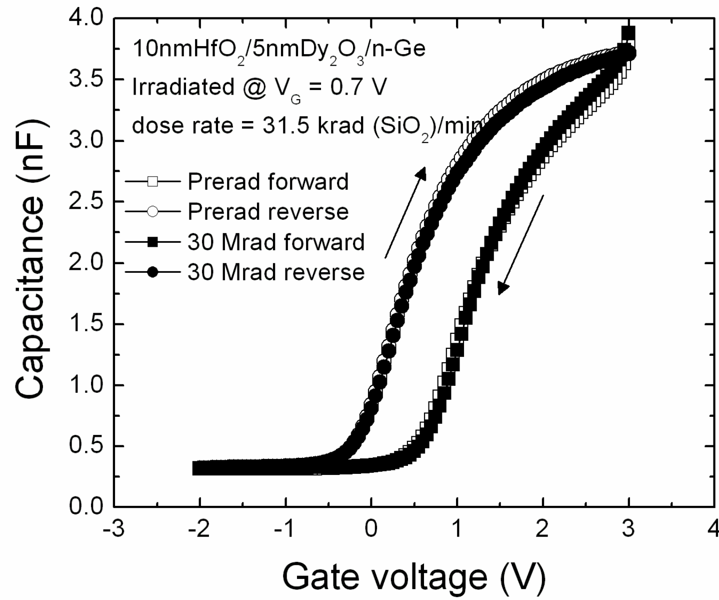

Fig. 8. 1 MHz C-V characteristics for 10 nm HfO_2/1 nm Dy_2O_3/n-Ge capacitor after irradiated to 30 Mrad(SiO_2) with $V_g = 0.7$ V during irradiation.

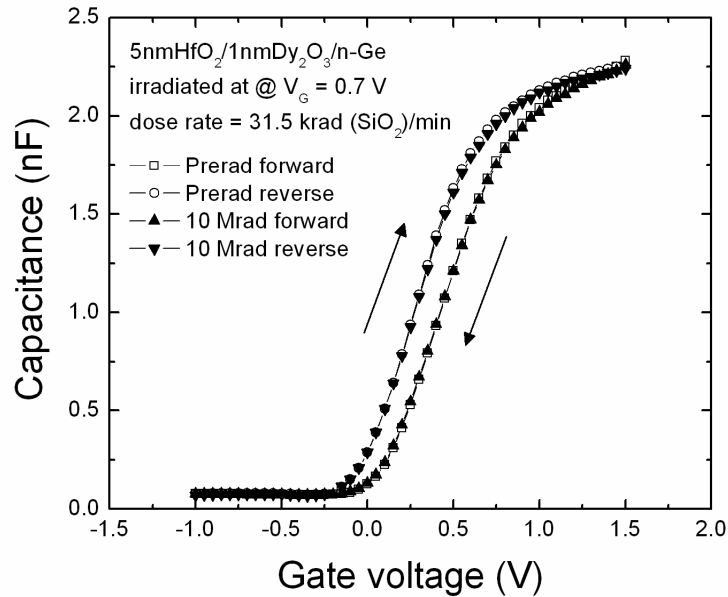

Fig. 9. 1 MHz C-V characteristics for 5 nm HfO_2/1 nm Dy_2O_3/n-Ge capacitor after irradiated to 10 Mrad(SiO_2) with $V_g = 0.3$ V during irradiation.

Gate Leakage Current

The gate leakage currents of these HfO_2 devices are higher than typical levels observed for SiO_2 on Si of similar physical gate oxide thickness, owing to the relatively small barrier height (Fig. 1). However, the current levels are much smaller compared to SiO_2/Si devices of equivalent oxide thicknesses (EOT ~ 1.1 and 1.9 nm). The *I-V* characteristics of these devices at V_g = 1 V (~ V_{fb} + 1 V) are shown in Fig. 10. The horizontal lines indicate the leakage levels for SiO_2/Si devices of equivalent gate oxide thicknesses biased at V_g = 1.5 V. For the 10 nm HfO_2 capacitors, $J_g = 5.17 \times 10^{-7}$ A/cm^2. The gate leakage current for the 5 nm HfO_2 capacitors is significantly higher, where $J_g = 8.7 \times 10^{-4}$ A/cm^2, owing primarily to electron tunneling. These gate current densities are reasonable for such thin effective oxide thicknesses; however, the current is high enough that gate current will neutralize efficiently any net positive oxide-trap charge. This neutralization will also occur for ultrathin SiO_2 when gate tunnel currents are high.

Figure 11 compares the gate leakage of devices in this report with various high-k dielectrics on Ge MOS devices. The leakage current for the 10 nm HfO_2 devices (EOT ~ 1.9 nm) in this work is comparable to the leakage current observed for HfO_2/Ge devices with ultrathin GeO_xN_y interfacial layers [14, 30]. The leakage for the 5 nm HfO_2 devices is slightly higher than the HfO_2/GeO_xN_y structure, which indicates the increased levels of degradation of the HfO_2/Dy_2O_3 and Ge interface. Nonetheless, the gate leakage currents for the HfO_2/Dy_2O_3/Ge devices here are comparable to recently reported leakage levels for the HfO_2/GeO_xN_y/Ge structure, which suggests that Dy_2O_3 can be incorporated with

HfO_2 without causing much of an increase in gate leakage current.

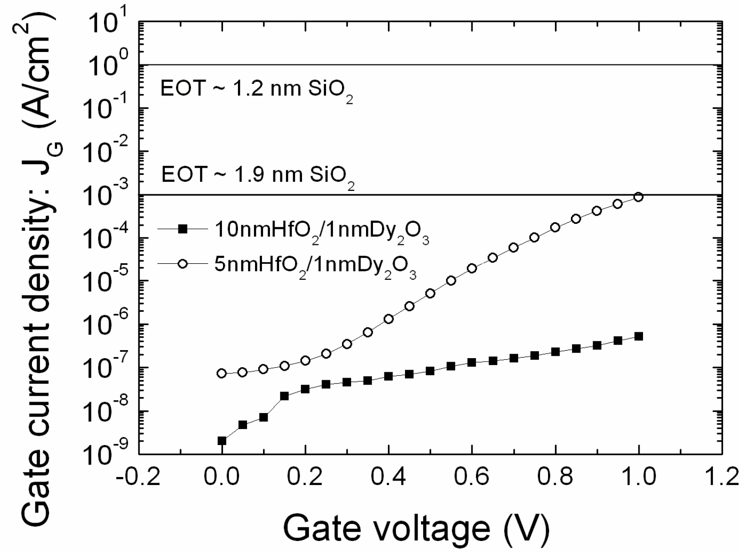

Fig. 10. Gate leakage current density vs. gate voltage for the 10 nm and 5 nm HfO_2 devices; $J_G = 5.17 \times 10^{-7}$ A/cm^2 and 8.7×10^{-4} A/cm^2 at 1 V, respectively. Horizontal lines indicate leakage levels for SiO_2 devices of similar EOT.

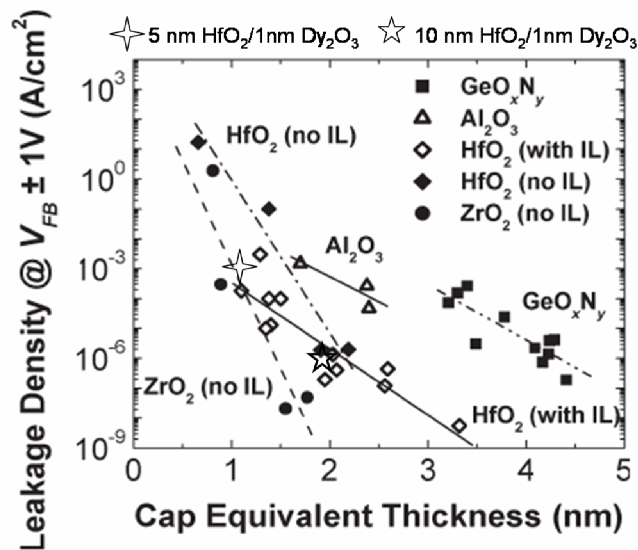

Fig. 11. Benchmark gate leakage levels for various high-k dielectrics on germanium MOS devices (After[14]).

Incorporating Dy_2O_3 as a barrier layer between the Ge and the HfO_2 may also help to reduce charge trapping. Electrical measurements of Si MOSFETs with various combinations of Dy_2O_3 and HfO_2 were reported in [16]. However, the devices exhibiting the lowest leakage current in [16] were MOSFETs with a Dy_2O_3 layer stacked on top of the HfO_2, which was in contact with the Si substrate. This contrasts with the devices considered here, in which the Dy_2O_3 layer is in contact with the substrate. Comparisons between devices of different Dy_2O_3 and HfO_2 layer thicknesses showed that the thinner Dy_2O_3 layer, with Dy_2O_3/HfO_3 thicknesses of 18/26 Å produced the smallest gate leakage [16]. Bias-temperature stability experiments performed on those devices showed that the Dy_2O_3/HfO_2 structure had smaller shifts in threshold voltage compared with HfO_2 devices of equal EOT.

Since HfO_2 has been known to trap high densities of electrons after X-ray irradiation, the balance of electron and hole trapping may partly contribute to the lack of change in the *C-V* characteristics after irradiation [29]. However, the neutralization of the radiation-induced charge build-up via the high gate leakage current is likely the more dominant mechanism. Although the gate leakage current levels for these devices are similar to HfO_2/Ge devices with other interfacial layers, like GeO_xN_y, the high border trap densities indicate that the interface quality between the HfO_2/Dy_2O_3 gate dielectric and Ge substrate is relatively poor [14]. Further research is necessary to form a higher quality interface with much reduced gate leakage current, border trapped charge density, and pre-irradiation interface trapped charge density.

CHAPTER IV

HAFNIUM SILICON OXYNITRIDE ON SILICON

This chapter explores the effects of X-ray radiation on HfSiON on Si MOS devices. HfSiON offers improved thermal stability and interfacial quality relative to HfO_2, while maintaining a relatively high dielectric constant value. The incorporation of nitridation further improves thermal stability by preventing dopant diffusion from the substrate. The higher thermal budget keeps the HfSiON film amorphous during high temperature anneals. Phase separation, which can occur at very high processing temperatures (>900°C), degrades the film quality by introducing grain boundary defects [9]. We examine the total dose irradiation and bias-temperature instabilities of a homogeneous HfSiON film and one which contains nano-crystalline HfO_2. We also compare the charge trapping behavior with previous Hf silicate [36] and HfO_2 devices [29, 37-38].

Device Processes

The devices here are MOS capacitors with aluminum front and back contacts, Hf Si oxynitride dielectrics, and p-type silicon substrates. The device cross section is shown schematically in Fig. 12. The devices were fabricated at North Carolina State University. The Hf/Ti source gases, 2% SiH_4 in He, and Hf(IV)/Ti(IV) *t*-butoxide were deposited using remote plasma enhanced chemical vapor deposition (RPECVD). Two different Hf

Si oxynitride pseudoternary alloys were integrated into these devices on nitrided, plasma-oxidized interfaces (e.g., SiON). These SiON interfacial layers are ~ 0.6 nm. After deposition, rapid thermal annealing (RTA) for ~ 1 minute in Ar was performed at 900 ^{o}C. The samples were packaged in 28-pin dual inline packages at Georgia Tech. The dielectric constant (*k*) for the low-Si_3N_4 ($Hf_{0.6}SiO_{0.2}N_{0.2}$) and high-Si_3N_4 ($Hf_{0.3}SiO_{0.4}N_{0.4}$) content alloy films are k = 14.6 and k = 12.7, respectively [8]. The low-Si_3N_4 content film contains crystalline HfO_2, while the high-Si_3N_4 content film is homogeneous [8]. The devices in this study have physical oxide film thicknesses of ~ 15 nm (EOT ~ 4 nm) and 2 nm (EOT ~ 0.5 nm).

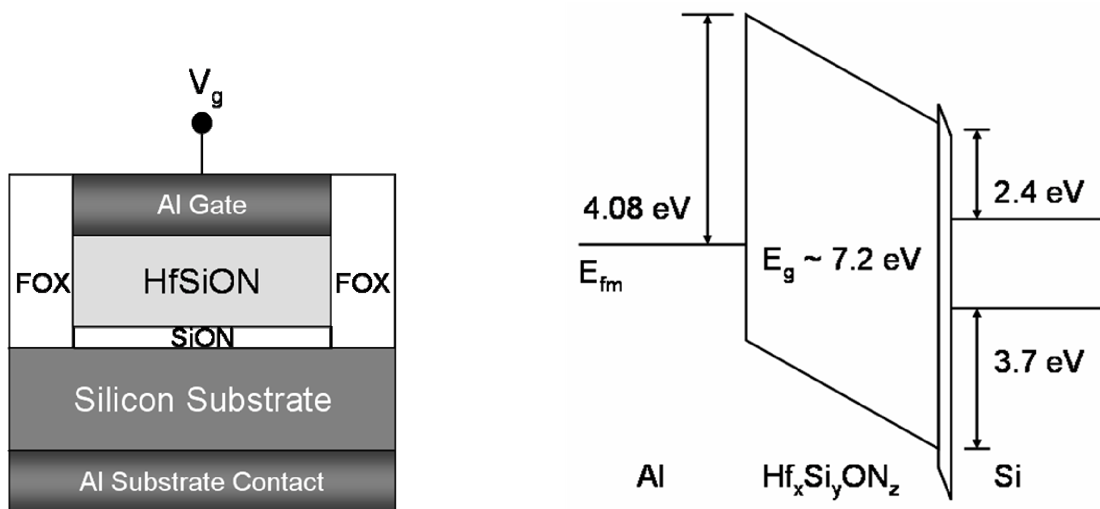

Fig. 12. Device structure and energy band schematic diagrams for Al/HfSiON/Si MOS capacitors.

Pre-irradiation characteristics

The pre-irradiation *C-V* characteristics showed considerable hysteresis in the thicker

devices (ΔV_{mg} ~ 150 mV and 200 mV for the high- and low-Si_3N_4 films, respectively). The hysteresis for a 15 nm low-Si_3N_4 content device is shown in Fig. 13. The hysteresis indicates a relatively high density of process-induced border traps [26]. The effective border trap densities (ΔN_b) are calculated from equation (3). The estimated ΔN_{bt} values are ~ 2.7×10^{11} cm^{-2} and 3.3×10^{11} cm^{-2} for the high- and low-Si_3N_4 devices, respectively. There is no measurable hysteresis in the 2 nm devices. There is also significant pre-irradiation interface trap charge density (N_{it} ~ 4×10^{12} cm^{-2}) in the 15 and 13 nm gate oxide devices. The pre-irradiation N_{it} is much smaller (N_{it} ~ 5×10^{11} cm^{-2}) in the 2 nm devices.

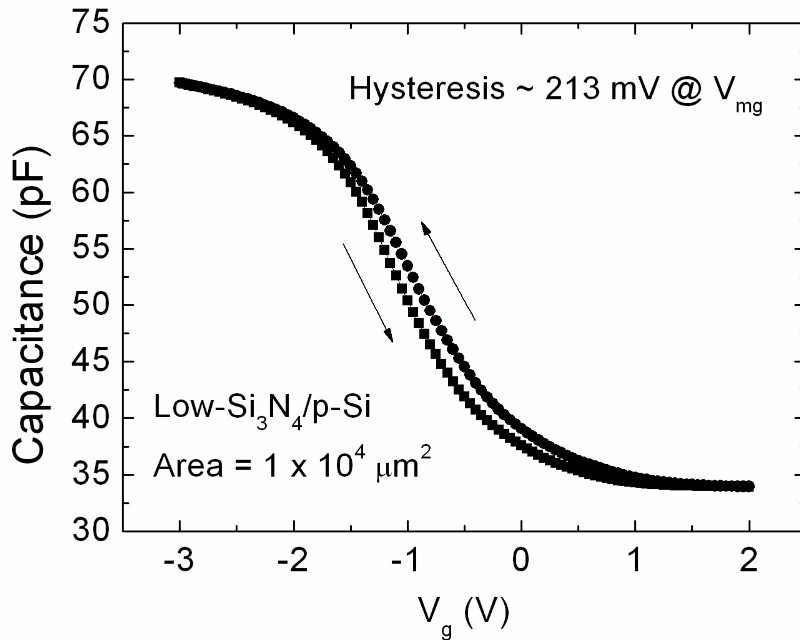

Fig. 13. 1-MHz capacitance-voltage characteristics for a 15 nm low-Si_3N_3 ($Hf_{0.6}Si_{0.2}ON_{0.2}$) film p-substrate MOS capacitor swept from accumulation to inversion and inversion to accumulation. The hysteresis is ~ 213 mV at midgap.

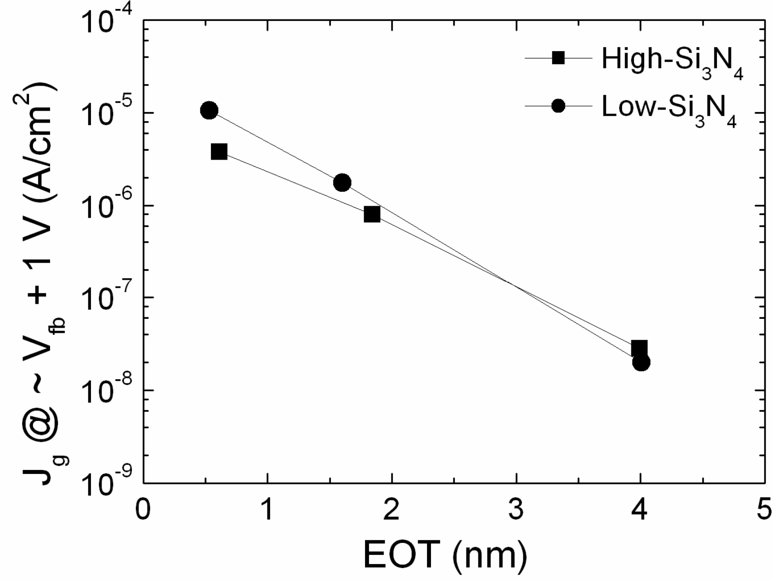

Fig. 14. Gate leakage current density (J_g) at V_{fb} + 1 V for low- and high-Si_3N_4 HfSiON devices with physical film thicknesses ~ 15, 6, and 2 nm.

The gate leakage is significantly reduced in high-k devices for equivalent oxide thicknesses relative to SiO_2 devices, owing to the physically thicker high-k gate oxides. However the smaller band gap increases electron tunneling, and the higher density of pre-irradiation interface traps induces larger trap-assisted tunneling. The band gap of HfSiON films ~ 7 – 8 eV (SiO_2 E_g ~ 8.9 eV). The small conduction band offset (ΔE_{cb} ~ 2.4 eV) makes electron tunneling more likely than in SiO_2 devices (ΔE_{cb} ~ 3.7 eV).

Figure 14 illustrates the gate leakage current densities at V_{fb} + 1 V for the low- and high-Si_3N_4 devices of various film thicknesses. The gate leakage for films of EOT = 2 nm is approximately 5 orders of magnitude less than in SiO_2 devices of equivalent electrical thickness. This demonstrates the main advantage of these devices relative to SiO_2 devices.

Also, the low- and high-Si_3N_4 films exhibit similar levels of gate leakage current for the thicker oxide devices. However, the low-Si_3N_4 film shows slightly higher leakage for thinner films. The higher density of defect states in the low-Si_3N_4 devices produces higher trap-assisted tunneling current [39], which is more significant in the thinner oxide devices.

X-ray Irradiation

The 15-nm low- and 13-nm high-Si_3N_4 content HfSiON capacitors were irradiated with various gate biases. Neither the hysteresis nor the gate leakage current changes significantly with radiation. Figure 15 shows the *C-V* characteristics of the 15-nm low-Si_3N_4 device with irradiation bias V_g = 0 V. The flatband voltage shifts (ΔV_{fb}) and midgap voltage shifts (ΔV_{mg}) were nearly identical for all bias conditions and all devices. Thus, radiation-induced changes in the *C-V* characteristics were predominantly due to radiation-induced oxide-trapped charge. The lack of significant change in interface trap density with irradiation most likely is due to the large pre-irradiation interface trap density in the 13- and 15-nm gate oxide devices.

Figure 16 shows ΔV_{mg} as a function of dose for the 15-nm low-Si_3N_4 devices irradiated to 5 Mrad(SiO_2) under various bias conditions. We observe similar changes in ΔV_{mg} for gate biases ranging from –1.5 to 1 V, with larger positive shifts occurring for gate biases of 1.5 and 2 V. The lack of significant bias dependence at moderate gate biases suggests a relatively uniform distribution of bulk charge traps, similar to previous

work on hafnium silicate films [36]. The charge centroid is not affected significantly at low electric fields due to the low mobility of holes in hafnium silicate and/or high bulk oxide-trap density [40]. The similar levels of ΔV_{mg} for devices irradiated with different biases may also be the consequence of a balance of electron and hole trapping in these nitrided Hf silicates. Previous work has shown that HfO_2 dielectric films are more susceptible to electron trapping than SiO_2 due to the large pre-irradiation bulk trap density [38]. Also, nitrided SiO_2 is known to contain both electron and hole traps [41, 42].

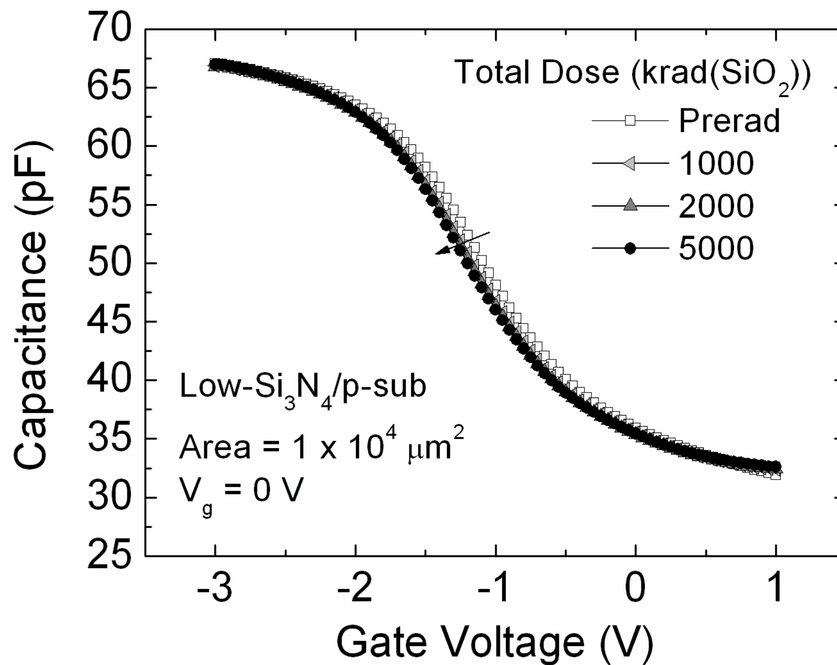

Fig. 15. 1-MHz capacitance-voltage characteristics for a p-substrate low-Si_3N_3 ($Hf_{0.6}Si_{0.2}ON_{0.2}$) film MOS capacitor irradiated with $V_g = 0$ V to 5 Mrad(SiO_2).

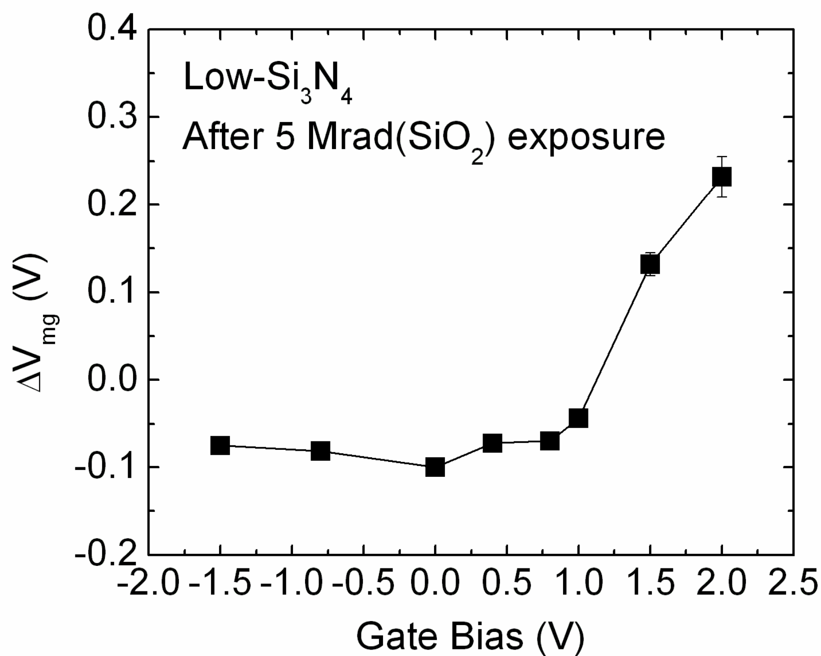

Fig. 16. ΔV_{mg} as a function of gate bias during irradiation for 15 nm low-Si_3N_4 ($Hf_{0.6}Si_{0.2}ON_{0.2}$) Si MOS capacitors irradiated to 5 Mrad(SiO_2).

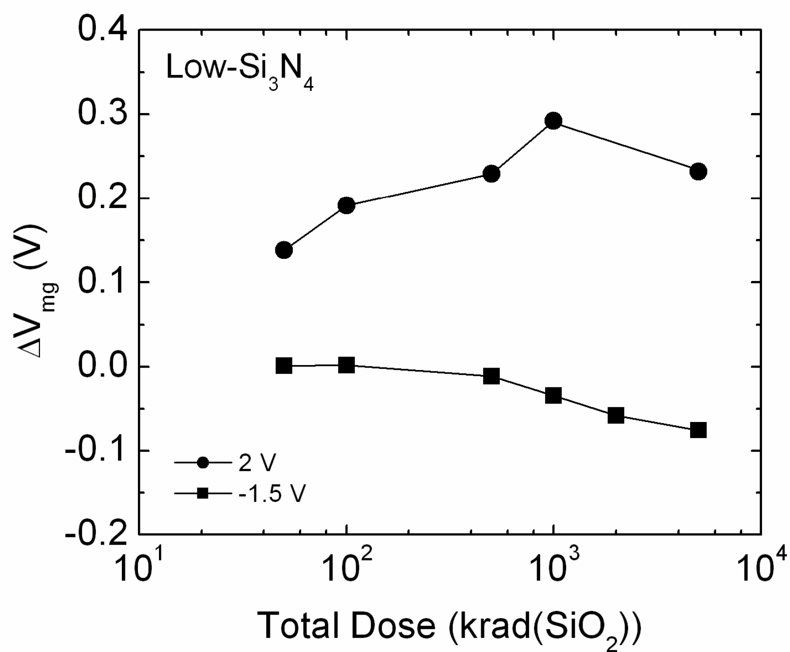

Fig. 17. ΔV_{mg} vs. total dose for 15 nm low-Si_3N_4 ($Hf_{0.6}Si_{0.2}ON_{0.2}$) Si MOS devices irradiated to 5 Mrad(SiO_2), with V_g = 2 and -1.5 V during irradiation.

The exceptions to the lack of bias dependence occur only at higher positive bias conditions (1.5 and 2 V). Figure 17 shows ΔV_{mg} vs. total dose for positive and negative bias conditions. The value of ΔV_{mg} decreases monotonically for the negatively biased device, indicating net positive charge in the oxide. In contrast, the positively biased device shows primarily electron trapping, although the turnaround at higher doses shows that the net positive shift reflects an increasing amount of hole trapping relative to electron trapping at the highest doses.

At the higher positive voltages during irradiation, the Si surface layer is in inversion, and significant electron tunneling occurs. Constant voltage stress (CVS) experiments revealed that electron injection during irradiation causes significant amounts of electron trapping at the higher dose levels, due to the additional time under bias for these (but not lower) bias conditions. The net electron trapping in Fig. 17 under large positive bias is a combination of electron injection and radiation-induced charge trapping. These combined effects are increasingly important in thin high-k dielectric layers [38, 43].

Figures 18 and 19 compare the total-dose responses of the low- and high-Si_3N_4 films with positive and negative irradiation biases. The radiation responses of the films are similar for the negative bias case; the low-Si_3N_4 films show slightly enhanced levels of charge trapping relative to the high-Si_3N_4 film. However, the positively biased devices behaved differently: the high-Si_3N_4 film did not exhibit significant levels of electron trapping after irradiation, so the midgap voltage shift was negative due to net positive charge trapping.

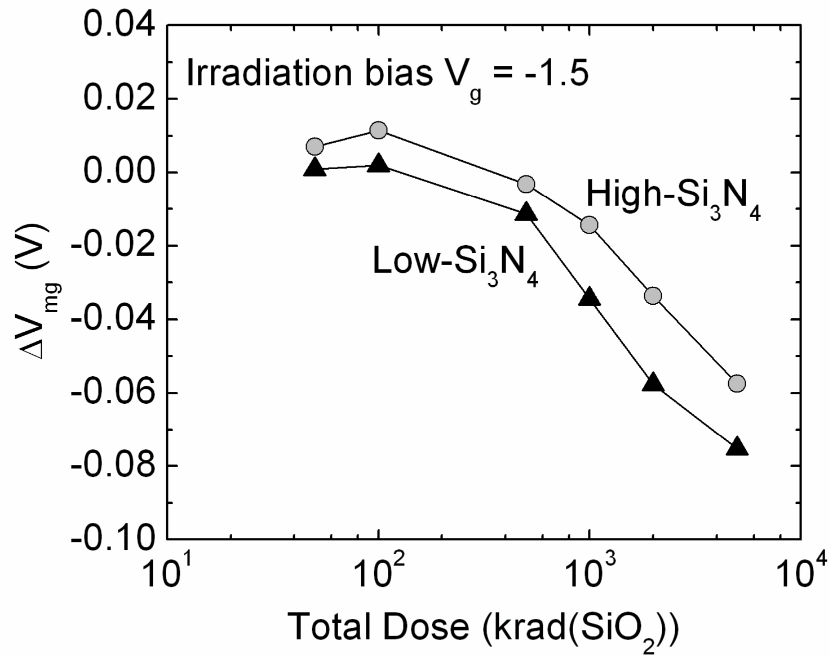

Fig. 18. ΔV_{mg} vs. total dose for 15-nm low-Si_3N_4 ($Hf_{0.6}Si_{0.2}ON_{0.2}$) and 13-nm high-Si_3N_4 ($Hf_{0.3}Si_{0.4}ON_{0.4}$) Si MOS devices irradiated to 5 Mrad(SiO_2) with V_g = -1.5 V.

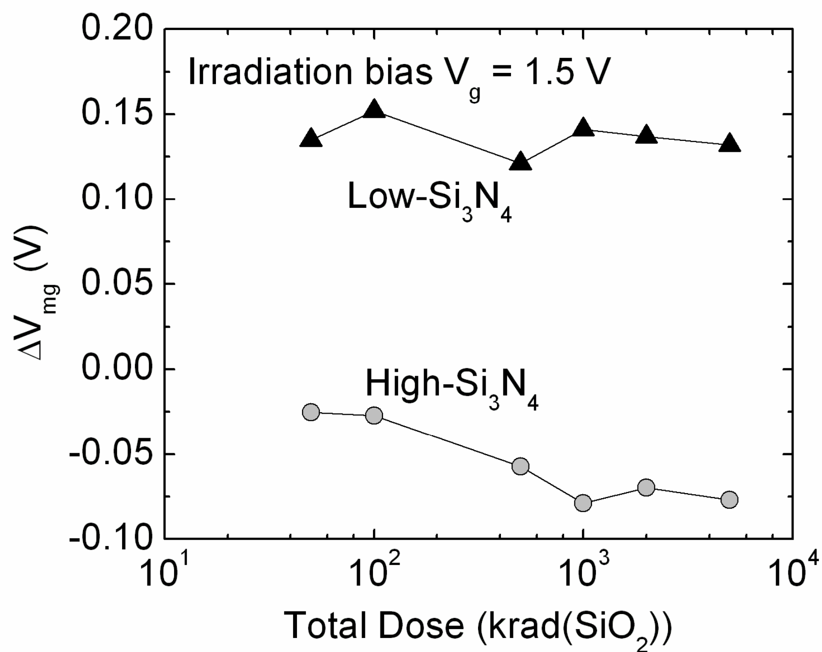

Fig. 19. ΔV_{mg} vs. total dose for 15-nm low-Si_3N_4 ($Hf_{0.6}Si_{0.2}ON_{0.2}$) and 13-nm high-Si_3N_4 ($Hf_{0.3}Si_{0.4}ON_{0.4}$) Si MOS devices irradiated to 5 Mrad(SiO_2) with V_g = 1.5 V.

Constant Voltage Stress

As demonstrated from the irradiation results, a significant amount of electron trapping occurs in the low-Si_3N_4 films only at relatively high positive gate biases during irradiation. CVS tests show that the positive gate bias induces considerable electron trapping via electron injection from the substrate. Figure 20 shows ΔV_{mg} vs. time for the low-Si_3N_4 film under various positive biases. Clearly, the amount of electron trapping is larger for higher stress voltages. In addition, the initial increase in ΔV_{mg} makes up the majority of the total shift. The sudden increase in ΔV_{mg} after the initial stress interval of ~ 100 s is followed by more gradual increases with stress time. This may be due to the presence of a higher density of defects near the high-k/Si interface. The HfSiON/Si MOS structure contains a thin interfacial layer of SiON between the high-k film and Si substrate. High densities of defects such as O vacancies are ideal trap sites for electrons/holes in these nitride-rich oxynitride layers [9, 44]. Electrons fill these traps before reaching the trap sites located deeper in the bulk oxide. The band diagram in Fig. 21 illustrates the electron trapping from substrate injection under positive gate bias. Negative gate voltages did not cause hole injection since the barrier height for hole tunneling is higher than for electrons. The valence band offset for HfSiON and Si is ~ 3.7 eV, whereas the conduction band offset is ~ 2.4 eV.

Figure 22 demonstrates the CVS data of the high- and low-Si_3N_4 devices stressed for times varying from 1 to 10^5 seconds. We observe large initial ΔV_{mg} even after 1 s. There is also a large increase in ΔV_{mg} after 10^4 s, as the injected electrons fill the bulk oxide traps.

These results are consistent with the injected electrons filling the traps near the oxynitride interfacial layer before reaching the bulk oxide traps.

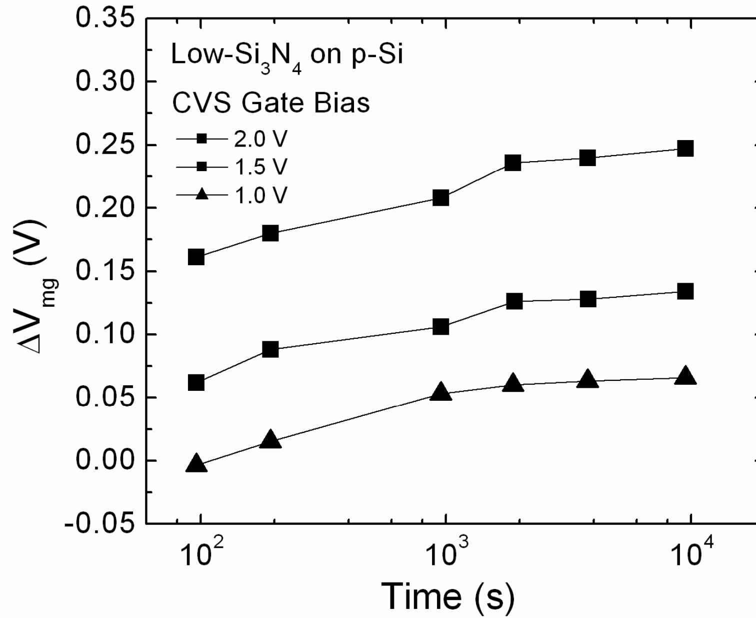

Fig. 20. ΔV_{mg} vs. stress time for 15-nm low-Si_3N_4 ($Hf_{0.6}Si_{0.2}ON_{0.2}$) Si MOS devices stressed with $V_g = 1$, 1.5, and 2 V at room temperature.

Additionally the *C-V* characteristics showed no significant change in interface trap densities after CVS. This result differs from previous work on p-substrate HfO_2 capacitors that showed significant interface trap formation after CVS [38]. However the HfO_2 devices in that work had much lower pre-irradiation interface trap charge density ($N_{it} < 1 \times 10^{11}$ cm^{-2}) than the devices here [38]. The nitride layers prevent H diffusion into the interfacial transition regions, thereby inhibiting interface trap formation; however, this may also limit one's ability to passivate Si dangling bonds at the interface during

processing [11],[22].

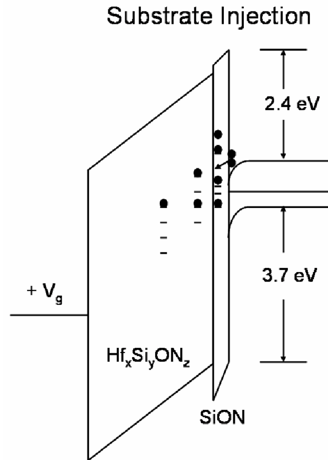

Fig. 21. Energy band diagram illustrating substrate electron injection for a p-substrate device under positive gate bias.

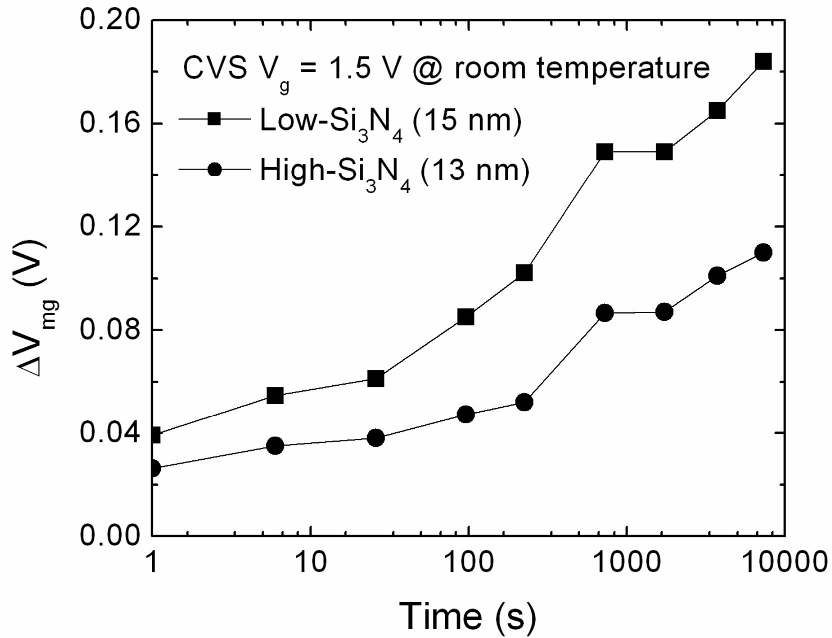

Fig. 22. ΔV_{mg} vs. stress time for 15-nm low-Si_3N_4 ($Hf_{0.6}Si_{0.2}ON_{0.2}$) and 13-nm high-Si_3N_4 ($Hf_{0.3}Si_{0.4}ON_{0.4}$) Si MOS devices with V_g = 1.5 V during constant voltage stress at room temperature.

The differences in the chemical structures of the two films evidently cause the differences in the radiation and CVS results. The high-Si_3N_4 content film chemically phase separates after 900°C annealing, containing crystalline HfO_2 and non-crystalline SiO_2 [8]. Crystalline HfO_2 contains grain boundaries that behave as electron trap sites [40]. The increased electron trapping in crystalline HfO_2 is primarily associated with O vacancies, which are clustered at internal grain boundaries [9]. Conversely, the high-Si_3N_4 content film remains non-crystalline after the 900°C anneal and contains fewer trap sites due to the absence of grain boundary defects. The reduced defect generation rate under X-ray irradiation is similar to SiO_2, consistent with a chemical self-organization that minimizes percolation of bond-strain preventing chemical phase separation [8]. Thus, the high-Si_3N_4 content film exhibits reduced charge trapping even at high positive bias conditions.

Comparison with Hf silicate

Figure 23 compares the worst-case irradiation results for the HfSiON devices with Hf silicate devices from a previous study [36]. The ΔV_{mg} curves of the Hf silicate devices in Fig. 12 are linear fits from data reported in [36]. They have similar dimensions (area = 1 $\times 10^{-4}$ cm^2 and EOT = 4.5 nm) as the HfSiON devices here. The Hf silicate devices also had a high pre-irradiation interface trap density ($N_{it} \sim 2 \times 10^{12}$ cm^{-2}). They displayed large C-V hysteresis (> 100 mV) after baking at 150°C [36]. These similar qualities allow for a fair comparison of their radiation responses.

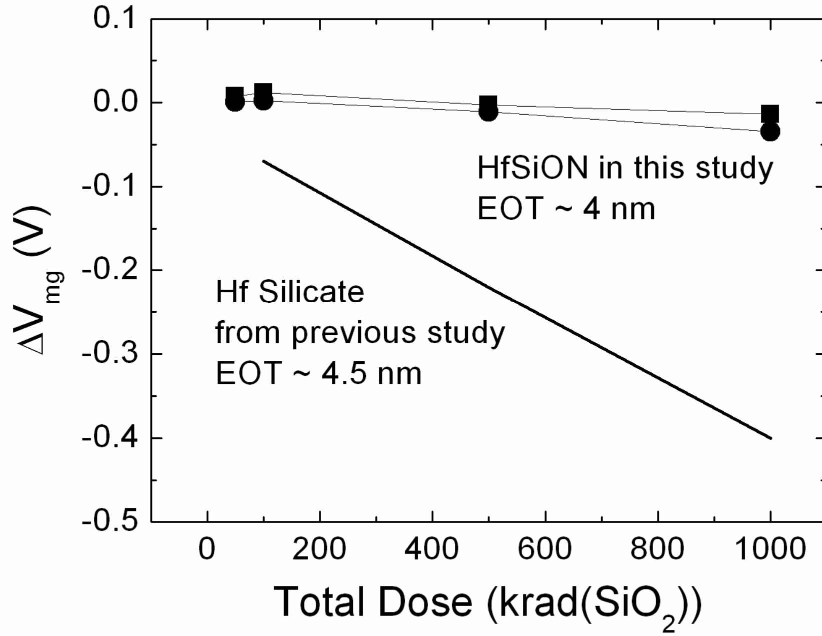

Fig. 23. ΔV_{mg} vs. total dose for the HfSiON devices (EOT = 4 nm) in this report and Hf silicate devices from a previous study [36] (EOT = 4.5 nm) with the same capacitor areas.

The radiation-induced net oxide-charge densities (ΔN_{ot}) as projected to the Si/SiO_2 interface were estimated from equation (1). After exposure to a total dose of 1000 krad(SiO_2) with V_g = -1.5 V, $\Delta N_{ot} = 7.7 \times 10^{10}$ cm^{-2} and 2.1×10^{11} cm^{-2} for the high- and low-Si_3N_4 content devices, respectively, while $\Delta N_{ot} = 1.2 \times 10^{12}$ cm^{-2} for the Hf silicate devices [36]. Hence, the amorphous high-Si_3N_4 film displays ~ 16× less ΔN_{ot} relative to the Hf silicate devices in [36]. With the exception of electron trapping at the highest applied electric fields, the low-Si_3N_4 content film still demonstrates improved charge trapping characteristics relative to the Hf silicate films, with ΔN_{ot} ~ 5.7× less, despite the presence of nano-crystalline HfO_2 grains. The high-Si_3N_4 content film is similar to a Hf silicate film due to its amorphous structure. However, the improvement exhibited by the

low-Si_3N_4 content films relative to the Hf silicate films is noteworthy, since crystalline HfO_2 has higher defect density and greater charge trapping than high quality Hf silicates [9].

The large pre-irradiation interface-trap density strongly affects the irradiation results in both the HfSiON devices here and the Hf silicate devices from [36]. The effects of the high pre-irradiation N_{it} are similar to the saturation of interface traps at higher doses in SiO_2 due to the exhaustion of precursor defects [44]. Nevertheless the sizeable reduction in the radiation-induced net oxide-trap charge indicates the advancement in fabrication processes of Hf alloy MOS devices since 2002, when results for an earlier generation of Hf silicate devices were reported [36]. The results indicate the promise of nitrided Hf silicates for potential future use in radiation environments. Furthermore, the HfSiON on Si devices showed superior pre-irradiation characteristics relative to the HfO_2 on Ge devices, such as reduced gate leakage current, border trap and interface trap densities. As a result, the pre-irradiation characteristics have less influence on the radiation response for the HfSiON on Si devices.

CHAPTER V

BIAS-TEMPERATURE INSTABILITY

Negative bias temperature instability (NBTI) is an important reliability concern for ultrathin gate oxide MOS devices. The applied bias at elevated temperatures induces interface traps and oxide trapped charges that affect the device threshold voltage and long term reliability [45]. Negative bias temperature instability (NBTI) is especially a concern for pMOS devices [46]. Previous experiments on SiO_2 and HfO_2 on Si MOS devices show positive interfacial and oxide charge generation [29, 37]. The mechanism for NBTI is still under debate [47]. However, a newly developed model that is especially relevant for relatively low fields and thin oxides [45, 48] involves the release and movement of hydrogen species to the interface. The mechanism proposes the depassivation of dangling bonds through the removal of H from P-H bonds. The stability of P-H bonds decrease as the n-type Si surface is biased to depletion. The H's trapped in P-H complexes are released at elevated temperature. The H's that migrate to the inversion layer become positively charged (H^+), and are swept to the interface. Some H^+ species overcome the barrier to SiO_2, and subsequently results in the buildup oxide-trapped charges.

We investigate the reliability of the HfSiON devices with bias temperature stress experiments. Bias temperature instability was observed to be more pronounced and more consistent in the 2 nm HfSiON films. Therefore, the following discussion focuses on

results of these thinner films.

Baking Effects

First we examine the effects of baking on the Hf silicate samples. As a part of the packaging procedure for drying the silver paste adhesive, the devices were baked at ~ 200°C for several hours after wire-bonding. The baking process can affect the pre-irradiation characteristics. In order to examine the effects of baking, some devices were left unbaked during the packaging process. These devices were first characterized via *C-V* measurements, then baked at various temperatures with different bias conditions (V_g = 0, -1.22 V, or floating). The devices were then treated with an additional bake at 200°C for 1 hour, unbiased. Figure 24 shows the ΔV_{mg} after each bias-temperature stress and after the 200°C anneal. The ΔV_{mg} increases after each bias-temperature stress for all devices. However, the device with V_g = -1.22 V showed larger magnitude increases in ΔV_{mg} relative to the devices with V_g grounded or floating. Additionally a turnaround in ΔV_{mg} is observed for the negatively biased device, but not for the other devices (V_g grounded or floating), after the 200°C (unbiased) annealing. This suggests a decrease in the Hf silicate pre-irradiation defect densities with increasing annealing temperature. Electron trapping via gate injection likely contributes to the total change in ΔV_{mg} for the negatively biased device. The stress-induced trapped electrons recombine and/or escape from the oxide during the unbiased bake at 200°C; as a result, the magnitude of ΔV_{mg} for the negatively biased device returns to similar levels as the other devices. The voltage

shifts for all devices saturate after baking at 200°C (unbiased) for an additional 30-60 minutes (not shown). The voltage shifts from baking the devices are significant with ΔV_{mg} ~ 200 mV, which corresponds to ΔN_{ot} ~ 1.2×10^{12} cm^{-2}. The results indicate a high density of post-process positive oxide-trapped charges that are neutralized via recombination with electrons after baking at temperatures up to 200°C.

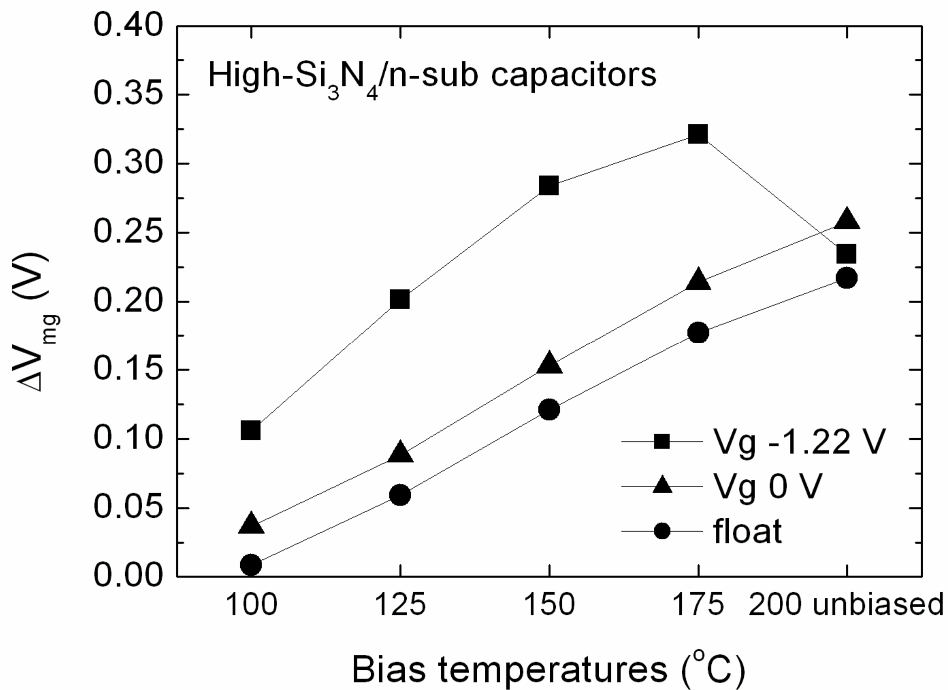

Fig. 24. ΔV_{mg} for high-Si_3N_4/n-substrate capacitors temperature-stressed (V_g = -1.22 V, 0 V, and floating), and annealed at 200°C unbiased for 1 hour.

Bias-temperature stress

Bias-temperature stress tests were performed on n-type substrate devices with applied gate biases ranging from –2 to 2 V (~ –11 to 9 MV/cm). The oxides break down

quickly for positive biases > 1 V. Figure 25 illustrates ΔV_{mg} as a function of stress temperature for both types of film compositions. Both types of films exhibited electron trapping under NBTS and hole trapping under PBTS. The NBTI results are unlike behavior typically found in thin HfO_2 devices, where positive interface and oxide trapped charge generation dominate [29, 37]. NBTS induces electron trapping that is likely caused by electron injection from the gate for the devices in this report. The electric fields applied during NBTS here are significantly higher than the values used in previous NBTI experiments on HfO_2/SiON devices that produced negative shifts in ΔV_{mg}, where V_g varied from ± 1-3 MV/cm [29, 37]. However, we found no measurable change in ΔV_{mg} for smaller values of gate bias. Moreover CVS performed at room temperature with similar gate biases and stress times as in the NBTS tests produced negligible change in ΔV_{mg} (not shown here). Therefore, the amount of charge trapping depends strongly on temperature. Figure 26 shows an Arrhenius plot of ΔN_{ot} vs. 1/T that illustrates the temperature dependence more clearly. The extracted activation energies for ΔN_{ot} are 0.56 eV and 0.44 eV for the low-Si_3N_4 and high-Si_3N_4 devices respectively. Although these values are similar to the activation energy for the diffusion of molecular hydrogen in SiO_2 (~ 0.45 eV) [37], the degradation mechanisms are different.

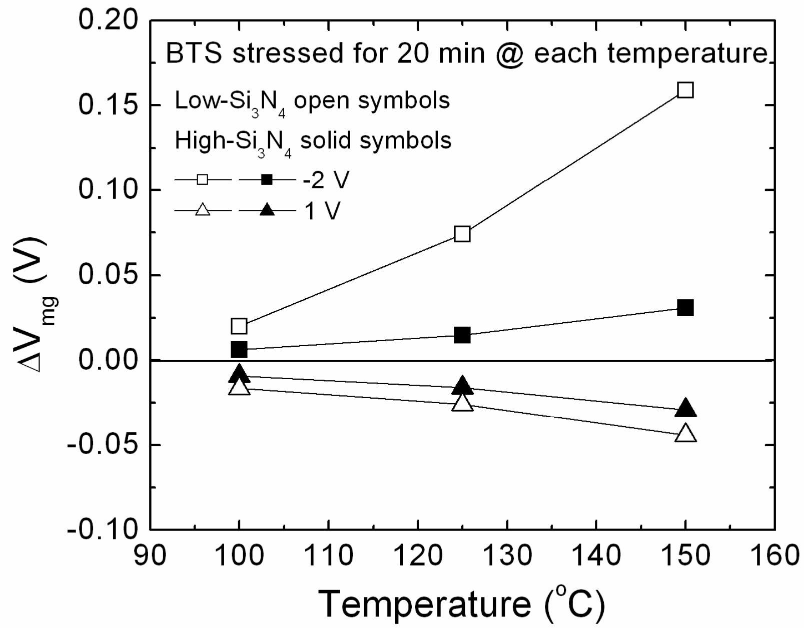

Fig. 25. ΔV_{mg} vs. stress temperature for 2 nm low-Si_3N_4 ($Hf_{0.6}Si_{0.2}ON_{0.2}$) and high-Si_3N_4 ($Hf_{0.3}Si_{0.4}ON_{0.4}$) Si MOS devices with BTS bias V_g = -2 and 1 V. Each device was stressed for 20 minutes at each temperature. C-V characteristics were measured after each stress interval when the device returned to room temperature.

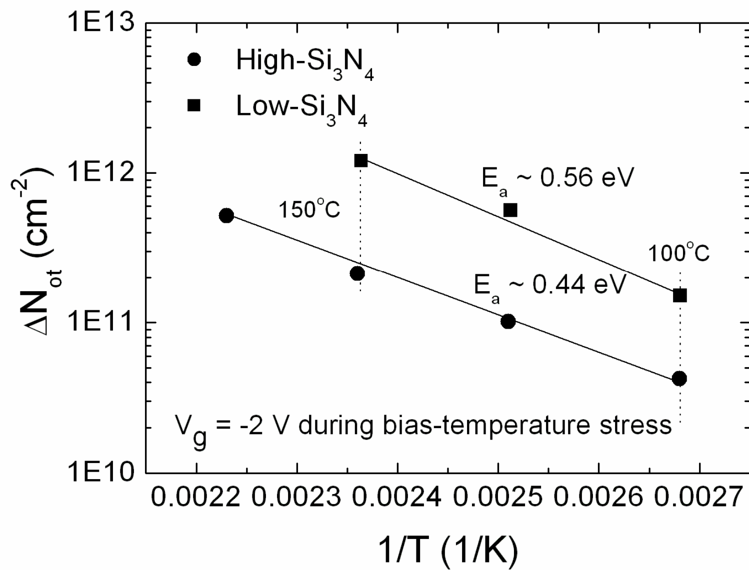

Fig. 26. ΔN_{ot} vs. inverse of temperature for 2 nm low-Si_3N_4 ($Hf_{0.6}Si_{0.2}ON_{0.2}$) and high-Si_3N_4 ($Hf_{0.3}Si_{0.4}ON_{0.4}$) Si MOS devices with BTS bias V_g = -2.

The amount of charge trapping depends on how much charge is injected during the stress. The gate injection current is likely caused by Fowler-Nordheim (F-N) and trap-assisted tunneling. The F-N tunneling current results in electron trapping via gate injection in SiO_2-based MOS capacitors at high electric fields (> 6 MV/cm) [49]. Studies have shown that the F-N emission rate increases with increasing temperature (in the range of 25 – 400^oC) [50]. Figure 26 illustrates the injected charge from each temperature stress for the HfSiON devices. We observe increasing charge injection with increasing temperature. Figure 27 shows the F-N plot for a 2-nm low-Si_3N_4 content device at room temperature and at 150^oC. The devices exhibit F-N tunneling at the higher gate biases (approaching -2 V). The higher magnitude of the curve for the device at 150^oC also indicates the higher F-N emission rate at elevated temperature.

The enhanced levels of charge trapping and current levels observed in the low-Si_3N_4 film, which contains more defect states than the high-Si_3N_4 film, also suggest that trap-assisted tunneling is an additional mechanism for the charge trapping. Trap-assisted tunneling contributes to the total leakage current in high-k dielectrics more substantially than in SiO_2 due to the higher density of post-process defect states in high-k materials [39].

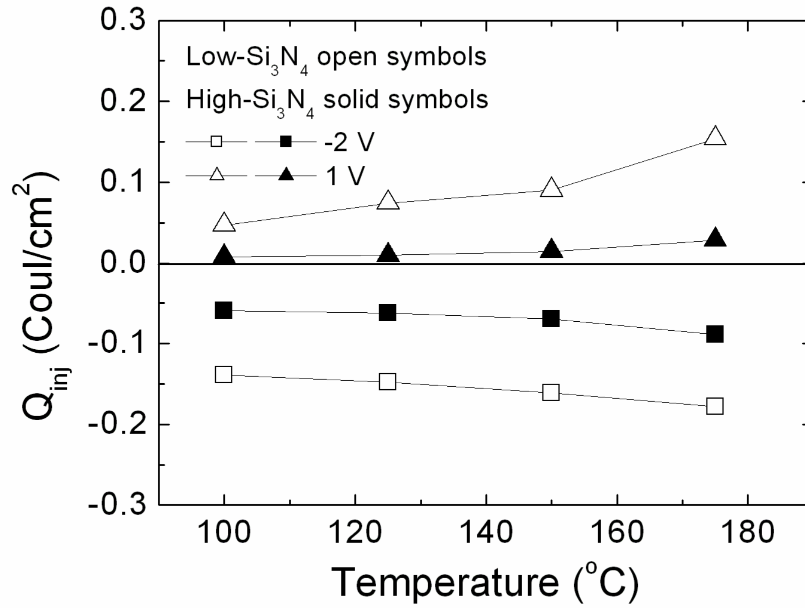

Fig. 27. Q_{inj} as a function of temperature for the low- and high-Si_3N_4 devices with BTS bias V_g = -2 and 1 V. The Q_{inj} represents injected charge after 20 minute stress at each temperature.

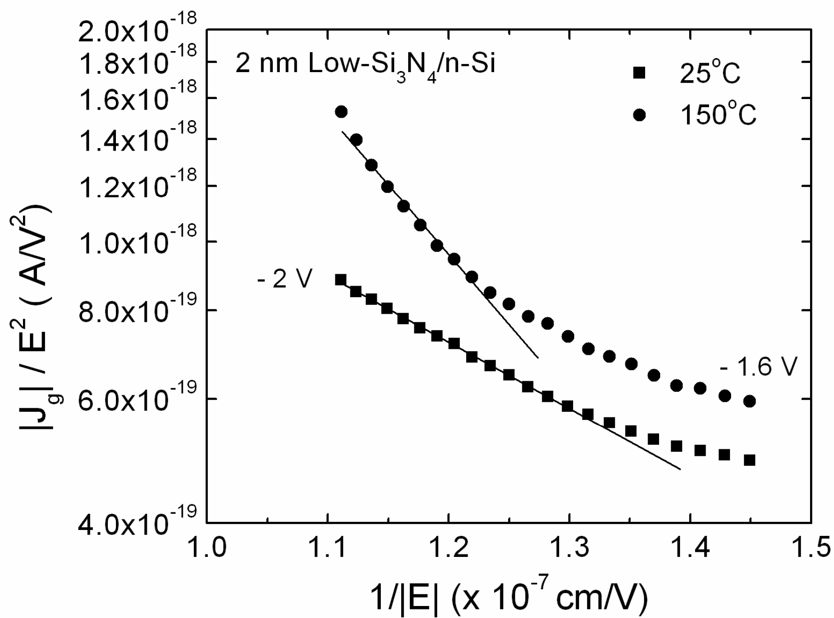

Fig. 28. Fowler-Nordheim fit ($|J_g|/E^2$ vs. $1/|E|$) for a 2 nm low-Si_3N_4/n-Si device at room temperature and 150°C.

The results indicate that these HfSiON/Si devices are less sensitive to bias temperature stress than previous HfO_2 devices [29, 37-38]. Very large electric fields that exceed typical operating voltages are required to cause charge injection from the gate. While the charge trapping depends strongly on temperature, the sources of bias-temperature stress degradation observed here are different than typical NBTI mechanisms. Unlike the HfO_2 devices in [29, 37], the HfSiON devices in this study were not treated with a hydrogen-containing (e.g., forming gas) anneal, which is reflected by the larger post-process interface trap density (N_{it} ~ 5×10^{11} cm^{-2}) for the devices used here. Because NBTI is sensitive to hydrogen [29, 37-38, 45-48], this may account for at least some of the difference in response. Further investigation in the future is necessary to fully understand the bias-temperature instabilities in HfSiON devices. The challenge in device processing is to introduce enough hydrogen to passivate the dangling bonds at the interface, without introducing so much that one sees radiation-induced interface-trap buildup and NBTI [29, 37-38, 45-48].

The long-term reliability of the HfSiON on Si devices is examined with baking and bias-temperature stress tests. Baking the devices at temperatures ranging from 100°C – 200°C resulted in a midgap voltage shift of ~ 200 mV in the 2 nm devices. This result revealed the high density of process-induced charges in the HfSiON film, and showed that processing steps, like baking, can significantly change the electrical characteristics. Bias-temperature experiments resulted in electron trapping at very high applied electric fields (~ 10 MV/cm), which is likely caused by Fowler-Nordheim and trap-assisted

tunneling. The atypical response is likely due to processing differences. Without the hydrogen containing anneal, the devices are less susceptible to bias-temperature instability, but suffers from higher density of process-induced interface trapped charges.

CHAPTER VI

CONCLUSIONS

We have examined and discussed the effects of X-ray irradiation and bias-temperature stress on high-k dielectric MOS devices in this thesis. The material properties and processing techniques play important roles in the radiation response and reliability for the high-k dielectric devices. For example, HfO_2 on Ge capacitors with Dy_2O_3 interfacial layers were investigated. These devices display gate leakage levels that are similar to HfO_2/Ge devices with other interfacial materials like GeO_xN_y. However, we also found high border trap densities (ΔN_{bt} ~ 4.36×10^{11} and 1.05×10^{11} cm^{-2} for the 10 nm and 5 nm HfO_2 samples) as determined from the large *C-V* hysteresis. Therefore, while Dy_2O_3 may be beneficial in preventing dopant diffusion, the high densities of border traps suggests a relatively poor interface quality. Although the gate leakage currents are significantly lower than Si/SiO_2 devices of equivalent oxide thicknesses, the current levels are still high enough to neutralize any radiation-induced oxide-trapped charge. HfO_2 has also been shown to trap large amounts of radiation-induced electrons, which may balance the net oxide-trapped charge [29]. As evident in the studies on these HfO_2 on Ge samples, the interface (between the gate oxide and substrate) quality can dominate the radiation response and the overall device electrical characteristics.

Hf Si oxynitride offers improved interface qualities relative to HfO_2. However, the

charge trapping characteristics significantly worsen for HfSiON films that phase-separate, which may occur during high temperature processes [9]. The irradiation and CVS responses of Si MOS devices with high-Si_3N_4 (amorphous) and low-Si_3N_4 (containing crystalline HfO_2) content HfSiON reveal important differences in the electrical characteristics. We found significant electron trapping in the low-Si_3N_4 content devices, but the high-Si_3N_4 content devices exhibited relatively little electron trapping. CVS experiments showed that positive bias caused considerable electron injection (from the substrate), especially in the low-Si_3N_4 content devices. Furthermore, by comparing the radiation response and CVS results of the low- and high-Si_3N_4 content devices, we conclude that electron trap sites originate from the grain boundary-induced defect states in the HfO_2 nano-grains in the chemically phase-separated low-Si_3N_4 film. Both types of devices showed considerable reduction in total-dose-induced net oxide charge relative to Hf silicate devices, with ΔN_{ot} approximately 16× less for the high-Si_3N_4 content device after 1 Mrad(SiO_2) exposure. The radiation-induced voltage shifts in these high-k devices are likely not a concern for the technology nodes of interest to terrestrial or space applications.

The HfSiON devices also exhibited improved bias-temperature instability relative to previous HfO_2 devices [29, 37-38]. However the stability may be the result of different device fabrication processes. That is, these devices would likely display enhanced bias-temperature instability had they been treated with a hydrogen-containing anneal. Such process will effectively lower the pre-irradiation interface density of the HfSiON

devices (N_{it} ~ $5 \times 10^{11} - 1 \times 10^{12}$ cm^{-2}), which is significantly higher than the HfO_2 devices in [29, 37-38]. It remains a challenge to balance the various factors involved in the fabrication of high-k materials that can affect the overall device performance. For example, the Hf silicates are more thermally stable than HfO_2, but have lower relative dielectric constant values. Nitridation brings advantages such as improved interface passivation, but nitrided layers are also more susceptible to electron trapping. It is unlikely that high-k dielectrics will fully replace SiO_2 technology until a generic processing method is developed that can be utilized to mass produce high quality high-k dielectric MOS devices at reasonable costs. The experimental results presented in this thesis show that considerable progress has been made in the fabrication techniques for Hf-based dielectric MOS devices. The research provides insights to the radiation degradation and long term reliability that are essential to the development of Hf-based MOS devices.

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