Improved effective mobility extraction in SOI MOSFETs.

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Abstract

The standard method of extracting a carrier effective mobility from electrical measurements on MOSFETs is reviewed and the assumptions implicit in this method are discussed. A novel technique is suggested that corrects for the difference in drain bias during IV and CV measurements. It is further shown that the lateral field and diffusion corrections, which are both commonly neglected, in fact cancel. The effectiveness of the proposed technique is demonstrated by application to data measured on a quasi- planar SOI MOSFET at 300 K and 4 K.

Keywords: Mobility, SOI, finFET, MOSFET

1. Introduction

The operation of a silicon MOSFET requires charge carriers to travel between its source and drain contacts, so any scattering of these carriers will limit the performance. The degree of carrier scattering can be quantified through the carrier mobility, which is proportional to the time between scattering events and represents the ability of a carrier to be accelerated in an electric field. By comparing the experimental mobility with model calculations over a range of carrier densities (or gate voltage V_g) and temperatures it is possible to work out which scattering mechanism are dominant in each region. However, the carrier mobility is not directly measured, but must be correctly extracted from the experimental data.

For bulk Si MOSFETs the effective mobility μ_{eff} has been extracted from numerous devices and found to follow a universal curve that depends only on the vertical electric field (E_{eff}) across the channel. As devices are scaled down to reduce

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the carrier transit time there is a need for tighter electrostatic control, which results in and increase in E_{eff} and a decrease in the effective mobility. Furthermore, access resistance has to be kept low, to avoid RC time constants limiting device switching speed, which entails heavy doping in the source and drain regions and also increases carrier scattering. This means that conventional scaling results in a significant drop in carrier mobility in small devices.

Beyond simple scaling, significant progress has been made in achieving electrostatic control through multiple gates and fabrication of MOSFETs on SOI. Similarly, developments in high-k gate dielectrics have led to reduced effective oxide thicknesses and smaller gate voltages, but at the cost of further scattering at the channel-gate dielectric interface. In each case it is important to know how the carrier scattering has changed and which factors limit the mobility. However, there are many pitfalls in extracting μ_{eff} from a fabricated device that can lead to erroneous conclusions.

In this paper we will discuss some commonly neglected corrections that should be applied when extracting the effective mobility of a MOSFET. We will propose a simple approach to correct the major source of error and show that others in fact cancel out. Finally, the method will be applied to data from wide finFETs at room temperature and 4 K.

2. Review of conventional approach

We will begin by following the usual method of extracting μ_{eff} for a MOSFET and identifying four sources of error. The effective mobility is commonly obtained by measuring the conductivity, from the drain current I_d at a drain bias of V_d, and dividing by the inversion charge density Q_{inv} using

$$\mu_{eff} = \frac{L}{W}\frac{I_d}{V_d Q_{inv}} \qquad (1)$$

where W is the device width and L the channel length.

The 1st source of error is the value of inversion charge used.

The inversion charge density is often simply calculated as $Q_{inv} = C_{ox}(V_g - V_t)/WL$ where C_{ox} is the measured oxide capacitance and V_t is the (often ill defined) threshold voltage. Improved accuracy can be obtained by using the split CV (capacitance-voltage) method [1], and integrating the measured gate-channel capacitance $C_{gc}(V)$ to find the charge in the channel

$$Q_{inv}(V_g) = \frac{1}{WL}\int_{-\infty}^{V_g} C_{gc}(V)\,dV \qquad (2).$$

Eq. (2) assumes that surface states, or significant

charge trapping in the dielectric, do not affect the measurement of C_{gc}. Thus, the most commonly used expression to extract μ_{eff} for a MOSFET is

$$\mu_{eff} = \frac{L^2 I_d}{V_d \int_{-\infty}^{V_g} C_{gc} dV} \quad (3)$$

Equation (3) can also be expressed by replacing I_d/V_d with the drain conductance $g_d = dI_d/dV_d$

$$\mu_{eff}\left(V_g\right) = \frac{L^2 g_d}{\int_{-\infty}^{V_g} C_{gc} dV}, \quad (4)$$

but clearly this will lead to discrepancies where the conductivity is non-linear.

The 2nd source of error is in combining data obtained with a different drain bias.

During the measurement of I_d a fixed drain bias V_d is applied, while the gate voltage is swept from below threshold to strong inversion. However, the inversion charge is usually measured from a CV scan with zero drain bias. This can lead to significant errors as the presence of a drain bias changes the charge distribution in the channel.

Ideally the conductivity would be measured at very low bias, but then noise is an issue so many $I_d\left(V_g\right)$ measurements use $V_d = 50$ mV [2,3,4] and in some cases 100 mV [5] or larger which creates a non-uniform channel. Alternative CV techniques have been devised that measure the gate-to-drain and gate-to-source capacitances separately whilst biasing the substrate and the source to create the same conditions as in the $I_d\left(V_g\right)$ measurement [6,7]. Modeling the channel as a transmission line network has also been employed with high frequency AC admittance measurements [8]. In each case, the measurement configurations are cumbersome and cannot be used for SOI devices that do not have a substrate contact.

In the next section, we will demonstrate a new and simple technique to extract either I_d/V_d or $g_d = dI_d/dV_d$ at $V_d = 0$ V , without resorting to elaborate measurement procedure, and combine this with an inversion charge from using the normal split CV setup [1].

There are, however, two further sources of error that should first be addressed by recapitulating the full expression for the drain current in an nMOSFET, which is composed of both drift and diffusion contributions [9]

$$I_d/W = Q_{inv}\mu_{eff}E_x - D\frac{dQ_{inv}}{dx} \quad (5)$$

where E_x is the electric field a distance x along the channel and D is the diffusion coefficient.

The 3rd source of error is in neglecting the diffusion term in the drain current.

Although the diffusion term can be safely

neglected before pinch-off, after that point all conduction at the drain end of the channel is by diffusion. Similarly the drain current is dominated by diffusion in the sub-threshold region. The diffusion coefficient is given by the well known Einstein relation $D = \varepsilon_d \mu_{eff} / q$, where q is the electronic charge and ε_d is the diffusion energy [10]. For single subband occupancy, $\varepsilon_d = kT\left(1+e^{-(E_F-E_0)/kT}\right)\ln\left\{1+e^{(E_F-E_0)/kT}\right\}$ with E_F being the Fermi energy, and E_0 the first sub-band minimum. This reduces to $\varepsilon_d = kT$ in weak inversion and $\varepsilon_d = E_F - E_0$ in strong inversion.

The 4th source of error is in assuming the drain voltage is dropped linearly along the channel.

It is often assumed that the lateral field is constant i.e., $E_x = V_d/L$, but this will not be the case in short channel devices, especially near to the source.

Providing V_d tends to zero, Sodini *et al.*[11] suggest these last two errors can be corrected for by making use of

$$E_x = F(V_g)V_d/L, \tag{6}$$

and $$\frac{dQ_{inv}}{dx} = -\frac{C_{ox}V_d F(V_g)}{WL^2}. \tag{7}$$

Using Eqs. (5-7) we may write

$$\frac{I_d}{W} = \mu_{eff}\frac{V_d}{L}F\left(V_g\right)\left\{Q_{inv} + \frac{\varepsilon_d}{q}\frac{C_{ox}}{WL}\right\} \tag{8}$$

And including the correct expression Eq. (2) for Q_{inv}

$$\mu_{eff} = \frac{\left(I_d/V_d\right)L^2}{F\left(V_g\right)\left[\int_{-\infty}^{V_g} C_{gc}dV + \frac{\varepsilon_d}{q}C_{ox}\right]} \tag{9}$$

Although Eq. (9) is simple enough, it was not explicitly stated in the original paper by Sodini *et al.*[11]. They did state that the two corrections have a "canceling effect", but again did not show this explicitly. Unfortunately, Sodini *et al.*'s expression for $F(C_{gc}/C_{ox})$, which was originally derived for bulk MOSFETs, gives unphysically large values of the mobility in the present case. More recently Zebrev and Gorbunov [12] have given a drift diffusion model for a fully depleted SOI MOSFET, from which

$$F = \beta\left(1+\frac{C_{ox}\varepsilon_d}{qQ_{inv}WL}\right)^{-1}, \tag{10}$$

where $\beta = 1+\frac{C_S C_{BOX}}{C_{ox}\left(C_S + C_{BOX}\right)}$ and C_S, C_{BOX} and C_{ox} are the capacitance of the silicon body, buried oxide and gate oxide respectively.

In the case where $C_{ox} >> C_{BOX}, C_S$, and hence $\beta = 1$, it can easily be seen by substituting Eq. (10) into Eq. (8), that any variation in the lateral field E_x is exactly compensated for by the

diffusion term, leaving the original "uncorrected" Eq. (3). However, the particular capacitance values must first be assessed to check $\beta = 1$ before making this assumption.

3. Proposed, improved approach

Following the above discussion we propose a new and simple technique to extract the effective mobility. The inversion charge is measured as a function of gate voltage using the normal split CV setup [1]. We then measure sets of $I_d(V_g)$ for different drain biases and perform linear regression to obtain the limiting value of either I_d/V_d or $g_d = dI_d/dV_d$ at V_d = 0 V. The approach is somewhat different in the regions of sub-threshold and strong inversion:

The drain current in *sub-threshold* is due to diffusion and given by

$$I_d = I_0\left(1 - e^{-\frac{qV_d}{kT}}\right) \tag{11}$$

$$\text{So } g_d = \frac{dI_d}{dV_d} = I_0 \frac{q}{kT} e^{-\frac{qV_d}{kT}}, \tag{12}$$

$$\text{or } \ln(g_d) = -\frac{q}{kT}V_d + \ln\left(\frac{q}{kT}I_0\right) \tag{13}$$

Hence a plot of ln(g_d) against V_d, at a particular gate voltage, is a straight line with the intercept yielding $g_d(V_g, V_d = 0) = I_0(V_g)\, q/kT$. Note that in the limit of small V_d Eq. (11) reduces to $I_d = I_0\, qV_d/kT$, so I_d/V_d is numerically equal to g_d in the limit of $V_d = 0$. The predicted slope of $-q/kT$ can be used to check the extraction is valid. Beyond threshold the drift term becomes dominant and the slope of the semi-log plot will be seen to deviate from $-q/kT$. In the strong inversion region, plots of I_d/V_d against V_d for given gate voltage yield straight lines with the obvious intercepts of I_d/V_d at V_d = 0V.

4. Measurements on finFET devices

To test the suggested methodology the various corrections are applied to a finFET of width 1.87 μm, at 300 K and 4 K. In research, wide finFETs (quasi-planar) serve as controls in comparing their narrow fin counterparts with standard top-gated MOSFETs. N-channel finFETs were fabricated at NXP Semiconductors on Si(100) substrates, with 145 nm buried SiO_2 and 65 nm SOI with a doping of 10^{15}cm^{-3}. Fins were defined in the <110> direction with (110) sidewall surfaces and a (100) top surface. The gate stacks consisted of 1 nm thermal SiO_2 followed by metal organic chemical vapour deposition of 2.3 nm $Hf_{0.4}Si_{0.6}O$ and 5 nm TiN deposited by plasma enhanced atomic layer deposition. After gate patterning, As extensions were implanted and spacers formed. Access resistance was reduced with 40 nm Si selective

epitaxy. As+P highly doped drain implantation and NiSi were used for source/drain contacts with a spike anneal at 1050°C to activate the dopants. A cross sectional TEM image of a device with a fin width of 13 nm is shown in Fig. 1. Additional details can be found in [13][14].

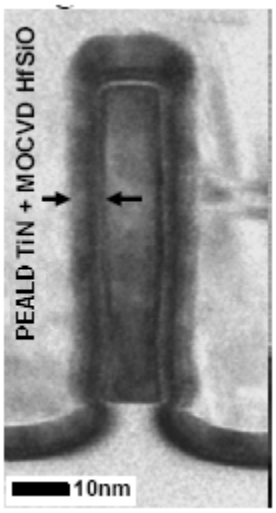

Figure 1: Cross sectional TEM image of a 13nm finFET after full device processing.[14]

In this work a quasi-planar device was investigated consisting of 10 parallel fins, each of width (W_{fin}) 1.872 μm, height (H_{fin}) 65 nm and length (L) 10 μm. The effective width is given by $W_{eff} = 10*(2H_{fin}+W_{fin}) = 20\mu m$. We measured $I_d(V_g)$ for drain biases in the range V_d = 5–100 mV and $C_{gc}(V_g)$ at a frequency of 100kHz both at 4K and 300K. We found that the access resistance was indeed negligible compared to the channel resistance for these long channel devices. However, at large gate voltage the measured drain current is reduced (I_{d0} in Fig. 2) due to gate leakage. This has been corrected for by adding back the gate leakage current I_g using $I_d = I_{d0} + I_g/2$ (as half the leakage current is to the source, half to the drain and body leakage can be ignored in the SOI structure) [15]. Figure 2 shows how this removes the apparent drop in drive current at high gate voltage.

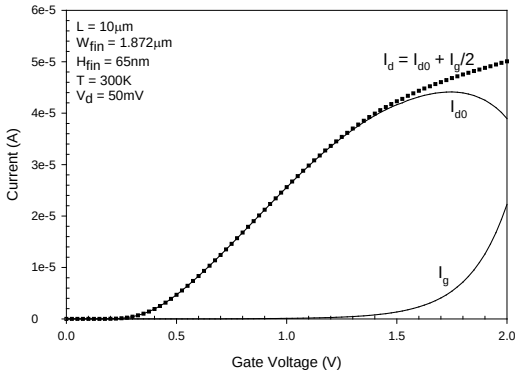

Figure 2: Gate leakage correction: I_{d0} and I_g are the measured drain and gate leakage currents, I_d is the corrected drain current.

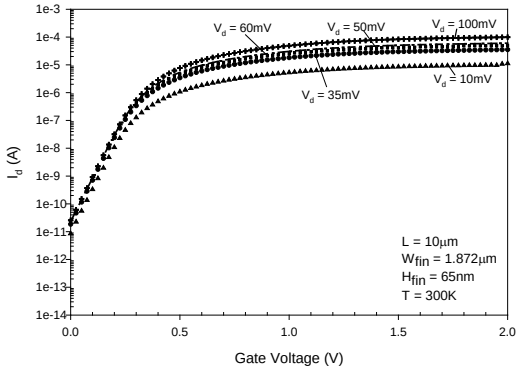

Figure 3: Corrected $I_d(V_g)$ data for a range of drain biases at 300 K.

Figure 3 shows the leakage corrected $I_d\left(V_g\right)$ at room temperature for a range of drain bias voltages. The conductivity at zero bias can now

be extracted for any chosen V_g. Figures 4 and 5 show examples of the regression used in sub-threshold, at V_g = 0.225 V, and in strong inversion at V_g = 0.70 V, respectively.

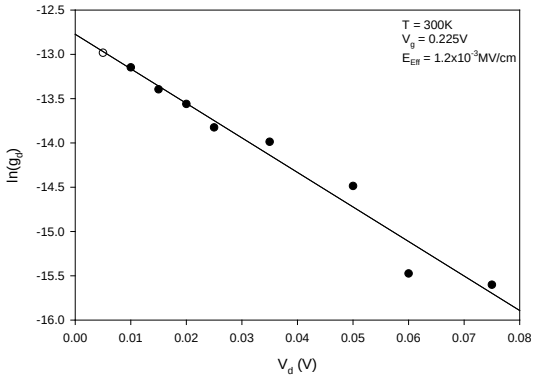

Figure 4: Semi-log variation of drain conductance g_d with drain bias in the sub-threshold region (V_g = 0.225 V), enabling $g_d(V_d = 0)$ to be extracted as the intercept.

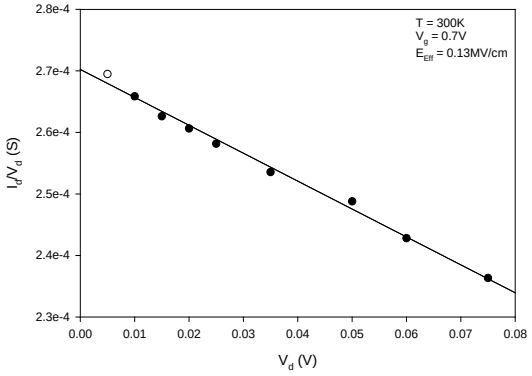

Figure 5: Variation of drain current with bias in **s**trong inversion (V_g = 0.70 V) from which the zero bias conductance can be extrapolated.

In each case we see the predicted straight line behavior and are able to extract a conductance value for zero bias. Fig. 4 has the correct slope of -38 V^{-1} and typical regression coefficients are better than 0.98, indicating high accuracy. Note that the conductance in strong inversion (where channel mobility is often reported) is already 8 % lower at the standard measuring bias of V_d = 50 mV than at zero bias.

We have also performed these measurements at low temperatures (4 K), where fewer scattering mechanisms need to be considered making the mobility results simpler to interpret, and again obtain good linear fits from which to extract zero bias conductivity values.

5. Carrier mobility in finFET devices

Having extracted the zero bias conductance values corresponding to each inversion charge density the electron mobility can be calculated with the first two errors corrected, as shown in Fig. 6 for the 4 K data as a function of Q_{inv}. The large suppression of inferred mobility at higher drain bias can clearly been seen, especially at low density, confirming the necessity of extrapolating to V_d = 0 V.

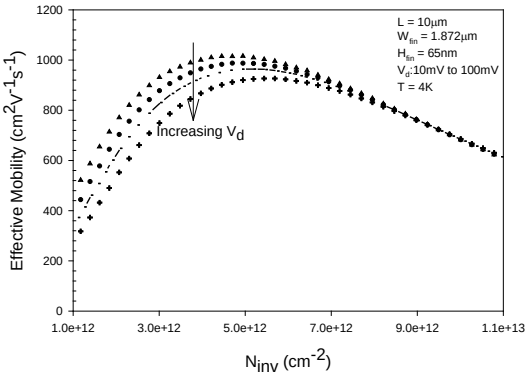

Figure 6: Extracted mobility at 4 K, showing the effect of increasing drain bias from 10 mV (▲) to 100 mV (+)**.**

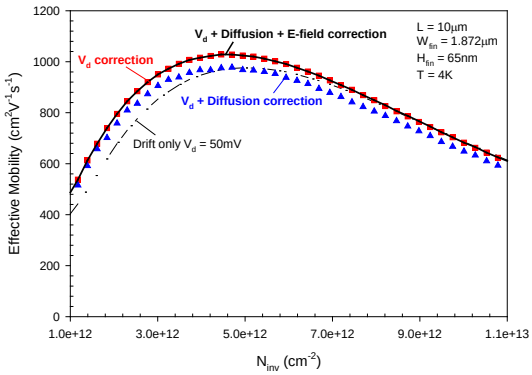

Figure 7: 4 K mobility values: uncorrected (broken line) and including corrections for drain bias only (squares), drain bias and diffusion (triangles), drain bias, diffusion and E_x-field (solid line).

Next we consider the additional corrections that arise from including carrier diffusion and non-uniform electric field along the channel. In order to consider the diffusion correction over the full range of gate biases we have calculated the Fermi energy in the quasi-2D electron gas, (the inversion layer) using a Poisson-Schrödinger simulator [16,17]. Figure. 7 shows how this diffusion correction reduces the mobility values extracted, particularly at high density, and how the further correction for non-uniform field exactly cancels this effect at all gate voltages.

A similar procedure has been followed for the room temperature data, shown in Fig. 8.

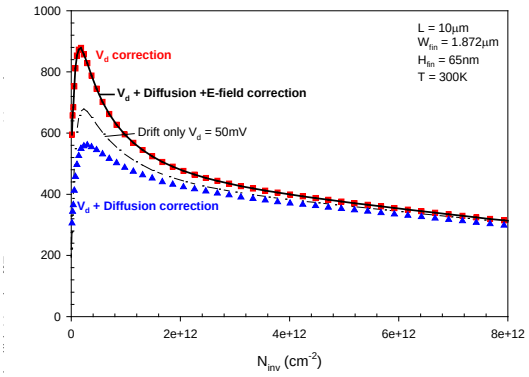

Figure 8: Mobility extracted from room temperature data, showing the effect of the various corrections as in Figure 7.

An interesting feature of the 300 K mobility is the sharp peak near threshold. Iyengar *et al.*[18] have seen this on the top surface of their finFETs with HfSiO gate dielectric, but offer no physical explanation. This pronounced peak is only observed in our wide quasi-planar finFETs (W_{fin} > 65 nm) and not for the devices with narrow fins. The magnitude of the peak is also very sensitive to variations in Q_{inv}. In the present case, the steep drop to the left of the peak in Fig. 8 is at least partially due to trapping processes that affect the CV measurement [19] and may be obviated by inversion charge pumping [20]. The fully corrected mobility values at 300 K and 4 K (solid lines from Figs. 7 and 8) are compared in Fig. 9. This shows that the anomalous peak at low density in the room temperature mobility leads to a higher mobility in that region for 300 K than at 4 K, contrary to all usual expectations. We do not currently have

an explanation for this either, but suspect that it may be related to the inversion charge density measurement close to threshold and suggest further work on this is required.

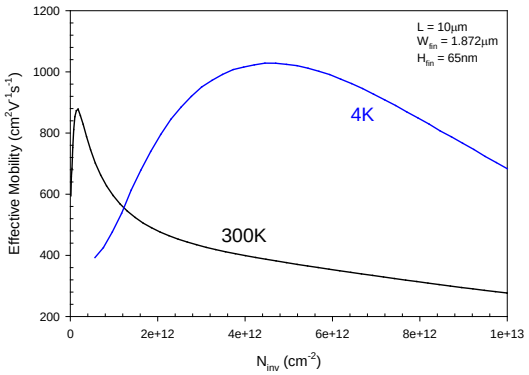

Figure 9: Comparison of the fully corrected mobility at 300 K and 4 K in a wide finFET.

6. Conclusion

Accurate mobility extraction is essential for assessing the benefits to be gained from novel device architectures and use of "high-mobility" channel materials, such as strained silicon or germanium. It is also vital to understand the relationship between experimentally extracted quantities and those used in device modeling. The usual method of mobility extraction has tended to ignore the difference in drain bias during IV and CV measurements. Whilst previous attempts to accommodate this have resulted in elaborate measurement techniques, we suggest a novel method to correct for the drain bias in the IV measurements so that the effective mobility is essentially extracted at zero drain bias. Furthermore, corrections for a non-uniform electric field in the channel and for the diffusion contribution to the drain current have been considered. Although these individually have a significant effect, when applied in combination they are shown to exactly cancel for the whole gate voltage range. Consequently provided that one is ignored they both can be! The methodology has been applied to extract effective mobility from experimental data on an SOI quasi-planar finFET, both at room temperature and 4 K. This has demonstrated that a drain bias of only 50 mV has a significant effect on the values obtained. Finally, we suggest that the drain bias correction can, and should, also be applied to ordinary bulk MOSFETs.

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