博士論文概要

論文題目

High Efficiency and Low Noise Charge Pump Circuits for Non-volatile Memories

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Along with the System-on-Chip (SoC) concept being widely adopted, more and more building blocks are to be implemented into one chip. However, those different building blocks are generally not all specified with the same supply voltage, for example, 1.8V for the digital parts while 3.3V for the analog parts in most 0.18um products. Generally, Low-Dropout (LDO) regulators are used to solve the problem at the cost of efficiency if all the required voltages are below the supply. On the other hand, switching regulators is able to provide both higher and lower voltages with very high efficiency, but the need for an inductor makes it quite area consuming and the efficiency drops tremendously in light load condition. Besides, the control loop also requires very sophisticated design. On the contrary, the charge pump circuit, owning to its relatively compact size and simple control strategy, has earned lots of attention in applications where an on-chip high voltage supply with relatively low output current is much preferred. Especially in non-volatile memories such as EEPROM or NAND flash, the performance is heavily dependent on the charge pump circuit which provides the required programming or erasing high voltage, usually more than 10V.

In recent years, since the stringent power budget of LSIs is continuously squeezing the supply voltage, two main challenges arise for the charge pump circuit design in non-volatile memory. The first challenge is related to the power efficiency. As the supply voltage of non-volatile memory scaling down, the stage number of the charge pump circuit must be increased, since the programming voltage is defined by the energy gap physically and is not likely to be lowered in the same way. As a result, the power penalty for the extra stages and the saturation effect caused by transistors' body effect deteriorates the efficiency, which becomes a very serious problem for those applications powered by batteries. Although many new structures have been worked out to improve the output linearity with respect to the stage number, the dynamic power loss problem due to the parasitic capacitance is seldom touched. The second challenge is related to the output noise. For non-volatile memory, lowering the operating voltage also means shrinking the threshold window and the noise margin as well. This makes the memory cell more sensitive to the programming noise, and thus more verifying process is required to correct the error at the cost of memory data throughput. Conventional noise suppression method relies on large output capacitance, while the large area overhead and the slow setup time are prohibitive for many applications.
This thesis is mainly written to address the above two problems based on the analysis and experiments. The charge pump circuit is introduced by its application in non-volatile memory. The basic knowledge of MOS transistor and analog circuit will not be restated, while the impact of some secondary effects is to be analyzed. The basic operation with the mathematical model will be derived step by step to provide a reference for the analysis of more in-depth problems. Different charge pump structures are also briefly described for comparison. Although there might be some overlapping, the charge pump efficiency and noise problems in this thesis will be discussed separately and independently. Detailed theoretical analysis is presented and the measurement results are given to prove the validity of the proposed solutions.

Chapter 1 begins with the introduction of the non-volatile memory. The program and erase method as well as their characteristic of the non-volatile memory cell are described, and the importance of the charge pump circuit is explained. The utilization of the charge pump circuit in other applications is also briefly mentioned. The main topics in this thesis are clarified as well.

Chapter 2 describes the basic operation of the charge pump circuit. The mathematical model is derived and the influence of the charge transfer unit is analyzed. The approximate result of the output ripple voltage and output voltage set up time are also given. The conventional Dickson charge pump is introduced with emphasis on explaining the threshold voltage loss, and the output voltage saturation problem is shown. The NMOS four phase charge pump circuit is then introduced to explain the threshold voltage cancellation method, and the limitation is described as well.

Chapter 3 concentrates on the design of a better charge transfer unit. A four phase switched polarity charge pump using triple well CMOS technology is presented. The architecture takes advantage of the threshold voltage cancellation scheme in the conventional four phase charge pump. With the body control technique, the body effect is eliminated. The charge transfer unit is shared in positive and negative operation, which makes the design more compact. Simulation results show that the proposed 5-stage charge pump is able to reach +8.22V/-8.05V (ideal: +9V/-9V) with estimated parasitics, and the output indicates good linearity with respect to the increase of stages.
Chapter 4 deals with the efficiency problem for low voltage supply. The charge pump efficiency is analyzed, and the influence of the bottom-plate parasitic is emphasized. Complementary charge pump architecture with charge sharing clock scheme is proposed to recover part of the dynamic loss during the pumping process, and the charge sharing order can be double or triple. A charge pump circuit with double charge sharing clock scheme is fabricated in 0.18um technology with a parasitic ratio of 0.1, and the measurement results shows more than 10% peak efficiency increase with no drivability decline. The proposed triple charge sharing scheme is able to recover nearly two-thirds of the charge from the parasitics charging, in which way the dynamic power loss in the pumping process is reduced to almost one-third. Under 0.18um technology with a bottom plate parasitic ratio of 0.2, the simulation results show an overall efficiency increase with a peak value of 62.8% comparing to 46.8% of a conventional one, and the output ripple voltage is reduced by nearly a half.

Chapter 5 deals with the output noise of the charge pump circuit. Different noise suppression methods are first introduced and their limitations are described. The output noise is then re-analyzed in spectrum domain. A hybrid decoupling scheme using both active decoupling and passive decoupling method is proposed to suppress the noise power without output capacitance increase. The mathematical model of the proposed scheme is carefully derived, and a fast optimization method is given to balance the active and passive decoupling path so that a maximum decoupling performance is able to be achieved. Test chip is also fabricated in 0.18um technology. The measurement results shows more than 15.4dB noise suppression improvement with the same output capacitance.

Chapter 6 concludes the thesis and gives the prospect on future design concerns.