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Front-end multi-channel PMT-associated readout chip for hodoscope application

Shiming.DENG*a,b, Hervé.MATHEZ*a,b, Denis.DAUVERGNEa, Yannick.ZOCCARATOa,b, Guo-Neng.LUC

*aInstitut de Physique Nucléaire de Lyon (IPNL), Université de Lyon, Université Lyon 1, CNRS/IN2P3, F-69622, Villeurbanne, France

Université de Lyon, Institut des Nanotechnologies de Lyon INL-UMR5270, CNRS, Université Lyon 1, Villeurbanne, F-69622, France

Abstract

For developing a prompt gamma imaging system, we have designed a 16-channel readout chip in a BiCMOS process to be associated with multi-anode photomultipliers (MaPMTs). Each channel has one current input and two separated outputs. The input has very low impedance to minimize electrical crosstalk and effects of capacitances. The two outputs serve to, respectively, detect signal event and quantify signal charge. The channel architecture is a current-mode one, employing a current conveyor to drive both a buffered current comparator and a charge-sensitive amplifier (CSA). The current conveyor is built with super-common-base (SCB) transistor structures to obtain input impedance in the order of a few ohms. Circuit design with the use of bipolar transistor components also improves frequency and noise performances. The chip has been tested and the evaluated characteristics meet the system requirements.

Keywords: prompt gamma imaging system, super-common-base(SCB), current conveyor, charge-sensitive amplifier (CSA),

1. INTRODUCTION

References

1. INTRODUCTION

Ion therapy is an innovating technique used to treat tumors with enhanced efficiency for the dose deposition conformation as compared to conventional radiotherapy. It requires real-time control of the dose localization during ion therapy, since slight deviations relative to treatment planning may lead to severe consequences. With the aim of developing a primary beam monitor (a beam hodoscope) for such a quality control [1], we propose a prompt gamma imaging system shown in Figure 1.

For typical proton and carbon therapeutic beams, the hodoscope should have a count rate capability of $10^8$ pps, with an accuracy of 1ns. This has led us to implement the system employing arrays of scintillating fibers with read out by MaPMTs or multi-channel plates (MCPs) [2].

The readout MaPMT-associated chip includes 16 channels whose input impedance should be very low (in the order of ten ohms) to minimize crosstalk and wiring capacitance effects. Each channel is a current-mode architecture (shown in Figure 1) defined to allow better achievements in speed and noise performances. It is composed of a current conveyor (with two current outputs) as an input stage, and two separated output stages: a current comparator as a discriminator for signal-event detection and a charge-sensitive amplifier (CSA) for signal charge quantification. The signal-event detection requires high-speed operations for the current conveyor and the current comparator, while the signal charge quantification has a major low-noise requirement for the current conveyor and the CSA.

2. CIRCUIT DESCRIPTION

2.1. Current Conveyor

The current conveyor has a low-impedance input and two high-impedance current outputs, with a 4-bit current gain control to compensate effects of optic fiber ageing and the MaPMT's gain dispersion. Figure 2(a) shows the structure of the current conveyor. It employs two Super Common-Base (SCB) transistors [4-5] (see Figure 2(b)) to drive complementary switched current mirrors having variable-gain output branches. The current input signal is applied to one SCB, and a referenced current is applied to the other to cancel bias offsets.

This process allows the use of RF and large-transconductance bipolar components, which is useful for the design of wide-band, low-impedance and low-noise circuits with improved performances[3].

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The SCB transistor shown in Figure 2(b) is basically a common-base topology \((Q_1)\) with a negative feedback loop \((Q_2)\). The input impedance of the current conveyor, mainly determined by that of the SCB, is expressed as:

\[
Z_{in} = \frac{1}{(1 + \frac{A_0}{(1+\omega A_0 T_{SCB}+\omega A_0 T_{SCB}+\omega A_0 T_{SCB}+\omega A_0 T_{SCB})}) \cdot g_m Q_1 + s C_A}
\]

\[A_0 = g_m Q_2 \cdot R_{SCB}\]
\[\omega A = \frac{g_m Q_1}{2 \pi \cdot C_A}\]

\[
\omega B = \frac{g_m Q_2 \cdot R_{SCB}}{2 \pi (1 + g_m Q_2 \cdot R_{SCB} + g_m Q_2 + \omega A_0 T_{SCB} + \omega A_0 T_{SCB})}
\]
\[C_A = C_{DB} + (1 + g_m Q_2 \cdot R_{SCB} \cdot (C_{m Q_1} + C_{m Q_2} + C_D)
\]

where \(A_0\) is the voltage gain of \(Q_2\) at low frequencies; \(C_A\) is the sum of parasitic capacitances at the input node A (including the detector output capacitance \(C_D\)), \(\omega A\) and \(\omega B\) are poles related respectively to nodes A and B. At moderate frequencies, the input impedance is given by \(Z_A \approx \frac{1}{(A_0 \cdot g_m Q_1)}\). Thanks to the use of large-transconductance bipolar components in the SCB, \(Z_{in}\) can be reduced to a few ohms.

The current gain of the current conveyor is given by:

\[
\frac{I_{out}}{I_{in}} = \frac{g_m MP_2 - MP_5}{g_m MP_1} \times \frac{1}{(1 + \frac{C_1}{g_m Q_1})(1 + \frac{C_2}{g_m MP_2})}
\]

with \(C_1 = C_{bc Q_1}\) and \(C_2 = \Sigma C_{node G}\)

where \(g_m MP_2 - MP_5\) is the total transconductance of the 4-bit switched transistors \(MP_2\) to \(MP_5\) in parallel. As \(g_m Q_1(BJT) \gg g_m MP_2(PMOS)\), and \(C_1 \ll C_2\), the bandwidth is limited by \(g_m MP_2\) and \(C_2\).

### 2.2. Current Comparator

The current comparator following the current conveyor detects current signal events. It compares the current conveyor’s corresponding output signal (typically lasting a few nanoseconds) with a referenced threshold current and produces a pulsed output voltage response.

Figure 3 shows the current comparator mainly consisting of a signal current mirror and a 2-stage output buffer. The signal current mirror employs bipolar transistor components to reduce its input impedance and improve the speed performance of the circuit. This current mirror performs current-to-voltage conversion at its output:
2.3. CSA (Charge Sensitive Amplifier)

The CSA consists of a buffered amplifier and a $R_C f$ feedback network (Figure 4(a)). For a fast input current pulse during a time $t_{puls}$ (~20ns), the CSA output produces a voltage swing given by:

$$\Delta V_{D} = \begin{cases} \frac{\Delta I_c}{g_{mQ_1}} \cdot \frac{1}{g_{mQ_2}} & \text{when } \Delta I_c = I_{in} - I_{ref} > 0 \\ 0 & \text{when } \Delta I_c = I_{in} - I_{ref} < 0 \end{cases}$$

(3)

The time constants at nodes C and D are respectively $\tau_C = C_C/g_{mQ_1}$ and $\tau_D = C_D/g_{mQ_2}$ with $C_C = C_{CQ_1} + C_{beQ_1} + C_{beQ_2} + (1 + g_{mQ_2}/g_{ds}) \cdot C_{Q_1}$ and $C_D = C_{CQ_2} + C_{inverted}$. As $C_C \gg C_D$ and $g_{mQ_2} < g_{mQ_1}$, the speed performance of the current comparator is determined by $\tau_C$. It can be optimized by careful layout and proper sizing of transistor components to reduce different capacitance contributions to $C_C$. The 2-stage buffer converts $\Delta V_D$ to a logic-level pulse.

The magnitude of $I_{in}(t)$ can thus be evaluated from the waveform of $V_{gen}$. By measuring directly the magnitude of $V_{in}$, the input impedance of the current conveyor can be determined by $Z_{in} = \frac{\Delta V_{in}}{I_{in}}$. We have obtained $Z_{in} = 12 \Omega$.

Figure 7 shows signal waveforms of a channel. The circuit operation is verified by observing the output signal of the current comparator $V_{out,comp}$ and that of the CSA $V_{out,CSA}$; the pulsed output of the current comparator indicates the signal event, and the output signal of the CSA gives a magnitude $\Delta V_{out,CSA}$, from which an input signal charge can be evaluated.

For signal-event detection, the detection threshold for the current comparator is set by $I_{ref}$, which can be adjusted from 100µA to 400µA.

For signal charge quantification, the conversion gain at the output of the CSA is 98mV/pC. The evaluated noise in ENC (Equivalent input RMS Noise Charge) is 91fC. The maximum measurable charge before saturation (limited by the current conveyor) is 10 pC. The dynamic range is 36 dB. The crosstalk between adjacent channels is 1.7% (i.e., 35 dB).

3. RESULTS AND DISCUSSION

Figure 5 shows the fabricated readout chip. The chip area including pads is 6.16mm². Each channel occupies a surface area of 680µm × 120µm. The chip has been tested using a board shown in Figure 6(a).

The test board includes a structure shown in Figure 6(b), to generate an input current signal for the testing:

$$I_{in}(t) = \frac{C_Q \cdot dV_{gen}(t)}{dt}$$

(5)
We would like to mention that, our readout chip has similar integrated functions to a 10-channel chip reported in [9]. The power consumption and chip sizes are also comparable. We have obtained improved performances especially in terms of input impedance (12Ω compared to 180Ω), thanks to optimal design with the use of bipolar components in a BiCMOS technology.

Table 1 summarizes the measured characteristics of the readout chip in comparison with post-layout simulation results.

We would like to thank Mr. E. Bechetoille and Mr Y. Zoccarato for their technical helps in layout optimization and ASIC design.

References

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We would also like to thank Mr. E. Bechetoille and Mr Y. Zoccarato for their technical helps in layout optimization and ASIC design.

Figure 7: Signal waveforms of a channel: the two outputs $V_{\text{out,CSA}}$ and $V_{\text{out,comp}}$, in response to $V_{\text{gen}}$.

Table 1: Summary of characteristics of the designed readout ASIC

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Post-Layout results</th>
<th>Test results</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power consumption /channel(under 3.3V) @ current gain from 0.25 to 2</td>
<td>15 to 22mW</td>
<td>16 to 23mW</td>
</tr>
<tr>
<td>Input dynamic range</td>
<td>50µA(525 fC) @ gain 2</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>2.4mA(25.2pC) @ gain 2</td>
<td>—</td>
</tr>
<tr>
<td>Input impedance @ working frequencies</td>
<td>4Ω</td>
<td>12Ω</td>
</tr>
<tr>
<td>Current Conveyor Bandwidth</td>
<td>200MHz</td>
<td>—</td>
</tr>
<tr>
<td>Current comparator Bandwidth</td>
<td>667MHz</td>
<td>—</td>
</tr>
<tr>
<td>CSA Peaking time</td>
<td>30ns</td>
<td>28ns</td>
</tr>
<tr>
<td>1-full-channel ENC</td>
<td>42fC</td>
<td>19fC</td>
</tr>
<tr>
<td>Xtalk</td>
<td>—</td>
<td>1.7%</td>
</tr>
<tr>
<td>Chip Size (including pads)</td>
<td>6.61mm²</td>
<td>6.61mm²</td>
</tr>
</tbody>
</table>

(≈ 1.7%). The evaluated speed and noise performances meet the system requirements. We are undertaking a new chip design with performance optimization to reduce power consumption per channel, for high-resolution hadroscopes.

5. ACKNOWLEDGMENT

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