High-Frequency Performance of Schottky Source/Drain Silicon pMOS Devices

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***Abstract*—A radio-frequency performance of 85-nm gate-length p-type Schottky barrier (SB) with PtSi source/drain materials is investigated. The impact of silicidation annealing temperature on the high-frequency behavior of SB MOSFETs is analyzed using an extrinsic small-signal equivalent circuit. It is demonstrated that the current drive and the gate transconductance strongly depend on the silicidation anneal temperature, whereas the unity-gain cut-off frequency of the measured devices remains nearly unchanged.**

***Index Terms*—Electrostatic measurement, microwave measurements, SB metal/source MOSFETs, scattering parameter measurement, Schottky barriers (SBs), semiconductor devices.**

I. Introduction

THE SCALING of MOSFETs to sub-50-nm gate lengths poses serious problems for doped source/drain (DSD) transistors. Short-channel effects due to proximity of source and drain become increasingly difficult to suppress. Complex fabrication processes that include precise implants and tight thermal budgets are required to achieve necessary shallow implants, abrupt junction profiles, and halo implants. As a result, many say that the end of Moore's law is approaching, and many research works are being devoted to alternative channel and junction materials to prolong the performance benefits gained by scaling.

Substituting a metal, typically a silicide, in place of the doped source and drain regions of a MOSFET offers an elegant solution to many short-channel effects. Like a p-n junction, a Schottky barrier (SB) formed at a metal–semiconductor interface exhibits rectifying properties and can be a drop-in replacement for source and drain that offers several advantages in highly scaled MOSFETs. It provides an abrupt junction due to an atomic interface between two materials, enabling very shallow low-resistivity junctions to be formed. Processing is simplified by obviating ion implantation and high-temperature dopant activation anneal steps along with their corresponding masks. All the while, this technique is wholly compatible with current CMOS processes since silicides are commonly used as source/drain contact materials. Although different nomenclatures exist, SB metal source/drain transistors will be referred to as SB MOSFETs throughout this letter.

Early SB MOSFETs suffered from low performance compared with their DSD counterparts [1], [2]. However, recent publications have shown SB-MOSFET devices exhibiting vastly improved performance [3], [4]. A complete review on the status and benefits of SB-MOS technology has recently been published in [5].

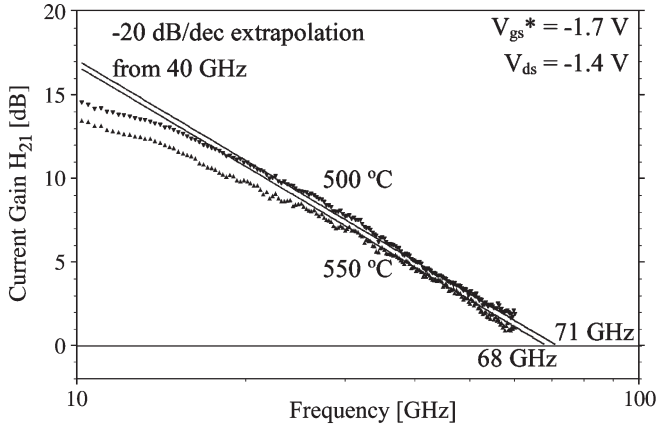

Fig. 1. Current gain versus frequency for wafers annealed at 500 °C and 550 °C.

Following on from previous work in [4], we have investigated the radio-frequency (RF) performance of 85-nm channel length SB PtSi source/drain MOSFETs under International Technology Roadmap for Semiconductors (ITRS)-based bias conditions for high-performance logic [6], since a very high drain bias of -2.5 V was used in [4]. Meaningful performance comparisons with conventional DSD devices have recently been presented in [7]. In this letter, the impact of silicidation annealing temperature on the high-frequency behavior of SB MOSFETs is analyzed through the extraction of an extrinsic small-signal equivalent circuit.

II. Experiment

Salient features of the present devices are a 100-nm-thick *in situ* phosphorous-doped amorphous silicon gate, a gate silicon dioxide layer of 1.8 nm, an effective gate length of 85 nm, and an As doping level of 5×10^{16} cm^{-3} at the surface of the channel. More details of the device fabrication have been given previously in [4]. The use of an n-type gate material instead of the usual p-type for p-channel MOSFETs is responsible for a threshold voltage shift of 1.1 V. Gate voltages presented in this paper are adjusted to account for this shift and are denoted by $V_{\rm gs}^{*}$ to distinguish it from the physically applied bias. SB MOSFETs consisting of two parallel gate fingers of 2-μm-width each (a total transistor width of 4 μm and an expected oxide capacitance $C_{\rm ox}$ of 1.6 fF/μm) are embedded in coplanar-waveguide (CPW) transmission lines for on-wafer microwave measurements. RF measurements are performed up

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TABLE I
MAIN SMALL-SIGNAL EQUIVALENT CIRCUIT PARAMETERS EXTRACTED AT $V_{\rm gs}^* = -1.7$ V AND $V_{\rm ds} = -1.4$ V FOR P-TYPE SB-MOS TRANSISTORS WITH PT CONTACTS ANNEALED AT 500 °C OR 550 °C

SB-MOSFET – Pt contact	Annealed at 500°C	Annealed at 550°C
G_m [μS/μm]	640	469
C_{gg} [pF/μm]	1.43	1.10
R_s [kΩ.μm]	0.56	1.2
R_g [Ω/sq.]	130	130
f_T [GHz]	71	68

to 60 GHz using an Agilent 8510XF network analyzer, in conjunction with a Cascade probe station with ground-signal-ground RF probe tips. Bias conditions based on ITRS [6] recommendations are used and adjusted for the n-poly gate and 1.8-nm-thick gate oxide ($t_{\rm ox}$). A $V_{\rm gs}^*$ of 0 V is chosen as the OFF-state, whereas $V_{\rm gs}^* = -1.7$ V is considered as the ON-state to achieve the same oxide field as present in a device with a $t_{\rm ox}$ of 1.5 nm at a gate bias of -1.4 V. A drain voltage of -1.4 V is applied as the saturation bias condition, as per ITRS roadmap recommendation [6].

For the de-embedding of contact pads and CPW feed lines from the measured transistor S parameters, the ColdFET de-embedding technique proposed in [8] is applied. It performs active and de-embedding measurements on the same device without recontacting. This enables accurate S parameter de-embedding even in the presence of contact repeatability problems and access structure or oxide-thickness variations.

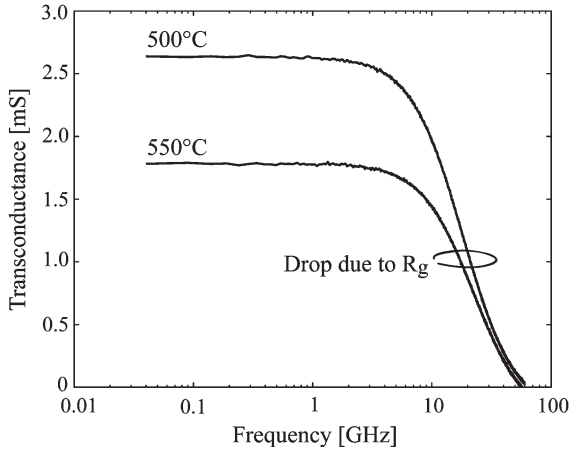

Fig. 2. Extracted extrinsic gate transconductance versus frequency for wafers annealed at 500 °C and 550 °C.

III. RESULTS AND DISCUSSION

RF characterization is performed under saturation conditions ($V_{\rm gs}^* = -1.7$ V and $V_{\rm ds} = -1.4$ V) sweeping from 45 MHz to 60 GHz. Current-gain plots along with the extrapolations at -20 dB/dec from 40 GHz to determine unity-gain cutoff frequencies (f_T) are shown in Fig. 1. The extrapolations are in good agreement with the measured data over a wide frequency range between 20 and 60 GHz. This approach returned cutoff frequencies of 71 and 68 GHz for wafers annealed at 500 °C and 550 °C, respectively. As discussed in [7], these unity-gain cutoff frequencies obtained on the two wafers characterized in this letter show improvements of 61% and 55% over the literature trend line at 85-nm gate length and even surpass the performance of devices of less than 40-nm gate lengths [9].

With $f_T = G_m/2\pi C_{\rm gg}$, this performance enhancement is partly due to the superior G_m (also reported in [7]), which might be expected as the result of the low-doped substrate and its beneficial impact on carrier mobility. $C_{\rm gg}$ is also expected to be smaller in SB MOSFETs. Doped source–drain devices require that the gate overlaps the source and drain extensions in order to confine carriers close to the channel, preventing current flow in low-doped higher resistivity regions and reducing current drive [10]. In contrast, optimum performance in SB MOSFETs is obtained with gate "underlap," which results in lower capacitance [11]. In addition, quantum effects in the inversion layer of modern thin-oxide devices have been shown to lower the gate capacitance, particularly when the substrate is low doped as in the present SB MOSFET [12].

From the measured S parameters converted to Y parameters, the main small-signal equivalent circuit parameters for both transistors are extracted under the bias condition of interest, i.e., $V_{\rm gs}^* = -1.7$ V and $V_{\rm ds} = -1.4$ V. These parameters are summarized in Table I. G_m is the extrinsic gate transconductance given by the real part of Y_{21}, $C_{\rm gg}$ is the total extrinsic gate capacitance given by the imaginary part of Y_{11}/ω, R_s is the source series resistance, and R_g is the gate resistance. The parasitic series resistances are extracted at high frequencies under the dc bias conditions of interest with the method described in [13].

Despite the substantially differing saturation transconductance values (Table I and Fig. 2) for the two analyzed wafers, the extracted cutoff frequencies are surprisingly very similar (Table I and Fig. 1). This could be explained by the difference of total gate capacitance extracted for both transistors shown in Fig. 3. Indeed, a high G_m is observed for the SB MOSFET annealed at 500 °C, but a higher $C_{\rm gg}$ at the same time, which results in a nearly constant value. It is worth noting that the equivalent source series resistance depends on the annealing temperature, with lower value for the wafer annealed at 500 °C. This suggests that the device capacitance and series resistances vary as a result of the differing SB heights on the two wafers. This hypothesis is in agreement with the finite-element and Monte Carlo simulation results presented in [14] and [15], respectively.

The high measurement noise observed at low frequencies is related to the high impedance mismatch between the low capacitive input value of such a small transistor and the internal

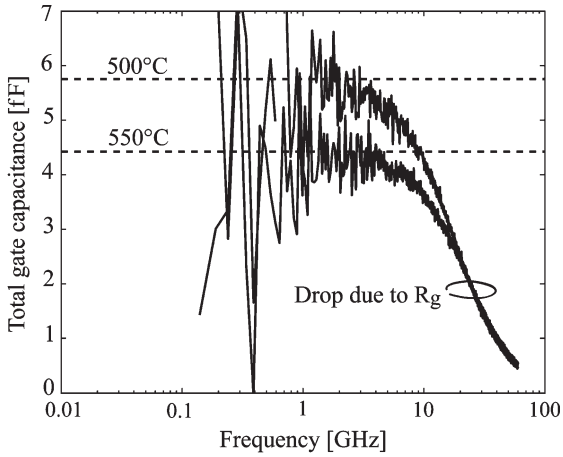

Fig. 3. Extracted extrinsic total gate capacitance versus frequency for wafers annealed at 500 °C and 550 °C.

reference impedance (50 Ω) of the vectorial network analyzer (VNA). Under this high mismatch level, the measurement dynamic of VNA limits the quality of the extracted parameters. But still, at low frequencies where R_g does not impact the extracted-capacitance values, the difference between extracted capacitances for both wafers can be clearly observed.

We note that the total gate capacitance $C_{\rm gg}$ extracted from the S parameters and given in Table I is lower than the oxide capacitance of 1.6 fF/μm [7], which is in contrast to the simulated and measured total gate capacitances in saturation for deep submicrometer DSD MOSFETs, as reported by Raskin *et al.* [16]. The lower capacitance value for the SB MOSFETs is linked to the presence of the SB as aforementioned, to the quantum effects, and also to the greatly reduced overlap capacitances, as discussed in [11].

IV. Conclusion

The RF performance of bulk Si PtSi source/drain SB MOSFETs with gate lengths of 85 nm has been analyzed for two different silicidation anneal temperatures. It has been demonstrated that the unity-gain cutoff frequency (f_T) is nearly independent of the silicidation anneal temperature, whereas the impact on the transconductance is important. Based on the extraction of an extrinsic small-signal equivalent circuit, the nearly unchanged value of f_T may be explained by the direct dependence of both the extrinsic transconductance and gate capacitance of SB MOSFETs on the SB height of the source- and drain-to-channel contacts.

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