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<b>Citation</b>	<b>Physica Status Solidi - Rapid Research Letters, 2016, v. 10 n. 9, p. 703-707</b>
<b>Issued Date</b>	<b>2016</b>
<b>URL</b>	<b><a href="http://hdl.handle.net/10722/231908">http://hdl.handle.net/10722/231908</a></b>
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# Effects of Y incorporation in TaON gate dielectric on electrical performance of GaAs metal-oxide-semiconductor capacitor

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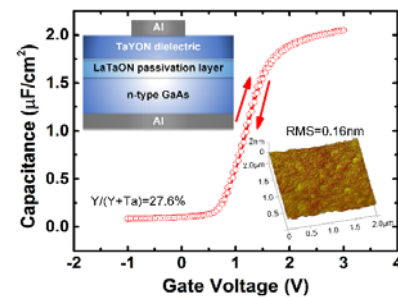
Received ZZZ, revised ZZZ, accepted ZZZ

Published online ZZZ (Dates will be provided by the publisher.)

**Keywords** GaAs MOS, High-k dielectric, Y incorporation, Interface-state density.

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In this study, GaAs Metal-Oxide-Semiconductor (MOS) capacitors using Y-incorporated TaON as gate dielectric have been investigated. Experimental results show that the sample with a Y/(Y+Ta) atomic ratio of 27.6% exhibits the best device characteristics: high k value (22.9), low interface-state density ( $9.0 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ ), small flatband voltage (1.05 V), small frequency dispersion and low gate leakage current ( $1.3 \times 10^{-5} \text{ A/cm}^2$  at  $V_{fb} + 1 \text{ V}$ ). These merits should be attributed to the complementary properties of  $\text{Y}_2\text{O}_3$  and  $\text{Ta}_2\text{O}_5$ : Y can effectively passivate the large amount of oxygen vacancies in  $\text{Ta}_2\text{O}_5$ , while the positively-charged oxygen vacancies in  $\text{Ta}_2\text{O}_5$  are capable of neutralizing the effects of the negative oxide charges in  $\text{Y}_2\text{O}_3$ . This work demonstrates that an appropriate doping of Y content in TaON gate dielectric can effectively improve the electrical performance for GaAs MOS devices.



Capacitance-Voltage characteristic of the GaAs MOS capacitor with TaYON gate dielectric (Y content=27.6%) proposed in this work with the cross sectional structure and dielectric surface morphology as insets.

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**1 Introduction** Advantages such as high electron mobility, direct bandgap, and high breakdown field make III-V compound semiconductors well-positioned in achieving better performance for high-power and high-speed MOS devices than Si [1]. Among them, GaAs MOS devices with high-k (dielectric constant) gate dielectric have received significant attention in recent years [2, 3]. The critical challenges for the GaAs MOS technology are to reduce the defect states near the valence band and meanwhile suppress the formation of the unstable native oxides of GaAs, whereby the Fermi-level pinning effect can be avoided at the high-k/GaAs interface [4]. Therefore, passivation of the GaAs surface becomes an essential approach for improving the performance of GaAs MOS devices. Previously, LaTaON has been demonstrated capable of effectively passivating the surface of both Ge

and GaAs, with reduced interface states and lower gate leakage current achieved [5, 6]. However, because of the hygroscopic nature of La-based materials, it seems not suitable to make LaTaON as gate dielectric. Recently, with a high k value of 20 ~ 30 (amorphous) [7],  $\text{Ta}_2\text{O}_5$  has been considered as a promising high-k material, especially in the DRAM [8], but its drawbacks like small bandgap (4.4 eV) and high concentration of oxygen vacancies might lead to large leakage current and charge trapping respectively [9, 10]. Moreover, it is worth noting that  $\text{Ta}_2\text{O}_5$  will react with the underlying substrate at high temperature, which will further degrade the device performance [11]. Although studies have pointed out doping nitrogen into  $\text{Ta}_2\text{O}_5$  (TaON) is capable of increasing its k value and reducing its border traps [12], the problems mentioned above still exist. On the other hand, the use of wide bandgap  $\text{Y}_2\text{O}_3$

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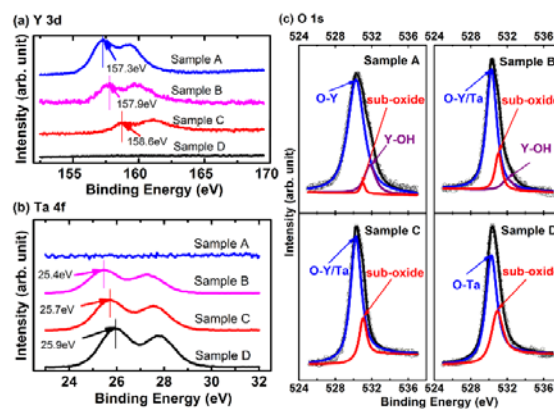
(5.5eV) can address the problem of leakage current, but its lower  $k$  value ( $\sim 14$ ) will limit further scaling of the device. In this work, a strategy by incorporating Y into TaON as gate dielectric of GaAs MOS capacitors has been proposed for improving interfacial and gate leakage properties meanwhile maintaining relatively high  $k$  value, riding on the advantages of wide bandgap of  $Y_2O_3$  and high- $k$  of  $Ta_2O_5$  concurrently. Moreover, by investigating the effects of Y-content in TaON gate dielectric, an appropriate Y/Ta ratio that enables GaAs MOS devices with optimal interfacial and gate leakage properties is obtained, with a high  $k$  value close to TaON and two-order lower gate leakage current than TaON devices.

**2 Experimental details** MOS capacitors were fabricated on Si-doped n-type GaAs wafers (100) with a doping concentration of  $0.5 \times 10^{18} \sim 1.0 \times 10^{18} \text{ cm}^{-3}$ . Wafers were first degreased in acetone, ethanol and isopropanol sequentially, and then dipped in diluted HCl to remove the native oxides, followed by sulfur passivation in  $(NH_4)_2S$ . After dried by  $N_2$ , the wafers were transferred immediately into the high vacuum chamber of a sputtering system. A thin LaTaON film ( $\sim 2 \text{ nm}$ ) as interfacial passivation layer was deposited by co-sputtering Ta and  $La_2O_3$  targets at room temperature in  $Ar/N_2$  ( $= 24/12$ ), followed by the deposition of TaYON gate dielectric layer ( $\sim 8 \text{ nm}$ ) by co-sputtering Ta and  $Y_2O_3$  targets in the same ambient. Different ratios of Y to Ta in the TaYON film were obtained by adjusting the DC/RF powers of Ta/ $Y_2O_3$  targets to 0A/55W, 0.03A/45W, 0.03A/35W and 0.03A/0W, denoted as samples A, B, C and D respectively. Subsequently, a post-deposition annealing (PDA) was carried out at  $600^\circ\text{C}$  for 60 s in  $N_2$  for all the samples. Al electrodes were then evaporated and patterned with an area of  $7.85 \times 10^{-5} \text{ cm}^2$ , followed by a forming-gas (95%  $N_2 + 5\% H_2$ ) annealing at  $300^\circ\text{C}$  for 20 min.

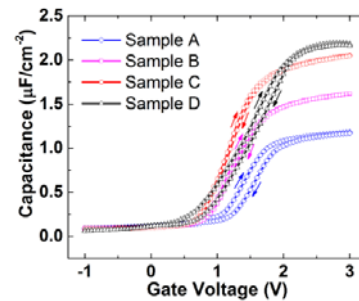
Capacitance-voltage (C-V) measurements were performed on MOS capacitors by HP 4284A. Gate leakage currents were tested by HP 4156A, and the thicknesses ( $T_{ox}$ ) and the bandgap of the dielectric films were measured by ellipsometry. Atomic force microscopy (AFM) was employed by Nanopics 2100 to evaluate the surface morphology of the gate dielectrics. Moreover, the chemical states in the high- $k$  dielectrics and at/near the high- $k$ /GaAs interface were analyzed by X-ray photoelectron spectroscopy (XPS).

**3 Results and discussions** XPS spectra of Y 3d, Ta 4f and O 1s are plotted in Fig. 1, from which the atomic ratio of Y to (Y+Ta) can be extracted to be 100%, 43.8%, 27.6% and 0% for the samples A, B, C and D, respectively. It has been reported that the oxygen vacancies in the dielectric film are positively charged and so an electric field can be generated [13, 14]. Since the core-level binding energy of an atom increases with a positive charge nearby [15], a shift of binding energy to higher value will happen when the amount of oxygen vacancies increases.

Obviously in Figs. 1a and 1b, both Y 3d and Ta 4f shift to lower binding energies as the Y content increases, indicating that Y can effectively passivate the oxygen vacancies in the TaON film. This can be confirmed by the O 1s spectrum in Fig. 1c (see more details on the subpeaks of O 1s in Table S1, supporting information), in which the intensity of the sub-oxide peak decreases with the increase of Y content, indicating the Y passivation role on oxygen vacancies. Moreover, the content of Y-OH bond caused by the slight hygroscopicity of  $Y_2O_3$  decreases from sample A to sample B and is negligible in samples C and D, implying its influence can be neglected at a relatively low Y content.



**Figure 1** XPS spectra of (a) Y 3d, (b) Ta 4f and (c) O 1s for the samples.



**Figure 2** High frequency (1MHz) C-V curves for the samples.

The 1-MHz C-V curves of the samples swept from inversion to accumulation and then back are shown in Fig. 2. The clockwise hysteresis for all the samples implying acceptor-like traps prevails in the dielectrics. Obviously, the accumulation capacitance per unit area ( $C_{ox}$ ) decreases with increasing Y content due to the lower  $k$  value of  $Y_2O_3$  than that of  $Ta_2O_5$ . However, the largest stretch out of C-V curve and a slight break down at high gate voltage are found in the sample D (TaON) with the largest  $C_{ox}$ , implying the worst interface quality. According to M.K. Bera, the dominant defects in bulk  $Y_2O_3$  are negative [16], which can be neutralized by the positively-charged oxygen vacancies in TaON, resulting in a smaller shift of C-V curve in the positive direction for lower Y content when

1 comparing the samples A, B and C. Although the C-V  
2 curve of the sample D begins transition from inversion to  
3 accumulation first, it reaches accumulation last due to its  
4 highest interface-state density ( $D_{it}$ ) described below.

5 The electrical and physical parameters of the samples  
6 extracted from their HF C-V curves are listed in Table 1.  
7 The equivalent k value ( $k_{eq}$ ) of the gate dielectrics can be  
8 calculated as

$$9 \quad k_{eq} = k_{SiO_2} T_{ox} / CET \quad (1)$$

$$10 \quad CET = k_0 k_{SiO_2} / C_{ox} \quad (2)$$

11 where CET is the capacitance equivalent thickness;  $k_0$  is  
12 the vacuum permittivity;  $k_{SiO_2}$  is the dielectric constant of  
13  $SiO_2$ . Flatband voltage  $V_{fb}$  is determined from flatband  
14 capacitance and thus the equivalent oxide-charge density  
15 ( $Q_{ox}$ ) can be obtained by

$$16 \quad Q_{ox} = -C_{ox} (V_{fb} - \Phi_{ms}) / q \quad (3)$$

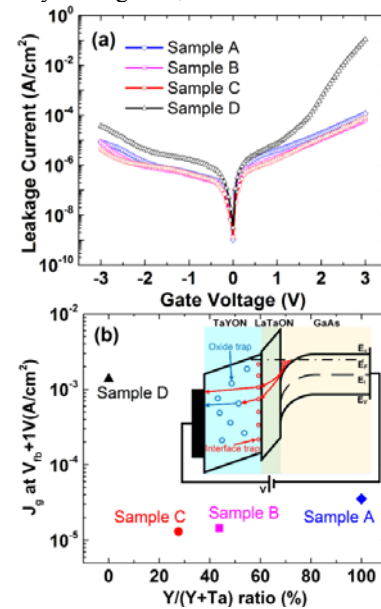
17 with  $\Phi_{ms}$  the work-function difference between the Al gate  
18 and GaAs substrate and  $q$  the electron charge. In Table 1,  
19 the two samples with TaYON as gate dielectric (the sample  
20 B and especially sample C) exhibit better electrical  
21 properties than the samples with TaON or YON as gate  
22 dielectric (the samples A and D). Positive  $V_{fb}$  for all the  
23 samples implies the presence of negative charges in the  
24 dielectric film.  $V_{fb}$  decreases from 1.37 V (for the sample  
25 A) to 1.05 V (for the sample C) with increasing Ta content,  
26 likely due to the neutralization between the effects of the  
27 positively-charged oxygen vacancies of TaON and the  
28 negative oxide charges of  $Y_2O_3$  as mentioned above.

29 **Table 1** Electrical and physical parameters of the samples.

Sample No.	A	B	C	D
Y/(Y+Ta) (%)	100	43.8	27.6	0
Bandgap (eV)	5.4	5.1	4.9	4.1
$T_{ox}$ (nm)	10.34	10.19	10.06	10.22
$C_{ox}$ ( $\mu F/cm^2$ )	1.17	1.61	2.05	2.18
$V_{fb}$ (V)	1.37	1.15	1.05	1.16
$Q_{ox}$ ( $cm^{-2}$ )	$-9.08 \times 10^{12}$	$-1.01 \times 10^{13}$	$-1.16 \times 10^{13}$	$-1.37 \times 10^{13}$
CET (nm)	2.97	2.13	1.71	1.59
$k_{eq}$	13.6	18.6	22.9	24.7
$D_{it}$ ( $cm^{-2}eV^{-1}$ )	$\sim 3.5 \times 10^{12}$	$\sim 1.0 \times 10^{12}$	$\sim 9.0 \times 10^{11}$	$\sim 8.5 \times 10^{12}$
Hysteresis (mV)	+160	+48	+35	+120
RMS (nm)	0.23	0.21	0.16	0.37

30  $D_{it}$  is extracted from the HF C-V curve by the Terman's  
31 method [17] for comparison (see the states distribution in  
32 mid-gap and more details in Fig. S1 and Table S2 of  
33 supporting information) and its value near mid-gap is listed  
34 in Table 1. Different values of  $D_{it}$  are obtained for the four  
35 samples even though they have the same LaTaON  
36 passivation layer on the GaAs substrate. This is because  
37 when the thickness of the passivation layer is small,

tunneling of carriers from the substrate becomes significant  
and the exchange of carriers between the states located at  
the dielectric/passivation-layer interface and the substrate  
can easily happen [18] (as shown and explained by Fig. S2.  
Among the four samples, the sample C ( $Y/(Y+Ta) = 27.6\%$ )  
exhibits the lowest  $D_{it}$ , least stretch-out and smallest  
hysteresis, which can result in least defect-related carrier  
scattering and thus highest carrier mobility, outweighing the  
slight reduction of k value relative to the sample D. Besides,  
the increased  $V_{fb}$  for the sample D (1.16 V) is possibly related  
to the larger stretch-out in C-V curve caused by its larger  
 $D_{it}$ .

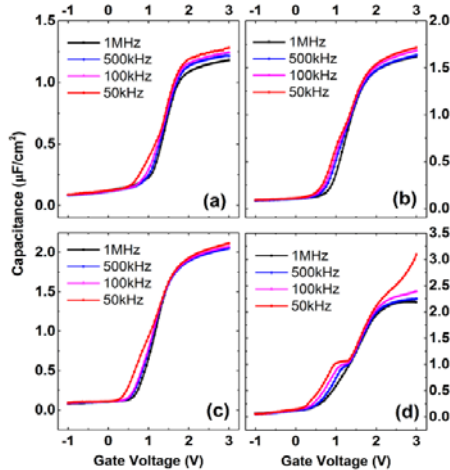


38 **Figure 3** (a) Gate leakage current density vs. gate voltage ( $J_g$ - $V_g$ )  
39 characteristics and (b) leakage current densities ( $J_g$ ) at  $V_g = V_{fb} + 1$  V  
40 for the samples A, B, C, and D.

41 Fig. 3a plots the gate leakage current density vs.  
42 voltage ( $J_g$ - $V_g$ ) curves of the four samples. The sample D  
43 with pure TaON as gate dielectric has the largest leakage  
44 current ( $1.85 \times 10^{-3} A/cm^2$  at  $V_g = V_{fb} + 1$  V), which should  
45 be ascribed to the small band gap of TaON and a large  
46 amount of oxide traps in the dielectric film. The samples B  
47 and C exhibit much smaller  $J_g$  than the sample D,  
48 indicating that incorporation of Y can effectively increase  
49 the band gap and passivate the traps of TaON. Although  
50 the samples B and C have almost identical  $J_g$ - $V_g$   
51 characteristics, the leakage current of the sample C is  
52 slightly smaller (e.g.  $1.30 \times 10^{-5} A/cm^2$  at  $V_g = V_{fb} + 1$  V)  
53 than that of the sample B ( $1.43 \times 10^{-5} A/cm^2$  at  $V_g = V_{fb} + 1$  V)  
54 according to Fig. 3b, which should be attributed to the  
55 smaller  $D_{it}$  of the former. Meanwhile, the sample A with  
56 pure YON as gate dielectric has larger leakage current  
57 ( $3.53 \times 10^{-5} A/cm^2$  at  $V_g = V_{fb} + 1$  V) than the samples B and C.  
This should be due to the larger  $D_{it}$  [19] of the sample A  
(as shown in Table 1) caused by the mismatch between the  
YON gate dielectric and LaTaON passivation layer due to

lack of Ta in the former, which might induce more dangling bonds, thus leading to trap-assisted tunneling of carriers as shown in the inset of Fig. 3b: under a positive gate voltage, the conduction band of GaAs is bent towards the Fermi level at the GaAs surface, and thus electrons can tunnel from the substrate to the traps at the dielectric/LaTaON interface and then collected by the gate electrode (via the traps in the dielectric and at/near the dielectric/passivation interface), resulting in higher leakage current [20, 21].

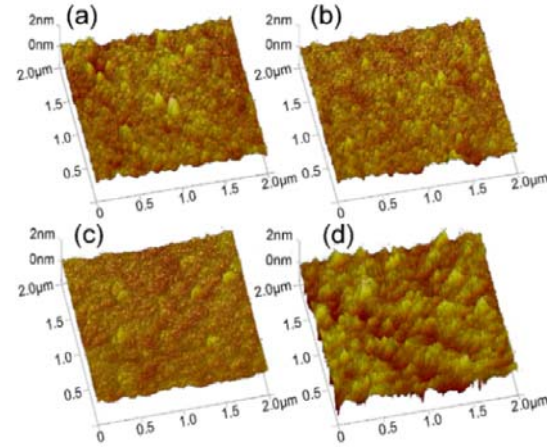
The C-V curves of the samples measured at 1 MHz, 500 kHz, 100 kHz and 50 kHz are displayed in Fig. 4. Since the presence of interface traps causes the frequency dispersion in the transition region, while the formation of an inhomogeneous layer at the gate dielectric/substrate interface (which induces a capacitance in series with the oxide capacitor) is the reason for the dispersion in the accumulation region [22, 23], the large  $C_{ox}$  increase and poor C-V behavior at low frequency for the samples A and D indicate poor interfacial property and Fermi-level pinning at their high-k/GaAs interface [24]. Small frequency dispersion is obtained for the samples B and C, with the smallest frequency dispersion for the sample C, which is consistent with its smallest  $D_{it}$ , further confirming that its interface quality has been improved by incorporating Y in its gate dielectric.



**Figure 4** Frequency dispersion of C-V curves: (a) sample A, (b) sample B, (c) sample C, and (d) sample D.

AFM images showing the dielectric surface morphology of the four samples are presented in Fig. 5, with their roughnesses in root-mean-square (RMS) listed in Table 1. Compared with the sample D (TaON), with Y incorporation, the RMS values of the samples B and C are improved from 0.37 nm to 0.16 nm and 0.21 nm, which is probably be ascribed to the different ionic radius of  $Y^{3+}$  (0.090 nm) with that of  $Ta^{5+}$  (0.064 nm) that improves the uniformity of the dielectric film by inducing mismatch between  $Y^{3+}$  ion and TaON (see detailed explanation in Fig. S3, supporting information) [25]. However, the increased

RMS value of the sample A (0.23 nm) is possibly caused by the mismatch between YON and LaTaON passivation layer as mentioned and the slight hygroscopicity of  $Y_2O_3$ . Good correlation of surface roughness and electrical properties discussed is obtained: the rougher the film, the worse the interfacial quality and gate leakage properties are.



**Figure 5** Surface morphology of TaYON dielectric with different Y contents: (a) sample A, 100%, (b) sample B, 43.8%, (c) sample C, 27.6%, and (d) sample D, 0%.

Considering the electrical properties of the devices might be influenced by the interface states at the LaTaON/GaAs interface, XPS test at the GaAs surface is implemented (see details of Ga and As 3d XPS spectra in Figure S4 and Tables S3 and S4, supporting information) peaks of As and Ga 3d spectra of the four samples exhibit almost the same binding energies and contents, meaning that under the presence of the LaTaON passivation layer, the interface quality at the surface of the GaAs substrate is hardly affected by the gate dielectric. Therefore, the  $D_{it}$  difference among the four samples might be caused by the interface states between the TaYON gate dielectric and LaTaON passivation layer.

**3 Conclusions** The effects of Y-doping in TaON gate dielectric on the performance of GaAs MOS capacitors with LaTaON passivation layer are investigated. With Y incorporation, the dielectric surface roughness is improved and the oxygen vacancies in TaON are effectively passivated. Moreover, the positively-charged oxygen vacancies in TaON can neutralize the effect of the negative oxide charges in  $Y_2O_3$ . Accordingly, gate leakage and  $D_{it}$  are significantly improved by incorporating Y in TaON dielectric, outweighing the slight loss in  $k$  value. Smallest dielectric roughness, lowest interface-state density, smallest leakage current and acceptably high  $k$  value can be achieved by an appropriate doping of Y content in TaON with an atomic  $Y/(Y+Ta)$  ratio of 27.6%. This work demonstrates that Y doped TaON can be a promising gate dielectric to achieve high-performance GaAs MOS devices.

1  
2 **Acknowledgements** This work was financially  
3 supported by University Development Fund  
4 (Nanotechnology Research Institute, 00600009) of the  
5 University of Hong Kong and the National Natural Science  
6 Foundation of China (Grant No. 61176100, 61274112).  
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