A study on the effects of accumulated and independent clock jitter on discrete-time delta-sigma modulators.

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IMTC 2005 – Instrumentation and Measurement
Technology Conference
Ottawa, Canada, 17-19 May 2005

A Study on the Effects of Accumulated and Independent Clock Jitter on Discrete-Time Delta- Sigma Modulators

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Abstract- *This paper describes the effects of accumulated and independent clock jitters on the tonality and the Signal-to-Noise Ratio (SNR) of discrete-time* ***Δ-Σ*** *modulators. Simulations demonstrate that accumulated clock jitter exhibits increased tonality in the magnitude spectrum of the* ***Δ-Σ*** *modulator output especially at very high frequencies, while having no significant effect on the SNR. Independent clock jitter, on the other hand, degrades SNR performance but causes no increase in tonality.*

I. INTRODUCTION

Clock jitter leads to non-uniform sampling of the analog input signal. As a result of the increase in clock jitter, the quantization noise power increases thus reducing the SNR [1]. The practical limitations associated with clock jitter in sampling circuits were discussed in [2]-[3]. Clock jitter in analog-to-digital conversion occurs at the sample-and-hold (S/H) circuit and in the sampling clock generator [4]. The former is termed aperture jitter and is caused by thermal noise in the S/H circuit. It is commonly modeled as an independent White Gaussian process [5], [6] and [7]. Accumulated clock jitter is caused by the phase noise of the oscillator and is modeled as a Wiener Process [1], [5], [8].

Independent jitter degrades the SNR performance of Discrete-Time (DT) and Continuous Time (CT) Δ-Σ modulators [7]. However, DT Δ-Σ modulators are insensitive to accumulated clock jitter (in the DAC feedback path) when realized using switched-capacitors. The reduction in the SNR is negligible as compared to CT Δ-Σ modulators. A detailed literature survey has shown that the effects of accumulated clock jitter in CT Δ-Σ modulators are reported in [9]. In addition, the effects of independent jitter in the S/H circuit for DT Δ-Σ modulators have been documented in [10]-[11].
However, realistic jitter consists of independent as well as accumulated jitter (VCO phase noise), whose effects on SNR and tonality are the subject of this paper.

The statistical properties and the modeling of independent and accumulated jitters are described in Section II. Section III describes the occurrence and the effects of clock jitter in Δ-Σ modulators. Section IV explains the tonality index used to evaluate these Δ-Σ modulators. Section V provides detailed simulations of the effects of clock jitter on the resolution and tonality content of DT Δ-Σ modulators. Section VI gives a summary covering the findings of this paper.

II. NON-UNIFORM SAMPLING

A harmonic signal with frequency f and random phase Φ can be represented as:

$$x(t) = \exp\{j(2\pi ft + \Phi)\} \quad (1)$$

Assuming that the signal is sampled randomly, the sampling instants are given by:

$$t_n = nT + \alpha_n, n = 0,1,2,..., N-1 \quad (2)$$

where T is the average sampling interval, N is the sequence length and $\alpha_i = \alpha_1, \alpha_2, .., \alpha_{n-1}$ are the random deviations from nT. Accordingly, the resulting sequence is

$$x(n) = \exp\left\{j(2\pi fT(n + \tfrac{\alpha_n}{T}) + \Phi)\right\} \quad (3)$$

In the case of independent jitter, the sampling instants (with respect to the average) are independent. The $\{\alpha_i\}$s are independent random variables (rv) having a Probability Density Function (PDF) P_α, whose statistical properties are non-varying. This is why jitter is often described as stationary clock jitter. This jitter is associated with S/H circuits and occurs when an accurate sampling clock is corrupted by noise. The time response (top), auto-correlation function (middle) and histogram distribution (bottom) of independent jitter for 10,000 samples (variance 0.001) are shown in Fig. 1.

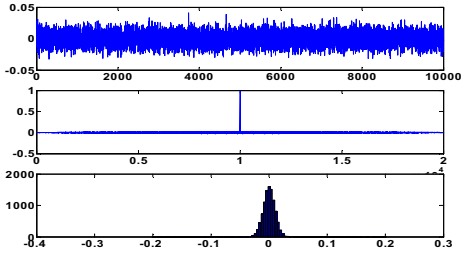

Fig. 1. Characteristics of Independent Jitter.

In the case of accumulated jitter, the sampling is considered as a random process in which jitter of the sampling instants with respect to the periodic sampling instants is the accumulation of jitter from different intervals.

Jitter is therefore termed as accumulated or white noise integrated jitter [6]. This type of jitter is encountered when the sampling clock has limited stability. Here if we define τ_i as the jitter of the ith sampling interval [t_{i+1}-t_i=T+T_i, i=0, 1, N-1], then the jitter of the sampling instants is the accumulation as given by:

$$\alpha_n = \sum_{i=0}^{n} \tau_i, \tau_0 = 0, n = 0,1,..,N-1. \quad (4)$$

Here $\{\tau_i\}$ are the rvs with PDF P_τ. As seen, the statistics of τ_i are stationary, while those of α_n are not. The variance of jitter increases as a function of time. The sampling due to accumulated clock jitter is therefore termed as non-stationary clock jitter. The noise distribution resembles a Random Walk and is termed Brown Noise as its samples resemble Brownian Motion [12]. It can be modeled as a Wiener Process [5]. The time response (top), auto-correlation function (middle) and histogram distribution (bottom) of accumulated jitter for 10,000 samples (variance 0.001) are shown in Fig. 2.

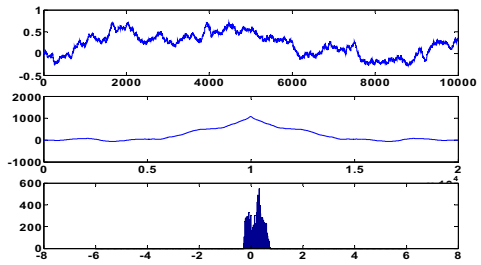

Fig. 2. Characteristics of Accumulated Jitter.

The auto-correlation function of independent jitter is an impulse function and that for accumulated jitter approximates a triangular function as demonstrated in Fig. 1 and Fig. 2. They therefore have different PDFs.

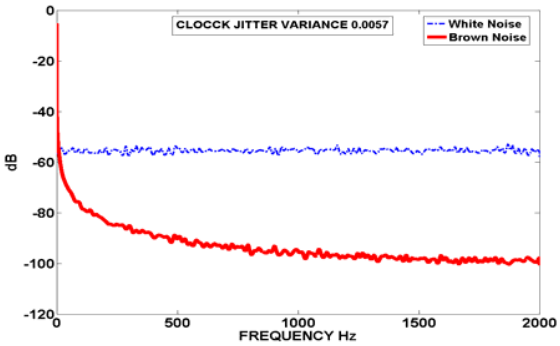

Fig. 3. Power Spectra for White & Brown Noise.

The power spectrum for independent jitter is constant over the entire frequency range (white noise), while that of accumulated jitter is frequency dependent ($1/f^2$ Brown Noise [12]). The power spectral densities of Brown and White Noise jitter samples using Burg's estimate [13] for an Auto-Regressive (AR) process (of order 200), 16384 FFT points and a sampling frequency of 4000 Hz are shown in Fig. 3.

III. CLOCK JITTER IN Δ-Σ MODULATORS

There are three sources where jitter can occur in DT Δ-Σ modulators; the S/H, the quantizer input and the DAC output. The jitter between the filter and the quantizer will have negligible effect, since the filter is designed to settle to a given accuracy within ½ the sampling period. If the quantizer's sampling instant occurs early or late, the decision remains correct, since the filter output would have already settled. Considering a typical feedback DAC waveform, DT Δ-Σ modulators are relatively insensitive to jitter due to the sloping pulse form of the feedback [9]. This slope arises from the capacitor being discharged over a switch with a very low 'on-resistance'. Therefore, the slope is very steep, following the time constant τ_{RC}=R_{on}.C. Since most of the charge transfer in a switched-capacitor (SC) circuit occurs at the beginning of the clock period, clock jitter introduces a minimal amount of error of the charge lost by the capacitor [9].

In contrast, for CT Δ-Σ modulators charge is transferred at a constant rate over the clock period, thus the charge loss due to clock jitter is proportionately greater than that of switched-capacitor Δ-Σ modulators. In CT Δ-Σ modulators, there are two error sources due to a jittered clock. The main type of error enters the system through the feedback DAC. Here the accumulated clock jitter dominates, because it enters the modulator at its input without noise-shaping. However, independent jitter will be noise-shaped by the modulator noise transfer function [7]. As a result of the noise shaping, the quantiser clock jitter will have a minimal effect on the passband performance of the modulator.

Simulations of accumulated jitter at the front-end of S/H DT Δ-Σ modulators indicate the formation of non-white noise skirts [7]. Therefore, while independent jitter produces a white noise floor, one must expect non-white spectral noise if accumulated jitter is present. While having no profound effect on the SNR, the accumulated jitter would be conducive to the formation of tones, since it has a coherent distribution. This is because for the same variance, the noise power across most of the spectrum for accumulated jitter is significantly less compared with white jitter as shown in Fig. 3. This corresponds to the addition of comparatively less random noise (dither) to the Δ-Σ modulator.

Moreover, since the power of accumulated jitter decreases as the inverse square of frequency ($1/f^2$), the high frequency components are subjected to less dither. This explains why most dominant tones occur in the spectral region (f_S/4 to f_S/2). On the other hand, independent clock jitter is likely to degrade the SNR more severely in comparison as the power across the spectrum for white jitter is greater compared to accumulated jitter for the same variance as shown in Fig. 3.

IV. TONALITY

The magnitude spectrum of the output of a Δ-Σ modulator contains discrete tones which are objectionable primarily in audio and other applications [14]. The tonality content in the magnitude spectra of Δ-Σ modulators can be evaluated using a Tonality Index (TI) [15]. This is defined as the ratio of the power in the dominant FFT bins to the total power of the input signal. The expression in (5) gives an adequate approximation of the tonality indices for white noise.

$$\tau_{bias} \approx \frac{2m}{N}\left[\ln\left(\frac{N}{2m}\right)+1\right] \tag{5}$$

where N is the FFT length and m is the number of dominant bins. In order to account for this skewing effect, the estimated bias is subtracted and the resulting index renormalized. The resulting tonality index is given by:

$$TI = \frac{\tau_o - \tau_{bias}}{1-\tau_{bias}} \tag{6}$$

V. SIMULATIONS

Behavioral-level simulations were performed in MATLAB SIMULINK to quantitatively determine the effect of independent and accumulated clock jitters on the resolution and tonal content of the second-order DT Δ-Σ modulator shown in Fig. 4.

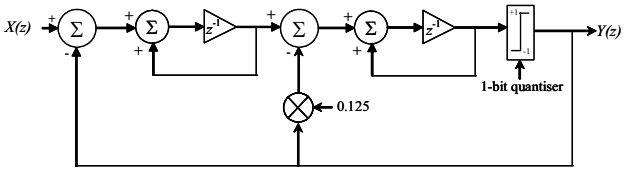

Fig. 4. Second order DT Δ-Σ modulator.

The parameters employed to conduct these simulations were m = 10, N = 16384, OSR = 105 and a single sinusoidal input of ν = 0.002 to the modulator.

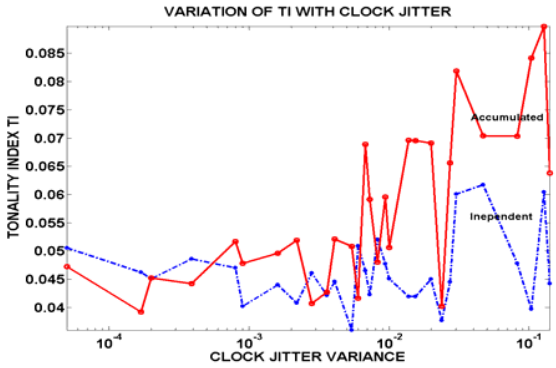

Fig. 5. Variation tonality index with clock jitter .

The results in Fig. 5 demonstrate that accumulated clock jitter exhibits more spectral tones in the Δ-Σ modulator output as indicated by the higher tonality index values. Moreover, the tonality index is observed to rise significantly with increased clock jitter variance. The difference of the tonality indices corresponding to accumulated and independent clock jitters are less significant for the clock jitter variance range (10^{-4} - 10^{-2}), but become markedly significant for a clock jitter variance in excess of 10^{-2}.

Fig. 6 shows that independent clock jitter degrades the SNR more severely in comparison with accumulated clock jitter. The differences in the SNR curves of the two jitters become considerably higher by as much as 25 dB for large clock jitter variance values. Simulations show the presence of a 'jungle of tones' between the $f_S/4$ to $f_S/2$ frequency range. Detailed power calculations reveal that this is the region where the 10 largest tones occur.

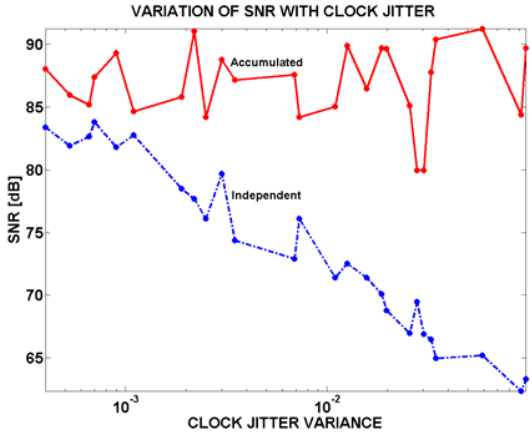

Fig. 6. Variation of SNR with clock jitter.

The power variation of these tones comparing the ideal case (no jitter) with the two types of clock jitter, are shown in Fig. 7.

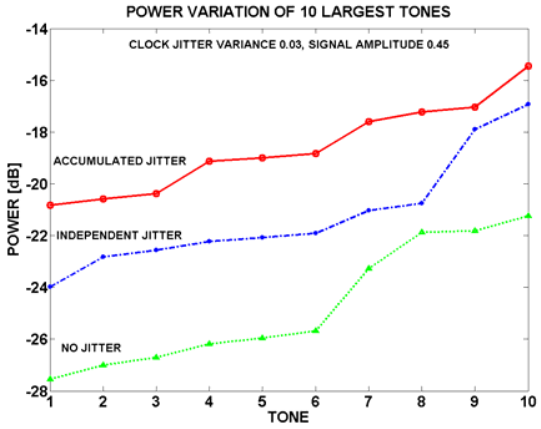

Fig. 7. Power of Ten Largest Tones.

As seen the presence of accumulated jitter increases the power of the ten most dominant spectral tones of the

modulator output in Fig. 8 by more than 6 dB compared with the ideal (no jitter) case. The proximity of these tones to $f_S/2$ yields inferior resolution as some of these tones can be folded to the baseband region.

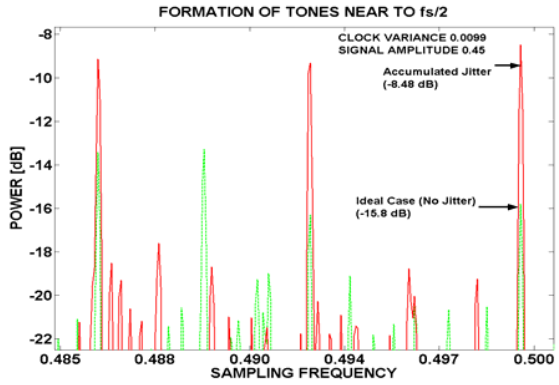

Fig. 8. Formation of tones near to $f_S/2$.

Fig. 9 shows the power variation of the ten largest tones for three different signal amplitudes.

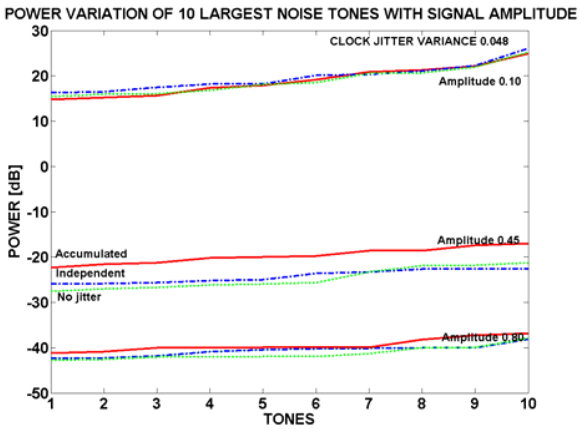

Fig. 9. Power variation with signal amplitude.

Fig. 10 demonstrates that the tonality indices are highest for small input amplitudes. They reduce quite steeply when the modulator input amplitude is 0.4 then become relatively constant for modulator input amplitudes greater than 0.6. Further simulations were carried out for a composite input signal to the modulator consisting of three tones at normalized frequencies of (1/250, 1/125, 1/63) with random amplitudes of 0.45, 0.225 and 0.337 respectively. The corresponding tonality indices for the ideal, independent and accumulated clock jitter case for a clock variance of 0.0405 were 0.0388, 0.0503 and 0.0999. These results confirm that accumulated clock jitter increases the tonal power even for composite input signals. The variation of TI for sinusoidal signals with dc offsets (0.000005, 0.0005 & 0.005) is shown in Fig. 11. It is observed that for small dc offsets (5×10^{-6}) the effect is the same as for pure sinusoidal signals. However as the dc offset is increased, the TI for both jitters decreases as well as the difference between them for various values of clock jitter. The simulation results in Fig. 12 demonstrate that the use of random initial conditions over zero initial conditions in the first accumulator consistently reduce the TI. These different- valued initial conditions increase the randomisation of the quantisation noise of the Δ-Σ modulator.

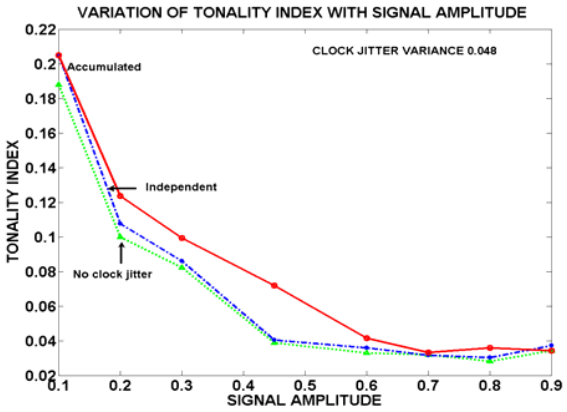

Fig. 10. Variation of tonality index with signal amplitude.

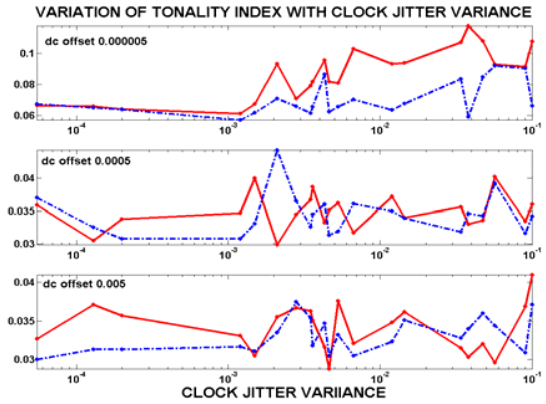

Fig. 11. Variation of tonality index for dc offset signals.

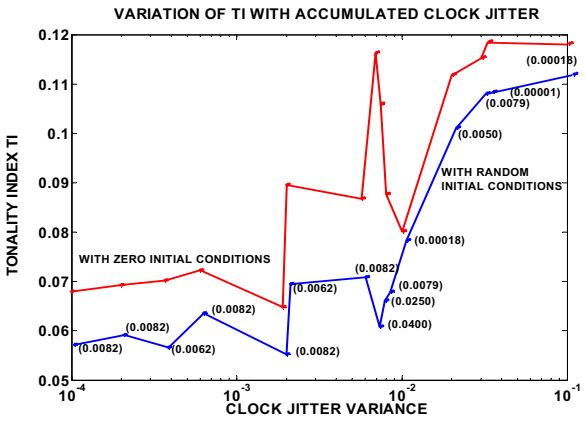

Fig. 12. Variation of tonality index with random initial conditions.

Fig. 13 shows that the use of random initial conditions also produces small improvements in the SNR for certain values of clock jitter variance. Simulations undertaken for a non-ideal Δ-Σ modulator showed increases in the TI as the finite dc op-amp gain decreased from ∞ to 1.13.

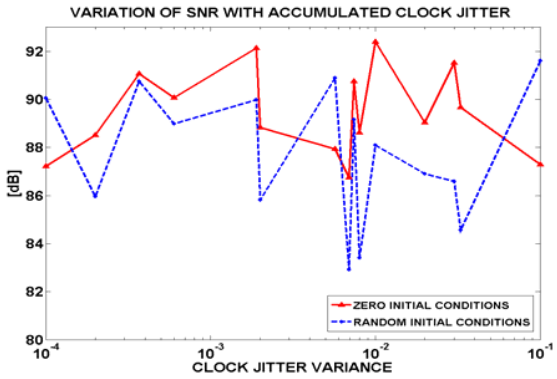

Fig. 13. Variation of SNR with random initial conditions.

VI. CONCLUSION

This paper has demonstrated through detailed simulations for single tone and multi-tone input signals that accumulated jitter significantly increases the tonal output of a DT second-order Δ-Σ modulator at high frequencies, while remaining relatively insensitive to the SNR. However, the use of random initial conditions in the first accumulator was shown to reduce the tonal content. Independent clock jitter was shown to result in inferior SNR, while having very little effect on tonality. The effects of accumulated and independent clock jitters for non-ideal discrete-time Δ-Σ modulators will be reported in a future publication.

REFERENCES

[1] Awad, S., S., "Analysis of Accumulated Timing-Jitter in the Time Domain", *IEEE Trans. IMTC.*, vol. 47, No.1, Feb 1998.

[2] Wagday, M., F., Awad, S., S., "Effect of Sampling Jitter on some Sinewave Measurements", *IEEE Trans. IMTCs.,* vol.39, pp.86-89, Feb 1990.

[3] Souders, T., M., Flach, D., R., Hagwood, C., Yang, G., L., "The Effects of Timing Jitter in Sampling Systems", *IEEE Trans. I MTCs.,* vol. 1M-39, pp. 80-85, Feb 1990.

[4] Kopmann, H., Gockler, H., Abdulazim, M., "Analog-to-Digital Conversion & Flexible FDM Demultiplexing Algorithms for Digital On Board Processing for Ultra Wideband FDM Signals", DSP Group (DISPO), Ruhr-Universitat Bochum, D44780 Bochum, Germany.

[5] Lohning, M., Fettwies, G., "The Effects of Aperture Jitter and Clock Jitter in Wideband ADCs", *Vodafone Chair Mobile Communication Systems,* Dresden University of Technology, D01061 Dresden, Germany.

[6] Berkovitz, A., Rusnak, I., "FFT Processing of Randomly Sampled Harmonic Signals", *IEEE Trans. Sig. Proc.,* vol. 40, No.11, Nov 1992.

[7] Ortmanns, M., Gerfers, F., Manoli, Y., "Fundamental Limitations of Jitter Insensitivity in Discrete and Continuous-Time Sigma Delta Modulators", *ISCAS*, 2003.

[8] Demir, A., Vincentelli, ALS, "Simulation of Phase Noise in Open Loop Oscillators", *IEEE Custom & Integrated Circuits Conference,* 1996.

[9] Ortmanns, M., Gerfers, F., Manoli, Y, "Clock Jitter Insensitive Continuous-Time Sigma Delta Modulators", *IEEE ICES 2001.*

[10] Malcovati, P., Brigati, S., Francesconi, F., Maloberti, F., Behavioral Modeling of Switched-Capacitor Σ-Δ Modulators", *IEEE Transactions on Circuits & Systems,* vol. 50, No. 3, Mar. 2003.

[11] Zare-Hoseini, H., Shoai, O., Kale, I., "Precise Behavioral Modeling of High-Resolution Switched-Capacitor Σ-Δ Modulators", *IMTC* Como, Italy, 18-20 May 2004.

[12] Clark, J., J., *Advanced Programming Techniques for Modular Synthesizers,* Dept. of Elect. & Compt. Engineering, Centre For Intelligent Machines, McGill University, Montreal Canada.

[13] Proakis, J., G., Manolakis, D., G., *Digital Signal Processing, Principles, Algorithms & Applications,* Prentice Hall, 1995.

[14] Norsworthy, S., R., "Effective Dithering of Sigma-Delta Modulators", Proceedings *IEEE Int. Sym. Circuits & Systems,* pp. 1304-1307, 1992.

[15] Schreier, R., "On the Use of Chaos to Reduce Idle-Channel Tones in Delta-Sigma Modulators", *IEEE Transactions on Circuits & Systems,* vol. 41, no. 8, pp. 539-547, Aug 1994.