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VLSI Architectures and Rapid Prototyping Testbeds for Wireless Systems

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***Abstract*— The rapid evolution of wireless access is creating an ever changing variety of standards for indoor and outdoor environments. The real-time processing demands of wireless data rates in excess of 100 Mbps is a challenging problem for architecture design and verification. In this paper, we consider current trends in VLSI architecture and in rapid prototyping testbeds to evaluate these systems.**

The key phases in multi-standard system design and prototyping include: *Algorithm Mapping to Parallel Architectures* – based on the real-time data and sampling rate and the resulting area, time and power complexity; *Configurable Mappings and Design Exploration* – based on heterogeneous architectures consisting of DSP, programmable application-specific instruction (ASIP) processors, and co-processors; and *Verification and Testbed Integration* – based on prototype implementation on programmable devices and integration with RF units.

***Index Terms*— Rapid prototyping, application-specific architectures, reconfigurable computing, digital baseband processing.**

I. Introduction

In this paper, we focus on strategies to explore, design and implement advanced architectures for new and multiple standards for wireless devices. The main focus will be on the **digital baseband** which recovers packets of transmitted information from noise corrupted received radio signals. An approach for enabling high-performance multi-standard wireless access [1] is to exploit fundamental commonalities in wireless baseband modules in various standards through the creation of Application Specific Instruction Processors (ASIPs).

Table I shows a representative set of standards to highlight the differences in data rates and application domain. The last column in Table I considers a block common to all the standards, modulation, to show that each standard uses a different modulation technology. Though seemingly different in their details, these wireless standards have several key similarities to enable efficient reconfiguration, (see Figure 1), that can be exploited in new processor architectures. Testbeds to explore these multiple antenna systems are emerging at many universities including Rice Univ., the 4G Lab at the Univ. of Oulu with Elektrobit [2], UCLA [3], the Univ. of Texas at Austin [4], and at Dresden Univ. of Technology and Signalion [5].

A. High Data Rate Embedded System Architectures

As communications algorithms transition to wireless embedded systems, a number of key issues and challenges arise based on algorithm partitioning, scheduling, and hardware resource allocation. Methodologies for embedded system design [10] are important to the design process. Many algorithms in signal processing systems which exhibit synchronous dataflow properties [11], [12], benefit from multi-processor implementations. Due to the variation in parallelism that is evident in many of these embedded systems, processor configurability and customized field programmable co-processors are increasing in importance [13]–[15].

General Purpose and DSP Processors: The need for multiple standard algorithm analysis and heterogeneous system partitioning is due to the fact that wireless algorithms present a high data rate yet unbalanced real-time workload. General purpose processors (GPP) do have potential for use in wireless systems however, their power consumption and cost are serious limitations. These "software radio" systems consist of mainly general-purpose processors and are therefore completely flexible and adaptable. However, the flexibility comes at the cost of reduced data-rate, even in the prototyping design phase, and significantly higher power consumption compared to the ASIC solution. DSP chips have been successful in current second generation wireless devices, however, 3G and 4G processing greatly exceeds the capabilities of DSP chips [16]–[18].

Application Specific Instruction Processors (ASIP): A new class of expandable media processors and co-processors are emerging that have enormous potential for wireless networks, for example the "Imagine" stream architecture [19] and the Transport Triggered Architecture [20]. These programmable parallel processors have a Very Long Instruction Word (VLIW) structure and the associated simulation tools to support architectural extensions and custom functional units to create *Wireless Application-Specific Instruction Processors (ASIPs)*. Due to the increased costs for design, test and fabrication of ASICs, recent related research is focusing on design methodologies, machine description languages, and functional unit selection for the ASIP design flow [21] along with integration of ASIPs into both FPGA and System on a Chip [22] architectures. Power reduction and power control through functional unit gating is an important factor in ASIP system [23] design. The use of ASIP architectures and hardware power-reduction provide a unique compromise between a general programmable processor and fixed function ASIC.

Custom FPGA / VLSI Architectures: In order to support the high data rates in wireless systems, a number of key subsystem blocks have been implemented as fixed ASICs [24], [25]. These ASICs offer benefits from advances in VLSI density. For example, architectural transformations, such as serial and parallel functional unit configurations, are utilized to adapt complex decoder algorithms to various physical system constraints [26]–[28].

TABLE I

MAJOR MOBILE WIRELESS STANDARDS: COMMUNICATION RANGE, PEAK DATA RATES AND BASEBAND MODULATION.

Network	Range	Data rates	Modulation
Personal Area (IEEE 802.15 [6])	10 m	55 Mbps	Frequency-hopping (FH)
Local Area (IEEE 802.11a [7])	100 m	54+ Mbps	FH, DS-CDMA or OFDM
Wide Area (3G, CDMA2000 [8])	2+ miles	2+ Mbps	DS-CDMA
Wide Area 4G [9]	up to 2 miles	100+ Mbps	MC-CDMA or OFDM

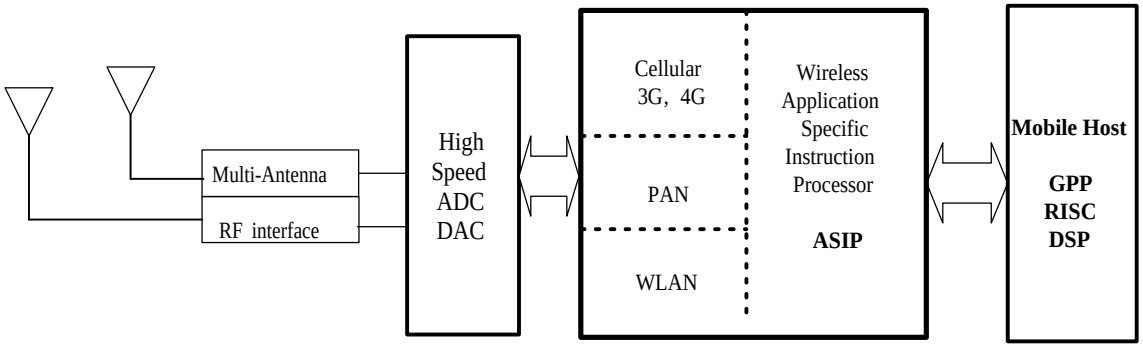

Fig. 1. Wireless communication system testbeds can be modified to support various emerging standards through heterogeneous processing with FPGA and DSP components programmed for the application specific algorithms.

A traditional approach is the creation of multiple fixed ASICs to support each of the wireless standards. The fully ASIC solution leads to a complicated system with a high part count. More importantly, ASIC based systems cannot be readily expanded to accommodate future wireless standards. Although FPGA systems are playing a major role in system design and prototyping by allowing flexibility, the higher power levels are inappropriate for volume mobile battery powered devices.

II. APPLICATION-SPECIFIC VLSI ARCHITECTURES

The focus of many research testbeds is in addressing novel schemes for fourth generation systems that will contain multiple antennas and multi-carrier W-CDMA systems to provide beyond 100 Mbps wireless access. There are many challenges to applying 3G to 4G [9], [29]–[31] which are the topics of current research. A main goal in rapid prototyping is the close integration of algorithm analysis, design exploration, and simulation and integration to produce architectures structured for wireless applications. The methodology is threefold: a detailed *algorithm analysis* covering area and time and power complexity, is followed by exploiting possibilities for *system configurability*, leading to the use of a flexible *research platform* to investigate and evaluate system performance tradeoffs.

A. Algorithm Mapping to Parallel Architectures

The physical layer of a typical communication system processes streams of data during both transmission and reception. For example, in voice transmission in a cellular W-CDMA system the input source is first sampled and then passed through a source coder. Then the signal passes through a channel encoder and modulator before a spreading code (composed of chips) is applied. The signal is then pulse shaped before being sent to the RF transmitter. At Rice, we have developed algorithms and real-time ASIC architectures for these wireless system algorithms [28], [32]–[36], One of our current focus areas is on design exploration for ASIP architectures for efficient mapping of these high data rate algorithms. The important issue for system design is that the data rate and corresponding computational workload increases as the signal approaches the transmitter due to the redundant error correcting information added.

WLAN systems are being introduced in high data rate demand "hot spots" in cellular networks, especially in schools, conference centers, and airports. There is great synergy developing between cellular and WLAN systems for next-generation data networks. The key blocks include: QAM modulation before the FFT blocks surrounded by serial to parallel (S/P) and parallel to serial (P/S) converters for high data rate transmission, along with cyclic prefix (CP) insertion and removal, and Viterbi decoding to correct for channel conditions.

The key challenge in algorithm mapping for wireless systems relates to modelling of the complexity of the various major application blocks. In an heterogeneous architecture of DSP, ASIP, and FPGA devices, the partitioning of the system, and the assignment of blocks to hardware and software devices is critical. Because of these challenges, initial partitioning may not yield system improvements. Each major algorithm block is characterized by data rate, latency, potential parallelism, and power budget. In addition, algorithm refinement and fixed-point wordlength analysis are key for reducing implementation complexity. The data communication between each major block also affects system performance.

1) Multi-Standard Operation and Configuration Challenges: Support for multi-standard operation is both difficult and challenging for power efficient wireless systems. In this

subsection, we describe configurable VLSI ASIC architectures for channel estimation and decoding, and mention the operational variations that motivate and challenge successful ASIP architectures.

Example 1: Joint Channel Estimation-Detection and FFT - ALU Parallelism: A major area of commonality between these wireless standards is in the complexity of the channel estimation and detection in W-CDMA compared with channel estimation and FFT in WLAN. Here the functionality is different, but the use and amount of parallelism is highly related. A major block in the W-CDMA structure is the channel estimator block that determines the delays and attenuations introduced in the wireless channel and then feeds this information to the detector. Many of the algorithms for channel estimation, channel equalization, and detection can benefit from a parallel array of multipliers and adders for high data rate applications [37], [38]. Similarly, for WLAN, a key block in the transmitter and receiver is the FFT/IFFT that relates the serial data stream with the parallel multiple RF carriers used for transmission.

Several key system parameters will determine the parallelism potential for the system. For W-CDMA, the spreading code which can vary from 4 to 256 chips per data bit depends on the user's data rate and system configuration. Since this "spreading" or processing gain allows more users in the cellular system while effectively multiplying the data rate processing requirements, it determines system complexity. For WLAN systems based on OFDM, the number of carriers used, typically 64, determines the number of points in the FFT to be performed in real-time.

Example 2: Reconfigurable Decoding Architectures - Scaling Interconnections: The Viterbi Algorithm is computationally demanding because a relatively simple set of operations must be applied to a large number of basic nodes or states at each discrete time step. The number of states grows exponentially with constraint length. With the limitations of present VLSI ASIC fabrication technology there has been a great incentive to devise algorithms to constrain interprocessor communication such that the area necessary to wire processor elements does not dominate the area required by the processors themselves. In fact, the Viterbi Algorithm has benefited much from research in the use of processor arrays, [27], [28] and these parallel array techniques are now being applied to Low Density Parity Check Codes [39].

B. Configurable Mappings and Design Exploration

With the rapid advance in computer-aided design tools, we are able to achieve better initial estimates of area, time, and power, for example with the Xilinx FPGA placement and Xpower power analysis tools.

ASIP architectures are emerging as candidate programmable processors in wireless communication and network processor applications. These architectures derive from the customization of ASICs with the flexibility of general purpose or DSP processors. In general, ASIPs are simpler, low-power processors with limited programmability focused on specific tasks. Several ASIP-like architectures and tools sets have been proposed in the literature and we will focus here on extensions of the Imagine [19] media stream processor and the Transport Triggered Architecture (TTA) [20], [40] concept shown in Figure 2 adapted for a channel equalizer application [38]. The TTA architecture is a VLIW system and a multi-cluster version of this system would be an interesting extension. Both

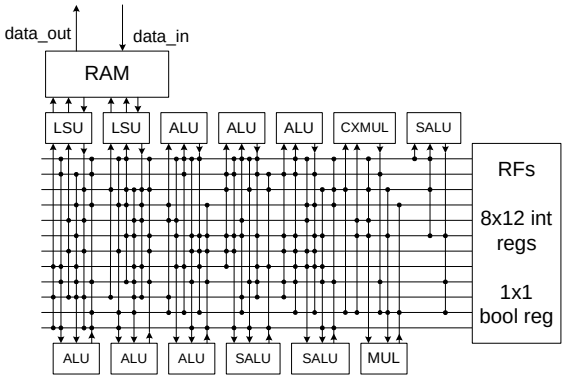

Fig. 2. Transport Trigger Architecture ASIP for Channel Equalization [38].

of these architectures are based on an extensible machine description (number of ALUs, load-store units, and register files) and retargetable compiler with accurate simulators and power models. The TTA tools are also capable of VHDL generation through the MoveGEN tools for synthesis and detailed modelling on FPGAs or ASIC libraries.

Design exploration is important for efficient use of the hardware units (adders, multipliers, register files) to tailor to a class of applications [41] as shown in Figure 3. As an example, from algorithm analysis of the underlying signal processing equations, we determined the ALU workload for multiuser channel estimation, multiuser detection and Viterbi decoding algorithms for a potential W-CDMA base-station. As can be seen from Figure 4, a 32-user system at 128 Kbps per user with spreading code length of 32 and a rate 1/2 decoding at constraint length 9, needs around 15 multipliers and 15 adders at 500 MHz to be kept busy every clock cycle doing useful work. Current single-processor DSP architectures do not contain enough functional units to meet these real-time requirements.

In order to investigate parallel ASIP architectures, we have also extended a stream processor simulator *isim* based on the "Imagine" media processor architecture at Stanford [19]. The simulator for the "Imagine" architecture is freely available and allows for architecture extension and exploration. This processor simulator allows us to investigate multi-cluster architectures with 10-1000's of ALUs. The base architecture is shown in Figure 5. Each cluster contains multiple functional units. A large general purpose stream register file (SRF) forms the heart of the system and is connected to the clusters, the memory system and the network. The stream register file is program-controlled and serves as a storage area for data used by other units. The number of memory accesses are minimized by keeping frequently used data in the SRF. The Imagine memory system allows multiple streaming accesses simultaneously and provides enough memory bandwidth for computational units.

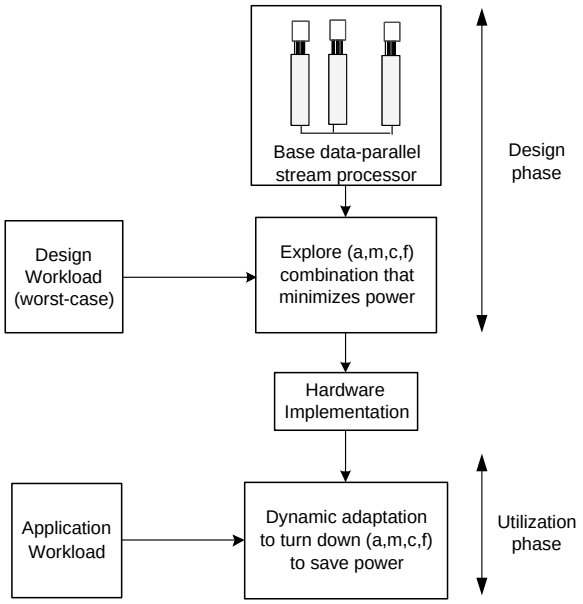

Fig. 3. Design Exploration Methodology for ASIP processors.

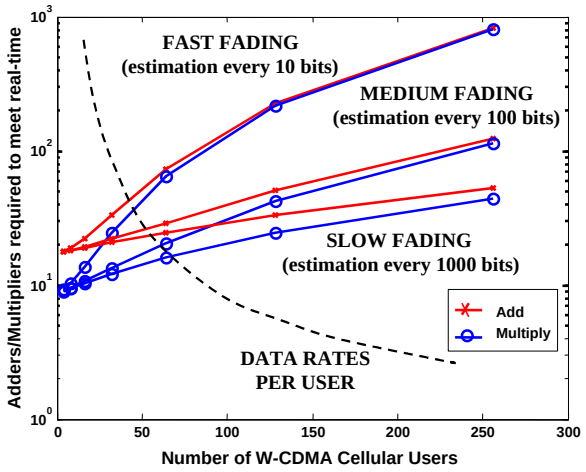

Fig. 4. Data rates and workloads for W-CDMA under various operating conditions.

III. Verification and Testbed Integration

The Rice Wireless Research Platform is reconfigurable and consists of DSP and FPGA devices along with high speed analog to digital and digital to analog converters. The testbed in the Rice CMC-Lab also allows end to end performance characterization via an attached 2.4 GHz radio subsystem using either antennas for a true wireless link or a wireless channel emulator for controlled experiments in multipath fading. Experiments on the testbed can be performed to allow for algorithm and partitioning verification, identification of unforeseen bottlenecks, and over the air bit and frame error rate (BER/FER) determination. Figure 6 show the programmable transceiver hardware which is connected to a general purpose host computer for control and interfacing. The Rice Wireless Research Platform is being expanded to support multiple antenna system (MIMO) algorithm prototyping [42]–[44] and wireless mobility studies.

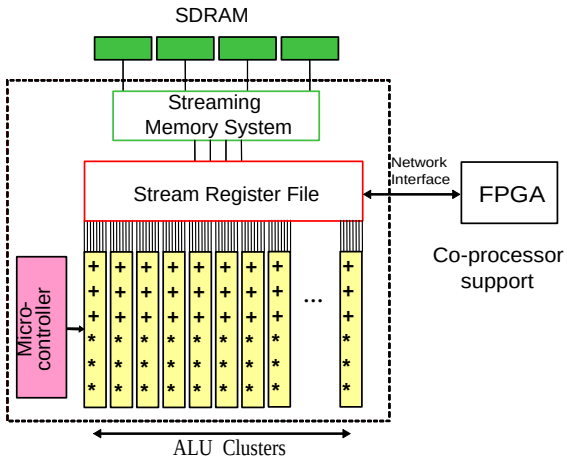

Fig. 5. Multi-cluster ASIP architecture and FPGA Co-processor [19], [41].

Fig. 6. Rice Reconfigurable Wireless Research Platform.

The testbed platform currently utilizes both the National Instruments LabVIEW and Mathworks Simulink environments for coordination and execution scheduling. The embedded hardware/software partitioning strategies are implemented at the design tool and algorithm level. Wireless algorithm design and mapping to parallel architecture prototypes on the FPGA boards is done via the LabVIEW FPGA and Xilinx System Generator design tools. The testbed uses the Nallatech Xilinx XtremeDSP FPGA System. This configuration allows for rapid prototyping with the National Instruments 2.4 GHz radio units for end-to-end laboratory experiments.

IV. Summary and Conclusions

In this paper, we have presented the design challenges for VLSI architectures for beyond 3G MIMO systems. Algorithm design and mapping to configurable application specific processors can allow for support of multiple standards which is particularly valuable in the design prototype phase. MIMO testbeds which combine programmable hardware with RF units are an active area of research at several universities worldwide.

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