Design of the CMS-CASTOR subdetector readout system by reusing existing designs

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Abstract

CASTOR is a cylindrical calorimeter with a length of 1.5m and a diameter of 60cm located at 14.3 meters from the CMS interaction point and covering the range in pseudo-rapidity corresponding to 5.1 < | eta | < 6.6. The CASTOR project was approved in the middle of 2007. Given the limited resources and time, developing a readout system from scratch was excluded. Here the final implementations of the readout chain, the considerations for the different choices as well as the performance of the installed equipment are discussed.

I. INTRODUCTION

CASTOR is an electromagnetic and hadronic calorimeter, based on a sandwich of tungsten and quartz plates, with a 14(16)-fold longitudinal (azimuthall) segmentation, positioned symmetrically around the beam pipe. In the longitudinal direction there are 2 segments for the electromagnetic and 12 segments for the hadronic part. In total there are 16 x 14 = 224 segments. The CASTOR detector was only installed at one side of the CMS experiment but for the readout design one had to take into account the possibility of a detector on both sides. PMT's are used as sensor elements that detect the Cherenkov light from one segment.

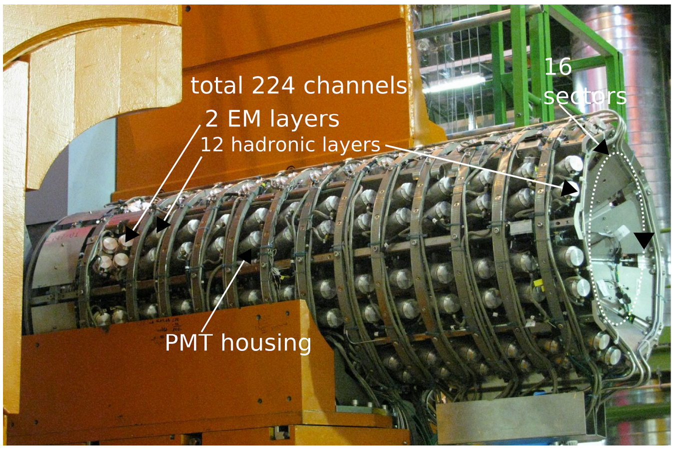

Figure 1: CASTOR detector installed on its support

The total integrated dose at the level of the PMT's is expected to be 20 kGy. The stray magnetic field measured near the PMT's is 0.16 T. The detector will be used to study several physics aspects, ranging from QCD to exotic physics. In proton-proton collisions, it will be used to flag the absence of energy or measure forward jets to allow the study diffractive scattering and the low-x proton structure. In heavy ion collisions it will be used e.g. for the search of "Centauro-events" and "strangelets". All these physics studies require specific trigger conditions and different dynamic ranges. For the absence of the rapidity gap a low energy detection is required while for jets, in case used as signature for discovery channels, the energy can be as high as 7 TeV.

Due to the limited time and manpower available for realisation it was clear from the start that one had to use existing designs for the readout system. To ensure active support and compatibility with the CMS readout system, it was decided to look only for designs that were used within CMS. Below we describe the systems that were evaluated in more detail.

II. THE SENSOR SYSTEM

The choice of the PMT is limited by available space, radiation environment, magnetic field, expected signal and cost. Although enclosed by the partially iron radiation shielding, the PMT has still to cope with an magnetic field of about 0.16 T as measured in 2008. This was higher than anticipated by magnetic field simulation as the model used in the magnetic field simulation was not detailed enough for this region. With such a high field a mesh PMT was the only option and the Hamamatsu type-R5505 PMT's from the SPACAL calorimeter of the H1 experiment [1] at DESY fit inside the given space and could be recovered for our calorimeter. The R5505 has a limit for the average anode current of 10uA, resulting in a limit of the gain that can be applied. Because of a possible reduced transparency of the PMT window due to irradiation, a maximal gain obtained with a cathode voltage of 2200V could be necessary. The PMT base offered by Hamamatsu didn't fit the mechanical and radiation tolerance constraints so a custom made PMT base using a two PCB implementation had to be designed. (see Figure 2).

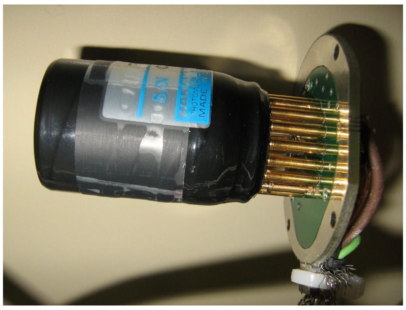

Figure 2: the R5505 PMT mounted on the CASTOR base

A simple bleeder and filter network is implemented with surface mounted components. An active network was not considered due to the high radiation environment. To guarantee a stable gain as a function of the activity in the detector the last dynode of the PMT has its own power supply line. The voltage step from cathode to first dynode was increased to increase the collection efficiency of the photo-electrons in a magnetic field environment.

To save space the cables were soldered to the PMT base. The cable and the base with the PMT mounted were tested before it was mounted on CASTOR. The HV power supply system from CAEN, the SY1527LC equipped with ten A1535N boards, is located in the service cavern and is connected via six ~100m long cables to the PMT bases in the experimental hall.

III. THE FRONT END CHOICES

Two front end architectures were considered: the front end components used for the CMS electromagnetic calorimeter (ECAL) and the components for the hadronic calorimeter (HCAL).

A. Evaluation of the HCAL front end architecture.

The forward hadronic calorimeter of CMS, called HF, uses also PMT's to detect Cherenkov light from relativistic particles. The occupancy of this detector is however lower than for the CASTOR detector. The front end architecture is built around three chips.

The QIE chip[2], integrates the charge from the PMT over one bunch crossing time interval. This is an important property for a detector with a high occupancy. The analogue to digital conversion is also done by the QIE chip.

The CCA [3] is a control chip that decodes the command bus and takes care of combining the data from three QIE chips. These data packets are serialized by the GOL chip [4].

The GOL [4] drives a 850 nm laser that transports the data over 80m fibre to the data processing cards.

Due to the radiation levels inside the detector volume it is not possible to place these readout chips near the PMT's. Coax cables have to be used for the transport of the PMT signal to the front end chips located in a rack about 6 m from the detector. The necessary cable length of 12m is twice as long compared to HF and causes an increase of the electronic noise. Due to the long cable length a good matching between the 50 **Ω** cable impedance and the QIE input impedance is important. During the initial testing of the QIE chips the chips with an impedance near 50 **Ω** were selected and were used for the HF readout cards or set apart as spares. Therefore although enough QIE chips were available it was not clear if there were enough left with the correct input impedance. The digital output of the QIE chip is 10000 counts (non- linear coding) which is not sufficient to cover the full dynamic range for the maximal expected energy and for the detection of halo muons that have to be used for calibration purposes.

B. Evaluation of the ECAL Front-end components

The ECAL front end architecture [5] is based on four chips. A multi gain pre-amplifier (MGPA), a four channel ADC [6], a data processing chip called FINEX [7] and a serializer chip GOL. The multi gain pre-amplifier together with the ADC provides a greater dynamic range in respect to the QIE and in addition the chips are able to withstand the radiation environment. Less space would be needed to transfer the signals in optical fibres compared with the QIE solution. But to operate the chips a well controlled cooling system was required and this could not be realized in time. Also it was considered to place the chips outside the CASTOR volume implying a 12m long cable between the PMT and the chip. In that case no changes of the existing design would be needed. The MGPA chip was however not designed for an application with long lines between the sensor and the chip. The shaper follows closely the function $f(t) = e^{-t/\tau}$ where τ is typically 40ns. The input signal can be reconstructed by a FIR filter. To study the signal reconstruction the pulse response of the MGPA was digitized with a 1 GHz digital oscilloscope just before the entrance of the ADC. This signal was used in a C++ program to study the effectiveness of a FIR filter. As input signal the simulation result from PYTHIA was used. For the ECAL a method is followed to find the best precision of the energy [8] in a certain bunch crossing. For CASTOR the aim was to minimize the residuals from signals from previous bunch crossings as the occupancy is factors higher in respect to the ECAL situation..

It was not possible to find weights for a FIR filter to lower the RMS value of the residual below 5 GeV taking into account the electronic noise, time jitter and the not ideal pulse response. An other risk was interference of external signals as the input of the MGPA chip is single ended.

C. Implementation of the front end electronics

As the studies on the ECAL front end showed that measurements for low energy would be worse the decision was made to continue with the QIE based architecture. Also the updated LHC schedule gave more time for selecting additional QIE chips. The shortcoming of the limited dynamic range of the QIE has to be dealt with by a trade off between the physics requirements has to be made to deal with the limited dynamic rang. For the calibration with muons special runs with higher gain settings for the PMT will be done. Finally 55 QIE cards were reproduced without changing the layout of the HF design. A new laser had to be selected and a solution was found for the different package of the laser. 39 cards are installed to readout the CASTOR detector and are placed inside three "HF crates". Six backplanes for the "HF-crate" had to be reproduced as well ten crate control modules (CCM). The extra components were needed to extent the number of spares and will be used for test setup. Especially for the backplane and CCM cards the production setup costs were the main cost factor due to the low quantities. The front end crates are powered by one MARATON system from Wiener. Due to space limitation in the rack it was not possible to have the same LV system as used by HCAL. The front end readout system was installed in autumn 2008.

D. LED pulser

The LED pulser is built as a module that fits in the "HF crate". The LED pulser is able to provide a light pulse of less then 20ns in a specific bunch crossing. Amplitude and bunch crossing can be selected by software via the CCM. The light from a blue LED is guided via a system of quartz fibres to the window of the PMT's. This signal is used for the commissioning and as reference signal during the calibration procedure.

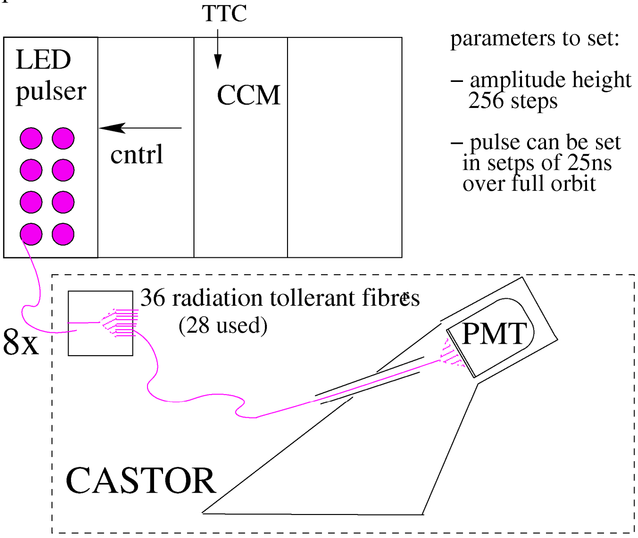

Figure 3: The LED monitoring system

IV. Evaluation of the Readout and Trigger Atchitecture.

The readout and trigger architecture provides the interface between the front end and the CMS-DAQ [9] interface called FRL [10]. Also it sends trigger information to the global trigger of CMS. For the DAQ interface the data from the different front ends has to be packed together, formatted and is sent via a data link (SLINK [11]) to the FRL.

As the readout units will have a high occupancy zero suppression or other data processing will not be done. The trigger logic has to convert the digitized code to an energy per readout unit. The energy per sector has to be summed up and has to be compared to a programmable threshold. A trigger logic card has to calculate the total energy inside CASTOR and will make a final trigger decision. Two different architectures were considered and described below.

A. Evaluation of the HCAL readout and trigger architecture

The HCAL readout and trigger architecture [12] consist of three different 9U-VME cards called the HTR, DCC[13] and TTCf (see Figure 4). There were not enough boards available to readout two CASTOR detectors. Using this architecture implied the production of these 9U-VME boards in small quantities. In addition the DCC board consist of different types of mezzanine cards. Al the reproduction work was considered as too expensive and time consuming. In addition some of the components were obsolete so small redesigns would be necessary. Also no existing hardware could be identified that could be used as the trigger logic card. This has led to decision to search for an alternative architecture to implement the readout and trigger functionality. But because of the reasons mentioned below it was recently decided to use this architecture. In the mean time the HCAL community decided to redesign and produce new DCC boards from which some are available for CASTOR. In addition it became clear that there will be no second CASTOR in the near future so less HTR cards are needed. An interface card called the oSLB [14], developed by the HCAL community, can be used as interface between the HTR cards and the trigger logic card. This possible solution for the trigger logic implementation has to be investigated in more detail.

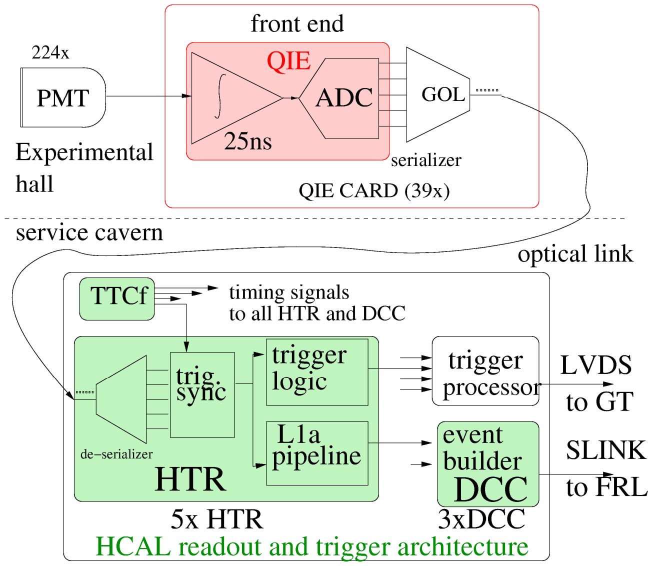

Figure 4: The HCAL readout architecture components

B. Evaluation of the CMS Preshower / TOTEM architecture.

The CMS Preshower collaboration and the TOTEM collaboration developed a common hardware platform for their readout and trigger architecture [15] [16] although they have different detectors with different front end architectures. The hardware is a 9U-VME host board with slots for mezzanines. The mezzanine that is used to de-serialize the optical signals from the front ends, called OptoRx [17] is used in both projects. CASTOR could join the final production of the VME host boards so minimizing the production costs and the time needed to follow up the production.

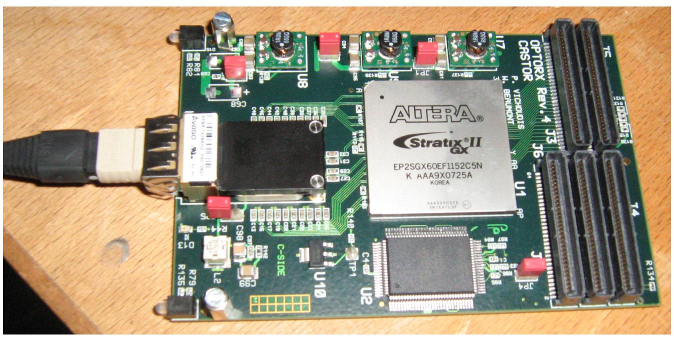

Figure 5: the CASTOR OptoRx

The OptoRx mezzanine could not be used as it was because the optical receiver (NGK POR10M12SFP) is qualified for data rates only up to 1.25Gbps with a wave length of 1310 nm while the GOL on the QIE card sends the data at 1600Mb/s and drives a 850 nm laser. In the CASTOR version of the OptoRx the NGK POR10M12SFP was replaced by a commercially available 12 channel optical receiver (AVAGO AFBR-742BZ) in a SNAP 12 package.

To exchange the receiver only a few changes were needed in the design. In addition the designer had already foreseen a cut-out in the VME host board that allows the use of OptoRx mezzanine equipped with SNAP12 optical receiver because the SNAP 12 package even without heat sink is 12 mm in height while the stacking height of the mezzanine is only 10mm.

The FPGA on the OptoRx performs operations that are comparable with the once implemented in the HTR card. The FPGA's of the VME host board will take care about the final formatting and the interface to the data link functions performed by the DCC in case of the HCAL architecture.

The trigger logic per sector will also be implemented in the OptoRx FPGA. The trigger information will be sent via the third mezzanine slot to the trigger logic card. The plan was to "transform" the OptoRx design to a transmitter. The OptoRx + VME host board combination can also be used as a trigger logic board as shown in Figure 6. Despite the flexibility of the system it was not possible to find a combination to make efficient use of all the optical inputs and to fulfil the trigger requirements. So it was decided to leave out the information of the two last layers for the trigger decisions.

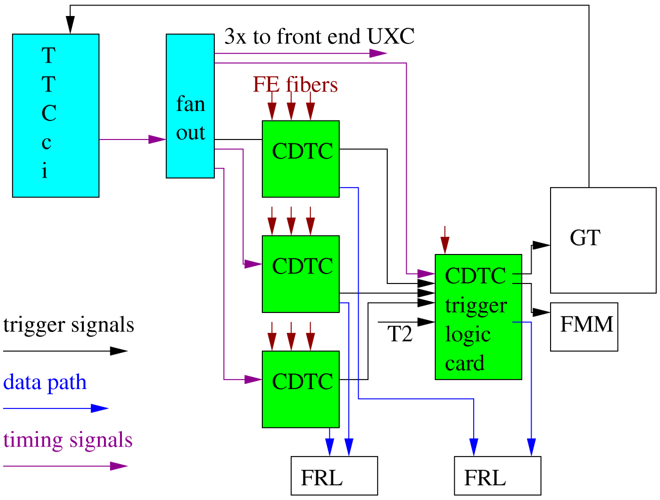

Figure 6: inter connections of the VME host boards equipped with OptoRx (CDTC)

Parts of the firmware could be copied from the various projects. The VME interface code was copied from the TOTEM project as well the code for memory control and local bus on the VME host board with slight modifications. Concerning the OptoRx the de-serializer code from the Preshower firmware was used as a starting point while for the data synchronization the HCAL firmware was used. Initially it was assumed the firmware could be ready in one year. But finally the firmware for the project is not yet finished although most of the functionality is implemented. The fact that the project is not finished in time is due to an underestimation of the complexity of the system aspects. More detailed system evaluation tests should have been done during the implementation phase. As the start of the LHC is a strict deadline, recently it was decided to use the HCAL readout and trigger architecture as final system. There were no technical difficulties that indicate that the VME host board with OptoRx could not fulfil the requirements. That the combination of OptoRx and VME host board could be used for our purpose is because of the modular approach of the architecture and that this architecture was designed to be used for different applications from the beginning.

V. Commissioning

In 2007 and 2008 a proto-type sector was tested in the H2 SPS beam line at CERN. From these tests the resolution of the detector was obtained. In figure 7 the result of the muon response is compared with the signal from the pedestal. The pedestal in the figure is taken as an average over 4 entries per event so the effective RMS value is 2.2 / √4 = 1.1 counts slightly higher then the expected value of 0.8 count. In 2009 the final half CASTOR structure equipped with 2 sectors was placed in the beam line to re-measure the calibration constants.

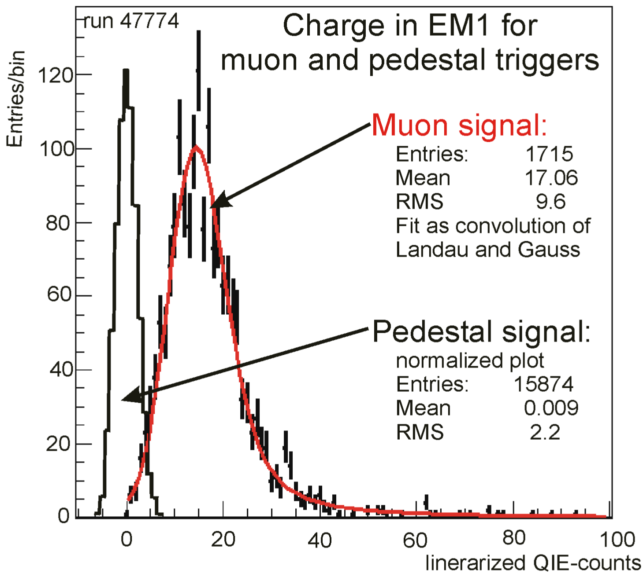

Figure 7: muon signal and pedestal obtained from the test beam 2008

After the detector was fully assembled the LED system was used to check the working of each individual PMT. It turned out that some fibres were not correctly installed. Some PMT's had short circuits between the last two dynodes. The PMT-cable test didn't cover the detection of this fault. Not all the PMT's suffering from this problem could be replaced due to lack of spare PMT's.

CASTOR was positioned on its support in CMS at the end of June 2009. The average noise level of a readout unit is one QIE count with no indication of a specific interference signal. There are 16 PMT's that don't response to the LED signal, of these 8 PMT's response on the environment light.

Since beginning October 2009 CASTOR is sending data to the CMS DAQ. The trigger logic has still to be implemented.

VI. CONCLUSION

The initial intention for the implementation of the readout architecture was to copy everything from the HCAL architecture. However the cost to reproduce all of the necessary components changed this intention. After some additional study the HCAL front end was nevertheless selected. For the readout and trigger architecture an alternative was proposed and worked out in detail and long time considered as the base line implementation. The firmware for the alternative architecture could not be finished in time so finally the complete HCAL architecture has been implemented as conditions have changed over time. CASTOR is now installed inside CMS and is ready to take data.

VII. ACKNOWLEDGEMENT

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