GENERAL PURPOSE DIGITAL SIGNAL PROCESSING VME-MODULE FOR 1-TURN DELAY FEEDBACK SYSTEMS OF THE CERN ACCELERATOR CHAIN

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Abstract

In the framework of the LHC project the concept has been developed of a global digital signal processing unit (DSPU) that implements in numerical form the architecture of low-level RF systems [1]. The approach, using an FPGA as core for the low-level system, is very flexible and allows the upgrade of the signal processing by modification of the original firmware [2]. The achieved performances of the LHC 1-Turn delay Feedback are compared with project requirements. The PS Transverse Damper DSPU, with automatic loop delay compensation adapting to the beam's time of flight and Hilbert Filter for single pick-up betatron phase adjustment, is presented. A modified DSPU with digital inputs for the LHC Transverse Damper is also presented.

INTRODUCTION

Circular accelerators encounter beam instabilities caused by machine impedances that limit their performance. There are two potential solutions: reducing the offending impedance in the ring and active damping by means of Feedback Systems acting in all three planes, vertical, horizontal and longitudinal. In the RF Feedback scheme applied to an RF cavity it can be shown [3, 4] that the apparent cavity impedance at resonance is proportional to the loop delay T and that the achievable bandwidth depends on the loop delay only. These are strong motivations for keeping the **loop delay short**. Conversely, in the long delay feedback systems, in order to compensate the exact portion of the beam that created the instability, the digital signal processor time-complements the correction to the beam **1-turn delay**. The closed loop response for a long delay cavity feedback system, Fig. 1, is represented by Eq. (1).

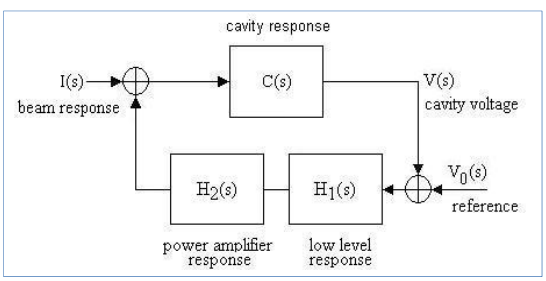

Fig. 1: Closed loop response for a cavity feedback system.

$$V(s) = \frac{C(s) \cdot I(s)}{1 - [H_1 \cdot H_2 \cdot C](s)} + \frac{[H_1 \cdot H_2 \cdot C](s) \cdot V_0(s)}{1 - [H_1 \cdot H_2 \cdot C](s)} \quad (1)$$

where:

$V(s)$ Actual cavity voltage; $V_0(s)$ Voltage reference;

$I(s)$ Beam current

$H_1(s)$ Low Level response; $H_2(s)$ Power Amp. response

If the objective is the design of a high-performance general purpose DSPU, the desirability of uniformity for certain circuit characteristics is clear. For purposes of this work, high-performance implies first, the possibility to design and implement all the functions fulfilling the low level response $H_1(s)$ for long-delay digital signal processing schemes suited for cavity feedback, cavity feedforward and transverse & longitudinal feedback loops employed in the LHC, SPS and PS accelerators complex [5], secondly, in view of stored beams, the minimization of the quantization error to reduce the injected noise and increase the beam lifetime and thirdly the ability to communicate at the highest data rate possible for a given channel bandwith.

THE LHC 1-TURN DELAY FEEDBACK

Each LHC 400.8 MHz cavity is equipped with an RF Feedback [6] that reduces the cavity loaded Q from 20000-180000 to 700. The 1-T Feedback, Fig. 2, is a Cartesian Feedback that implements in an FPGA two identical filter chains acting on the baseband I and Q error signals sampled at 40.08 MHz by 14 bit ADCs [7]. Comb filters further increase the open-loop gain, by a factor of 20 dB, at the revolution frequency side-bands thereby reducing the transient beam loading and the resulting longitudinal instability threshold [3]. The phase response seen by the 1-T Feedback is linear only in a ± 500 kHz band. The bandwidth is limited by a FIR LPF with a pass band up to 870 kHz and a stop band starting at 1.3 MHz. The narrow transition band is realized by reducing the original clock rate (40.08 MHz) to 10.02 MHz using a CIC decimator [8]. The sampling rate after the filter is increased using a CIC interpolator to create a smooth output. The 1-T Feedback bandwidth can be extended with a FIR phase equalizer. An I/Q phase rotator is also implemented for fine adjustment of the 400.8 MHz phase. The 1-T delay is implemented in the FPGA RAMs with independent read-write clocks. The fine delay is implemented by shifting the read clock with respect to the write clock. The FPGA includes a baseband network analyzer to measure the frequency/step response using the logging of re-sampled input and output signals in diagnostic memories. A serial function generator and a serial control link for parameter control during the cycle are also provided. Loop gain adjustment is provided by programmable attenuators, preceding the input ADCs, and by controlling the current reference of the output 14 bit DACs. The full scale spurious-free response approaches a level of 80 dB. A control feature is provided for selecting and mapping internal signals to the output ports permitting optimization of the transfer functions.

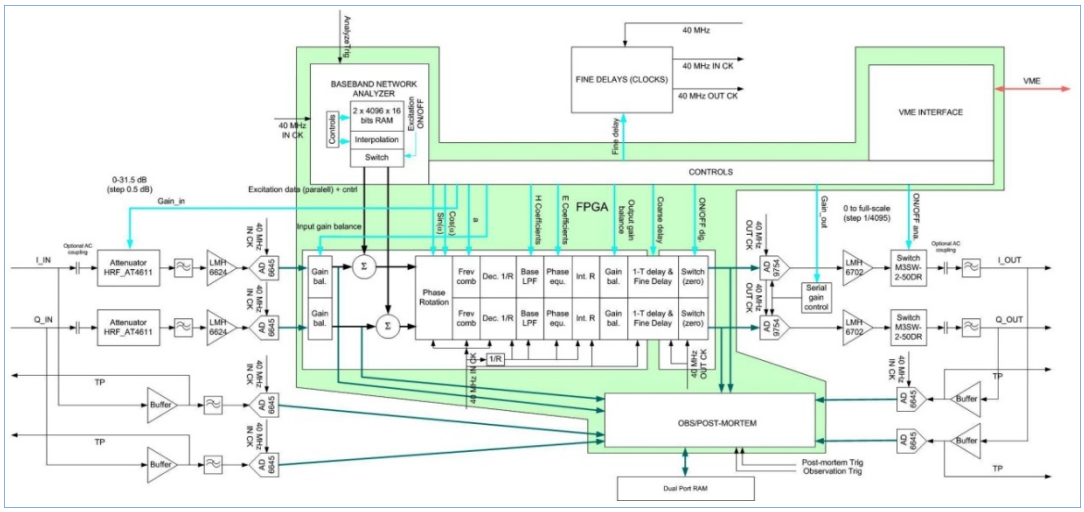

Fig. 2: The LHC 1-Turn Feedback implemented in the module EDA-01150. The shaded area denotes the FPGA.

LHC Cavity Impedance Reduction

The results on LHC cavity impedance reduction with the RF Feedback and 1-T delay Feedback are presented.

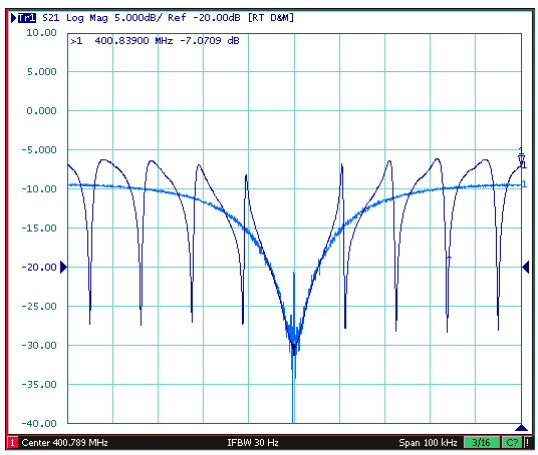

Fig. 3: Effective cavity impedance, 100 kHz span around the cavity centre frequency of 400.789 MHz.

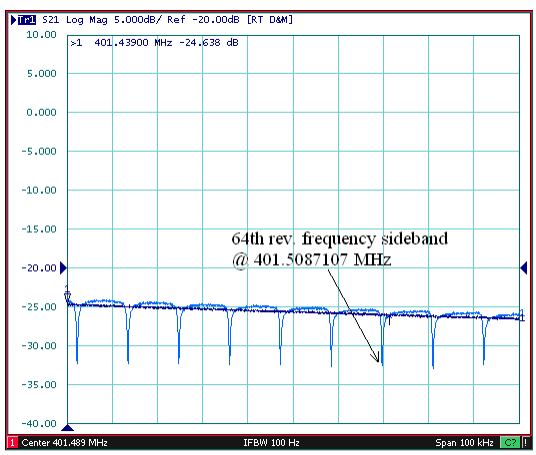

Fig. 4: Effective cavity impedance, 100 kHz span around the frequency of 401.489 MHz.

Fig. 3 and Fig. 4 show the superconducting cavity impedance as seen from the beam, closed loop. The smooth traces are the result with RF Feedback only. The reduced impedance at the centre frequency in Fig. 3 is caused by the increased gain obtained with the digital part of the RF Feedback [6]. The second traces show the reduction added by the 1-T Feedback at the revolution frequencies lines: from 20 dB close to the centre frequency, Fig. 3, down to 8 dB at ± 750 kHz. The vertical scale calibration is -20 dB ≃ 10 kΩ; 20 dB/decade in Ω and the cavity loaded Q is 60000.

DSPU FOR THE PS TRANSVERSE FEEDBACK, BASED ON EDA-01150

Compared to the SPS and LHC Transverse Feedback systems, the PS requires a dynamic delay-compensation circuit to adapt the feedback loop delay τ_{signal} to the particle flight-time τ_{beam} that changes much during acceleration [9]. To maintain the tracking between beam and correction, the following identity, Eq. (2), shall be satisfied during acceleration:

$$\tau_{beam} = \tau_{signal} = T_{FIX} + T_{CLK} + T_{VAR} + T_{FINE} \quad (2)$$

where:

T_{FIX} fixed delay; T_{CLK} fixed clock latencies; T_{VAR} variable number of clocks; T_{FINE} fine delay. The automatic delay compensation, Fig. 5, computes the delay in terms of clock periods and of fractional fine delay, Fig. 6, from a measurement of the revolution frequency. The cycle computation time is 32 µs for a resolution of ± 0.5 ns. To avoid the saturation of the Power Amplifier the closed orbit is rejected by a notch filter whose transfer function is $(1 - z^{-N})$. A Hilbert filter allows the phase adjustment with a single pick-up and/or a dual pick-up mixing scheme. The Hilbert filters' transfer function is given by Eq. (3), where $h(n)$ are the Hilbert transform impulse response coefficients.

$$H(z) = h(0) \cdot z^{-3N} + h(1) \cdot (z^{-2N} - z^{-4N}) + h(3) \cdot (1 - z^{-6N}) \quad (3)$$

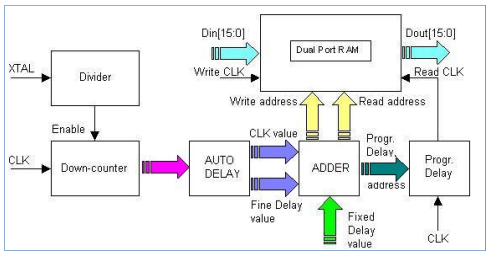

Fig. 5: Automatic Delay Compensation. Block diagram.

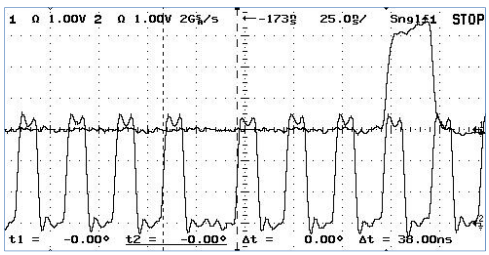

Fig. 6: Read data of RAM are synchronized to the read clock (bottom) changing just before the end cycle (top).

DIGITAL SIGNAL PROCESSING FOR THE LHC TRANSVERSE FEEDBACK

In the LHC, Transverse Feedbacks acting both in the horizontal and vertical planes are needed for transverse injection oscillations damping, for curing transverse coupled bunch instabilities and also for excitation of transverse oscillations for beam measurements [10]. The signal processing for each damping loop is implemented in the module originally designed for the 1-T Feedback on the LHC cavities, figure 7. Its firmware has been adapted to the transverse damper processing and analog inputs have been replaced by digital ones designed for low quantization noise [11], figure 8. The serial data streams

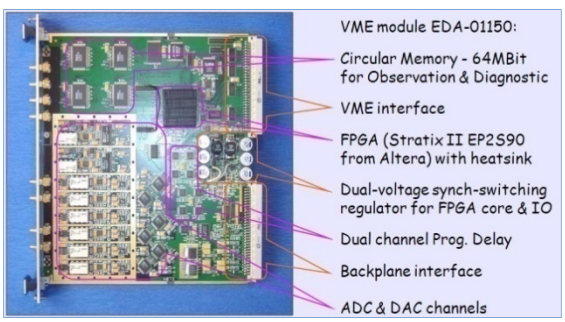

Fig. 7: LHC 1-T Feedback, VME module EDA-01150.

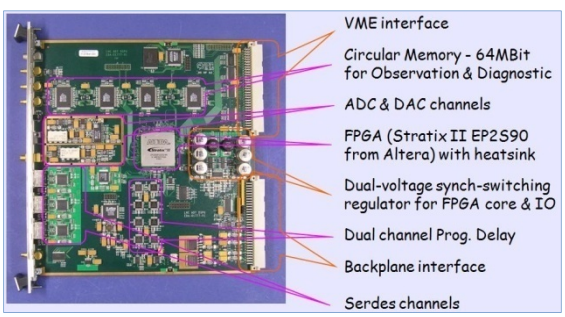

Fig. 8: LHC ADT DSPU, VME module EDA-01777.

from two pick-ups, bunch-by-bunch position at 40.08 MHz, are sent to the DSPU at a rate of 1 Gbit/s. Serdes channels convert the serial data into parallel 16 bit words. The first processing blocks in the FPGA resynchronize the data with the bunch synchronous 40.08 MHz clock. To avoid Power Amplifier saturation, the closed orbit is rejected by notch filters. A Hilbert FIR filter is provided for each pick-up allowing the phase adjustment with a single pick-up and/or a dual pick-up scheme, see Eq. (4). The DSPU also include CIC interpolators, a FIR filter and a Phase Equalizer for compensating the non linear response of the Power Amplifier. The transverse kick for each bunch is calculated on the transverse bunch positions measured on the previous turn and time-complemented to the LHC 1-T delay by programmable coarse and fine delay by using two clock domains with a resolution of 10 ps. Two fine delay chains are provided, the first for the main 80.16 MHz clock and the second for the revolution frequency of 11 kHz. The FPGA contains the processing blocks described above and the VME interface for setting the various parameters and for reading logging memories.

CONCLUSION

Global digital synthesis implements in numerical form the architecture of low level RF systems. So far the LHC 1-T Feedback has been commissioned, the LHC ADT DSPU and the PS DSPU are installed and ready for beam.

ACKNOWLEDGMENTS

P. Baudrenghien, O. Brunner, W. Höfle, J. Molendijk and the RF teams who helped make the system tests possible.

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