ALIBAVA: A portable readout system for silicon microstrip sensors

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Abstract

A portable readout system for micro-strip silicon sensors has been developed. The system uses an analogue pipelined readout chip, which was developed for the LHC experiments. The system will be used to characterise the properties of both non-irradiated and irradiated micro-strip sensors. Heavily irradiated sensors will be operated at the Super LHC (SLHC).

The system hardware has two main parts: a daughter board and a mother board. The daughter board contains two readout chips, analogue data buffering, power supply regulation and chip-to-sensor fan-in structures. The mother board is intended to process the analogue data that comes from the readout chips and from external trigger signals, to control the whole system and to communicate with a PC via USB. There is provision for an external trigger input (e.g. scintillator trigger) and a synchronised trigger output for pulsing an external excitation source (e.g. laser system). A prototype of the system will be presented.

I. INTRODUCTION

The main properties of highly irradiated micro-strip silicon sensors has been studied since this type of detectors are currently used at the LHC experiments. It would be important to predict the behaviour of this type of sensors under certain circumstances, as the irradiation dose, since a higher luminosity is intended to be achieved at SLHC experiments, Among these properties, the collected charge when a charged particle crosses the detector is important for knowing the performance of the detector. Currently, it is not easy to carry out valuable measurements of the collected charge in micro-strip silicon sensors because a custom and expensive laboratory set up is needed. Other reason is that the measurements obtained are often not comparable since different equipments are used depending on the laboratory facility,. Finally, this type of sensors may have hundreds of channels for reading.

It would be also interesting to test this kind of detectors with an electronic system as similar as possible to those used at the LHC experiments. Therefore, a front-end readout chip used at the LHC experiments should be used. An analogue measurement of the pulse shape would be preferred because it would be more reliable than with a binary measurement for charge collection research.

In order to generate the charged particles in a laboratory, two main setups are usually used [1]. A radioactive source setup, where the charged particles are generated randomly, and a laser setup, where a laser light is generated exciting a laser source with a pulsed signal [2].

Taking in consideration all this, an electronic system which can acquire an analogue measurement using a front end readout chip with a laser setup and a radioactive source setup has been developed. The aim is reconstructing the analogue pulse shape at the readout chip front end with the highest fidelity.

For fulfilling these requirements the system has been designed with a particular characteristics. The system is compact and portable. It has its own supply system and it contains two front-end readout chips to acquire the detector signals. The system is connected to a PC via USB, which will store and will process the data acquired. This system is controlled from a PC software application in communication with a FPGA which will interpret and will execute the orders. Finally, the system will be used with two different laboratory setups so it will have an external trigger input, from one or two photomultipliers (radioactive source), and an external trigger output for pulsing an external excitation source (laser system).

II. SYSTEM ARCHITECTURE

The system has been divided into two main parts, a hardware part and a software part. The hardware part will acquire the micro-strip silicon sensor signals, from an external trigger input or a synchronised external trigger output, and will process the data in order to be stored in a PC or laptop.

This hardware part is a dual board based system. A mother board which is intended to process the analogue data that comes from the readout chips, to process the trigger input signal in case of radioactive source setup or to generate a trigger signal if a laser setup is used, to control the whole system and to communicate with a PC via USB. The daughter board is a small board which contains two Beetle readout chips [3] and has fan-ins and detector support to interface the sensors. The main reason for dividing the hardware into two boards is to prevent the rest of the hardware from the aggressive environment (radiation or very low temperatures) that will suffer the detectors. Both boards are communicated by 'twist and flat' ribbon cable for the analogue data signals coming from the Beetle chips, slow and fast control digital signals to the Beetle chips, a temperature signal as well as the supply level for the Beetle chips. The high voltage detector power supply will be provided directly to the daughter board.

Regarding the software part of the system, its function is mainly controlling the whole system and processing the data acquired from the sensors in order to store it in an adequate format file. This format file will be compatible with software

used for further data analysis, as the ROOT framework. The software is a Linux based program. With this software the system will be able to be configured and calibrated. Acquisitions with a laser setup or a radioactive source setup will be able to be carried out as well.

III. DAUGHTER BOARD

The daughter board is a small board with the minimum components needed for accommodating two Beetle chips, a temperature sensor and the sensors support (fan-ins and power supply). The block diagram of the daughter board is shown in figure 1. There are two Beetle readout chips used to read the detector channel signals. There is a thermistor as close as possible to the detectors in order to have a temperature readout on each acquisition as well. A DC supply level (5V) is sent from the mother board. This supply level is regulated by two low drop out (LDO) linear regulators for obtaining the DC supply levels required by the readout chips and the buffer stage (2.5V). The detector high voltage power supply is supplied directly to the daughter board. There is a decoupling stage for this supply prior to the detector.

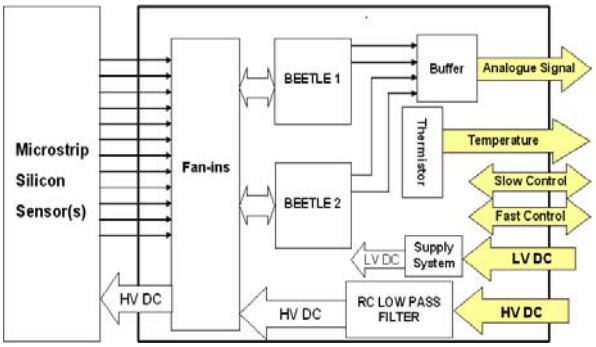

Figure 1: Daughter board block diagram.

The main characteristics of the Beetle readout chip can be found on [3]. Currently, the Beetle chip analogue output on one port is used. In this case the analogue front-end pulse signal is sampled into the pipeline with the frequency of the Beetle chip clock which has been fixed to 40 MHz (period of 25 ns). The peak voltage of the front-end pulse signal is proportional to the collected charge at the detector channel The peak time this signal is about 25 ns (depending on the load capacitance among other parameters) and the remainder of the peak voltage after 25 ns is below 30 %. Therefore, a 65-70 ns pulse length is considered in order to reconstruct the pulse. Once the pulse has been sampled into the analogue pipeline, for reading out a particular position of this pipeline is needed to trigger a signal (TRIGGER) related in time with the readout chip clock (CLK). The analogue pipeline latency has been fixed to 128, so the TRIGGER signal will have to be active 128 CLK cycles (3.2 µs) after a particular front-end signal point of interest has been sampled.

Once the TRIGGER has been activated (at least a 25 ns pulse), the readout of the analogue output on one port data will start synchronous to CLK. A DATAVALID signal will be activated 25 ns before the readout starts and it will be deactivated 50 ns before the readout ends. This analogue output signal is a multiplexed signal composed of a 16 bits header and 128 data channels, whose voltage amplitude will correspond to the particular front-end sample. The width of each header bit or each channel is 25 ns, so the length of each readout frame will be 3.6 µs. The header bits will not be used on this system. The readout chip will be operated in a single readout scheme, that is, the TRIGGER signal will not be activated while a readout is carried out.

Regarding the fast control of the Beetle readout chip, three LVDS fast control signals (CLK, TRIGGER and DATAVALID) has been already presented. There are two more signals that belongs to the LVDS fast control, RESET and TESTPULSE. The RESET signal is used for resetting the Beetle. The chip's slow control interface is a standard mode I2C slave [4]. The bias settings and various other parameters like the trigger latency or the injected test pulse amplitude can be controlled by this control.

The analogue output buffer is a current buffer so the analogue output signals are current differential signals. The loop for each signal will be closed with a 100 Ω resistor on the daughter board and the voltage over that resistor will be the analogue output voltage. These outputs will be buffered at the daughter board by means of a differential line driver (AD8130, Analog Devices). No line equalization will be required at the mother board if the cable is no longer than 10 m [5]. Finally, the analogue output dynamic range will be in the linear area as could be seen on [6]. This will correspond to ± 66000 electrons or ± 0.5 V approximately.

As it has been mentioned before, there are two Beetle chips on the daughter board and a parallel configuration has been considered. In this case, there are two different analogue data lines one for each Beetle chip but the fast and slow control lines are shared by the Beetle chips.

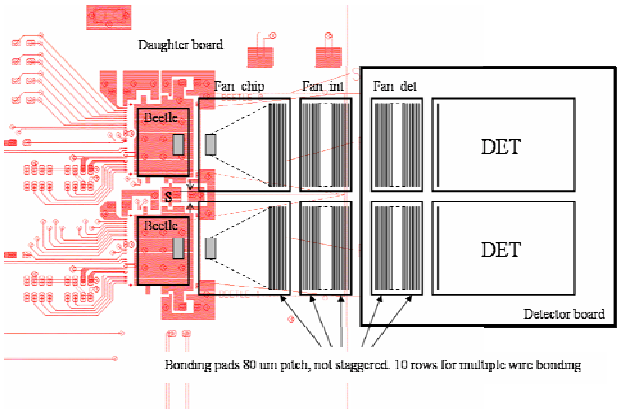

Figure 2: Fanins design diagram.

A mechanical connection system and fan-ins are provided for connecting the detectors. The fan-ins design can be seen in figure 2.

There are three fanins, a chip fanin, an intermediate fanin and a detector fanin. Each fanin has pads of 80 um pitch not staggered and 10 rows for multiple wire bonding. The purpose is to use the system with different kind of detectors so multiple wire bonding is necessary.

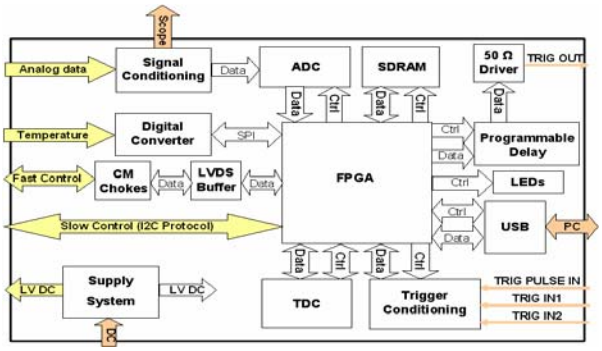

Figure 3: Mother board block diagram.

IV. MOTHER BOARD HARDWARE

A. Board Hardware

The mother board block diagram is shown in figure 3. The main component of the system is a FPGA which will implement the logic for controlling the rest of the blocks. The signal conditioning block is intended for transforming the differential voltage analogue input signal in order to drive an oscilloscope, which requires a single ended signal, and an analogue to digital converter (ADC), which requires a differential input signal shifted signal. A detailed description of this block can be found on [1]. The thermistor signal coming from the daughter board is digitized at the digital converter block.

The Beetle fast control signals have a LVDS format. The FPGA can manage directly with this format but in order to protect this component these signals have been buffered with two LVDS repeaters, one for the output signals to the daughter board (CLK, TESTPULSE, TRIGGER and RESET) and another one for the input signals from the daughter board (DATAVALID1 and DATAVALID2). Also a common mode noise suppressor choke have been provided for each signal. The I2C slow control signals (SCL and SDA) are generated directly by the FPGA. There are also a SDRAM of 256 Mbits. The function of this memory is temporally storing the digitized data in each acquisition either with the radioactive source setup or with the laser setup prior to be read by the software.

In case of the radioactive source setup, a trigger from an external source will be generated. This input trigger can come from one or two photomultipliers (TRIG IN1 or TRIG IN2) or can be positive/ negative pulse up to ±5V or fast negative NIM (TRIG PULSE IN). From this inputs, the Trigger conditioning block will generate four signals in LVPECL indicating if TRIG IN1 or TRIG IN2 is active (with a leading edge discriminator), or if a negative or a positive pulse have been received on TRIG PULSE IN (with two discriminators). The four discriminators are implemented with two dual LVPECL high speed comparators. Four voltage thresholds are needed in this block, two will be the discrimination levels for TRIG IN1 and TRIG IN2, and the other will be the discrimination levels for positive and negative pulses (TRIG PULSE IN). These voltage thresholds will be programmable by the user and a DAC of 12 bits is used for this. The TDC block will be used with radioactive source setup. This block is composed only of a TDC integrated circuit with a resolution of 600 ps and a dynamic range of 100 ns. This TDC will measure the time passed between a start signal generated every 100 ns (time window) and a trigger signal generated if TRIG IN1 and/or TRIG IN2 are active, or TRIG PULSE IN are active.

In case of the laser setup, a synchronised trigger signal (TRIG OUT) will be generated to drive a laser source so that the pulse shape will be able to be reconstructed. For this reason a programmable delay circuit (3D7428, Data Delay Devices) is used. With this circuit TRIG OUT will be able to be delayed up to 255 ns in 1 ns steps by a 8 bits parallel programming code from the FPGA. Following this block a 50 Ω driver has been incorporated for driving a pulse generator input that will pulse the laser source. For communicating with the PC or the laptop a USB block is used. This block will have a USB controller for USB to FIFO parallel (8 bits) bidirectional data transfer. Two LEDs are provided to inform about the system state to the user.

The supply system has been centralized on the mother board. A DC input level (5 V) is generated with a portable AC adapter. From this DC level the mother board digital levels (1.2 V, 2.5 V and 3.3 V) by means of two DC-DC converters and a LDO regulator. The mother board analogue levels (5 V, -5 V and 3.3 V) are generated with a DC-DC converter and a LDO regulator. The daughter board supply level (3.3 V) is generated by a DC-DC converter.

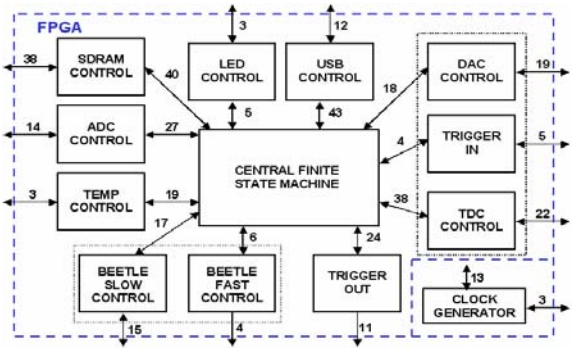

Figure 4: Block diagram of the logic that will be implemented in the FPGA

B. FPGA Hardware

The FPGA block is composed of a FPGA and all the support for programming it (Flash PROM and connector). The FPGA is clocked with a 40 MHz crystal. The main function of the FPGA is implementing all the logic in order to control the hardware and to communicate with the PC. The block diagram implemented in the FPGA can be seen in figure 4.

The CFSM (Central Finite State Machine) block controls the system hardware part by interpreting the orders that the system software part (PC software) sends by USB. Depending on the current state the CFSM will use different blocks and it will enable the communication among those blocks. This is the reason why the rest of blocks are not connected to one another but rather they are connected only to CFSM.

The slow control block controls the I2C bus in order to program the Beetle configuration registers. The fast control

block generates the LVDS output signals (CLK, RESET, TRIGGER, TESPULSE) for the Beetle fast control. The TESTPULSE is generated from an internal calibration signal. The TRIGGER signal is generated from an internal TRIG_L signal (in case of laser setup) or from an internal TRIG_R signal (in case of radioactive source setup) taking into account both the Beetle analogue pipeline latency and the particular synchronization delay.

The trigger out block is used for the laser setup and it produces an external trigger signal (TRIG OUT) and an internal trigger signal (TRIG_L) for the Beetle fast control block. This block also controls the programmable delay circuit. In this way, by programming a variable delay (up to 255 ns in 1 ns steps) the system can acquire a desired point of the Beetle front-end analogue pulse.

The trigger in block generates an external and internal trigger signal (TRIG and TRIG IN, respectively) from signals SIN1 and/or SIN2 (discriminated signals from two photomultipliers), PPOS (external positive pulse) or PNEG (external negative pulse) coming from the trigger conditioning block. The coincidence of SIN1 and SIN2, as well as which inputs will be used, can be programmed. The DAC control block controls the DAC that supplies the four voltage thresholds for the trigger conditioning comparators. The TDC block controls the TDC, which measures the time from a START leading edge signal (100 ns periodic signal) to the TRIG leading edge. It also generates a TRIG_R signal (for the Beetle fast trigger control) related in time to the TRIG signal when the last will be active.

The ADC block controls the ADCs, it reads the digitalized data frames when the corresponding DATAVALID signal will be active and it stores these frames in a internal FIFO RAM. The SDRAM control block controls the SDRAM. It also implements the read/write data and control interface with the CFSM block. The digitized data from Beetle chips (256 by 16 bits per two chips readout), the TDC data (32 bits per readout) as well as the temperature data (16 bits per readout) can be stored. The USB control has to control the USB chip and to implement the data input/output and control interface with the CFSM. The clock generator block supplies the FPGA internal clock signals and reset signals. The temperature control block reads the digital conversion of the thermistor signal from the digital converter by serial interface. The LED control block activates a red LED or a green LED depending on its input code value. This is used to show to the user the state of the system.

As can be seen in the figure 5, the CFSM and the SDRAM block have been implemented using an embedded processor. A Microblaze processor (32 bits RISC) has been used [7]. The interface used with the embedded processor are six Fast Simplex Links (FSL). These FSLs are uni-directional FIFOs. Four FSLs has been implemented for direct communication with the ADC block and USB block and two FSLs has been implemented for general communication with the rest of the blocks. For this communication an arbitrer block has been designed. This block implements the direct data communication with the USB block and ADC block. It also implements different registers for capturing the data signals coming from the rest of the blocks or for generating the signals required for controlling all the blocks.

By using this architecture in the FPGA, an embedded processor, the functionality of the system could be easily defined by the firmware. On the other hand, this functionality can be easily redesigned by means of a new firmware without changing the implementation of the FPGA hardware. The functionality of the system has been defined by programming a Finite State Machine (FSM) in the embedded processor.

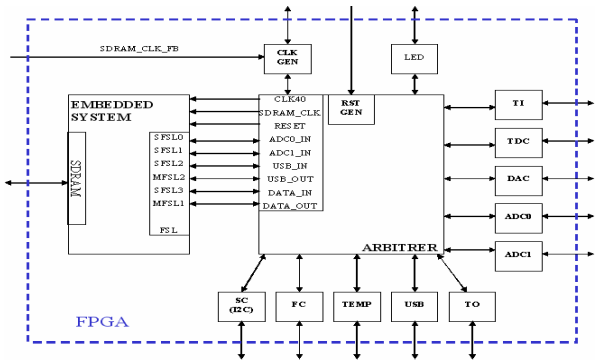

Figure 5: Block diagram of the logic that will be implemented in the FPGA

V. MOTHER BOARD FIRMWARE

The CFSM main state is a waiting state. When CFSM will be in this state, it will wait for an order coming from the PC software (by means of the USB control). Depending on the order, CFSM will choose among the rest of states as it is shown in figure 6.

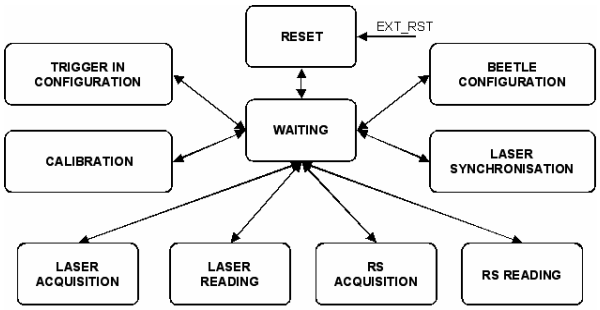

Figure 6: Central finite state machine possible states.

When the system will be powered on or with an external reset, the CFSM will go to the reset state prior to the waiting state. In this state, all the system will be initialized. After the FPGA configuration, the system also will go to this state.

In the Beetle configuration state, the configuration registers of the Beetle chips will be configured by slow control. In the calibration state, the system will be calibrated by the Beetle internal test pulse generator, that is, known amplitude readouts will be acquired in order to have calibration data. In the trigger in configuration state, the DAC voltage thresholds will be programmed as well as the trigger inputs scheme will be configured. In the laser synchronization state, the system will be synchronized in order to sample a particular point of the Beetle front-end pulse. This point will be programmable by the user (in 1ns steps).

In the laser acquisition state, a programmable number of readouts will be able to be acquired. Up to 64776 readouts will be acquired and stored in the SDRAM. For each event a Beetle chips readout (256 by 16 bits) and a temperature readout (16 bits) will be stored in the SDRAM. The TRIG OUT frequency will be 1 KHz. In the laser reading state, the last laser acquisition will be read from the SRAM and data will be sent to PC. In the RS (Radioactive Source) acquisition state, a programmable number of readouts will be able to be acquired. Up to 64776 readouts will be acquired and stored in the SDRAM. For each event a Beetle chips readout (256 by 16 bits), a TDC readout (32 bits) and a temperature readout will be stored in the SDRAM. In the RS reading state, the last RS acquisition will be read from SDRAM and data will be sent to PC.

VI. Software

Regarding the software part, the main requirements of this part are the following. First, it must control the whole system for configuration, calibration and acquisition. Second, the software has to be the interface with the system (GUI). Third, it must generate information of about the acquisition (output file).The software has been designed using two levels. A low level for communication between the software and the mother board by USB. No driver design is required at this level since the manufacturer of the USB controller provides with a ready-to-use driver (Virtual Com Port Driver). A high level for Graphic User Interface (GUI) and output file generation. The software has been designed using C++ and has been implemented with ROOT framework. Currently, the software is compatible with Linux but in the near future a Windows version is expected.

VII. Conclusion

A portable readout system for silicon micro-strip sensors has been presented. The system is divided in a software part and a hardware part. The hardware part is based in a dual board scheme, a daughter board and a mother board. This system uses two Beetle chips as a readout chips. Also, it can be used with a laser setup and a radioactive source setup.

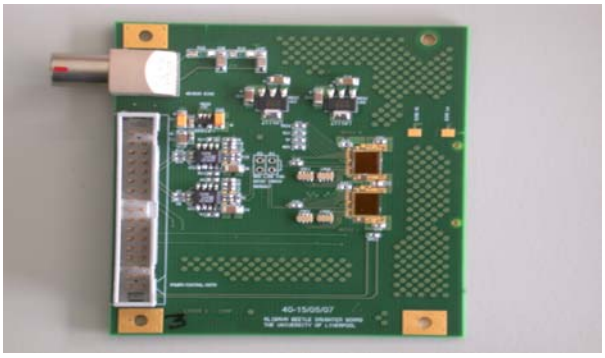

Figure 7: Daughter board fully populated.

At the present time, the system is almost finished. Regarding the daughter board, twenty PCBs have been already produced. Five of them are fully populated as it is shown in the figure 7. The fan-ins are already designed and produced.

Regarding the mother board, a first PCB prototype has been already produced and partially populated for testing the system with laser setup as it can be seen in figure 8. The FPGA firmware has been finished for the laser setup. Two blocks are being developed for the radioactive source setup (TDC Control and DAC Control). The rest of FPGA blocks have been developed. The power supply, SDRAM, USB controller, analogue processing block, FPGA hardware and FPGA firmware structure have been already tested and they work as expected.

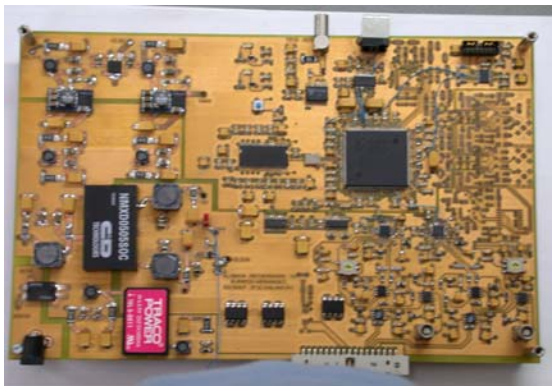

Figure 8: Daughter board fully populated.

The software is fully developed and it has been tested with an emulator. The next step is testing the daughter board, mother board and PC Software together for validating the design. The first aim is being able to use the system with the Laser Setup and then, it is expected to be able to use the system with the Radioactive Source Setup.

VIII. References

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