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The Organic Power Transistor: Roll-to-Roll Manufacture, Thermal Behavior, and Power Handling When Driving Printed Electronics**

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We present flexible organic power transistors prepared by fast (20 m min^{-1}) roll-to-roll (R2R) flexographic printing[1] of the drain (D) and source (S) electrode structures directly on polyester foil. The devices have top gate architecture and were completed by spin coating or slot-die coating of the organic semiconductor poly-3-hexylthiophene (P3HT) and the dielectric material polyvinylphenol (PVP) before the gate (G) was applied by either screen printing or evaporation of silver. We explore the footprint and the practically accessible geometry of such devices with a special view toward being able to drive large currents while handling the thermal aspects in operation together with other organic printed electronics technologies such as large area organic photovoltaics (OPV)[2] and large area electrochromic displays (EC).[3] We find especially that an elevated operational temperature is beneficial with respect to both transconductance and on/off ratio. We achieve high currents of up to 45 mA at a temperature of 80 °C with an on/off ratio of 100 which is sufficient to drive large area organic electronics such as an EC device powered by OPV devices that we also demonstrate. Finally, we observe a significant temperature dependence of the performance which can be explored further in sensing applications.

The printed organic electronics toolbox already includes a large number of components and technologies such as displays,[4] EC,[3,5] transistors (OFET),[6–9] memory,[10,11] OPV,[2,12,13] sensors,[14] supercapacitors,[15] batteries,[16] and antennas.[17] All exist in a number of forms and all will be required for the realization of complex circuitry according to the vision of integrated organic electronics (IOC).[18,19] Thus, briefly explained it is a thin flexible material with complex function that allows for human interaction while presenting ultrafast manufacturing routes, using only abundant materials, with a low thermal budget and a low environmental impact in preparation, use, and disposal. The majority of research has been focused at improving and perfecting each individual device type and has with excellence explored the boundaries of each phenomenon when viewed academically and technologically. The next level comprises the integration of these individual device types into operational circuitry, and here, the individual requirements of each technology suddenly place both demands and constraints on each other. As an example, the driving of a large area EC using an organic transistor powered by an organic solar cell presents new limits according to the application and not limits arbitrarily chosen by experiment. For a given area of the electrochromic, a certain drive current will be needed and, therefore, the current handling of the transistor must match the electrochromic and the supply of power from the solar cell must match both voltage and current requirements under a given set of light harvesting conditions that will determine the area of the solar cell. The compatibility between device technologies in the toolbox is thus at the verge of exploration and further progress of printed organic electronics relies on the boundaries being fully charted. In addition to the operational requirements, further constraints are imposed by the route to manufacture which most logically should be a R2R printing methodology in order to address the vision of fast manufacture at low impact. In the case of solar cells, electrochromics, and transistors, the scaled manufacture[20–23] has been amply demonstrated, but in the case of the organic transistor, little development has been dedicated to devices with fully flexoprinted S/D, with large power handling capacity, and especially, the thermal behavior has not been addressed in the context of integration which we report here.

The thermal behavior of the materials that comprise a transistor is influential on the available power handling and choosing organic materials as the source has some implications when it comes to power handling. The substrate material polyethyleneterphthalate (PET), the active material (P3HT),

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and the dielectric (PVP), all have very similar and low thermal diffusivity (in the range of 0.08–0.144 $mm^2 s^{-1}$)[24] which is far from the inorganic materials currently employed in electronics such as silicon (88 mm^2 s^{-1}). Similarly, the thermal conductivity is also lower for these materials by orders of magnitude with values in the range of 0.33–0.52 $W \cdot m^{-1} \cdot K^{-1}$ compared to silicon (148 $W \cdot m^{-1} \cdot K^{-1}$). This can of course be expected to severely limit use in some areas but can perhaps also be used as an advantage in certain areas of application such as thermal sensing and when used in combination with other technologies having similar requirements. The manufacture also places some constraints, since printing methods has limitations to the achievable resolution as compared to lithographic techniques commonly used in inorganic semiconductor processing.

Based on this, we propose an extreme design where the S/D electrodes are fully flexoprinted with an interdistance channel length (L) smaller than 50 μm by deliberate exploitation of smearing and the halo effect in flexoprinting yielding an active transistor area of 0.2 cm^2, for a device of 0.7 cm^2, in order to maximize current and thermal diffusion. The interdigitating S/D pattern design has 41 terminals connected in series; a schematic is shown in Figure 1a and an optical image detail is reported in Figure S1. With this design, S and D are interchangeable and applying positive or negative SD voltages is equivalent. The length of a terminal is 0.9 cm, which corresponds to the single channel width (W).

We use standard P3HT material[25–28] deposited in air under ambient conditions. Under these conditions, we are able to fabricate and study a non-ideal device that presents intrinsic doping, due to impurities, defects, and charge trapping.[29,30] The semiconductor in the OFET has a certain level of oxidation, whereby, we obtain a p-type transistor with no threshold G voltage.

The device is built on a 125 μm PET substrate where silver S/D electrodes are flexoprinted with a R2R machine at a web speed of 20 m min^{-1} (see Figure 1b–d). For the prototype development, a P3HT layer of 100 nm is spin coated and covered with 1 μm PVP dielectric material,[31,32] also spin coated, followed by thermal evaporation of the silver G electrode on top. After optimization of the thicknesses, the fabrication with slot-die coating of P3HT and PVP followed by screen-printing of the silver G electrode was successfully carried out (see Figure 1e) with the same thicknesses (for a detailed Experimental Section see SI). These fabrication methods might overcoat the S/D collectors and the finger electrode ends with P3HT, which can induce additional parasitic effects and variations from a standard OFET.[33]

We set the characterization voltage in the linear region for the P3HT transistor, with measurements between –30 and 30 V. The transistor output characteristic at a room temperature of 25 °C shows the absence of a threshold voltage current due to intrinsic doping/impurities of the material as shown in Figure 2a. The applied G voltage can vary the transistor characteristics, and a G voltage of 30 V is not sufficient to switch off the device (the current is reduced by a factor 2). We present the transfer characteristics at the same temperature in Figure 2b. Here, it is clear how the G voltage has little influence on the device performance. This is probably due to the formation of trapping sites that inhibit the conduction of carriers.[34,35]

Depending on the temperature, we expect that the behavior of the transistor will change. We avoid other source of variations due to the top G configuration: the OFET can be considered light independent, because of its thick silver G; and air invariant, because of its 1 μm PVP layer. To evaluate the OFET dependency on temperature, we set the starting temperature, when no current is passing through the device, and then, we measure the OFET characteristics. When we set the temperature to 80 °C, we observe that the device exhibits the highest current achievable (Figure 2c). This is probably due to a higher carrier mobility, for the mobility values see Table S2, and the filling of charge trapping states inside the semiconductor. Because of the higher temperature, the P3HT material responds better to the G voltage (Figure 2d). In this case, a G voltage of 30 V is enough to turn off

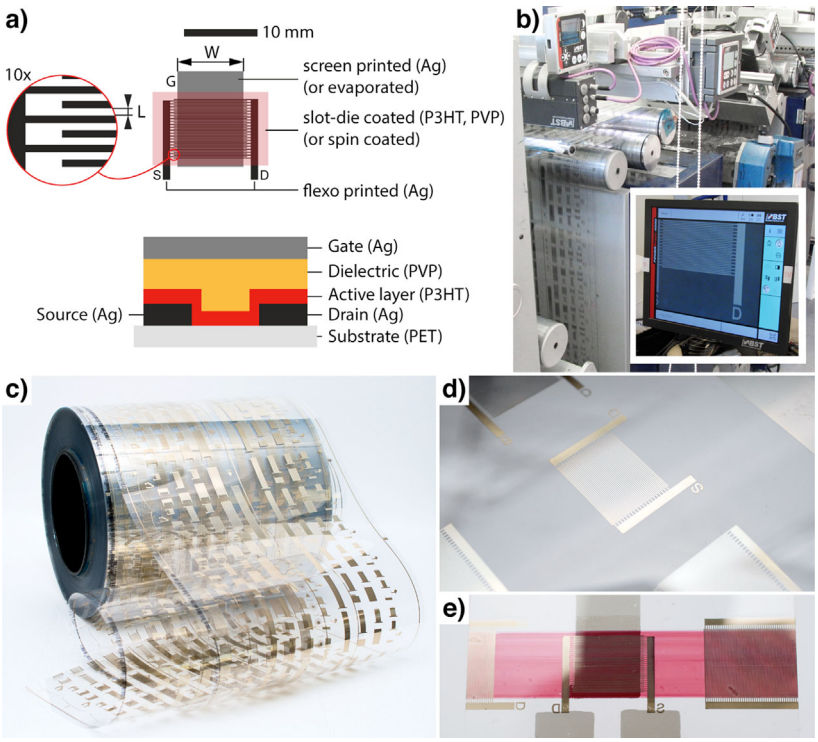

Fig. 1. Schematic and pictures of the manufactured P3HT OFET: (a) OFET top view schematic (above) and side view schematic (below). (b) R2R flexo printed process for S and D electrodes, (c) flexo printed silver electrodes, (d) detail of the SD printed electrode in the R2R process, (e) slot-die-coated P3HT layer combined with the flexo printed SD electrode and screen printed G electrode.

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the transistor giving an on/off ratio of 40 for a SD voltage of between 20 and 30 V.

At a temperature of 120 °C (Figure 2e), the material performance decreases probably due to the PET substrate deformation and an increase in thermal noise in the semiconductor.[36] Not all the charges contribute to the SD current of the device. Figure 2f illustrates that for a temperature of 120 °C, a G voltage of 30 V is effective in bringing the current close to zero, achieving an on/off ratio of 100 for a SD voltage of between 20 and 30 V. The first effect that we notice is the increase of carrier mobility with respect to the temperature. The second noticeable effect is how the trapping states, inside the semiconductor, are less important above 25 °C. At higher temperatures, the current grows almost linearly until 80 °C. Then, as a third effect, we observe that the "thermal noise" reduces the current until 120 °C. The temperature limit for the device is 140 °C, since this is both the damage threshold for the P3HT material and for the PET substrate.

An important point can be extrapolated by observing the increase in temperature due to the high current flowing between S and D; when we deal with currents on the order of tens of milliamperes, the temperature increase (ΔT) in such device can easily be above 15 °C. In our setup, we place the OFET on top of a Peltier cell (see Figure 2g) to control the starting temperature and we use an IR camera for monitoring the device temperature locally, see SI for more details. In Figure 2h, we show the thermal map image of the OFET in an OFF state (see the transfer characteristic of Figure 2d). The SD voltage is fixed to 30 V and the G voltage is 24 V. Here the current is around 1 mA and the top temperature is about 82 °C. When we drive the OFET to the ON state and to its maximal current, 45 mA, the ΔT is above 15 °C and the device reaches a top temperature of 97.5 °C (Figure 2i). We assume that ΔT is one of the reasons why we start to see a nonlinear behavior with a G around –30 V.

In Figure 3a, we lowered the SD voltage to 2 V because we wanted to interface the OFET to an EC cell, for the driving circuit diagram see Figure S3. At this low voltage, we can also better understand the physics of the device, and indeed, it indicates that there is not only a thermal noise that reduces the overall current of the device above 90 °C but also that the semiconductor can support electron diffusion. At a low SD voltage of 2 V, we observe a growing drift current, symbolized

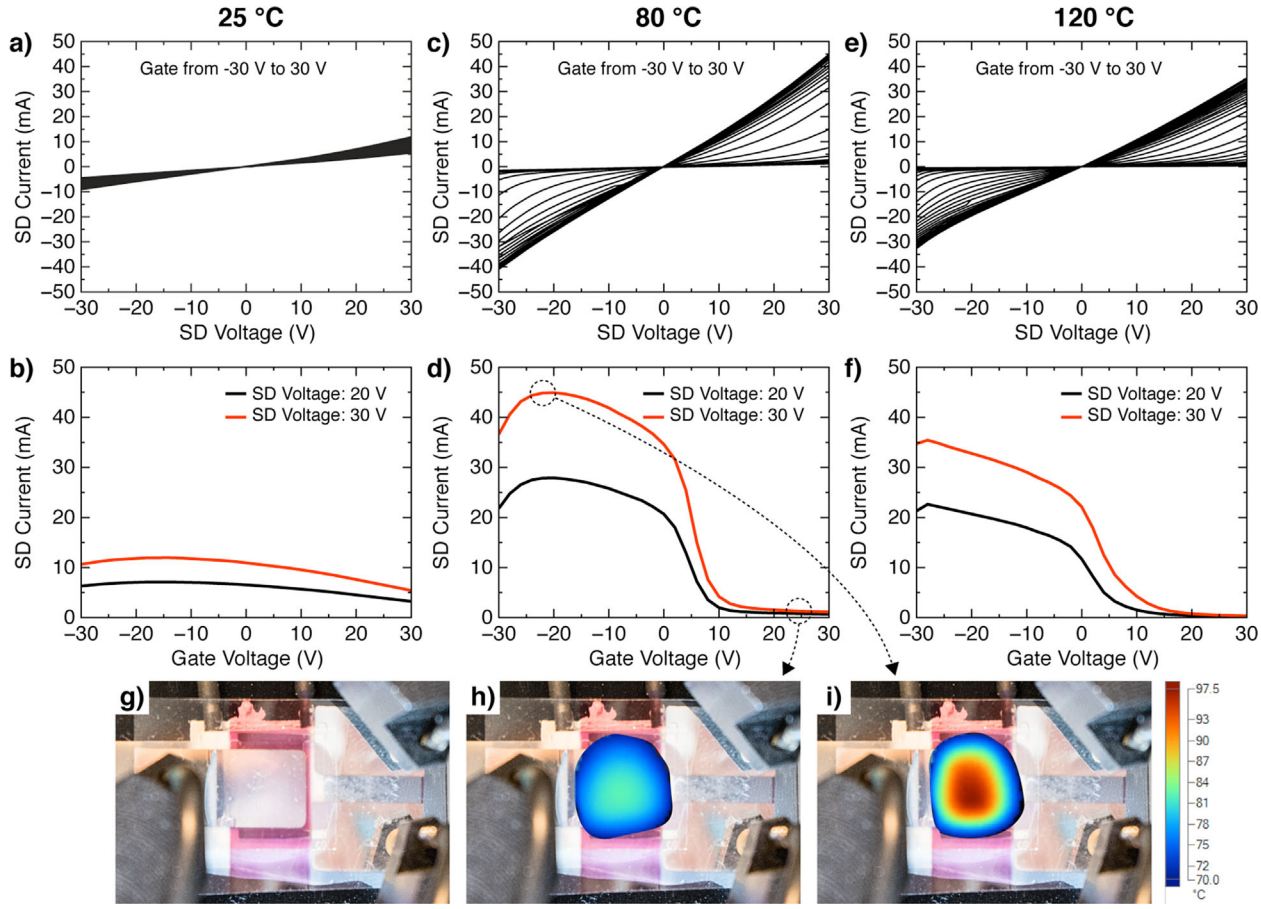

Fig. 2. Characteristics of the OFET and thermal mapping: (a) output characteristic at 25 °C, (c) at 80 °C, (e) at 120 °C; (b) transfer characteristics at 25 °C, (d) at 80 °C, (f) at 120 °C; (g) optical picture of the device in the measurement setup; (h) optical and thermal image for the device in OFF state, G at 24 V and SD at 30 V, and (i) device in ON state, G –24 V and SD at 30 V.

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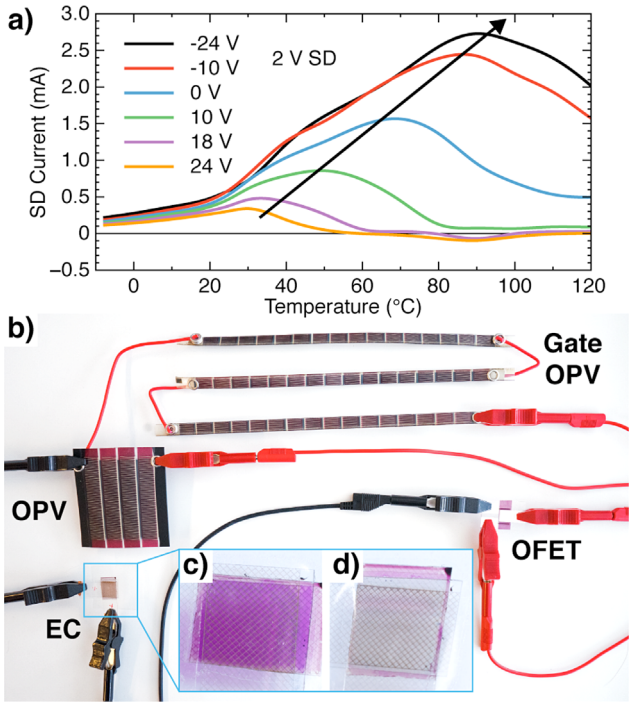

Fig. 3. Operating conditions and circuit image of the OFET when driving an EC cell: (a) temperature dependence of the OFET for SD voltage = 2 V; (b) OPV module on the left delivers the power to the OFET and the EC, the OPV stripe above is used to provide the G voltage (for driving circuit diagram see Figure S3) (c) EC OFF state, the light is blocked; (d) EC on state, the light can pass through.

by the arrow in Figure 3a, from a +10 V G voltage and down to –24 V. Instead, for an electric potential tension between +10 and +24 V, we are in a subthreshold current region. Here, we see not only that the channel for holes is closed but also that the semiconductor can support (at temperatures between 60 and 100 °C) the transport of electrons. In this temperature range, and with a G voltage of about 20 V, we observe an inversion of the dominant charge carrier. This can be due to three effects: firstly, all the trap states for electrons are filled for a certain temperature/voltage condition. Secondly, at high temperature, the semiconductor reduces temporally its high level of oxidation that can be combined reversibly with free radicals.[37] Thirdly, reduction of the potential barrier for the electrons increases their contribution to the overall current in the semiconductor.

To test the fabricated OFET, we designed a circuit employing fully R2R printed OPVs and ECs as shown in Figure 3b which has a 2 V high current OPV module comprising four serially connected single junctions as a solar power source connected to the transistor across the S/D terminals. The G voltage is kept at 24 V by use of another low current OPV module comprising 48 serially connected single junctions. The circuit is connected to an electrochromic device that is in a colored "OFF" state (Figure 3c) when no current is passing through the circuit and in the colorless "ON" state (Figure 3d) when the current is passing through the circuit. At room temperature and with a G voltage of 24 V, the current can circulate (see Figure 3a) and the EC cell is in an "ON" state where the light transmission is maximal (Figure 3d). When the transistor temperature reaches 60 °C, the current channel is closed and the EC device naturally evolves to an "OFF" state where the light transmission is minimal (Figure 3c).

Dimensioning the various elements, we know that if we want to fully switch the EC during the course of 1 min with a voltage of 2 V, we need 1 mA for every 100 cm^2. This implies that for 100 cm^2 of EC area, we only need 1 cm^2 of transistor and roughly 1 cm^2 of OPV that can also provide power with solar irradiation below 0.2 sun. The gate OPV stripe can be as thin as few millimeters because we only need it to supply a G voltage with minimal current. With a meter long stripe of our OFET, it would be possible to guarantee power for a square meter of an EC window. In Figure 4, we schematize the real size proportion of the various components for a plastic foil standalone EC device comprising both power supply and drive electronics. This configuration can be fully printed and applied to any sun-exposed surface as a simple coated and printed film without the need of external power supplies.

In conclusion, we have reported a new large area OFET that can be thermally and/or electrically driven. The different layers of the device were manufactured with flexoprinting and slot-die thin film techniques. The high precision flexographic technique results in an interdistance channel length, L, lower than 50 μm. This contributes in having an unprecedented peak current of 45 mA when the device has an initial temperature of 80 °C. We used such a transistor in a standalone circuit with an OPV module as power source, another OPV module for the G voltage, and an EC as the load device. The EC was driven utilizing the OFET at different temperatures. We showed the possibility of implementing this

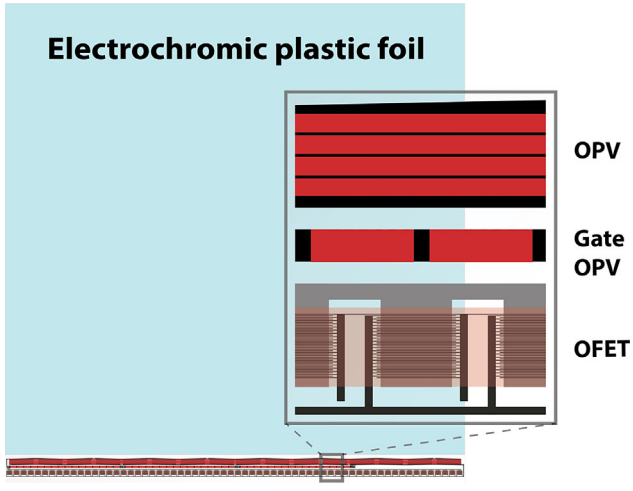

Fig. 4. Illustration of the achievable footprint of respectively the EC, OPVs, and transistors on plastic foil for shading application to apply to, for instance, a window surface. The light cyan background represents the area of the EC device that can be electrically driven and switched on and off using OPVs and transistors at the very bottom. The inset magnifies the 3 stripes below the EC area, the first stripe represents the OPVs for power generation, the second one is for the G voltage OPVs, and the last stripe represents the OFETs.

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printed standalone solution prospecting a future for fully R2R processed IOC.

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