THÈSE

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Circuits CMOS et BiCMOS pour une conversion de fréquence efficace jusqu'aux fréquences millimetriques

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Thesis in Co-tutele

with

University of Modena and Reggio Emilia

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Director: Prof. Giorgio Matteo VITETTA

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Ecole Doctorale Génie Electrique, Electronique, Télécommunications

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Alessandro MAGNANI

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in: **Electronics and Telecommunications**

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Discussion scheduled for 14 April 2014

Examinators:

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Docteur

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Alessandro MAGNANI

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1 General Introduction

The continuous improvements of SiGe BiCMOS and Si CMOS technologies have made it possible to build low-cost radio receivers up to millimeter-wave frequencies [1]. As well known, the front-end receiver is a building block of primary importance in wireless communication systems. Its main purpose is to recover the high frequency transmitted signal and make it available for the base-band signal processing. A building block diagram of a general front-end receiver architecture is depicted in figure 1.1. The antenna picks up the high frequency signal emitted by a remote transmitter and delivers it to the front-end input. First of all this signal undergoes a low noise amplification performed by the Low Noise Amplifier (LNA). The LNA amplifies the signal amplitude to a large enough value for the following signal conditioning. As a second step, the amplified high frequency signal is pass-band filtered for sake of image frequency rejection and finally it is down-converted by the mixer to an intermediate frequency (IF).

In the case of an homodyne receiver architecture, where the intermediate frequency is the base band, the image rejection filter before the mixer is no more required. The down-conversion mixer is driven by the local oscillator tone (LO), which is generated by a frequency synthesizer, that usually comes in the form of a PLL synthesizer.

The performance of the whole radiofrequency front-end should satisfy the specifications imposed by the addressed telecom standard. Usually this is obtained by a tricky trade-off work carried out through a spreadsheet in the easiest cases or through system level simulations in the hardest ones. In this optimization procedure, the performance of each building block is traded off with the performance of the others. To put the output of the system level optimization into the real world, that is to translate the system level spec of each building block in silicon, it is of primary importance to be able to manage at the best the performance of each building block at physical level, which means to master at the best the circuit in terms of both at schematic and layout level.

In particular, the research activity reported in the present PhD thesis addressed the PLL and down-conversion mixer topics with the idea in mind of investigating the potentialities of the 130 nm silicon technology for applications in the Ku (12-18 GHz) and K (18-27 GHz) frequency band. For the lowest band a bulk pure 130nm CMOS technology

by ST Microelectronics has been employed to design a PLL useful for Digital Video Broadcasting Satellite (DVB-S) applications. For the highest band a more sophisticated 130 nm SiGe BiCMOS technology by IBM has been preferred to design a high frequency sampling passive down-converter. The present PhD thesis is organized as in the follows.

Chapter 2 concerns the design of the Ku band PLL. The fabricated prototype is a meaningful breakthrough of the current state-of-the-art, because it is, at the best knowledge, the first CMOS PLL providing evidence that a pure, low-cost, bulk CMOS technology can be addressed for the fabrication of a DVBS synthesizer, where, in the literature, more expensive integrated and/or discrete technologies are employed.

Chapter 3 is devoted to the design of the down-converter. The fabricated prototype outperforms the literature, because it is the first example of high frequency sampling passive down-converter working up to K band frequencies. The chapter therefore highlight the potentialities of this circuit topology well beyond the actual low frequency operating range.

Finally, chapter 4 proofs, thanks to sub-sampling technique applied to the chip realized in the chapter 3, its operating frequency range extension up to millimeter-wave frequencies. The 60 GHz Industrial, Scientific and Medical (ISM) band has been targeted. The work presented in both chapter 3 and 4 was supported under the Région Midi-Pyrénées and French state ELECTRA 2010 funded project WIATIC.

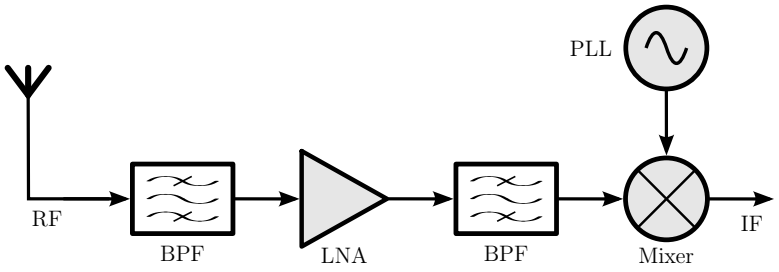


Figure 1.1: *Receiver block diagram.*

2 Ku-band Phase Locked Oscillator

2.1 Introduction

Several mass market applications, as for example, Standard and High Definition TeleVision (SDTV and HDTV), interactive multimedia, data content distribution and professional TV applications use a portion of Ku band spectrum reserved for point to point and broadcasting satellite communications. Nowadays, in satellite receivers, the signal is picked up by the dish antenna and then amplified and down-converted by a low noise front-end. This block is frequently built using discrete compound semiconductor High Electron Mobility Transistors (HEMT) and implements Dielectric Resonator Oscillators (DRO), as well. This discrete approach is expensive due to components, assembling operations, and the resonator manual tuning [2]. A silicon-based monolithic integrated receiver offers secure advantages in term of cost and size, especially using an integrated local oscillator. Nevertheless, performance limitations of integrated solutions are still restricting this kind of solutions for penetrating high frequency mass market applications such as Digital Video Broadcasting Satellite (DVB-S) [3]. Some efforts have led to several prototype as a monolithic 0.8 µm bipolar technology Low Noise Block (LNB) by STMicroelectronics [2], and more recently, a 0.25 µm SiGe:C commercially available BiCMOS technology LNB was reported by NXP Semiconductors [3]. Avoiding the use of bipolar transistors is of great interest as well, which is the aim of [4] and [5], presenting a 0.18 µm CMOS LNA/down-conversion mixer chain and a LNB, respectively. In all reported examples, the frequency synthesizer used to generate the local oscillator (LO) signal consists in a Phase Locked Loop (PLL). This kind of implementation requires a programmable frequency divider in the feedback loop. To easier demonstrate the potentiality of a technology for a given application where a local clock and/or a local frequency are required, the use of a Phase Locked Oscillator (PLO) can be then a good alternative because the frequency divider in a PLO exhibits a fixed modulus, making in this way easier the design. The present chapter reports on the design and the characterization of a Ku-band PLO realized with a bulk 130 nm CMOS technology. The operation frequency of the PLO was chosen so that to test its potentiality for both up-link

($12.9 \div 18.4\,\text{GHz}$) and down-link ($10.7 \div 12.75\,\text{GHz}$) frequency band. Particular attention has been done on phase noise which is the hardest specification to be satisfied. This because the modulations schemes (APSK) adopted in DVB-S standard exhibits a round constellation where excessive rotational errors due to excessive phase noise would produce a burst of error [6]. The PLO can be also used as local oscillator in the architecture of a microwave radiometric front-ends [7]. Several applications in the microwave radiometry field, such as industrial harsh plants, where conventional sensor can not be employed, or automotive safety, require cost and size reductions of the radiometer. For example, in order to keep low the cost, the emitted black-body radiation is usually detected with a low cost printed antenna array [7, 8], which size depends on the operation frequency. Therefore, a PLO working at higher frequency allows a reduction of the antenna size. For a 8×8 array patch-antenna with a gain of 25 dB, when the operation frequency moves from X-band to Ku-band, as in the present case, the antenna area shrinks of 2.5 times, from $10 \times 10\,\text{inch}^2$ to $6.3 \times 6.3\,\text{inch}^2$ [9]. Microwave radiometry is considered also an interesting solution for wild fire detection. In order to minimize the maintenance cost of the batteries, the microwave radiometer collocated in each node of the smart sensor network distributed on the wild area should be energy independent as much as possible, exploiting renewable energy sources, as integrated microphotovoltaic cells or harvesting circuits [10]. Therefore, dissipated power reduction is a further parameter of paramount importance. Using, as in this case, low power technology allows to solve this constraint, making easier to target the energy independence of each node of the smart sensor network. When bias voltage moves from a 3.3 V of a 0.35 µm technology to a 1.2 V of a 130 nm technology, a significant reduction of the dissipated power has to be expected. Therefore, the use of a higher operation frequency and more scaled technology with respect to those reported in [7] allows to address the above discussed advantages of reduction in size and dissipated power. This chapter is organized as follows. After a brief theoretical recall of PLL linear model in 2.2, the PLO architecture and the design of each building block are described in Section 2.3. Simulations resuls and experimental results are summarized in Section 2.4 and Section 2.5 followed by some considerations. Finally conclusions are drawn in Section 2.6.

2.2 Theoretical recalls

2.2.1 Phase locked loop linear model

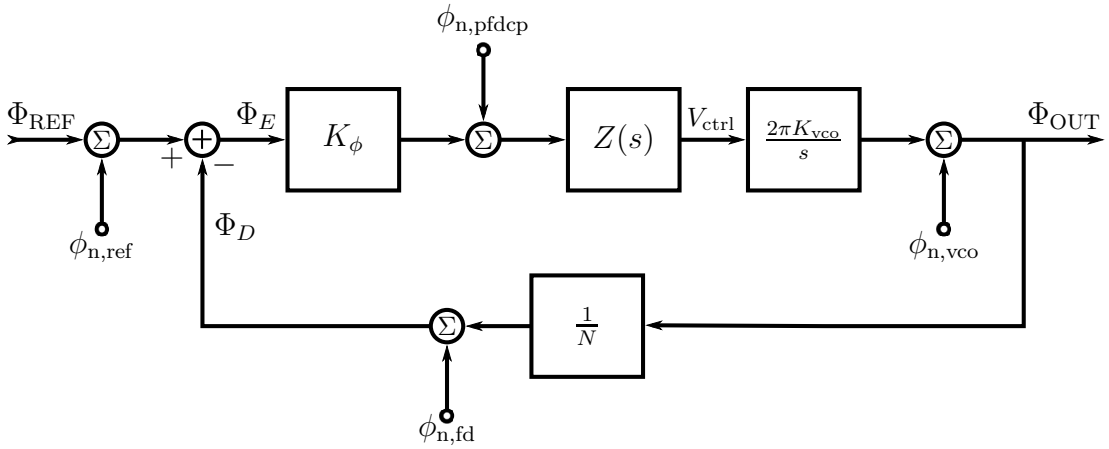


Figure 2.1: *PLL linar phase-domain model.*

For good loop estimation performances, whole PLL system can be described using a linearized model. For modeling the behavior of the PLL to small perturbations when the PLL is in lock condition, the PLL linear phase-domain model depicted in figure 2.1 can been used as indicated in [11].

As known, the voltage controlled oscillator converts its input voltage to an output signal with a known frequency $f_{OUT}(t) = K_{VCO} \cdot v_{ctrl}(t)$ where K_{VCO} is the VCO gain in $\mathrm{V} \cdot \mathrm{Hz}^{-1}$. Integrating and applying the Laplace transform at this expression, VCO phase-domain characteristic needed in a phase-domain model is obtained

$$\Phi_{OUT}(s) = \mathcal{L}\left\{2\pi \cdot \int K_{VCO} v_{ctrl}(t)\, dt\right\} = \frac{2\pi K_{VCO}}{s} V_{ctrl}(s) \tag{2.1}$$

Given a signal $v_i(T)$, a frequency divider will produce an output signal $v_o(NT)$ where N is the divide ratio. Therefore, the phase transfer characteristic of a divider is

$$\Phi_o = \frac{\Phi_i}{N} \tag{2.2}$$

Divided signal is compared with the reference by the phase frequency detector. The phase difference Φ_E is converted in a current signal by the charge pump. The output of the charge pump immediately passes through a low pass filter with $Z(s)$ transfer function that it carry out both current-voltage conversion and high frequencies signal suppression.

So, the pulse nature of charge pump output can be ignored and hence the average charge pump current will be take into account [11]. Thus, the transfer characteristic of the combined PFD-CP become

$$< i_{\mathrm{cp}} >= I_{\mathrm{CP_{max}}} \frac{\Phi_{\mathrm{REF}} - \Phi_D}{2\pi} = K_\phi \cdot (\Phi_{\mathrm{REF}} - \Phi_D) \tag{2.3}$$

where $K_\phi = I_{\mathrm{CP}}/2\pi$ is the PFD-CP characteristic gain.

For PLL noise phenomena study, single noise sources of the PLL components as integrated in the model. Generally, there can be identified two principal noise transfer functions. The noise sources that can be referred back to the input such as PFD-CP, frequency divider, loop filter and reference signal (generically indicated by $\phi_{\mathrm{n},in}$) undergo a low-pass function F_{ref} whereas the VCO contribution that is referred to the output undergoes a high pass function F_{vco} [12].

$$F_{\mathrm{ref}} = \frac{\Phi_{\mathrm{out}}}{\phi_{\mathrm{n},in}} = \frac{\frac{K_\phi Z(s) 2\pi K_{\mathrm{vco}}}{s}}{1 + \frac{K_\phi Z(s) 2\pi K_{\mathrm{vco}}}{Ns}} \tag{2.4}$$

$$F_{\mathrm{vco}} = \frac{\Phi_{\mathrm{out}}}{\phi_{\mathrm{n},vco}} = \frac{1}{1 + \frac{K_\phi Z(s) 2\pi K_{\mathrm{vco}}}{Ns}} \tag{2.5}$$

Defining the open loop gain G_{OL} as

$$G_{\mathrm{OL}}(s) = \frac{\Phi_I}{\Phi_E} = \frac{K_\phi Z(s)}{N} \frac{2\pi K_{\mathrm{vco}}}{s} \tag{2.6}$$

equations (2.4) and (2.5) become

$$F_{\mathrm{ref}} = \frac{N G_{\mathrm{OL}}(s)}{1 + G_{\mathrm{OL}}(s)} \tag{2.7}$$

$$F_{\mathrm{vco}} = \frac{1}{1 + G_{\mathrm{OL}}(s)} \tag{2.8}$$

If $s \to \infty$ ($\omega \to \infty$) because of the VCO's pole the open loop gain $G_{\mathrm{OL}} \to 0$ hence F_{vco} and F_{ref} tend to 1 and 0 respectively. Therefore, at higher frequency the noise of the PLL is that of the VCO as expected because the low-pass filter blocks any feedback at high frequency. Instead, if $\omega \to 0$, ever for the VCO's pole this time $G_{\mathrm{OL}} \to \infty$ and consequently $F_{\mathrm{vco}} \to 0$ and $F_{\mathrm{ref}} \to 1$. Otherwise, at low frequency, the VCO noise is lowered by the loop gain and the PLL noise depends by the noise contributions of PFD-CP, frequency divider, loop filter and reference signal. In latter case, further considerations on the VCO noise can be done. Knowing that VCO power spectral density $S_{\phi_{\mathrm{vco}}}$ neglecting

flicker noise is directly proportional to $1/\omega^2$, filter presence become important. Indeed, if $Z(s) \propto 1$ (without the filter) the VCO output noise power $F_{\text{vco}}^2 S_{\phi_{\text{vco}}}$ is finite and nonzero. However, choosing charge pump topology, $Z(s)$ adding at least one pole hence the VCO output noise power goes to zero [11].

2.2.2 Loop filter

Overal system order depends on the selected loop filter order. The simpler solution is a two poles 2^{nd}-order filter shown in figure 2.2a to build a 3^{rd}-order overall system. It is composed by capacitance-resistance series shunted with a second capacitance. The latter C_2 is recommended to avoid discrete voltage step in the VCO's control voltage node due to instantaneous sudden charge pump output variations, answerable for references spurs. If a stronger spurs suppression is required, another pole should be added using 3^{rd}-order filter shown in figure 2.2b, for a 4^{th}-order overall system. Taking into account the simpler case, the filter transfer function becomes:

$$Z(s) = \left(R_1 + \frac{1}{sC_1}\right) // \frac{1}{sC_2} = \frac{1}{sC_2} \cdot \frac{T_p}{T_z} \cdot \frac{1 + sT_z}{1 + sT_p} \tag{2.9}$$

where $T_z = R_1 C_1$ and $T_p = R_1 C_1 C_2 / (C_1 + C_2)$ are zero and pole time constants respectively.

Substituting the $Z(s)$ expression 2.9 in 2.6 results that

$$G_{\text{OL}}(s) = \frac{K_\phi 2\pi K_{\text{VCO}}}{sN} \cdot \frac{1}{sC_2} \cdot \frac{T_p}{T_z} \cdot \frac{1 + sT_z}{1 + sT_p} \tag{2.10}$$

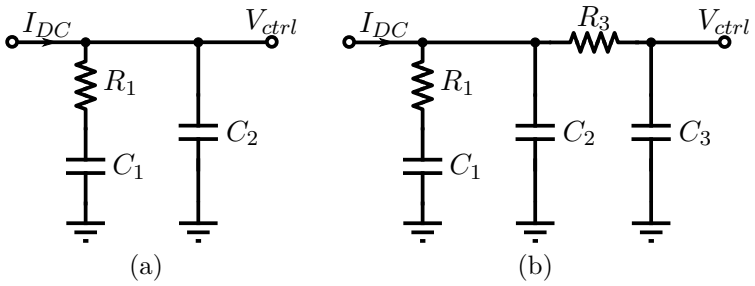


Figure 2.2: *Schematic of 2^{nd} (a) and 3^{nd}-order (b) loop filter.*

Since $s = j\omega$ open loop magnitude and phase expression is equal to:

$$|G_{\mathrm{OL}}(j\omega)| = \frac{K_\phi 2\pi K_{\mathrm{VCO}} T_p}{\omega^2 N C_1 T_z} \cdot \frac{\sqrt{1+(\omega T_z)^2}}{\sqrt{1+(\omega T_p)^2}} \tag{2.11}$$

$$\underline{/G_{\mathrm{OL}}}(j\omega) = 180 + \arctan(\omega T_z) - \arctan(\omega T_p) \tag{2.12}$$

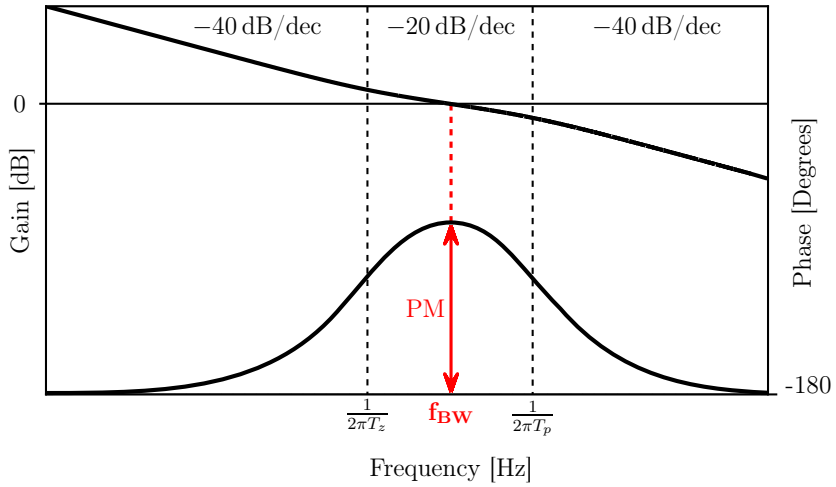


Figure 2.3: 3^{rd}*-order overall system magnitude and phase information of open loop gain.*

whose trend is plotted in 2.3. The two PLL parameters of paramount importance for the design are the bandwidth f_{BW} and the phase margin PM, highlighted in 2.3. The first is the frequency ω_{BW} corresponding to $|G_{\mathrm{OL}}(j\omega)| = 0\,\mathrm{dB}$ while the second is evaluated as the difference between -180° and $\underline{/G_{\mathrm{OL}}}(j\omega)$ when the frequency is equal to ω_{BW}. In order to ensure stability, the phase margin must be chosen between 30° and 70°: trade off between higher stability and slower loop response time should be considered. Nonetheless it should be no less than 45°and also to reduce peaking in closed-loop gain which produce excess phase noise, the phase margin is typically 60°or more [11].

To find the frequency point for which the phase reaches the maximum (2.12) is derived and forced to 0 to obtain a bandwidth relationship depending on pole and zero value:

$$f_{\mathrm{BW}} = \frac{1}{(2\pi\sqrt{T_z T_p})} \tag{2.13}$$

In the same wave, putting $\omega = \omega_{\mathrm{BW}} = 2\pi f_{\mathrm{BW}}$ in (2.12), equation (2.14) is obtained

$$\tan(PM) = \frac{\omega_{\mathrm{BW}} T_z - \omega_{\mathrm{BW}} T_p}{2} \tag{2.14}$$

Using equations (2.13) and (2.14) after some mathematical steps reported in [13], T_z and T_p expression results become

$$T_p = \frac{\sec(PM) - \tan(PM)}{\omega_{\mathrm{BW}}} \tag{2.15}$$

$$T_z = \frac{1}{\omega_{\mathrm{BW}}^2 T_P} \tag{2.16}$$

Therefore, for both bandwidth and phase margin given and knowing whole block parameters such as K_{VCO}, K_ϕ and N, the LF components value are obtained using equations (2.17), (2.18) and (2.19)

$$C_1 = C_2 \left(\frac{T_z}{T_p} - 1 \right) \tag{2.17}$$

$$C_2 = \frac{K_\phi 2\pi K_{\mathrm{VCO}}}{\omega_{\mathrm{BW}}^2 N} \cdot \frac{T_p}{T_z} \cdot \frac{\sqrt{1 + (\omega_{\mathrm{BW}} T_z)^2}}{\sqrt{1 + (\omega_{\mathrm{BW}} T_p)^2}} \tag{2.18}$$

$$R_1 = \frac{T_z}{C_1} \tag{2.19}$$

If a 3^{rd}-order filter is used, the attenuation introduced by the third poles is $\alpha_{\mathrm{dB}} = 20 \log \left[(2\pi f_{REF} T_{P_3})^2 + 1 \right]$ where T_{P_3} is the time constant. For good dimensioning, this additional pole must be lower than the reference frequency in order to significantly attenuate the spurs but must be at least five time higher than the loop bandwidth otherwise the loop will almost assuredly become unstable. Recalculating the loop filter component with T_{P_3} contribution, C_1 and R_1 remain unchanged and C_2 become:

$$C_2 = \frac{K_\phi K_{\mathrm{VCO}}}{(\omega_{\mathrm{BC}})^2 N} \cdot \frac{T_p}{T_z} \cdot \frac{\sqrt{\left[1 + (\omega_{\mathrm{BC}} T_z)^2\right]}}{\sqrt{\left[1 + (\omega_{\mathrm{BC}} T_p)^2\right] \left[1 + (\omega_{\mathrm{BC}} T_{P_3})^2\right]}} \tag{2.20}$$

where f_{BC} is the new open loop unity gain frequency reported in [14]. As regards C_3 and R_3, they are normally arbitrarily chosen. General thumb rule is taking C_3 ten times smaller than C_2 to avoid T_{P_3} interaction with primary poles and R_3 must be chosen twice R_1.

2.3 Circuit design

2.3.1 General architecture

Figure 2.4 depicts the building block diagram of the designed PLO. It is constituted by a Phase Frequency Detector (PFD), a Charge Pump (CP), a second order Loop Filter (LF), a fixed modulus Frequency Divider (FD), and a Quadrature Voltage Controlled Oscillator (QVCO). The frequency division ratio (256) of the frequency divider is set for enabling the generation of Ku-band tone from an external reference frequency f_{ref} of about 60 MHz. The frequency divider is implemented from eight division-by-two stages. The first three stages are designed using a Current Mode Logic (CML) to achieve high operation frequency. Each CML stage is buffered in order to be able to drive the following divider stage. The division chain is completed with five low power digital frequency dividers realized with transmission gate registers. Because of the QVCO implementation, four output phases are available at PLO outputs. Finally, it is worth noticing that the loop filter is integrated on die for low cost considerations.

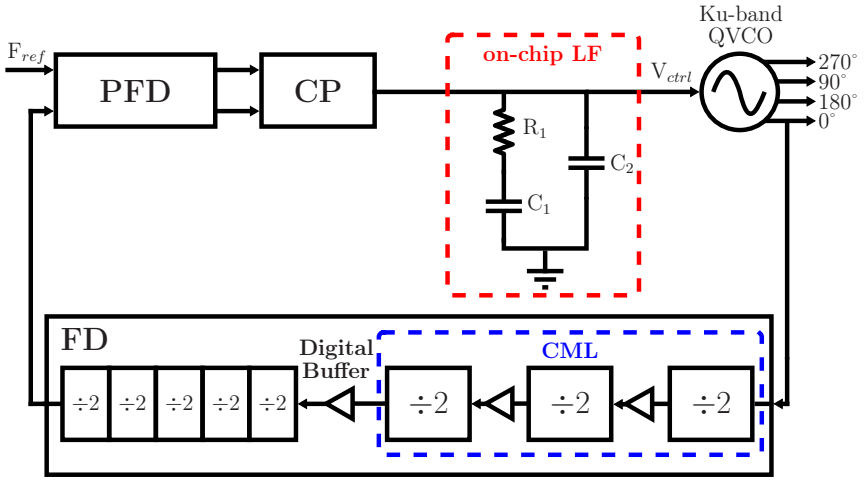


Figure 2.4: *Phase Locked Oscillator Blocks Diagram.*

2.3.2 Employed technology

The circuit is designed to fit with the commercial HCMOS9GP technology from STMicroelectronics. It is a triple well bulk CMOS technology with multiple voltage threshold transistors, for low leakage or high speed purposes, featuring an effective gate length of 130 nm. As shown in figure 2.5, the back-end features six copper layers with low-k inter-level dielectric and one aluminium layer on top, as reported in [15], [16], [17]. The

bias supply is typically 1.2 V even if the 2.5 V option is also available [16]. For the present design, low leakage, low threshold voltage transistors have been used with a supply voltage of 1.2 V. Several kinds of resistors are also available, as diffusion, salicied or unsalicied poly, and high resistivity poly resistors [18]. MIM capacitors, spiral inductors, and varactors are also available.

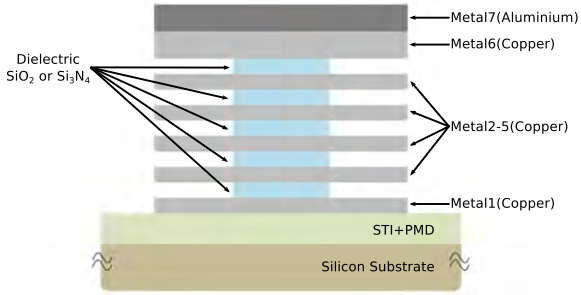


Figure 2.5: 130 nm *CMOS STM technology (HCMOS9GP).*

2.3.3 Quadrature voltage controlled oscillator

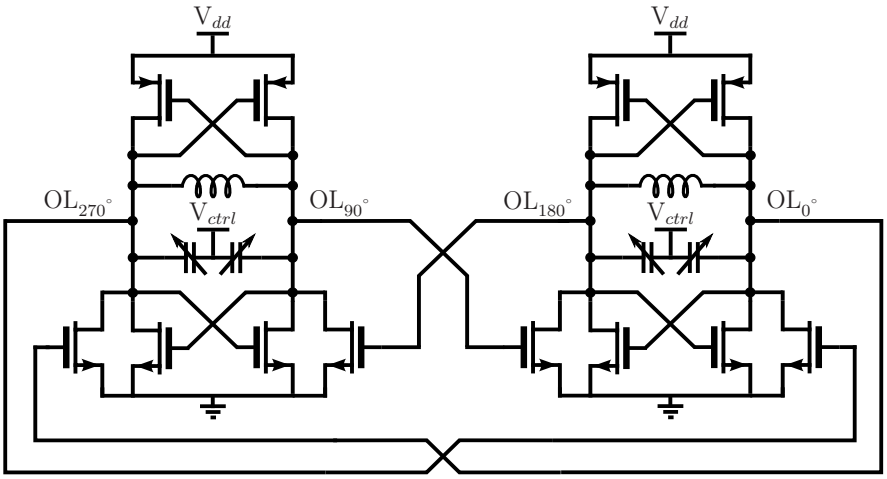


Figure 2.6: *Schematic of the Quadrature VCO.*

For generating signals in quadrature, the main techniques usually used are poly-phase filters, ring oscillators or frequency dividers. Nevertheless, for the present work targeted application, a solution from two cross-connected symmetric LC VCOs has been preferred because of the LC-oscillators good phase noise performances.

The schematic of the QVCO used in the present design is depicted in figure 2.6 and was previously reported in [19]. Here some features and performances are quickly

reminded; more details are available in [19]. The circuit is biased without current mirror to minimize the phase noise, the power consumption, and also to avoid any automatic control circuit. All transistors exhibit the minimum gate length. The width of the PMOS transistors is wide enough to ensure robustness against fabrication tolerances. The octagonal inductor at 15 GHz in the tank exhibits an inductance of about 290 pH and a maximum quality factor of 27. The tuning capability is achieved using two 20 fingers MOS varactors with a minimum gate length of 350 nm. For a carrier frequency ($f_{carrier}$) of 15 GHz, the dissipated power (P_{DC}) is 11 mW and the measured phase noise L(Δf) is -106 dBc/Hz at a carrier frequency offset (Δf) of 1 MHz.

2.3.4 Frequency divider

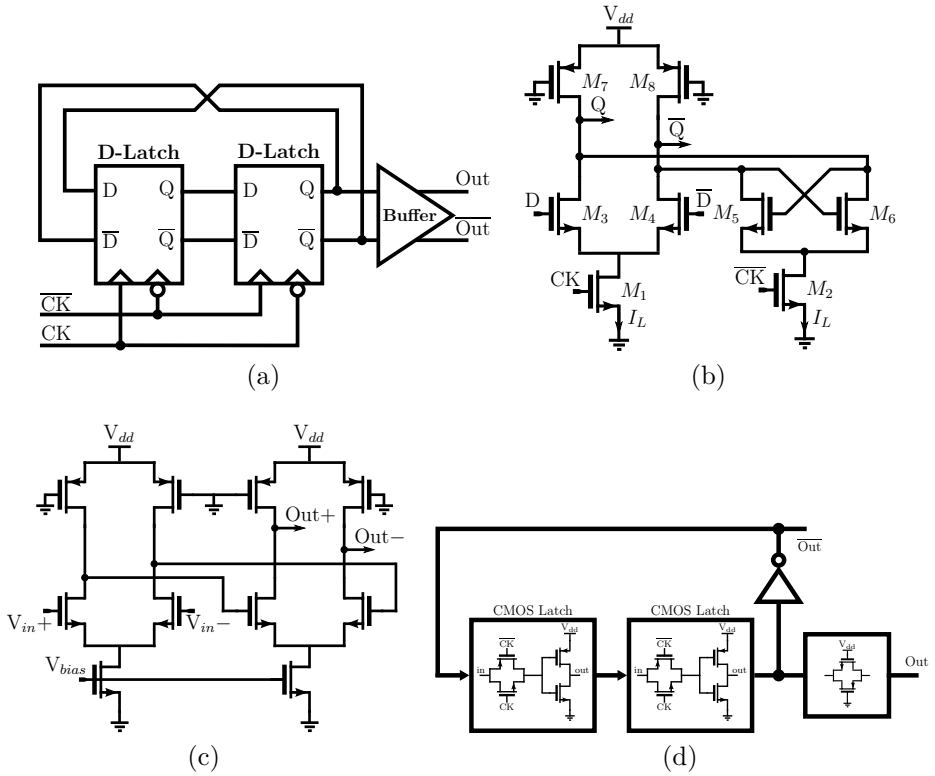


Figure 2.7: *Schematic of: (a) Master-Slave divide-by-two frequency divider, (b) CML latch, (c) CML buffer, (d) Digital divider*

As previously stated, the frequency divider is composed of eight division stages. Because it operates at high frequencies, each of the first three division-by-two stages is implemented from the CML latch depicted in figure 2.7b. The frequency division is

carried out by two latches arranged in a master-slave configuration and closed in feedback, as depicted in figure 2.7a.

The output buffer required for the driving of the following division stage, whose schematic is shown in Figure 2.7c, is designed from CML structures [20], as well. It is worth noticing here that the use of CML structures is well suited since their differential intrinsic topology contributes to reject the common mode noise injected from the supply and the substrate. Once related with PLO performances, this rejection translates into lower jitter and therefore into lower phase noise [21]. In the present work the CML latch, and of course the resulting frequency division CML chain, is inductor-less, using PMOS transistors as loads to minimize the layout area of circuits. Because of the low voltage bias, the traditional tail current bias is removed [22]. The inductor-less solution sounds reasonable, since it can provide a 130 nm CMOS static frequency divider operating up to 45 GHz frequency. Inductors become mandatory when a 130 n meter CMOS frequency divider should target millimeter wave frequencies [23].

Main feature of frequency divider design is the latch transistors sizing, especially for high frequency application. For this reason, several guideline have been followed. As reported in [24], using unstable circuits is necessary for efficient frequency divider design. Therefore, the following necessary and sufficient condition for instability (2.21) must be satisfied

$$g_{m5,6} \cdot R_{out} > 1 \tag{2.21}$$

where R_{out} is the output latch charge load and $g_{m5,6}$ is the small signal transconductance of cross-coupled transistors. Circuits that do not satisfy this condition may still function but a larger input clock amplitude is required [24]. Coarse maximum operation frequency f_{max} could be estimated using the following equation:

$$f_{max} < \frac{1}{2\ln(2)\, C_{out} R_{out}} \approx \frac{\sqrt{\mu_n C_{ox} \left(\frac{W}{L}\right)_{5,6} I_L}}{2\ln(2)\, C_{out}} \tag{2.22}$$

where $(W/L)_{5,6}$ is the cross-coupled latch section transistor size of $M_{5,6}$, I_L is the latch current, and C_{out} the whole capacitance viewed at the output [23] ($C_{out} \approx C_{gs}^{M_{3,4}} + C_{gs}^{M_{5,6}}$ neglecting C_{db}). To increase maximum operating frequency both the following solutions are possible:

1. increase I_L by increasing the transistors size. This would mean increase the capacitance C_{out} and the power dissipation making unattractive this solution.

2. reducing C_{out}; Since drive transistor $M_{3,4}$ should be large enough to quickly switch the latch output state between the available output swing, $C_{gs}^{M_{3,4}}$ cannot be much reduced. Therefore, the only way is to decrease $C_{gs}^{M_{5,6}}$ by decreasing the $M_{5,6}$ transistors size. This solution involves a transconductance loss directly proportional to $\sqrt{W_{5,6}}$ which will be compensate increasing R_{out}. Because of this, too small $W_{5,6}$ value must be avoided to keep satified equation (2.21)

For leading the next stage, higher output voltage swing V_{OS} is preferred to minimize $M_{3,4}$ transistors size. Logic high and low output voltage levels are V_{dd} and $V_{dd} - R_{out}I_L$ respectively. Therefore, the output voltage swing equation becomes:

$$V_{OS} = R_{out} \cdot I_L = \frac{I_L}{\sqrt{\mu_n C_{ox} \left(\frac{W}{L}\right)_{7,8} (V_{GS} - V_{TH})}} \tag{2.23}$$

V_{OS} is inversely proportionals to $\sqrt{W_{7,8}}$, hence for high output voltage swing $M_{7,8}$ small transistors sizes are better. The trade-off between instability condition and f_{max} as indicated in (2.22) should be take into account for the R_{out}. Finally input transistors $M_{1,2}$ should be large enough to minimize the voltage drop across the transistor keeping the parasitic capacitances as small as possible [22]. For the most critical first CML stage, the used transistor sizes are reported in Table I.

Transistors	Width [µm]
$M_{1,2}$	10
$M_{3,4}$	6
$M_{5,6}$	1.4
$M_{7,8}$	10

Table I: *First stage CML frequency divider transistrors width.*

Another paramount design features are good extraction and minimization of parasitics at the interface between the VCO and the frequency divider. Unpredicted and/or too large parasitics can translate into a frequency mismatch between the tuning range of the VCO and the sensitivity range of the frequency divider, making impossible the lock of the PLO. Therefore, a compact and carefully laid out layout of the frequency divider front-end allows the optimization of this interface by minimizing the parasitics. In order to assess the robustness of the circuit against technology dispersions, several post-layout simulations have been carried out under RC parasitic worst case of the VCO/divider interface and for several corner cases for transistors. Figure 2.8 plots the simulated

output frequency versus input frequency of the first CML divider stage. A slope of 0.5 certifies the proper operation of this divide-by-two stage. figure 2.8 shows that in the 6 GHz to 16 GHz frequency range, the CML divider stage is able to correctly work not only under the typical corner case (TT) but also under the Slow-Slow (SSA) and the Fast-Fast (FFA) corner cases, i.e. when the transistor transconductance is lower and higher than its typical value, respectively. Note that the frequency range where the circuit correctly works is larger (narrower) than the typical case when the transistors are fast (slow). The SSA case is therefore the most critical one. Similar simulations have been carried out for the other CML stages.

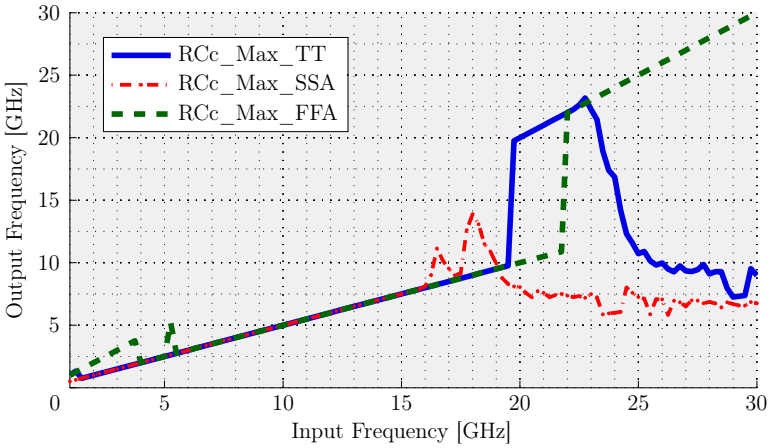


Figure 2.8: *Output frequency versus input frequency of the first CML divide-by-two frequency divider for several corner cases under worst case parasitic extraction.*

As far as the implementation of the last five division-by-two stages operating at lower frequencies, CMOS latches are used as basic cells for a dynamic solution where the transmission gates sample the input data and synchronize the transparent and opaque states as shown in figure 2.7d. As pointed out in figure 2.4, a digital buffer, simply composed by a cascade of two inverters, connects the CML and low frequency blocks. The whole division chain exhibits a simulated power consumption of about 10.5 mW. The small size of the whole frequency divider (figure 2.9), of $44 \times 154\,\mu m^2$, is mainly resulting from the inductor-less approach. Because in these conditions the connection between the QVCO output and the frequency divider can be very short (only few microns as pointed out in figure 2.9), RLC parasitic components of the connection are minimized ensuring a good frequency matching of these blocks.

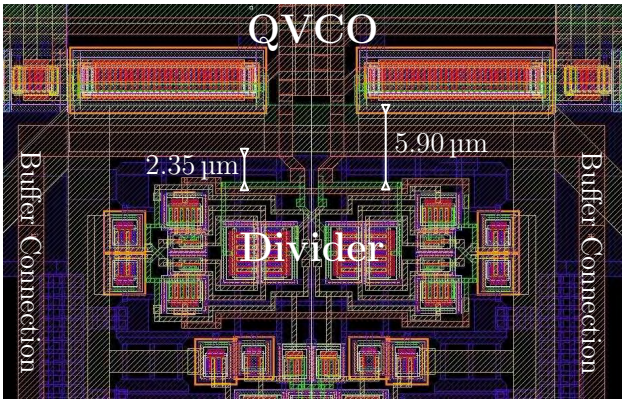


Figure 2.9: *Detailed layout of the interface between the QVCO and the frequency divider.*

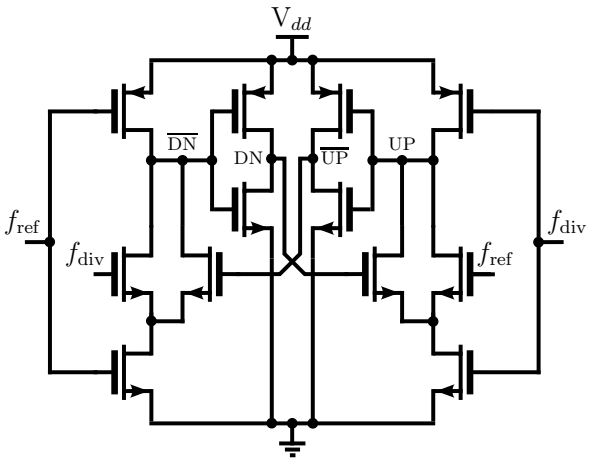
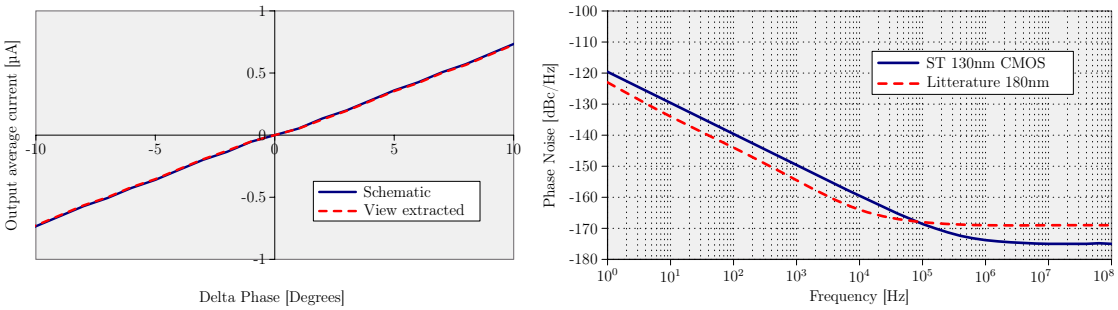


Figure 2.10: *Schematic of the designed PFD.*

2.3.5 Phase frequency detector

Figure 2.10 shows the schematic of the designed Falling-Edge (FE) PFD [25]. When input signals f_{ref} and f_{div} are low, UP and DN are low and $\overline{\text{UP}}$ and $\overline{\text{DN}}$ are in pre-charge mode. UP and DN go high only when both input signals are high and they go down only in correspondence to f_{div} and f_{ref} falling-edge, respectively. Phase difference is equal to the width difference between UP and DN signal. When locking condition has been reached, phase difference fall to zero and output signals width are the same. For this reason charge pump current should be matched as much as possible. Thanks to the absence of a reset signal, as more traditional PFD's often require, this configuration is dead zone free as demonstrates the simulated phase characteristic for small differents phase shift shows in figure 2.11b. This property leads to a better phase noise of the PLO.

It is worth noticing that the True Single Phase Clock (TSPC) solution is dead zone free as well, but its implementation requires more transistors than the FE solution [25]. As it combines good phase noise and compact layout, the FE solution has been adopted in the present work. Further advantages offered by this structure are low dissipated power and high speed operation. It is worth pointing out that for getting no dead zone and a



(a) (b)

Figure 2.11: *Simulated PFD phase characteristic for small differents phase shift (a) and PFD phase noise performance (b).*

good linearity of the phase characteristic, the FE PFD should compare signals exhibiting the same duty cycle with a value in the range of 50 % [25], which is the case of the PLO reported in the present chapter. Under these conditions, the simulated phase noise of the designed FE PFD, figure 2.11b is about −173.8 dBc/Hz at frequency offset of 1 MHz, outperforming the −168.8 dBc/Hz claimed in [25]. Moreover, it has to be pointed out that the PFD schematic depicted in figure 2.10 exhibits a differential structure. This topology not only makes the PFD robust against common mode noise sources but also provides up and down signals in both true and false forms, so that a differential CP can be driven.

2.3.6 Charge pump and Loop Filter

To optimize in-band phase noise performances, CP should be carefully designed. For this, a differential topology whit single ended output is selected for the CP, which is able to improve the common mode noise rejection [21]. The schematic of the designed CP is shown in figure 2.12. As previously highlighted, used PFD need good matched charge pump currents. Nonetheless, output node mismatch between NMOS and PMOS may cause mismatch current. To keep current mismatch as small as possible and hence keep small refernce spurs amplitude, following solutions have been observed. Keeping in mind the mobility difference between PMOS and NMOS, $M_{7,8}$ are sized for transistors

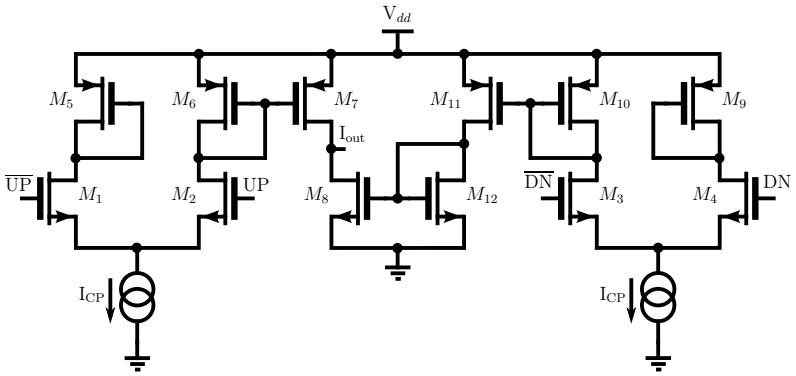


Figure 2.12: *Schematic of the designed CP.*

transconductance matching. Furthermore, $M_{7,8}$ output resistance r_{ds} should be as high as possible [12]. Longer devices and small charge pump current I_{CP} are therefore better.

Longer channel transistors are also used in the bias current mirrors to improve the current matching, as much as possible [26]. Finally, as known, the values of capacitance and resistance implemented in the loop filter (see figure 2.4) depend on the desired open loop gain. More precisely, as indicated in section 2.2 the capacitances are directly proportional to $K_\varphi \cdot K_{\mathrm{VCO}}/(\omega_{\mathrm{BW}})^2 \cdot N$, where K_φ is the gain of the CP, ω_{BW} the bandwidth of the PLO, and N is the division ratio of the frequency divider. Considering $K_\varphi = I_{CP}/2\pi$, values of the capacitances are also directly proportional to this current. Hence, the size of the loop filter is kept small by setting I_{CP} to 25 µA. Table II summarizes the transistor size of the designed CP. This low current value allows a second order loop filter to be designed on chip ($C_1 = 44\,\mathrm{pF}$, $R_1 = 27.09\,\mathrm{k\Omega}$ and $C_2 = 3.39\,\mathrm{pF}$). The resulting bandwidth and phase margin are 500 kHz and 60 degrees, respectively. To shrink the filter size as much as possible, polysilicon n-well capacitors are used for their higher capacitance-area ratio.

Transistors	W/L
M_{5-7} and M_{9-11}	12 µm/0.5 µm
$M_{1,2}$ and $M_{3,4}$	8 µm/0.13 µm
I_{CP} Current Mirror	12 µm/0.6 µm
$M_{8,12}$	8.3 µm/1.2 µm

Table II: *CP transistrors width.*

2.4 Simulated performances

Because of computation time, the simulation of the locking transient of the whole PLL was possible only at schematic level, that is in post-layout simulation were addressed.

As shown in figure 2.13, the QVCO control voltage V_{tune} reaches a steady value often about 5 µs, demonstrating that the PLO feedback loop properly works. A small periodic steady variation was observed, as highlighted in figure 2.13, which is due to the input reference. RCc simulations predict a −15 dBm buffer output tone on 50 Ω load, overall

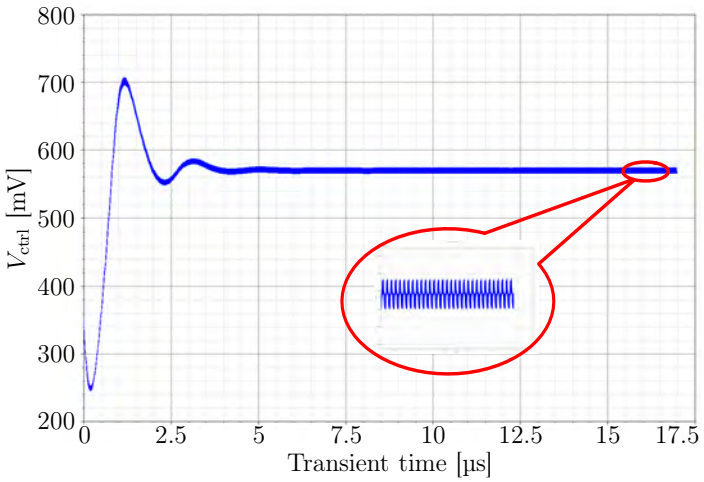


Figure 2.13: *Simulated transient PLO behavior.*

biased with about 86 mA. The PLO output signal picked out before buffers (charged on higher impedance) shows a great peak to peak sinusoidal amplitude of about 950 mV.
To perform a phase noise analysis with Cadence®, SpectreRF must first find a steady-state solution of the DUT (device under test) with PSS (Periodic Steady State) analysis. If the circuit has a periodic solution, then is possible perform a noise simulation. Nonetheless, the time t_c required to compute the noise depends on the number of circuit equations describing the DUT ($N_{\text{circuits\_ equations}}$) and on the numbers of time points needed to accurately render a single period of the solution ($N_{\text{time\_ point}}$), the latter when simulate a PLL with large division ratio could be too higher making simulation impossible in practice [11].

$$t_c \propto N_{\text{circuits\_equations}} \cdot N_{\text{time\_point}} \tag{2.24}$$

To walk around this problem, linear model based simulation tool described in [13] was used. The tool was developed using MATLAB® Graphical User Interface environment to build easier user interface and Simulink® models. The tool receives as input whole

loop characteristic (such as K_{VCO}, N, I_{CP}, B_W, PM and f_{REF}) and the phase noise contributions for each building block simulated as in PLO lock condition at transistor level. Using these input the tool computes both the open and closed loop responses together with the loop design specification, the zero-pole information, and the phase noise spectra as well [13]. Each simulated buildings box phase noise contribution is reported in figure 2.14, where the noise contribution of the reference signal is also reported (sky-blue curve), as well. From these results, the PFD/CP block can be identified as the main contributor to the PLO overall phase noise. Therefore, if the CP noise contribution will be drastically reduced, the overall PLO performances may respect the stringent DVB-S phase noise standard. This topic will be addressed in the experimental performances section 2.5.

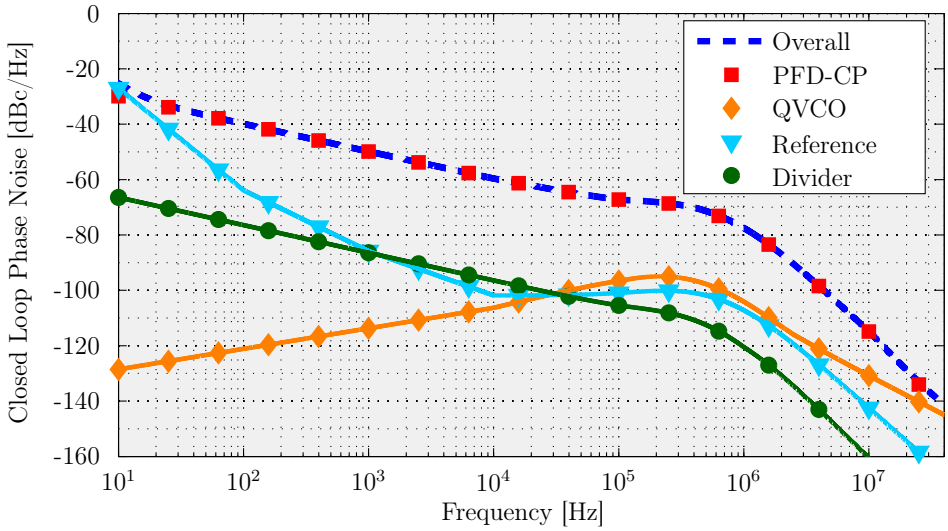
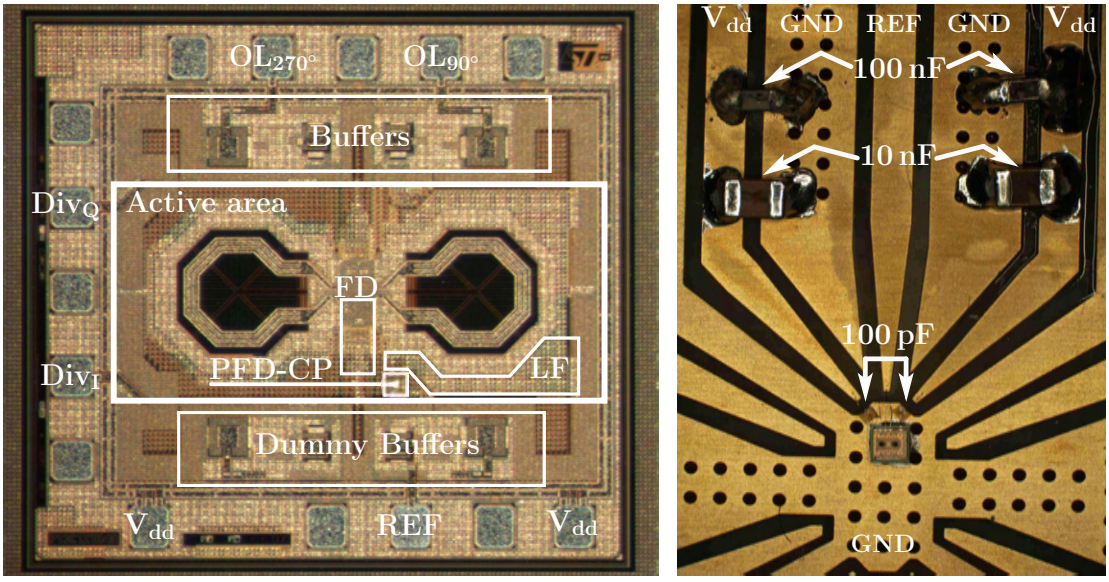


Figure 2.14: *Simulated closed loop phase noise contributions.*

2.5 Experimental performances

2.5.1 Measurements setup

Figure 2.15a shows the microphotograph of the fabricated prototype where each building block of the PLO is highlighted. Note the buffers driving the 50 Ω load of the external instruments in the higher chip side.The GSGSG pads for the differential RF output ($OL_{90°}$, $OL_{270°}$) are also visible on the top of the chip. To keep the circuit as symmetric as possible for the best balanced operation of the QVCO, two dummy buffers are connected on both other RF outputs. These outputs are not available over pads for experimental test simplification. Both pads on the left are implemented for the measurement of the frequency divider output signals (Div_Q et Div_I). On the bottom, pads are visible for the reference signal and power supply. The size of the whole chip is $920 \times 1010\,\mu m^2$, pad enclosed but the PLO active area without buffers is about $450 \times 900\,\mu m^2$, which is quite compact.



(a) (b)

Figure 2.15: *(a) Die microphotograph of the fabricated PLO, (b) test board detail with filtering capacitors highlighted*

For test simplification and quality purpose, the die is mounted on a PCB test board and bias pads as well as the reference low frequency pad are wire-bonded to interconnection lines. High frequency output signals are measured using coplanar micro-probes. Under these conditions, only one differential RF probe is required, and the bias can be correctly

filtered with 100 pF microcapacitors located as close as possible to the die and with several smd capacitors with higher capacitance values of 10 and 100 nF placed more distant as indicated in figure 2.15b. The bias voltage is supplied by a TTi Thurlby Thandar Instruments PL330 32V-3A Power Supply Unit. Finally, measurements are carried out inside a Faraday shielding, in order to minimize possible interferences with parasitic signals.

2.5.2 Results

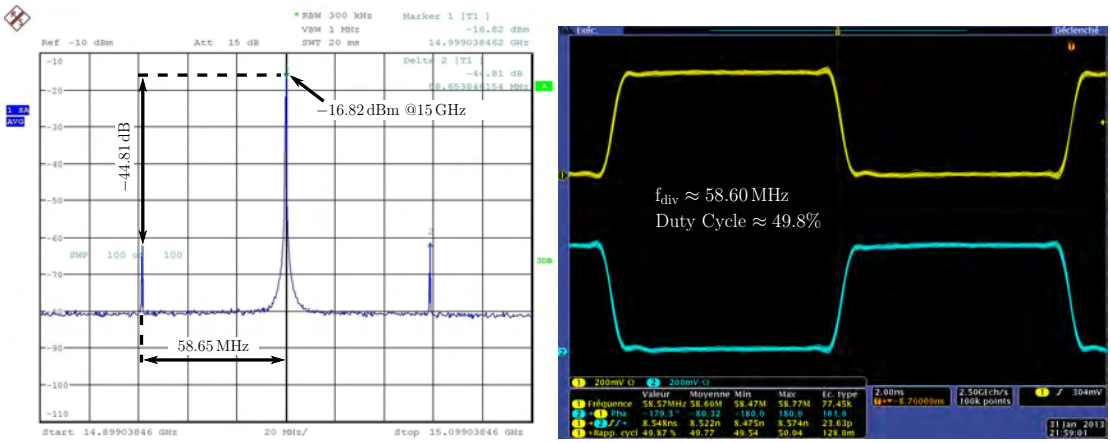
The differential output is applied to the single-ended input of the Rohde&Schwarz FSU67 Spectrum Analyzer by picking up only one signal and closing the other one on a 50 Ω load. The tuning external reference frequency is obtained from the Marconi instruments 2042 low noise signal generator (10kHz ÷ 5.4GHz). figure 3.4 shows the measured spectrum. By sweeping the external reference frequency, a range of $f_{carrier}$ from 14.2 GHz to 15.1 GHz is observed, which matches the expected tuning range.

The PLO delivers a power of about −16.8 dBm on a 50 Ω load, and it is biased under a current of 23.7 mA from 1.2 V supplied voltage (this bias is not taking into account buffers consumptions which simulated values have been removed from the overall bias of 92 mA). These results are not far from simulated performances reported in 2.4.

The frequency divider output was tested using Tektronix DPO4054 500 MHz 2.5 GS/s digital phosphor oscilloscope connected with Div_Q et Div_I. Using a 58.6 MHz reference frequency, square waves with about f_{div} of 58.6 MHz and 50% duty cycle have been measured as shown in figure 2.16b, proof that the frequency divider properly work. Unfortunately, quadrature information could not be obtained because of earlier phase information is lost through frequency divider chains.

Then, the phase noise is measured using the Agilent Technology signal source analyzer E5052B (10 MHz ÷ 7 GHz) associated with the microwave downconverter E5053A (3 GHz ÷ 26.5 GHz). Figure 2.17 shows the measured phase noise (red curve) for $f_{carrier} =$ 15 GHz into a span Δf from 10 Hz to 40 MHz. For example, the PLO exhibits a phase noise $L(\Delta f) = -86.3\,\text{dBc/Hz} \,@\, \Delta f = 1\,\text{MHz}$ and $L(\Delta f) = -122.2\,\text{dBc/Hz} \,@\, \Delta f = 10\,\text{MHz}$.

Figure 2.17 shows a very good agreement between measured (red curve) and simulated (dotted blue curve) phase noise, indicating that the phase noise simulation tool correctly works. It is here worth reminding that previous simulations (see section 2.4 gave evidence that the PFD and the CP are the main contributions to the phase noise of the whole PLL. Therefore, in order to discriminate between PFD and CP, the PFD phase noise performance has been investigated using the following Figure-of-Merit for PFD



(a) (b)

Figure 2.16: *Measured output spectrum (a) and Div_Q et Div_I frequency divider output (b)*

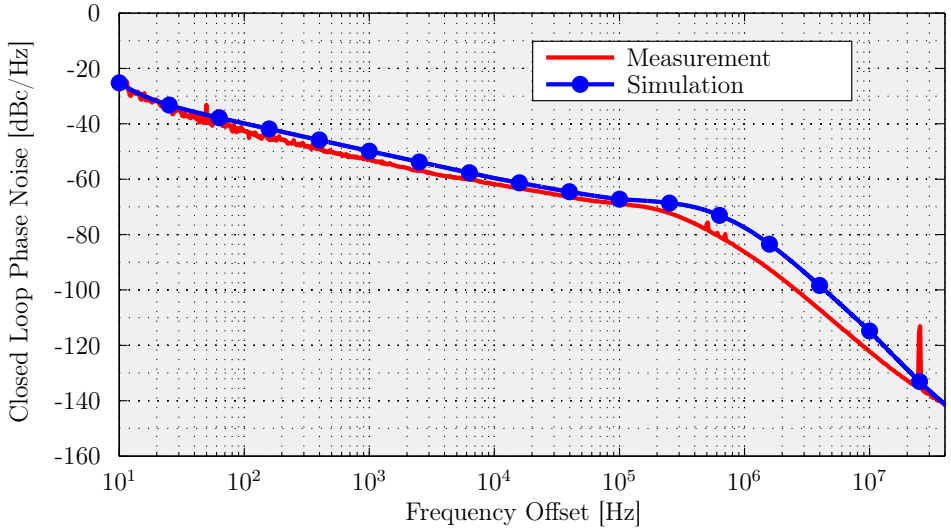


Figure 2.17: *Comparison between measured and simulated phase noise.*

(FOM_{PFD}) based on Barenjee model and reported in [27]:

$$FOM_{PFD}(dBc/Hz) = L(\Delta f) - 20\log_{10} N - 10\log_{10} f_s \tag{2.25}$$

where N is the division ratio of the frequency divider and f_s the external reference frequency. The computed FOM_{PFD} are listed in Table III. The FOM_{PFD} exhibited in the present work is only slightly higher than those claimed in the literature. This result suggests that the PFD is not the circuit to be deeply improved.

Therefore, using FOM_{PFD}, allows to find the circuit part that must to be enhanced, as

	Process	f_s [MHz]	N	Phase Noise [dBc/Hz]	FOM_{PFD} [dBc/Hz^2]
This Work	CMOS 130nm	58.6	256	-68.9@100kHz	-194.7
[28]	CMOS 130nm	1118.75	34	-85@100kHz	-205.9
[29]	CMOS 130nm	78	257	-77@100kHz	-204.1
[30]	CMOS 130nm	600	32	-85.6@100kHz	-203.5
[31]	CMOS 130nm	45.1	1024	-63@100kHz	-199.8
[32]	CMOS 65nm	18	1160	-55@50kHz	-188.8
[33]	CMOS 180nm	72	200	-73@100kHz	-197.6
[34]	SiGe:C BiCMOS	81.1	256	-68.66@100kHz	-
[35]	SiGe:C BiCMOS	250	63	-83@100kHz	-203

Table III: *In-Band performances comparison with other silicon-based PLL*

in our case confirm the previous suspects that indicate the CP. Then, further investigation on the CP phase noise is carried out. As indicated in [12], the phase noise contribution of the CP is referred to the PLL input by dividing the total average noise at the CP output by the gain K_φ of this device. The following simple phase noise expression can be derived:

$$\theta_n = 2\pi \sqrt{\left[\frac{2K\mu}{L^2\, f\, I_{CP}} + 4kT\left(\frac{2}{3}\right)\sqrt{\frac{2\mu\, C_{OX} W}{I_{CP}^3\, L}}\right] \cdot \left(\frac{t_{CP}}{T_0}\right)} \tag{2.26}$$

where K is a proportionality constant depending on the process, L is the channel length of the CP's transistors, μ is the channel electron mobility and t_{CP} is the time both current sources of the charge pump are on during each period T_0. Equation (2.26) indicates that, even if a low maximum value of the CP current I_{CP} allows lower total average noise, as reported in [21], for lower phase noise a higher I_{CP} value is better [12].

As an illustration, Figure 2.18 compares two phase noise spectra simulated for the previous I_{CP} value of 25 µA and for a higher value of 300 µA. These spectra are then compared with the DVB-S standard phase noise limits (red symbols) [6]. A phase noise reduction of about 20 dB is observable, demonstrating the importance of the CP contribution to the overall PLO phase noise. Moreover, Figure 2.18 points out that the higher value $I_{CP} = 300$ µA allows keeping the phase noise fair close to limits set by the DVBS standard. In particular, the PLO phase noise is better than the standard close to the carrier for offset frequency lower than 10 kHz, and away from carrier for offset frequency higher than 1 MHz. In the 10 kHz÷1 MHz offset frequency range, the obtained phase noise is fairly comparable with the standard. As already pointed out, since the

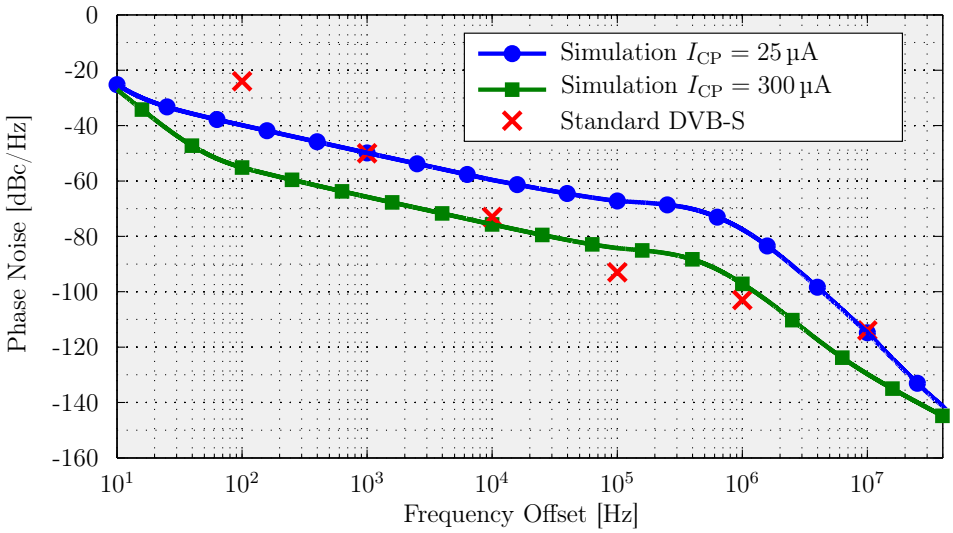


Figure 2.18: *Comparison between the simulated phase noise with* 25 µA *and* 300 µA *charge pump current; red symbols are DVB-S standard phase noise limits.*

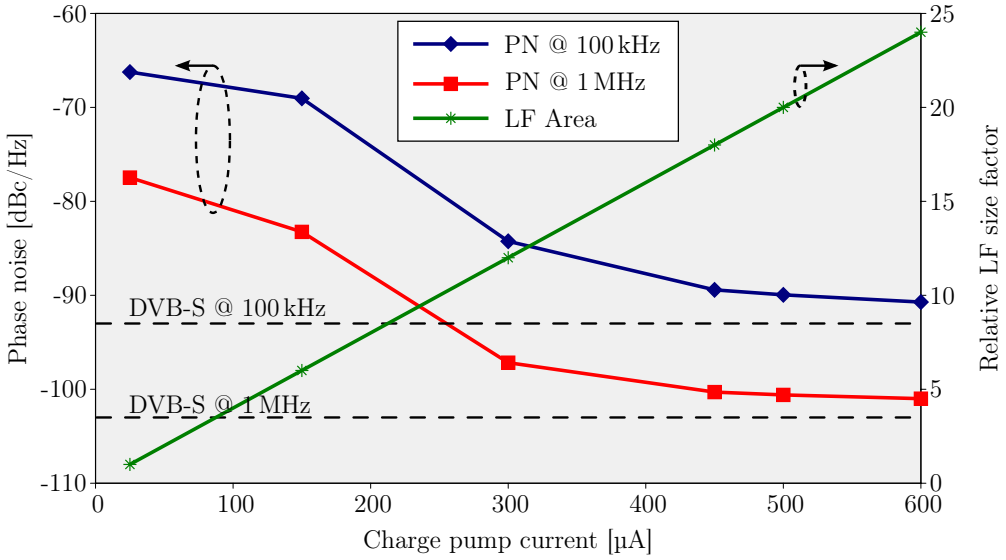


Figure 2.19: *Charge pump current effects on phase noise performances reported with LF relative size*

capacitances are directly proportional to the gain of the charge pump, a trade-off between the loop filter size and the phase noise performance must be found. In particular, a $I_{CP} = 300\,\mu A$ would require to increase by a factor of about twelve ($C_1 = 527.7\,pF$, $R_1 = 2.25\,k\Omega$ and $C_2 = 40.82\,pfarad$) the value of the capacitances. For instance, the loop filter of the measured prototype (figure 2.15a) occupies an area of about $15\,800\,\mu m^2$

($0.016\,\mathrm{mm}^2$); whereas for $I_{CP} = 300\,\mu\mathrm{A}$, the occupied area of this filter increases to about $189\,200\,\mu\mathrm{m}^2$ ($0.189\,\mathrm{mm}^2$). As indicated in figure 2.19, increasing more charge pump current value, phase noise performance keep improving until about $I_{CP} = 450\,\mu\mathrm{A}$ at only 2 dB of the DVB-S standard. Furthers charge pump current augmentation does not allow essential performances improvements.

	This Work 1	This Work 2	[28]	[29]	[30]
Process	CMOS 130 nm	CMOS 130 nm	CMOS 130 nm	CMOS 130 nm	CMOS 130 nm
Frequency [GHz]	15	15	38	20.05	19.2
Freq. Range [GHz]	14.2 ÷ 15.1	14.2 ÷ 15.1	37 ÷ 38.5	20.05 ÷ 21	17.6 ÷ 19.4
Supply [V]	1.2	1.2	1.2	1.5	1.3÷1.5
Power [mW]	28.43*	28.43*	51.6*	22.5	480.4
Chip Area [mm^2]	0.45 × 0.9*	0.45 × 1.3*	1.5 × 1.1	0.6 × 1	1.7
Phase Noise [dBc/Hz]	-68.9@100kHz -86.28@1MHz -122.3@10MHz	-84.3@100kHz -97.17@1MHz -129.7@10MHz	-85@100kHz -97.5@1MHz	-77@100kHz -98.5@1MHz -116.1@10MHz	-84@100kHz -101.2@1MHz -113.5@10MHz
Ref. Frequency	58.6 MHz	58.6 MHz	1.1875 GHz	78 MHz	600 MHz
Bandwidth [Hz]	500k	500k	15.625M	400k	≈4M
Filter/ Division_Ratio	Integrated/Fixed	Integrated/Fixed	Integrated/Fixed	Integrated/Progr	Integrated/Fixed
I_{CP} [µA]	25	300	250	70	-
Reported jitter rms [ps]	-	-	0.24	-	0.65
Calculated jitter rms [ps] (Integration Range)	3.31 (10kHz÷40MHz)	0.64** (10kHz÷40MHz)	0.36 (10kHz÷40MHz)	0.67 (50kHz÷40MHz)	0.78 (10kHz÷40MHz)
FOM [27]	-215.1	-229.3**	-235.3	-230	-216.9
	[31]	[32]	[33]	[34]	[35]
Process	CMOS 130 nm	CMOS 65 nm	CMOS 180 nm	SiGe:C BiCMOS 0.13 µm	SiGe:C BiCMOS 0.25 µm
Frequency [GHz]	46.2	20.88	15	20.76	15.75
Freq. Range [GHz]	45.9 ÷ 50.5	19.44 ÷ 21.6	13.9 ÷ 15.6	20.51 ÷ 21.27	14.25 ÷ 15.75
Supply [V]	1.5	1.2 ÷ 1.8	1.8	1.5	2.5÷1.5
Power [mW]	57, 45.8*	80	70	40	288
Chip Area [mm^2]	1.16 × 0.75	1.6 × 1.9	1	0.84 × 0.57	0.7 × 0.8
Phase Noise [dBc/Hz]	-63@100kHz -72@1MHz -99@10MHz	-65@100kHz -100@1MHz -126@10MHz	-73@100kHz -103.8@1MHz	-68.66@100kHz -97.17@1MHz	-68.66@100kHz -97.17@1MHz
Ref. Frequency	600 MHz	36 MHz	71 MHz	81.1 MHz	250 MHz
Bandwidth [Hz]	500k	≈70k	200k	-	≈3MHz
Filter/ Division_Ratio	Integrated/Fixed	External/Progr	Integrated/Progr	Integrated/Fixed	Integrated/Progr
I_{CP} [µA]	-	-	600	100	-
Reported jitter rms [ps]	-	-	-	-	-
Calculated jitter rms [ps] (Integration Range)	2.57 (2kHz÷20MHz)	4.14 (10kHz÷40MHz)	1.56 (10kHz÷40MHz)	-	1.44 (10kHz÷40MHz)
FOM [27]	-214.5	-208.6	-216.7	-	-212.3

** Without buffers implemented for characterization purpose*
*** With $I_{CP} = 300\,\mu\mathrm{A}$*

Table IV: *Performances comparison summary with other silicon-based PLL.*

For an evaluation of this work, the proposed PLO is compared with other silicon-based PLL already reported in the literature. The comparison is carried out by using the following Figure-of-Merit [27]:

$$FOM_{PLL}(dB) = 10\log_{10}\left[\left(\frac{\sigma_{t,PLL}}{1s}\right)^2 \cdot \left(\frac{P_{DC}}{1mW}\right)\right] \tag{2.27}$$

where $\sigma_{t,PLL}$ is the RMS jitter and P_{DC} is the DC power consumption. When only the phase noise spectrum is reported, a short script, developed in Matlab code, computes

the jitter through the following formula [27]:

$$\sigma^2_{t,PLL} = \frac{1}{2\pi^2 f^2_{carrier}} \int_0^{\infty} L_{PLL}(\Delta f) d\Delta f \cong \frac{1}{2\pi^2 f^2_{carrier}} \int_W L_{PLL}(\Delta f) d\Delta f \qquad (2.28)$$

where L_{PLL} is the phase noise of the PLL and W is the finite offset frequency integration range. The used value of W for each reference is listed in Table IV. In the limits of the data available in each reference, efforts are made to keep W as uniform as possible (about $10\,\text{kHz} \div 40\,\text{MHz}$ frequency range), in order to get a homogeneous comparison. figure 2.20 shows the computed results where each reference is related at the DC Power consuming and jitter variance. The FoM of the proposed PLO is well located in the comparison with the literature, since it is close to $-215\,\text{dB}$ in the case of a $I_{CP} = 25\,\mu\text{A}$ and falls down to about $-230\,\text{dB}$ in the case of a $I_{CP} = 300\,\mu\text{A}$. figure 2.20 shows also the jitter variance limit (red line) calculated with equation (2.28) using the phase noise limit of the DVBS standard, which is previously reported in figure 2.18. One can see that the presented PLO comes closer to the two best performances [28], [29] and it is close to the DVBS jitter limit when an increase of the loop filter occupied silicon space is acceptable, in relation to the increase of the charge pump current.

A more detailed performances comparison is summarized in Table IV. Note the low power consumption of the PLO described in the present chapter when the buffer contribution is neglected; its 28mW are challenged only by the PLL reported in [29] and several times lower, between two and sixteen times, the power dissipated by the other PLL's. This result in addition with the small silicon occupied area give to the proposed PLO a large interest in the case of mobile and/or energy self-sustaining applications where the dissipated power should be kept as low as possible.

2.6 Conclusions

This chapter reports on the design of a low-power integer-N PLO fabricated in a low cost 130 nm CMOS technology. The proposed PLO operates in the Ku-band, generating an output tone in the $14.16 \div 15.12\,\text{GHz}$ frequency range. The power delivered to a $50\,\Omega$ load is about $-16.8\,\text{dBm}$ and the phase noise is $-86.3\,\text{dBc/Hz}$ for an offset frequency of 1 MHz and of $-122.2\,\text{dBc/Hz}$ for an offset frequency of 10 MHz. The PLO sinks 23.7 mA from 1.2 V supply. The discussion of the experimental data points out that the charge pump is the main responsible for the measured phase noise level. Once compared in terms of jitter with other silicon-based PLO's and PLL's reported in the literature, the

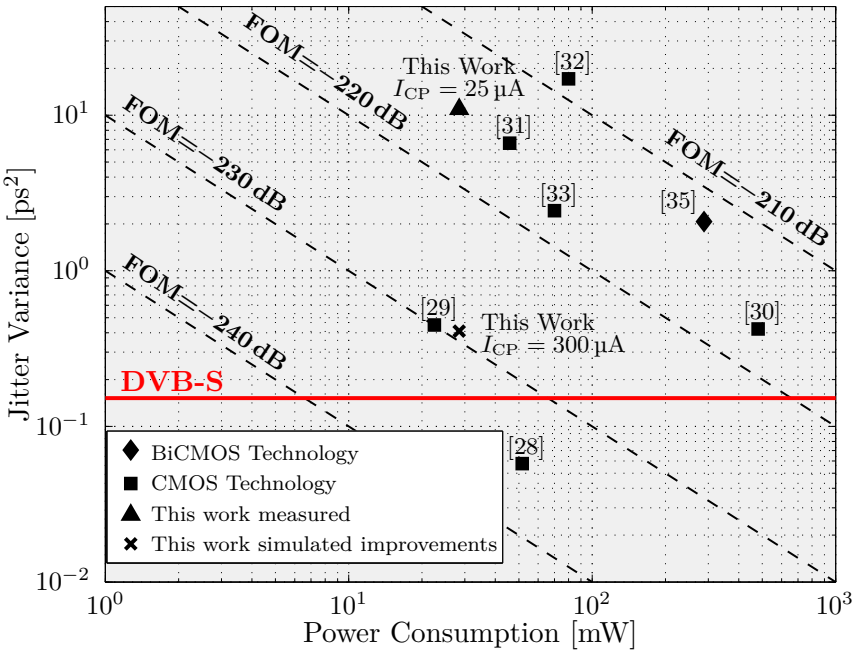


Figure 2.20: *Jitter and power comparison between the PLO reported in this work and others PLL reported in the literature in term of FOM_{PLL}.*

PLO of this work is well aligned if the charge pump current is set to a value that keeps the loop filter integration. For higher charge pump current the PLO performs better than a large number of the other PLO's and PLL's, even if this high level of performances goes with an increase of the loop filter silicon area. These results demonstrate that a low-cost 130 nm CMOS technology is very promising for DVBS, where only discrete components or SiGe technologies have been employed until now. On the other hand, the reported prototype opens also the way to the fabrication of the front-end of a Ku-band microwave radiometer. For this application, the interest of the proposed PLO comes from the large reduction of the antenna size with respect to X-band radiometer, because of the higher operation frequency. In addition, its low dissipated power makes the proposed PLO up-and-coming for use in a smart sensor network for the detection of wild fire in outdoor environment. In this case, the low DC consumption is very welcome to supply the electronics with a small dimension energy harvester.

K-band Fundamental Sampling Mixer

3

3.1 Introduction

The main purpose of a receiver is to recover the transmitted signal from an often jammed noisy RF spectrum. This situation results in stringent constraints on the overall noise figure, gain and linearity of such component straightly relied to the performance level of the whole wireless system. In such receiver, the down-conversion mixer may impact the overall receiver's performances, especially at very high frequencies, because of the limited gain values of the preceding LNA. Active mixers (e.g. Gilbert's Cell and its derivatives) are often employed since they usually provide some gain and are known to require a low power level as local oscillator (LO) signal. However, linearity and noise performances are averages. On the other hand, passive mixers are preferred in zero-IF receiver architectures thanks to the absence of flicker noise. They also provide very good linearity and low intermodulation, but suffer from conversion losses. More recently, passive mixers pumped by a 25 % duty-cycle square LO signal have been introduced [36]. This technique cancels out the crosstalk usually observed in IQ receivers driven by 50 % duty-cycle LO signal and increases the overall receiver's gain by at least 3 dB [37, 38]. Additionally, the resistive mixer operates as a sampler and the conversion losses are almost entirely cancelled theoretically when used in a voltage-driven configuration [39]. However, this solution appears to be frequency-limited because of the circuits involved in the generation of such low duty-cycle LO signal since they cannot be pushed beyond few GHz [40, 41].

The work presented in this chapter proposes to extend the frequency-range of such architecture by at least one decade, up to 27 GHz. After a short introduction on the application of sampling theory to perform frequency conversion, an analytical model of a double-balanced sampling mixer is described. Thanks to this model, the main factors limiting the frequency of operation of the mixer are identified and used to specify the LO signal waveform.

These constraints are taken into account in the design an original circuit, which might be described as a pulse shaper. The circuit is fully described in section 3.5.

Finally, a sampling mixer is designed and presented. Simulations and measured results are given in Section 3.6.

3.2 The frequency translation using sampling theory

As known, a mixer performs the frequency shifting operation by multiplying two signal. The mixing operation can be obtained by either device nonlinearities or using quasi-linear perfect multipliers (e.g. Gilbert-cell with LO and RF voltages amplitudes lower than U_t).

Another way to perform frequency mixing is to take advantage of sampling theory to design a sampling mixer [42]. The circuit is built with a switch (MOS device) loaded by a capacitor and operates as a sample-and-hold circuit (see figure 3.1).

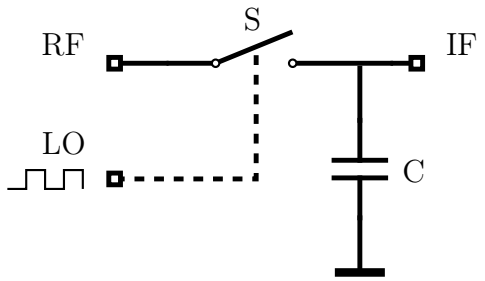


Figure 3.1: *Simplified model of sampling mixer.*

The IF voltage $v_{\text{if}}(t)$ is determined by convolving the sampled RF voltage $v_{\text{rf}}(t)$ with rectangle function $\Pi(\frac{t}{T_{\text{LO}}} - \frac{1}{2})$:

$$v_{\text{if}}(t) = \left[v_{\text{rf}}(t) \cdot \sum_{n=-\infty}^{+\infty} \delta(t - nT_{\text{LO}}) \right] * \Pi(\frac{t}{T_{\text{LO}}} - \frac{1}{2}) \tag{3.1}$$

The Fourier transformation of 3.1 gives the spectrum of $V_{\text{if}}(f)$:

$$V_{\text{if}}(f) = sinc(\pi\, fT_{\text{LO}}) \cdot \sum_{n=-\infty}^{+\infty} V_{\text{rf}} \left(f - \frac{n}{T_{\text{LO}}} \right) \cdot e^{-j\pi fT_{\text{LO}}} \tag{3.2}$$

The spectrum of the IF voltage is periodic. It exhibits a *sinc* trend as depicted in figure 3.2 where the zeros of the function are placed at every n/T_{LO} multiples. Mixing operation occurs and the RF spectrum is duplicate at IF frequency and also around the zero of the sinc.

This basic theory helps to understand how it is possible to perform frequency mixing signal using an ideal switch.

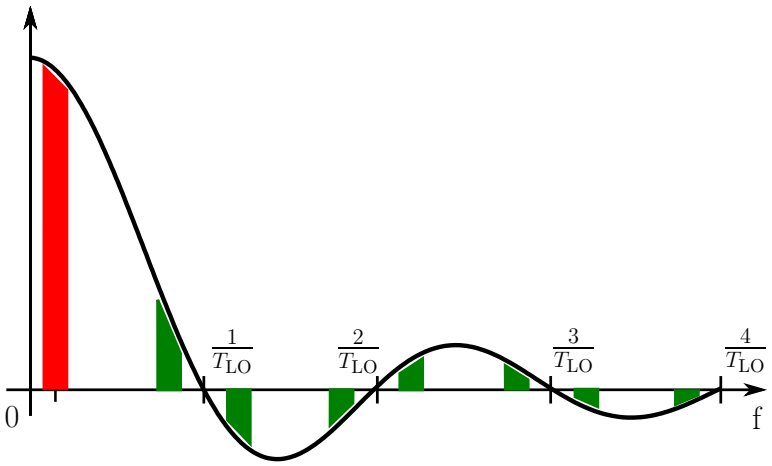


Figure 3.2: *Spectrum of the IF voltage.*

However, the sampling mixing operation also depends on LO signal characteristics such as amplitude, duty-cycle and transition times. A more elaborated model is developed in the following section to take these contributions into account and hence establish the design constraints of the following pulse generator.

3.3 Analytical modeling of sampling mixer

The ring mixer structure is constituted by four NMOS transistors connected as shown in figure 3.3. A differential LO signal, identified with LO and $\overline{\text{LO}}$ labels respectively, is applied to the gates of each transistor pairs $M_1 - M_3$ and $M_2 - M_4$. The differential RF signal enters the circuit by the drains of each transistor while IF is collected between each pair of sources by an IF amplifier.

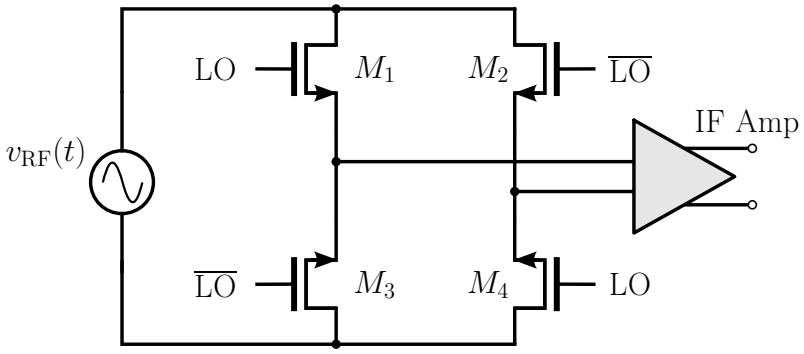


Figure 3.3: *Schematic of a ring mixer.*

To perform the conversion gain calculation, this mixer is reduced to the circuit network shown in figure 3.4a. Each transistors pair of the mixer is modeled by a time-varying drain-source conductance $g(t)$ and $g\left(t - T_{\mathrm{LO}}/2\right)$ driven by LO and $\overline{\mathrm{LO}}$ voltage respectively. The input of the IF amplifier is modeled by a capacitor named c_L.

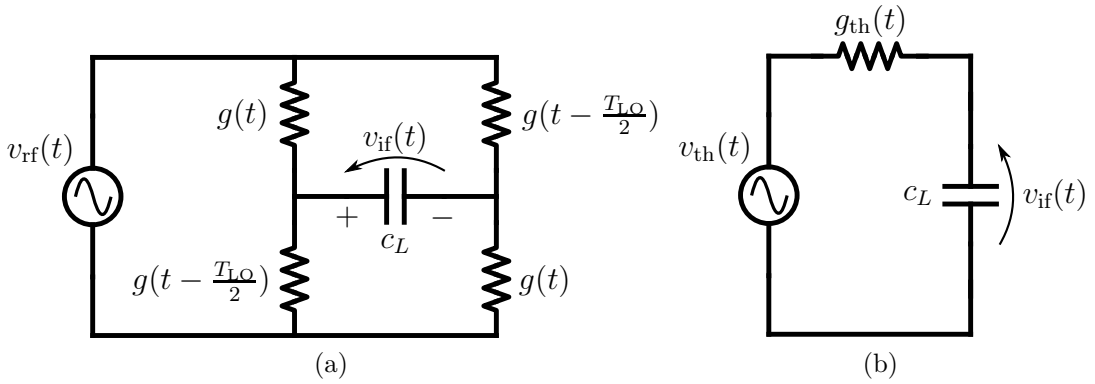


Figure 3.4: *Equivalent schematic of the mixer (a) and its Thévenin representation from IF balanced output (b).*

3.3.1 Simplified electrical network derivation

The following analysis employs analytical developments similar to [43]. But unlike this reference, the drain-source time-varying conductances are assumed to swing between two finite limits $1/r_{ON}$ and $1/r_{OFF}$, defining the ratio $\gamma = r_{\mathrm{OFF}}/r_{\mathrm{ON}}$. Finite and equals rise and fall times are also accounted through the parameter τ_r. These parameters depend on LO voltage amplitude along with gate-source DC voltage bias. Starting with these assumptions, the variations over time of conductances $g(t)$ and $g\left(t - T_{\mathrm{LO}}/2\right)$ are illustrated in figure 3.5 from low duty-cycle LO and $\overline{\mathrm{LO}}$ voltages.

From the balanced IF output point of view, the network of the figure 3.4a can be simplified into a Thévenin equivalent generator. The result of this transformation is shown in figure 3.4b with an open voltage $v_{\mathrm{th}}(t)$ and an equivalent conductance $g_{\mathrm{th}}(t)$ both expressed as:

$$v_{\mathrm{th}}(t) = v_{\mathrm{rf}}(t) \cdot \frac{g(t) - g\left(t - \frac{T_{\mathrm{LO}}}{2}\right)}{g(t) + g\left(t - \frac{T_{\mathrm{LO}}}{2}\right)} = v_{\mathrm{rf}}(t) \cdot m(t) \tag{3.3}$$

$$g_{\mathrm{th}}(t) = g(t)//g\left(t - \frac{T_{\mathrm{LO}}}{2}\right) = \frac{g(t) + g\left(t - \frac{T_{\mathrm{LO}}}{2}\right)}{2} \tag{3.4}$$

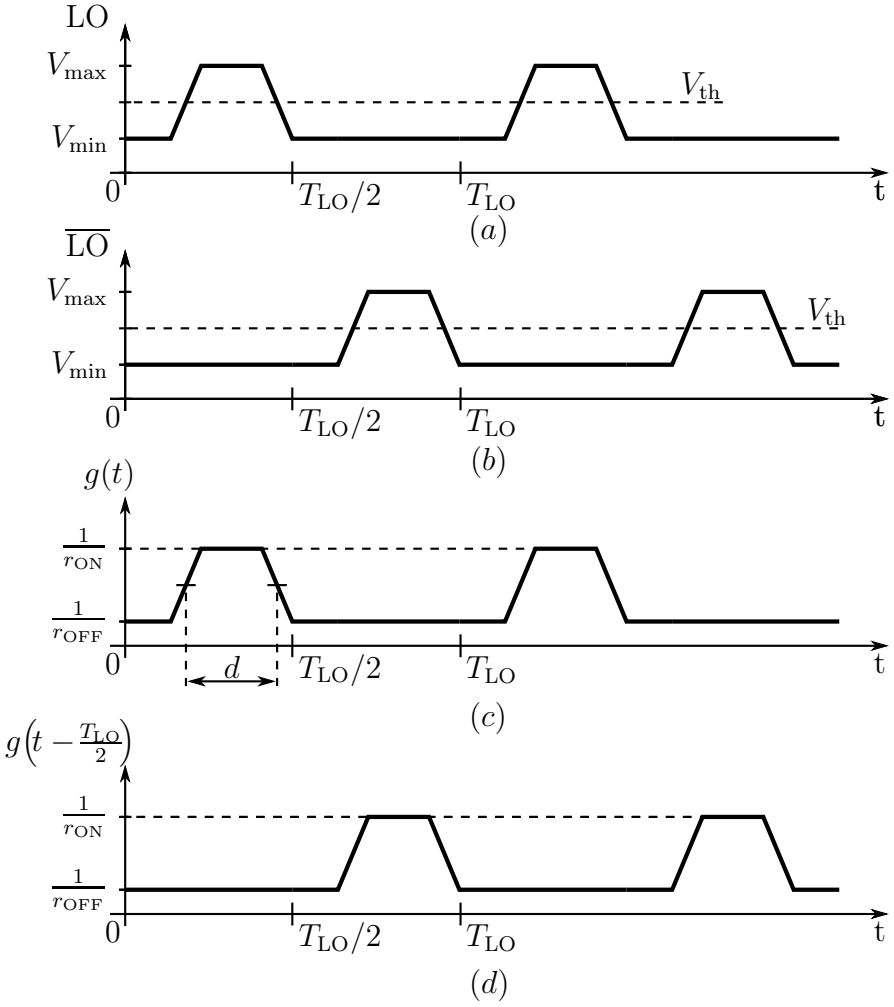


Figure 3.5: *Waveform of the driven voltage signals LO and $\overline{LO}$ (a),(b) and the relative conductances variation.*

This simplification defines a mixing function $m(t)$ and the Thévenin conductance $g_{\mathrm{th}}(t)$, whose variations over time are plotted in figure 3.6. The peak conductance $g_{\mathrm{th}_{\mathrm{max}}}$ and the mean value $g_{\mathrm{th}_{\mathrm{max}}}$ of $g_{\mathrm{th}}(t)$ are also derived and expressed by:

$$g_{\mathrm{th}_{\mathrm{max}}} = max\left(\frac{g(t) + g\left(t - \frac{T_{\mathrm{LO}}}{2}\right)}{2}\right) \tag{3.5}$$

$$\overline{g_{\mathrm{th}}} = \frac{1}{T_{\mathrm{LO}}} \int_0^{T_{\mathrm{LO}}} g_{\mathrm{th}}(t)\, dt \tag{3.6}$$

$$= \frac{d\,(r_{\mathrm{OFF}} - r_{\mathrm{ON}}) + r_{\mathrm{ON}}}{r_{\mathrm{OFF}} r_{\mathrm{ON}}} \tag{3.7}$$

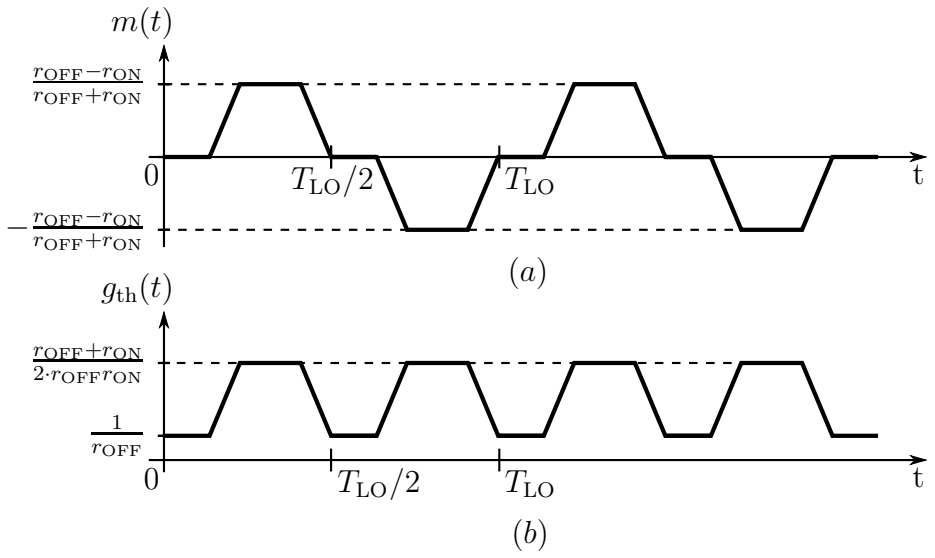


Figure 3.6: *Waveforms of mixing function $m(t)$ (a), and Thévenin conductance $g_{th}(t)$ (b).*

3.3.2 Time-domain analytic conversion gain calculation

Starting from this representation of the mixer, it is demonstrated in [43] that the circuit can be cut out in several cascaded transfer functions as illustrated in figure 3.7. The input RF voltage $v_{rf}(t)$ is multiplied by a function $m^{'}(t)$, amplified by a factor A, and filtered by a single-pole low-pass filter. $m^{'}(t)$ and A are derived from previous calculations and are defined as follows:

$$m^{'}(t) = \frac{g_{\mathrm{th}}(t)}{g_{\mathrm{th}_{\mathrm{max}}}} m(t) \tag{3.8}$$

$$A = \frac{g_{\mathrm{th}_{\mathrm{max}}}}{\overline{g_{\mathrm{th}}}} \tag{3.9}$$

A conversion gain function $G_C(t)$ is then defined in the following relation (3.10). Its transient variation exhibits a trapezoidal waveform as shown in figure 3.8.

$$G_C(t) = \frac{g_{\mathrm{th}}(t)}{\overline{g_{\mathrm{th}}}} \cdot m(t) = \frac{g(t) - g\left(t - \frac{T_{\mathrm{LO}}}{2}\right)}{2\,\overline{g_{\mathrm{th}}}} \tag{3.10}$$

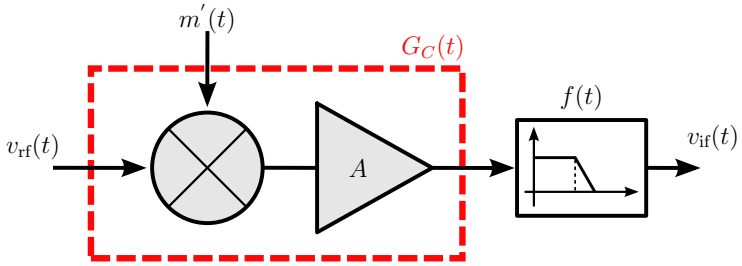


Figure 3.7: *Equivalent block diagram of the sampling mixer for conversion gain calculation*

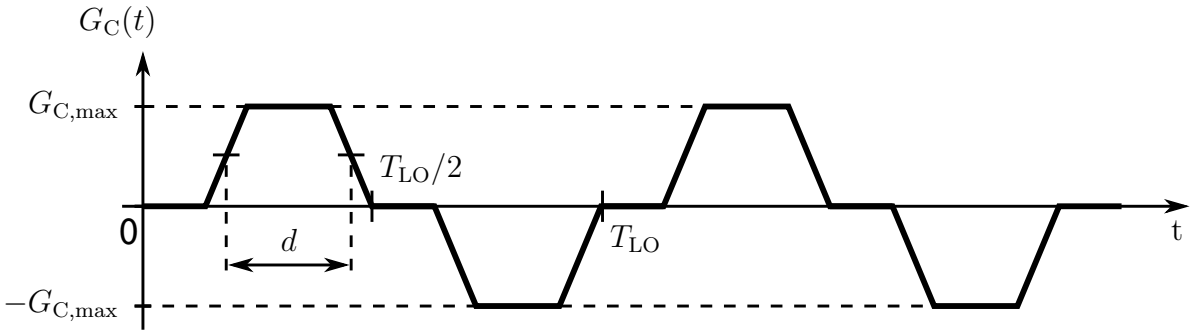


Figure 3.8: *Conversion gain function waveform.*

3.3.3 Discussion on the low-pass filter

The low-pass behavior of the mixer is due to the capacitive input impedance of the amplifier connected at the IF terminal. This equivalent capacitor c_L is essential to let the mixer operate as a sample-and-hold circuit. The cut-off frequency of this filter is ω_c, expressed in (3.11).

$$\omega_c = \frac{\overline{g_{\text{th}}}}{c_L} \tag{3.11}$$

Its value has to be very carefully chosen. ω_c must be much lower than $2\omega_{\text{LO}}$, as demonstrated in [43]. But it also must be higher than ω_{IF} to avoid any filtering effect on the IF signal. Both limitations lead to the following inequality:

$$\omega_{\text{IF}} << \frac{\overline{g_{\text{th}}}}{c_L} << 2\omega_{\text{LO}} \tag{3.12}$$

In other words, c_L must remain within a limited range of values illustrated by the following graph (figure 3.9) to avoid unnecessary extra losses on mixer's conversion gain.

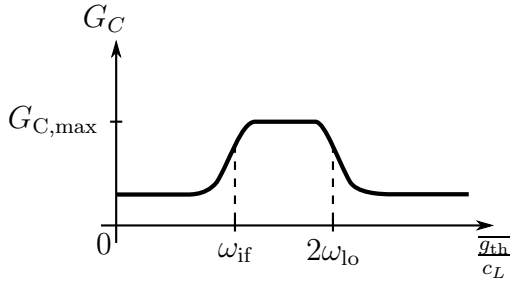


Figure 3.9: *Condition on c_L to optimize conversion gain.*

3.3.4 Frequency-related analytic conversion gain derivation

It is now easy to derive the frequency-related analytic conversion gain from the time-domain expression (3.10) using Fourier transformation. The full calculation is given in appendix A but the main result is reported as follows:

$$\mathcal{F}\left(G_C(t)\right) = G_{\mathrm{C,max}} \cdot sinc\left(\pi\tau_r f_{\mathrm{RF}}\right) sinc\left(\pi\frac{f_{\mathrm{RF}}}{f_{\mathrm{LO}}}\gamma\right)\left(1 - e^{-j\pi\frac{f_{\mathrm{RF}}}{f_{\mathrm{LO}}}}\right) \tag{3.13}$$

In this expression, $G_{\mathrm{C,max}}$ depends on r_{ON}, r_{OFF} and the duty-cycle d. Its expression is calculated as detailed below:

$$G_{\mathrm{C,max}} = max\left(\frac{g(t) - g\left(t - \frac{T_{\mathrm{LO}}}{2}\right)}{2\,\overline{g}_{\mathrm{th}}}\right) \tag{3.14}$$

$$= \frac{r_{\mathrm{OFF}} - r_{\mathrm{ON}}}{2 \cdot \left[d\left(r_{\mathrm{OFF}} - r_{\mathrm{ON}}\right) + r_{\mathrm{ON}}\right]} \tag{3.15}$$

The conversion gain is finally deduced from (3.13) using (3.15) and becomes:

$$G_{c1}(\gamma, d) = \frac{(\gamma - 1)\,d}{2\left[d\left(\gamma - 1\right) + 1\right]} \cdot sinc\left(\pi\tau_r f_{\mathrm{RF}}\right) sinc\left(\pi\frac{f_{\mathrm{RF}}}{f_{\mathrm{LO}}}d\right)\left(1 - e^{-j\pi\frac{f_{\mathrm{RF}}}{f_{\mathrm{LO}}}}\right) \tag{3.16}$$

However, this relation is only valid if the condition $d \geq \tau_r$ is respected. If $0 < d < \tau_r$, the conversion gain vanishes as channel conductance is no longer able to reach the maximal $1/r_{ON}$ value. In this range, the conductance variation behavior over time follows a triangle shape leading to another expression of the conversion gain summarized

below and developed in appendix A:

$$G_{c2}(\gamma, d) = \frac{(\gamma - 1)}{2\left[d\left(\gamma - 1\right) + 1\right]} \cdot \left(\frac{d^2}{\tau_r f_{\mathrm{LO}}}\right) \cdot sinc^2\left(\pi d \frac{f_{\mathrm{RF}}}{f_{\mathrm{LO}}}\right) \left(1 - e^{-j\pi \frac{f_{\mathrm{RF}}}{f_{\mathrm{LO}}}}\right) \tag{3.17}$$

3.3.5 Discussion on sampling mixer's conversion gain

Using expressions (3.16) and (3.17), it is now possible to plot the conversion gain for any duty-cycle comprised between 0 and 0.5. Based on data found in the literature [44], γ ratios have been deliberately chosen in the range 0 to 100. A fixed value of 5 ps for τ_r is also chosen to keep calculations within realistic ranges further observed by electrical simulations and presented later in this chapter. A first example calculated for $f_{\mathrm{LO}} = 19\,\mathrm{GHz}$ and $f_{\mathrm{RF}} = 20\,\mathrm{GHz}$ is plotted in figure 3.10. This graph shows that conversion losses lower than 2.1 dB are reached among duty-cycle values ranging from 12 % to 29 % and γ ratios exceeding 40. This result is in line with what was expected from such mixer topology.

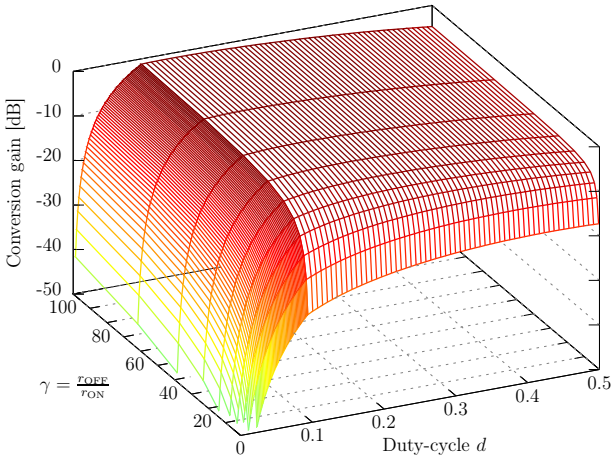


Figure 3.10: *Conversion gain with* $f_{LO} = 19\,\mathrm{GHz}$, $f_{RF} = 20\,\mathrm{GHz}$

The $sinc(x)$ function within (3.16) also suggests that the conversion gain may be canceled at RF frequencies around $2f_{LO} \pm f_{IF}$. On the contrary, the mixer might be able to downconvert RF frequencies around $3f_{LO} \pm f_{IF}$ with moderate losses. Both assumptions are verified by the model using the aforementioned LO frequency of 19 GHz but with RF frequencies of 39 GHz and 58 GHz. These results are displayed in figures 3.11a and 3.11b respectively. At an RF frequency of 39 GHz, the conversion gain is always lower than $-23\,\mathrm{dB}$ regardless γ and d values. On the contrary, conversion gains going up

to −5 dB are predicted by the model using duty-cyle from 5 % to 22 % when frequency of the RF signal is centered around the third harmonic of LO frequency. However, practical implementation of such mixer will induce stringent constraints on the duty-cycle of LO pulsed signal since conversion gain vanishes as duty-cycle tends toward values around 33 % and because the best conversion gain is obtained at a d of 10 %, a quite hard-to-reach value especially when the fundamental frequency increases beyond tens of GHz.

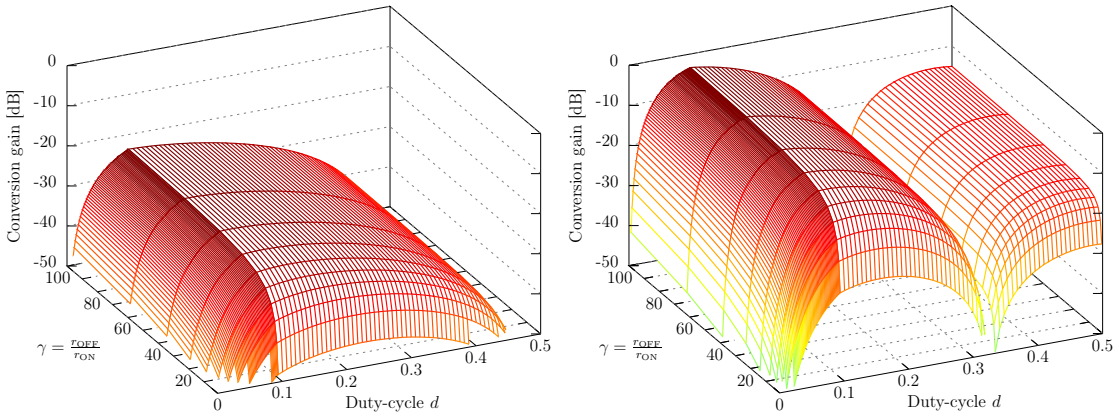


Figure 3.11: *Calculated conversion gain with* $f_{RF} = 39$ GHz *in (a) and* 58 GHz *in (b).* $f_{LO} =$ 19 GHz.

The best possible conversion gain can be reached by setting τ_r to zero with an infinite γ. The expression (3.17) then simplifies as

$$G_{c3} = \frac{1}{2} \cdot sinc\left(\pi \frac{f_{\mathrm{RF}}}{f_{\mathrm{LO}}} d\right) \left(1 - e^{-j\pi \frac{f_{\mathrm{RF}}}{f_{\mathrm{LO}}}}\right) \tag{3.18}$$

The maximum conversion gain of the fundamental sampling mixer is plotted in figure 3.12 with $0 < d < 0.5$. Its value can reach 0 dB at a zero duty-cycle but this limit is impractical because of the finite values taken by τ_r (figure 3.12.a) and γ (figure 3.12.b). These graphs show that τ_r must be lower than 7 ps at 19 GHz. The optimal duty-cycle is 16 % with a γ of 60. One must note that the very well-known conversion losses of $2/\pi$ (~ 4 dB) is found at a 50% duty-cycle with this analytic model.

The maximum conversion gain of the sub-sampling mixer is plotted in figure 3.13 with $0 < d < 0.5$. The condition on τ_r is now more stringent than previous configuration since the optimal duty-cycle is 8 % with the same γ of 60.

This section has investigated the development of an analytic model for a sampling

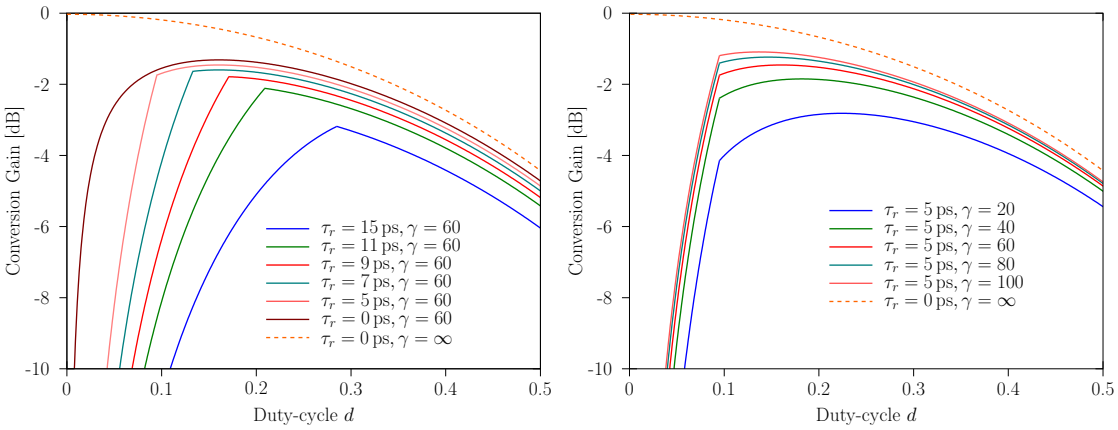


Figure 3.12: *Estimated conversion gains by the model in "normal condition" ($f_{LO} = 19\,\text{GHz}$, $f_{RF} = 20\,\text{GHz}$) with: (a) different τ_r values fixing $\gamma = 60$ and (b) different γ values fixing $\tau_r = 5\,\text{ps}$.*

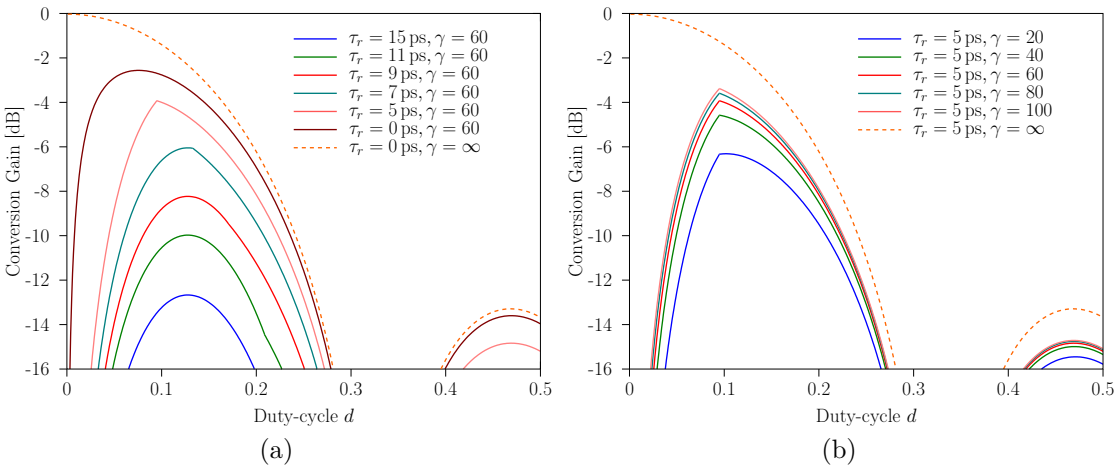


Figure 3.13: *Estimated conversion gains by the model in "sub-harmonic condition" ($f_{LO} = 19\,\text{GHz}$, $f_{RF} = 58\,\text{GHz}$) with: (a) different τ_r values fixing $\gamma = 60$ and (b) different γ values fixing $\tau_r = 5\,\text{ps}$.*

mixer based on a double-balanced passive topology involving NMOS devices. The goal was to predict the behavior of the circuit at RF frequencies around LO frequency and its harmonics. Two efficient operating conditions have been highlighted using RF frequencies around $f_{LO} \pm f_{IF}$ and $3f_{LO} \pm f_{IF}$. The conditions on τ and γ have been defined to optimize the conversion gain in both configurations. These conditions will serve as starting points for the design of a pulse-shaping circuit described in the next part of this work.

3.4 K-band pulse shaping circuit

The previous section has highlighted the importance attached to the LO voltage duty-cycle d as well as the ratio γ of time-varying conductances in maximizing the conversion gain of a sampling mixer. It must be recalled that γ depends on LO voltage amplitude and the higher the LO voltage amplitude, the greater is the challenge for transition time τ_r minimization. It has been shown that the generated pulses should have an amplitude able to provide γ ratios higher than 40, duty-cycle values comprised between 20 and 25 % and an estimated rise-fall time lower than 7 ps.

The previous model does not clarifies its dependence over LO voltage amplitude since only γ is used. Because the channel of the NMOS becomes capacitive when turned in its OFF state, γ appears as a frequency-dependent dynamic parameter. It is then difficult to define a rigorous relationship between γ, the amplitude of the LO voltage and V_{th}. Electrical simulations are preferred in such conditions. A 19 GHz LO voltage with a duty-cycle of 25 % has been applied to a ring mixer loaded by an optimal capacitor regarding the IF frequency of 1 GHz. The RF frequency has been set to 20 GHz.The simulation results are presented in figure 3.14 using three different minimum LO voltage levels from 100 mV to 200 mV under V_{th}. Conversion gain is plotted at LO voltage amplitudes in the range 150-500 mV. These data demonstrate that the minimum voltage amplitude to consider is 400 mV to obtain conversion losses better than 2.3 dB. This value has been used in the following analysis.

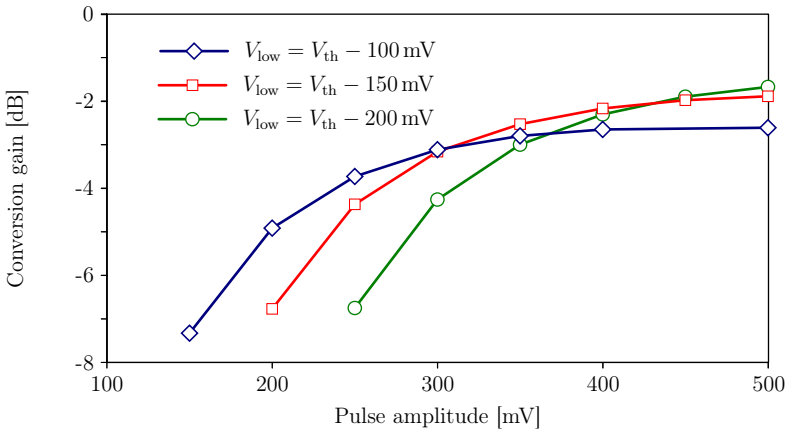


Figure 3.14: *Different conversion gain obtained by different* 25 % *LO square wave voltage amplitude.*

3.4.1 Pulse generators in the literature

Pulse generators are widely employed in several circuits such as sampling mixer or impulse-based Ultra Wide Band (UWB) transceiver. Impulse-radio UWB often employ Gaussian pulse generators [45, 46]. These circuits employ very different topoloies using combinational logic blocks, or fully analog circuits. They often exhibit amplitude levels going up to 600 mV but with a pulse repetition frequency always far lower than 1 GHz making them unsuitable for our application.

25% duty-cycle pulsed voltage generators are also widely used to drive sampling mixers [37] or passive mixers [47–49]. All these published works implement logic-based circuit topologies involving several logic latches and gates. For example, [46] employs an inverting delay line and a NOR gate to generate narrow pulses. Inverters and AND gates are used in [47]. The major issue of such circuit topologies is that they cannot be pushed beyond few GHz. The highest operating frequency has been spotted at 5 GHz in [40]. Since an operating frequency higher than 20 GHz is targetted here, logic-based circuits are really unpractical using actual CMOS technologies. Even very fast ECL logic circuits will lead to insufficient voltage levels and cannot be considered as well. The only remaining solution is to consider fully analog circuits. Rather than creating a pulse, the solution proposed bellow is to implement a system capable of transforming a sinusoidal voltage to a voltage pulse.

3.4.2 A pulse-shaping circuit based on Class-C technique

The schematic of the pulse shaper is shown in Fig.3.15. Heterojunction bipolar transistors (HBT) have been preferred instead of NMOS devices thanks to their much higher f_t. It is worth noticing that a device with higher f_t frequency means that the device presents both lower parasitic capacitances and time delays.

A class-C low conduction-angle amplifier has been chosen to create current pulses from the sinusoïdal input voltage V_{in}. The principle of operation of such circuit is illustrated in figure 3.17. Q_1 is used in a common-emitter (CE) configuration and is responsible of the current pulse generation. A common-base (CB) is added to reduce the transition time, increase the gain and the bandwidth of the cascode circuit formed by both transistors Q_1 and Q_2. Thanks to this circuit, the sinusoïdal input voltage V_{in} is translated into an high-amplitude low-duty-cycle current at the collector of Q_2 as seen in figure 3.17(b). This current produces an high-amplitude high-duty cycle voltage across the L_1R_1 network (figure 3.17c). The DC voltage signal V_{ctrl} drives the conduction angle of Q_1 and subsequently on pulse width, transition times, and amplitude. The

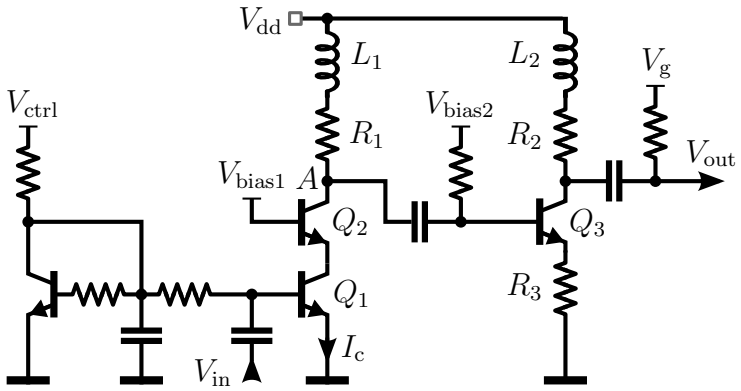


Figure 3.15: *Schematic of the pulse shaper.*

inductor added to the load L_1 provide some peaking and resonate with parasitic output capacitances helping to reduce transition times of the pulsed current. The effect of L_1 on the output voltage of the first stage V_A is shown in figure 3.16. The best compromise was found with values in the range 130-200 pH. In this range, the amplitude is improved with no increase in the duty-cycle. Placing this inductance in series with R_1 makes less sensitive the circuit to inductance variations. A value of 165 pH has been chosen for L_1.

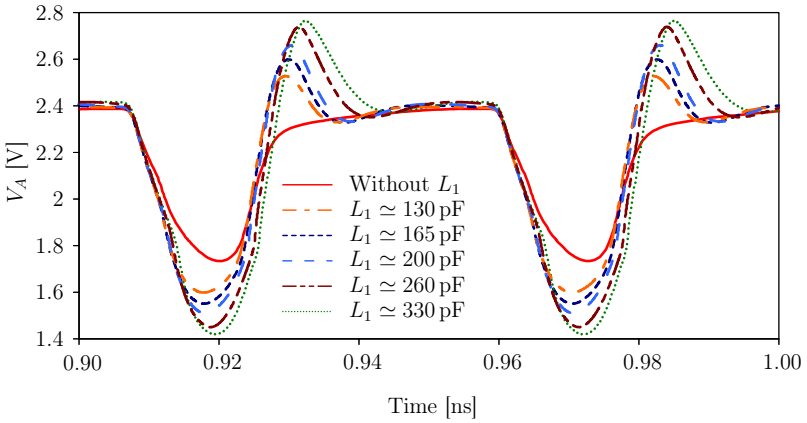


Figure 3.16: *Simulated waveform at the class-C output with different L_1 values comparison.*

3.4.3 Class-A inverting amplifier

The first stage creates a reversed voltage pulse which is placed in the right direction by the second stage. This part of the pulse shaping circuit employs an ultra-wideband degenerated common-emitter amplifier featuring nearby unity gain. This stage must be able to handle up to $1V_{pp}$ amplitude without saturating. The linearity, bandwidth and

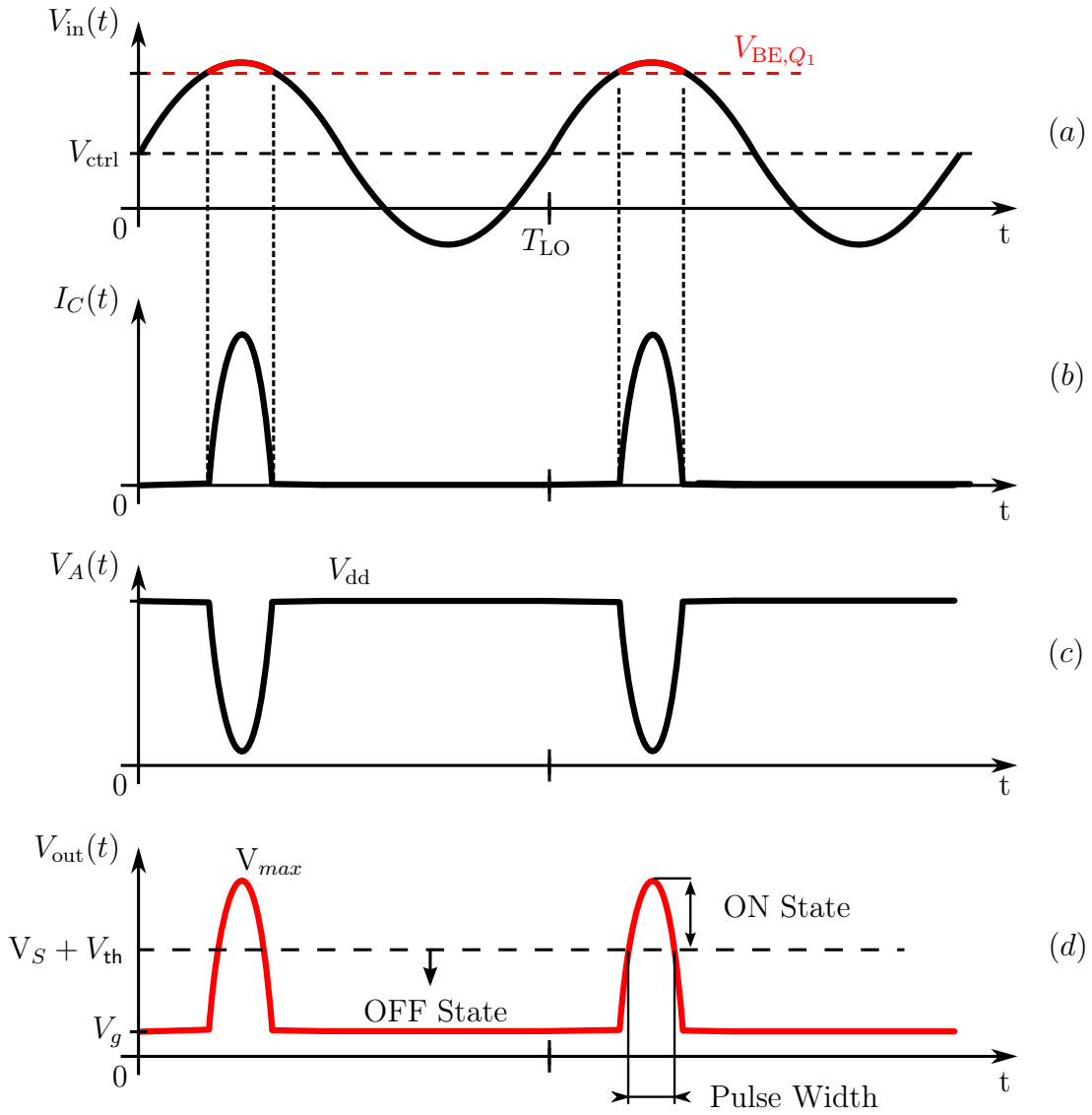


Figure 3.17: *Pulse waveforms in different points of the pulse shaper: sinusoïdal input voltage (a), class-C current (b), output voltage (c), and output class-A voltage (d).*

gain are adjusted by using the degeneration resistance R_3. The bandwidth was of major concern since all harmonics of the pulsed signal need to be reversed to keep the sharp rise and fall times of the incoming signal. Q_3 is biased at the optimal collector current (around 14 mA) to provide the required bandwidth. This solution was preferred against cascode topology because of linearity requirements. Finally, the inductor L_2 placed after R_2 improves the bandwidth by about 28 GHz as shown in figure 3.18.

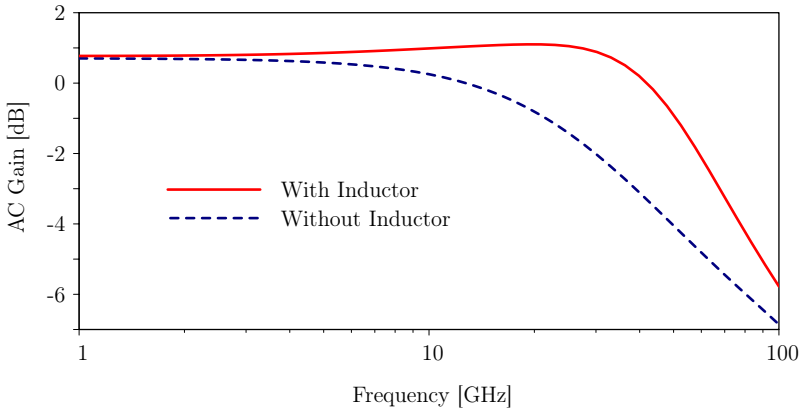


Figure 3.18: *Simulated AC gain of Class-A amplifier.*

3.4.4 Layout considerations and final simulations

The layout of the circuit is reported in figure 3.19. The contribution of interconnects parasitics is considered using 3D electromagnetic simulations (EM) because parasitic extraction tools are not reliable at very high frequencies since inductive contribution is neglicted. Both inductors L_1 and L_2 are also modeled through EM simulations to benefit from their accuracy.

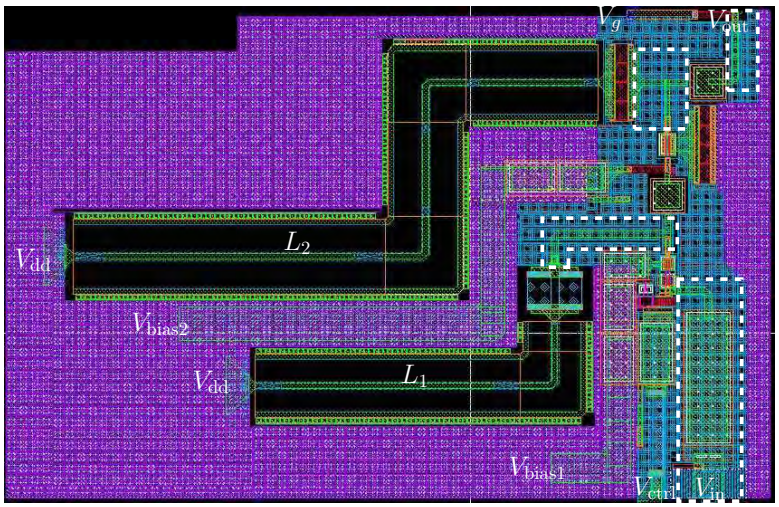


Figure 3.19: *Pulse shaper layout.*

The post-layout simulated output waveform is plotted at 19 GHz in figure 3.20 with and without inductors L_1 and L_2 to highlight their benefits. The displayed voltage is characterized by a duty-cycle of 22 % and a peak-to-peak amplitude of 560 mV. The pulse

waveform can be approximated by a trapezoidal waveform also represented in figure 3.20, defined with a τ_r of 5 ps which has been used into the model reported in section 3.3.

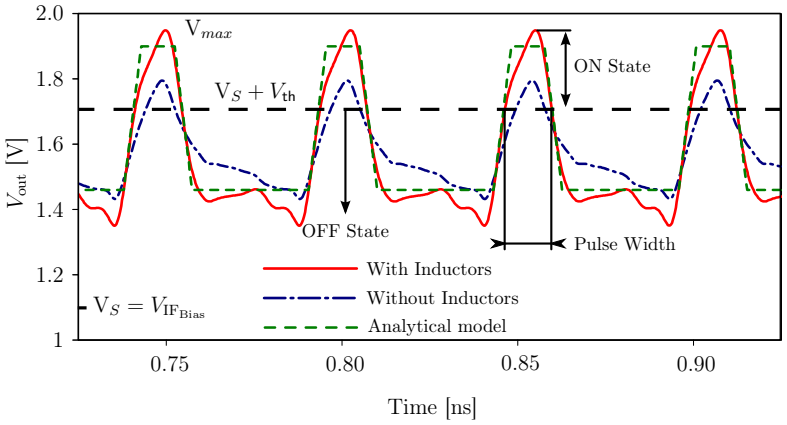


Figure 3.20: *Simulated output waveform of the pulse shaper at* 19 GHz.

The circuit draws 45 mW from a supply voltage of 2.4 V. 5 mA is sank in class-C pulse shaper and 14 mA by the class-A. The consumption is somewhat high, but it wasn't of concern. There is a large room for improvements, by using better bias strategies, changing active device sizes, finding better compromises, improving the layout footprint, etc. However, all these results indicate that a sampling mixer may be able to perform very well at 19 GHz.

Finally, the figure 3.21 represents a Monte Carlo analysis of the peak-to-peak amplitude regarding process and mismatch variations within active and passive devices. This simulation has been performed for 100 samples at a constant temperature of 27 °C. This graph shows a peak voltage around 550 mV with more than 70 % of samples included in a range from 480 to 620 mV. This result is satisfying and demonstrates the robustness of the design.

Since this pulse shaper has been designed to drive the capacitive impedance of the gate of MOS transistors, the circuit hasn't been tested stand-alone. It's experimental evaluation has been performed indirectly through the mixer characterization described in section 3.6.

3.5 Description of the fundamental sampling mixer

To design the frequency converter, the pulse shaper described in the previous paragraph is associated with a ring mixer. Two copies of this circuit are required. A balanced amplifier is connected at the IF outputs of the ring mixer. This circuit brings the

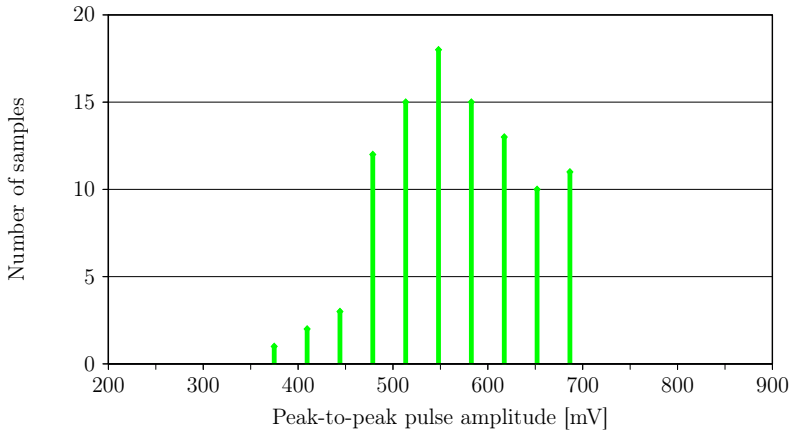


Figure 3.21: *Monte Carlo simulations representing Peak-to-peak amplitude for 100 samples.*

capacitive impedance c_L mentioned in the theoretical study in section 3.2. Such an input impedance is crucial for the proper functioning of the whole down-converter. An arbitrary IF frequency of 1 GHz is chosen. No amplifier is added before the mixer to avoid limiting the RF bandwidth by this amplifier. In doing so, the RF bandwidth of the down-converter is set by the pulse generators, which is precisely what we are looking after. The block diagram of the chip is depicted in figure 3.22.

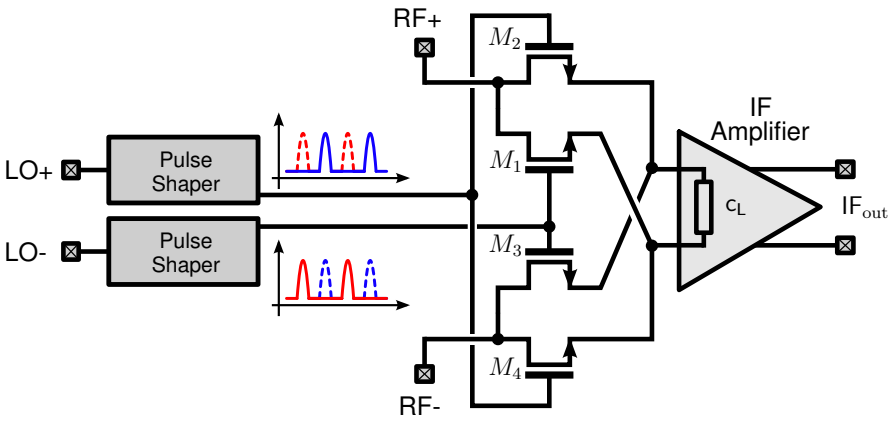


Figure 3.22: *Block diagram of the fundamental sampling mixer.*

3.5.1 Mixing device sizing optimization

The mixer employs the well known ring topology (see figure 3.22). It involves four NMOS devices biased at $V_{DS} = 0V$ to provide a time-varying conductance between drain and source, driven by the voltage applied between gate and source. Since device geometry

strongly affects the mixer performances in terms of conversion gain and linearity, the number of gate fingers, the length and width must be chosen very carefully. The mixing devices geometry also influences the transition times of the pulsed LO voltage due to the overall capacitor brought between gates connections of the ring mixer.

Several electrical simulations were performed on the ring mixer driven by pulse shapers to determine the geometry leading to the best performances and/or compromise. The smallest NMOS length of 120 nm is used to minimize the gate capacitor and to avoid penalizing the linearity [50]. Twelve gate fingers are also used to minimize the gate extrinsic resistance. The mixer linearity and conversion gain are plotted in figure 3.23 for various NMOS widths between 6 and 200 µm. These results demonstrate that conversion gain and linearity cannot be optimized together using the same device. A compromise has to be found and a NMOS size of $36 \times 0.12\mu m^2$ is chosen. With this device, the linearity picked at the mixer's output reach −3.8 dBm and conversion losses are about 2.2 dB. Since the mixer is based on voltage sampling, the linearity expressed in dBm is obtained from the IF output voltage assuming an ideal unity-gain differential buffer loaded by 50 Ω at each output.

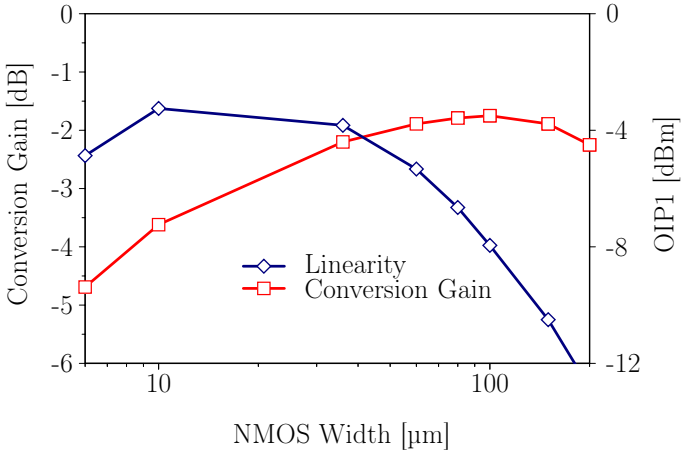


Figure 3.23: *Conversion gain and linearity variations of the ring mixer versus NMOS widths.*

3.5.2 IF Amplifier

This circuit employs a schematic developed in a previous project, given in figure 3.24. The bias current of the input differential pair is adjusted to provide a sufficiently high input impedance (1 kΩ) with the correct capacitance at 1 GHz to fit mixer's requirements. The differential pair is followed by two collector-coupled buffers to lower the output impedance without degrading the voltage gain of the first stage. Due to tight time constraints, we

have not adjusted the linearity of the circuit. The measurements presented in the next section highlight the lack of linearity of this circuit, preventing us from knowing the true measured linearity of the mixer. The simulated voltage gain of this circuits is 15.3 dB

The DC bias voltage present at both input terminals is 1.9 V. This voltage is also applied to the sources of the mixing devices. A bias tee has been added at the output of the pulse shaper (see figure 3.15) to provide the required DC voltage V_g at the gates of the mixing devices.

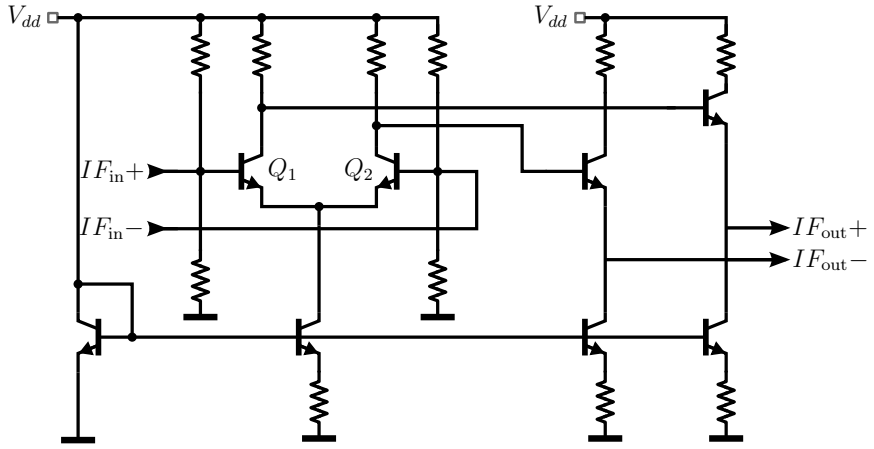


Figure 3.24: *Schematic of the IF amplifier.*

3.6 Experimental results

The circuit has been processed using a 0.13 µm BiCMOS SiGe technology from IBM. The die photograph is shown in figure 3.25, where each building blocks of the downconverter are highlighted. The GSGSG RF input pads are placed in the left of the chip while LO and IF terminals are at the bottom and the right of the chip respectively. Each block is fed with separate supply voltages to monitor the power consumption of the different parts of the chip. The dimensions are $1.2 \times 2.4\ mm^2$ including pads. The whole chip is biased under 2.4 V and consumes about 109 mW, split into 87 mW for both pulse shapers and 22 mW for the IF amplifier.

3.6.1 Description of the test-bench

A test-bench presented in figure 3.26 has been assembled to measure conversion gain, 1 dB compression point and noise figure (NF). The chip is characterized using RF-probes at RF and IF ports. The IF balanced output is attached to an external 180° hybrid coupler

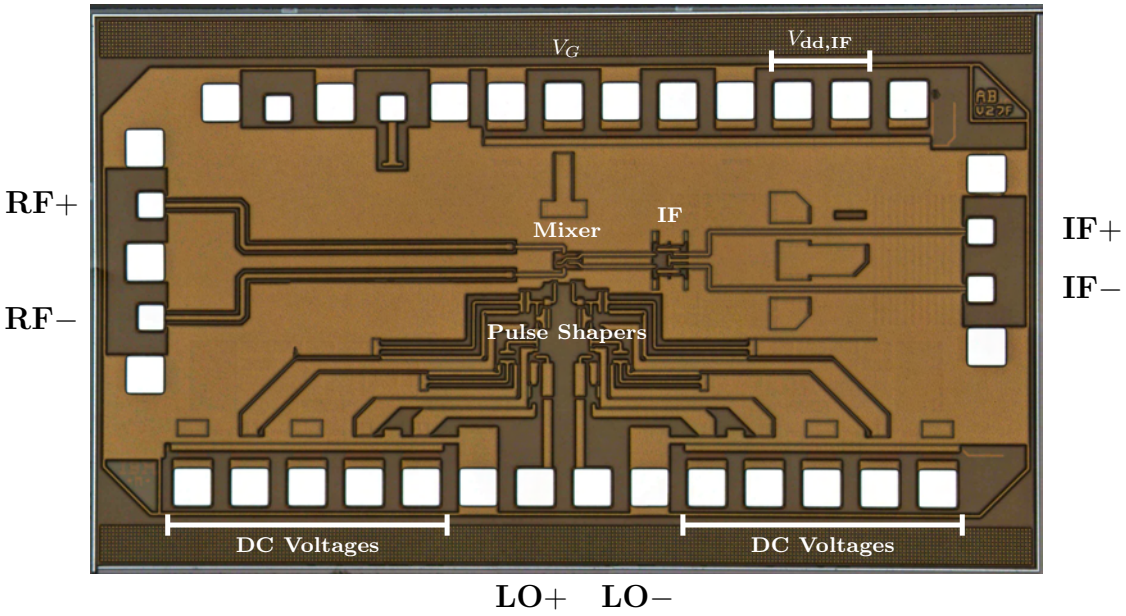


Figure 3.25: *Die micro-photograph of the fabricated down-converter.*

through a GSSG RF-probe. An Agilent Vector Network Analyser PNA-X N5247A is connected at the RF terminals of the chip. This equipment contains two RF internal sources which can be synchronized in phase and amplitude. This ability has been employed to deliver a perfectly differential RF signal to the corresponding pads of the chip. This solution is far more flexible, accurate and broadband than using an external balun since an RF balanced signal covering the full range of the PNA-X starting from 10 MHz to 67 GHz can be synthesized.

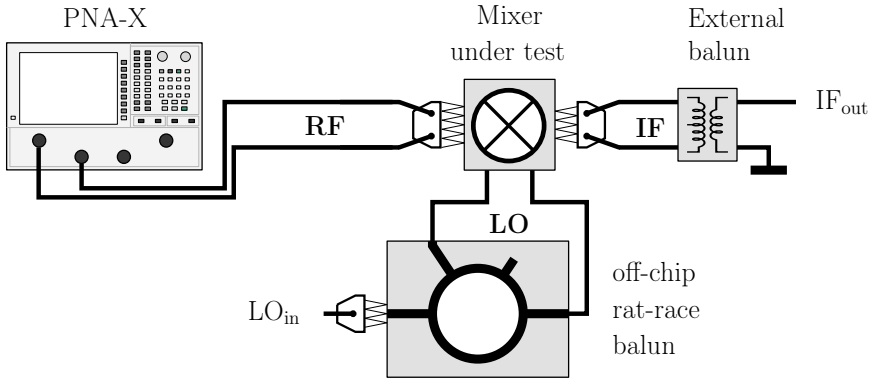


Figure 3.26: *Test-bench used for mixer characterization*

Finally, a rat-race balun fed by a GSG RF-probe provides the required balanced

LO signal to the chip. It has been designed over alumina and optimized for a center frequency of about 19 GHz and is detailed in the following subsection 3.6.2. All cables, RF-probes and external baluns are de-embedded to shift the RF and IF measurement reference planes to the pads of the chip.

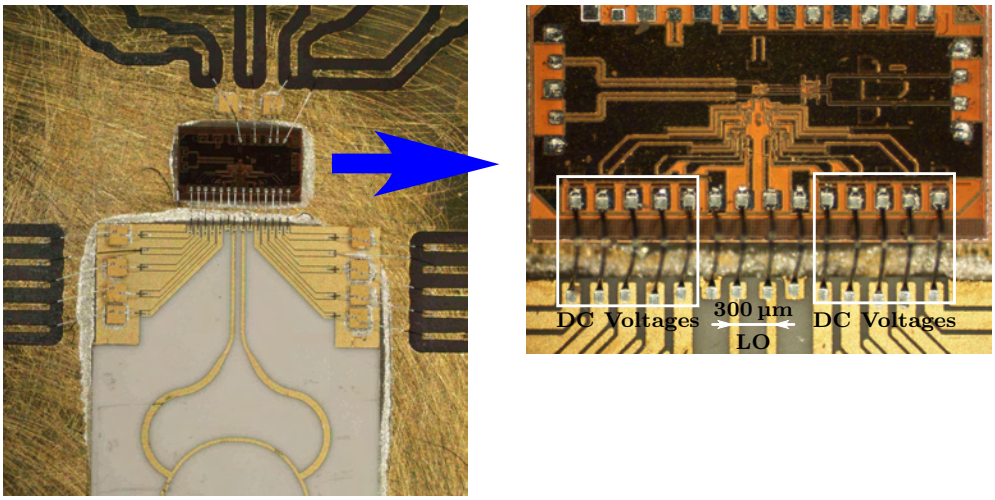


Figure 3.27: *Balun-die interface with wires bonding and DC-filtering microcapacitors.*

3.6.2 K-band rat-race balun

The balun has been designed on a 5 mils (127 µm) alumina substrate to keep microstrip lines compatible with the size of the RF pads of the chip. It is placed close to the chip and stuck on a FR4 test board (Figure 3.28). Both circuits are connected together using bonded wires as shown in figure 3.27. The coupler is optimized to match the low input impedance of about 34 Ω at 19 GHz of both pulse shaping circuits. An open circuit is uesd at the isolated port (N°4) instead of the usual matched load to avoid via hole drilling to the ground underneath. The balun microphotograph is shown in figure 3.30. The upper sides of this circuit have been used to provide DC bias voltage. Decoupling chip capacitors are also displayed. The design has been verified using 3D EM simulation. Measured and simulated S-parameters are presented in figure 3.29 and EM simulation are fitting fairly well to measurements. The usable LO frequency range extends from 14 to 26 GHz. Its center frequency is around 17.8 GHz and has driven the experiments presented in following sections.

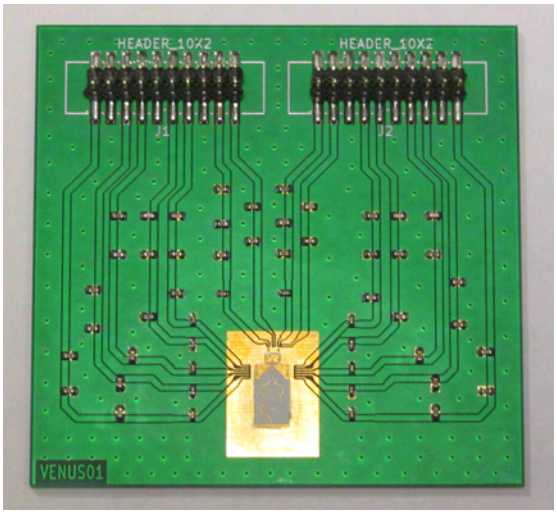


Figure 3.28: *FR4 test board.*

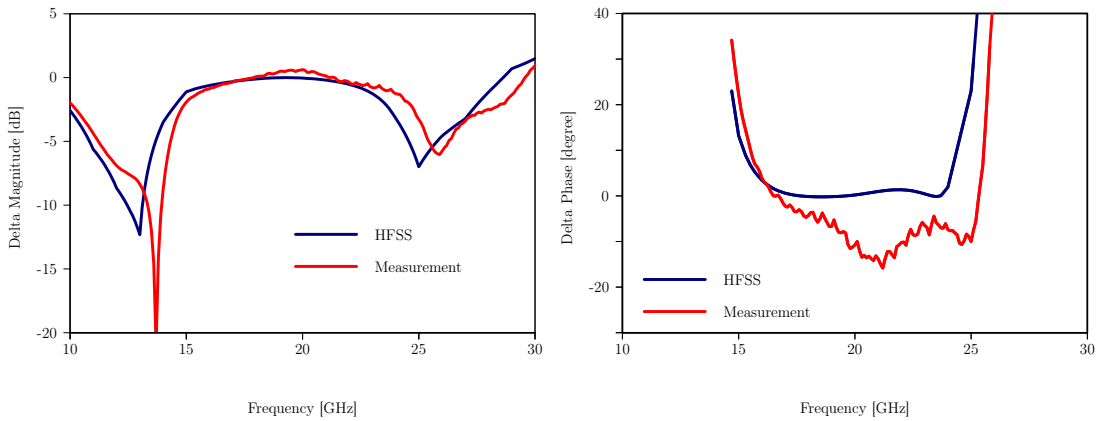


Figure 3.29: *Simulated and measured S-parameters delta magnitude (a) and delta phase (b) of the alumina balun.*

3.6.3 Conversion Gain

Fig.3.31 shows simulated and measured power conversion gains with $f_{RF} = 18.8\,\text{GHz}$ and $f_{LO} = 17.8\,\text{GHz}$ in the LO power range starting from $-11\,\text{dB}$ to $2\,\text{dB}$. This result is plotted at a constant V_G of $2.45\,\text{V}$ but V_{ctrl} is adjusted to the optimal result for each displayed data point. Electrical simulations agree very well with measurements with a nearly constant offset of $0.2\,\text{dB}$ in favor of simulations within the displayed LO power range. Knowing the simulated voltage gain of the IF amplifier, the mixer voltage

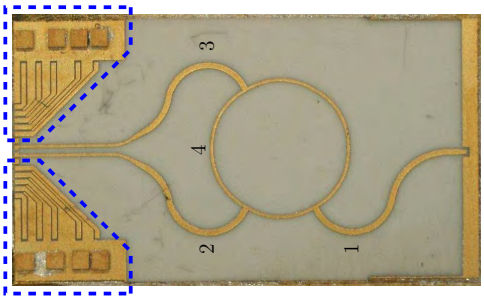


Figure 3.30: *Rat-race balun microphotograph.*

conversion gain is estimated and displayed in figure 3.32. Using this graph, a conversion gain of −2.1 dB is observed with a LO power of −1 dBm. This result is very close to the −2 dB predicted by the analytic expression ((3.16)) with an estimated duty-cycle of 28%, a ratio γ of 60 and a transition time of 5 ps.

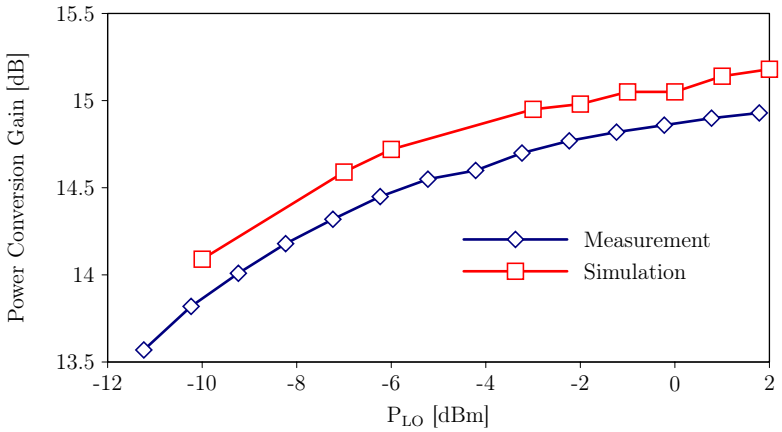


Figure 3.31: *Measured and simulated conversion gain.*

3.6.4 1 dB Compression point

Measured input and output referred 1 dB compression points of −25.7 dBm and −12.3 dBm respectively are extracted from figure 3.33 at a LO power of −1 dBm. Once again, this result is very close to simulated data (−24.5 dBm and −10.8 dBm respectively) and are limited by the IF amplifier. If this amplifier is replaced by its small-signal model in electrical simulations, the limitation brought by the ring mixer can be extracted. Such electrical simulations result in another input-referred 1 dB compression point of −5 dBm for the passive mixer which leads to an output referred compression point of +8.7 dBm.

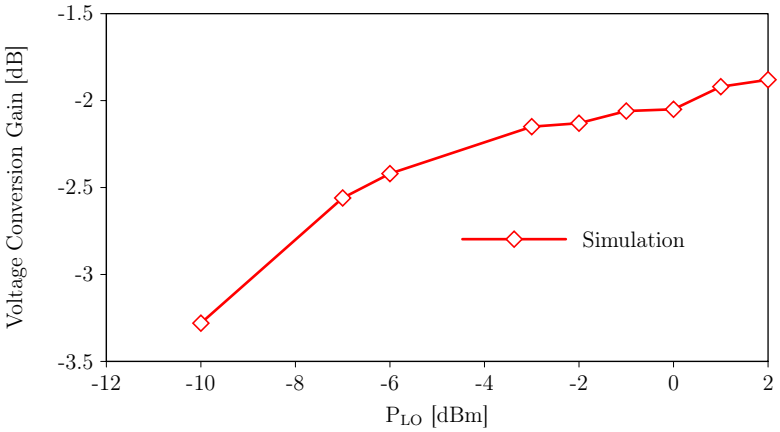


Figure 3.32: *Mixer-only simulated conversion gain.*

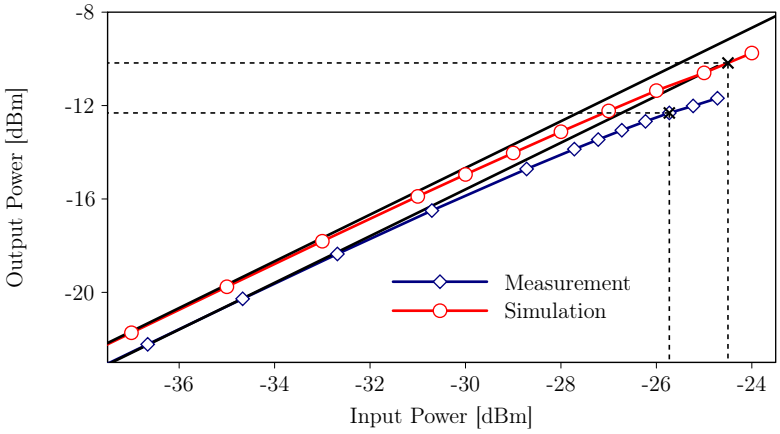


Figure 3.33: 1 dB *compression point extraction with* $f_{RF} = 18.8\,\text{GHz}$ *and* $f_{LO} = 17.8\,\text{GHz}$.

3.6.5 Noise Figure

The cold source technique is employed to measure the noise figure of the down-converter. Two $50\,\Omega$ resistances placed at room temperature (297 K) are connected to the RF terminals of the mixer. The noise power N_{mix} produced at the output of the circuit is amplified by an external LNA and measured using a spectrum analyzer. The test-bench contribution is de-embedded from the raw measured noise power spectrum density, and the equivalent noise temperature of the mixer T_{mix} is computed using (3.19):

$$T_{mix} = \frac{N_{mix}}{\sum G_c \cdot \Delta f} \tag{3.19}$$

All the RF frequency bands falling into the same IF must be counted for a reliable equivalent temperature extraction. Those bands are centered on $kf_{OL} \pm f_{IF}$ ($k \in \mathbb{N}$). Fortunately, conversion gains vanish as k increases. The measured conversion gains around two or tree times the LO frequency are displayed in figure 3.34. These data are used in (3.19) and the noise figure NF_{mix} is extracted using:

$$NF_{mix} = 1 + \frac{T_{mix}}{T_0} \tag{3.20}$$

Where T_0 is 290 K. This definition is equivalent to an all-sidebands (ASB) noise figure since more than two sidebands translate toward the same IF frequency [51].

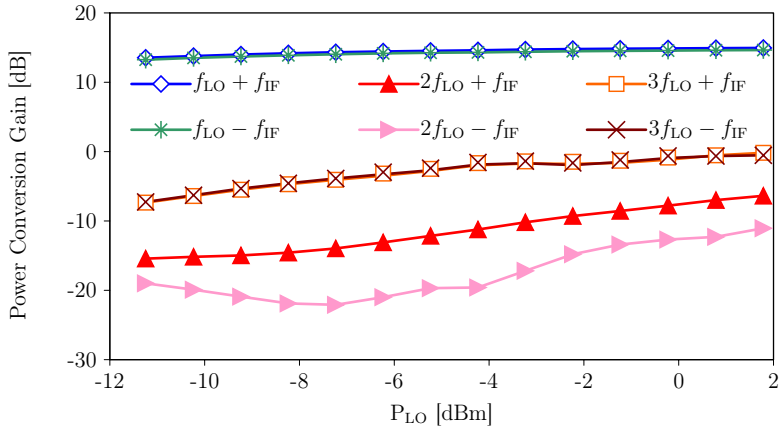


Figure 3.34: *Measured conversion gains around* $2\prod$ *and* $3\prod$ *the LO frequency.*

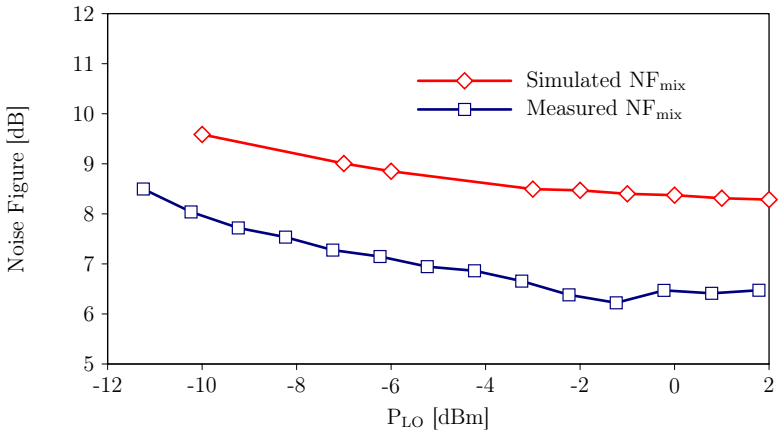


Figure 3.35: *Simulated and measured noise figure.*

The noise figure is extracted from (3.19) and (3.20) and shown in figure 3.35. The

lowest measured NF is about 6.3 dB at a LO power of −1.2 dBm. These results are compared to electrical simulation with a difference of about 2 dB in favor of measurements all over the investigated LO power range. These results must be analyzed very carefully. Convergence problems in the Cadence simulator forced us to use the ADS version of the design kit for which parasitic extraction tools doesn't exist. We noticed some differences in the simulated conversion gain and linearity which might influence the noise performance. Furthermore, this result arises from the hot-cold method, which does not match the method used in practice.

Although noise contribution of the IF amplifier is included, this result still represents a significant improvement over usual 50% duty-cycle driven passive mixers which are penalized by their conversion losses, around $9 \div 10$ dB at best for the passive mixer in the same frequency range [52, 53].

3.6.6 Measured bandwidth of the sampling mixer

To find the RF bandwidth of the down-converter, the RF and LO frequencies have been swept from 4 GHz to 27 GHz while maitaining a constant IF frequency of 1 GHz. Two measurement campaigns were required because of the limited bandwidth of $15 - 27$ GHz of the rat-race balun. From 4 GHz to 20 GHz, this rat-race balun has been replaced by an external 180° hybrid coupler (Krytar Ref.4060265). These results, shown in figure 3.36, demonstrate an ultra-wide bandwidth starting from 4 GHz up to 27 GHz at a nearby constant gain. This result is at the state of the art. The lower limit is forced by the values of the coupling capacitors used within LO pulse-shaping circuit while the external rat-race balun sets the higher limit. The electrical simulation carried on the same circuit shows that the real bandwidth extends well below 31 GHz.

The estimated voltage conversion gain of the mixer is presented in the figure 3.37. This result confirms the very high bandwidth of the mixer.

3.6.7 Conclusion and state-of-the-art comparison

Theses measurements validate the first ever reported sampling mixer exceeding the GHz range. An original analog-based pulse shaping circuit is used to provide the required low duty-cycle LO voltage, allowing the passive ring mixer to work as a sampling-and-hold circuit up to almost 30 GHz.

All the results are summarized in the table I and compared to others passives operating at frequencies comprised between 2 GHz and 27 GHz.

Our circuit is the first low duty-cycle sampled mixer demonstrated at these frequencies.

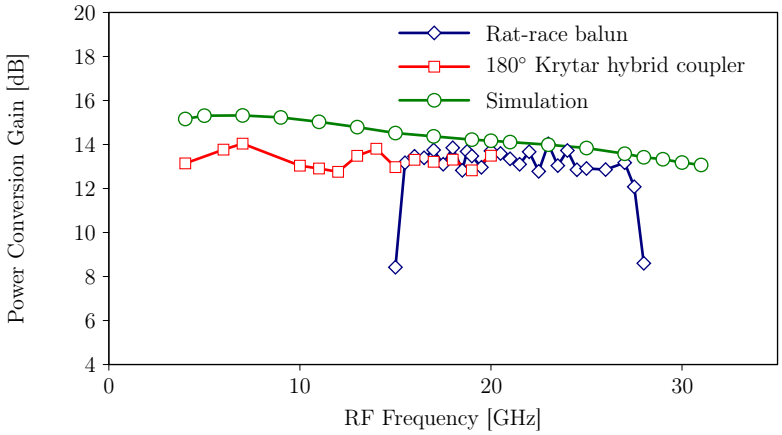


Figure 3.36: *Simulated and measured bandwidth of the sampling mixer.*

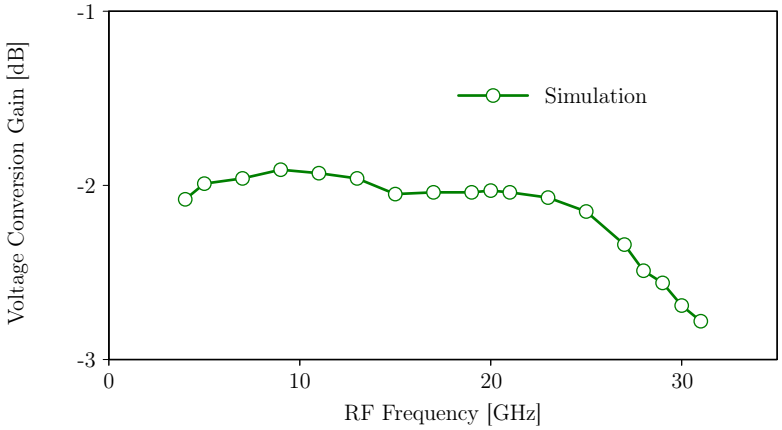


Figure 3.37: *Simulated voltage conversion gain of the sampling ring mixer.*

Its performances are compared with some usual 50% duty-cycle driven passive mixers in Table I. Is presents a conversion losses at least $3 \div 4$ times lower at the best value finds in the litterature on a very wide RF frequency range. Best noise performances are also obtained. All of this using the lower driving LO signal power.

Ref	Technology	RF Frequency [GHz]	LO Power [dB]	Conv. Losses [dB]	Noise Figure [dB]	OP1dB [dBm]	Topology
[52]	CMOS 130 nm	19 ÷ 26.5	6	8 ÷ 12	9 (@20 GHz)	-7.3	FET, DB Fundamental
[54]	CMOS 130 nm	20 ÷ 26	0	9 ÷ 12	20 (@20 GHz)	-14.5	FET, SB Fundamental
[55]	CMOS 180 nm	7 ÷ 23	11	10.6 ÷ 13.7	-	-	FET, DB Fundamental
[56]	CMOS 250 nm	2 ÷ 9	10	6.4 ÷ 7.9	-	-1.6	FET, DB Fundamental
This Work	BiCMOS 0.13 µm	4 ÷ 27	-1 (@17.8 GHz)	2 ÷ 2.4*	6.3 (@18.8 GHz)	8.7**	SS-FET, DB Fundamental

* Voltage conversion losses of ring mixer only ** Value extrapolated using a linear IF amplier (−12.3 dBm really measured)

Table I: *Performances comparison summary with other passive mixers.*

Bandwidth Extension to V-band Using Sub-sampling Technique

4

4.1 Introduction

Since the V frequency band, ranging from 50 to 75GHz, presents several wide free spectrum bandwidth, it has attracted even more researchers interest in the last years. Above all, the large ISM (Industrial, Scientific and Medical) license-free band of 7 GHz centered at 60 GHz offers many advantages for short-range consumer applications such as Wireless Local Area Networks (WLAN) or Wireless Personal Area Networks (WPAN) [57]. Indeed, the large available spectrum allows high data rates for multi-Gb/s wireless data transmission and the short wavelength leads to small antenna dimensions with the theoretic option to realize compact multi-antenna systems.

However, on the receiver side, front-ends should conciliate several stringent requirements regarding noise figure, gain, linearity as well as local oscillators (LO) phase noise to support very high data-rates [58]. Several 60 GHz receivers have been reported last years, using BiCMOS or pure CMOS technologies. Most of them adopt a super-heterodyne architecture but the strategy regarding the first mixing stage varies. Some receivers are based on moderate IF frequencies. In this case, a millimeter-wave LO signal is then required [59]. Other receivers implement high-IF solutions [60] or multiplied LO signals [1, 61–63] to reduce the LO frequency. Since the phase noise of millimeter-wave oscillators suffer from the poor Q-factors of varactors and others passive elements, both last approaches may allow higher phase noise performances by generating a much lower LO frequency for which Q-factors are better. Instead of using a multiplied LO frequency, similar results can be achieved with a sub-harmonic mixer [64]. This approach may lead to a simplified circuit but the issue in this case is the conversion gain and difficulties to keep an acceptable value.

In this chapter, we propose the analysis and the characterization of this last sub-harmonic operation. This study is developped on the previous presented topology pumped by a nearby 20 GHz LO signal with the aim of the design of a V-band receiver first frequency translating stage. Despite its benefit of lower LO frequency generation, this kind of mixer displays high conversion losses when a passive circuit topology is involved.

As explained in previous chapter, these losses may be considerably reduced by using a voltage-driven sampled resistive mixer fed with 25% duty-cycle LO driving signals. The originality of this work is hence to combine the advantages conferred by both sub-harmonic and sampling-mixer techniques in one circuit. A brief overview of the 60 GHz mixer state-of-the-art is reported in section 4.2. Simulations and experimental results are summarized in section 4.3, for the original solution we propose. The comparison with both passive and active mixers is realized in section 4.4 and some conclusions are given in 4.5.

4.2 60 GHz mixer state-of-the-art

Several V-band mixer topologies found in literature are here classified (figure 4.1). For each type, the main characteristics and drawbacks are briefly reported.

4.2.1 Fundamental mixers

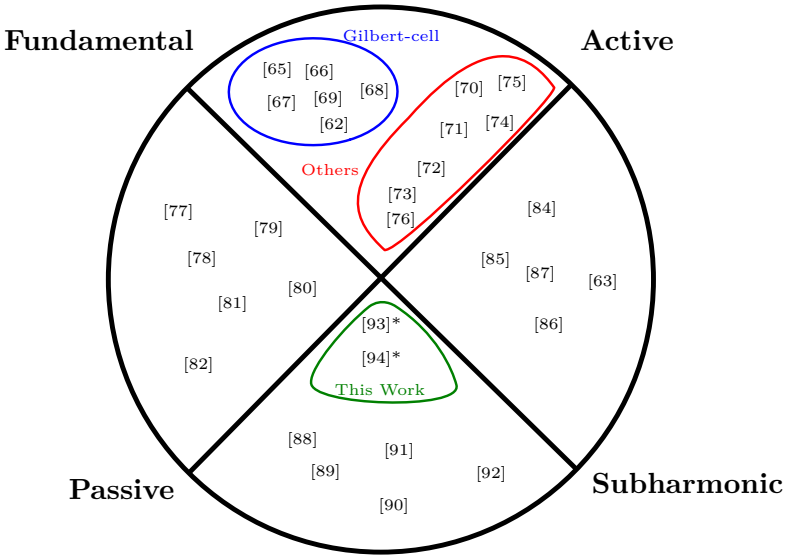
Active mixers are largely used at RF frequencies, since they supply high conversion gain and quite good noise performances, while their great integration capabilities lead to small chip areas. Their drawbacks are the high dc power consumption and the limited linearity. Besides, noise performances degrade when frequencies are increased up to millimeter-wave. The most commonly used active mixer is the double-balanced Gilbert-cell structure. Around 60 GHz, it usually provides moderate conversion gain and good port-to-port isolation with high power consuming. At these frequencies, there are some Gilbert-cell mixers designed into CMOS [65–67] and BiCMOS [62] technologies. Recently, some improved Gilbert-cell mixers have been demonstrated. In [68] conversion gain, noise figure and bandwidth of a 65 nm CMOS Gilbert mixer are substantially improved by placing an inter-stage inductance between the transconductance and the switching stages. Otherwise a current-reuse technique which allows high conversion gain and lower power consumption can be implemented as reported in [69] for a 90 nm CMOS technology. Recently, low-voltage and low-power active mixer topologies have been investigated with different CMOS technologies. In the double-balanced gate-pumped topology reported in [70, 71], both RF and LO signals are combined with a 180° hybrid combiner and applied on the four gates of the mixer aloows to reduce the supply voltage and hence the dc consumption. Similar approach using 90° hybrid coupler is presented in [72, 73]. In [74], the classical passive resistive ring mixer structure has been modified by introducing a DC path on drain terminal to bias the transistors of the core at weak inversion region.

When devices are biased in this region, drain-source current has a non-linear exponential characteristic hence the transistors have higher g_m/I_{DS} ratio which makes it suitable for very low power applications. Source-pumped version with forward body-biased (FBB) to reduce threshold voltage is reported in [75]. Also, in the NMOS bulk-driven topology presented in [76], transistors are biased with a DC voltage alwais on drain terminal. Nonetheless, some difference exist with the pumping signal applied to the bulk. Since threshold voltage depends on bulk-source voltage, it can be modulated by injecting a LO signals into the NMOS bulk isolated by deep N-well. Thus, FETs are turned ON and OFF and mixing operation occurs. These last mixer topologies exhibit low DC power consumption while they present a linearity in line with the best Gilbert cell one [11]. These mixers topologies require lower LO driving power, as well, but their conversion gain is small, when they do not present conversion losses, and their noise figure is usually high.

On the other hand, passive mixers allow high linearity, low power consumption and lower flicker noise due to the absence of bias current, but suffer from high conversion losses. Consequently, an high gain IF amplifier stage and a high LO power driving signal are usually needed. Passive mixers with FET transistors have been presented in [77–80]. Receiver first mixer based on power-matched FET passive mixer are also demonstrated in [81]. Besides the FET mixers, another way to implement a passive mixer is to use diodes. In [82] Schottky-barrier diodes have been employed. Nonetheless, thanks to its much linear channel than a diode junction, FET resistive mixers show lower distortion and higher saturation level [83]. All topologies we have just presented use a millimeter-wave frequency LO pump signal. LO design as well as the receiver phase noise are then important issues. Next paragraph presents sub-harmonic operation which can bring a good solution to these issues.

4.2.2 Sub-harmonic mixers (SHM)

As previously outlined, the main advantage of sub-harmonic mixers is that lower LO frequency is required, which decreases LO design challenge. Into the 60 GHz frequency band and based on the LO 2^{nd} harmonic mixing, some active gate-pumped and Gilbert-cell SHM are presented in [84,85] and [86,87], respectively. The main features of these mixers are similar at the same topologies in fundamental configuration previously described. The same also applies at the passive mixer configuration with FET devices which have been employed in [88,89]. At millimeter-waves frequencies, anti-parallel diode pair (APDP) is frequently used in such mixer [90–92]. The main advantage of this topology is that



* Realizations at 2.4 GHz.

Figure 4.1: *Different categories of* 60 GHz *mixers published to date.*

even-order intermodulation products are rejected without any balun [95].

It is worth noticing that sub-sampling (SS) technique belongs to sub-harmonic mixer category (4.1). In the sampling process, the harmonic component generated by the switching operation at LO frequency mixes with the RF input producing replicas each time f_{RF} is around multiples of f_{LO} [96].This technique has been demonstrated at low frequency in [93, 94]. Because of the pulsed LO signal generation becomes challenging at higher frequencies, its utilization has been limited at few gigahertz. However, in this chapter a broadband sub-sampling mixer suitable for 60 GHz applications is demonstrated.

4.3 Characterization of the mixer in a sub-sampling operation

Using the same measurement setup previously described, the circuits has been tested in subharmonic configuration. It worth remembering that this test has been possible because no balun has been integrate on-chip and thanks to VNA PNA-X which allows to generate the CW RF differential signal. The only change involves control voltages of the pulse shapers V_{ctrl} and V_G. The circuit bias is 44.2 mA at 2.4 V. The current splits into 35 mA and 9.2 mA for both pulse generators and IF-amplifier, respectively. As in previous fundamental mixing setup, once the value of V_G is fixed (this time equal to 2.37 V), V_{ctrl}

is swept to find the best conversion gain (in this case 4 dB for 0 dBm LO power) as shown in figure 4.2. An horizontal shift of about 0.04 V is observed between simulation and measurement, but similar trend in the first parts of the graph has been obtained. This difference is probably due to the pulse shapers behavior slightly different between simulation and measurement. The agreement between simulations and measurements is still quite good. Simulations are also used to estimate the equivalent duty-cycle values (figure 4.3) because this characteristic can not be measured.

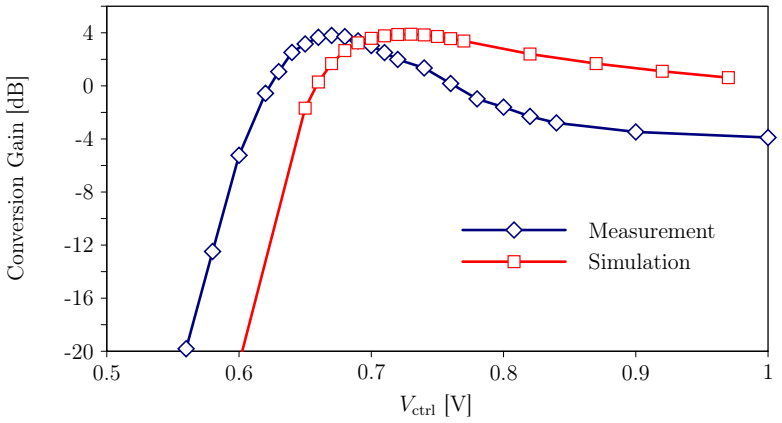


Figure 4.2: *Simulated and measured conversion gain variations for different values of V_{ctrl} for a fixed value of $P_{LO} = 0$ dBm.*

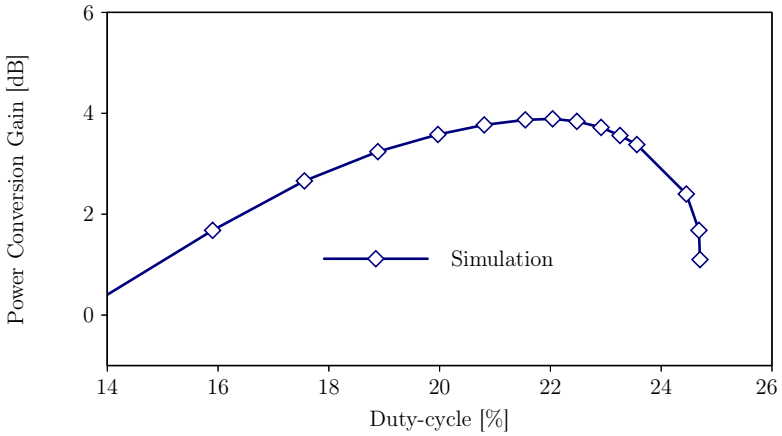


Figure 4.3: *Simulated conversion gain variations for different values of duty-cycle with $P_{LO} =$ 0 dBm.*

As depicted in figure 4.3 with a LO applied power $P_{\mathrm{LO}} = 0$ dBm the best performances are obtained with a duty-cycle of about 22 % which is quite lower than the value of 28 % that has been required for the fundamental mixing operation. This difference is due to

the 3^{rd} harmonic excitation which needs a lower duty-cycle to be maximized as expected from the analytical model reported in section 3.3. Finally, it must be noticed that all measurements are carried out, here, with a different prototype than the one used in chapter 3 for the mixer characterization under fundamental operation. This time the optimum LO frequency is 19 GHz , because a new LO balun is used, and all tests are driven under this frequency. The results are reported in the following paragraphs.

4.3.1 Conversion Gain

4.3.1.1 Conversion gain versus LO power

Figure 4.4 compares measured and simulated conversion gain versus LO power at a RF frequency of 58 GHz. Once again electrical simulations agree very well with measurements. A conversion gain of 4 dB at 0 dBm LO input power for the integrated circuit which includes the mixer and the IF-amplifier. The equivalent voltage conversion gain value given by simulation is 7.4 dB. This difference is still due to the lack of matching into the RF paths between pads and mixer ports. For the mixer on its own, voltage conversion losses can be evaluated around 7.8 dB (figure 4.5). Increasing the drive LO power signal up to 4 dB these conversion losses decrease down to 7.2 dB, whereas decreasing the LO power, the conversion losses stay lower than 12 dB with a minimum LO power of −8 dBm, as depicts figure 4.5.

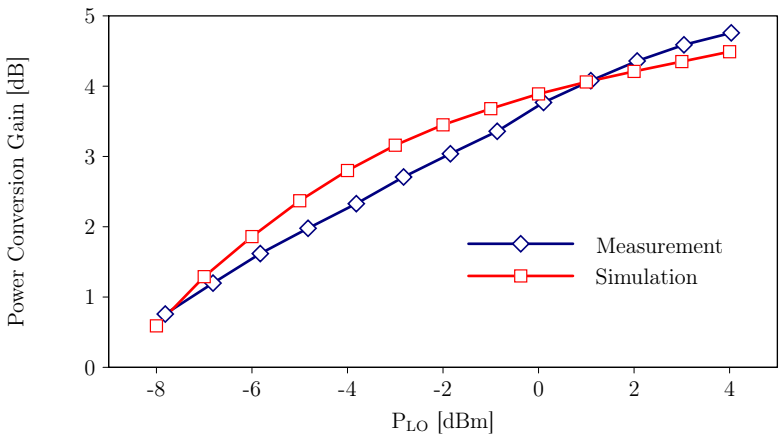


Figure 4.4: *Measured and simulated power conversion gain of the couple mixer/IF-amplifier, at a RF frequency of* 58 GHz.

In the 60 GHz frequency range, conversion losses of 7.8 dB can be compared with others resistive mixers operating from a fundamental LO frequency [77] or in a sub-harmonic configuration [88]. Both mixers offer conversion losses higher than 12 dB

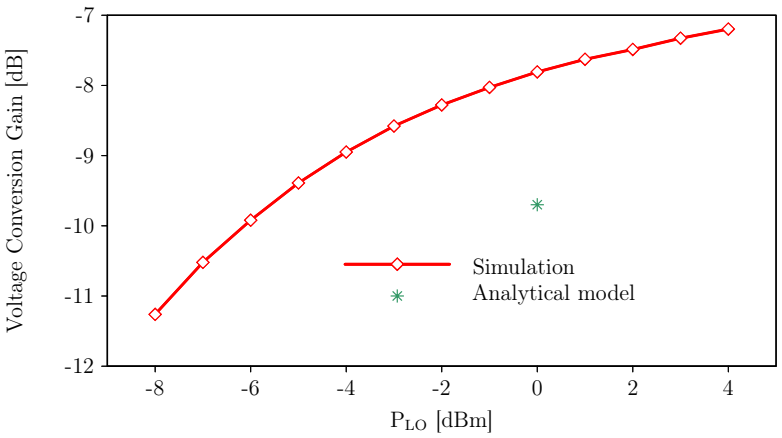


Figure 4.5: *Mixer-only simulated voltage conversion gain at a RF frequency of* 58 GHz

reached with LO powers of 8 dBm and −1 dBm, respectively. As a summary, our circuit presents well-lower losses for an equal LO power, or equivalent losses for a well-lower LO power. In the first case, less gain is required for IF-amplifier, while in the second case the local oscillator design is once more relaxed and results to a "low" frequency / low output power oscillator design.

4.3.1.2 Model comparison

Considering the estimated duty-cycle of 22 % reached with $P_{\mathrm{LO}} = 0$ dBm, the analytical model developed in paragraph 3.3.5 predicts a conversion gain of about −9.7 dB, which is about 2 dB lower than the −7.8 dB simulated value. Nevertheless, this result can be considered to be quite satisfactory since the simplified nature of the model and since a small error on duty-cycle estimation can lead to a high discrepancy on conversion gain prediction (the slope giving the voltage conversion gain versus duty-cycle for a 3^{rd} LO harmonic pumping signal is quite high as plotted in 3.13b). The simulated value is obtained for a duty-cycle of 20 %.

4.3.1.3 Conversion gain versus RF frequency

Measured and simulated down converter (mixer associated with the IF-amplifier) conversion gains are plotted in figure 4.6 for a RF frequency ranging from 10 GHz to 76 GHz while the IF frequency is kept constant at 1 GHz. For measurements, the highest test frequency is limited by the RF synthesizer of the VNA PNA-X which maximum frequency is 67 GHz. Moreover, two configurations are used for the experimental characterization : since the integrated LO balun presents a low cut-off frequency of about 14.5 GHz (which

limits the low RF frequency around 45 GHz), in the second configuration, a commercial external 180° hybrid coupler is connected by way of a GSSG probe at the LO pads of the circuit. In this second case, the low RF frequency can be decreased down to 16 GHz (f_{LO}=5 GHz). Since on-chip pads are realized in aluminum, the RF probe contact quickly degrades after few probings and the measurement become very sensible and difficult. This reason could explain measurements results slightly perturbed especially those made with the 180° hybrid coupler that come after. Nevertheless, measurements and simulations performed on the down-converter are in a quite good agreement. All observed differences can be attributed to discrepancies in performances of the pulse shapers between simulations and measurements. Simulated voltage conversion gain of the whole downconverter is depicted in figure 4.7 and stays included in the range from 6.5 to 8.3 dB. Performances of the mixer on its own are also extracted from simulation and plotted in figure 4.8. Because the impulsion shape is closer to ideal when OL frequency is decreased, reduced mixer conversion losses around 6.9 dB up to f_{RF} = 50 GHz (LO frequency up to 16 GHz) are observed, and these losses are lightly increasing after.

As a conclusion, these results demonstrate that, experimentally, the down-converter works properly on the whole RF frequency test range from 16 GHz to 67 GHz. Furthermore, simulations show that sthis RF frequency range can be expanded from 10 GHz to 76 GHz taking into account the experimental pulse shaper frequency performances. Based on this reporting, one can state that a sub-sampling mixer is able to present very broad-band performances.

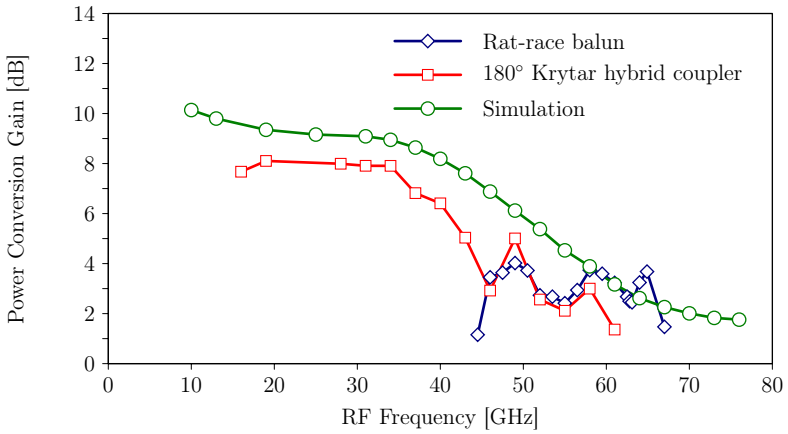


Figure 4.6: *Simulated and measured power conversion gain for the down-converter, LO power is 0dBm.*

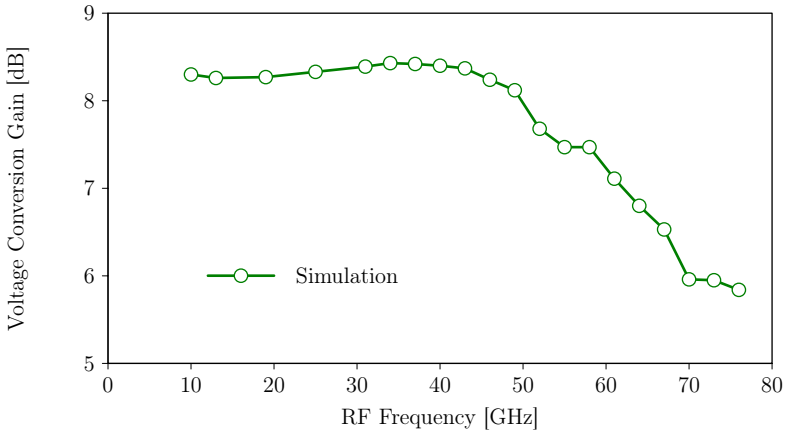


Figure 4.7: *Simulated voltage conversion gain of the downconverter versus RF frequency, LO power is 0dBm.*

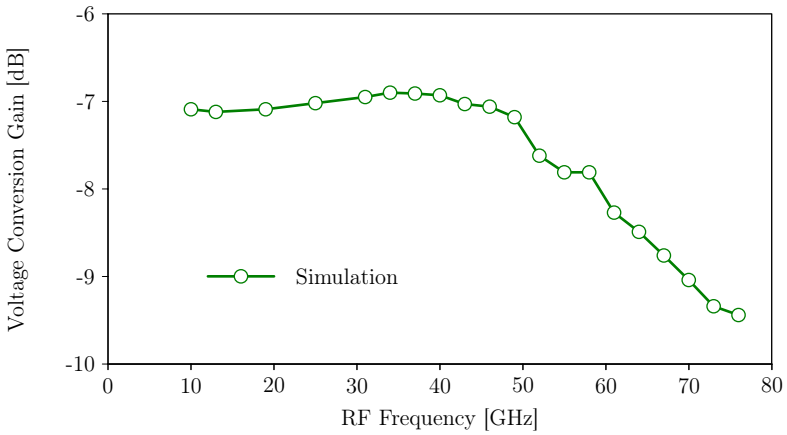


Figure 4.8: *Simulated voltage conversion gain of the single mixer versus RF frequency, LO power is 0dBm.*

4.3.2 1 dB Compression point

Measured input and output referred 1 dB compression points of −16.4 dBm and −13.4 dBm respectively are extracted from figure 4.9 at a LO power of 0 dBm. This result is close to simulated data (−13.5 dBm and −10.5 dBm respectively). As for LO fundamental operation (see paragraph 3.6.4), these two compression points are limited by the IF amplifier. Replacing this amplifier by its small-signal model in electrical simulations gives an estimation of the expected output compression point which becomes −1 dBm.

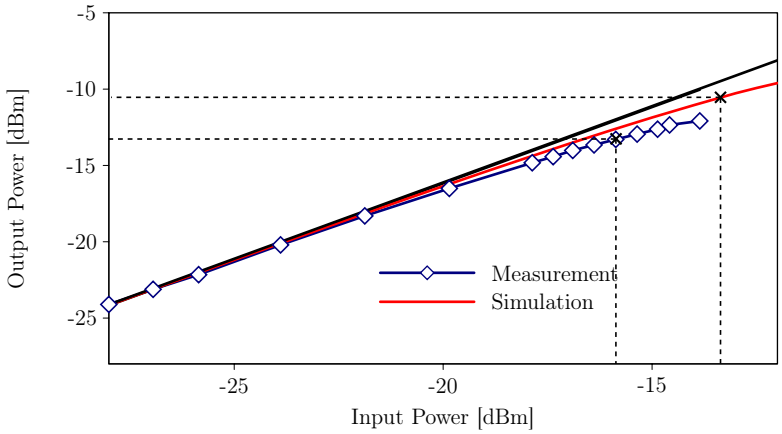


Figure 4.9: *Measured and simulated output IF power versus input RF power at an input RF frequency of* 58 GHz.

4.3.3 Noise Figure

The noise figure is measured using the technique previously reported in section 3.6.5. In this case as well, given the pulse-shaped LO voltage and the broadband RF input of the mixer, RF signals at $3f_{LO} \pm f_{IF}$ and $f_{LO} \pm f_{IF}$ are down-converted by the circuit. Conversion gains for all these RF frequency bands have to be characterized to be able to extract the ASB noise figure which definition has been reported in section 3.6.5. Measured and simulated ASB noise figure are shown in figure 4.10.

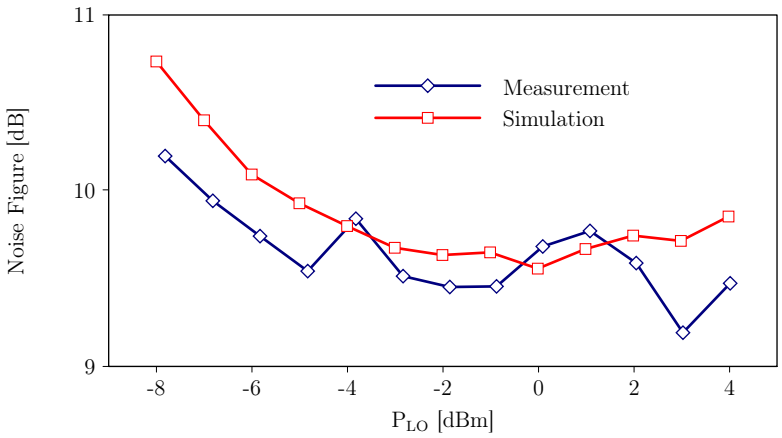


Figure 4.10: *Simulated and measured down-converter noise figure. Frequencies* 58 GHz

At a LO power of 0 dBm, frequencies 58 GHz, a NF of 9.7 dB is obtained, always including the noise contribution of the IF amplifier. This result is better than the few references where the NF is directly reported [80, 91]. Nevertheless, since the FET noise is

minimized when the conversion losses are minimized and that the best achievable noise figure is ideally equal to the losses [83], a wider comparison can be carried out taking into account the conversion losses (Table I). On this basis, we can state that our circuit may reach one of the best performances.

4.4 State-of-the-art comparison

To our knowledge, this sub-sampled (SS) FET mixer topology has not been yet published at these frequencies. In table I, our sub-sampled FET mixer is compared with other FET and APDP (anti-parallel diode pair) passive mixers designed for the same RF frequency range conversion but different IF frequencies. The SS down-converter we propose presents the best conversion losses over the largest operating frequency range, figure 4.11a.

On the linearity, the contribution of the IF amplifier associated with this SS mixer must be removed to fairly compare its performance level with other passive mixers. To calculate this compression point, we assumed that the voltage at IF terminals was buffered by a unity gain voltage amplifier. The output compression point was then measured at the outputs of this balanced amplifier, loaded by $2Z_0$. As shown in figure 4.11b, the obtained compression point remains very close to usual passive mixers operating at similar LO power levels, which allows us to conclude that the SS operation does not worsen linearity against usual configuration.

Ref	Technology	RF Frequency [GHz]	LO Power [dBm]	Conv. Losses [dB]	Noise Figure [dB]	OP1dB [dBm]	Topology
[77]	65 nm CMOS	51 ÷ 62	8.7	12.5 ÷ 15	-	-8.5	Fundamental FET
[78]	0.18 µm CMOS	18 ÷ 50	10	14 ÷ 17	-	-6.5	Fundamental FET
[79]	45 nm CMOS SOI	40 ÷ 50	15	8.35	-	-4.85	Fundamental FET
[80]	90 nm CMOS	33 ÷ 58	10	6 ÷ 9	11 ÷ 13.4	-11	Fundamental FET
[88]	130 nm CMOS	56 ÷ 66	-1	13	-	-16	SHM ×2 FET
[89]	0.15 µm mHEMT	58 ÷ 62	8	15.3	-	-12.8	SHM ×4 FET
[91]	SiGe	56 ÷ 64	5.5	8.3 ÷ 10	12	-16.3	SHM ×2 APDP
[92]	180 nm CMOS	57 ÷ 66	1	15	-	-	SHM ×2 APDP
This Work	0.13 µm BiCMOS	16 ÷ 67	0	6.9 ÷ 8.8*	9.7 (@58 GHz)	-15**	SHM ×3 SS-FET

* Voltage conversion losses of the mixer alone
** Value extrapolated using a pure linear (Av=1) IF amplifier (−13.4 dBm really measured)
APDP = Anti-Parallel Diode Pair, SS = Sub-sampled, SHM = Sub-harmonic mixer

Table I: *Performances comparison summary with other passive mixers.*

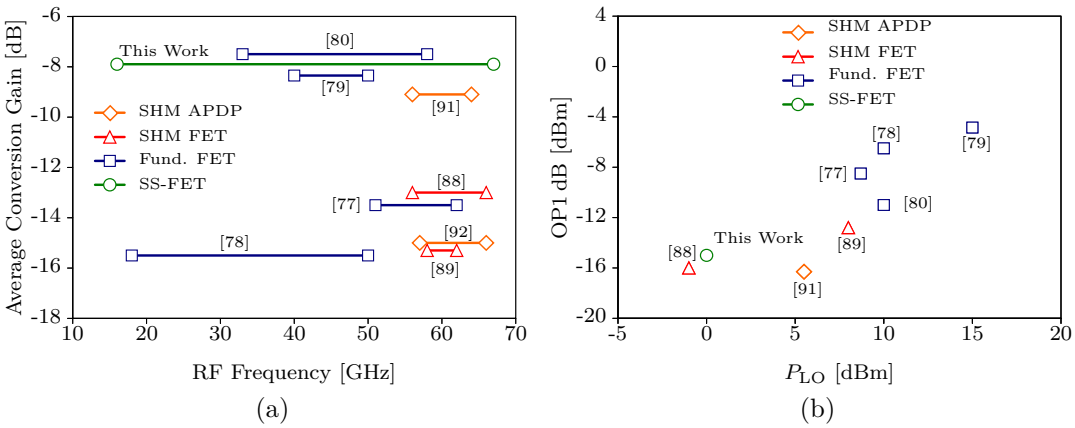


Figure 4.11: *Comparison of monolithic integrated wideband passive mixers by the average conversion losses on the RF frequency bandwidth (a) and the linearity performances versus the applied LO power signal (b).*

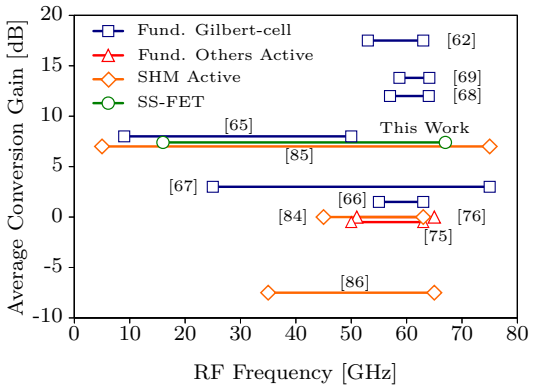


Figure 4.12: *Comparison of the passive proposed down-converter with monolithic integrated wideband active mixers by the average conversion gains on the RF frequency bandwidth.*

Since for the conversion of the 60 GHz RF frequency-band many active mixer integrated circuits exist as reported in section 4.2, a comparison with the active mixer state-of-the-art is carried out in Table II.

Both LO fundamental and LO sub-harmonic active mixers are evaluated. For this comparison our mixer is considered in association with the IF amplifier. The conversion gain is plotted in Figure 4.12. One can notice that the performances reached by our passive down-converter are similar and sometime better than active mixer ones when they address a wide RF frequency range. Some Gilbert-cells exhibit higher conversion gains but on a limited RF bandwidth [68, 69] and with the implementation of an IF amplifier after the active mixer core. As well, mixer linearity is compared in figure 4.13a

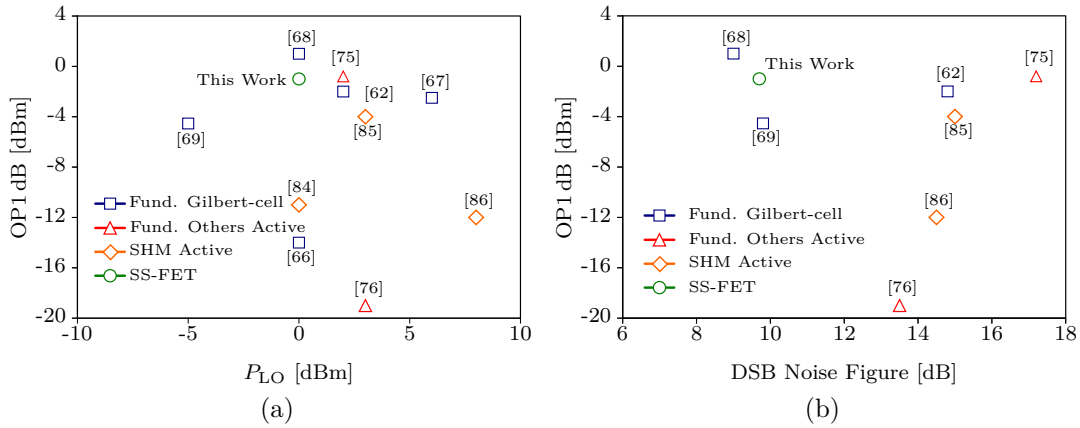


Figure 4.13: *Comparison of the passive proposed down-converter with monolithic integrated wideband active mixers by the linearity versus both applied LO power (a) and noise figure (b).*

versus the LO power. The down-converter we propose exhibits similar performance than the best linear active down-converters [68, 75]. On figure 4.13b. the linearity is reported versus the noise figure. We can see that the down-converter we propose presents one of the higher linearity associated with the lower noise figure.

The only drawback which can be pointed out is the power consumption level of our circuit. However, because no specification has been considered for power consumption during the design, an class-A amplifier is implemented into both LO analog pulse shapers where 60 % of the DC current is sunk. A new design of OL pulse shapers could fix this issue. So, this work demonstrates that sub-sampling passive mixer can be used up to the V-band with attractive performances.

4.5 Conclusion

This chapter presents a sub-sampling passive mixer operating up to millimeter-wave V-band. Driving a resistive ring mixer by a low duty-cycle LO voltage, the RF signal is sub-sampled around the LO 3^{rd} harmonic frequency to give the IF low frequency signal. The originality of this work is to combine the advantages conferred by both sampling-mixer and sub-sampling techniques. Low conversion losses are reached thanks to the low duty-cycle driving signal, while the LO pulse shaper design is quite relaxed because only one third of the LO frequency used for a fundamental mixing is required here. It is even possible to go further and write that the sampling technique for the low IF conversion of V-band signals would not have been possible without the implementation of sub-sampling.

Ref	Tech.	RF Freq. [GHz]	LO Power [dBm]	Conv. Gain [dB]	NF_{DSB} [dB]	OP1dB [dBm]	P_{DC} [mW]	Topology
[68]	65 nm CMOS	57 ÷ 64	0	10 ÷ 14	9 (sim)	1	38.4	Fundamental Gilber-cell
[67]	90 nm CMOS	25 ÷ 75	6	1 ÷ 5	-	-2.5 (@60 GHz)	93	Fundamental Gilbert-cell
[65]	130 nm CMOS	9 ÷ 50	5	5 ÷ 11	16.4 (@15 GHz)	-	97	Fundamental Gilbert-cell
[66]	130 nm CMOS	55 ÷ 63	0	0 ÷ 3	-	-14	-	Fundamental Gilbert-cell
[69]	90 nm CMOS	58.7 ÷ 64.1	-5	12.1 ÷ 15.5	9.8	-4.5	17	Fundamental Gilbert-cell
[62]	0.12 µm SiGe	53 ÷ 63	-	15 ÷ 20	14.8	-2	148.5	Fundamental Gilbert-cell
[76]	130 nm CMOS	51 ÷ 65	3	−1.5 ÷ 1.5	13.5 (@57 GHz)	-19	3	Fundamental Bulk-driven
[75]	130 nm CMOS	50 ÷ 63	2	−5 ÷ 4.2	17.2 (@56 GHz)	-0.8	3	Fundamental FBB
[86]	130 nm CMOS	35 ÷ 65	8	−6 ÷ −9	14.5	-12	90.8	SHM ×2 Gilbert-cell DB
[85]	65 nm CMOS	5 ÷ 75	3	3 ÷ 11*	15	-4	3	SHM ×2 Gate-pumped
[84]	90 nm CMOS	45 ÷ 63	0	0	-	-11	2.4	SHM ×2 Gate-pumped
This Work	0.13 µm BiCMOS	16 ÷ 67	0	(6.5 ÷ 8.3)* (2.3 ÷ 9.8)**	9.7 (@58 GHz)	-1***	106	SS-FET SHM ×3

* Voltage conversion gain.
** Power conversion gain.
*** Value extrapolated using a linear IF amplier (−13.4 dBm really measured)
SS = Sub-sampled, SHM = Sub-harmonic mixer

Table II: *Performances comparison summary with other active mixers.*

The integrated circuit used to demonstrate the potential of V-band sub-sampling passive frequency conversion has been described in chapter 3. Under sub-sampling operation, conversion losses of the mixer on its own are about 8 dB with an output compression point estimated around −1 dBm, for a RF frequency of 58 GHz. The noise figure of the whole circuit including IF amplifier is less than 10 dB at this same RF frequency value. All these performances that are measured for this down-converter are at the state of the art when compared to both passive mixers and active mixers. Furthermore, it is worth noticing that to our knowledge it is the first time the sub-sampling technique is implemented for V-band frequency conversion. Finally, measured performances of the sub-sampling passive down-converter we propose highlight how passive mixers can be an efficient alternative to active mixers, whereas Gilbert-cell are still largely used for the 57 GHz to 64 GHz ISM band dow-conversion.

5 General Conclusions

The demand for higher performances circuits together with lower cost and greater functionality keep increasing at RF and millimeter-wave applications [42]. Therefore this leads to ever new challenges for integrated circuit design, such as front-end receiver, in several frequencies bands and for several applications.

In particular, in the present PhD thesis the research activity addressed the optimization, in 130 nm CMOS silicon-based technologies, of a key building blocks of the receiver front-end as the frequency synthesizer and the down-conversion mixer.

As far as it concerns the frequency synthesis a whole low-power PLO was designed and fabricated. The PLO was designed to work in the Ku band, because the idea in mind was to investigate the feasibility of replacing with cheap pure CMOS technology the expensive and/or discrete technologies nowadays used to design the LNB in the DVBS applications. In particular, the fabricated prototype generates an output tone in the 14.2÷15.1 GHz frequency range and exhibit a phase noise of −86.3 dBc/Hz for an offset frequency of 1 MHz from the 15 GHz carrier. A significant improvement in the phase noise up to 10 dBc/Hz for an offset frequency of 1 MHz was demonstrated by increasing the charge pump current from 25 µA value to 300 µA value. These results has been compared in terms of Figure of Merit (FOM), which takes into account both jitter and power consumption performances, with other silicon-based PLO's and PLL's reported in the literature. The performances of our PLO is well aligned when the charge pump current is set to a value that keeps the loop filter integration (25 µA) whereas it exhibits better performances close to the state-of-the-art when higher charge pump current was employed even at the cost of increasing the loop filter area on the silicon die. These results demonstrate that a low-cost 130 nm CMOS technology is very promising for DVBS, where only discrete components or SiGe technologies have been employed until now.

Thanks to the low power consumption and the high frequency the reported prototype opens also the way to the fabrication of the front-end of a Ku-band microwave radiometer. A X-band radiometer has been recently reported in [7]. Higher frequency allows the large reduction of the antenna size with respect to X-band radiometer. Moreover, its low

power feature makes the proposed PLO up-and-coming for use in outdoor environments as for example a smart sensor network for the detection of wild fire in isolated forest area. In these cases, the low DC consumption is very welcome to supply the electronics with a small dimension energy harvester.

In summary, the PLO reported in the present work demonstrates that the DVB-S compliant phase noise performance can come together with a low power dissipation in a PLL designed in a bulk low cost 130 nm CMOS technology.

Concerning the frequency down-conversion, the design of a K band sampling mixer with 130 nm BiCMOS SiGe technology has been addressed. First, since this mixer topology was demonstrated only at few gigahertz applications, an analytical model has been before developed to evaluate its performances at higher frequency and at the same time to fix the pulses waveform constraints. After, because of the pulse generators found in literature do not work at the required frequencies, an original analog-based pulse shaping circuit is designed here to provide the required high-frequency, high amplitude and low duty-cycle LO voltage waveform defined by the theory. Thanks to this driving signal the down-converter properly works up to almost 30 GHz exhibiting a conversion losses at least $3 \div 4$ times lower than the best value claimed in the literature. It is worth noticing that our circuit is the first low duty-cycle sampled mixer demonstrated at these frequencies.

Finally, in the last section of this PhD thesis, the potentialities for millimeter-wave applications of the fabricated mixer were investigated. In, particular, the mixer was employed in the sub-sampling mode. Thanks to the advantages conferred by both sampling-mixer and sub-sampling techniques, all the obtained performances are at the state of the art when compared to both passive and active mixers. The obtained performances highlight how passive mixers can be an efficient alternative to active mixer, which are largely employed for 60 GHz IMS band. Once again to the best knowledge it is the first time that the sub-sampling technique is implemented for V-band frequency conversion.

All these good results open the way to several future activities. On the PLO side, switched capacitors bank in the VCO topologies can be inserted to increase the tuning range specifications and to reduce the phase noise of the VCO at the same time (decreasing the KVCO).

On the down-converter side, the first future activity would be to replace the actually intermediate amplifier with more suited circuits, to solve the linearity problems faced during the research activity. In addition, a re-design of the pulse shaper would be to carry out with the idea in mind of reducing the power consumption.

Trapezoidal, triangular and square waves Fourier transform calculation

A

The analytical modeling of the sampling mixer needs the Fourier transform calculation of several temporal waveform. In this appendix, the calculations of the Fourier transform of trapezoidal, square and triangular shapes are reported.

A.1 Trapezoidal waveform

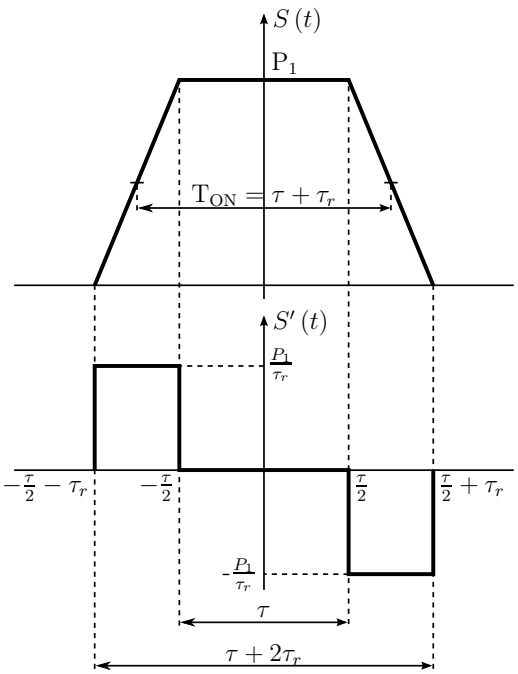


Figure A.1: *Considered trapezoidal waveform $S(t)$ and its derivate $S'(t)$.*

The considered trapezoidal waveform $S(t)$ is reported in figure A.1. It is characterized by an amplitude of $G_{C,\max}$, a rise-fall time equal to τ_r and a on-time $T_{ON} = \tau + \tau_r$ at the half dynamic-range amplitude. The simplest way for Fourier transform calculation $\mathcal{F}(S(t))$ is to use the following property

$$\mathcal{F}\left(S(t)\right) = \frac{\mathcal{F}\left(S'(t)\right)}{j2\pi f} \tag{A.1}$$

In this way only the Fourier transform of two rectangles must be calculated as shown the $S'(t)$ trend in Figure A.1. The Fourier transform of the derivate $\mathcal{F}\left(S'(t)\right)$ is then calculated as follows

$$\mathcal{F}\left(S'(t)\right) = \int_{-\frac{\tau}{2}-\tau_r}^{-\frac{\tau}{2}} \frac{G_{C,\max}}{\tau_r} e^{-j2\pi ft}\, dt - \int_{\frac{\tau}{2}}^{\frac{\tau}{2}+\tau_r} \frac{G_{C,\max}}{\tau_r} e^{-j2\pi ft}\, dt \tag{A.2}$$

$$= \frac{G_{C,\max}}{\tau_r} \cdot \frac{1}{-j2\pi f} \left[\frac{e^{j2\pi f\frac{\tau}{2}} + e^{-j2\pi f\frac{\tau}{2}}}{2} - \frac{e^{j2\pi f\left(\frac{\tau}{2}+\tau_r\right)} + e^{-j2\pi f\left(\frac{\tau}{2}+\tau_r\right)}}{2} \right] \tag{A.3}$$

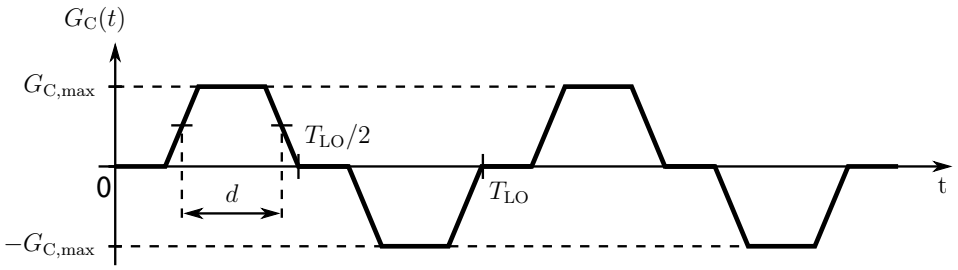


Figure A.2: $G_C(t)$ *signal.*

Using the Euler's formula $cos\,\alpha = \frac{e^{j\alpha}-e^{-j\alpha}}{2}$ the expression (A.3) becomes a sum of cosines which can be written differently using the sum-to-product trigonometric transformation (A.4) and the *sinc* definition ($sinc\,\alpha = \frac{sin\,\alpha}{\alpha}$) finding the Fourier transform of $S'(t)$, (A.6)

$$cos\,x - cos\,y = -2\,sin\left(\frac{x-y}{2}\right)\,sin\left(\frac{x+y}{2}\right) \tag{A.4}$$

$$\mathcal{F}\left(S'(t)\right) = \frac{G_{C,\max}}{\tau_r} \cdot \frac{1}{-j2\pi f} \left[cos\left(2\pi f\frac{\tau}{2}\right) - cos\left(2\pi f\left(\frac{\tau}{2}+\tau_r\right)\right)\right] \tag{A.5}$$

$$= \frac{G_{C,\max}}{\tau_r} \cdot \frac{1}{-j2\pi f} \left[-2\,sin\left(\pi f\tau_r\right) \cdot sin\left(\pi f\left(\tau-\tau_r\right)\right)\right]$$

$$= 2\,G_{C,\max} \cdot sinc\left(\pi f\tau_r\right) \cdot sin\left(\pi f(\tau+\tau_r)\right) \tag{A.6}$$

Therefore, putting this result in the previously reported equation (A.1), the Fourier

transform of the trapezoidal waveform shows in Figure A.1 is obtained

$$\mathcal{F}\left(S(t)\right) = G_{C,\max} \cdot (\tau + \tau_r) \cdot sinc\left(\pi f \tau_r\right) \cdot sinc\left(\pi f(\tau + \tau_r)\right) \quad . \tag{A.7}$$

The overall signal $G_C(t)$ shows in Figure A.2 is a $T_{\mathrm{ON}}/2$ anti-periodic function. Take advantage of the basic Fourier transform proprieties, the second semi-period part of $G_C(t)$ signal presents the same transform of the first, time-shifted by $T_{\mathrm{ON}}/2$. The $\mathcal{F}\left(G_C(t)\right)$ reduces to

$$\mathcal{F}\left(G_C(t)\right) = \mathcal{F}\left(S(t)\right) + \mathcal{F}\left(-S(t)\right) e^{-j2\pi f \frac{T_{\mathrm{LO}}}{2}} \cdot \frac{1}{T_{\mathrm{LO}}} \sum_{n=-\infty}^{+\infty} d(f - \frac{n}{T_{\mathrm{LO}}}) \tag{A.8}$$

$$= \mathcal{F}\left(S(t)\right)\left(1 - e^{-j2\pi f \frac{T_{\mathrm{LO}}}{2}}\right) \cdot \frac{1}{T_{\mathrm{LO}}} \sum_{n=-\infty}^{+\infty} d(f - \frac{n}{T_{\mathrm{LO}}}) \tag{A.9}$$

where $\frac{1}{T_{\mathrm{LO}}} \sum_{n=-\infty}^{+\infty} d(f - \frac{n}{T_{\mathrm{LO}}})$ is a burst of Dirac pulses spaced for $1/T_{\mathrm{LO}}$ introduced because of $G_C(t)$ is a periodical signal with period T_{ON}.

Substituting in this equation the result of (A.7), it become

$$\mathcal{F}\left(G_C(t)\right) = G_{\mathrm{C,max}}\left(\tau + \tau_r\right) sinc\left(\pi \tau_r f\right) sinc\left(\pi f\left(\tau + \tau_r\right)\right)\left(1 - e^{-j\pi f T_{\mathrm{LO}}}\right) \cdot \frac{1}{T_{\mathrm{LO}}} \sum_{n=-\infty}^{+\infty} d(f - \frac{n}{T_{\mathrm{LO}}}) \tag{A.10}$$

From the Figure A.1, the ON time is arbitrary picked up at the half rise-fall time and it is equal to $T_{\mathrm{ON}} = \tau + \tau_r = d\,T_{\mathrm{LO}}$ where d is the duty-cycle. Introducing this last consideration into $\mathcal{F}\left(G_C(t)\right)$, the final results is following reported

$$\mathcal{F}\left(G_C(t)\right) = G_{\mathrm{C,max}} d sinc\left(\pi \tau_r f\right) sinc\left(\pi \frac{f}{f_{\mathrm{LO}}} d\right)\left(1 - e^{-j\pi \frac{f}{f_{\mathrm{LO}}}}\right) \cdot \sum_{n=-\infty}^{+\infty} d(f - n\, f_{\mathrm{LO}}) \tag{A.11}$$

A.2 Triangular waveform

The triangular shape is shown in Figure A.3. The method is the same used in previous case. The Fourier transform of derivate is following calculated:

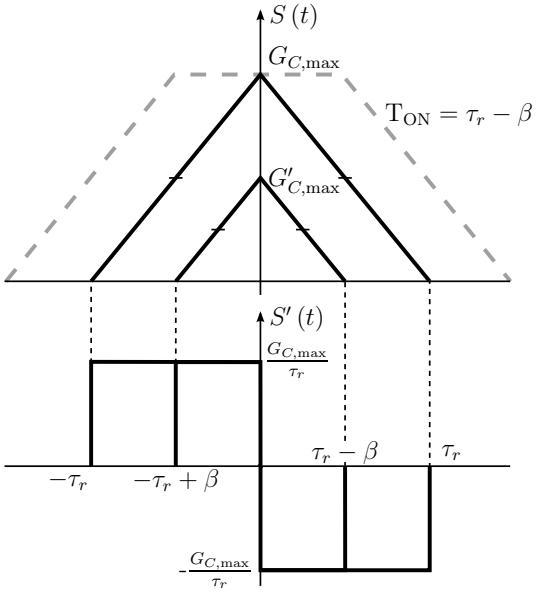


Figure A.3: *Considered triangular waveform $S(t)$ and its derivate $S'(t)$.*

$$\mathcal{F}\left(S'(t)\right) = \int_{-\tau_r+\beta}^{0} \frac{G_{C,\max}}{\tau_r} e^{-j2\pi ft}\, dt - \int_{0}^{\tau_r-\beta} \frac{G_{C,\max}}{\tau_r} e^{-j2\pi ft}\, dt \tag{A.12}$$

$$= \frac{G_{C,\max}}{\tau_r} \cdot \frac{1}{-j\pi f} \left[\frac{e^{j2\pi f(\tau_r-\beta)} + e^{-j2\pi f(\tau_r-\beta)}}{2} - 1 \right] \tag{A.13}$$

Knowing that $cos\,\alpha = \frac{e^{j\alpha}-e^{-j\alpha}}{2}$, $cos\,2\alpha = cos^2\alpha + sin^2\alpha$ and $cos\,2\alpha = cos^2\alpha + sin^2\alpha$ (A.13) become

$$\mathcal{F}\left(S'(t)\right) = \frac{G_{C,\max}}{\tau_r} \cdot \frac{1}{-j\pi f} \left[cos\,2(\pi f(\tau_r-\beta)) - 1\right] \tag{A.14}$$

$$= \frac{G_{C,\max}}{\tau_r} \cdot \frac{1}{-j\pi f} [cos^2\pi f(\tau_r-\beta) + sin^2\pi f(\tau_r-\beta) + -cos^2\pi f(\tau_r-\beta) - sin^2\pi f(\tau_r-\beta)]$$

$$= \frac{G_{C,\max}}{\tau_r} \cdot \frac{1}{j\pi f} \cdot 2\, sin^2\pi f(\tau_r-\beta) \tag{A.15}$$

Now using the equation (A.1) and keeping in mind the *sinc* definition, the Fourier transform $\mathcal{F}\left(S(t)\right)$ has been calculated

$$\mathcal{F}\left(S(t)\right) = G_{C,\max}\left(\frac{d^2}{\tau_r f_{\mathrm{LO}}}\right) T_{\mathrm{ON}} \cdot sinc^2\left(\pi f\left(\tau_r - \beta\right)\right) \tag{A.16}$$

Finally, putting this result in the $G_C(t)$ expression reported in (A.8), its Fourier transform with a triangular waveform results

$$\mathcal{F}\left(G_C(t)\right) = G_{C,\max}\left(\frac{d^2}{\tau_r f_{\mathrm{LO}}}\right) \cdot sinc^2\left(\pi f\left(\tau_r - \beta\right)\right)\left(1 - e^{-j\pi f T_{\mathrm{LO}}}\right) \cdot \sum_{n=-\infty}^{+\infty} d(f - \frac{n}{T_{\mathrm{LO}}}) \tag{A.17}$$

A.3 Square waveform

The Fourier transform for a square waveform can be easily calculated using the same method. However is can be directly derived setting τ_r value equal to 0 into equation (A.11):

$$\mathcal{F}\left(S(t)\right) = G_{C,\max} \cdot \left(\tau + \tau_r\right) \cdot sinc\left(\pi f \tau_r\right) \cdot sinc\left(\pi f(\tau + \tau_r)\right) \tag{A.18}$$

and consequently the G_C Fourier transform built with this waveform become

$$\mathcal{F}\left(G_C(t)\right) = G_{\mathrm{C,max}} dsinc\left(\pi \frac{f}{f_{\mathrm{LO}}} d\right)\left(1 - e^{-j\pi \frac{f}{f_{\mathrm{LO}}}}\right) \cdot \sum_{n=-\infty}^{+\infty} d(f - n\, f_{\mathrm{LO}}) \tag{A.19}$$

Publications

Journal

- A.Magnani, M.Borgarino, C. Viallon, T. Parra, G. Jacquemod "A Low Power Ku Phase Locked Oscillator in Low Cost 130 nm CMOS Technology", Microelectronics Journal, 2014, 45 (6), pp.619-626

Conferences

- A. Magnani, C. Viallon, I. Burciu, T. Epert, M. Borgarino and T. Parra "A K-band BiCMOS Low duty-cycle Resistive Mixer" *IEEE Radio and Wireless Week, SiRF 2014*, January 2014

National Conferences

- A. Magnani, P. Lucchi, T. Parra, G. Jacquemod, M. Borgarino "A Phase Noise Performance Study of 15 GHz Phase Locked Loop in 130nm CMOS Technology for DVB-S Application", *In SAME - Sophia Antipolis MicroElectronics forum*, Sophia Antipolis (France), October 2012
- A. Magnani, T. Epert, C. Viallon, M. Borgarino, T. Parra "Convertisseur de fréquences BiCMOS en bande K basé sur un mélange passif à faibles pertes", *JNM2013*, May 2013

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