

Cost Effective Mask Design in CMOS Transistor Fabrication for Undergraduates Program

M. Morsin¹, R.Sanudin², M. Elias³, M. Z. Sahdan⁴ and M.S. Sulong⁵

Abstract— This paper presents a new innovative way of teaching undergraduate program using low cost masks. In MOSFET fabrication, the cost to produce a complete mask set for pattern transfer process is extremely high and not cost effective for undergraduates program. The purpose of these masks is to define certain functional region on a wafer. In this work, low cost masks have been fabricated with a simple technology. An economical solution of masks using transparency films with various channel lengths from 300 μm to 500 μm has been produced. Six layer photolithography masks of MOSFET were designed using AutoCAD drawing tools and then printed using high resolution laser printer on the transparency film. Contact printing method has been utilized to transfer the mask layouts onto a 4-inch silicon wafer using standard photolithography techniques to check the line uniformity. Optical observation using high power microscope shows that the mask layouts were successfully transferred onto photoresist with minimum variation. These masks are used to fabricate an n-well CMOS transistor and then tested using Keithley 2400 source meter with Lab-view measurement software. The cost effective mask design proposed was really practical for teaching microfabrication undergraduates program.

Keywords: AutoCAD, Mask fabrication, Metal Oxide Silicon Field Effect Transistor (MOSFET), Transparency film.

I. INTRODUCTION

In IC fabrication process, there are many steps involved such as photolithography, oxidation, diffusion and metallization. Photolithography is used to transfer a designated pattern onto a wafer [1], [2]. This process is similar to the process of transferring an image from a camera film onto a photo paper.

However, in photolithography process, several masks will be required to transfer the device pattern onto the wafer. Unfortunately, the masks available in market are really expensive and not practical for teaching purposes [1], [3].

An economical solution was developed to substitute the expensive masks to a low cost masks using simple technology. Hence, six level masks were designed with various channel lengths from 300 μm to 500 μm using transparency film [1], [4].

The masks were designed using AutoCAD 2002 and printed onto standard transparency using high resolution Hewlett Packard printer. This simple mask design and generation procedure allows process flexibility at minimum cost. This low cost mask design is very suitable for education, research purposes and fabrication process.

II. MASK DESIGN AND CREATION

The n-well CMOS process flow being developed is tailored for the processing of 4-inch wafer in the UTHM cleanroom. The process flow consists of total 56 process steps including process measurements. The flow starts with definition of starting wafer, followed by photolithography, diffusion, etching, and metallization steps.

M.Morsin, R. Sanudin, M.Z.Sahdan, and M.S Sulong are with Faculty of Electrical and Electronic Engineering, University of Tun Hussein Onn Malaysia, 86400 Parit Raja, Batu Pahat, Johor, Malaysia, Tel:07-4537524, Fax:07-4536060, (e-mail: marlia, rahmats, zainizan, msuhaimi}@uthm.edu.my)

M.Elias is a M.Eng's student at University of Tun Hussein Onn Malaysia, 86400 Parit Raja, Batu Pahat, Johor, Malaysia, (e-mail:mariza_iejaja@hotmail.).

For photolithography process, the process development of CMOS transistor started from mask design. Figure 1 show all the six masks of n-well CMOS transistor integrated together. There were a total of six photolithography masks. There were 3 set of masks with various channel length comprised of 300 μm , 400 μm and 500 μm .

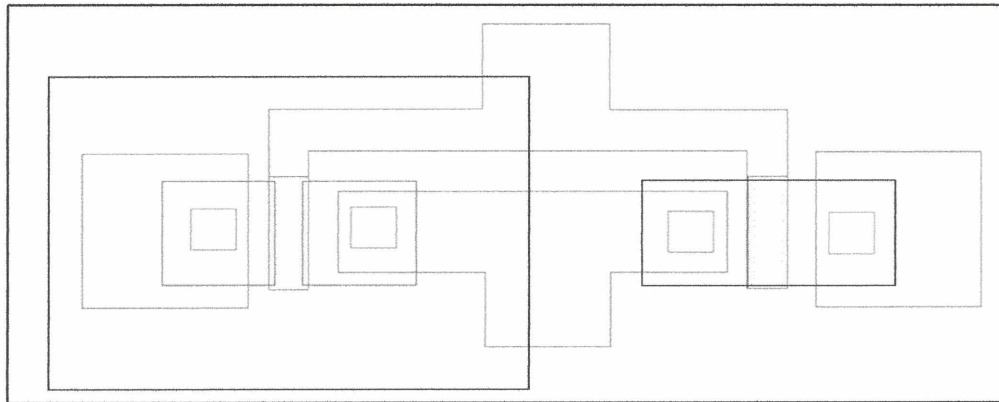


Figure 1: Integrated n-well CMOS transistor

The photolithography masks were designed by using AutoCAD 2002 drawing tools. These masks were printed on transparencies film using high resolution Hewlett Packed Laser Printer. The steps of designing mask set are depicted in figure 2.

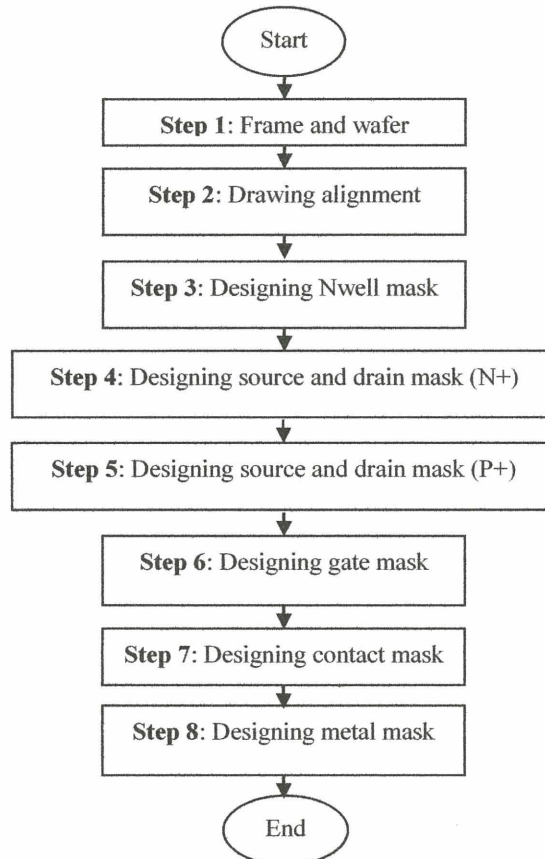


Figure 2: The steps of mask design

The first step is designing size of the frame and wafer. The sizes of the frame and wafer diameter are 150 millimeter x 150 millimeter and 100 millimeter. The second step in producing the mask was drawing the alignment mark. This alignment mark is used as a reference for alignment between layers. The alignment mark shown in figure 3 (a) was designed for the first mask. The dark field would leave cross island on the wafer after lithography process. This island would act as an indicator for the following masks in the alignment process. Figure 3 (b) shows the mark design for mask 2 to mask 6. The cross is made bright, while the outer cross is made dark. It is simply to make a window transparent so that alignment can be made by looking the cross island through the window.

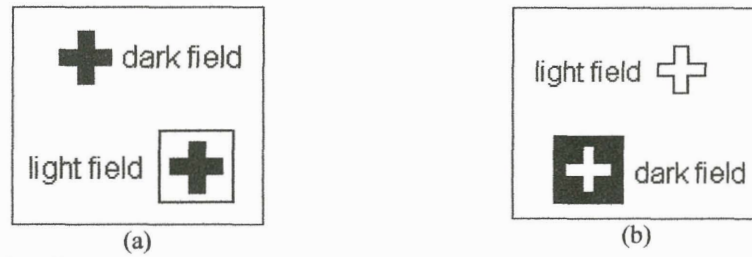


Figure 3: Alignment mark; (a) mask 1 (b) mask 2, mask 3, mask 4, mask 5 and mask 6

The third step of designing the CMOS transistor was designing nwell mask to separate the NMOS and PMOS transistor. The nwell diameter is designed to $8500\mu\text{m} \times 6000\mu\text{m}$ on the mask as shown in figure 4 (a).

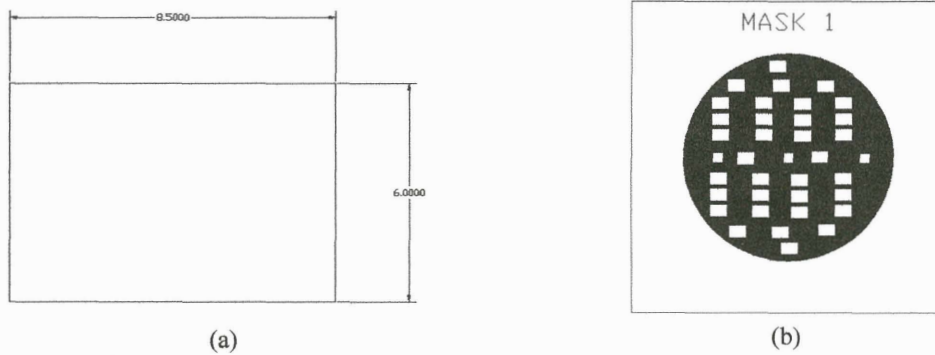


Figure 4: (a) Dimension of Nwell (b) Layout impressions of Nwell mask CMOS transistor on silicon wafer.

The fourth and fifth steps were designing the source and drain (SD) region. The SD region was designed in the p substrate as depicted followed with designing the SD region in n substrate. The channel length is varied from $300\mu\text{m}$, $400\mu\text{m}$ and $500\mu\text{m}$ for both NMOS and PMOS as shown in figure 5(a). Figure 5(b) and (c) show the source and drain mask for both N+ and P+.

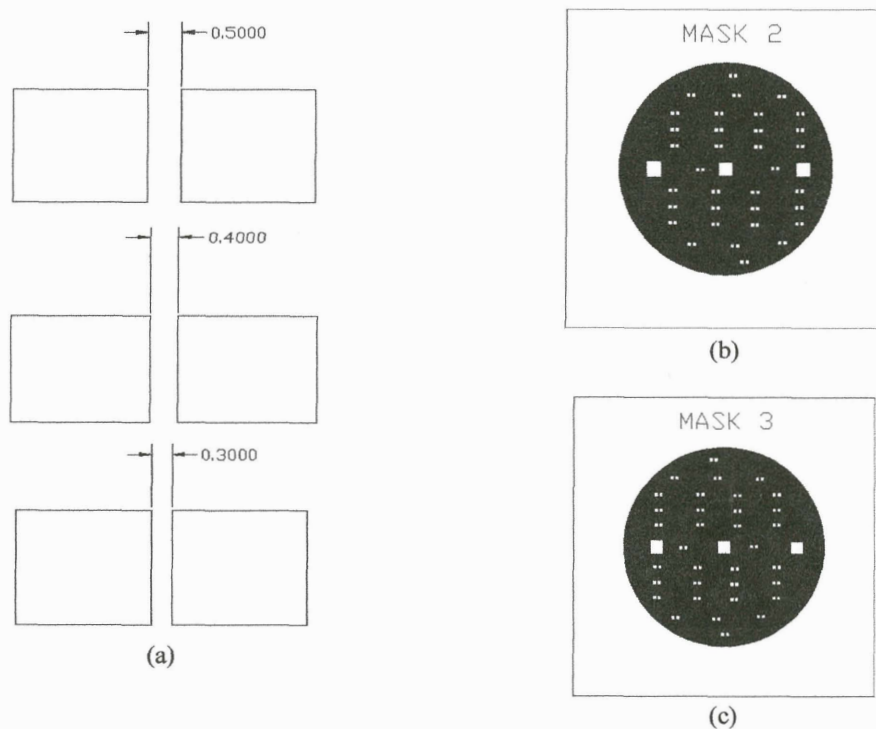


Figure 5: (a) Dimension of three (3) different channel length of CMOS (b) Layout impressions of (b) source and drain (N+) (c) source and drain (P+) mask CMOS transistor on silicon wafer.

The next step is designing the gate length which is same length as the channel. The gate mask is depicted in figure 6. The sixth step in this mask design was to create the contact hole mask as shown in figure 7 (a). The dimension for the entire contact region is $800\ \mu\text{m} \times 800\ \mu\text{m}$.

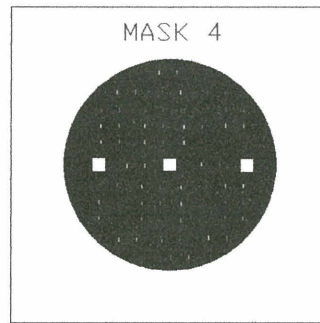


Figure 6: Layout impressions of gate mask CMOS transistor on silicon wafer.

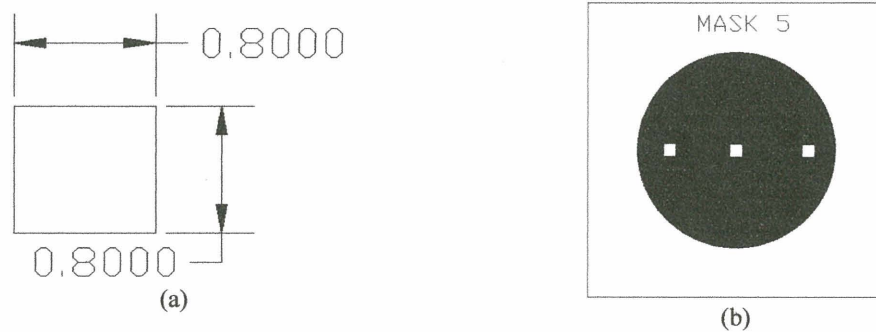


Figure 4: (a) Dimension of Nwell (b) Layout impressions of Nwell mask CMOS transistor on silicon wafer.

The final step of mask design was creating the metallization mask. This mask is designed to create a routing for contact and gate to probing pads. The dimension of the pad is $1\text{mm} \times 1\text{mm}$. The metallization mask pattern on transparency film is shown in figure 8.

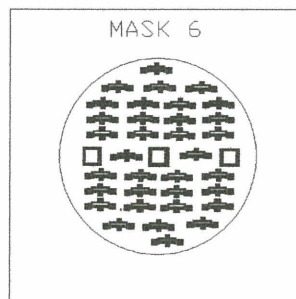


Figure 8: Layout impressions of metal mask CMOS transistor on silicon wafer.

All the masks produced are used in photolithography process to transfer a complete CMOS pattern using photoresist to define source drain region, gate region, contact hole and Aluminum routing.

III. RESULT AND ANALYSIS

After the photolithography process, the pattern is transferred one after another onto the wafer to produce CMOS transistor. The image of the patterned after utilizing the masks has been captured using high power optical microscope. The critical stages are step 4 and 5 which are transferring source and drain pattern onto the wafers. It is hard to do because of the source and drain in P+ and N+ are difficult to place manually using mask aligner system. It requires very clear and precise observation and repeated many times before the desired patterns are obtained. The observation after pattern transferring for each stage is shown in figure 9 (a)-(f).

The photolithography process consist of several repeated steps which are resist coating, soft bake, align expose, develop and oxide etching. For metal masking there is a difference in its final step namely metal etching. The solution used in metal etching is ALUM Etchant. Figure 9 (a) shows the image of nwell region after nwell masking process. The image taken is after oxide etching. The light grey area is an oxide layer for nwell region. Figure 9(b) shows the whole wafer after mask 1-nwell masking. Figure 9(b) depicted the images of source and drain region (N+) after photoresist strip. The source and drain region are successfully transferred onto the wafer.

Figure 9(c) depicted the images of source and drain region (N+) after photoresist strip. The transferred pattern shows the P+ source and drain in rectangle shape. Figure 9 (d) shows the image of gate region after etching process. The region on the center is the high quality gate oxide while the outer region is the thick oxide layer. The gate region is placed in between source and drain region. Figure 9 (e) shows the image of contact region after oxide etching. The contact region is in the center of image taken with square dimension. This contact is placed inside source and drain region for both N+ and P+ and act as a route for metal.

After metallization process completed, the aluminum routing is formed as shown in figure 9 (f). The bright region is the aluminum region while the dark region is the oxide layer. The problems occurred in the metal masking process were some of the metal was not properly placed in the desired position. It touched the unwanted region such as the metal on the gate also contact the metal on the source or drain region. This error affected the devices performance and the short circuit problem will occurred if the voltage is supplied to the devices. Because of that, the metal masking process must be repeated to get the required pattern.

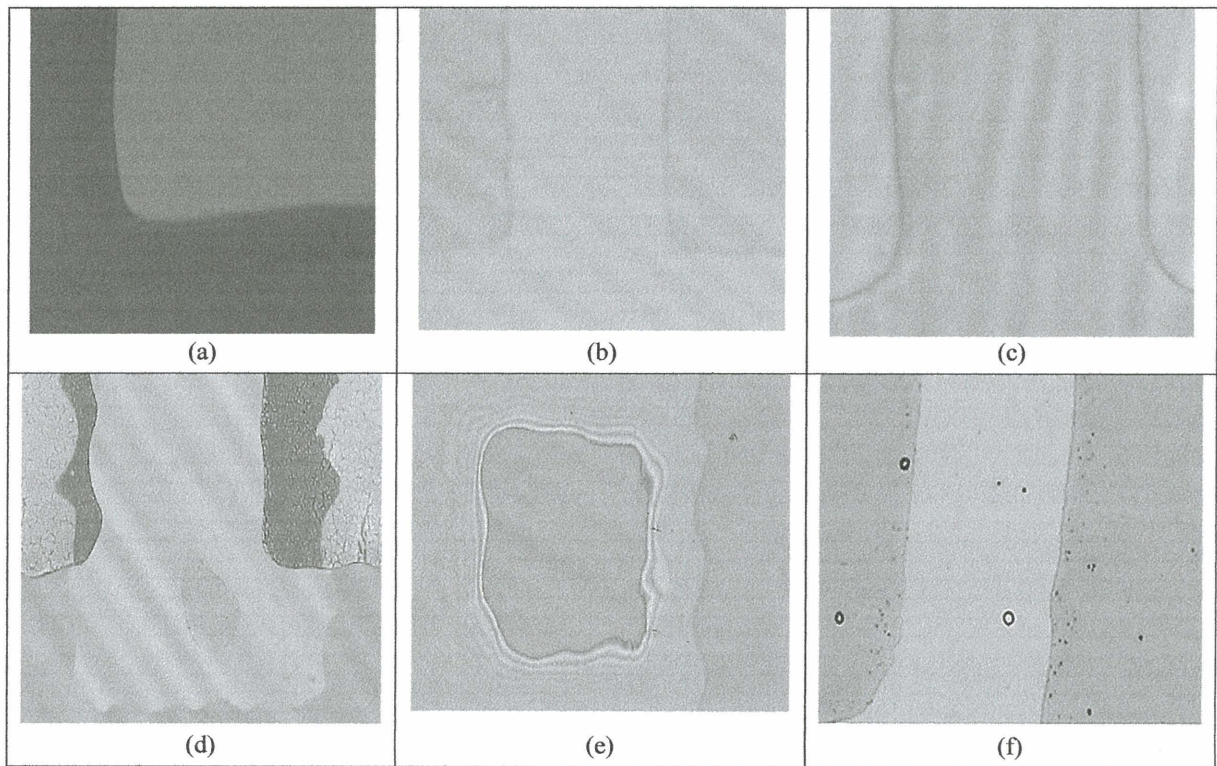


Figure 9: Images of CMOS transistor after fabricated using 6 masks. (a) Nwell region (b) source and drain region (N+) (c) source and drain region (P+) (d) gate region (e) contact region (f) metallization region

After the CMOS transistor has been fabricated, the device was then tested to check the IV characteristic using electrical probe station and device characterization software. The result obtained shows that the source-drain voltage, V_{DS} starts at 1 Volt and stop at 10 Volt.

IV. CONCLUSION

In microelectronic fabrication, the industrial way of producing mask sets are very expensive and not cost effective for teaching undergraduates. The concept of utilizing transparency film is an alternative to the mask making and significantly reduces the cost of mask design. Although the process has its limitation in producing structures of an order of magnitude smaller than described, it is sufficient for essential electrical characterization work. In this manner, the student will be more flexible to design a circuit and allow them to fabricate their own device.

V. REFERENCES

- [1] M. Sahdan, Uda Hashim, Hashim Saim, M.Morsin., "Cost Effective Mask Design for Undergraduates Program", *Journal of Solid State Science and Technology Letters*, Vol. 13 No. 1, Jan. pp 2006.
- [2] Hsiang, W. L, Yit P. K, Abdul Aziz, A., "Mask Fabrication and Photolithography in 30um Process", *National Physics Conference 2003*, pp. 61-61, 2003.
- [3] Johnson C. and Ula, N., "Incorporating Computer Aided Device and Process Simulated Tool in Undergraduates Course", *Department of Electrical Engineering and Computer Science, Loyola Marymount University, 2003*
- [4] David, T. G., Timmons, C. and Robert W. H., "Process Development for Undergraduate Microchip Fabrication Facility", *American Society for Engineering Education Annual Conference & Exp.*, 2001