NASA SP-6507

PARTS, MATERIALS, AND PROCESSES EXPERIENCE SUMMARY

Volume II

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

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FOREWORD

Scientific and engineering organizations within the National Aeronautics and Space Administration, the Department of Defense, and throughout the aerospace industry are greatly concerned about the impact of system failures related to parts, materials, and processes. Establishment of the NASA ALERT reporting program in 1964, expanded in 1968 to include participants of the Government-Industry Data Exchange Program (GIDEP), provided the means for sharing and benefiting from each other's experience with these types of failures. Extensive data accumulated from ALERT reports have proved a valuable method of communicating problems and providing assistance in avoiding or minimizing recurrences.

In order that this accumulated experience be made readily available, this publication, *Parts, Materials, and Processes Experience Summary*, condenses and catalogs ALERT and other information on basic design, reliability, quality and application problems. Designers, engineers, failure analysts and other reliability and quality personnel will find the answers to many application and problem-avoidance questions.

This publication was developed under contract NAS2-6060 by the Lockheed Missiles & Space Company, Inc., Sunnyvale, Calif., under the leadership of W.L. Finch, W. Geller, and S. Ognibene. The contract was administered under the technical direction of NASA's Ames Research Center, Moffett Field, Calif., with G.E. DeYoung as technical monitor. This effort and the significant assistance provided by the members of the NASA Parts Steering Committee are gratefully acknowledged.

This issue of the *Summary* is a revision of CR-114391, Feb. 24, 1972. It includes, new, expanded, and revised material reflecting additional NASA experience and responses to the questionnaire sent to Government and industry personnel.

It is expected that this summary will be revised periodically to disseminate new and expanded information on existing topics and possibly new topics. Any suggestions or recommendations that will enhance its usefulness will be most welcome and should be referred to the Office of Safety and Reliability and Quality Assurance, NASA Headquarters, Washington, D.C. 20546.

GEORGE C. WHITE
Director, Safety and Reliability
and Quality Assurance

INTRODUCTION

OBJECTIVE

The objective of this *Parts, Materials, and Processes Experience Summary* is to provide the general engineering community with the accumulated experience from ALERT reports issued by NASA and the Government-Industry Data Exchange Program (GIDEP), and related experience gained by Government and industry. It provides expanded information on selected topics by relating the problem area (failure) to the cause, the investigation and findings, the suggestions for avoidance (inspections, screening tests, proper part applications, requirements for manufacturer's plant facilities, etc.), and failure analysis procedures.

ALERT PROGRAM

The ALERT program is a system for communicating common problems with parts, materials, and processes. The ALERT program has as its basic objective the avoidance, or at least the minimization, of the recurrence of parts, materials, and processes problems, thus improving the reliability of equipment produced for and used by the Government. An ALERT report is prepared when an item is believed to be in common usage and the problem may affect other users; copies are distributed to all participants in the ALERT program.

Information on the ALERT program may be obtained from the Office of Safety and Reliability and Quality Assurance, NASA Headquarters, Washington, D.C. 20546 (phone 202-755-2284); or from the GIDEP Administration Office, Fleet Missile Systems Analysis and Evaluation Annex, Code 862, Naval Weapons Station, Seal Beach, Corona, Calif. 91720 (phone 714-736-4677; Autovon: 933-4677).

ORGANIZATION OF SUMMARY

This two-volume publication is divided into 18 sections, one of which is a miscellaneous category. The other sections represent 17 major topics derived from the GIDEP major classification code. The GIDEP code number is shown on each section divider to assist in obtaining related data from test and qualification reports on parts and materials, scientific reports, technical information, manufacturing techniques, and specifications contained in the GIDEP file. Each section presents fundamental concepts followed by problems that have been experienced and suggestions for their avoidance; guidelines for producing good parts and materials; and procedures for determining why a failure occurred. Introductory remarks and a table of contents precede each section.

The 17 major topics (attaching methods, capacitors, transistors, etc.) were selected because they represent 82 percent of the ALERT reports issued by NASA and GIDEP through Aug. 31, 1972. The remaining reports are included through the medium of ALERT summaries in the miscellaneous section of Volume I.

ALERT ITEM NO.

Where appropriate within a section, each ALERT report has been assigned an "ALERT ITEM NO." in order to provide a cross reference between an ALERT referenced in the Problem/Screening Summary subsection and the same ALERT shown in the ALERT Summaries subsection.

CODE FOR PROBLEM AREAS AND CAUSES

Some sections employ a coding system to identify the major problem areas and their causes. The code is entered in the Problem/Screening Summary subsections, on the assembly flow diagrams, and on the failure analysis flow diagrams. A separate foldout (Problem Codes and Definitions) defines the code used in a particular section of the publication. All foldouts are located in the appendix. The coding system ties together the problem area/cause, the preventive action, the critical process during assembly, and the failure analysis step. For instance within Section 3 (Capacitors), ALERT Item No. 7 in the Problem/Screening Summary subsection indicates a "Short" as the problem area, with the cause being "Breakdown of dielectric." Also shown are the suggested screens that should detect the problem area/cause. The foldout for Section 3 (Capacitors) establishes the problem code of the area/cause as "IID." This code in the Ceramic Capacitor–Typical Assembly Flow with Related Problem Codes diagram (fig. 3-2) indicates that "thin spots and contamination" during the "slip cast dry and roll green stock" operation can eventually cause a short because of dielectric breakdown. In a similar manner, the Ceramic Capacitor–Failure Analysis Flow with Related Problem Codes diagram (fig. 3-3) shows that the problem area/cause can be detected at the "radiographic inspection," or at the "depotting and examination" or the "dissection and examination" stages of the failure analysis procedure. The two diagrams can also be used in other ways. Possible problem areas/causes are depicted for any stage in the assembly operation, thus facilitating the creation of a process control check-off list. If the problem area is known, possible causes are shown for any stage in the failure analysis procedure.

REFERENCES

The title and responsible agency for a military standard or specification, or for a NASA special publication or handbook, are given in the list of references located at the back of the publication.

KEYWORD INDEX

Keyword indexing is provided in order to facilitate easy search and reference; e.g., an ALERT report for a particular relay may contain the words: "relay," "contamination," and "solder." Looking up those words in the index will lead to that particular relay problem; the words "contamination" or "solder" will also lead to other ALERT reports on other types of parts.

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SECTION 16
DIODES
(GIDEP CODE 741)

CONTENTS

INTRODUCTION

OBJECTIVE

The objective of this section is to identify the major problem areas associated with the use of semiconductor diodes and to suggest approaches (developed from experience) for dealing with those problems.

SECTION ORGANIZATION

The diode section is presented with the following organization:

General

1. Basic failure problems associated with diodes are identified based upon ALERT and industry experience.

2. Where applicable, a screening technique is suggested for detecting finished parts having a potential for failure.

Subtopics - Treatment of Specific Types

1. Diode type background.

2. A portion is devoted to describing the construction and manufacture of diodes as an aid in the selection of parts and manufacturers. Particular emphasis is placed on those design and manufacturing anomalies associated with identified diode failure mechanisms.

3. Basic failure analysis techniques are provided as an aid in developing a competent failure analysis plan where corrective action at the part level is required. The material is so arranged that a specific problem can identify those steps in the failure analysis process most likely to reveal that problem.

Diode Types. Diodes have been divided into subtopics according to their function. Rectifier and switching, zener, and RF diodes have been discussed in depth. Other subtopics dealing with silicon controlled rectifiers, varactor diodes, etc., include only summaries of ALERT reports.

DIODE FUNDAMENTALS

What a Diode Should Do. The diode is a two-terminal electrical device offering low resistance to current flow in one direction and high resistance to current flow in the other direction. In its simplest form a diode consists of two layers of semiconducting material with impurities purposely introduced such that one layer (the N-type) has an excess of electrons, and the other layer (the P-type) has a deficiency of free electrons. (A deficiency of free electrons may be thought of as an excess of free positive charge.) If a potential is applied across the junction between the layer such that resultant electric field passes from the P-type to the N-type layer, the free charges are urged toward the junction where they neutralize each other and a current flows. If the field is reversed, the charges are urged away from the junction and no current flows. Modern junction diodes take the form essentially as described. Older types (point contact, copper-cuprous oxide, selenium-iron, selenium-aluminum) are more complicated in form, although often simpler to build, operate on essentially the principle described above. The operating characteristics of germanium and silicon diodes are determined by: doping, diffusion temperature, diffusion time, die size, packaging, etc.

Practical Considerations. As in all devices, the design of a diode to perform a given function requires a series of compromises. An improvement in one design parameter (e.g., forward conduction) is accompanied by the deterioration of another design parameter (e.g., reverse breakdown). In considering design compromises, one is faced with the parasitic effects of: capacitance, reverse leakage current, forward voltage drop, and temperature. It is only by recognizing and controlling all factors that reliable diodes can be developed and manufactured. Most diode characteristics (be they design or parasitic) are established by the type of diode being built, the intended application, and the resultant package.

FAILURE MODES

Failure Categories. Part level failure problems associated with diodes may be lumped under four basic categories: catastrophic opens, catastrophic shorts, electrical parameter deviation, and external mechanical anomalies. It must be recognized that catastrophic opens and shorts are worst-case conditions of certain electrical parameter deviations.

False Failed-Equipment Indicators. At the equipment level, high forward voltage drop can appear to be an open, and high reverse leakage current may appear to be a short. A failure mechanism producing an apparent open or short (e.g., a parameter deviation), in its extreme condition, becomes an open or a short. Only failure analysis on the piece part level can distinguish between these conditions and result in corrective action.

ELIMINATING DEFECTIVES

Problem Solving Approach. The approach taken in this section will be to identify the user-encountered problem areas associated with a particular type of diode, then provide suggestions for eliminating those diodes prone to exhibiting those problems at the finished diode level, the design level, and at the manufacturing level.

Finished Diode Level. Realizing that most consumers use finished diodes that are on hand, information is provided on screening of the devices, that is, sorting the bad diodes from the good ones. Suggestions are made as to environmental and electrical testing which will identify defective units while having no deleterious effects on good units. This technique is used not only for sorting but for providing assurance that the manufacturer has controlled his processes.

Design Level. While screening has proven capable of providing good diodes, it does not provide a solution to the problem of design compromises and/or design deficiencies. Certain design compromises cannot be avoided; however, reliable equipment can be built if allowance is made in the equipment design to minimize the effect of these compromises. Design deficiencies, wherever encountered, must be identified and eliminated.

Manufacturing Level. The most carefully conceived design and the best of parts can amount to nought if manufactured in an environment lacking necessary controls over materials, processes, and workmanship. As no screening is 100 percent effective in removing defective parts, it is more desirable to correct manufacturing anomalies through the use of adequate controls and inspection points.

FAILURE ANALYSIS

Objective. The primary objective of failure analysis is to identify failure mechanisms at a level such that corrective action can occur. Knowing that a diode is open is of no consequence in that corrective action is not possible. Knowing that a diode is open because of a defective bond allows for correction of future bonding operations and the elimination of that problem cause.

Failed Part Rarity. A part in a failed condition must be considered a "once-in-a-million" occurrence, a phenomenon which may never again occur. It is only by using this premise that successful failure analysis can be performed.

Failure Verification. After recording all identifying external markings, visually inspecting, photographing identification and damage, and radiographically inspecting, the first requirement is to verify the failure. Too often the wrong part is removed from the circuit or an equipment test error, rather than a part failure, results in a good part being delivered for failure analysis. Many times the actual part failure is different from that specified, as such, a note of this fact must be made.

Analysis Direction. The process of analyzing a failure, performing those steps necessary to identify a specific correctable failure mechanism, requires the coordination of one having a knowledge of failure mechanisms, diode design, and diode manufacturing techniques; and the ability to form a practical plan of action.

When to Analyze. In many cases diode failures occur for which device corrective action is not required, however, in almost all cases some form of corrective action is necessary. Corrective action can be required of circuit designers, assembly manufacturers, test organizations, etc., as well as on parts. As such, it is suggested that very strong cause must exist before failure analysis is abbreviated or foresaken.

Reliability/Life. It is anticipated that as a result of screening, analysis of design and manufacturing, and effective failure analysis (all at the part level), that significant improvement in reliability and life will be realized.

PROBLEM/SCREENING SUMMARY

Scope. The problem summation presents the cause and effect of failures and suggests action to be taken to identify and screen out devices with latent or incipient defects. This summary is an accumulation of information and experience obtained from working with diode failures and in avoiding those failures.

This summary is intended to identify diode problem areas and problem causes. Having identified the problems, suggestions are made for the elimination of problem parts on hand through the use of recommended screening tests derived from industry experience. Problem areas have been grouped under the basic categories of open, short, parameter deviation, and mechanical anomaly.

ALERT Item No. Where directly applicable, the "ALERT Item No." of the ALERT report describing a specific cause for a failure is listed against that cause. Thereby, a cross reference is provided between a specific failure cause found in the "ALERT Summaries" and the broader failure experience/avoidance knowledge shown in this presentation.

Misapplication. Experience has shown that the major cause of diode failure has been misapplication. However, the most frequent failure mode attributable to the parts themselves is open.

PROBLEM AREA/CAUSE AND SUGGESTED ACTION

RECTIFIER AND SWITCHING DIODES

PROBLEM AREA/ Cause	ALERT ITEM NO.	SUGGESTED ACTION - SCREEN (see "Screening Inspections and Tests")
OPEN Inadequate bonds Chip lifted	1 2, 3, 4, 5, 6	High Temperature Storage, Thermal Shock, Acceleration, Burn-In, and Electrical Testing
SHORT Lack of hermetic seal	7	Hermetic Seal, Electrical Testing, and Visual Examination - Internal (cavity types only)
SHORT Conductive contamination	8	Acceleration, Electrical Testing, X-ray, and Visual Examination - Internal (cavity types only)
ELECTRICAL PARAMETER DEVIATION Contamination	9	High Temperature Reverse Bias Test, Hermetic Seal, Electrical Testing, and Visual Examination - Internal (cavity types only)
MECHANICAL ANOMALY Hydrofluoric etchant	10	Visual Examination - External
MECHANICAL ANOMALY Defective weld	11	High Temperature Storage, Thermal Shock, Acceleration, Burn-In, and Electrical Testing

ZENER DIODES

PROBLEM AREA/ Cause	ALERT ITEM NO.	SUGGESTED ACTION - SCREEN (see "Screening Inspections and Tests")
OPEN Inadequate bond	12, 13	High Temperature Storage, Thermal Shock, Acceleration, Burn-In, Electrical Testing, and Visual Examination - Internal (cavity type only)
SHORT Conductive contamination - Internal (cavity type only)	14, 15	Acceleration, Electrical Testing, X-ray, and Visual Examination - Internal (cavity type only)
ELECTRICAL PARAMETER DEVIATION Incorrect guard band limits	16	Electrical Testing
ELECTRICAL PARAMETER DEVIATION Contamination	17	High Temperature Storage, High Temperature Reverse Bias Test, Burn-in, and Electrical Tests
MECHANICAL ANOMALY Improperly formed weld	18	Visual Examination - External

ZENER DIODES

PROBLEM AREA/ Cause	ALERT ITEM NO.	SUGGESTED ACTION - SCREEN (see "Screening Inspections and Tests")
MECHANICAL ANOMALY Oxidation of Dumet copper	19	Acceleration, Electrical Testing, X-ray, and Visual Examination (cavity type only)
MECHANICAL ANOMALY Shrinkage of die bond material	20	Thermal Shock, Acceleration, Burn-In, Electrical Testing, X-ray, and Visual Examination (cavity type only)

MISCELLANEOUS DIODES

TYPE	PROBLEM AREA/ Cause	ALERT ITEM NO.	SUGGESTED ACTION - SCREEN (see "Screening Inspections and Tests")
OPTOELECTRONICS	MECHANICAL ANOMALY Freon TMC	21	Visual Examination - External
SCR	OPEN Inadequate bond	22	High Temperature Storage, Thermal Shock, Acceleration, Burn-In, and Electrical Testing
SCR	ELECTRICAL PARAMETER DEVIATION Contamination	23	High Temperature Storage, High Temperature Reverse Bias Test, Burn-In, and Electrical Testing
SCR	MECHANICAL ANOMALY Poor lead plating	24	Visual Examination - External
VARACTOR	OPEN Mechanically overstressed	25	Overstressing of parts should be avoided. If required in application, screening should incorporate that requirement
VARACTOR	SHORT Contamination	26	High Temperature Storage, Thermal Shock, Acceleration, Burn-In, Electrical Testing, X-ray, and Visual Examinations - Internal (cavity type only)

SCREENING INSPECTIONS AND TESTS

Screening inspections and tests for rectifier, switching, and zener diodes are very similar. Differences (electrical parameter measurements) are shown in the descriptions of the individual tests.

Basic Screening. The screening inspections and tests suggested for diodes included in the "Problem/Screening Summary" are as follows:

1. Visual Examination - Internal (cavity types only)
2. High Temperature Storage
3. Temperature Cycling
4. Acceleration
5. Seal Test (for cavity types only)
6. Electrical Measurements (Pre-Burn-In)
7. Burn-In; sometimes called "Operation Stabilization"
8. Electrical Measurements (with "Delta" criteria)
9. Radiographic Inspection (cavity devices only)
10. Visual Examination - External

Objective. The purpose of the screening is to allow detection of parts that: (1) have been improperly processed by the manufacturer, (2) contain flaws or weak spots (including voids and contamination), (3) have poor solder or weld connections, or (4) have any other anomalies that could result in a failure under normal operating conditions.

Additional Screening. In cases where specific characteristics are critical in the function of the using equipment, those parameters should be added to the screening requirements.

Envelope Removal/Dissection. The basic approach taken here is to subject each of the devices to a test procedure in order to make a one-by-one acceptance determination. The disadvantage of this approach is the underlying assumption that the internal construction materials, processes, etc. from part-to-part are homogeneous so that the devices can be treated as a uniform lot. If the devices are not produced under similar design criteria and manufacturing controls which permit a heterogeneous lot to exist, a single screening procedure may not be the optimum for all units. For this reason, it is frequently desirable to examine the internal design and construction. This is accomplished, first, by a nondestructive radiographic inspection; and second, by performing a destructive envelope removal or dissection on a limited sample of devices. This procedure is more meaningful if a design/construction baseline has been established as a comparison criterion.

1. VISUAL EXAMINATION - (INTERNAL)

   This test should provide for inspection of transparent, cavity type diodes for internal construction anomalies and extraneous matter. Inspection should be made after sealing and prior to painting.

2. HIGH TEMPERATURE STORAGE - MIL-STD-750, METHOD 1031 (ref 4)

   This test is normally performed at the absolute maximum high temperature rating of the device under test. The intent is the stabilization of electrical characteristics. The test has been used to detect problems with contamination, die bonds, lead bonds, metallization, oxide, and bulk wafer properties.

   Diode instability during high temperature storage testing would be revealed by high delta shifts in electrical characteristics - I_R and/or V_F for rectifier and switching; I_R for zener diodes.

3. TEMPERATURE CYCLING - MIL-STD-750, METHOD 1051 (10 CYCLES) (ref 4)

In this test, diodes are cycled from their highest rated storage temperature to their lowest rated storage temperature. Devices are stabilized for a minimum of fifteen minutes at each temperature extreme and transfer time, from one extreme to another, is minimized. Diodes should be cycled for a minimum of 10 cycles and would not normally be cycled for more than 20 cycles.

The intent of this test is to check the mechanical integrity of the package in that it would reveal problems with internal and external bonding techniques. Loss of mechanical integrity internally would be revealed by a high delta shift in electrical characteristics - V_F for rectifier and switching; BV and/or Z_z for zener diodes. Loss of external mechanical integrity would result in a loss of hermeticity with a subsequent inability to pass hermetic seal testing.

4. ACCELERATION - MIL-STD-750, METHOD 2006 (ref 4)

Acceleration is normally performed at 20,000 g force for one minute with the device mounted, with respect to the center of the centrifuge, such that the force generated would tend to separate weak chip bonds. Test conditions can vary considerably depending upon the type of case of the diode tested.

The intent of this test is to check the mechanical integrity of the diode. Internal integrity is determined by electrically testing - V_F for rectifier and switching; BV and Z_z for zener diodes. A high delta shift would indicate problems with the internal lead to chip bond or chip bond. Loss of external integrity is revealed by hermeticity problems during hermetic seal testing.

5. SEAL TEST (HERMETIC SEAL) - MIL-STD-750, METHOD 1071 (ref 4)

All cavity type diodes are subjected to hermetic seal testing in the form of fine and gross leak testing. Fine leak testing is normally performed by placing the diode in a chamber, reducing the atmospheric pressure, and backfilling with helium - in essence, attempting to pump out and replace the gas inside with helium. The part is then "sniffed" with a helium detector. This method can detect leak rates of less than 1×10^{-8} atm cc/sec.

Gross leak testing has been done by a number of methods, the latest of which is the use of liquid fluorocarbons at elevated temperature. If bubbles are seen to emanate from the diode, the device is rejected.

The test objective is to verify the external integrity of the diode by assuring that it has no hermeticity problems.

6. ELECTRICAL MEASUREMENTS (PRE-BURN-IN)

Electrical measurements shall be performed prior to submission of diodes to Burn-In. The objective of electrical testing is to eliminate devices which have failed previous screening tests. A more detailed description of electrical tests normally performed is presented in item 8 below.

7. BURN-IN - MIL-STD-750, METHOD 1026 (ref 4)

Power Burn-In of diodes is usually performed for 168 hours.

Rectifier diodes are normally biased for 60 cycle half-wave rectification. Switching diodes are usually reverse biased, I_R test condition, for burn-in. In both conditions, test current and external temperature are adjusted so as to maintain an absolute maximum rated junction temperature for the device being tested.

Zener diodes are either reverse biased at 80 percent of BV or at I_{ZT} for Burn-In. Test current/voltage and external temperature are adjusted so as to maintain an absolute maximum rated junction temperature for the device being tested.

The test objective of Power Burn-In is essentially the same as that of High Temperature Storage, that is, the stabilization of electrical characteristics. Once again, in bad parts Burn-In reveals problems concerning contamination, chip bond, lead bonds, metallization, oxide, and bulk wafer properties.

Diode instability during Power Burn-In is revealed in high delta shifts in electrical characteristics - I_R and/or V_F for rectifier and switching; BV and/or Z_z for zener diodes. In addition, burn-in stresses the internal mechanical construction of diodes. Loss of internal mechanical integrity is revealed by a high delta shift in electrical characteristics - V_F for rectifier and switching; BV for zener diodes.

8. ELECTRICAL TESTING

Electrical testing is essential in the determination of the quality of a diode. As has been shown in other screening tests, I_R and V_F on rectifier and switching diodes, or I_R, Z_z, and BV on zener diodes are those electrical tests required to verify the status of a diode. In addition to the above tests, certain other tests should be specified following Burn-In depending upon applications and/or minimum requirements.

The objective of electrical testing, aside from verifying specification requirements, is in determining delta shift. Delta shift is the amount that a measured electrical value has changed during an environmental test such as Burn-In, i.e., the amount of change between Pre- and Post-Burn-In electrical measurements.

The delta shift of diode electrical parameters is usually limited as follows:

Rectifier and Switching Diodes

ΔI_R = ±100% of the previous test value or ±10% of the specification limit, whichever is greater.[3]

ΔV_F = ±2.5 to 3% of the previous test value dependent upon the actual specification limit.[3]

Zener Diodes

ΔI_R = ±100% of the previous test value or ±10% of the specification limit, whichever is greater.[3]

ΔBV = 0.1.1% of the actual specification limit dependent upon tolerance of part being screened.[3]

ΔZ_Z = ±10% of initial value.[3]

Delta criteria should always be specified after Power Burn-In but can be useful before and after any individual screening test. In addition, 100 percent electrical testing should be performed prior to and immediately following completion of screening.

9. RADIOGRAPHIC INSPECTION - MIL-STD-750, Method 2079 (ref 4)

Radiographic inspection (X-ray) of cavity type diodes is normally performed on a 100 percent basis following completion of the previous screening tests. The intent of X-ray inspection is to detect conductive particles and internal construction anomalies which may affect the reliable operation of the diode.

10. VISUAL EXAMINATION - EXTERNAL

External visual examination is normally performed as the final screening test. This inspection is required to detect package defects, part marking defects, and external lead defects.

11. ENVELOPE REMOVAL/DISSECTION

A sample from each lot (e.g., lot-date-code) has its envelope removed and/or is dissected in order to detect internal anomalies such as part damage, poor workmanship, improper materials, etc. It is suggested that a sample base line dissected part be used as a standard for comparison.

NOTE:
3. Actual test value shall not exceed the specification limit.

RECTIFIER, SWITCHING, AND ZENER DIODES

CHARACTERISTICS

Semiconductor Characteristics. When considered as a group, rectifier, switching, and zener diodes are essentially the same, i.e., they all conduct current in one direction and block it in the other. In describing the differences in characteristics it can be said that switching and zener diodes can be used as rectifiers, but that rectifiers would not normally be used as switching and/or zener diodes, that is, an additional characteristic is required to describe a diode as either a switching or zener diode. A switching diode is a device with a specific ability, faster than normal, of switching from the forward to the reverse state and/or the reverse to the forward state. A zener diode is a device with a specified and controlled ability to block current in the reverse direction.

Package Characteristics. Generally speaking, it is difficult (without special package markings), to differentiate between rectifier, switching, and zener diodes of the same power rating by observing the package. However, with difficulty, certain zener diodes, having transparent packages, can be differentiated as they may have more than one chip. For this reason the next subsection (describing problem areas and causes found in diodes caused by design deficiency, lack of process control, and inadequate quality control) will contain a drawing for rectifier and switching diodes, and a drawing for zener diodes.

RECTIFIER, SWITCHING, AND ZENER DIODES

DESIGN AND PRODUCTION CONSIDERATIONS

Failures Related to Process. Typical rectifier/switching, and zener diodes (Figures 16-1 and 16-2) and typical assembly flows (Figures 16-3 and 16-4) are presented together with the suggested controls required to assure a reliable part. The "Critical Process" is defined for each of the manufacturing steps. Relationship is established between failure causes and the manufacturing process. Having experienced a specific problem, one could identify those manufacturing steps with potential for contributing to the failure.

TYPICAL RECTIFIER/SWITCHING DIODE DESIGN (Figure 16-1)

ITEM NO.	ITEM NAME	MATERIAL OF CONSTRUCTION
1	Leads	Dumet - MIL-STD-1276, Type D (ref 6)
2	Braze Joint	
3	Disk	99.99% copper clad with tin and gold
4	Die Bond Eutectic	Silicon-gold-tin intermetallic
5, 6	Chip	Doped silicon
7	Etched Mesa Portion of Chip	Etched and oxide passivated doped silicon
8	Metal Contact	Electroplated nickel
9	S-Bend Whisker	Electronic grade A nickel
10	Cathode Identification Band	External paint
11	Glass Body	Glass
12	Glass-to-Metal Seal Area	Note: Can be detected only with difficulty
13	Spot Weld Joint	

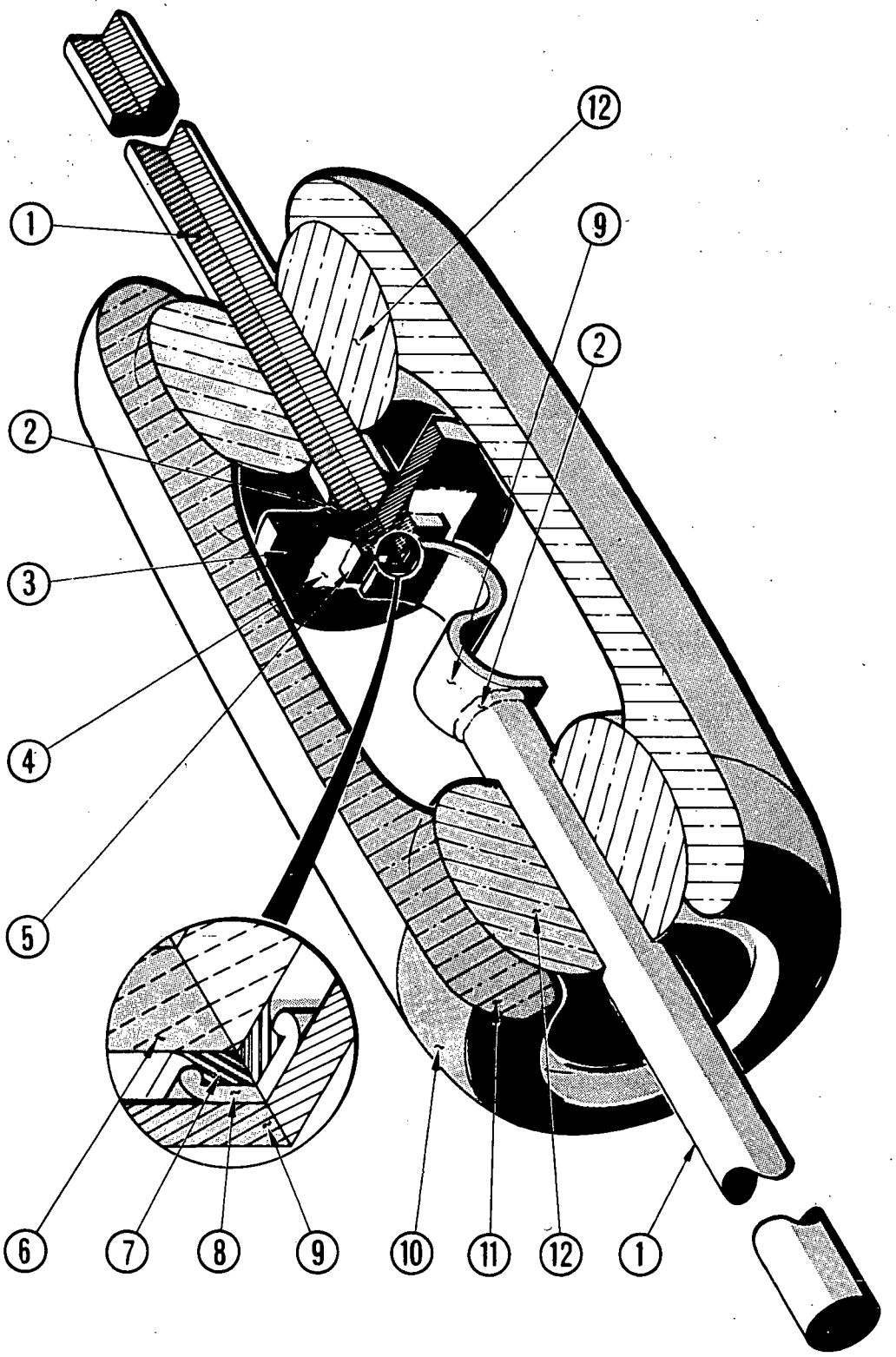


Figure 16-1. Typical Rectifier/Switching Diode

TYPICAL ZENER DIODE DESIGN (Figure 16-2)

ITEM NO.	ITEM NAME	MATERIAL OF CONSTRUCTION
1	Lead Wires	Dumet - MIL-STD-1276, Type D (ref 6)
2	Polarity Band	Thermosetting epoxy ink
3	Glass Wall and Second Seal	Glass
4	Weld Flash	
5	C Bend Whisker	Gold covered inconel embossed
6	Compensating Forward Dice	Silicon
7, 8	Solder Clad Nickel Disk	Nickel (cladding 95% lead, 5% tin)
9	Copper Sheath	Copper
10	Core	Nickel-iron
11	Weld Contact	Dumet
12	Reverse Dice	Silicon

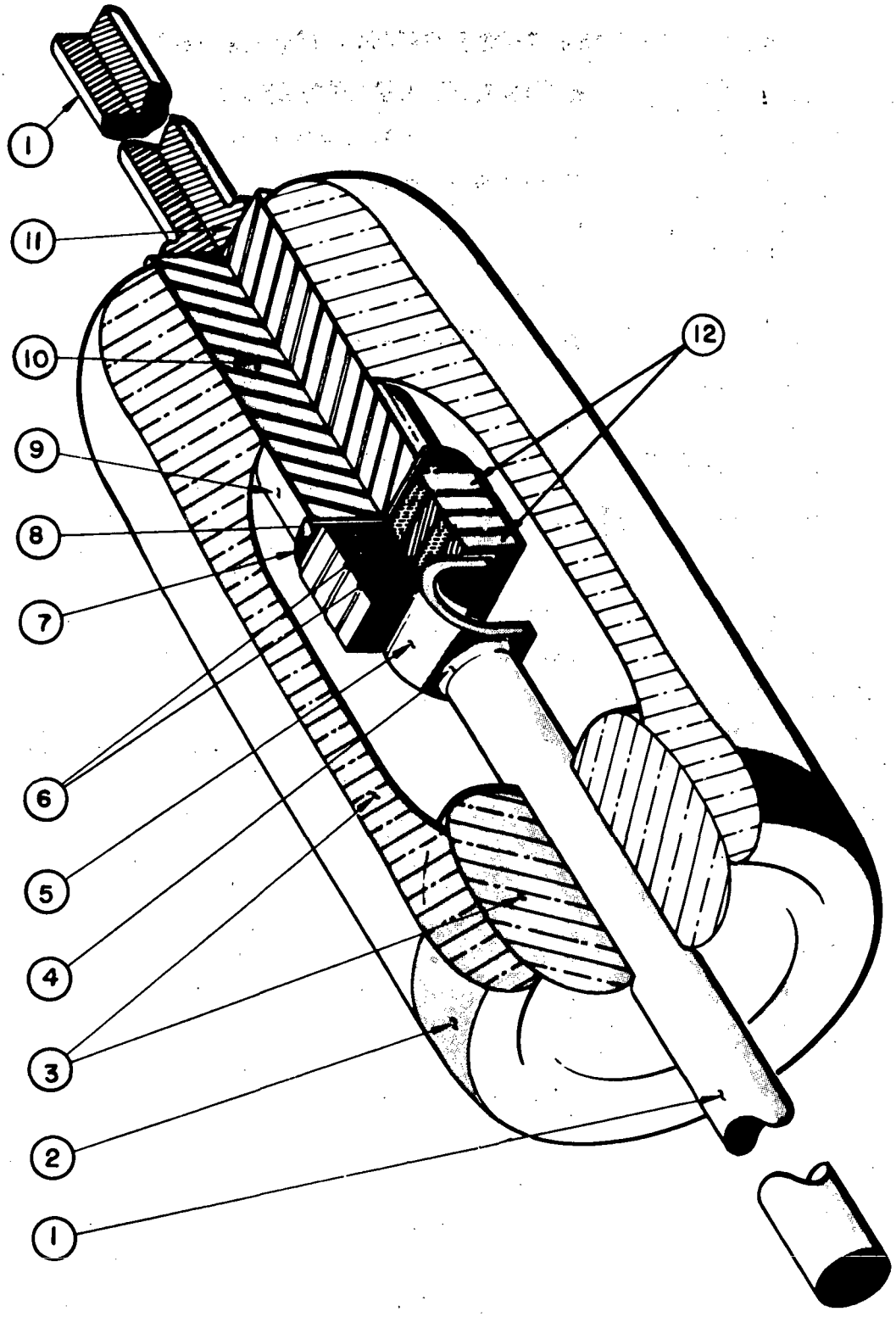


Figure 16-2. Typical Zener Diode

ASSEMBLY FLOW

General. Typical manufacturing flows for rectifier/switching and zener diodes (Figures 16-3 and 16-4) are presented together with the process name and the constituent added. Included in each typical manufacturing flow is a listing of the significant variable for each process - a significant variable is one which if not closely controlled will result in an inferior if not useless product. Circled numbers in the constituent added column are directly related to the circled numbers in the typical diode drawings and the item numbers in the materials list.

Assembly Precautions. Contamination, conductive and nonconductive, is the greatest cause of diode failure that is directly related to the assembly process. As such, one should assure that specific in-process inspection and testing be designed so as to eliminate and/or detect contamination.

The following is a partial list of the most probable sources of contamination:

1. Conductive Contamination
   a. Lead bonding processes (weld splash)
   b. Chip bonding process (loosely attached expulsion)
   c. Can-to-header welding process (weld splash) - metal-can devices only
2. Nonconductive Contamination
   a. Sealing process (moisture sealed in)
   b. Cleaning processes (corrosive chemical residue)
   c. Chip passivating process (contaminants in passivating material)

FLOW DIAGRAM			RELATED PROBLEM CODES (see foldout in the Appendix)			
MATERIAL	MANUFACTURING OPERATION	CRITICAL PROCESS	OPEN I	SHORT II	PAR DEV III	MECH ANOM IV
Wafer (5)	Clean wafer	Removal of contamination, and uniformity of finished surface		D4	A6, 7; B5	
Photo-resist	Photoresist deposition, spin, and bake	Uniformity of deposition, temperature, time, and cleanliness		D4	A6, 7; B5	
Mask	Mask alignment and exposure	Contact pressure and flatness, and exposure time		D4	A6, 7; B5	
Developer	Photoresist developing and bake	Development time, temperature, and atmosphere		D4	A6, 7; B5	
Etchant and Cleaning Compound	Etching and cleaning	Cleanliness and purity of materials and time		D4	A6, 7; B5	
Dopant	PN junction, dopant deposition and diffusion	Cleanliness, time, temperature, humidity, and furnace profile		D3, 4	A5, 6, 7; B5	
Photo-resist, Mask, Developer and Etchant	Mesa photoresist deposition, mask alignment, exposure, developing, etching, and cleaning	See above materials added and processes		D3, 4	A5, 6, 7; B5	
	Back lap	Thickness and uniformity of finish	B3	D1, 2	A4, 7; B1, 2, 4	
Gold	Evaporate and diffuse gold	Cleanliness, uniformity of deposition, purity, temperature and time	A5; B1, 2	D2, 5	A7; B1, 3, 4	
Nickel (8)	Evaporate and sinter nickel	Cleanliness, uniformity of deposition, temperature, and time	A5; B1, 2	D2, 5	A7; B1, 3, 4	

Figure 16-3. Rectifier/Switching Diode - Typical Assembly Flow with Related Problem Codes

FLOW DIAGRAM			RELATED PROBLEM CODES (see foldout in the Appendix)			
MATERIAL	MANUFACTURING OPERATION	CRITICAL PROCESS	OPEN I	SHORT II	PAR DEV III	MECH ANOM IV
Nickel (8)	Nickel plate	Cleanliness, thickness, and uniformity of deposition	A5; B1,2	D2,5	A7; B1,3,4	
Gold	Gold plate	Cleanliness, thickness, uniformity of deposition and purity	A5; B1,2	D2,5	A7; B1,3,4	
	Scribe and sort	Scribe pressure and time	B3	A2;	A4; B2	
First Seal (Anode Lead, Disk, Glass Body) (1) (3) (5) (11)	Clean, stack and "solder" mount assembly to chip	Cleanliness, time, temperature, and environment	A1,2; B1,2	A1,2;	A2; B1,3	A1,2,3, 4,5;
Whisker Assembly (Whisker with Cathode Lead Attached) (1) (9) (12)	Clean whisker assembly and insert	Cleanliness	A1,2,4	A1,5	B1	A1,2,3, 4,5
	Final seal	Temperature, time, and atmosphere		A (all); B	A2,3	B2,3
	High temperature age					
Plating Material (1)	Plate leads	Purity of plating and thickness				A1,4
	Screening tests					
	Test and inspect	Testing process				A2; B2
	Mark, pack, and ship	Paint quality, type, and marking process				A2; B4,5

NOTE: For items (1) through (11) see Fig. 16-1

Figure 16-3. Rectifier/Switching Diode - Typical Assembly Flow with Related Problem Codes

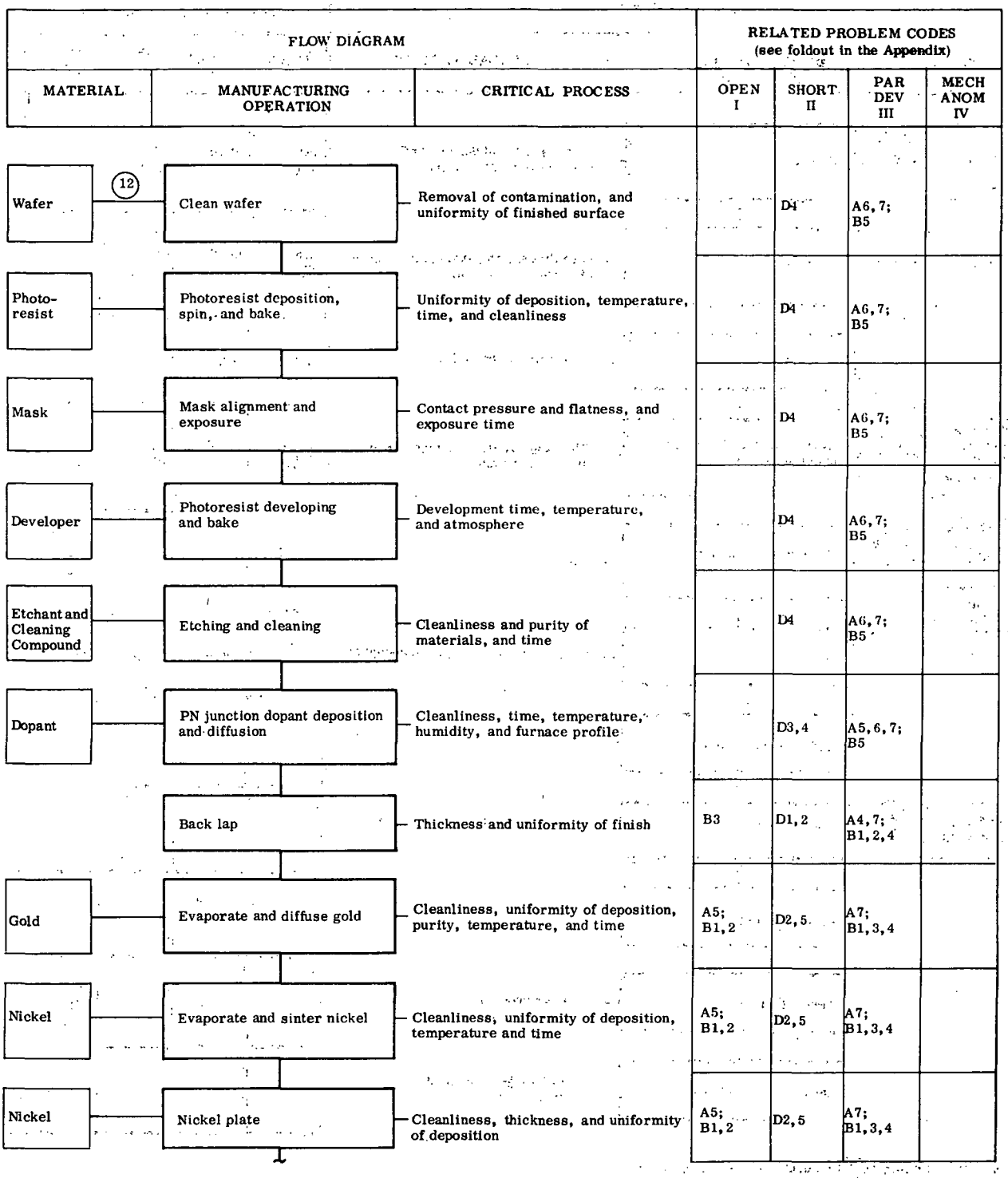
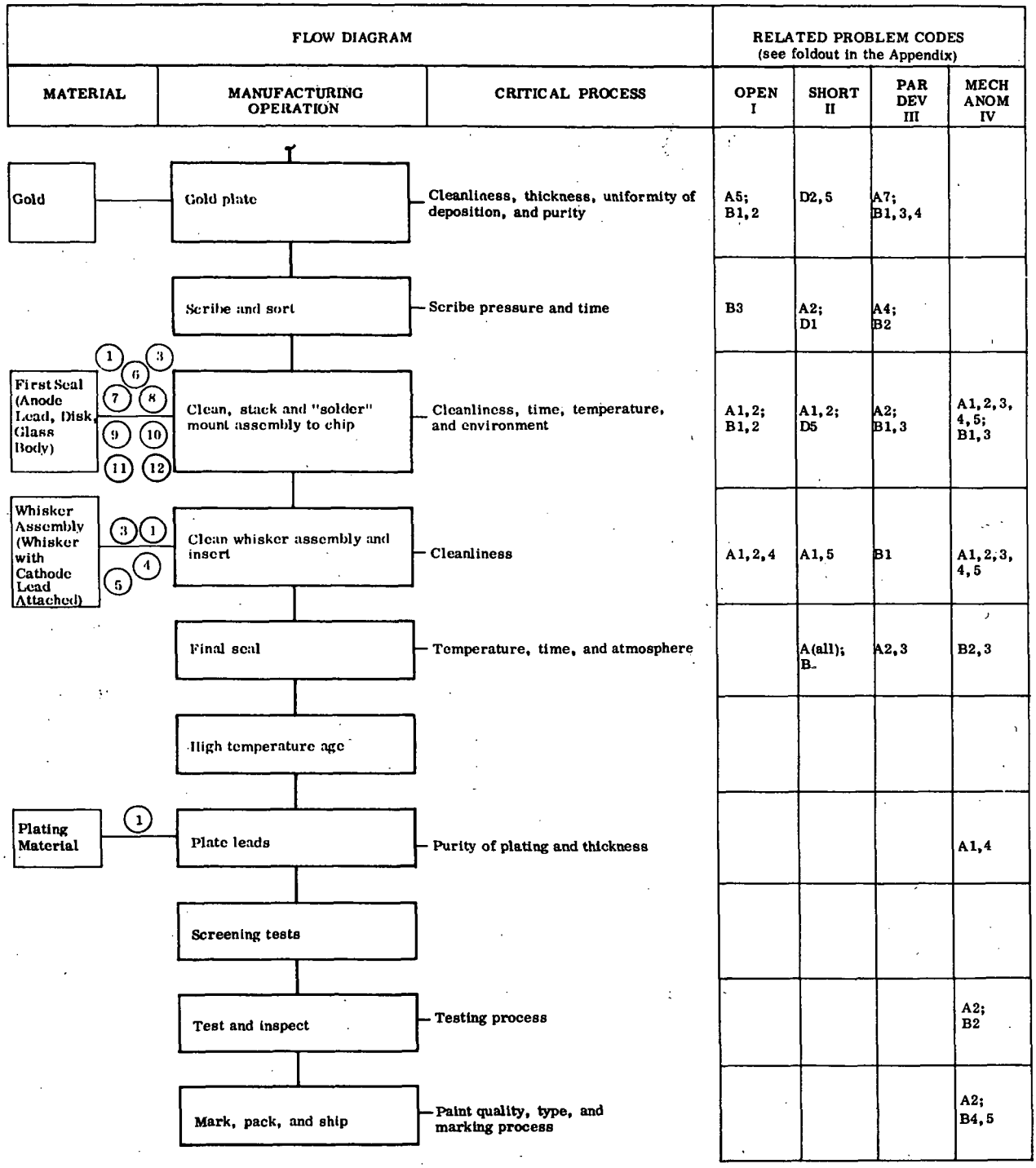


Figure 16-4. Zener Diode - Typical Assembly Flow with Related Problem Codes



NOTE: For items (1) through (12) see Fig. 16-2

Figure 16-4. Zener Diode - Typical Assembly Flow with Related Problem Codes

RECTIFIER, SWITCHING, AND ZENER DIODES

FAILURE ANALYSIS TECHNIQUES

General. Failure analysis is a corrective action-related procedure. Only after knowing why a part failed can action be taken to minimize future failures. Failure analysis findings can show the need for redesign (improvement in materials, processes, and controls) or proper part application.

Predominant Failures. Failures of rectifier/switching, and zener diodes most frequently result from misapplication, either as a result of marginal design or as a result of misapplication of power during use. Indications of misapplication of power are normally burn marks, melted leads, unusual discoloration, and massive cracks with burning and/or discoloration. Misapplication in mounting of diodes can result in corrosion of leads, cracking of the diode body (damaged package), destruction of seals, and shorting of external leads.

Dissection Precautions. Grinding and polishing, if not performed in small increments, can easily pass through the failed area without detecting its presence.

Failure Analysis Flow. The failure analysis flow diagram (Figure 16-5 which follows) provides for maximum nondestructive evaluation of the failed part prior to the dissecting or depotting operation.

Relationship to Failures. Where it is relevant, each step of the failure analysis procedure (Figure 16-5) is related to one of the four major problem areas and their causes by a coding system which is defined on the foldout in the Appendix. Thus, one experiencing a specific type of failure can identify those steps in the failure analysis most likely to reveal the problem.

NOTE

RECORD AND/OR PHOTOGRAPH ALL OPERATIONS AND ANOMALIES DURING THE FAILURE ANALYSIS PROCEDURE

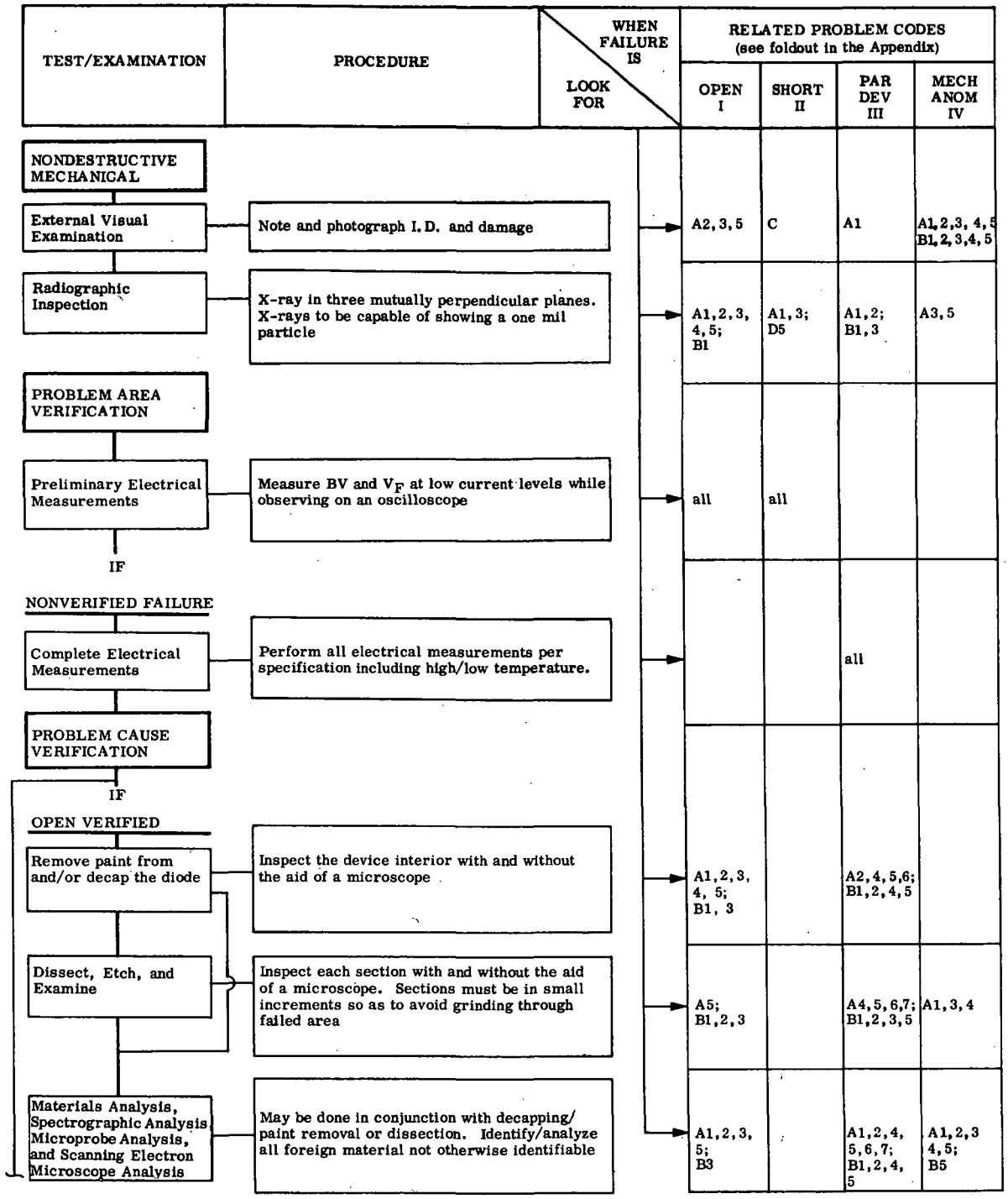


Figure 16-5. Rectifier/Switching, and Zener Diodes - Typical Failure Analysis Flow with Related Problem Codes

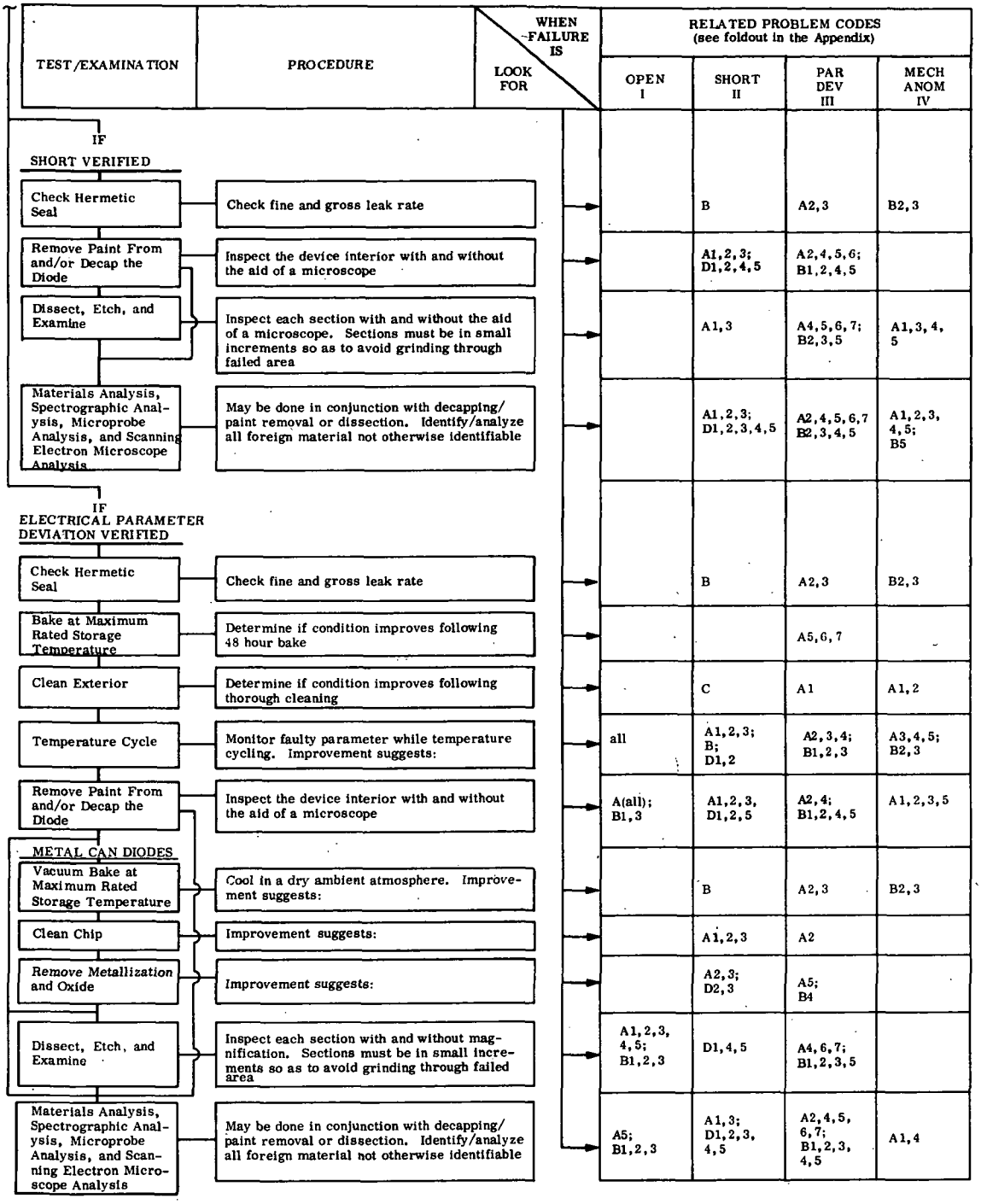


Figure 16-5. Rectifier/Switching, and Zener Diodes - Typical Failure Analysis Flow with Related Problem Codes

RF DIODES

CHARACTERISTICS

All specialized diode types designed to perform a particular application at radio frequencies (rf) are placed in a class called rf diodes. These include IMPATT, hot carrier (Schottky), step recovery, and pin diodes. As a class, rf diodes have one thing in common when compared to a conventional diode, namely, minority carrier storage and lifetimes are closely controlled.

Operation. The basic function of a diode is to pass current in the forward direction and block current in the reverse direction. Of special interest is when the diode has been conducting in the forward direction and then is suddenly reverse biased. Ideally, the diode should change state instantaneously and block current, but actually the diode will continue to conduct for a finite period of time until all the stored minority carriers near the junction are recombined. This period of time is known as reverse recovery time (t_{rr}) and is the limiting factor in operating frequency. In rf diodes several techniques are employed to control t_{rr}.

Hot Carrier (Schottky) Diodes. In hot carrier diodes minority carriers are virtually eliminated through the use of a metal-to-semiconductor junction, hence, t_{rr} approaches zero. A drawback of this scheme, however, is higher reverse leakage current and lower working voltage.

Step Recovery Diodes. In these devices the minority carrier storage and lifetimes are closely controlled so that the device will conduct in the reverse direction for a predetermined time and then abruptly block the reverse current. This feature is well suited for applications requiring harmonic generation. As with all semiconductor devices, when fabricated to idealize a given parameter, other considerations will suffer. In this case, the step recovery diode is very susceptible to temperature variation. Minority carrier lifetime increases at a linear rate of 0.5 to 1.0 percent per degree centigrade and requires external circuitry for temperature compensation.

Pin Diodes. Again, minority carrier lifetime is controlled but this time it is maximized. When operated at the proper rf frequency the minority carrier is much longer than the period of the controlled signal. Hence, the pin diode never completely turns on or off but, rather, behaves much like a rf resistor. The rf resistance can be varied by changing the magnitude of the bias, so that pin diodes are wll suited as rf attenuators.

IMPATT Diodes. IMPATT (Impact Ionization Avalanche Transit Time) diodes are designed to be operated with sufficient reverse bias to cause avalanche breakdown. At microwave frequencies, the combination of avalanche generation and drift of minority carriers across the diode active region produces negative resistance. This feature makes the IMPATT diode very suitable as the active element in a microwave oscillator.

Package Configuration. With the semiconductor properties of rf diodes closely controlled, the performance of the device is often limited by parasitic effects introduced by the package configuration. Many package schemes are employed to minimize capacitance, inductance, and equivalent resistance. Additionally, consideration is given to providing an effective thermal path to remove heat from the semiconductor.

Despite the above precautions, the device performance may still degrade due to parasitic effects introduced when installed into equipment. Equal care and consideration should be given to this operation.

RF DIODES

DESIGN AND PRODUCTION CONSIDERATIONS

Failures Related To Process. A typical rf diode (Figure 16-6) and a typical assembly flow (Figure 16-7) are presented together with the suggested controls required to assure a reliable part. The "Critical Process" is defined for each of the manufacturing steps. Relationship is established between failure causes and the manufacturing process. Having experienced a specific problem, one could identify those manufacturing steps with potential for contributing to the failure.

TYPICAL RF DIODE DESIGN (Figure 16-6)

ITEM NO.	ITEM NAME	MATERIAL OF CONSTRUCTION
1	Heat Sink, Cathode	Kovar, gold plated
2	Cathode to Ring Weld	Gold preform
3	Cathode Ring	Kovar, gold plated
4	Ring and Anode Heat Sink to Body Weld	Gold preform
5	Ceramic Body	Alumina, 96%
6	Preform Bond	Gold, (scrub)
7	Heat Sink, Anode	Kovar, gold plated
8	Interconnect Mesh	Gold, 99.99%
9	Cathode Guard Ring Passivation	Silicon dioxide
10	Cathode and Anode Metallization	Chrome moly
11	Cathode Diffusion	Phosphorous doped silicon
12	Cathode Guard Ring Diffusion	Phosphorous, heavily doped, silicon
13	Anode Diffusion	Boron doped silicon
14	Intrinsic Material	Boron, very slightly doped, silicon
15	Anode Guard Ring Diffusion	Boron, heavily doped, silicon
16	Chip Preform	Tin, gold, copper core, gold, tin sandwich
17	Chip Bonding Material	Gold, 99.9%
18	Anode and Anode Guard Ring Passivation	Silicon dioxide
19	Bonding Ball	Gold, 99.99%

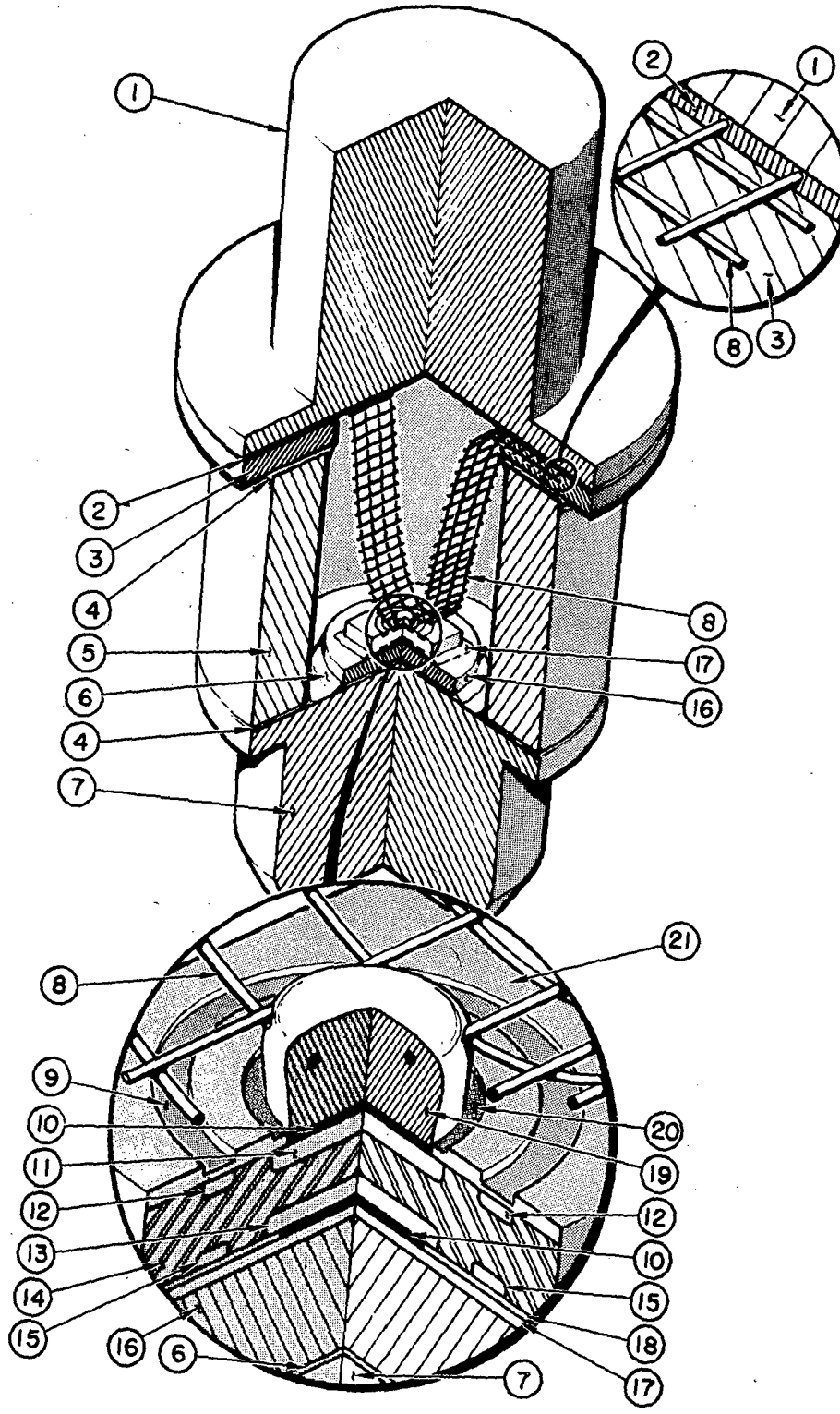


Figure 16-6. Typical RF Diode

MATERIAL	MANUFACTURING OPERATION	CRITICAL PROCESS	RELATED PROBLEM CODES (see foldout in the Appendix)			
			OPEN I	SHORT II	PAR DEV III	MECH ANOM IV
Wafer	Clean wafer	Removal of contamination and uniformity of finished surface		D4	A6; B5	
Photoresist-Anode	Photoresist process-anode	Spin speed, temperature, mask contact pressure, exposure time, and developer		D4	A6; B5	
(13) Dopant	Anode predeposition	Time, temperature, humidity, source, and furnace profile		D4	A6; B5	
	Measure V/I	Probe pressure	B3	D1	A4; B2	
	Clean wafer	Wafer cleanliness		D4	A6; B5	
	Anode drive-in	Time, temperature, and humidity		D3, 4	A5, 6; B5	
	Measure V/I	Probe pressure	B3	D1	A4; B2	
Photoresist-Anode Guard Ring	Photoresist process-anode guard ring	Spin speed, temperature, mask contact pressure, exposure time, and developer		D4	A6; B5	
(15) Dopant	Anode guard ring diffusion	Time, temperature, humidity, source, and furnace profile		D3, 4	A5, 6; B5	
	Clean wafer	Wafer cleanliness		D4	A6; B5	
Photoresist-Cathode	Photoresist process-cathode	Spin speed, temperature, mask contact pressure, exposure time, and furnace profile		D4	A6; B5	
(11) Dopant	Cathode diffusion	Time, temperature humidity, source, and furnace profile		D3, 4	A5, 6; B5	
	Clean wafer	Wafer cleanliness		D4	A6; B5	
Photoresist	Photoresist process	Spin speed, temperature, mask contact pressure, and exposure time		D4	A6; B5	
Cathode Guard Ring	Cathode guard ring	Developer		D4	A6; B5	

Figure 16-7. RF Diode - Typical Assembly Flow with Related Problem Codes

MATERIAL	MANUFACTURING OPERATION	CRITICAL PROCESS	RELATED PROBLEM CODES (see foldout in the Appendix)			
			OPEN I	SHORT II	PAR DEV III	MECH ANOM IV
Dopant (12)	Cathode guard ring diffusion	Time, temperature, humidity, source, and furnace profile		D3,4	A5,6; B5	
	Clean wafer	Wafer cleanliness		D4	A6; B5	
Chrome Moly (10)	Chrome moly evaporation	Pressure (vacuum)	A1,5	D2	A7; B1,4	
Photoresist-Metal Removal	Photoresist process-metal removal	Spin speed, temperature, mask contact pressure, exposure time, and developer	A1,5	D2	A7; B1,4	
	Clean wafer	Wafer cleanliness	A1,5	D2	A7; B1,4	
	Back lap	Thickness and uniformity of finish	B1,2		B3	
Gold (17)	Gold evaporation	Pressure (vacuum)	B1,2	D5	A7; B3,4	
Photoresist-Metal Removal	Photoresist process-metal removal	Spin speed, temperature, mask contact pressure, exposure time, and developer	B1,2	D2,5	B3,4	
	Clean wafer	Wafer cleanliness	B1,2		B3,4	
	100% Test	Probe pressure	B3	D1	A4; B2	
Dice	Scribe and break	Freedom from cracks, fractures, and chipouts	B3	A2; D1	A4; B2	
Anode Heat Sink Preform and Die (16) (7) (21)	Preform and die attach	Temperature, pressure, and alignment	B1,2,3	A1,2; D1,5	A4; B1,2,3	A3,5; B1,2,3
Wire Mesh (8)	Wire mesh attach	Temperature	A1,2		B1	
Ceramic Body (5)	Install on anode heat sink and seal	Alignment and temperature		A1; B	A2,3	A3,5; B1,2,3
Cathode Heat Sink (1)	Install and final seal	Alignment, temperature and N_2 atmosphere		A1; B	A2,3	A3,5; B1,2,3
	Age					
	Seal test	Materials and processes used			A1,2	
	DC test					A2
	Mark, pack, and ship	Paint used and cleanliness				A2; B4,5

NOTE: For items (1) through (21) see Fig. 16-6.

Figure 16-7. RF Diode - Typical Assembly Flow with Related Problem Codes

RF DIODES

FAILURE ANALYSIS TECHNIQUES

General. Failure analysis is performed to establish the cause of failure, provide guidelines for corrective action, and determine the relevancy or impact of the failure in a given application. The primary goal of failure analysis is to provide corrective action to prevent recurrence of the failure mode or mechanism involved. They may take the form of changes in materials or processes, package configuration, installation techniques, or reconsideration of the device to perform in its particular application.

Predominant Failures. The predominant failure in rf diodes is a phenomenon known as "burn out", and is usually associated with some form of misapplication of the device. Burn out results from the inability to remove heat from the semiconductor junction and, depending on the internal construction, can cause open, short, or parametric degradation. Factors contributing to burn out include electrical and/or thermal overstresses, improper mounting techniques, or inadequate heat-sinking. Burn out is usually initiated by a high current density through the junction resulting from electrical overstress and subsequent thermal overstress.

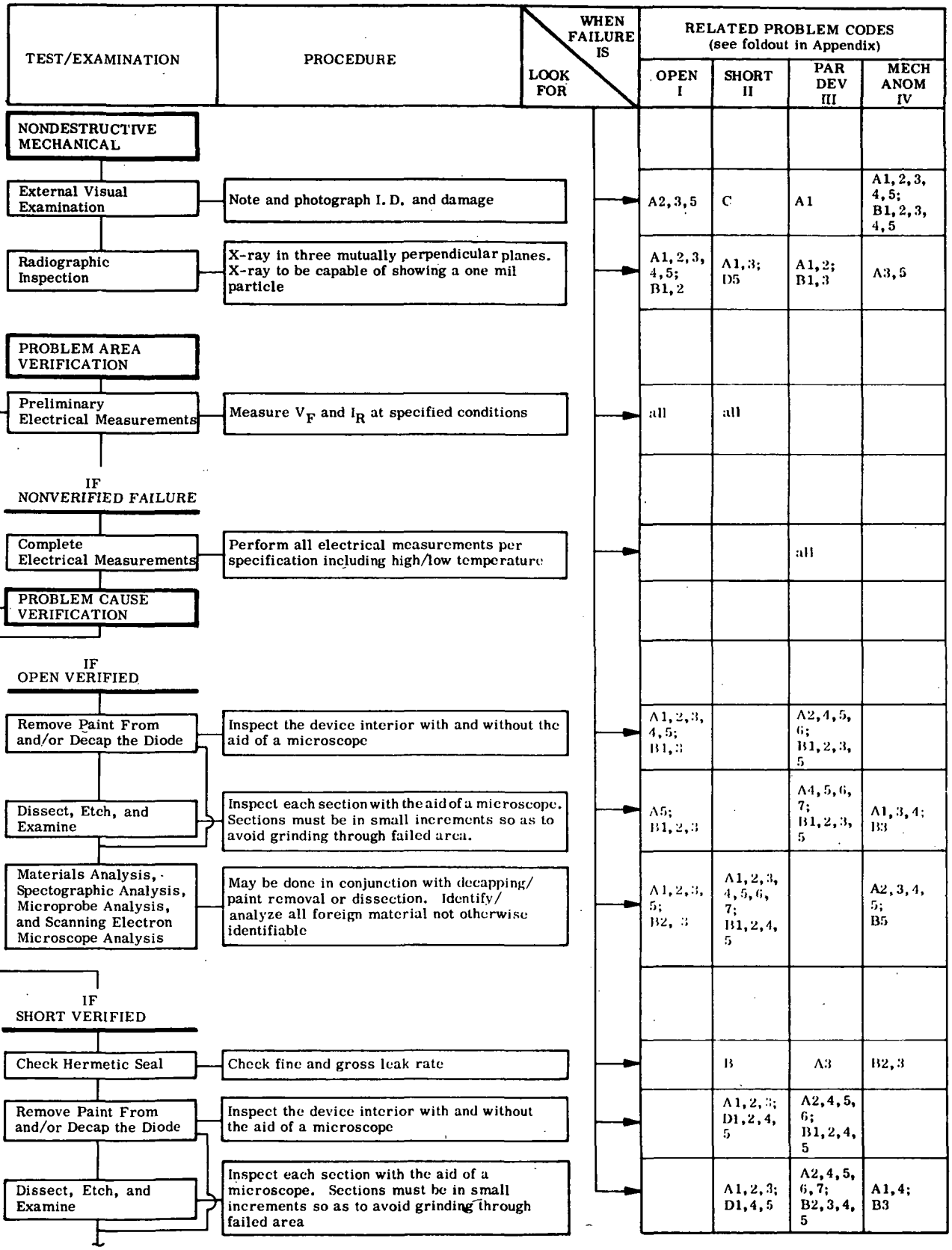
Dissection Precautions. Due to the many variations in package design and configuration encountered in rf diodes, it is a good practice to X-ray the device prior to dissection. Sufficient exposures (generally 3 mutually perpendicular axes) should be taken to adequately define internal details and thus provide the best approach in the particular dissection process. As with all semiconductor devices, grinding and polishing should be performed in small increments to assure that the failed area is not passed through without detecting its presence.

Failure Analysis Flow. The failure analysis flow (Figure 16-8) which follows provides for maximum nondestructive evaluation of the failed part prior to the dissecting or depotting operation.

Relationship to Failures. Where it is relevant, each step of the failure analysis procedure is related to one of the four major problem areas and their causes by a coding system which is defined on the foldout in the Appendix. Thus, one experiencing a specific type of failure can identify those steps in the failure analysis most likely to reveal the problem.

NOTE

RECORD AND/OR PHOTOGRAPH ALL OPERATIONS AND ANOMALIES DURING THE FAILURE ANALYSIS PROCEDURE.



TEST/EXAMINATION	PROCEDURE	WHEN FAILURE IS / LOOK FOR	RELATED PROBLEM CODES (see foldout in Appendix) OPEN I	SHORT II	PAR DEV III	MECH ANOM IV
NONDESTRUCTIVE MECHANICAL						
External Visual Examination	Note and photograph I. D. and damage		A2,3,5	C	A1	A1,2,3,4,5; B1,2,3,4,5
Radiographic Inspection	X-ray in three mutually perpendicular planes. X-ray to be capable of showing a one mil particle		A1,2,3,4,5; B1,2	A1,3; D5	A1,2; B1,3	A3,5
PROBLEM AREA VERIFICATION						
Preliminary Electrical Measurements	Measure V_F and I_R at specified conditions		all	all		
IF NONVERIFIED FAILURE						
Complete Electrical Measurements	Perform all electrical measurements per specification including high/low temperature				all	
PROBLEM CAUSE VERIFICATION						
IF OPEN VERIFIED						
Remove Paint From and/or Decap the Diode	Inspect the device interior with and without the aid of a microscope		A1,2,3,4,5; B1,3		A2,4,5,6; B1,2,3,5	
Dissect, Etch, and Examine	Inspect each section with the aid of a microscope. Sections must be in small increments so as to avoid grinding through failed area.		A5; B1,2,3		A4,5,6,7; B1,2,3,5	A1,3,4; B3
Materials Analysis, Spectographic Analysis, Microprobe Analysis, and Scanning Electron Microscope Analysis	May be done in conjunction with decapping/paint removal or dissection. Identify/analyze all foreign material not otherwise identifiable		A1,2,3,5; B2,3	A1,2,3,4,5,6,7; B1,2,4,5		A2,3,4,5; B5
IF SHORT VERIFIED						
Check Hermetic Seal	Check fine and gross leak rate			B	A3	B2,3
Remove Paint From and/or Decap the Diode	Inspect the device interior with and without the aid of a microscope			A1,2,3; D1,2,4,5	A2,4,5,6; B1,2,4,5	
Dissect, Etch, and Examine	Inspect each section with the aid of a microscope. Sections must be in small increments so as to avoid grinding through failed area			A1,2,3; D1,4,5	A2,4,5,6,7; B2,3,4,5	A1,4; B3

Figure 16-8. RF Diode - Typical Failure Analysis Flow with Related Problem Codes

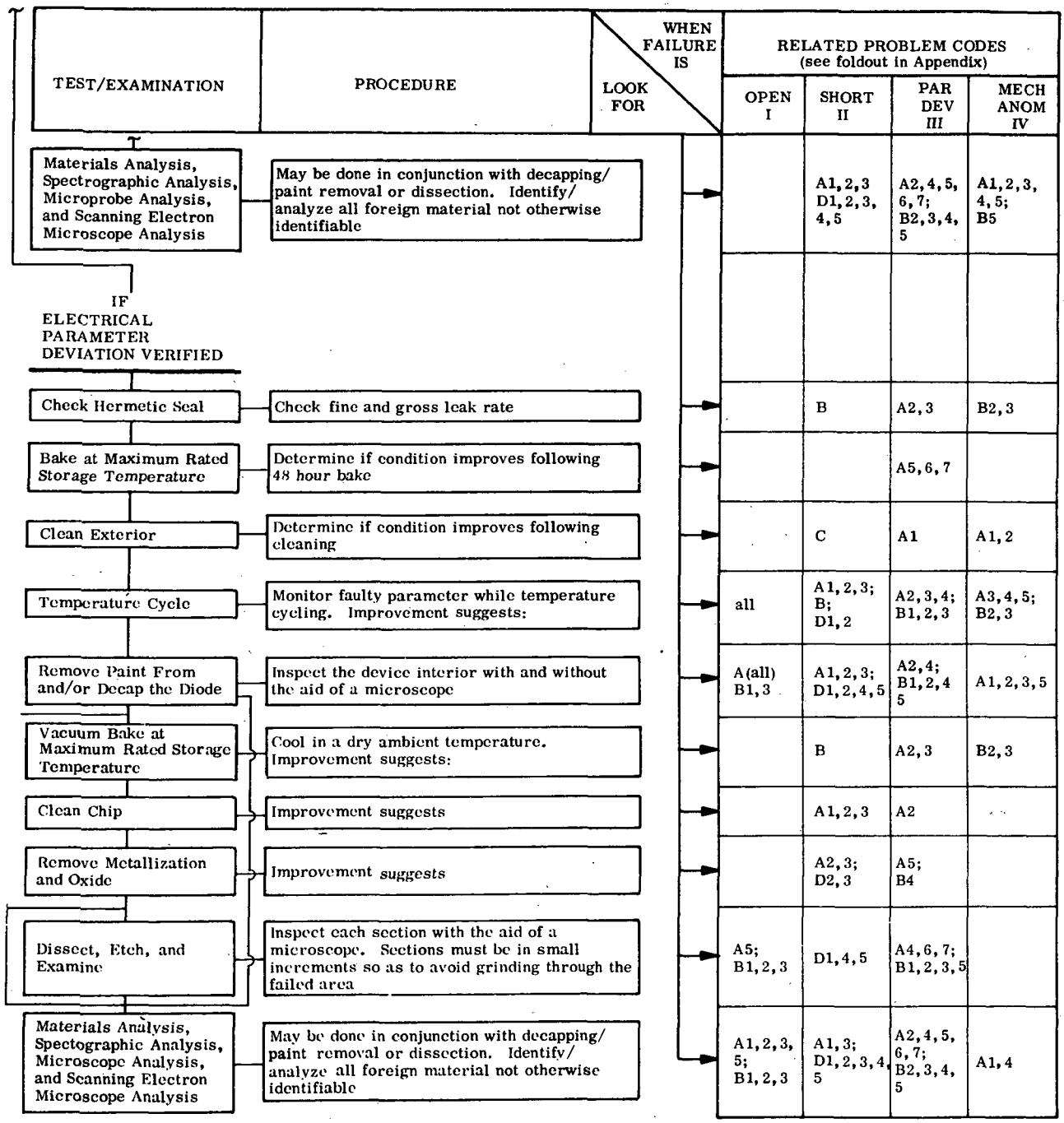


Figure 16-8. RF Diode - Typical Failure Analysis Flow with Related Problem Codes

ALERT SUMMARIES

Summaries of ALERT reports issued against Rectifier/Switching, Zener, and Miscellaneous Diodes are shown below. They are listed according to Problem Area, except the Miscellaneous are listed by type. The "ALERT ITEM No." (first column) references each summary back to the "Problem Area/Cause, and Suggested Action" table.

RECTIFIER AND SWITCHING DIODES

ALERT[1] ITEM NO./ GIDEP NO.	PROBLEM AREA/ Cause	PROBLEM DESCRIPTION	PROBLEM ANALYSIS
1 MSFC-71-01	OPEN Inadequate bonds	Plastic encapsulated diodes used in "cordwood" modules open circuited at the cathode lead to chip bond.	Discrepant parts used gold-germanium soldering of the cathode lead to die bond and could not endure temperature stress when used in "cordwood" modules. Parts were changed to a nonplastic device using a thermocompression bond.
2 K4-71-01	OPEN Chip lifted	Intermittent malfunction of equipment occurring during temperature cycling was traced to a PC containing diodes.	Tests of diodes revealed opens or high voltage drops. When sample diodes were opened, the die in each case fell out due to little or no bonding to either internal heat sink (slug). The problem was traced to incompatible thermal coefficient between the externally fused glass and the die assembly.
3 S8-71-01	OPEN Chip lifted	Diodes failed to pass surge current requirement of the military specification.	The normal failure mode would be an open circuit. The problem is due to incompatible thermal coefficient between the externally fused glass and the die assembly.
4 F9-71-01	OPEN Chip lifted	Diodes failed open during equipment tests.	Diode types constructed with compression bonding with only the glass body material holding the chip and lead terminals together, were opening at the connection between chip and terminals. Diodes constructed with silicon die metallurgically bonded directly to the terminal pins displayed no problems in identical applications. The problem is due to incompatible thermal coefficient between the externally fused glass and the die assembly.
5 MSFC-71-04	OPEN Chip lifted	Diodes failed open during manufacturing tests of Skylab components.	The diodes opened at the connection between chip and studs. Diode construction uses compression bonding with the glass body material holding the chip and lead studs together mechanically. The problem is due to incompatible coefficient between the externally fused glass and the die assembly.
6 K9-71-22	OPEN Chip lifted	Electrical testing showed that the diodes were intermittently open.	Microscopic examination revealed that the chip was detached from the lower mounting stud and was held in place only by the silicone rubber seal.

RECTIFIER AND SWITCHING DIODES

ALERT[1] ITEM NO./ GIDEP NO.	PROBLEM AREA/ Cause	PROBLEM DESCRIPTION	PROBLEM ANALYSIS
7 C6-68-03	SHORT Lack of hermetic seal	Hermetic seal failure during installation which resulted, ultimately, in the diode shorting.	Moisture entered the broken seals and lead oxide formed over the chip by galvanic action between the silver "whisker" and the chip "button." It was recommended that the military specification require higher torquing requirements.
8 MSC 3-10-66	SHORT Conductive contamination	Silver contamination caused a diode in a Control Programmer qualification unit to fail short.	The silver contamination was weld splash resulting from a resistance weld. A hex-crimp is incorporated to prevent weld splash from entering the diode cavity.
9 MSFC-68-10	ELECTRICAL PARAMETER DEVIATION Contamination	During functional testing, parts exhibited excessive reverse current.	Defective tabulation seal and surface contamination which was conductive during high humidity conditions. All of the defective diodes were rejected.
10 B1-68-01	MECHANICAL ANOMALY Hydrofluoric etchant	Corrosion of cathode lead at point of connection to the body such that normal handling resulted in lead breakage.	A minute amount of hydrofluoric etchant was trapped in the small cavity between the glass and the lead of the first seal. Over a period of time the lead was etched and the nickel-iron core exposed, which then corroded. Additional in-house, in-process controls were established to control the level of rinse water, the concentration of etch solution, and the effectiveness of the rinse.
11 F3-71-01	MECHANICAL ANOMALY Defective weld	Diodes came apart at the brazed joint during assembly operation (soldering to diode stud).	Metallurgical analysis revealed the failure was caused by absence or improper use of flux, and because the two butted ends were not flat.

ZENER DIODES

ALERT[1] ITEM NO./ GIDEP NO.	PROBLEM AREA/ Cause	PROBLEM DESCRIPTION	PROBLEM ANALYSIS
12 MSC 1-26-67	OPEN Inadequate bond.	Zener diodes failed open or operated intermittently.	Defective gold plating on a copper stud base prevented adequate bonding of the silicon chip. Defective plating is being controlled through specification changes and institution of incoming materials inspection.
13 MSC 9-16-66	OPEN Inadequate bond	Open and/or intermittent operation in a dynamic environment.	Displacement of "S" bend ribbon at point of contact with die metallization as a result of shock or vibration. A solid feed-through lead has been incorporated to avoid this problem.

ZENER DIODES

ALERT[1] ITEM NO./ GIDEP NO.	PROBLEM AREA/ Cause	PROBLEM DESCRIPTION	PROBLEM ANALYSIS
14 GSFC-71-04	SHORT Conductive contamination	Failure of a subsystem during bench test was traced to a diode.	Failure analysis revealed that a loose particle inside the diode had shorted across the silicon die. The particle had formed by undercutting the gold/germanium solder during the die etching process. Also, the silicone varnish, used to passivate the surface, was missing from the die because of an error in the manufacturing process.
15 G4-71-01	SHORT Conductive contamination	Diode was found with alloy 52 particles internal to the package.	The problem was traced to the manufacturer's welding and machining processes.
16 BED-69-01	ELECTRICAL PARAMETER DEVIATION Incorrect guard band limits	Devices exceeded I_R limit at high and ambient temperature, and exceeded maximum breakdown voltage.	Q.C. sample monitoring was insufficiently tight, resulting in discrepant parts being accepted.
17 GSFC-71-07	ELECTRICAL PARAMETER DEVIATION Contamination	Diodes failed to meet reverse leakage current limits during burn-in test.	Failure analysis revealed ionic contaminants on the die surfaces had created inversion layers in the silicon on two devices. Another device failed because the "C" spring had contacted the silicon die.
18 DG-68-01	MECHANICAL ANOMALY Improperly formed weld	Zener physically fell apart	Weld was improperly formed at the interface of the "top hat" and "stud header".
19 MSC 11-23-64	MECHANICAL ANOMALY Oxidation of Dumet copper	A commercial glass diode was purchased which was contaminated.	Dumet copper sheath oxidized during first seal operation. Avoid use of commercial parts for high reliability applications as they are not intended to be well-produced or well-inspected products.
20 MSFC-64-02	MECHANICAL ANOMALY Shrinkage of die bond material	X-ray inspection revealed voids and a subsequent visual examination showed cracks in the die bonding material.	Silver paste die bonding material shrinks during cure or annealing process. Physical and electrical testing showed no apparent degradation in performance.

MISCELLANEOUS DIODES

TYPE; ALERT[1] ITEM NO./ GIDEP NO.	PROBLEM AREA/ Cause	PROBLEM DESCRIPTION	PROBLEM ANALYSIS
21 OPTOELECTRON-ICS SI-70-01	MECHANICAL ANOMALY Freon TMC	Softening and clouding of clear plastic lens when vapor cleaned with Freon TMC and alcohol to remove rosin flux residue.	The clear lens contains a large proportion of methylene chloride which will soften and cloud when exposed to Freon TMC. Flux was changed to water soluble flux and the lens is cleaned with water containing a mild detergent.
22 SCR LeRC 3-10-67	OPEN Inadequate bond	Inconsistent gate triggering levels in receiving inspection and a static inverter failure.	Excessive crimping of the aluminum gate lead resulted in an intermittent open gate.
23 SCR MSFC-68-23	ELECTRICAL PARAMETER DEVIATION Contamination	SCR would trigger with the application of anode voltage.	Contamination introduced with wafer processing or in the silicone rubber passivation caused improper operation of "mesa" type SCR. SCR now uses a planar chip.
24 SCR GSFC 5-15-67	MECHANICAL ANOMALY Poor lead plating	Leads of silicon controlled rectifier failed to solder.	Leads were contaminated during high temperature bake. Subsequent cleaning processes failed to remove the contamination.
25 VARACTOR GSFC-70-15	OPEN Mechanically overstressed	Varactor diodes failed while being operated in a parametric amplifier at -165°C. Maximum rating is -65°C.	It was determined that bonding of the die occurred over less than 25% of the available bonding area, therefore, the parts were more susceptible to failure during mechanical overstress than they should have been. The device has been subsequently redesigned.
26 VARACTOR GSFC 5-19-67	SHORT Contamination	Varactor diodes exhibited a high failure rate during vibration testing.	Dissection of the diodes revealed solder balls, loose silicon "chips," and gold overhang near the junction.

NOTE:
1. Where no ALERT number (GIDEP) exists, the originator and date are shown.

SECTION 17
INTEGRATED CIRCUITS
(GIDEP CODE 515)

CONTENTS

INTRODUCTION

OBJECTIVE

The objective of this section is to identify the major problem areas associated with the use of integrated circuits and to suggest approaches (developed from experience) for dealing with these problems.

SECTION ORGANIZATION

The Integrated Circuit section is organized as follows:

1. Problem/Screening Summary

   This subsection delineates the various problem areas which may be encountered in the usage of Integrated Circuits. There are minor differences in construction between the Diode-Transistor-Logic (DTL), Transistor-Transistor-Logic (TTL), and Linear circuits, hence the failure modes and mechanisms applicable to one may also similarly be found in the other.

2. Screening Inspections and Tests

   Reliability screening of packaged devices prior to use performs an important function in eliminating infant failures as well as marginally performing devices. Reliability screening is patterned after MIL-STD-883, Method 5004 (ref 34), Classes A, B, and C. The choice of screening per any one Class of Method 5004 is dependent on the degree of reliability required.

   a. Class A. Devices intended for use where maintenance and replacement are extremely difficult or impossible, and reliability is imperative.

   b. Class B. Devices intended for use where maintenance and replacement can be performed, but are difficult and expensive, and where reliability is imperative.

   C. Class C. Devices intended for use where maintenance and replacement can be readily accomplished and down time is not critical.

3. Design and Production Considerations for DTL, TTL, and Linear Integrated Circuits

   These subsections discuss the typical DTL, TTL, and Linear constructional details with the inclusion of a typical process flow. Sectional steps within this flow are again keyed to the potential problem areas possible as noted in the foldout in the Appendix.

4. Failure Analysis For DTL, TTL, and Linear Integrated Circuits

   Integrated Circuit failure analysis of DTL, TTL, and Linear follow similar procedures and techniques because of the close similarity in construction of the two digital circuits. The subsection is presented in methodical format. This is necessary because of the inherent danger of inadvertently destroying failure evidence should a haphazard approach be made. Each failure procedure is sequenced so that the succeeding procedure will have an equal chance at uncovering the failure mechanism. The format thus presented is keyed to the foldout in the Appendix.

5. Handling of MOS Devices

Because of perplexing problems in relation to all MOS devices and occurrences where perfectly screened devices arrive inoperative at users' plants, there is included a brief MOS handling subsection. This subsection presents the various methods of handling MOS devices to preclude the shorting out of the gate element caused by electrostatic discharges.

ALERT Summaries

6. This subsection presents summaries of the ALERT reports issued against integrated circuits.

PROBLEM/SCREENING SUMMARY

Scope. This problem summary subsection is a compilation of problem areas derived from the ALERT reports and the wide experience acquired over years of such encounters. It does not presume to list all possible problem areas/causes possible within digital integrated circuits, but is an attempt at compiling the most commonly encountered failures/problems. The problem areas for DTL, TTL, and Linear are similar to a great extent and hence this section applies to both types of logic.

Problems in this summary are keyed to the foldout in the Appendix and delineate the possible causes of failure and the recommended screens to eliminate such causes. Wherever applicable, the failure/problem area will be keyed to the pertinent ALERT report.

PROBLEM AREA/CAUSE AND SUGGESTED ACTION

INTEGRATED CIRCUITS

PROBLEM AREA/ Cause	ALERT ITEM NO.	SUGGESTED ACTION - SCREEN (see "Screening Inspections and Tests")
OPEN Microcracks at window cutout	1,2,3,4,5	1. 100% Electrical Tests following 30 cycles minimum Temperature Cycling - this test may not screen out marginal failures. 2. Invoke Scanning Electronic Microscope scans on sample basis as part of 100% screen.
OPEN Aluminum wire corrosion - reaction with glass spatter and moisture	6	1. 100% Precap Visual Inspection to MIL-STD-883 (ref 34). 2. Utilize Gross Leak Tests per MIL-STD-883, method 1014, Condition C in lieu of ethylene glycol immersion.
OPEN Cracked die - mismatch of coefficients of expansion of bonding pyroceram and silicon dice	7	1. 100% Precap Visual Inspection to MIL-STD-883 (ref 34). 2. Temperature Cycling -55°C to 150°C range. 3. Electrical Testing 100%.
OPEN Lifted chip	8,9,10,11	1. 100% Precap Visual Inspection. 2. Variable Frequency Vibration per MIL-STD-883 (ref 34). 3. Constant Acceleration per MIL-STD-883, (Centrifuge). 4. Electrical Testing 100%. 5. Radiographic Inspection (preferably Vidicon X-ray).
OPEN Voids and overetched metallization	12	1. 100% Dynamic Electrical Testing.
OPEN Lifted bond - purple plague caused by formation of gold-aluminum intermetallic		1. 100% Precap Visual Inspection to MIL-STD-883 (ref 34). 2. Mechanical Shock per MIL-STD-883. 3. Thermal Shock. 4. Constant Acceleration. 5. Random Vibration.
OPEN Lifted bond - poor aluminum adhesion to silicon caused by improper alloying temperature/time		1. Lot Sample Bond Pull Strength Tests. 2. Mechanical Stressing Tests, Vibration, etc. 3. Tighter process controls on pressure, time, temperature.
OPEN Periphery plague - aluminum pad area too small or bond misplaced on thinner region of aluminum interconnect		1. Sample Bond Pull Strength Tests. 2. Mechanical Stressing, i.e., Vibration, Shock, Centrifuge. 3. Tighter control of bond placement during bonding and/or use of larger aluminum bond pads.

INTEGRATED CIRCUITS

PROBLEM AREA/ Cause	ALERT ITEM NO.	SUGGESTED ACTION - SCREEN (see "Screening Inspections and Tests")
OPEN Overbonding - excessive temperature and/or pressure		1. Stabilization Bake per MIL-STD-883 (ref 34). 2. Precap Visual Inspection per MIL-STD-883 (ref 34). 3. Bond Pull Strength Tests. 4. Tighter process controls on bonding operation.
OPEN Improperly placed thermocompression bond		1. Precap Visual Inspection per MIL-STD-883 (ref 34). 2. Mechanical Stressing, i.e., Vibration, Shock, and Centrifuge.
OPEN Rebonds - original bond area was bonded a second time		1. Precap Visual Inspection. 2. Prohibit rebonds on same area if silicon is exposed. 3. Mechanical Stressing, i.e., Vibration, Shock and Centrifuge.
OPEN Corrosion - aluminum interconnects reacting with dissimilar metal contacts in presence of excessive moisture (hydrated alumina)		1. Stabilization Bake period prior to seal. 2. Hermetic Seal Tests following seal per MIL-STD-883 (ref 34). 3. Control atmosphere during preseal storage.
OPEN Scratches - improper handling and/or assembling		1. Train operators to exacting procedures in handling. 2. Precap Visual Inspection per MIL-STD-883 (ref 34). 3. Power Life Tests. 4. Institute adequate "in-transit" or "in-process" packaging and handling procedures.
OPEN Thinning of aluminum over step in oxide		1. Use multiple aluminum source evaporation technique. 2. Use planetary motion during evaporation of metal. 3. Use heated substrates. 4. Increase aluminum thickness. 5. Decrease height of oxide steps. 6. Screen out during Power Burn-in, 168 hours at elevated temperature.
OPEN Open in aluminum near contact window caused by aluminum pulling toward alloyed contact		1. Precap Visual Inspection per MIL-STD-883 (ref 34). 2. Sample Scanning Electron Microscope scans. 3. Increase aluminum thickness. 4. Check aluminum alloy procedure.

INTEGRATED CIRCUITS

PROBLEM AREA/ Cause	ALERT ITEM NO.	SUGGESTED ACTION - SCREEN (see "Screening Inspections and Tests")
OPEN Opens in aluminum contacts, interconnects-faulty oxide removal		1. Tighten process controls during fabrication, particularly oxide etches. 2. Temperature Cycling followed by measurement at low voltages. 3. Bake at temperatures. 4. Power Burn-In at temperatures per MIL-STD-883 (ref 34). 5. Precap Visual Inspection per MIL-STD-883. 6. 100% Electrical Tests.
SHORT Bulk shorts - secondary breakdown or uncontrolled PNPN switching when device design permits floating internal junctions		Properly specify electrical characteristics.
SHORT Bulk short - phosphorous or boron spikes during diffusion or dendritic growths caused by silicon crystal imperfections and pinholes		1. Improve on process controls. 2. Thermal Bakes and Operating Life Tests. 3. Precap Visual Inspection per MIL-STD-883 (ref 34).
SHORT Bulk short - misalignment of diffusion patterns		1. Improve on process controls. 2. Maintain Visual Inspections during processing.
SHORT Interconnect metallization short - scratches, smears, or unetched metallizations		1. Improve photoresist and aluminum etching procedures. 2. Improve operator handling during assembly. 3. Precap Visual Inspection per MIL-STD-883 (ref 34). 4. Passivate chip surface with silicon nitride or pyrolytic glass.
SHORT Metallization to silicon shorts - pinholes or entrapped impurities.	13	1. Improve process controls. 2. Make parametric measurements. 3. Apply current limited, over-voltage to confirm such anomalies.
SHORT Metallization to silicon shorts - metallization mask misalignment		1. Precap Visual Inspection per MIL-STD-883 (ref 34). 2. Improve on alignment procedures and masks.
SHORT Ball bond to silicon shorts - lead bond placement too close to edge of silicon die Bond pads positioned too close to edge of die Poor scribing and/or dicing or poor alignment during dicing Bond made over steep oxide step (punches through oxide)		1. Improve on design and layout of circuit on die. 2. Improve on process control, i.e., lead bonds. 3. Precap Visual Inspection per MIL-STD-883 (ref 34). 4. 100% Electrical Tests.

INTEGRATED CIRCUITS

PROBLEM AREA/ Cause	ALERT ITEM NO.	SUGGESTED ACTION - SCREEN (see "Screening Inspections and Tests")
SHORT Shorts between internal leads - outer lead shorted to supply voltage terminal	14	1. Improve on chip orientation in design. 2. Improve on bonding techniques. 3. Precap Visual Inspection per MIL-STD-883 (ref 34).
SHORT Shorts between internal leads - incorrect orientation of die	15	1. Improve on assembly quality control inspections. 2. 100% Electrical Tests. 3. Precap Visual Inspections per MIL-STD-883 (ref 34).
SHORT Shorts between internal leads - sagging leads		1. Precap Visual Inspections per MIL-STD-883 (ref 34). 2. Vibration Tests per MIL-STD-883. 3. Shock Tests per MIL-STD-883.
SHORT Shorts between internal leads - leads touch edge of die		1. Operator training. 2. Precap Visual Inspections per MIL-STD-883 (ref 34). 3. Vibration Tests per MIL-STD-883.
SHORT Shorts between internal leads - excessive lead lengths/loops shorting to metal parts of package.(i.e., cover)		1. Electrical Measurements at Pre-Burn-In. 2. Radiographic Inspection. 3. Improve design of package. 4. Utilize insulated cover or cover of insulator material.
SHORT Extraneous conductive material - extraneous leads or bonds	16	1. Improve process controls. 2. Precap Visual Inspection per MIL-STD-883 (ref 34). 3. Electrical Testing on 100% basis. 4. Radiographic Inspection. 5. Mechanical Stressing, i.e., Vibration, Shock or Centrifuge.
SHORT Extraneous conductive material - free conducting materials	17,18,19,20, 21	1. Improve process controls, i.e., alloy mount process, use of laminar flow benches, cleaning procedures. 2. Precap Visual Inspection per MIL-STD-883 (ref 34). 3. Radiographic Inspection.
SHORT Extraneous conductive material - carbonized material (lint, cotton etc.,) on surface of die		1. Inspect per MIL-STD-883, Method 2010.1 (ref 34). 2. Improve process controls and cleaning procedures.
SHORT Extraneous conductive material - excess flow of eutectic during die attach		1. Improve process control on die attach. 2. Precap Visual Inspection per MIL-STD-883 (ref 34). 3. Radiographic Inspection.

INTEGRATED CIRCUITS

PROBLEM AREA/ Cause	ALERT ITEM NO.	SUGGESTED ACTION - SCREEN (see "Screening Inspections and Tests")
SHORT Extraneous conductive material - loose particles due to package sealing process	22	1. Improve process control, sealing techniques, and/or equipment. 2. Radiographic Inspection. 3. Electrical Tests.
SHORT Oxide anomalies - pinholes		1. Precap Visual Inspection per MIL-STD-883 (ref 34). 2. Improve process controls. 3. Temperature Cycling per MIL-STD-883. 4. 100% Electrical Tests.
SHORT Oxide anomalies - cracks in oxide due to improper oxide growing techniques or stresses in oxide		1. Slow cooling of slices after diffusion during processing. 2. Visual Inspection at very high magnifications. 3. Temperature Cycling per MIL-STD-883 (ref 34).
SHORT External leads - formation of lead precipitates between leads	23	1. 100% Visual Inspection at precap and external Visual Inspection points during screening. 2. 100% Electrical Tests.
SHORT Electrostatic discharge (MOS devices) - punch-through	24	1. Provide adequate handling and testing procedures. 2. Provide for diode protection during design phase. 3. Provide for common ground of all test equipment. NOTE: Special MOS device handling instructions are given in this IC section.
SHORT Diffusion anomalies	25	1. 100% Precap Visual Inspection per MIL-STD-883 (ref 34). 2. 100% Temperature Cycling per MIL-STD-883. 3. 100% Electrical Tests including temperature tests.
OPERATIONAL DEGRADATION Design deficiency - counter miscounts because of oversensitivity to voltage variation	26,27	Electrical Tests at ambient and extreme temperatures.
OPERATIONAL DEGRADATION Flip-flop reset rates slowed in critical applications - the fix for open contact window metallization slowed f/f reset rates from 1 μSec to 3 μSec	28	1. 100% Electrical Tests of reset controls. Note: device affected only in certain critical applications.

INTEGRATED CIRCUITS

PROBLEM AREA/ Cause	ALERT ITEM NO.	SUGGESTED ACTION - SCREEN (see "Screening Inspections and Tests")
OPERATIONAL DEGRADATION Excessively high leakage failure rates - overfritting of glass during die bonding; glass extends up side and onto chip surface	29	1. 100% Precap Visual Inspection per MIL-STD-883 (ref 34). 2. 100% Electricals prior to shipment. 3. 150°C Bake for 168 hours with Electricals before and after Bake. This is in addition to 100% Screens.
OPERATIONAL DEGRADATION Loss of gain due to inversion - inversion of N type lateral transistor caused by use of phosphorous glass passivation providing surface instabilities	30	100% Electrical Tests under temperature conditions.
OPERATIONAL DEGRADATION Nontriggering of monostable multivibrator - previous mask changes by original manufacturer to correct one deficiency affected output pulse fall-time to extent it will not trigger in cascade	31	1. In critical cascade applications, the user should evaluate impact of external C_x which cannot be used due to this problem. 2. In applications where one monostable multivibrator is used and where external C_x is not depended on for pulse width extension, this device may be used. 3. Critical usage applications should change procurement documents to invoke tests which will eliminate failures due to too large an external capacitor C_x .
OPERATIONAL DEGRADATION Oversensitivity to temperature variation - output decreases to zero under temperature condition (140°F) - degradation caused by reaction of output PNP lateral transistor reacting with plastic case material	32	NOTE: The manufacturer acknowledged this problem and has discontinued manufacturing this type of case. Use of plastic cases for space applications is not recommended.
OPERATIONAL DEGRADATION Latch-up failure of linear output - failure caused by: (1) damage to input circuitry as a result of exceeding the positive common mode limit, (2) exceeding the differential input voltage, and (3) supply voltage polarity reversal - this causes forward biasing of the isolation diode and shorts the power supplies resulting in large surge currents	33,34,35	1. 100% Electrical Screens will invariably detect these failures. NOTE: The following precautions should be followed during assembly and/or test: a) Ascertain good grounds and unwanted transients during assembly (welding, soldering, etc.) and test. b) Assure power supply decoupling, short ground leads and shielded power supply leads.
OPERATIONAL DEGRADATION Numerous systems test failures - failures attributed to the following: (1) cracked wafers, (2) foreign material - photoresist residues, (3) metallization scratches, and (4) pyroceram voids in die to header bonds	36	1. 100% Precap Visual Inspection per MIL-STD-883 (ref 34). 2. 100% Radiographic Inspection. 3. 100% Electrical and Environmental Tests per MIL-STD-883, Method 5004, Condition A or B.

PROBLEM AREA/ Cause	ALERT ITEM NO.	SUGGESTED ACTION - SCREEN (see "Screening Inspections and Tests")
OPERATIONAL DEGRADATION J-K flip-flop fails under elevated temperatures but returns to normal when at 25°C, room ambient temperature - failures attributed to: (1) design error - a missing n+ diffusion used for ohmic contact to the n- type resistor tub associated with the 'J' inputs, and (2) surface inversion caused by either bulk oxide or oxide surface contamination which was production lot dependent	37,38	1. Redesign. 2. 100% Electrical Screen with the following additional parameters to be checked: a. V_{cc} to substrate leakage current: V_{cc} = .4V, and $I_{leakage}$ = 1.0 uA max. b. Clear to substrate leakage current: Clear = 5V, $I_{leakage}$ = 1.0 uA max. c. High temperature 'inhibit' functional test: for 48 hours with Ta = 125°C conditions: Input J's = .8V, Clock = ±2.4V V_{cc} = 5 V., Under conditions, Q must remain at logical '1' level.
OPERATIONAL DEGRADATION Electrostatic discharge	39	1. Use sinks with lower susceptibility to static charge build-up. 2. Use antistatic procedures during manufacturing and grounding procedures during testing.
OPERATIONAL DEGRADATION *Offset voltage drift*	40	1. Manufacturer implement: a. Vacuum oxidation photoresist removal and clean-up. b. Pre-aluminum gettering: deposit of phosphor to entrap any ions that become mobile under temperature and biased conditions. 2. MIL-STD-883, Method 5004, Class A (ref 34), with 240 hours burn-in at 125°C and computation of pre-post burn-in delta drifts of offset voltage and currents.
EXTERNAL ANOMALY Illegible identification - surface contamination prior to marking causes nonsolvent resistance to tests per MIL-STD-202, Method 215 (ref 2).	41	1. 100% Visual Inspection. 2. Screen for legibility of identification per requirements of MIL-STD-202, Method 215.
EXTERNAL ANOMALY X-ray rejection - formation of intermetallics Au-Al (gold-aluminum) because of overflow of gold-silicon chip bond eutectic to aluminum bond on substrate trace	42	1. 100% Precap Visual Inspection per MIL-STD-883 (ref 34). 2. 100% Radiographic Inspection. 3. High Temperature Storage per MIL-STD-883. 4. Thermal Cycling per MIL-STD-883. 5. Shock, Acceleration, Variable Frequency Vibration.
EXTERNAL ANOMALY Misidentification	43,44	1. 100% screening per MIL-STD-883, Method 5004, Class A (ref 34). 2. Perform interim Electrical Tests at 25°C prior to Temperature Bake to determine correctly marked devices.

PROBLEM AREA/ Cause	ALERT ITEM NO.	SUGGESTED ACTION - SCREEN (see "Screening Inspections and Tests")
EXTERNAL ANOMALY Damage to package	45	1. Do not conformal coat bases of DIP packages. 2. Visual examination for glass-to-metal seal problems.

SCREENING INSPECTIONS AND TESTS

OBJECTIVE.

Screening of microcircuits has been standardized in the form of MIL-STD-883 (ref 34). This standard was generated to establish standardized forms of screening tests applicable to integrated microcircuits. Reliability of devices destined for space flight and/or avionics usage requires extensive controls and tests to eliminate infant mortality failures and assure a reliable end product.

The following discussion briefly describes the various screens in their logical sequence as required by the different classes of screens shown in Method 5004 of MIL-STD-883. The failure mechanisms normally weeded out as a result of the test are also noted.

1. PRECAP VISUAL INSPECTION — MIL-STD-883, METHOD 2010, Conditions A and B (ref 34)

   Purpose. This inspection is designed to eliminate failures due to workmanship anomalies before the device is sealed. It ensures that the internal components of an integrated circuit as listed below are within the design constraints of the device.

   Procedure. The inspections performed on monolithic and hybrid integrated circuits are normally sequenced just prior to the lid sealing operation. Devices to be examined are placed on firm fixturing devices in order to prevent any damage during the handling and inspection. Optical microscopes capable of the desired magnifications (100X and 45X or greater) are utilized with the appropriate illumination. Inspection is based on two magnifications, i.e., 100X minimum for all anomalies associated with the chip surface and 45X minimum for all anomalies associated with the over-all interior of a monolithic IC package or associated substrate circuitry of a hybrid circuit. Criteria used for rejection will be based on the choice of Test Conditions A or B. Test Condition A provides a rigorous and detailed procedure for internal visual inspection intended for high reliability monolithic or hybrid microcircuits.

   Characteristics Inspected:

   Monolithic IC

   Package — exterior and interior

   Package leads — damage, corrosion, plating, and finish

   Chip bonding — eutectic or noneutectic, flatness, and adequacy of bond

   Wire bonding — thermocompression ball bonds, ultrasonic bonds (gold and aluminum), stitch bonds, wedge bonds, parallel gap welds, and lead dress

   Chip surface — diffusion anomalies, silicon dioxide anomalies (e.g., voids, pinholes), metallization anomalies (e.g., unetched metal, smears, voids, scratches), and general workmanship characteristics (e.g., freedom from etchant strains, polymeric residues, and foreign material conductive or nonconductive)

   Effectiveness. The effectiveness of a precap visual inspection to established criteria found in MIL-STD-883, Method 2010, Conditions A or B, cannot be overemphasized. The rejection of anomalous devices accounts for the greatest ratio of rejections over the whole span of processes an integrated circuit undergoes. Precap visual inspection, when properly conducted and on a 100 percent basis, eliminates most failures commonly found in the "infant mortality" section of a reliability "bathtub" curve.

2. STABILIZATION BAKE — MIL-STD-883, METHOD 1008 (ref 34)

   Purpose. This test is performed at elevated temperatures indicated by the choice of a test condition letter pertinent to the required temperature. Its purpose is to determine effects of elevated temperature on microcircuits with no electrical stresses applied. Forty-eight hours duration is normally specified but not necessarily limited to this figure. The test is applicable to Classes A, B, and C of Method 5004.

Effectiveness. This test method serves as an effective screen for devices having the following failure modes/ mechanisms:

a. Degradation of junction characteristics due to contamination.

b. All oxide and diffusion anomalies, such as mask misalignment, masking flaws, oxide pinholes, oxide voids, nonuniform thicknesses of oxide, and improper doping levels of active or passive elements.

c. Contamination effects from etchant residues and photoresist residues.

d. Metallization problems such as improper alloying temperatures or time, misalignments of metallizations, contamination, and separation.

e. Lifted or cracked dies.

f. Lifted lead bonds and plague formations at bonds.

g. Inversion or channelling.

h. Hermeticity failures as a result of faulty glass-to-metal seals.

3. THERMAL SHOCK — MIL-STD-883, METHOD 1011 (ref 34)

Purpose. This test exposes components to sudden extreme temperature changes. The resistance of the components to sudden temperature variations is verified following the test by visual inspection for damage such as cracking, opening of terminal seals and case seams, and permanent change of operational electrical characteristics as determined by post test measurements, or by die separation.

Procedure. Specified choice of test condition letters of this method, determines choice of extreme temperatures to be used. Apparatus used consists of temperature controlled baths of suitable liquids held at the specified temperature extremes and in close proximity to one another to facilitate specified transfer times between fluids. The devices tested are immersed in the high temperature bath for a specified period of preconditioning then transferred to the cold temperature extreme bath and held there for 5 minutes before being transferred back to the high temperature bath and again held at this high temperature for 5 minutes. Transfer time shall not exceed 10 seconds. Unless specified otherwise, the total number of cycles used shall be 15 cycles. One cycle consists of transfer from hot to cold then back to the hot bath. This test is required of Class A screening only.

Effectiveness. Thermal shock tests induce stresses on bulk silicon, metallization and its interfaces, and bonding agents. The marginal failures which would normally pass other tests invariably fail a thermal shock test, providing the appropriate shock temperature ranges are invoked. This test would weed out mechanically poor wire bonds (thermocompression and/or ultrasonic), cracked silicon chips, potential crystal dislocation failures, weak bonds caused by intermetallics, microcracked contact window cutouts (metallization separations), improperly bonded chip, and improper lid seals.

4. TEMPERATURE CYCLING — MIL-STD-883, METHOD 1010 (ref 34)

Purpose. Like Thermal Shock, this test subjects devices under test to extremes of elevated temperature. Unlike Thermal Shock, the apparatus used involves twin temperature chambers where the temperatures therein are maintained within the specified tolerances of the temperature extreme. This test determines the effect of device exposure to the specified temperature extremes and their resistance to its effects are verified by visual examination for delamination of finishes, cracking and/or crazing of the packages, damage to case seams and terminal seals, and permanent electrical characteristic changes.

Procedure. Samples are placed in the cold temperature chamber and allowed to stabilize for 10 minutes after which they are transferred to the high temperature chamber going through a room ambient temperature region. The transit time through the 25°C region shall not exceed 5 minutes. The duration of stabilization in the high temperature chamber is 10 minutes, following which, the devices are again transferred to the 25°C region and remaining in the 25°C region no longer than 5 minutes. The foregoing constitutes one cycle and unless specified otherwise, the test is run for ten cycles. The temperature extremes are specified by the choice of a test condition letter.

Effectiveness. This test serves as an effective screen for the following failure modes/mechanisms and especially for all aluminum metallization systems:

a. Chip: cracks in chip, chip-outs and contamination, degradation of characteristics, and chip separation

b. Passivation: pinholes, voids

c. Diffusion anomalies: masking misalignments, faulty masks, contamination effects, and faulty doping of active/passive elements

d. Chemical contamination: results of etchant residues or photoresist residues

e. Metallization anomalies: opens, near opens, potential shorts, intermittent shorts, scratches, pinholes under metallization, corrosion effects, thin metallization (especially over oxide steps), separation at steps, and improper alloying due to temperature or time

f. Wire bonds: lifted bonds, contaminated bonds, and cracked bonds

5. MECHANICAL SHOCK — MIL-STD-883, METHOD 2002 (ref 34)

Purpose. This test determines the capability of electronic components to withstand suddenly applied, moderately severe mechanical shocks or stresses as a result of abrupt changes in motion produced by rough handling during transportation or at rocket ignition. Damage to internal elements may occur or permanent changes to the operating characteristic may result.

Procedure. The devices under test are rigidly mounted on a level and sturdy shock test apparatus with adequate protection from damage for the device leads. Selection of a test condition letter determines the shock level required. Unless otherwise specified, the device is subjected to 5 blows of pulse duration between 0.1 to 1.0 msec in two directions of each of three axes. The g force level pertaining, would be Condition B and is 1,500 g level (peak).

Effectiveness. This test effectively eliminates devices with the following potential anomalies:

a. Improper lead dress

b. Inadequately bonded wire bonds

c. Inadequately bonded chip bonds

d. Mobile contaminant particulates

e. Intermittent opens

f. Cracked substrates

g. Inadequate lid seals

Defectives are detected by subsequent electrical testing, X-rays and/or hermetic seal tests.

6. CENTRIFUGE OR CONSTANT ACCELERATION — MIL-STD-883, METHOD 2001 (ref 34)

Purpose. This test is used to determine the effect of a centrifugal force on components of a microcircuit device. Various types of structural or mechanical weaknesses are brought to light and which are not normally detected in shock or vibration tests. It is an excellent test to eliminate devices with less than nominal mechanical strengths in the internal metallization system, lead systems, chip and substrate attachments, and lid seals.

Procedure. Test Condition letter chosen, specifies the g stress level of the test. Devices under test are securely mounted in their specified axis in a test fixture. The Y_1 axis is normally used and the duration of centrifugal acceleration of 20kg, is usually one minute.

Effectiveness. This test effectively screens out devices with inadequate lead dress, wire bonds, die bonds, substrate bonds, cracked substrates, and lid seals.

7. HERMETIC SEAL TESTS — MIL-STD-883, METHOD 1014 (ref 34)

Purpose. This test determines the effectiveness of the seal of devices under test. Its purpose is to weed out cavity devices with potentially defective seals which show up as latent failures when exposed to moisture or gaseous contaminants.

Procedure. This test involves the use of two test methods for fine leaks and two test methods for gross leaks.

FINE LEAK:

Test Condition A — Tracer Gas (helium) Fine Leak. The devices under test are pressurized in an helium atmosphere for a period of time and pressure specified in the test specification. They are then removed to an evacuation chamber where a vacuum is applied and the leak is measured through use of a mass spectrometer.

Test Condition B— The devices are placed in a radioactive tracer gas (krypton-85) activation tank which had been previously evacuated to a 0.5 mm Hg level. The devices are then subjected to a minimum of 5 atmospheres absolute pressure of krypton-85/dry nitrogen mixture for a minimum of 12 minutes, actual pressure and soak time shall be predetermined by a mathematical formula given in MIL-STD-883. Following pressurization, the krypton-85/dry nitrogen mixture is evacuated back to storage until a 0.5 mm Hg vacuum exists in the activation tank. The tank is then backfilled with air (air wash). The devices are then removed from the tank and leak tested within 4 hours after removal with a scintillation crystal-equipped counting station. The actual leak rate of the component is then calculated with an equation per Method 1014 of MIL-STD-883.

GROSS LEAK:

Test Condition C — Fluorocarbon Gross Leak. This test involves the use of two steps. Step No. 1 checks for leak rates $\geq 10^{-3}$ atm/cc/sec, and consists of an immersion test in fluorocarbon FC43 held at 125°C. The leak will be indicated by a single bubble or a stream of bubbles emanating from the body of the device.

Step No. 2 subjects devices under test to a vacuum purge where 1 torr of vacuum pressure is applied for 1 hour. Then, without breaking the vacuum condition, the devices are immersed in a bomb fluid FC-78 and pressurized for 3 hours at either 90 psig or 50 psig, dependent on internal cavity size. The pressure is removed at the end of this time and the devices are retained in the bath until ready for the next phase of the test. The devices to be tested are removed singly from the bath and dried for 3 minutes, then immersed in the indicator fluid FC43. Leakers are identified by an emanated stream of bubbles or a single bubble.

Test Condition D — Penetrant Dye Gross Leak. Devices tested to this condition, are subjected to a pressurization in the fluid for 2 hours at 100 psig minimum. Thereafter, they are removed and washed in a cleaner like acetone or trichloroethylene followed by an alcohol rinse. They are then examined under 7X to 20X magnification using an ultraviolet light. Evidence of dye penetration to package cavity constitutes a leak failure.

Effectiveness. This test eliminate devices with defective seals between lid and package or between external leads and package. Defective glass seals or metal-to-metal, or metal-to-glass seals will be indicated as either a fine leak or a gross leak dependent on the size of the leak.

8. BURN-IN SCREEN — MIL-STD-883, METHOD 1015 (ref 34)

Purpose. Devices subjected to this screen are operated under specified test conditions and temperature. Devices with inherently weak electrical and/or mechanical characteristics are eliminated as evidenced by failures following post-burn-in electrical measurements. Time and temperature dependent failures are accelerated when subjected to an appropriate Power Burn-In screen.

Procedure. Selection of a test condition letter (A through E) determines one of five potential stresses with or without elevated temperature. Operational ac power testing similar to Test Condition E with or without temperature has been found to be most successful in eliminating time/temperature dependent failures. Pre- and Post-Burn-In electrical measurements must be specified. Unless otherwise specified, the test duration for Class A screen is 240 hours and that for Class B screen is 168 hours.

The five test conditions allow for the following stresses:

a. Condition A — Steady state, reverse bias

b. Condition B — Steady state, power

c. Condition C — Steady state, power, and reverse bias

d. Condition D — Parallel excitation

e. Condition E — Ring oscillator

Effectiveness. This test is effective in eliminating the following anomalies:

a. Metallization: devices having potential shorts, intermittent shorts or opens, near opens or shorts as a result of scratches or voids in metallization, near shorts caused by pinholes under the metallization, and corrosion of metallization.

b. Crystal defects: dislocations, irregular surfaces, cracked chip, diffusion anomalies, pinholes through oxide, contamination because of residues, and improper doping levels.

9. RADIOGRAPHIC INSPECTION — MIL-STD-883, METHOD 2012 (ref 34)/NHB 5300.4(3E)(ref 35)

Purpose. The purpose of this test is to detect internal defects within the microcircuit such as loose extraneous wires, solder extrusions, improper interconnecting wires, die mount integrity, and lid sealing surfaces.

Effectiveness. This test effectively eliminates defects normally occurring following lid seal, e.g., solder extrustions or mobile conductive particles. It also brings to light defects inherent in the process not visually detectable, e.g., die mount adhesion. Defects missed by visual examination are found through X-rays only if the material is not impervious to X-rays. Silicon and aluminum will not be visible on X-rays.

10. SCANNING ELECTRON MICROSCOPE METALLIZATION INSPECTION — GSFC-S-311-P-12A (ref 36)

Purpose. The purpose of this inspection is to assure the acceptable quality of metallization on integrated circuits, hybrid microcircuits, transistors, and other thin film devices. It should be noted that the current issue of the MIL-STD-883 does not accommodate usage of the above inspection nor of its specification.

Effectiveness. This inspection is performed during wafer fabrication processes immediately after metallization deposition and etch. It assures the acceptability of the metallization as a result of batch processing. It also assures the integrity of metallization on devices specifically at contact cutouts and at locations where oxide steps may be too steep to allow for even evaporation of the metallization at the step. In addition, this inspection eliminates faulty metallization as a result of microcracking, over or under etching, and metallization peeling.

Inspection is performed on a lot acceptance sampling basis and is delineated in the referenced specification originated by Goddard Space Flight Center.

DESIGN AND PRODUCTION CONSIDERATIONS FOR DIODE-TRANSISTOR-LOGIC (DTL) INTEGRATED CIRCUITS

General. The Diode-Transistor-Logic devices offer the following advantages:

1. Moderate speed: 10 to 80 nanoseconds
2. Good noise immunity
3. Low noise generation
4. High degree of logic flexibility
5. Relative economy

Assembly Flow. A typical DTL integrated circuit (Figure 17-1) and a typical assembly flow (Figure 17-2) are presented in the following pages. In Figure 17-1, the symbols located around the die periphery depict the die active elements and the various inputs and outputs with pin locations. These may be referenced to the schematic (Figure 17-1A). Figure 17-2 depicts a step-by-step process flow from wafer polishing to the finished product.

Controls. To assure a high reliability end product, various rigid controls and checks are instituted throughout the processing. The critical processes with their attendant potential problems are so indicated by the accompanying key to the problem codes found on the foldout in the Appendix.

Tests. Various environmental and electrical tests are part of the process flow. These tests are necessary to assure stability of the various parameters and also as a check of the various preceding process controls.

Screens. Reliability screening follows the completion of all manufacturing processes. These high reliability tests follow the sequence delineated in MIL-STD-883, Method 5004 (ref 34) for the various classes of reliability. The hi-rel screening serves an important function by eliminating potentially weak or marginal operating devices commonly termed as infant mortality failures. Reliability screening commences with 100 percent Pre-Seal Visual Examination and on through final external examination. It includes Power Burn-In for a minimum period of 168 hours and in some cases, High Temperature Reverse Bias Burn-In for 72 hours minimum with delta criteria invoked.

Typical DTL. A typical DTL ceramic flatpack consists of the IC monolithic silicon chip with aluminum metallization. This chip is glass-frit mounted in the ceramic package (Al_2O_3 90%) and hermetically capped with a similar material. Wiring between the chip bonding pads and the lead frame (Alloy 42) is accomplished through the use of 0.001 inch aluminum wire (Al 99%, Si 1%) ultrasonically bonded at both terminations.

TYPICAL DTL INTEGRATED CIRCUIT DESIGN (Figure 17-1)

ITEM NAME	MATERIAL OF CONSTRUCTION
Wafer	Silicon
Aluminum Metallization	Aluminum 99.999%
Gold Charge	Gold 99.999%
Lead Frame	Alloy 42
Base	Al_2O_3
Aluminum Wire Interconnects	Aluminum 99%, Silicon 1%
Cap	Al_2O_3

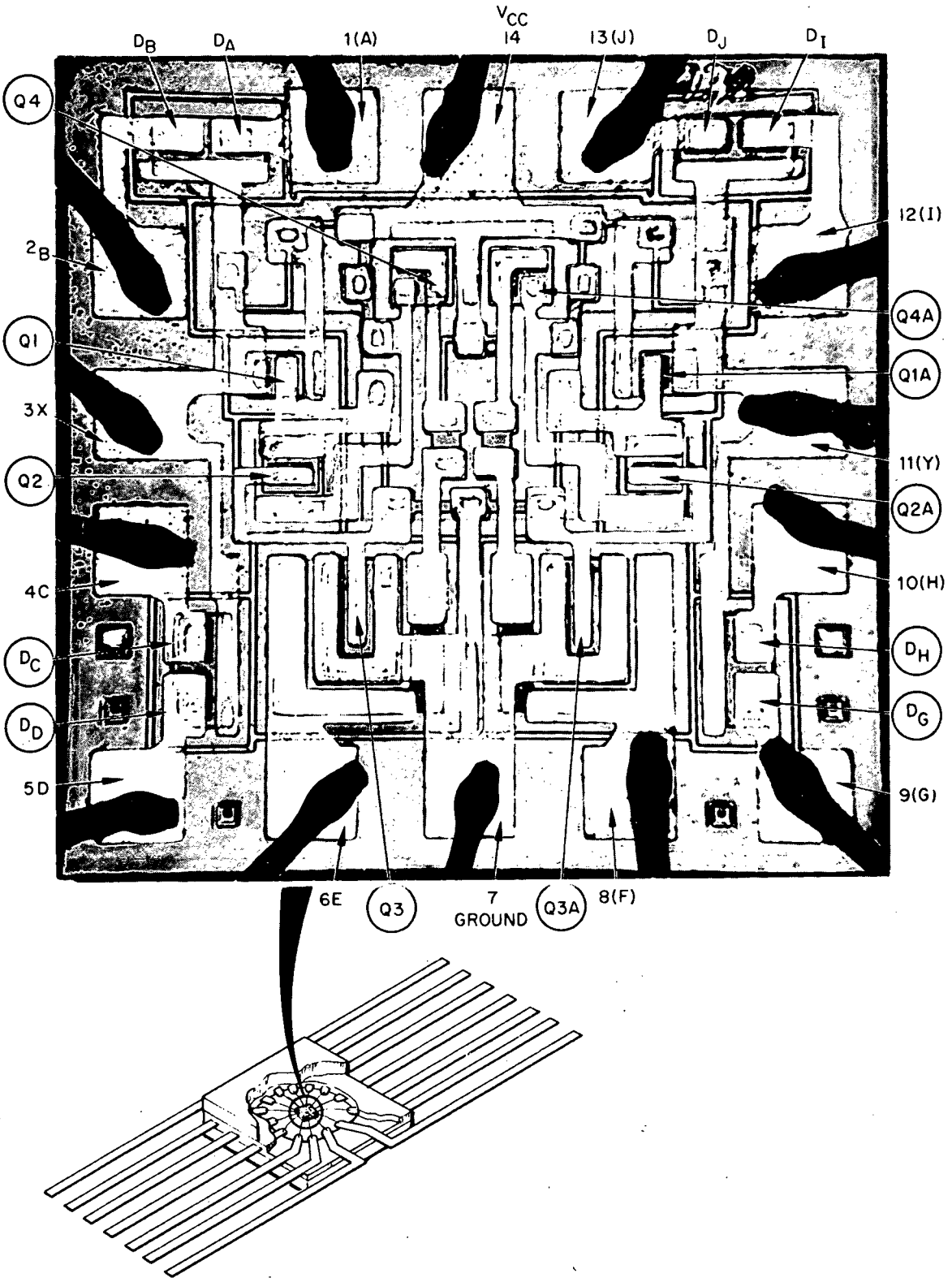


Figure 17-1. Typical DTL Integrated Circuit

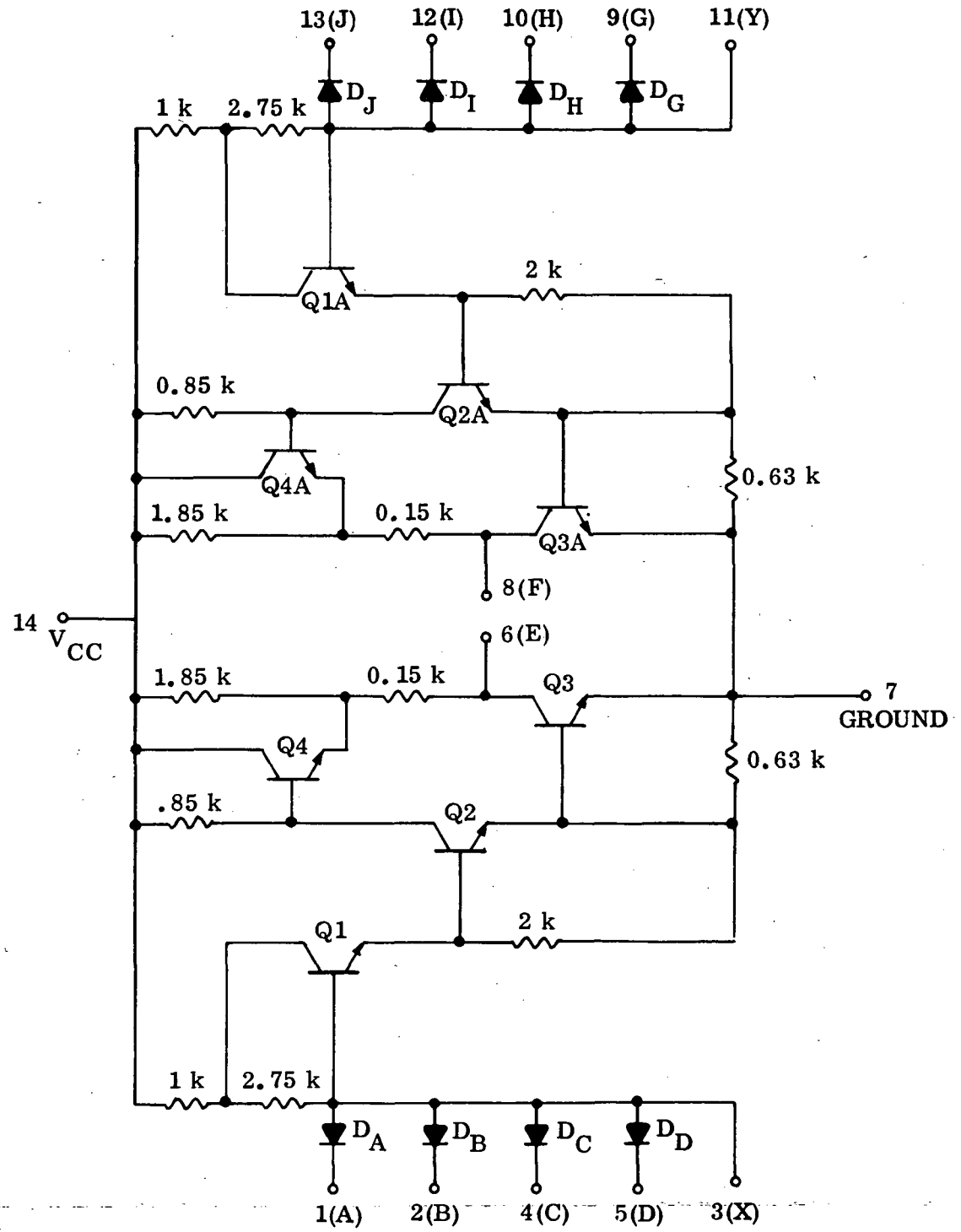


Figure 17-1A. Typical Schematic Diagram - DTL

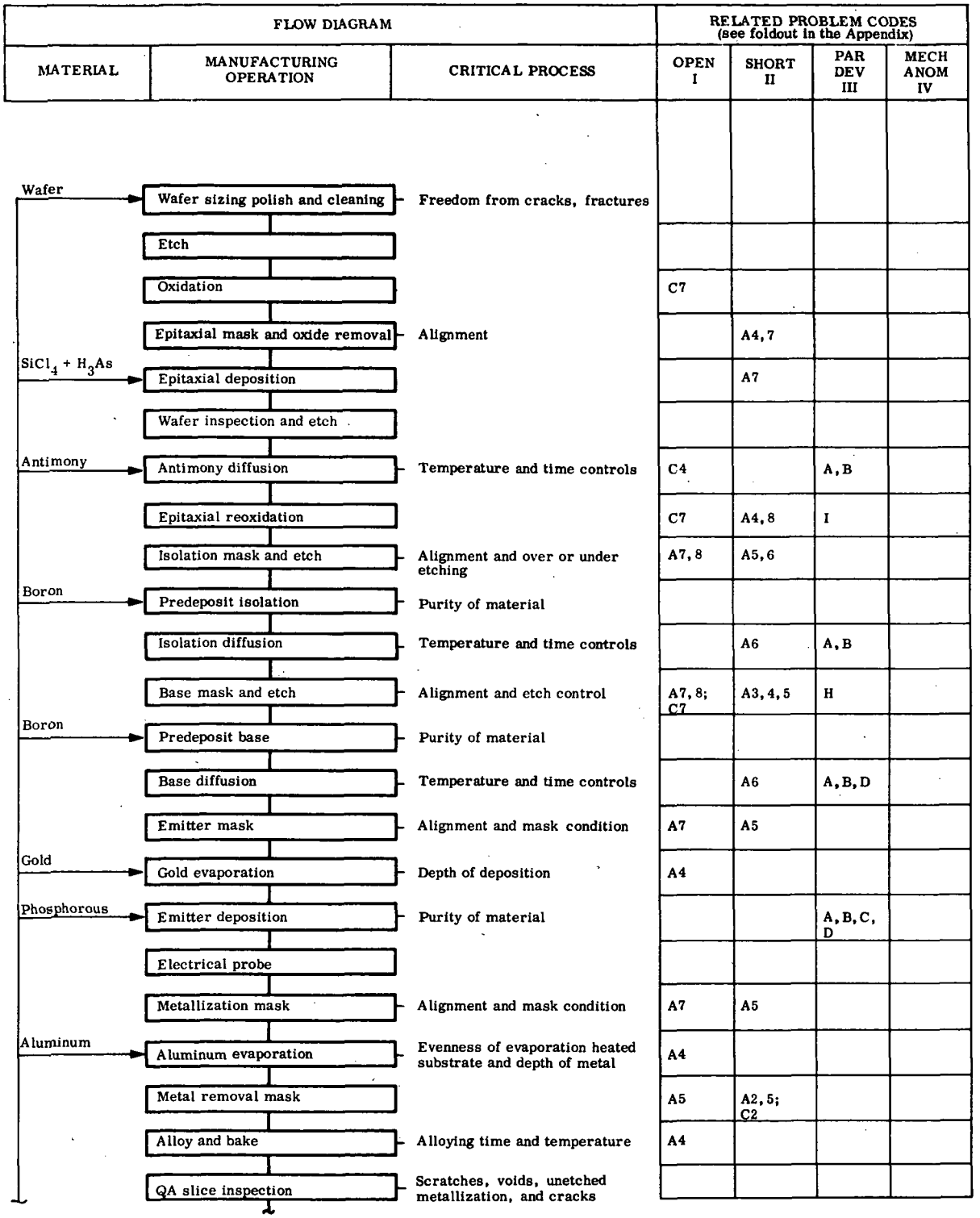


Figure 17-2. DTL - Typical Assembly Flow with Related Problem Codes

FLOW DIAGRAM			RELATED PROBLEM CODES (see foldout in the Appendix)			
MATERIAL	MANUFACTURING OPERATION	CRITICAL PROCESS	OPEN I	SHORT II	PAR DEV III	MECH ANOM IV
	Wafer electrical test	Parameters tested			A, B, C, D, E, F	
	Scribe and break wafer into dice	Controls against misalignment, cracks, and chip-outs	C1	A11; C7		
Frame and Base	Mount I.C. and clean	Control of glass frit, chip orientation and cleaning process	C1, 2	A8, 12; C4, 7; D1		
	Ultrasonic bond	Bonder pressure/timer control	B(all)	B(all)		
	100% preseal inspect	Per MIL-STD-883, Method 2010, Cond. A.	all	all	G, H	
Cap	Seal	Control of hermeticity		D2, 3		D, E
	Thermal cycle and centrifuge		B1, C1, 2, 3	A9; B2, 3, 8; C5, 7	F	C, D
	Lead straightening and plating		B4	D4		D
	Leak test, fine and gross			D3		E
	Lead clip					D, H
	Electrical test, final	Controlled parameters	all	all	A-F	B, D
	Visual inspect – external	Damage and I.D. control				A, B, C, D, E, G, H, I
	Centrifuge & seal — Inspect	Weak bonds control	B1; C1, 2	A9; B2, 3, 4, 8; C5, 7	K	C, D
	Inspect electrical and visual		all	all	A-F	all
	Sample AC parameters	Checks device response			H, I	
	Mark, straighten lead and serialize					A, D
	Functional test, AC				A-F	
	Power burn-in	Eliminates weak/marginal devices			A-F	
	Post burn-in electricals		all	all	A-F, K	B, D
	High temperature reverse bias	Eliminates channeling/ inversion prone devices			A, B, C	
	Post HTRB electricals				C	
	X-rays — Inspect	Checks package interior	B6	A9; B8; C, 5, 7; D1, 3		F
	Functional and visual sample			D4		A, B, C, D, E, G, H, I
	Ship					

Figure 17-2. DTL - Typical Assembly Flow with Related Problem Codes

DESIGN AND PRODUCTION CONSIDERATIONS FOR TRANSISTOR-TRANSISTOR-LOGIC (TTL) INTEGRATED CIRCUITS

General. Transistor-Transistor-Logic or TTL is a later development of the logic system technology. It utilizes the silicon planar epitaxial manufacturing technique and as such is somewhat similar to Diode-Transistor-Logic technology of the preceding section. This TTL section presents the differences in the two technologies and circuit/process dissimilarities. The potential problem areas related to the manufacturing sequences and keyed to the problem codes (see Appendix) are incorporated.

Design Advantages. The speed/power advantages of the TTL integrated circuit are optimized in the family of devices available. The inherent advantages of the saturated logic and monolithic semiconductor technology provides for improved performance in these devices where transistors are used instead of diodes and resistors in the circuit. Fluctuations in currents are buffered by the use of transistors and improved performance results. The use of multiple emitters in the input transistor replaces the conventional input diode and the active pull-up at the output eliminates slow rise times which are common to passive pull-ups.

The TTL family of digital logic offers the following advantages:

Approximately 100 distinct logic functions to choose from

Three compatible performance ranges, i.e., 54/74 standard power, 54H/74H high power, and 54L/74L low power

High speed — typical delays of 10 nsec

High dc noise margin

Low output impedance provides low ac noise susceptibility

Low power dissipation

High fan-out capability

Compatible with other current-sinking logic devices — DTL or other TTL

Basic Construction. The basic TTL gate on a monolithic silicon chip consists of a diffused multiemitter input transistor and its associated current gain drive circuitry. The multiemitter transistor and the other drive transistors are fabricated by diffusing an isolated collector region. The base region is then diffused into this collector region and the several emitter regions are diffused as separate areas within the base region. Between diffusions, there are repetitive steps consisting of oxide growth, masking, etching, isolation, deposition, then diffusion.

The conducting paths in this TTL integrated circuit are accomplished by use of deposited metals, i.e., molybdenum-gold. Gold wires (.001 inches diameter) are then utilized for external connections through use of thermocompression gold ball bonds and wedge bonds.

Isolation of individual elements and circuits is achieved through use of reversed biased junctions. This method of isolation is adequate for many applications, is easier to fabricate, and is the most common isolation method employed in volume production lots.

The TTL chip of this typical sample is eutectically bonded within a metal package which is hermetically sealed (solder-sealed) at completion of the wire bonding operation, and the various cleaning and visual inspections.

Controls. The various rigid process controls necessary in the production of the DTL and other integrated circuits are again necessary in producing high reliability TTL. Reliability screening is included in the typical manufacturing process flow which follows. The 100 percent screening commences with precap visual inspection and includes environmental and electrical tests, 240 hours power burn-in, X-ray and final visual inspections.

Assembly Flow. A typical TTL integrated circuit (Figure 17-3) and a typical assembly flow (Figure 17-4) are presented on the following pages. In Figure 17-3, the symbols located around the die periphery depict the die active elements and the various inputs and outputs with associated pin locations. These may be referenced to the schematic (Figure 17-3A). Figure 17-4 depicts a step-by-step process flow from wafer polishing to the finished product.

TYPICAL TTL INTEGRATED CIRCUIT DESIGN (Figure 17-3)

ITEM NAME	MATERIAL OF CONSTRUCTION
Wafer	Silicon
Die Metallization	Sputtered gold with evaporated molybdenum and platinum
Lead Frame	Gold plated Kovar
Package	
Top and Bottom	Gold plated Kovar
Sides	Gold plated Kovar with Type 7052 glass feed-through
Wire Interconnects	Gold wire, 1 mil

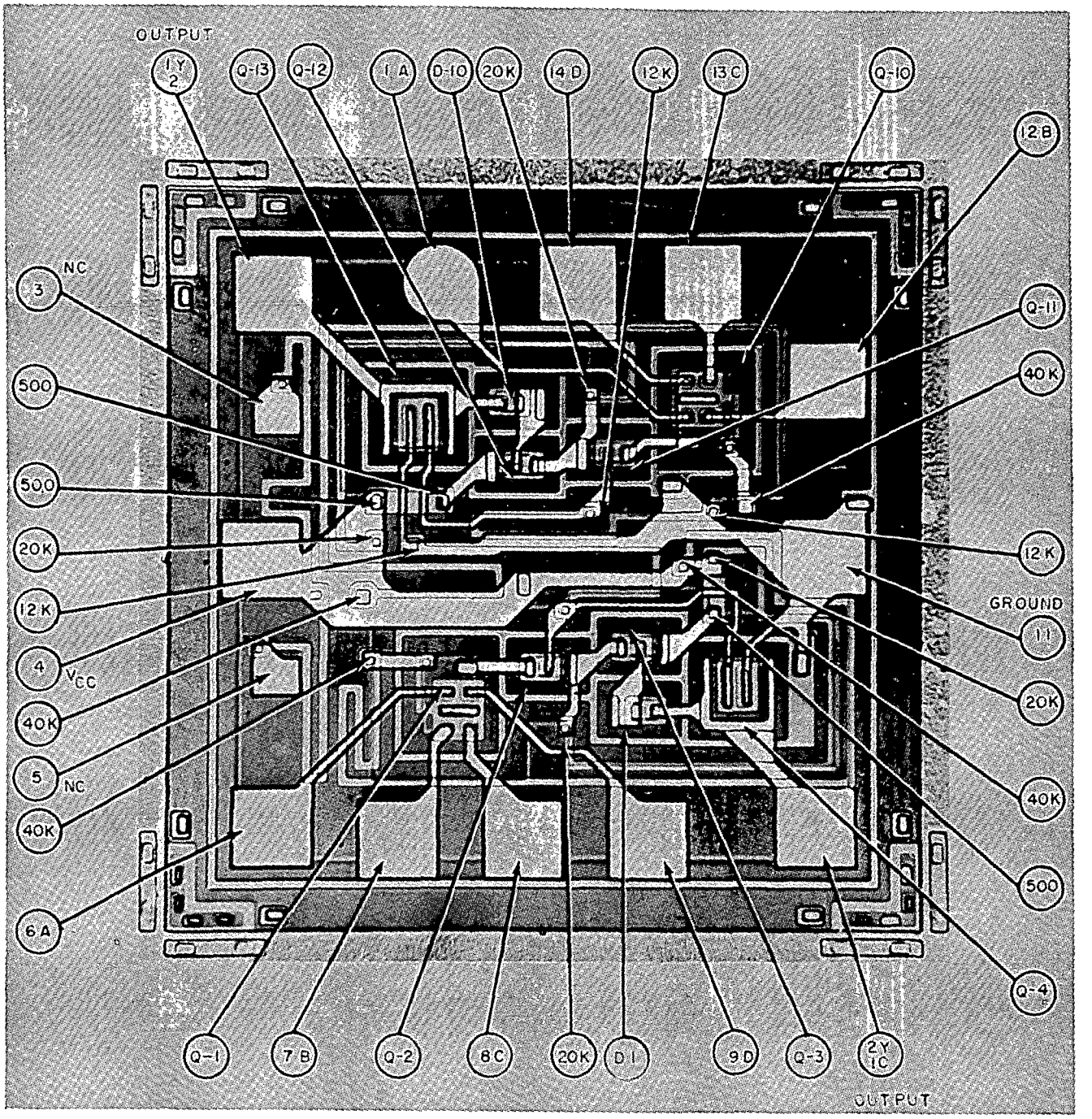


Figure 17-3. Typical TTL Integrated Circuit

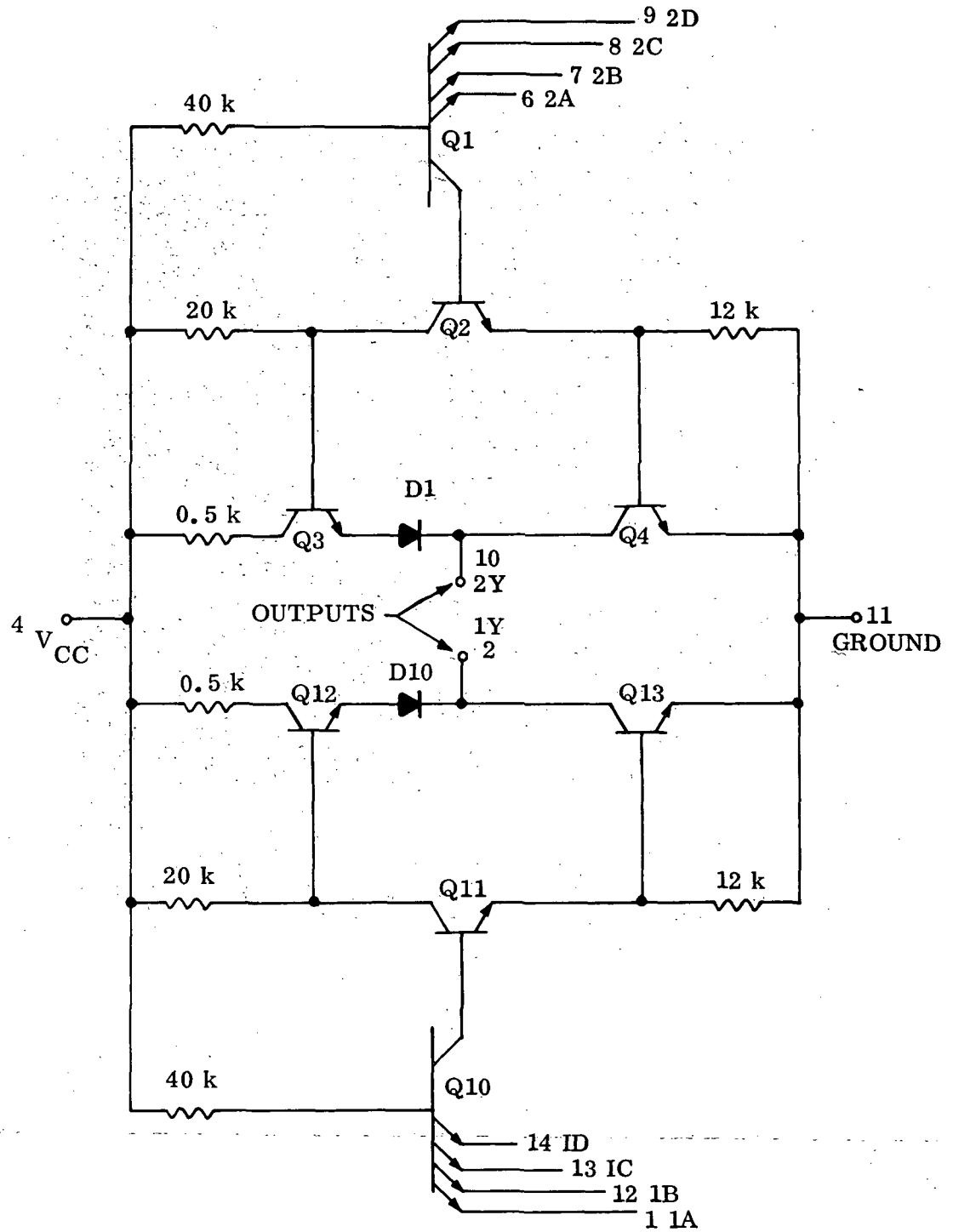


Figure 17-3A. Typical Schematic Diagram - TTL

FLOW DIAGRAM			RELATED PROBLEM CODES (see foldout in the Appendix)			
MATERIAL	MANUFACTURING OPERATION	CRITICAL PROCESS	OPEN I	SHORT II	PAR DEV III	MECH ANOM IV
Epitaxial slice	Oxidation		C7	A4-7		
	Isolation mask and etch	Alignment and etch time	A8; C4	A5, 6, 7		
Boron	Isolation, diffusion, and deposition	Purity of material and time/temperature controls	A7, 8	A5, 6, 7		
	P+ mask and etch	Alignment and etch time	A7, 8	A5, 6, 7	D	
Boron	P+ deposition and diffusion	Purity of material and time/temperature diffusion	A7, 8	A5, 6, 7		
	Base mask and etch	Alignment and etch time	A7, 8	A5, 6, 7	D	
Boron	Base deposit and diffusion	Purity of material and time/temperature diffusion	A7, 8	A5, 6, 7	D	
	Emitter mask and etch	Alignment and etch time	A7, 8	A5, 6, 7	D	
Phosphorous	Emitter deposition and diffusion	Purity of material time/temperature diffusion	A7, 8	A5, 6, 7	D	
	Contact mask and etch	Alignment and etch time	A7, 8; C5	A5, 8, 9; C2		
	Sintered platinum deposit					
Moly-Gold	Mo sputter - Au evaporation	Thickness of metal	A4; C6	A2, 3, 5, 9, 10; C2, 7	H	
	Metal etch and alloy	Etch time and alloy temperature	A4, 6 C5	A1, 2, 3, 7, 9; C1, 2	H	
	Electrical probe	Critical parameters and tolerances checked	A1-9; C1-7	A(all); C1-4, 7	A-L	
Headers	Scribe and break	Scribe alignment and cleavage accuracy	C1, 4, 5, 7	A9, 11		
Preforms	Bar mount, hot (scrub)	Temperature and motion and cleanliness of header	C2	A12	G	
Gold Lead Wire	Ball bond lead	Pressure and temperature of bonder	B1-9	B1-8		
	Precap visual (40X and 100X)	Per requirements of MIL-STD-883, Method 2010, Cond. A.	all	all	G, H	G, H
Lids	Seal (stitch weld)	Hermeticity of seal and inertness of sealing chamber		B4; C7; D1, 3		E

Figure 17-4. TTL - Typical Assembly Flow with Related Problem Codes

FLOW DIAGRAM			RELATED PROBLEM CODES (see foldout in the Appendix)			
MATERIAL	MANUFACTURING OPERATION	CRITICAL PROCESS	OPEN I	SHORT II	PAR DEV III	MECH ANOM IV
	Stabilization bake	Eliminates surface instabilities			A, B, C, F	
	Thermal cycle and centrifuge	Eliminates weak bonds	B1, 3; C1, 2, 3	A7, 8, 9, 13 B2, 3, 4, 8; C3, 7; D1, 3, 4	K	C, D, E
	Fine leak	Checks hermeticity		D3		E
	Electrical test 25°C, 125°C, -55°C	Assures design specifications and operation at temperature extremes	all	A(all); B(all); C(all); D1, 2, 4	all	B, D, H
	Gross leak	Checks hermeticity		D3		E
	Mark	Lead No. 1 orientation mark and part identification are critical				A, B
	X-ray	Checks cavity and lid seal integrity	B6	A9, 12; B2, 4, 8; C5, 6, 7 D(all)		F, H
	Record data, burn-in and re-record data					
	Electrical test 25°C, 125°C, -55°C	Double checks stability of previous measurements	all	A(all); B(all); C(all); D1, 2, 4	all	B, D, H
	Q. A. electrical test	Quality audit	all	A(all); B(all); C(all); D1, 2, 4	all	B, D, H
	Visual examination and clip leads					all
	Fine leak	Seal integrity		D3		E
	Q. A. hermeticity test	This checks glass-to-metal seals at lead egress from metal package and lid seal		D3		E
	Packing					C
	Q. A. final external inspection					A, B, D
	Ship					

Figure 17-4. TTL - Typical Assembly Flow with Related Problem Codes

DESIGN AND PRODUCTION CONSIDERATIONS FOR LINEAR INTEGRATED CIRCUITS

General. The design of linear circuits involves the selection and interconnection of an optimum combination of active and passive components to accomplish a signal-processing function with maximum efficiency and minimum cost.

Linear integrated circuits achieve this objective through use of simultaneous fabrication techniques and interconnections, and the effective use of transistor and diode elements to substitute for inductive and capacitive reactances. The improvement of an already existing technology or technique, rather than use of radically new processes, has led to the current state-of-the-art proliferation of linear circuits. The introduction in 1965 of the 709, the first monolithically constructed integrated circuit amplifier, has led to today's wide acceptance of the Linear Operational Amplifier, the most versatile amplifier in the linear integrated circuit field. It will not be possible to delve into all of the technical and application considerations; however, in the linear integrated circuit field current technology generally employs the six-mask silicon, planar epitaxial fabrication techniques not unlike those utilized in the fabrication of DTL/TTL digital integrated circuits.

Linear integrated circuits, by virtue of the wide variety of design requirements, fall into two general categories (1) general and widely accepted circuit configurations which lend themselves to a wide variety of circuit applications, in addition to being readily adapted to monolithic construction to warrant large volume production, and (2) customized circuit configurations for multiple circuit application in specialized high usage areas such as chroma demodulators, IF strips, oscillator circuits, etc.

It is the intent of this section to cover the first category of linear circuits which are readily available off-the-shelf but built as high reliability screened devices.

Design Advantages and Considerations. This discussion will comment on design advantages in a general way due to the multitude of designs. Considerations in design will be addressed specifically to that work horse of the linear field, the Operational Amplifier.

The design advantages in the linear intgrated circuits are self evident in the monolithic construction of these devices. The availability of linear integrated circuits in their various package configurations allows a designer a wide choice of packaging. The current lowered cost due to volume production of linear integrated circuits are welcome advantages. The not so evident advantages in the fabrication of linear integrated circuits result because the size (generally 45 to 55 mil square die) allows for batch processing of wafers, thus better process control on a large volume of similar devices. This in turn requires standardization of processing techniques, testing equipment, higher reliability, and improved quality controls. The design of the circuitry on the chip (because of the monolithic construction) allows for synthesis of electronic functions, optimization of active components, matching of component parameters, and better control of thermal effects by judicious placement of temperature sensitive components.

The operational amplifier, basically a very high-gain dc coupled amplifier using either external or internal frequency compensation and external feedback for control of response characterisitcs, employs three circuits dc coupled together. The input buffer, amplification, and output stages are designed for specific applications due to the impossible task of designing a universal operational amplifier to meet all criteria. Certain designs favor certain parameters like high frequency gain application at the expense of other performance criteria. Some designs favor higher dissipations at lower frequency gain, and some favor higher input impedances of FET inputs at the risk of higher leakages, hence the necessity for additional circuitry to offset the high leakage.

The input stage usually comprises a differential amplifier stage cascaded push-pull to a second stage for amplification. This buffer stage makes the circuit operation insensitive to variations in gain of the various transistors. The final stage or output stage utilizes Class "B" amplification to reduce quiescent current consumption.

In order to reduce the use of high value resistors for collector loads and base resistors, which in turn requires greater diffusion area, active collector loads and pinch resistors are used. These active collector loads are particularly effective with the low collector currents below 20 microamps. The active collector loads are essentially current sources and permit low current operation without large resistance values. Their use simplifies operational amplifier design while increasing impedance levels and reducing power consumption. They also provide for operation over a much wider range of voltages, offering high gain with very small voltage drops which is conducive to large linear voltage swings. Additionally, the use of active collector loads allows for higher gain per stage, hence fewer stages need be used. The design goal in designing the input stage would be to assure the dc bias levels at the input and the output are equal. This becomes a necessity to insure that the external feedback loop network connected between the input and output stages does not upset either

the differential or the common mode dc bias. The use of dual power supplies in most operational amplifier applications also mandate the establishment of a standard supply value for which both the input and output bias levels will be at zero voltage potential with respect to circuit ground.

The use of supergain transistors in the input stage of the amplifier can provide better than one order of magnitude improvement in the input current specification of monolithic operational amplifiers. Because these transistors operate at zero collector-base voltage, temperature leakage currents do not show up on the input. Due to their susceptibility to leakage currents under temperature conditions, and the fact that FET transistors cannot be operated without gate junction voltage, the supergain transistors are preferred over the FET inputs. Furthermore, matched pairs of supergain transistors exhibit typically low offset voltages of 0.5 millivolts and temperature drifts of 2 microvolts per degree centigrade compared with 40 millivolts and 50 microvolts per degree centigrade of the field-effect transsitors.

Temperature compensation within an operational amplifier poses some problems in the design of these circuits. Operation of an amplifier over a wide temperature range without appreciably affecting its characterisitcs is being achieved today in various operational amplifier designs. Design of amplifiers which have the characteristics change in a predictable way is also possible. Operation of integrated circuits so that they become insensitive to temperature is achieved through balanced configurations so that only matching of component parts is important. Due to the proximity of active devices on an integrated circuit chip, this close matching is relatively easy to achieve. The operation of some parameters must remain constant over the operating temperature range, e.g., the reference voltage for a regulator or the gain of a sense amplifier. This prediction of the V_{BE} over a temperature range can be determined through the known drift over temperature at a known current. This is another technique utilized by the integrated circuit manufacturers in optimizing designs.

Basic Construction. A typical integrated circuit operational amplifier is shown in Figure 17-5. This is either a LM101A or LM107, the difference between the two being the compensation capacitor for internal compensation used in the LM107.

The basic construction utilizes the basic 6-mask diffusion, photochemistry, metallization, and planar epitaxial technique; not unlike that found in the manufacture of the TTL and DTL devices described earlier.

Extreme care is used in the design of these operational amplifiers, especially in the design of the input and output circuitry to prevent latch-up problems that were so prevalent in the earlier 709 operational amplifiers. Metallization problems as a result of steep oxide steps are also prevented through the use of heated substrates, sloped oxide steps, and planetary dome rotation metallization depositions.

The integrated circuit chip, following scribing and visual examination, is mounted eutectically on metal headers (TO-99 or TO-100 metal cans). Wiring schemes are predominantly aluminum wires to aluminum chip surface metallizations. The bonds are achieved through ultrasonic bonding methods at both the chip bonding pads and the posts, or package lands (dual-in-line or flatpack devices).

Following assembly of the package header, but prior to sealing, a thorough precap visual examination is made of the device. For high reliability devices, it is imperative that this be conducted on a 100 percent basis in accordance with the requirements of MIL-STD-883, Method 2010, Condition A (ref 34). The devices are capped or sealed following a final cleaning step. Sealing is performed in an inert atmosphere to keep out contaminants and moisture. Extensive electrical testing under ambient and temperature extremes are then performed. Devices meeting the designed temperature range of -55°C to 125°C are categorized as full military temperature range devices, and those meeting lesser temperature extreme limits are relegated to either the industrial temperature range of -25°C to 85°C, or to the commercial temperature range of 0°C to 70°C. Only the full military temperature range devices are recommended for space flight applications.

Controls. The process and design controls normally found in the manufacture of high reliability digital devices are also required for the manufacture of linear integrated circuits. The difference between the two may lie in the design constraints necessary due to the complexity of the linear designs. In the digital devices the circuits are much simpler and are repetitive on any single chip, whereas on the linear devices various techniques are employed to produce the nearest equivalent to an ideal operational amplifier, i.e., infinite input impedance, zero offset currents and voltages, infinite open loop gain, and minimum output impedance; coupled with the desired short circuit proof innovations at input and outputs and latch-up prevention techniques. Linear devices, because of their linear transfer functions, are utilized in a variety of designs and applications. The multitude of designs necessitate extensive parameter testing over various temperature ranges. Testing of linear devices thus becomes highly sophisticated by calling for advanced state-of-the art instrumentation together with speed and accuracy. It can be said that the testing of linear devices involves more repetitive tests per device than for digital devices.

Screens. High reliability screening follows the procedure outlined in MIL-STD-883, Method 5004, Class A (ref 34). It commences at precap visual examination and continues through the various environmental and electrical tests of Method

5004. Power burn-in is performed in accordance with the optional methods outlined in MIL-STD-883, Method 1015. Dynamic burn-in, as opposed to static application of power to the device, is the preferred burn-in method. Burn-in for linear devices, unlike digital devices, requires a minimum of 240 hours at 125°C. Pre- and post-burn-in electrical measurements are made with delta drift computation of selected parameters (input offset voltage, input offset current, and small signal voltage gain) being a mandatory feature.

Assembly Flow. Figure 17-6 depicts a typical assembly flow for the manufacture of an internally compensated operational amplifier (LM107). It follows a methodically sequenced set of operations, from wafer sizing and polishing to final test, inspection, and shipping.

TYPICAL LINEAR INTEGRATED CIRCUIT (Figure 17-5)

ITEM NAME	MATERIAL OF CONSTRUCTION
Chip to Header Bond	Gold-silicon intermetallization
Seal	Glass
Stand-off	Ceramic-alumina
Leads	Kovar, gold plated, MIL-STD-1267, K (ref 6)
Header	Kovar, gold plated
Wafer	Doped silicon with phosphorous doped silica glass passivation on top and mounted via a gold preform on base
Interconnect	Aluminum with 1 percent silicon
Metallization (not shown)	Aluminum, 99.99 percent

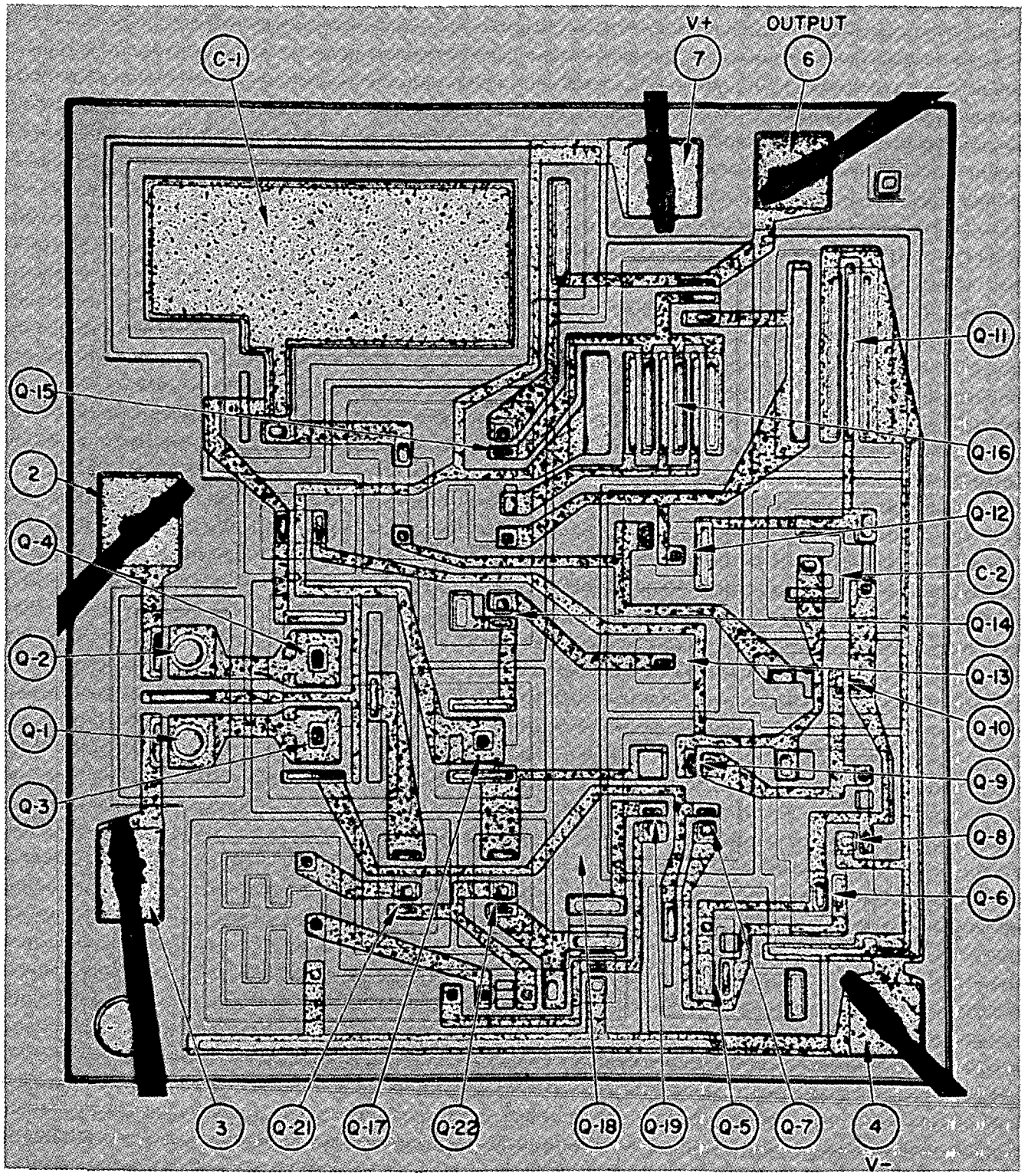


Figure 17-5. Typical Linear Integrated Circuit

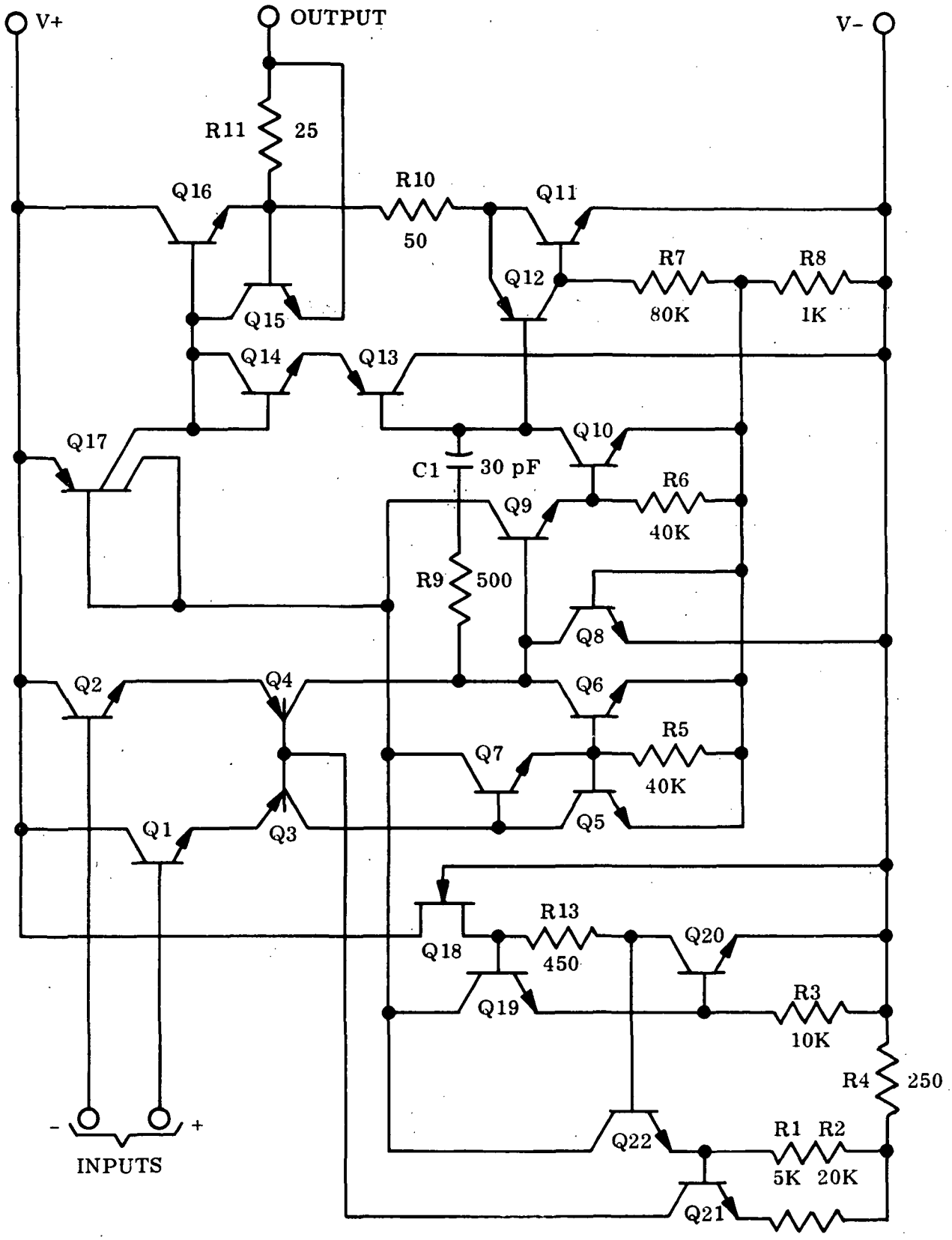


Figure 17-5A. Typical Schematic Diagram - Linear Integrated Circuit

FLOW DIAGRAM			RELATED PROBLEM CODES (see foldout in the Appendix)			
MATERIAL	MANUFACTURING OPERATION	CRITICAL PROCESS	OPEN I	SHORT II	PAR DEV III	MECH ANOM IV
Wafer	Wafer sizing and polishing	Freedom from cracks and fractures				
	Oxidation		C7			
	Epitaxial mask and oxide removal	Alignment		A4,7		
Antimony	Antimony diffusion	Temperature and time controls	C4		A,B	
$SiCl_4 + As_5H_3$	Epitaxial deposition			A7		
	Epitaxial reoxidation		C7	A4,8	I	
	Isolation mask and etch	Alignment and over-or under-etching	A7,8	A5,6		
Boron	Predeposit isolation	Purity of material				
	Isolation diffusion	Temperature and time controls		A6	A,B	
	Base mask and etch	Alignment and etch control	A7,8; C7	A3,4,5	H	
	Iso-diode check	Breakdown of substrate diode				
Boron	Predeposit base	Purity of material				
	Base diffusion	Temperature and time controls		A6	A,B,D	
	Emitter mask and etch	Alignment and mask condition	A7	A5		
	BV_{CBO} check	Collector/base breakdown. Extremely critical in use of punch-through transistors				
Phosphorous	Emitter deposition	Purity of material and depth of diffusion			A,B,C,D	
	Metallization mask and etch	Alignment and degree of etch controls and mask condition	A7	A5		
Aluminum	Aluminum evaporation	Evenness of evaporation, heated substrate, planetary dome usage, and depth of metal	A4			
	Metal removal mask		A5	A2,5; C2		
	Alloy	Alloy time and temperature	A4			
	Electrical probe	Electrical breakdown and continuity				
Phosphorous and Silane	Glassification (Vapox)	Depth of coverage and pinholes				
	Mask windows and etch	Alignment and pad exposure				
	Wafer electrical test	Parameters tested	A1,5	A1-11,14	A-F	
	Scribe and break wafer into dice	Misalignment, cracks, and chipouts	C1	A11; C7		
Header and Preform	Mount IC and clean	Eutectic scrub, die orientation, and cleaning process	C1,2	A8,12; C4,7; D1		
	Ultrasonic bond leads	Bonder pressure and timer control	B(all)	B(all)		
	100% precap examination		all	all	G,H	
Can	Seal	Hermeticity		D2,3		D,E
	Stabilization bake				A,B,C	
	Thermal cycle, centrifuge, and mechanical shock	Mechanical integrity	B1; C1,2,3	A9; B2,3,8; C5,7	F	C,D
	Leak test (fine and gross)	Hermeticity		D3		C,D,E
	Electrical test (interim)	Controlled parameters	all	all	A-F	B,D
	Power Burn-In	Elimination of weak or marginal devices			A-F	
	Post-Burn-In electrical at ambient and temperature extremes	Controlled parameters and deltas	all	all	A,B,C, D,E,F, K	B,D
	X-ray inspection	Package interior	B6	A9; B8; C5,7; D1,3		F
	Functional/visual-sample			D4		A,B,C, D,E,G, I
	Pack and ship					

Figure 17-6. Linear Integrated Circuit - Typical Assembly Flow with Related Problem Codes

FAILURE ANALYSIS TECHNIQUES FOR DTL, TTL, AND LINEAR INTEGRATED CIRCUITS

Failure analysis may take various forms dependent on the extent of the failures, but invariably consists of a set procedure as noted on the following flow diagram. The success or failure of an analysis is strongly dependent on the method of approach and the sequencing of nondestruct methods before that of a destructive nature. The degree of investigation is determined by the complexity of the failure and the analysis is terminated when the failure mechanism is located, or sufficient information is derived so as to generate corrective action or preventive steps to preclude such failures in the future.

Failure analysis may be performed with minimal equipment or it may entail the use of expensive and highly sophisticated pieces of equipment. It is not the intent of this section to list all the possibilities in failure analysis. The reader will be acquainted with the procedures normally taken in arriving at a successful conclusion of failure identification and the necessary corrective action required to eliminate (from either the processing or usage of the devices) those procedures, processes, or materials, or lack of them, to prevent recurrence of such failures.

Failure analysis of linear circuits should be approached with the same care and methodology as for any other integrated circuits. Due to the complexity of the circuitry only minimal PN junction characteristics may be derived through point-to-point curve tracing; therefore, one must resort to dynamic tests. Failure modes of linear devices are different from digital devices so failure analysis proves to be more of a challenge. Infrequently a conclusive failure verification may be made prior to delidding of the defective device. Failures of linear devices frequently are of the degradational type such as loss of gain, oscillation, and latch-up of outputs. With the improvements in design of linear devices incorporating latch-up proof safeguards, the latter failure mode has been lessened. Other failure modes are more easily determined, e.g., overstressed inputs, or in the case of some operational amplifiers, the application of input signal voltage prior to power turn on often results in the overstress of the base to collector junction.

To aid in further identifying the potential failure mechanisms which may cause the predominant failure modes noted in the ALERT summaries, the reader should refer to the Problem/Screening Summary section.

As the manufacturing technology is very similar for DTL, TTL, and linear devices the accompanying analysis flow is applicable to these types of devices.

TEST/EXAMINATION	PROCEDURE	WHEN FAILURE IS / LOOK FOR	RELATED PROBLEM CODES (see foldout in the Appendix)			
			OPEN I	SHORT II	PAR DEV III	MECH ANOM IV
Box Level Mode Verification	Box level failure symptons and/or trouble shooting information should be documented – serves as invaluable aid to component failure analysis					
Failure Mode Verification Data Evaluation	Most failures indicate failure mode readily, e.g., opens, shorts, etc.					
Photograph Device as Received. Examine Device for Anomalies/ Damage	Upon receipt of the device at the analysis laboratory, the device should be photographed noting all identification and marks and all damage. Of particular note, the pin orientation mark should be readily evident			D2,4		all except F
Radiographic Inspection	The device should be X-rayed in the normal plane, plus one side plane, at various intensities and exposure times to expose potential anomalies, as well as lid seal integrity			B1,3,6	A9,12,13; B2,3,4,8; C5,7; D1,3	
Duplicate Failure Mode at Component Level to Pinpoint Location	Pinpointing of failure by curve-trace diode characteristic checks, or bench dynamic tests and parametric measurements, should be made at this point		all	all	all	all
Hermeticity Tests	If warranted, perform to MIL-STD-883, Method 1014, Cond. A and C					E
Delidding of Package	Due to proliferation of packaging styles, various procedures will have to be employed. The procedure will expose the internal cavity and chip with no induced damage. For the various packages use: Metal package: a special cutting tool is available Metal to glass seals: use a hot plate Ceramic flatpacks or ceramic dual-in-lines: encapsulate in epoxy then grind open CAUTION: During grinding, care should be taken that grinding debris does not fill cavity. Plastic packages: Various solvents/chemicals are to be used. Vendor recommendations should be followed					
Chip Microscopic Examination	Use various magnifications of optical microscopes, metallographs, Scanning Electron Microscope. In the case of difficult analysis, further analysis testing is necessary following required photography		all	A,B,C	G,I	
Microprobe Testing and Isolation at Chip Level	Electrical microprobe testing and physical isolation of component may be required. Utilize curve-trace PN junction characteristic and input/output characteristics checks. Voltage phase contrast tests using the Scanning Electron Microscope may be needed		A1-9; B5,7,9; C4,5,6,7	A3,4,5,6, 7,8,14; B3; C2,3,6,7	A-F,H	
Metallization Strip	In some cases of analysis, this step may be employed, e.g., pinhole shorts and thin oxide anomalies. The stripper used will be dependent on the metallization material of the chip		A4	A3,4,7		
Microsection of Chip	This procedure is used in conjunction with etchant chemicals to identify interfacing junctions and materials. This is a destructive test and should be kept to the very end. An electron emission microprobe may also be used at this stage to identify materials under test Photograph each microsectioned plane using color photography wherever warranted		A1,4,5, 6,8; B1,5,7; C1,2,3, 5,6,7	A3,4,6, 7,12,14; C4,7	L	

Figure 17-7. DTL, TTL, and Linear Integrated Circuits - Typical Failure Analysis Flow with Related Problem Codes

HANDLING OF MOS DEVICES

MOS (Metal-Oxide-Semiconductors) technology combines the integration of insulated gate field-effect transistor circuits on a high density monolithic chip. Various types of MOS devices are available, e.g., P-channel MOS, N-channel MOS, Complementary Symmetry MOS, etc. All these various types of MOS are fabricated around the basic insulated gate field effect transistor technology. Due to the construction of these devices, the susceptibility to high voltage static discharges is inherent from handling, hence this section treats the subject of MOS handling in the four detailed sections, i.e., Receiving, Storage and Moving, Assembly, and Final Test.

Purpose. The purpose of this section is to alert personnel handling MOS devices to the special handling procedures necessary to avoid damage to the devices. There are certain good practices which must be applied to all semiconductors, however, the high input impedance of MOS devices poses a special problem with regard to static charges. Therefore, it is suggested that the following procedures be followed when handling these devices.

1. Receiving Inspection Precautions.

   a. Place parts on a grounded metal plate as soon as they are unpacked from their containers.

   b. Use conductive containers when moving parts from one area to another and place the containers on a grounded metal plate at any station where operations are to be performed.

   c. The inspector must be grounded on a metal plate before handling a device.

   d. Smocks made of nylon or other synthetic materials shall not be worn when performing inspection of MOS devices. Cotton is an acceptable substitute.

   e. Inspection benches and seats must be of a conductive material and grounded in order to preclude the high static charge created by the sliding of the body on an insulated bench or seat.

   f. Handle devices only when necessary and then by first grasping the ceramic body or the metal can before touching any of the individual leads with tweezers or other tools. Ceramic packages with brazed leads require extra careful handling to avoid breaking off the leads since bending and twisting can fracture the braze.

   g. Repack MOS devices in their containers in the same configuration as they were originally shipped. The devices are shipped with leads shorted with wire, foil, or special conductive packaging, and/or placed in plastic containers specially treated with an antistatic spray to avoid damage in transit.

2. Storage and Moving Precautions.

   a. Electrically ground all metal cabinets and metal containers used for storing MOS devices.

   b. Maintain the short on the device leads and case.

   c. Acquaint all Material personnel with damage potential.

3. Assembly Precautions.

   a. Perform all assembly operations involving MOS devices on a grounded metal plate.

   b. Chair seats in the assembly area must be of a conductive material and must be grounded.

   c. Smocks made of nylon or other synthetic materials shall not be worn. Cotton is an acceptable substitute.

   d. Maintain the short placed on the devices' leads and/or keep devices in the specially treated plastic containers until time of assembly.

   e. The assembler must be grounded on a metal plate before handling a device. PC board bench clamps or vises must also be grounded.

f. MOS devices must be handled by either the ceramic body (flatpacks and dual-in-lines) or the metal cans (TO-5, TO-99, or other canned devices).

g. All electrical assembly equipment, e.g., soldering irons and tips, insulation strippers, heat guns, etc. must be grounded. All solder pots, reflow soldering equipment, and desoldering tools must also be grounded.

h. When testing is specified, all the test equipment contact pins must be grounded while the device is placed in the test socket. This action avoids the possibility of a charged test set discharging into the device as it is placed in the test socket.

i. Prevent the accumulation of solder flux between adjacent pins which may cause leakage paths. MOS device operation depends upon the high impedance between certain circuit elements and ground. Solder fluxes in the presence of a humid atmosphere can be very conductive.

4. Test Precautions.

a. Ground all test equipment.

b. Dielectric strength or insulation resistance tests are not recommended for equipment containing MOS devices.

c. Continuity tests must be performed only when authorized by the cognizant engineer. Certain MOS devices have built-in protective diodes which cannot sustain more than 10 mA current. A Simpson 260 VOM is capable of producing as high as 300 mA for short periods of time on the X1 ohmic scale.

d. Perform all operations on a grounded metal plate on the test bench. Periodic checks of assembly, rework, and test stations must be made to assure adequate grounding. Sources of static discharge and floating 60 cycle ac resulting from faulty ground connections must be eliminated.

5. Design Precautions. Do not connect an input (gate) directly to a printed wiring board contact or connector pin unless the gate has internal diode protection; or unless a bleeder resistor to ground is provided to protect the MOS gate from detrimental static charge accumulation.

ALERT SUMMARIES

Summaries of ALERT reports issued against Integrated Circuits are shown below. They are listed according to Problem Area - most frequent to least frequent occurrences. The "ALERT ITEM NO." (first column) references each summary back to the "Problem Area/cause and Action" table.

INTEGRATED CIRCUITS

ALERT ITEM NO./ GIDEP NO.	PROBLEM AREA/ Cause	PROBLEM DESCRIPTION	PROBLEM ANALYSIS
1 GSFC-68-04	OPEN Microcracks at window cutout	Low power DTL microelectronic circuits failed during box level tests and were analyzed.	Analysis confirmed "open" condition and subsequent Scanning Electron Microscope scans disclosed lack of contact between metallization to contact windows (emitter contact windows and/or resistor contact windows). Cause was attributed to the metallization deposition process over steep oxide steps at emitter and resistor contact windows, where metallization tends to separate.
2 MSFC-68-16	OPEN Microcracks at window cutout	Operational Amplifier failed in test.	Failure analysis, using the Scanning Electron Microscope, revealed an open metallization condition at the emitter of Q9 over the steep oxide step. Failure was at the small emitter contact window where the oxide step is somewhat steep. Deposition of aluminum at step periphery tends to be extremely thin and metallization opens occurred when the metal separated.
3 LeRC-71-02	OPEN Microcracks at window cutout	Hybrid failures occurred during subassembly and assembly test at room ambient and during life testing at 100°C.	Opens occurred at oxide step for contact windows. Evaluation of dice lots by Scanning Electron Microscope confirmed that microcracks existed to some extent in the majority of dice examined.
4 MSFC-71-13	OPEN Microcracks at window cutout	Integrated circuit failed to switch during computer system integration testing	Analysis of several devices by a Scanning Electron Microscope revealed severe metallization cracks at the contact window and poor metallization.
5 MSFC-71-19	OPEN Microcracks at window cutout	A Skylab experiment failure was traced to a microcircuit device.	Failure analysis revealed the problem to be open metallization at a window contact caused by a microcrack at the oxide step.

INTEGRATED CIRCUITS

ALERT[1] ITEM NO./ GIDEP NO.	PROBLEM AREA/ Cause	PROBLEM DESCRIPTION	PROBLEM ANALYSIS
6 MSC-69-06	OPEN Aluminum wire corrosion	Failure occurred in a high gain, wide band, DC amplifier in a hardglass flatpak with a Kovar lid using a low temperature glass seal.	Failure analysis revealed an aluminum lead wire corroded in two with a powdered or crystalline substance varying in color from white to brown noted on both bonds and near the separation. Two potential causes have been postulated: 1. Glass splatter: The manufacturer claims that during sealing operations, sealing glass from the lid may be deposited on the lead. The elements within the glass react with the aluminum causing corrosion. 2. Moisture corrosion: Possibility exists that moisture entered the package and promoted electrolytic corrosion. This type of corrosion is time dependent and with a rate strongly influenced in this case by package leakage rate, contaminants in the package, humidity of storage environment, physical and chemical condition of the aluminum wire, etc. Visual examination will not reveal extent of reaction progression towards failure.
7 GSFC-70-06	OPEN Cracked die	TTL Quad 2-Input positive NAND gate (with open collector output) failed in systems acceptance test.	Analysis revealed a cracked die causing the open circuit. It was concluded that the crack was the result of a temperature coefficient of expansion mismatch between the silicon die and the pyroceram bonding material used to bond the chip to the package.
8 GSFC-68-09	OPEN Lifted chip	Operational Amplifier and Clock Driver failures occurred during incoming inspection and environmental vibration testing of system.	Failure caused by silicon die coming loose and subsequent movement of die caused the bonding wires to break "open" because of inadequate adhesion of Pyroceram 89 used to bond the chip to the package. Mixture of pyroceram used was made by several different people in different locations, hence the proper mix may not have been attained.
9 B8-68-01	OPEN Lifted chip	TTL J-K flip-flop failed during powered flight vibration tests.	X-rays revealed bond wire severance from package leads due to chip separation and subsequent movement. Cause was lack of adhesion between pyroceram and chip.
10 J5-70-02	OPEN Lifted chip	High incidence of failures (6 to 20%) during manufacturer in-house life tests.	Failures attributed to floating die problem, i.e., silicon chip separating from bonding material. Cause was insufficient adhesion of chip to package.
11 C6-72-01	OPEN Lifted chip	Intermittent operation of a decoder during random vibration testing was traced to an integrated circuit.	Failure analysis revealed deficient die bonds which allowed the dice to become detached from the header.

INTEGRATED CIRCUITS

ALERT[1] ITEM NO./ GIDEP NO.	PROBLEM AREA/ Cause	PROBLEM DESCRIPTION	PROBLEM ANALYSIS
12 GSFC-69-04	OPEN Voids and overetched metallization	Dual 25-bit shift register failed in clock circuit board with no output from one of its registers. This defect is not visible at 140X magnification precap visual inspection.	Manufacturer attributed the problem to the presence of holes in the photoresist which permitted etchant to penetrate the masked area. This is a process problem. This condition cannot be detected with nondestructive testing.
13 WS-70-02, 02A	SHORT Pinholes at input metallization to silicon substrate	Three devices failed serially during bench check-out of PCM encoder.	Failure caused by pinholes in the silicon dioxide beneath the die interconnection penetrating through to the bulk silicon substrate.
14 D7-69-03	SHORT Output lead shorted to supply voltage terminal.	Following installation on PC boards, 17 of 50 Triple 3 - Input NAND gate devices were found defective. The output of each device was found shorted to the supply voltage terminal.	Manufacturing anomaly. Supply voltage bonding pad was in too close proximity to the adjacent metallization.
15 E9-68-03	SHORT Incorrect orientation of die	Lead orientation dot on package exterior was 180° misoriented, causing application of IC in a misoriented configuration.	Devices will be catastrophically destroyed through short circuits, and/or disable operation of device. Cause was workmanship error.
16 B1-70-01	SHORT Extraneous conductive material	Two out of three operational amplifiers failed during acceptance test at contractor's plant.	Analysis revealed that both failures were caused by faulty integrated circuits due to extraneous bonding wires within the TO-99 cases. The wire was identified as gold bonding wire.
17 GSFC-69-09	SHORT Extraneous conductive material	Fourteen lead flatpack hybrids failed during post-vibration electrical tests of the prototype NIMBUS-D clock.	Analysis indicated a short circuit within the device being caused by extraneous loose conductive particles (one was 14 mils long).

INTEGRATED CIRCUITS

ALERT[1] ITEM NO./ GIDEP NO.	PROBLEM AREA/ Cause	PROBLEM DESCRIPTION	PROBLEM ANALYSIS
18 SC-71-01	SHORT Extraneous conductive material	During random vibration testing of two separate computers, (5 g-rms random, hard mount), over 4% of TTL digital IC made during 1968 and 1969 failed catastrophically due to the inclusion of loose gold particles. The gold particles were from the preform used in die attach and appear to be a general problem, unrelated to the device type.	Ceramic DIP devices manufactured during 1968 through August 1969 used a ceramic base with a small gold mounting dot. During the alloy mount process, when the chip was scrubbed into the gold, small balls of gold were sometimes formed. During sealing operation any gold balls which were not removed by an air blast at precap inspection were subsequently melted and could partially attach on the bare ceramic. These particles would then break loose during vibration and short the IC circuitry.
19 MSC-71-04, MSC-71-21	SHORT Extraneous conductive material	Integrated circuits failed in a tape recorder data conditioner	Failure analysis disclosed internal metallic contamination.
20 MSFC-71-02	SHORT Extraneous conductive material	Integrated circuits failed during initial acceptance vibration testing.	Failure analysis revealed loose gold-tin balls caused a short across the metallization inside the package. Scanning Electron Microscope and microprobe analysis indicated the source of the balls was the gold eutectic used in sealing the lid to the package.
21 F3-A-72-05	SHORT Extraneous conductive material	Assembly failed in production acceptance test.	Examination established hard welded gold flake short in output transistor of operational amplifier. Gold flake particulate contamination found in three other lots.
22 WS-70-01, 01A, 01B	SHORT Extraneous conductive material	Failure occurred during vibration tests (0.7-13g, 10-2000 Hz) of TTL digital logic integrated circuits - gates and flip-flops.	Short circuits were caused by particle contamination from lid sealant material breaking loose. Short circuits were also of the intermittent varieties. The metal lid (Kovar) solder sealant material broke loose and became mobile during vibration causing intermittent shorts and in one known case, the conductive sliver became permanently lodged causing a permanent short.

INTEGRATED CIRCUITS

ALERT[1] ITEM NO./ GIDEP NO.	PROBLEM AREA/ Cause	PROBLEM DESCRIPTION	PROBLEM ANALYSIS
23 MSFC-68-08, 08A	SHORT Shorted external leads	This potential failure mode is the result of a study to determine the mechanisms of precipitate formation so that preventive action could be taken.	Packages employing soft lead glass seals when in the presence of cleaning detergents, phosphates and moisture can precipitate lead (Pb). This may also be initiated by electrolysis reduction of PbO to metallic Pb when exposed to a moderate temperature, and chemical reducing agents. Electrolytic precipitation can also occur by impressing 5-10 Vdc between any two terminals in the presence of moisture.
24 EE-69-01	SHORT Electrostatic discharge	Case 1. During cold temperature components parts tests, release of compressed carbon-dioxide (CO_2) coolants initiates a large electrostatic charge build-up which then discharges through MOS gate to source/drain terminals. Case 2. During box level low temperature tests where coolants (CO_2) are again released, the electrostatic charge build-up causes inadvertent pulsing of logic circuits with no permanent damage.	CO_2 coolant upon release in temperature chambers builds up massive electrostatic charges on ungrounded equipment and later discharges through the equipment/parts under test. MOS devices are particularly susceptible to such electrostatic discharges.
25 M1-68-01	SHORT Diffusion anomalies	Failure of an operational amplifier was caused by breakdown of isolation junction between input transistors and substrate, with interruption of positive power supply and a low impedance path from input to ground resulting.	Diffusion anomalies (oxide deposition and isolation diffusion) are primarily responsible.

ALERT[1] ITEM NO./ GIDEP NO.	PROBLEM AREA/ Cause	PROBLEM DESCRIPTION	PROBLEM ANALYSIS
26 F7-70-01	OPERATIONAL DEGRADATION Design deficiency	Four-bit binary counter device does not count properly when operated in a counter configuration.	Cause of the problem not identified but the manufacturer acknowledged the problem and solved same by a mask redesign. Analysis revealed problem to be in the following areas: 1. Parts are not usable below 4.75 volts DC supply voltage. 2. Clock fall time must be greater than 200 nanoseconds or the clock pulse width in off position must not exceed 1.5 microseconds.
27 J5-70-03	OPERATIONAL DEGRADATION Design deficiency	Four-bit binary counter device will not count properly in a counter configuration.	Cause of the problem has not been identified but the manufacturer acknowledged the problem and solved same by a mask redesign. Analysis also revealed the device would operate erroneously at higher frequencies when the supply voltage varied 100 mV.
28 GSFC-69-05	OPERATIONAL DEGRADATION Flip-flop reset rates slowed in critical applications	The metallization fix affected the "reset" rates of clocked flip-flops, making them slower. The reset rates now approximate 1 to 3 microseconds. Pre-fix devices had reset rates typically around 1 microsecond.	Metallization fix to counteract past aluminum deposition problems causing emitter contact window to show open, now affects the reset rates of the flip-flop. The manufacturer does not routinely monitor reset rates during manufacture, hence the process fix is not monitored for the effects to the reset rates.
29 GSFC-69-06	OPERATIONAL DEGRADATION Excessively high leakage failure rates	Failures discovered during incoming inspection when excessive high leakage rates of low power DTL gates and flip-flops were found during electrical testing.	Failure attributable to overflow of the glass frit onto the top surface of the chip. Cause was manufacturing anomaly; overfritting of glass bonding material over the sides and top of the monolithic chip.
30 G2-69-01, LeRC-69-03	OPERATIONAL DEGRADATION Inversion of N type silicon caused by use of phosphorous glass passivation.	Failures of operational amplifiers found during system level testing and during reliability testing.	Failure mode is a reduction in gain to less than specification level. Failures have been extremely heat sensitive. The gain decreases abnormally to out-of-specification levels as the ambient temperature increases. Cause of failure was attributed to inversion of N type silicon due to use of phosphorous glass.

INTEGRATED CIRCUITS

ALERT[1] ITEM NO./ GIDEP NO.	PROBLEM AREA/ Cause	PROBLEM DESCRIPTION	PROBLEM ANALYSIS
31 E9-68-05	OPERATIONAL DEGRADATION Failure to trigger	DTL monostable multivibrator fall-time of pulse degraded to extent it will not trigger.	Manufacturer mask change with no subsequent data sheet notification of its effect on output pulse fall time which degraded and became wholly dependent on external capacitor, C_x. Device will not operate with larger values of C_x - manufacturer's data sheet did not specify a limit on C_x.
32 EM-68-01	OPERATIONAL DEGRADATION Reaction of PNP lateral output transistor with the plastic case.	Dual Operational Amplifier in plastic case failed during temperature tests at 140°F.	Output decreases to zero because of reaction of lateral PNP output transistor with the plastic material of the case. Manufacturer acknowledges this anomaly and has discontinued manufacturing this type of case. Silicon lateral PNP transistor at output reacts with the plastic encapsulant of the case.
33 E9-68-02	OPERATIONAL DEGRADATION 1. Damage to input circuitry 2. Differential input voltage exceeded 3. Supply voltage polarity reversal	All three cases above caused failure of an operational amplifier.	1. Latch-up condition of the device has been found to be caused by degradation of the input caused by exceeding the positive common mode limit. This causes excessive currents at the input causing damage. 2. Ungrounded soldering irons during assembly, improper grounding of test equipment, and welding processes in installing devices into modules, all contribute to the failure through degradation of the input currents. This is caused by the differential inputs exceeding ±5 volts. 3. Supply voltage polarity reversal forward biases the isolation diode and shorts the power supplies resulting in a large surge current which will melt the aluminum traces. Some power supplies also have turn-on transients which the device would see as an effective voltage reversal.
34 LeRC-71-01	OPERATIONAL DEGRADATION Loss of gain	Launch vehicle became unstable, resulting in vehicle tumbling and loss of mission	Analysis identified most probable cause of failure as an integrated circuit. The flight failure was simulated by inducing damage to the input transistors of the integrated circuit causing latch-up of the output.
35 F9-71-02	OPERATIONAL DEGRADATION 1. Offset voltage drift 2. Loss of gain 3. Latching	Operational amplifier failures were detected during equipment level burn-in	The mode of failure was attributed to offset voltage drift, loss of gain, and "latching" to either the positive or negative power supply voltage. Failure analysis revealed inversion layer formation, metallization opens, and corrosion of aluminum bonding wire and pad bonds.

INTEGRATED CIRCUITS

ALERT[1] ITEM NO./ GIDEP NO.	PROBLEM AREA/ Cause	PROBLEM DESCRIPTION	PROBLEM ANALYSIS
36 GSFC 10-29-65	OPERATIONAL DEGRADATION Numerous systems test failures	A high incidence of failures of flatpacks was observed in the AIMP lunar aspect system. Twenty-two units out of approximately five hundred used, failed during system tests.	Analysis revealed failures were caused by manufacturing anomalies: (1) cracked wafers, (2) foreign material - photoresist residues, (3) metallization (aluminum) interconnect scratches, and (4) pyroceram voids in die to header bonds.
37 F9-70-01, F9-70-02	OPERATIONAL DEGRADATION Design error and surface inversion	J-K master Slave Flip-Flops failed at elevated temperatures. Failure mode was identified as output "inhibit" mode functional failure. The devices recover upon return to room ambient temperature.	The analyzed failures exhibited excessive leakage current (V_{cc}-substrate and Clear-substrate) at 25°. These leakage currents were verified on the chip by internal probing on the die surface and experimentally observed to be unstable and time dependent under bias at elevated temperature (125°F). The failures were shown to be recoverable after zero bias bakeout at 150°C, and then driven into failure again by elevated temperature testing with bias applied. The V_{cc}-sub and Clear-Sub leakage currents decreased under zero bias bakeout and increased again at elevated temperature with bias applied. This behavior is typical of surface inversion. This establishes the correlation between the 25°C leakage currents and inhibit function failure at elevated temperature.
38 J5-71-06-06A	OPERATIONAL DEGRADATION Design deficiency	Integrated circuit failed at high temperature operation	A defect in the temperature sensitive mask resulted in the master reset being unable to control the device outputs at high temperature. The manufacturer determined that the mask was missing a N+ diffusion bridge.
39 K9-71-01,01A	OPERATIONAL DEGRADATION Electrostatic discharge	Hybrid circuits exhibited voltage drift problems	Investigation revealed that the value of the thick film resistors used in the circuits changed because of electrostatic charge/discharge during packaging.
40 X9-72-01	OPERATIONAL DEGRADATION Offset voltage drift	Operational amplifiers failed when placed in operating equipments	Laboratory testing indicated that failures could be induced by maintaining the devices in an input-offset voltage test configuration. Failure analysis revealed the failures were caused by contamination on the chip surface or in the thermal oxide. The contamination caused inversion of the laterally diffused PNP transistor.

INTEGRATED CIRCUITS

ALERT[1] ITEM NO./ GIDEP NO.	PROBLEM AREA/ Cause	PROBLEM DESCRIPTION	PROBLEM ANALYSIS
41 G4-69-04	EXTERNAL ANOMALY Illegible identification	IC in glass flatpacks had package identification obliterated because of solvents.	Nonresistance to solvents per MIL-STD-202, Method 215, was caused by contamination on package prior to identification.
42 G4-69-05, 05A	EXTERNAL ANOMALY X-ray rejection	Formation of gold-aluminum intermetallic at an aluminum lead bond on gold bond pad of a substrate in the presence of gold-silicon eutectic from chip bond scrub.	This is a hybrid configuration where one aluminum lead from the input logic IC (monolithic chip) is bonded to the gold trace on the substrate. This gold trace is also the extension of the IC chip bond pad area which had its eutectic scrub material spread to the location of the aluminum lead bond. In the presence of +450°C lid sealing temperatures, the intermetallic at the aluminum bond formed.
43 GSFC-71-05	EXTERNAL ANOMALY Misidentification	Integrated circuits failed to meet performance requirements prescribed for the indicated parts	Investigation revealed the parts had been mismarked. They performed properly when tested to the appropriate specifications.
44 F9-71-03, F9-71-04	EXTERNAL ANOMALY Misidentification	Functional failure during engineering breadboard testing was traced to an integrated circuit	Investigation revealed that the part had been mismarked. It performed properly when tested to the appropriate specifications.
45 F3-72-08, MSFC-A-72-12	EXTERNAL ANOMALY Damage to package	Cracking observed on ceramic dual-in-line packages (DIP) integrated circuits mounted on printed circuit boards conformally coated with PR-1538.	Conformal coating between the DIP base and the printed circuit board caused cracks at the lead frame area of the DIP during thermal cycling. Flexing of coated and uncoated boards during normal manufacturing processing has also caused cracks.

NOTE:
1. Where no ALERT number (GIDEP) exists, the originator and date are shown.

SECTION 18
TRANSISTORS
(GIDEP CODE 742)

CONTENTS

INTRODUCTION

OBJECTIVE

The objective of this section is to identify the major problem areas associated with the use of transistors and to suggest approaches (developed from experience) for dealing with those problems.

SECTION ORGANIZATION

The transistor section is presented with the following organization:

General

1. Basic failure problems associated with transistors are identified based upon ALERT and industry experience.

2. Where applicable, a screening technique is suggested for detecting finished parts having a potential for failure.

Subtopics - Treatment of Specific Types

1. Transistor type background

2. For those in the process of selecting parts and manufacturers, or attempting to eliminate part problems at the manufacturer levels, a portion is devoted to describing the inner construction of selected types and describing the manufacturing sequence necessary to produce the part. Particular emphasis is given to the design or manufacturing deficiencies associated with the identified failure mechanisms.

3. Basic approaches are provided to assist in developing a competent failure analysis plan where corrective action at the part level is desired. The material is arranged so that one experiencing a specific problem can identify those steps in the failure analysis process likely to reveal that problem.

Transistor Types. Transistors have been divided into subtopics according to their type of construction. Bipolar, metal-oxide-semiconductor field-effect, and junction field-effect transistors have been discussed at length. Other types of transistors include only summaries of ALERT reports.

Transistor Fundamentals

What a Transistor Can Do. The transistor is a semiconductor device performing the function of an amplifier and/or switch, a switch being in reality a special case of an amplifier. An input current varies a resistance in the output circuit so as to control current, voltage, or power as required. If the input current takes on only two limiting values, at one of which the output resistance is so large that its terminal voltage is determined only by the external circuit, and at the other of which the output resistance is so small that the current through it is determined only by the external circuit, then the transistor is acting as a switch. If the current through the output resistance (or the voltage across it) is determined by the combined effects of the input current and the external circuit then the device is an amplifier. Input current changes are associated with changes of voltage and power as are output current changes. Normally the ratio of at least one of the output parameters to the corresponding input parameters exceeds unity. In its simplest form the transistor consists of three layers of semiconductor material with purposely introduced impurities such that the outer layers have an excess (or deficiency) of free electrons and the inner layer has a deficiency (or excess) of free electrons. The transistor is an NPN (or PNP) type and consists in effect of two back-to-back diodes. If electrons are injected into (withdrawn from) the inner layer, or base, of a NPN (PNP) transistor its normally nonconducting state between the outer layers becomes conductive in accordance with the amount of injected current. The operating characteristics being determined by: doping, diffusion temperature, diffusion time, die size, packaging, etc.

Practical Considerations. As in all designs, the design of a transistor to perform a given function requires a series of compromises. An improvement in one design consideration results in the deterioration of another design consideration. In addition to design compromises, one is faced with the parasitic characteristics of transistors: capacitance, leakage currents, voltage drops, temperature, etc. It is only by minimizing and controlling these effects that reliable transistors

have been developed and manufactured. Transistor design characteristics and the resultant parasitic characteristics are established by the type of transistor being built, its intended application, and its resultant package.

Failure Modes

Failure Categories. Part level failure problems associated with transistors may be lumped under four basic categories: catastrophic opens, catastrophic shorts, electrical parameter deviation, and mechanical anomalies. It must be recognized that catastrophic opens and shorts are worst-case conditions of certain electrical parameter deviations.

False Failed Equipment Indicators. At the equipment level, high forward voltage drop can appear to be an open, and high reverse leakage current may appear to be a short. A failure mechanism producing an apparent open or short (e.g., a parameter deviation), in its extreme condition becomes an open or a short. Only failure analysis on the piece part level can distinguish between these conditions and result in corrective action.

Eliminating Defectives

Problem Solving Approach. The approach taken in this section will be to identify the user encountered problem areas associated with a particular type of transistor, then provide suggestions for eliminating those transistors prone to exhibiting those problems at the finished transistor level, the design level, and at the manufacturing level.

Finished Transistor Level. Realizing that most consumers are required to use finished transistors that are on hand, information is provided on the screening of the devices, that is, sorting the bad transistors from the good ones. Suggestions are made as to environmental and electrical testing which will identify defective units while having no deleterious effects on good units. This technique is used not only for sorting, but for providing assurance that the manufacturer has controlled his processes.

Design Level. While screening has proven capable of providing good transistors, it does not provide a solution to the problem of design compromises and/or design deficiencies. Certain design compromises cannot be avoided; however, reliable equipment can be built if allowance is made in the equipment design to minimize the effect of these compromises. Design deficiencies, wherever encountered, must be identified and eliminated.

Manufacturing Level. The most carefully conceived design and the best of parts can amount to nought if manufactured in an environment lacking necessary controls over materials, processes, and workmanship. As no screening is 100 percent effective in removing defective parts, it is more desirable to correct manufacturing anomalies through the use of adequate controls and inspection points.

Failure Analysis

Objective. The primary objective of failure analysis is to identify failure mechanisms at a level such that corrective action can occur. Knowing that a transistor is open is of no consequence if corrective action is not possible. Knowing that a transistor is open because of a defective bond allows for correction of future bonding operations and the elimination of that problem cause.

Failed Part Rarity. A part in a failed condition must be considered a "once-in-a-million" occurrence, a phenomenon which may never again occur. It is only by using this premise that successful failure analysis can be performed.

Failure Verification. After recording all identifying external markings, visually inspecting, photographing identification and damage, and radiographically inspecting, the first requirement is to verify the failure. Too often the wrong part is removed from the circuit or an equipment test error, rather than a part failure, causes a good part to be delivered for failure analysis. Many times the actual part failure is different from that specified, hence, a note of this fact must be made.

Analysis Direction. The process of analyzing a failure (performing those steps necessary to identify a specific correctable failure mechanism) requires the coordination of one having a knowledge of failure mechanisms, transistor design, transistor manufacturing techniques, and the ability to form a practical plan of action.

When To Analyze. In many cases transistor failures occur for which device corrective action is not required, however, in almost all cases some form of corrective action is necessary. Corrective action can be required of circuit designers,

assembly manufacturers, test organizations, etc., as well as on parts. As such, it is suggested that a very strong cause must exist before failure analysis is abbreviated or forsaken.

Reliability/Life. It is anticipated that as a result of screening, analysis of design and manufacturing, and effective failure analysis (all performed at the part level) that significant improvement in reliability and life will be realized.

PROBLEM/SCREENING SUMMARY

Scope. The problem summaries present the cause and effect of failures and suggest action to be taken to identify and screen out devices with latent or incipient defects. This summary is an accumulation of information and experience obtained in working with transistor failures and in avoiding those failures.

This summary is intended to identify transistor problem areas and problem causes. Having identified the problems, suggestions are made for the elimination of problem parts through the use of suggested screening tests derived through experience. Problem areas have been grouped under the basic categories of open, short, parameter deviation, and mechanical anomaly.

ALERT Item No.. Where directly applicable, the "ALERT Item No." of the ALERT report describing a specific cause for a failure is listed against that cause. Thereby, a cross reference is provided between a specific failure cause found in the "ALERT Summaries" and the broader failure experience/avoidance knowledge shown in this presentation.

Misapplication. Experience has shown that the major cause of transistor failure has been misapplication. Experience also indicates that the most frequent failure attributable to the part itself is open.

PROBLEM AREA/CAUSE AND SUGGESTED ACTION

TRANSISTORS

PROBLEM AREA/ Cause	ALERT ITEM NO.	SUGGESTED ACTION - SCREEN (See "Screening Inspections and Tests")
OPEN Lifted bonds Bad solder connection Broken bond Poor crimp connection	1 thru 11 12 13 14	High Temperature Storage, Thermal Shock, Acceleration, Burn-In, and Electrical Testing
OPEN Separation of metallization from chip	15,16	High Temperature Storage, Acceleration, Burn-In, and Electrical Testing
OPEN Corrosion of metallization	17,18	Thermal Shock, Acceleration, Hermetic Seal, Burn-In, and Electrical Testing
OPEN Loose internal heat sink	19,20	Thermal Shock, Acceleration, and Electrical Testing
OPEN Poor glass-to-metal seal	21	Acceleration, Hermetic Seal, Electrical Testing, and Visual Examination
OPEN Open in metallization path	22	High Temperature Storage, Burn-In, and Electrical Testing
SHORT Conductive contamination	23 thru 33	Acceleration, Electrical Testing, and Radiographic Inspection
SHORT Build-up of tolerances and drooping leads	34	Acceleration, Electrical Testing, and Radiographic Inspection
SHORT Tin whisker	35	Acceleration, Hermetic Seal, Electrical Testing, and Radiographic Inspection
ELECTRICAL PARAMETER DEVIATION Channeling	36 thru 40	High Temperature Reverse Bias, Burn-In, and Electrical Testing
ELECTRICAL PARAMETER DEVIATION Moisture in package (dew point problem)	41,42	Dew Point Test (special screen test), and Hermetic Seal
ELECTRICAL PARAMETER DEVIATION Partial bond Cracked chip	43 44	High Temperature Storage, Thermal Shock, Acceleration, Burn-In, and Electrical Testing
ELECTRICAL PARAMETER DEVIATION Defective hermetic seal	45	Hermetic Seal
ELECTRICAL PARAMETER DEVIATION Secondary breakdown	46	Electrical Testing
ELECTRICAL PARAMETER DEVIATION Cracked glass	47	100% Screening
ELECTRICAL PARAMETER DEVIATION Contamination	48,49	High Temperature Storage, High Temperature Reverse Bias, Burn-In, and Electrical Testing

TRANSISTORS

PROBLEM AREA/ Cause	ALERT ITEM NO.	SUGGESTED ACTION - SCREEN (See "Screening Inspections and Tests")
MECHANICAL ANOMALY		Visual Inspection
Contamination	50	
Notched leads	51	
Corrosion and embrittlement	52	
MECHANICAL ANOMALY		100% Screening
Cracked packages	53	

SCREENING INSPECTIONS AND TESTS

Screening inspections and tests for the various types of transistors are very similar, differences being in electrical parameter measurements. The differences for bipolar, MOS FET, and JFET are described when applicable.

Basic Screening. The screening inspections and tests suggested for transistors included in the "Problem/Screening Summary" are as follows:

1. Precap Visual Examination - Internal
2. High Temperature Storage
3. Temperature Cycling
4. High Temperature Reverse Bias
5. Acceleration
6. Seal Test
7. Burn-In (sometimes called "Operational Stabilization")
8. Electrical Testing
9. Radiographic Inspection (X-ray)
10. Visual Examination - External

Objective. The purpose of the screening is to allow detection of parts that: (1) have been improperly processed by the manufacturer, (2) contain flaws or weak spots (including voids and contamination), (3) have poor solder or weld connections, or (4) have any other anomalies that could result in a failure under normal operating conditions.

Additional Screening. In cases where specific characteristics are critical in the function of the using equipment those parameters should be added to the screening requirements.

Envelope Removal/Dissection. The basic approach taken here is to subject each of the devices to a test procedure in order to make a one-by-one acceptance determination. The disadvantage of this approach is the underlying assumption that the internal construction materials, processes, etc., from part-to-part are homogeneous so that the devices can be treated as a uniform lot. If the devices are not produced under similar design criteria and manufacturing controls which permit a heterogeneous lot to exist, a single screening procedure may not be the optimum for all units. For this reason if the first test is not performed, it is desirable to examine the internal design and construction. This is accomplished, first, by a nondestructive radiographic inspection; and second, by performing a destructive envelope removal or dissection on a limited sample of devices. This procedure is more meaningful if a design/construction baseline has been established as a comparison criterion.

1. PRECAP VISUAL EXAMINATION - INTERNAL - MIL-STD-750, METHOD 2072 (ref 4)

   Internal visual examination of transistors is normally performed on a 100 percent basis as the first screening test. It is performed to detect chip and package defects such as metallization anomalies, oxide and diffusion faults, scribing defects, bonding defects, lead wire anomalies, die mounting defects, and foreign materials.

2. HIGH TEMPERATURE STORAGE - MIL-STD-750, METHOD 1031 (ref 4)

   Transistors are normally subjected to their maximum rated storage temperature for a minimum of 24 hours. Storage time would not normally exceed 168 hours as a screening requirement.

   Test objective would normally be the stabilization of transistor electrical characteristics. The test has been used to reveal problems with contamination, die bond, lead bonds, metallization, oxide, and bulk wafer properties.

   Transistor instability during high temperature storage testing would be revealed by high delta shifts in the following electrical characteristics:

Bipolar: I_{CBO}, I_{EBO}, and/or low current h_{FE}

MOS FET (enhancement mode): I_{DSS}, I_{SDS}, and/or $I_{G(f)}$

MOS FET (depletion mode): I_{GSS}, I_{GDS}, and/or I_{DGO}

MOS FET (depletion-enhancement mode): I_{GSS}, I_{GDS}, and/or I_{DGO}

JFET: I_{GSS}, I_{GDS}, and/or I_{DGO}

3. TEMPERATURE CYCLING (THERMAL SHOCK) - MIL-STD-750, METHOD 1051 (ref 4)

In this test transistors are cycled from their highest rated storage temperature to their lowest rated storage temperature. Transistors are generally stabilized for a minimum of 15 minutes at each temperature extreme, and transfer time, from one extreme to another, is minimized. Devices are cycled for a minimum of 10 cycles and would not normally be cycled more than 20 cycles.

Test objective would be to check the mechanical integrity of the package in that it would reveal problems with internal and external bonding techniques. Loss of mechanical integrity internally would be revealed by high delta shifts in the following electrical characteristics:

Bipolar: $V_{BE}(sat)$, and/or $V_{CE}(sat)$

MOS FET (enhancement mode): rds (on), $I_D(on)$, $V_{DS}(on)$, and/or $|Y_{fs}|$

MOS FET (depletion mode): $I_D(on)$, I_{DSS}, $|Y_{fs}|$, and/or $|Y_{os}|$

MOS FET (depletion-enhancement mode): $I_D(on)$, I_{DSS}, $|Y_{fs}|$, and/or $|Y_{os}|$

JFET: I_{DSS}, $V_{DS}(on)$, $r_{ds}(on)$, $|Y_{fs}|$, and/or $|Y_{os}|$

Loss of mechanical integrity externally would result in hermeticity problems and subsequent failure to pass hermetic seal testing.

4. HIGH TEMPERATURE REVERSE BIAS (HTRB)

During HTRB testing bipolar, MOS, and junction field-effect transistors are subjected to an ambient temperature equal to 75 percent of their maximum rated storage temperature and the following voltage applied:

60-80 percent of the maximum rated collector to base voltage (reverse biased)

60-80 percent of the maximum rated gate to source voltage (reverse biased) (MOS and JFET)

Test time is usually 12 to 24 hours and does not normally exceed 168 hours as a screening requirement. Occasionally field-effect transistors may be HTRB tested at temperatures as high as 97.5 percent of their maximum rated storage temperature. Test time at these temperatures should be limited.

Note: Following HTRB testing, test voltages must remain applied until the ambient temperature has been reduced to 25°C (+5°, -0°).

Bipolar. Test objective for bipolar transistors would be to determine if the parts were subject to "inversion channeling" problems. Inversion channeling would be revealed by high delta shift in I_{CBO}, and/or I_{EBO} electrical characteristics (when compared to pre-HTRB electricals).

MOS FET. Test objective for MOS FET would be to determine if the parts were susceptible to "wandering threshold" problems. Such problems would be revealed by high delta shift in $V_{GS}(th)$ for enhancement mode MOS FET, and $V_{GS}(off)$ for depletion and depletion-enhancement MOS FET.

JFET. Test objective for JFET would be to determine if parts had surface contamination problems. Such problems would be revealed by high delta shifts in V_P, I_{GSS}, I_{GDS}, and/or I_{DGO} electrical characteristics (when compared to pre-HTRB values).

5. ACCELERATION - MIL-STD-750, METHOD 2006 (ref 4)

Acceleration is normally performed at 20,000 g force for one minute with the transistor leads toward the center of the centrifuge. Test conditions can vary considerably depending upon the case type of the device being tested.

Bipolar. This test is intended to check the mechanical integrity of bipolar transistors. Internal integrity is determined by electrically testing $V_{BE}(sat)$ and $V_{CE}(sat)$. High delta shifts would indicate problems with the internal lead-to-die bond, lead-to-post bond, and/or die-to-header bond. Loss of external integrity is revealed by hermeticity problems during hermetic seal testing.

MOS FET. This test is intended to check the internal and external integrity of MOS FET. High delta shifts in rds(on), $I_D(on)$, $V_{DS}(on)$, and/or $|Y_{fs}|$ for enhancement mode MOS FET; and $I_D(on)$, I_{DSS}, $|Y_{fs}|$, and/or $|Y_{os}|$ for depletion and depletion-enhancement mode MOS FET would indicate problems with the internal die bonds, post bonds, and/or die mounting. Loss of external integrity would be revealed by the hermetic seal test.

JFET. This test is intended to check the internal and external mechanical integrity of JFET. Internal mechanical integrity is verified by electrically checking $V_{DS}(on)$, $r_{ds}(on)$, I_{DSS}, $|Y_{fs}|$, and/or $|Y_{os}|$. High delta shifts would indicate problems with internal lead-to-die bond, lead-to-post bond, and/or die-to-header bond. Loss of external mechanical integrity, would be revealed by failure to pass hermetic seal testing.

6. HERMETIC SEAL - MIL-STD-750, METHOD 1071 (ref 4)

All cavity type transistors are subjected to hermetic seal testing in the form of fine and gross leak testing. Fine leak testing is normally performed by placing the transistor in a chamber, reducing the atmospheric pressure and backfilling with helium, in essence, attempting to pump out and replace the gas inside the transistor with helium. The part is then "sniffed" with a helium detector. This method can detect leak rates of less than 1×10^{-8} atm cc/sec.

Gross leak testing has been done by a number of methods, the latest of which is the use of liquid fluorocarbons at elevated temperature. If bubbles are seen to emanate from the transistor, the device is rejected.

The test objective of hermetic seal tests is to verify the external integrity of the transistor by assuring that it has no hermeticity problems.

7. BURN-IN (OPERATIONAL STABILIZATION - MIL-STD-750, METHOD 1026 (ref 4)

The test objective of Power Burn-In is essentially the same as that of High Temperature Storage, that is, the stabilization of electrical characteristics. Once again, in bad parts Burn-In reveals problems concerning contamination, die bond, lead bonds, metallization, oxide, and bulk wafer properties.

Bipolar. Power Burn-In of bipolar transistors is usually performed for 168 or 240 hours using common base biasing. Collector to emitter voltage, collector current, and external ambient temperature are adjusted to obtain the desired power dissipation and junction temperature equal to the absolute maximum rated junction temperature of the device being tested.

Transistor instability during Power Burn-In is revealed in high delta shifts in I_{CBO}, I_{EBO}, and/or low current h_{FE} electrical characteristics. In addition, Burn-In stresses the internal mechanical construction of transistors. Loss of internal mechanical integrity is revealed by high delta shifts in $V_{BE}(sat)$ and/or $V_{CE}(sat)$ electrical characteristics.

FET. Power Burn-In of field-effect transistors is usually performed for 168 or 240 hours using common source biasing. Drain to source voltage, drain current, and external ambient temperature are adjusted to obtain the desired power dissipation and a junction temperature equal to the absolute maximum rated junction temperature of the device being tested.

It should be noted that many companies perform what is in reality an HTRB test for Power Burn-In on FET. This test is much easier, but is considered inferior to the Burn-In test referenced above. HTRB testing, whether called HTRB or Burn-In, should be limited to approximately 168 or 240 hours maximum. The following is a listing of Power Burn-In methods for FET shown in order of preference:

a. Specific I_D (shown above)

b. I_{DSS} (current limited)

c. I_{DSS}

d. I_{GSS} (HTRB)

MOS FET. Instability in bad parts is revealed as high delta shifts in I_{DSS}, I_{SDS}, and/or $I_{G(f)}$ for enhancement mode MOS FET; and I_{GSS}, I_{GDS} and/or I_{DGO} for depletion mode and depletion-enhancement mode MOS FET. In addition, Burn-In stresses the internal mechanical construction of MOS FET. Loss of internal mechanical integrity is revealed through high delta shifts in $r_{ds}(on)$, $I_D(on)$, $V_{DS}(on)$ and/or $|Y_{fs}|$ for enhancement mode MOS FET; and $I_D(on)$, I_{DSS}, $|Y_{fs}|$ and/or $|Y_{os}|$ for depletion and depletion-enhancement mode MOS FET.

JFET. Instability in bad parts is revealed as high delta shifts in V_P, I_{GSS}, I_{GDS}, and/or I_{DGO}. In addition, Burn-In stresses the internal mechanical construction of JFET. Loss of internal mechanical integrity is revealed by high delta shifts in I_{DSS}, $V_{DS}(on)$, $r_{ds}(on)$, $|Y_{fs}|$, and/or $|Y_{os}|$.

8. ELECTRICAL TESTING

Bipolar. Electrical testing is essential in the determination of the quality of a bipolar transistor. As has been shown in other screening tests I_{CBO}, I_{EBO}, low current h_{FE}, $V_{CE}(sat)$, and $V_{BE}(sat)$ are those electrical tests required to verify the status of a transistor. In addition to these electrical tests, BV_{CEO} should be tested as this junction must meet certain minimum requirements for actual transistor application and is not specifically checked in the other electrical tests.

The objective of electrical testing, aside from verifying specification requirements, is in determining delta shift. Delta shift is the amount that a measured electrical parameter has changed between any two electrical tests, such as Pre- and Post-Burn-In electrical tests. The delta shift of bipolar transistor electrical parameters is usually limited as shown below:

ΔI_{CBO} and ΔI_{EBO} = ±100% of the previous test value or ±10% of the specification limit whichever is greater[3].

Δh_{FE} = ±15% to ±25% of the previous test value dependent of how large the specification limit is[3].

$\Delta V_{BE}(sat)$ and $\Delta V_{CE}(sat)$ = ±50 mVdc from previous test value or ±10% of the specification limit whichever is greater[3].

Delta criteria should always be specified before and after Power Burn-In and HTRB, but can be useful before and after any screening test as indicated in the individual screening tests. In addition, 100 percent Electrical Testing should be performed prior to and following completion of screening.

MOS FET. Electrical Testing is essential in the determination of the quality of a MOS FET. As has been shown in other screening tests I_{DSS}, I_{SDS}, $I_{G(f)}$, $I_D(on)$, rds(on) $V_{DS}(on)$, $|Y_{fs}|$, and $V_{GS}(th)$ are those electrical tests required at various times to verify the status of various enhancement mode MOS FET. I_{GSS}, I_{GDS}, I_{DGO}, $I_D(on)$, I_{DSS}, $|Y_{fs}|$, $|Y_{os}|$, and $V_{GS}(off)$ are those electrical tests required at various times to verify the status of certain depletion and depletion-enhancement mode MOS FET. In addition to the above electrical tests, BV_{DSS}, BV_{SDS}, BV_{GDO}, BV_{GSO}, and/or BV_{GBO} should be tested as these functions must meet certain minimum requirements for actual MOS FET operation, and have not been specifically checked in the other electrical tests. Naturally, most MOS FET, regardless of type, will not have all the above electrical tests specified.

The objective of electrical testing, aside from verifying specification requirements, is in determining the delta shift. Delta shift is the amount that a measured electrical parameter has changed between any two electrical tests, such as Pre- and Post-Burn-In electrical tests.

The delta shift of MOS FET electrical parameters is usually limited as shown below.

a. Enhancement Mode (Type C) MOS FET

ΔI_{DSS}, I_{SDS}, and $I_{G(f)}$ = ±100% of the previous test value or ±10% of the specification limit whichever is greater[3].

Δrds(on), $I_D(on)$, and $|Y_{fs}|$ = ±10% of the previous test value[3].

$\Delta V_{GS}(th)$ = ±10% of the previous test value[3].

b. Depletion (Type A) and Depletion - Enhancement (Type B) Mode MOS FET.

ΔI_{GSS}, I_{GDS}, and I_{DGO} = ±100% of the previous test value or ±10% of the specification limit whichever is greater[3].

ΔI_{DSS}, I_D(on), $|Y_{fs}|$ and $|Y_{os}|$ = ±10% of the previous test value[3].

ΔV_{GS}(off) = ±10% of the previous test value[3].

Delta criteria should always be specified before and after Power Burn-In and HTRB, but can be useful before and after any screening test as indicated in the individual screening tests. In addition, 100 percent Electrical Testing should be performed prior to and following completion of screening.

JFET. Electrical testing is essential in the determination of the quality of a JFET. As has been shown in other screening tests I_{GSS}, I_{GDS}, I_{DGO}, I_{DSS}, V_{DS}(on), r_{ds}(on), $|Y_{fs}|$, $|Y_{os}|$, and V_P are those electrical tests required at various times to verify the status of JFET. In addition to the above electrical tests, BV_{DSS}, BV_{SDS}, BV_{GDO}, BV_{GSO}, and/or BV_{GSS} should be tested as these functions must meet certain minimum requirements for actual JFET operation, and have not been specifically checked in the other electrical tests. Naturally, most JFET will not have all the above electrical tests specified.

The objective of electrical testing, aside from verifying specification requirements, is in determining the delta shift. Delta shift is the amount that a measured electrical parameter has changed between any two electrical tests, such as Pre- and Post-Burn-In electrical tests.

The delta shift of JFET electrical parameters is usually limited as shown below.

ΔI_{GSS}, I_{GDS}, I_{DGO} = ±100% of the previous test value or ±10% of the specification limit whichever is greater.

ΔI_{DSS}, V_{DS} (on), r_{ds} (on), $|Y_{fs}|$, $|Y_{os}|$, and V_P = ±10% of the previous test value[3].

Delta criteria should always be specified before and after Power Burn-In and HTRB but can be useful before and after any screening test as indicated in the individual screening tests. In addition, 100 percent electrical testing should be performed prior to and following completion of screening.

9. RADIOGRAPHIC INSPECTION (X-RAY)

Radiographic inspection of transistors is normally performed on a 100 percent basis following completion of the preceding screening tests. The objective of X-ray inspection is the detection of internal conductive particles, excessive internal lead lengths or any other internal anomaly which may affect the reliable operation of the transistor that is detectable by X-ray.

10. VISUAL EXAMINATION - EXTERNAL

External visual examination of transistors is normally performed on a 100 percent basis as a final screening test. External visual inspection is performed to detect package defects, marking defects and external lead defects.

NOTE:
3. Actual test value shall not exceed the specification limit.

BIPOLAR TRANSISTORS

CHARACTERISTICS

The distinguishing feature of a transistor, as a semiconductor device, is the ability to provide power or voltage amplification. This ability is most often expressed as a ratio of the collector current to the emitter current (alpha in common base circuits) or the collector current to the base current (beta in common emitter circuits). The value of alpha or beta is affected by the temperature and the operating frequency.

Temperature Effects. As the operating temperature of a transistor increases so does the "alpha" and the "beta" with alpha approaching unity current gain. The maximum normal temperature, wherein transistor action is expected, is 85°C for germanium and 150°C for silicon. Conversely, the forward current transfer ratio decreases as the operating temperature decreases. The minimum temperature at which a useful beta can be expected is -65°C.

Frequency Effects. As the operating frequency of a transistor increases the forward current transfer ratios (alpha and beta) decrease. The "cutoff frequency" being that frequency at which the value of alpha (for common base) or beta (for a common emitter circuit) drops to 0.707 times the value at one kilohertz. The frequency effects on beta can also be expressed using the "gain bandwidth product", the frequency at which the common emitter current gain is one.

Additional Characteristics. Other electrical characteristics such as "collector reverse leakage" I_{CBO} and "base-emitter voltage" V_{BE} vary with temperature, I_{CBO} doubling for every 8 to 10°C of temperature increase.

Still other electrical characteristics such as collector capacitance (C_{ob}, C_{oc}) contribute to poor transistor high frequency response.

Package Characteristics. The performance of transistors in equipment depends on several factors besides the basic electrical characteristics. The two most important factors being the design and fabrication of the transistor as well as the type of circuit used. This section will deal with the former two realizing that the latter, circuit design, may be a major cause of transistor problems but that it is not normally included in ALERT reports.

Transistors have been made using several techniques in an attempt to construct two parallel P-N junctions with controlled spacing and impurity levels. The various basic techniques are presented below in an approximate order of appearance with respect to time.

1. Point Contact
2. Grown Junction
3. Alloy Junction
4. Diffused Junction
5. Planar
6. Epitaxial

The next subsection (describing problems and failure mechanisms found in transistors caused by design deficiency, lack of process control, and inadequate quality control) contains a drawing, a materials list, and a manufacturing flow diagram for the latest type of transistor technique — planar epitaxial.

BIPOLAR TRANSISTORS

DESIGN AND PRODUCTION CONSIDERATIONS

Failures Related to Process. A typical bipolar transistor (Figure 18-1) and a typical assembly flow (Figure 18-2) are presented together with the suggested controls required to assure a reliable product. The "Critical Process" is defined for each of the manufacturing steps. Relationship is established between failure causes and the manufacturing process. Having experienced a specific problem, one could identify those manufacturing steps with potential for contributing to the failure.

Assembly Flow. A typical manufacturing flow for transistors is presented together with the process name and the constituent added. Included in the typical manufacturing flow is a listing of the significant variable for each process; a significant variable is one which if not closely controlled will result in an inferior if not useless product. Circled numbers in the constituent added column are directly related to the circled numbers in the typical drawings.

Assembly Precautions. Contamination, conductive and nonconductive, is the greatest cause of transistor failure and is directly related to the assembly process. As such, one should assure that specific in-process inspection and testing be designed so as to eliminate and/or detect contamination.

The following is a partial list of the most probable sources of contamination:

1. Conductive Contamination
   a. Wire Bonding Process (bits of loose wire)
   b. Chip Bonding Process (loosely attached expulsion or die bonding material drawn across die by tweezers)
   c. Can-to-Header Welding Process (weld splash)
2. Nonconductive Contamination
   a. Sealing Process (moisture sealed in)
   d. Cleaning Processes (corrosive chemical residue)
   c. Chip Passivating Process (contaminants in passivation material)

TYPICAL BIPOLAR TRANSISTOR (Planar Epitaxial) DESIGN (Figure 18-1)

ITEM	ITEM NAME	MATERIAL OF CONSTRUCTION
1	Can	Gold plated Kovar, TO-18
2	Base Interconnect Wire	Gold
3	Collector Lead to Header Weld	
4	Header	Gold plated Kovar
5	Glass Seal	#5072 or equivalent glass
6	Collector Lead	Kovar
7	Emitter Lead	Kovar
8	Header Orientation Tab	

ITEM	ITEM NAME	MATERIAL OF CONSTRUCTION
9	Emitter Interconnect Wire	Gold
10, 13	Chip to Header Scrub Bond	
11	Base Post	Kovar
12	Header	Kovar, TO-18
13, 10	Gold Bond Between Header and Chip	
14	Collector	Phosphorous doped silicon
15	Base Diffusion	Boron doped silicon
16	Emitter Diffusion	Phosphorous doped silicon
17	Passivation	Silicon dioxide
18	Emitter Metallization	Vacuum deposited aluminum
19	Base Metallization	Vacuum deposited aluminum
20	Epitaxial Layer	Heavily phosphorous doped silicon
21	Annular Ring Diffusion	Phosphorous doped silicon

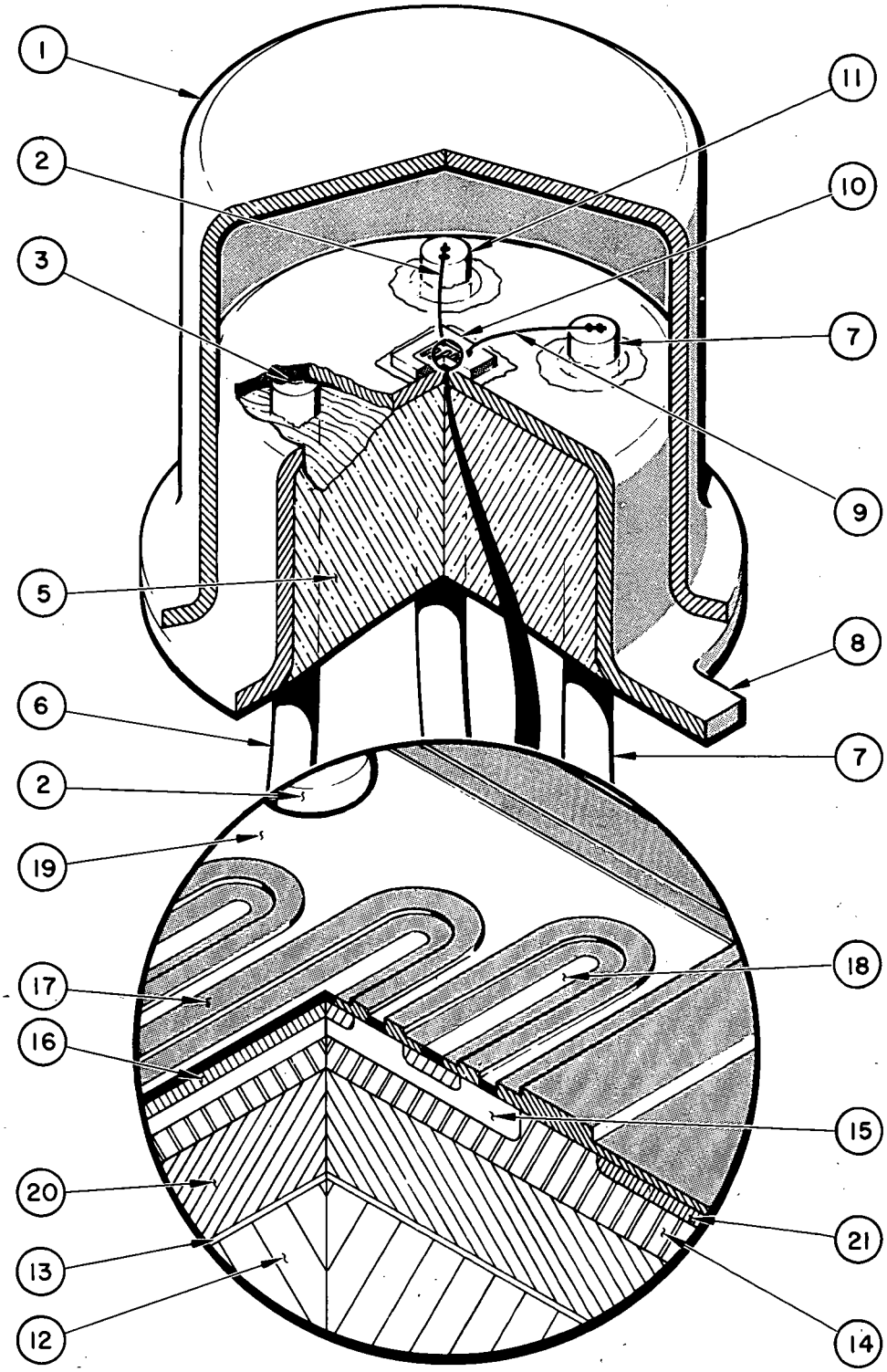


Figure 18-1. Typical Bipolar Transistor (Planar Epitaxial)

FLOW DIAGRAM			RELATED PROBLEM CODES (see foldout in the Appendix)			
MATERIAL	MANUFACTURING OPERATION	CRITICAL PROCESS	OPEN I	SHORT II	PAR DEV III	MECH ANOM IV
Epitaxial Wafer	Clean wafer	Removal of contamination and uniformity of finished surface		E4	A9; B5	
Photoresist, Base Mask	Photoresist process – base	Spin speed, temperature, mask contact pressure, exposure, time, and development		E4	A9; B5	
(15) Dopant	Base predeposition	Time, temperature, humidity, source, and furnace profile		E3, 4	A1, 8, 9; B5	
	Measure V/I	Probe pressure	B3	E1	A7; B2	
	Clean wafer	Wafer cleanliness		E4	A9; B5	
	Base drive-in	Time, temperature, and humidity		E4	A9; B5	
	Measure V/I	Probe pressure	B3	E1	A7; B2	
Photoresist, Emitter and Annular Ring Mask	Photoresist process – emitter and annular ring	Spin speed, temperature, mask contact pressure, exposure, time, and development		E4	A9; B5	
	Clean wafer	Wafer cleanliness		E4	A9; B5	
(16) (21) Dopant	Emitter and annular ring diffusion	Time and temperature		E3, 4	A8, 9; B5	
	Clean wafer	Wafer cleanliness	B4		B4	
(18) (19) Aluminum	Aluminum evaporation	Pressure (vacuum)	B4		B4	
Photoresist, Metal Removal	Photoresist process – metal removal	Spin speed, temperature, mask contact pressure, exposure, time, and development	B5, 6	E2	B4	
	Clean wafer	Wafer cleanliness			A10	
	Aluminum alloying	Time and temperature			A10	
	Test wafer		all	all	all	
	Back lap	Grit size and time				
(10) (13) Gold	Gold evaporation	Pressure (vacuum)	A5; B1, 2	E5	B3	
	100% test		all	all	all	
	Scribe and break	Point pressure	B3	E1	A7; B2	
(4) Header	Chip attach	Temperature	B1, 2	E5	B4	A1, 2, 3, 4, 5; B1, 2, 3
(2) (9) Internal Leads	Wire bond	Temperature and pressure	A1, 2	B	B1	
	100% visual	Inspector training and vision		B		
	Wash and bake	Cleanliness		A1, 2	A2, 4	
(1) Can	Weld on can	N_2 atmosphere, pressure, and heat		A2; C	A2, 4, 5	
	High temperature storage					
	Temperature cycling					
	100% screening					
	Group "A" and "B" sample testing					
	Mark, pack, and ship					B4, 5

NOTE: For items (1) through (21) see Fig. 18-1.

Figure 18-2. Bipolar Transistor - Typical Assembly Flow with Related Problem Codes

BIPOLAR TRANSISTORS

FAILURE ANALYSIS TECHNIQUES

General. Failure analysis is performed to establish remedies for the cause of component failure. It is used to define changes, where required, in component application criteria and/or installation and testing procedures. Very often it reveals subtle modifications in component manufacturing materials and processes and/or screening that can enhance application capability of the component. Failure analysis findings can show the need for transistor redesign (improvement in materials, processes and controls) and, most important, the need for proper part application.

Predominant Failures. Misapplication, whether caused by a marginal circuit design or the improper application of power during use, is the greatest cause of transistor failure. Burn marks, melted leads, unusual discoloration, massive cracks with burning and/or discoloration are the usual indications of misapplication. Misapplication can also occur in the mounting of the transistor. Indications of improper mounting application would be corrosion of external leads, cracking of the lead-to-header seal resulting in destruction of the hermetic seal, and shorting of external leads to the package.

It is important to note that the collector is almost always connected to the transistor case, a fact which has resulted in the collector being shorted to case ground, to other unrelated collector circuits (through common heatsinks), circuit board traces, etc.

Dissection Precautions. Grinding and polishing, if not performed in small increments, can easily pass through the failed area without detecting its presence.

Failure Analysis Flow. The failure analysis flow which follows provides for maximum nondestructive evaluation of the failed part prior to decapping and subsequent dissection.

Relationship to Failures. Where it is relevant, each step of the failure analysis procedure (Figure 18-3) is related to one of the four major problem areas and their causes by a coding system which is defined on the foldout in the Appendix. Thus, one experiencing a specific type of failure can identify those steps in the failure analysis most likely to reveal the problem.

NOTE

RECORD AND/OR PHOTOGRAPH ALL OPERATIONS AND ANOMALIES DURING THE FAILURE ANALYSIS PROCEDURE.

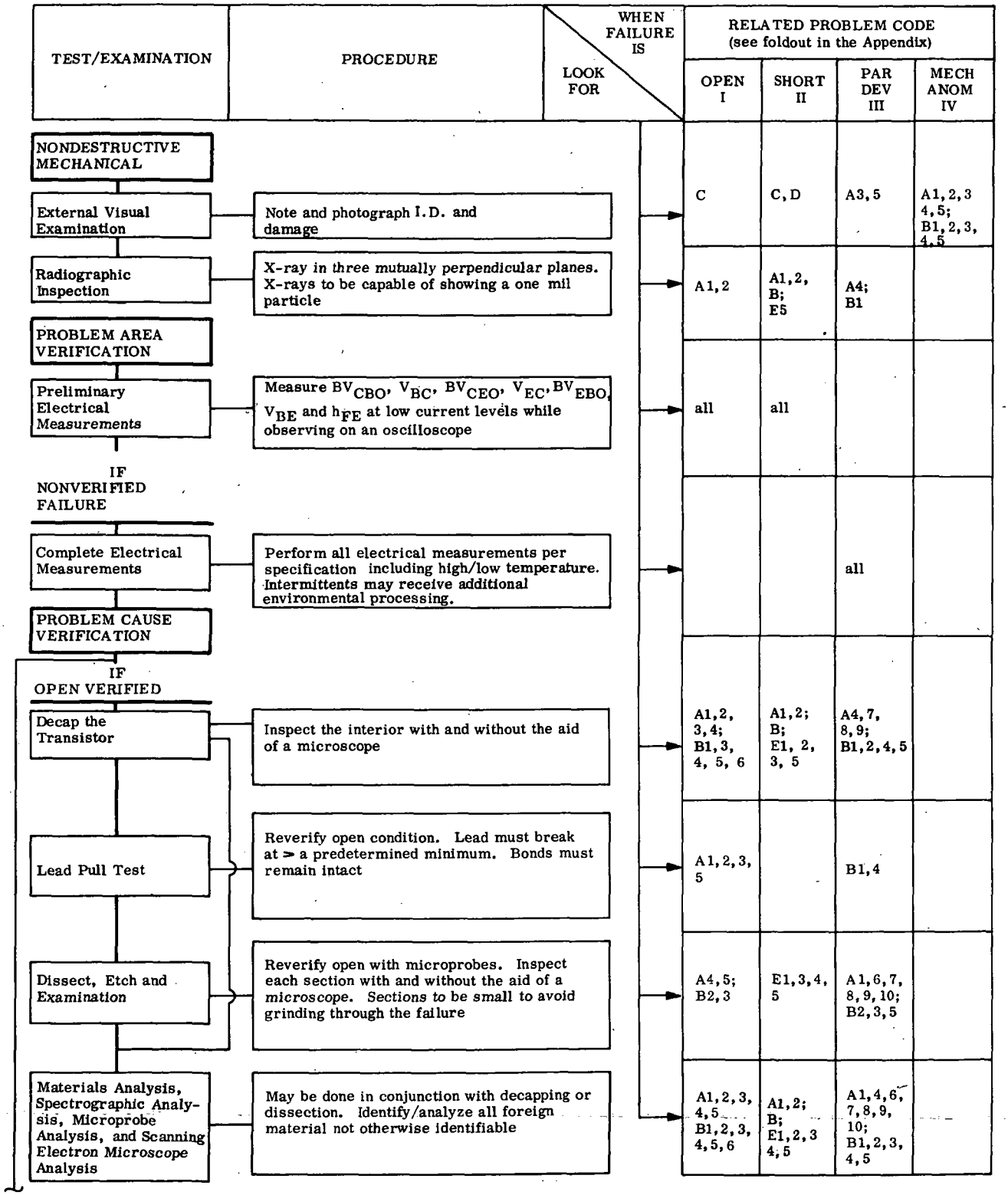


Figure 18-3. Bipolar Transistor - Typical Failure Analysis Flow with Related Problem Codes

TEST/EXAMINATION	PROCEDURE	WHEN FAILURE IS / LOOK FOR	RELATED PROBLEM CODE (see foldout in the Appendix)			
			OPEN I	SHORT II	PAR DEV III	MECH ANOM IV
IF SHORT VERIFIED						
Check Hermetic Seal	Check fine and gross leak rate		C	C	A5	B2,3
Decap the Transistor	Inspect the interior with and without the aid of a microscope		A1,2,3; B1,3,4,5,6	A1,2; B; E1,2,3,4,5	A4,7,8,9; B1,2,4,5	
Metallization Removal	Remove chip metallization and microprobe the bare chip. Improvement suggests:		B4,5,6	E2,3	A8; B4	
Dissect, Etch and Examination	Inspect each section with and without the aid of a microscope. Sections to be small to avoid grinding through the failure		A4,5; B2,3	E1,3,4,5	A1,6,7,8, 9,10; B2,3,5	
Materials Analysis, Spectrographic Analysis, Microprobe Analysis, and Scanning Electron Microscope Analysis	May be done in conjunction with decapping, metallization removal and/or dissection. Identify/analyze all foreign material not otherwise identifiable.		A1,2,3,4,5; B1,2,3,4,5,6	A1,2; B; E1,2,3,4,5	A1,4,6,7, 8,9,10; B1,2,3,4,5	
IF ELECTRICAL PARAMETER DEVIATION VERIFIED						
Check Hermetic Seal	Check fine and gross leak rate		C	C	A5	B2,3
Bake at Maximum Rated Storage Temperature	Determine if condition improves following 48 hour bake				A1	
Clean Exterior	Determine if condition improves following thorough cleaning. Improvement suggests:			D	A3	
Temperature Cycle	Monitor faulty parameter while temperature cycling. Improvement suggests:		A3,4; B3	A1,2; B; E1	A2,4,7; B1,2	
Decap the Transistor	Inspect the interior with and without the aid of a microscope		A1,2,3; B1,3,4,5,6	A1,2; B; E1,2,3,4,5	A4,7,8,9; B1,2,4,5	
Vacuum Bake at Maximum Rated Storage Temperature	Cool in a dry ambient atmosphere. Improvement suggests:				A2	
Clean Chip	Improvement suggests:			A (all)	A4	
Remove Metallization Oxide	Improvement suggests:		B4,5,6	E2,3	A8; B4	
Dissect, Etch and Examination	Inspect each section with and without magnification. Sections must be in small increments so as to avoid grinding through the failed area		A4,5; B2,3	E1,3,4,5	A1,6,7,8, 9,10; B2,3,5	
Materials Analysis, Spectrographic Analysis, Microprobe Analysis, and Scanning Electron Microscope Analysis	May be done in conjunction with decapping or dissection. Identify/analyze all foreign material not otherwise identifiable		A1,2,3,4,5; B1,2,3,4,5,6	A1,2; B; E;,2,3,4,5	A1,4,6,7, 8,9,10; B1,2,3,4, 5	

Figure 18-3. Bipolar Transistor - Typical Failure Analysis Flow with Related Problem Codes

METAL-OXIDE-SEMICONDUCTOR FIELD-EFFECT TRANSISTORS

CHARACTERISTICS

The most distinguishing feature of a MOS FET as a semiconductor device is the extremely high input impedance (expressed as gate to source current). Gate to source current in a MOS FET is not affected by the polarity of the voltage source and will be in the order of 10 to 100 picoamperes maximum, i.e., with a voltage source of ±25Vdc the input resistance would be 4×10^{13} to 4×10^{12} ohms minimum. A special handling problem is associated with this high input resistance in that, prior to installation, the leads must be shorted together to avoid damage by an accumulation of excess static charge.

The metal-oxide-semiconductor field-effect transistor uses a metal gate electrode separated from the semiconductor material by an insulator. This insulated gate can deplete and/or enhance the conductivity of the channel without increasing steady-state input current or reducing power gain.

Three types of MOS FET are possible. These are: The type "A" depletion MOS FET, the type "C" enhancement mode MOS FET, and the type "B" depletion and enhancement mode MOS FET. In the depletion type, charge carriers are available in a "channel" between the drain and source when no gate voltage is available. Application of a gate voltage "depletes" the "channel" of charge carriers thereby reducing the drain to source conductivity. In the enhancement mode MOS FET there are no charge carriers in the channel until the gate is forward biased. Forward biasing of the gate provides charge carriers to the "channel" thereby enhancing the drain to source conductivity. The type "B" MOS FET is in fact the result of a type of application rather than a specific design. That is, when a type "A" depletion mode MOS FET gate is forward biased additional charge carriers are available thereby enhancing the channel conductivity. Therefore, all depletion mode MOS FET are in fact type "B" depletion-enhancement mode devices.

The next subsection describes problems and failure mechanisms found in MOS FET caused by design deficiency, lack of process control, and inadequate quality control. It contains a drawing, a materials list, and a manufacturing flow chart for an enhancement mode MOS FET. The depletion mode MOS FET is manufactured in the same manner except for an additional channel diffusion process.

METAL-OXIDE-SEMICONDUCTOR FIELD-EFFECT TRANSISTORS

DESIGN AND PRODUCTION CONSIDERATIONS

Failures Related to Process. A typical enhancement mode MOS FET (Figure 18-4) and a typical assembly flow (Figure 18-5) are presented together with the suggested controls required to assure a reliable product. The "Critical Process" is defined for each of the manufacturing steps. Relationship is established between failure causes and the manufacturing process. Having experienced a specific problem, one could identify those manufacturing steps with potential for contributing to the failure.

Assembly Flow. A typical manufacturing flow for a MOS FET is presented together with the process name and the constituent added. Included in the typical manufacturing flow is a listing of the significant variable for each process; a significant variable is one which if not closely controlled will result in an inferior if not useless product. Circled numbers in the constituent added column are directly related to the circled numbers in the typical drawing.

Assembly Precautions. Contamination, conductive and nonconductive, is the greatest cause of MOS FET failure directly related to the assembly process. As such, one should assure that specific in-process inspection and testing be designed so as to eliminate and or detect contamination.

The following is a partial list of the most probable sources of contamination:

1. Conductive Contamination
   a. Wire Bonding Processes (bits of loose wire)
   b. Chip Bonding Process (loosely attached expulsion or die-bonding material drawn across die by tweezers)
   c. Can-to-Header Welding Process (weld splash)
2. Nonconductive Contamination
   a. Sealing Process (moisture sealed in)
   b. Cleaning Processes (corrosive chemical residue)
   c. Chip Passivating Process (contaminants in passivating material)

CAUTION

HANDLING. IN ADDITION TO THE CAUTION NOTES BELOW, SEE PAGE 17-37 FOR HANDLING PRECAUTIONS.

MOS FIELD-EFFECT TRANSISTORS HAVE EXTREMELY HIGH INPUT RESISTANCE. THEY CAN BE DAMAGED BY THE ACCUMULATION OF EXCESS STATIC CHARGE. AVOID POSSIBLE DAMAGE TO THE DEVICES WHILE HANDLING, TESTING, OR IN ACTUAL OPERATION, BY FOLLOWING THE PROCEDURES OUTLINED BELOW:

1. TO AVOID THE BUILD-UP OF STATIC CHARGE, THE LEADS OF THE DEVICES SHOULD REMAIN SHORTED TOGETHER EXCEPT WHEN BEING TESTED OR USED.

2. AVOID UNNCESSSARY HANDLING. PICK UP DEVICES BY THE CASE INSTEAD OF THE LEADS.

3. DO NOT INSERT OR REMOVE DEVICES FROM CIRCUITS WITH THE POWER ON BECAUSE TRANSIENT VOLTAGES MAY CAUSE PERMANENT DAMAGE TO THE DEVICES.

TYPICAL MOS FET (ENHANCEMENT MODE) DESIGN (Figure 18-4)

ITEM	ITEM NAME	MATERIAL OF CONSTRUCTION
1	Can	Grade "A" nickel, TO-18
2	Drain Internal Lead	99.9% Gold, 1 mil diameter
3	Gate Internal Lead	99.9% Gold, 1 mil diameter
4	Chip	Silicon
5	Header	Kovar, gold plated
6	Seal	Type D-120 glass
7	Case Lead	Kovar (butt welded), gold plated
8	Gate Lead	Kovar, gold plated
9	Drain Lead	Kovar, gold plated
10	Source Lead	Kovar, gold plated
11	Chip-to-Header Scrub Bond	Gold silicon eutectic
12	Source Internal Lead	99.9% Gold, 1 mil diameter
13	Gate Metallization	Vacuum deposited aluminum
14	Source metallization	Vacuum deposited aluminum
15	Drain Metallization	Vacuum deposited aluminum
16	Passivation	Silicon dioxide and silicon nitrate
17	Substrate	Boron doped silicon
18	Drain Diffusion	Heavily phosphorous doped silicon
19	Source Diffusion	Heavily phosphorous doped silicon

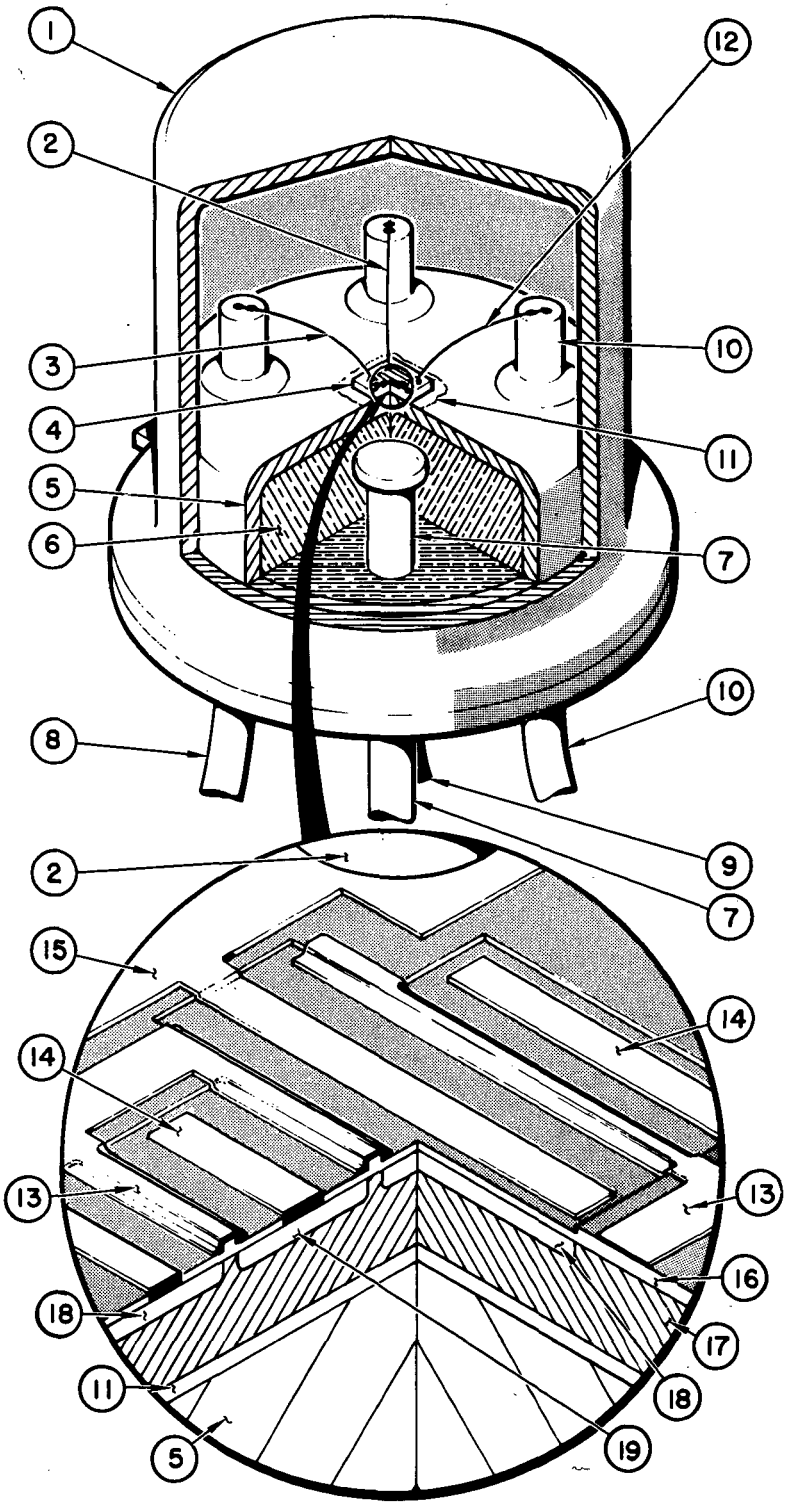
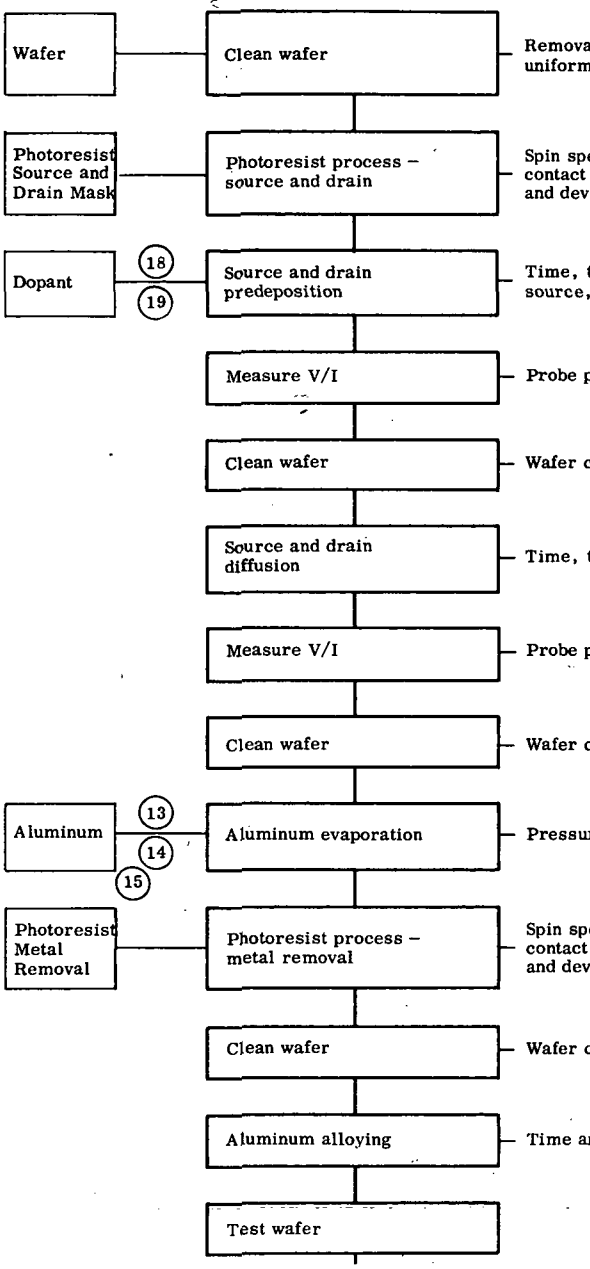
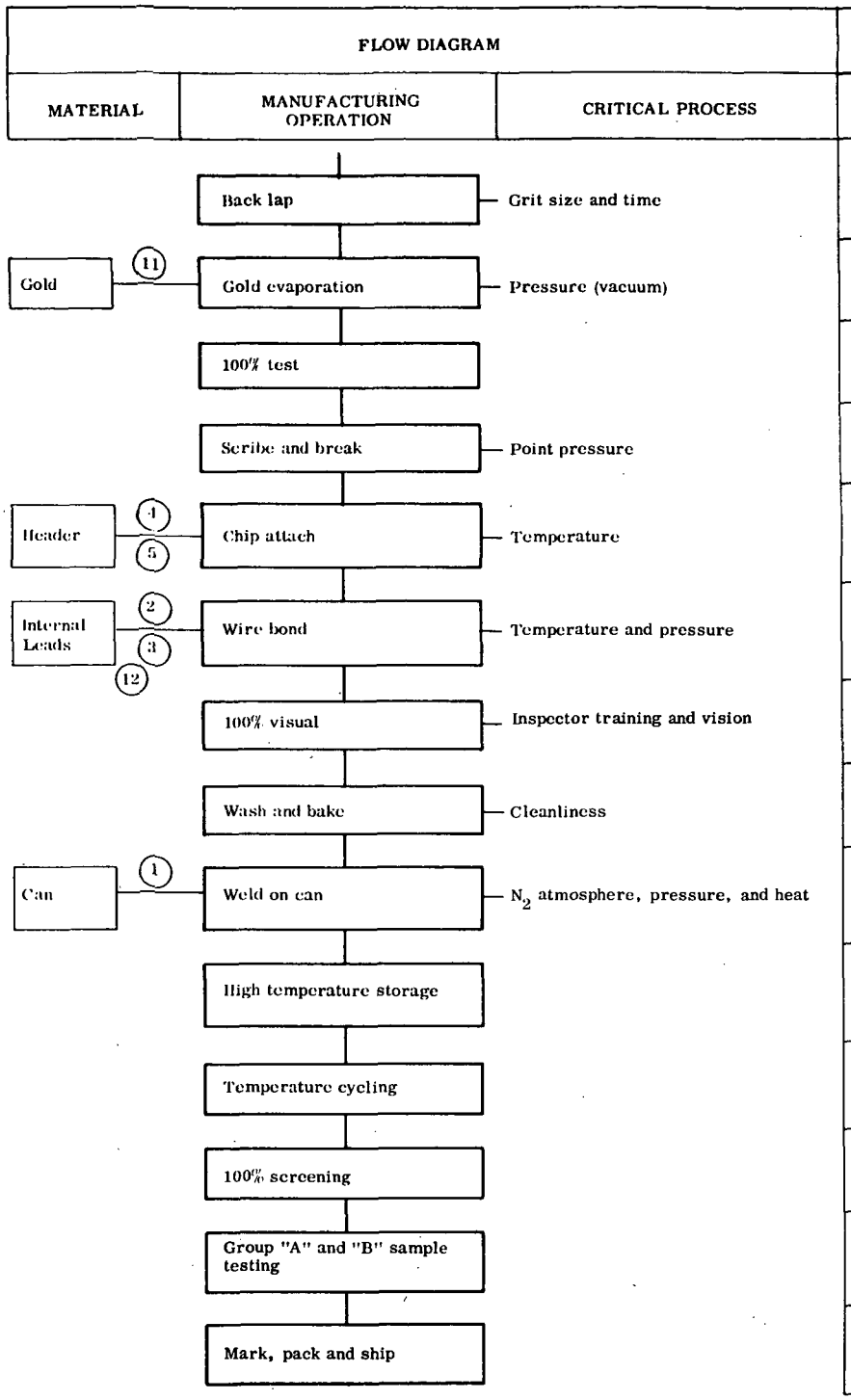


Figure 18-4. Typical MOS FET (Enhancement Mode)



FLOW DIAGRAM			RELATED PROBLEM CODES (see foldout in the Appendix)			
MATERIAL	MANUFACTURING OPERATION	CRITICAL PROCESS	OPEN I	SHORT II	PAR DEV III	MECH ANOM IV
	Clean wafer	Removal of contamination and uniformity of finished surface		E4	A9; B5	
	Photoresist process – source and drain	Spin speed, temperature, mask contact pressure, exposure time, and development		E4	A9; B5	
	Source and drain predeposition	Time, temperature, humidity, source, and furnace profile		E3,4	A8,9,11; B5	
	Measure V/I	Probe pressure	B3	E1	A7; B2	
	Clean wafer	Wafer cleanliness		E4	A9; B5	
	Source and drain diffusion	Time, temperature, and humidity		E3,4	A8,9,11; B5	
	Measure V/I	Probe pressure	B3	E1	A7; B2	
	Clean wafer	Wafer cleanliness	B4		B4	
	Aluminum evaporation	Pressure (vacuum)	B4		B4	
	Photoresist process – metal removal	Spin speed, temperature, mask contact pressure, exposure time, and development	B5,6	E2	B4	
	Clean wafer	Wafer cleanliness			A10	
	Aluminum alloying	Time and temperature			A10	
	Test wafer		all	all	all	

Figure 18-5. MOS FET - Typical Assembly Flow with Related Problem Codes



FLOW DIAGRAM			RELATED PROBLEM CODES (see foldout in the Appendix)			
MATERIAL	MANUFACTURING OPERATION	CRITICAL PROCESS	OPEN I	SHORT II	PAR DEV III	MECH ANOM IV
	Back lap	Grit size and time				
Gold (11)	Gold evaporation	Pressure (vacuum)	A5; B1,2	E5	B3	
	100% test		all	all	all	
	Scribe and break	Point pressure	B3	E1	A7; B2	
Header (4, 5)	Chip attach	Temperature	B1,2	E5	B4	A1,2,3,4,5; B1,2,3
Internal Leads (2, 3, 12)	Wire bond	Temperature and pressure	A1,2	B	B1	
	100% visual	Inspector training and vision		B		
	Wash and bake	Cleanliness		A1,2	A2,4	
Can (1)	Weld on can	N_2 atmosphere, pressure, and heat		A2;C	A2,4,5	
	High temperature storage					
	Temperature cycling					
	100% screening					
	Group "A" and "B" sample testing					
	Mark, pack and ship					B4,5

Figure 18-5. MOS FET - Typical Assembly Flow with Related Problem Codes

METAL-OXIDE-SEMICONDUCTOR FIELD-EFFECT TRANSISTORS

FAILURE ANALYSIS TECHNIQUES

General. Failure analysis is performed to establish remedies for the cause of component failure. It is used to define changes (where required) in component application criteria and/or installation and testing procedures. Very often it reveals subtle modifications in component manufacturing materials and processes and/or screening that can enhance application capability of the component. Failure analysis findings can show the need for transistor redesign (improvement in materials, processes, and controls), and, most important, the need for proper part application.

Predominant Failures. Misapplication, whether caused by a marginal circuit design or the improper application of power during use, is the greatest cause of MOS field-effect transistor failure.

Burn marks, melted leads, unusual discoloration, massive cracks with burning and/or discoloration are the usual indications of misapplication. Misapplication can also occur in the mounting of the transistor. Indications of improper mounting application would be corrosion of external leads, cracking of the lead-to-header seal resulting in destruction of the hermetic seal, and shorting of external leads to the package.

Dissection Precautions. Grinding and polishing, if not performed in small increments, can easily pass through the failed area without detecting its presence.

Failure Analysis Flow. The failure analysis flow which follows provides for maximum nondestructive evaluation of the failed part prior to decapping and subsequent dissection.

Relationship to Failures. Where it is relevant, each step of the failure analysis procedure (Figure 18-6) is related to one of the four major problem areas and their causes by a coding system which is defined on the foldout in the Appendix. Thus, one experiencing a specific type of failure can identify those steps in the failure analysis most likely to reveal the problem.

NOTE: 1. Record all operations and photograph all anomalies during the failure analysis procedure.

2. Be sure that the extremely high gate input impedance is not misinterpreted as an open circuit condition.

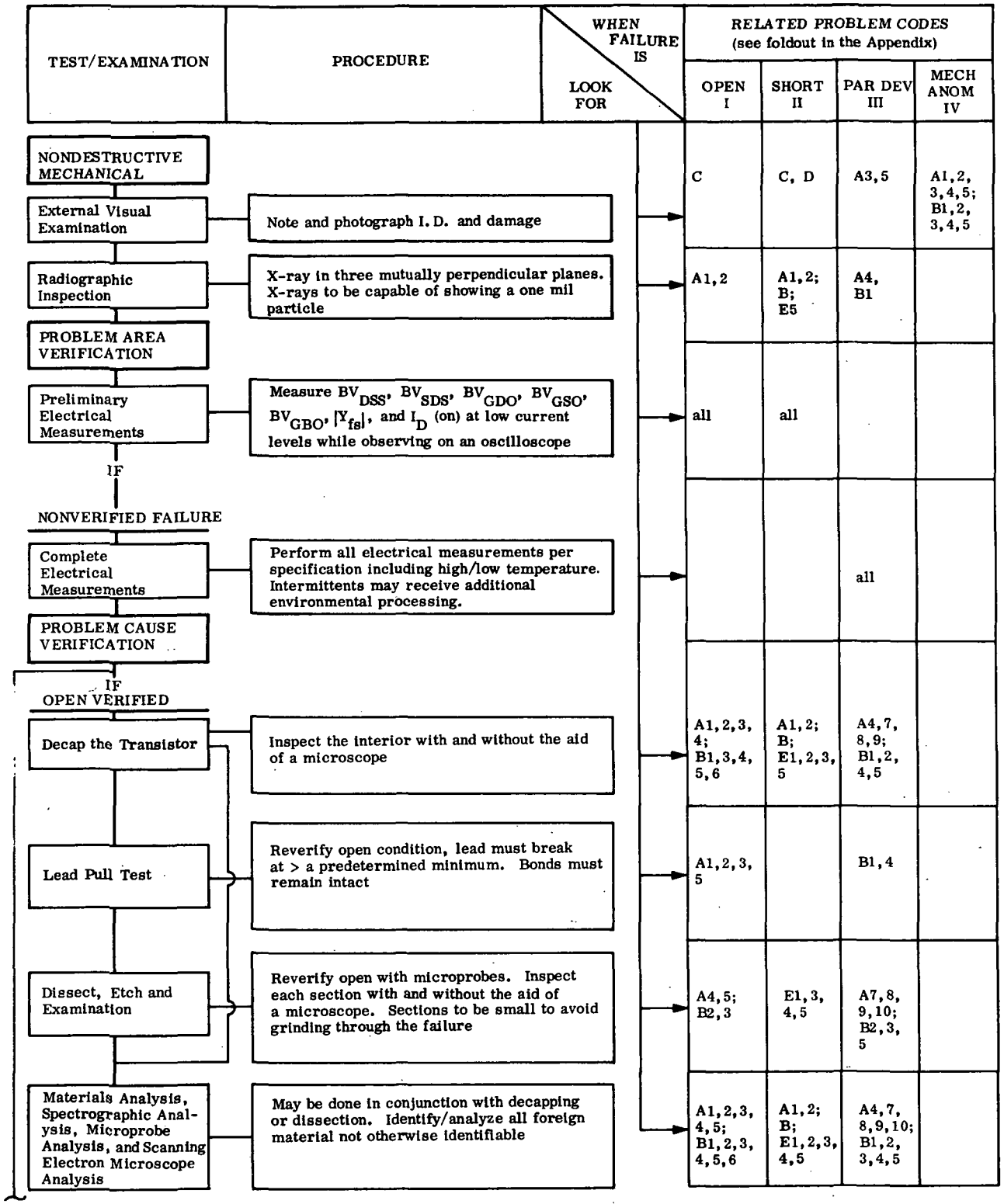


Figure 18-6. MOS FET - Typical Failure Analysis Flow with Related Problem Codes

TEST/EXAMINATION	PROCEDURE	WHEN FAILURE IS / LOOK FOR	RELATED PROBLEM CODES (see foldout in the Appendix)			
			OPEN I	SHORT II	PAR DEV III	MECH ANOM IV
IF SHORT VERIFIED						
Check Hermetic Seal	Check fine and gross leak rate		C	C	A5	B2,3
Decap the Transistor	Inspect the interior with and without the aid of a microscope		A1,2,3; B1,3,4, 5,6	A1,2;B; E1,2,3,4, 5	A4,7,8,9; B1,2,4,5	
Metallization Removal	Remove chip metallization and microprobe the bare chip. Improvement suggests:		B4,5,6	E2,3	A8;B4	
Dissect, Etch and Examination	Inspect each section with and without the aid of a microscope. Sections to be small to avoid grinding through the failed area		A4,5; B2,3	E1,3,4,5	A7,8,9,10; B2,3,5	
Materials Analysis, Spectrographic Analysis, Microprobe Analysis, and Scanning Electron Microscope Analysis	May be done in conjunction with decapping, metallization removal and/or dissection. Identify/analyze all foreign material not otherwise identifiable		A1,2,3,4, 5; B1,2,3, 4,5,6	A1,2; B; E1,2,3,4,5	A4,7,8,9, 10, B1,2,3,4, 5	
IF ELECTRICAL PARAMETER DEVIATION VERIFIED						
Check Hermetic Seal	Check fine and gross leak rate		C	C	A5	B2,3
Bake at Maximum Rated Storage Temperature	Determine if condition improves following 48 hour bake				all	
Clean Exterior	Determine if condition improves following thorough cleaning. Improvement suggests:			D	A3	
Temperature Cycle	Monitor faulty parameter while temperature cycling. Improvement suggests:		A3,4; B3	A1,2; B;E1	A4,7; B1,2	
Decap the Transistor	Inspect the interior with and without the aid of microscope		A1,2,3; B1,3,4,5,6	A1,2;B; E1,2,3,4,5	A4,7,8,9; B1,2,4,5	
Vacuum Bake at Maximum Rated Storage Temperature	Cool in a dry ambient atmosphere. Improvement suggests:				A2	
Clean Chip	Improvement suggests:			A (all)	A4	
Remove Metallization and Oxide	Improvement suggests:		B4,5,6	E2,3	A8; B4	
Dissect, Etch and Examination	Inspect each section with and without magnification. Sections must be in small increments so as to avoid grinding through the failure		A4,5; B2,3	E1,3,4,5	A7,8,9,10; B2,3,5	
Materials Analysis, Spectrographic Analysis, Microprobe Analysis, and Scanning Electron Microscope Analysis	May be done in conjunction with decapping or dissection. Identify/analyze all foreign material not otherwise identifiable		A1,2,3,4, 5; B1,2,3,4, 5,6	A1,2;B; E1,2,3,4, 5	A4,7,8,9, 10; B1,2,3,4,5	

Figure 18-6. MOS FET - Typical Failure Analysis Flow with Related Problem Codes

JUNCTION FIELD EFFECT TRANSISTORS (JFET)

CHARACTERISTICS

The JFET differs distinctly from the conventional junction transistor because its operation depends upon the flow of majority carriers only. Therefore, it falls into the class of unipolar transistors, or those in which only one type of carrier predominates. It is a normally "on" device, i.e., a conducting channel of "N" or "P" semiconductor material connects the source-to-drain even in the absence of a gate-to-source voltage (V_{GS}). The channel will conduct in either direc ion. As voltage is applied between gate and source (positive for P-channel and negative for N-channel), the channel depletes, thereby reducing drain to source conduction. The magnitude of V_{GS} required to reduce channel conduction to "zero" is called pinch off voltage (V_P).

Input impedance of a JFET is resistive, appearing as a reverse biased diode (approximately 10^{10} ohms), whereas the input impedance of a MOS FET is capacitive.

Temperature Effects. I_{GSS}, the total gate leakage current flowing from gate to channel with $V_{DS} = 0$, doubles for approximately every 10°C increase in temperature. V_P, gate-to-source voltage required to pinch off the channel, increases by about 2.2 mV/°C with increasing temperature for both P- and N-channel types.

Mechanical Characteristics. Several process techniques are available for the manufacture of JFET - predominant are the double diffused and epitaxial diffused techniques. The next subsection describes problems and failure mechanisms found in JFET caused by design deficiency, lack of process control, and inadequate quality control; and contains a drawing, a materials list, and a manufacturing flow diagram for a typical N-channel epitaxial-diffused JFET.

JUNCTION FIELD-EFFECT TRANSISTORS

DESIGN AND PRODUCTION CONSIDERATIONS

Failures Related to Process. A typical N-channel JFET (Figure 18-7) and a typical assembly flow (Figure 18-8) are presented together with the suggested controls required to assure a reliable product. The "Critical Process" is defined for each of the manufacturing steps. Relationship is established between failure causes and the manufacturing process. Having experienced a specific problem, one could identify those manufacturing steps with potential for contributing to the failure.

Assembly Flow. A typical manufacturing flow for a JFET is presented together with the process name and the constituent added. Included in the typical manufacturing flow is a listing of the significant variable for each process; a significant variable is one which if not closely controlled will result in an inferior if not useless product. Circled numbers in the constituent added column are directly related to the circled numbers in the typical drawing.

Assembly Precautions. Contamination, conductive and nonconductive, is the greatest cause of JFET failure directly related to the assembly process. As such, one should assure that specific in-process inspection and testing be designed so as to eliminate and or detect contamination.

The following is a partial list of the most probable sources of contamination:

1. Conductive Contamination
   a. Wire Bonding Processes (bits of loose wire)
   b. Chip Bonding Process (loosely attached expulsion or die-bonding material drawn across die by tweezers)
   c. Can-to-Header Welding Process (weld splash)
2. Nonconductive Contamination
   a. Sealing Process (moisture sealed in)
   b. Cleaning Processes (corrosive chemical residue)
   c. Chip Passivating Process (contaminants in passivating material)

TYPICAL JFET (N-CHANNEL) DESIGN (Figure 18-7)

ITEM	ITEM NAME	MATERIAL OF CONSTRUCTION
1	Can	Nickel - electronic grade A
2	Source Lead	Gold plated Kovar
3	Drain Interconnect Wire	Aluminum wire (99 percent) or Gold wire (99.99 percent), 1 mil
4	Chip	Doped silicon
5	Header	Gold (50 μ inch) plated Kovar
6	Glass Seal	Type 7052 or equivalent
7	Gate Lead	Gold plated Kovar
8	Die Attach Area	
9	Butt Weld Area	
10	Index Tab	Extension of header
11	Epitaxial Silicon (Channel)	N-type (phosphorous dopant)
12	Drain Diffusion Area	N+type (phosphorous dopant)
13	Drain Metallization	Vacuum deposited aluminum
14	Passivation Layer	Silicon dioxide SiO_2)
15	Gate Lead	Gold plated Kovar
16	Gate Lead Plating	Electrolysis deposited gold
17	Solder Preform	
18	Metallized Backing	Vacuum deposited gold
19	Silicon Substrate	P-type (boron dopant)
20	Gate Diffusion	P-type (boron dopant)
21	Source Metallization	Vacuum deposited aluminum
22	Drain metallization	Vacuum deposited aluminum
23	Drain Pad	Vacuum deposited aluminum
24	Drain Interconnect Wire Bonded to Pad	Aluminum wire (99 percent) or Gold wire (99.99 percent), 1 mil

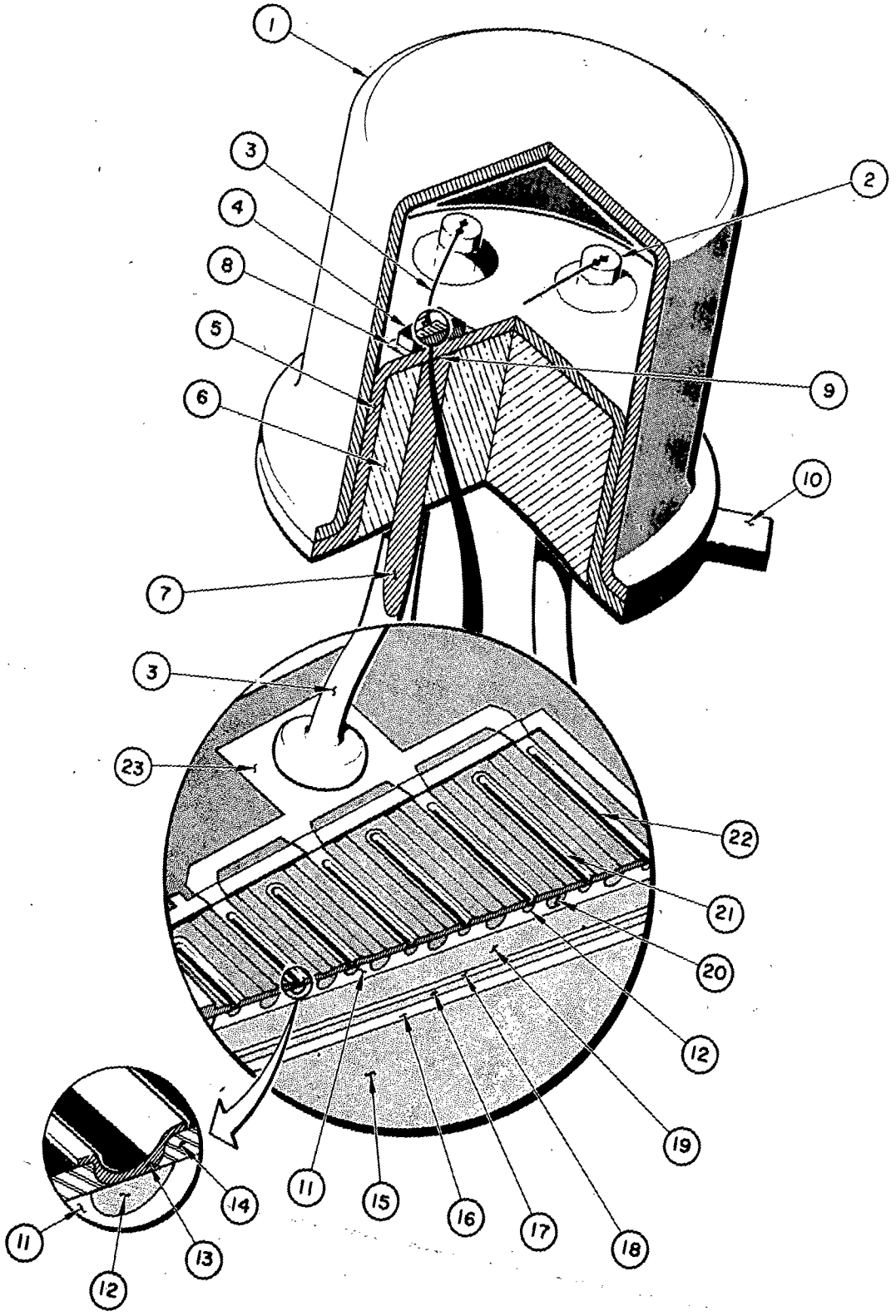


Figure 18-7. Typical JFET (N-Channel)

FLOW DIAGRAM			RELATED PROBLEM CODES (see foldout in the Appendix)			
MATERIAL	MANUFACTURING OPERATION	CRITICAL PROCESS	OPEN I	SHORT II	PAR DEV III	MECH ANOM IV
Wafer	Clean wafer	Removal of contamination and uniformity of finished surface		E4	A9; B5	
Photoresist-Isolation Mask	Photoresist process-isolation	Spin speed, temperature, mask contact pressure, exposure time, and development		E4	A9; B5	
Dopant	Isolation predeposition	Time, temperature, humidity, source, and furnace profile		E3, 4	A8, 9, 11; B5	
	Measure V/I	Probe accuracy and pressure	B3	E1	A7; B2	
	Isolation diffusion	Time, temperature, and humidity		E3, 4	A8, 9, 11; B5	
	Measure V/I	Probe accuracy and pressure	B3	E1	A7; B2	
	Clean wafer	Wafer cleanliness	B4		B4	
Photoresist-Gate Mask	Photoresist process-gate	Spin, speed, temperature, mask contact pressure, exposure time, and development		E4	A9; B5	
Dopant (20)	Gate predeposition	Time, temperature, humidity, source, and furnace profile		E3, 4	A8, 9, 11; B5	
	Measure V/I	Probe accuracy and pressure	B3	E1	A7; B2	
	Gate diffusion	Time, temperature, and humidity		E3, 4	A8, 9, 11; B5	
	Measure V/I	Probe accuracy and pressure	B3	E1	A7; B2	
	Gate oxidation	Flow rate of air and furnace profile		E3, 4	A8, 9, 11; B5	
Photoresist, Drain and Source Mask	Photoresist process-drain and source	Spin, speed, temperature, mask contact pressure, exposure time, and development		E4	A9; B5	
Dopant (12)	Drain and source predeposition	Time, temperature, humidity, source, and furnace profile		E3, 4	A8, 9, 11; B5	
	Measure V/I	Probe accuracy and pressure	B3	E1	A7; B2	
	Drain and source diffusion	Time, temperature, and humidity		E3, 4	A8, 9, 11; B5	
	Measure V/I	Probe accuracy and pressure	B3	E1	A7; B2	
	Clean wafer	Wafer cleanliness	B4		B4	
Aluminum (13) (23) (21) (22)	Aluminum evaporation	Pressure (vacuum) and aluminum purity	B4		B4	

Figure 18-8. JFET (N-Channel) - Typical Assembly Flow with Related Problem Codes

FLOW DIAGRAM			RELATED PROBLEM CODES (see foldout in the Appendix)			
MATERIAL	MANUFACTURING OPERATION	CRITICAL PROCESS	OPEN I	SHORT II	PAR DEV III	MECH ANOM IV
Photoresist-Metal Removal	Photoresist process-metal removal	Spin, speed, temperature, mask contact pressure, exposure time, and development	B5, 6	E2	B4	
	Clean wafer	Wafer cleanliness			A10	
	Aluminum alloying	Time and temperature			A10	
	Back lapping	Grit size and time				
	Wafer probe		all	all	all	
(18) Gold	Gold evaporation	Pressure (vacuum) and gold purity	A5; B1, 2	E5	B3	
	Electrical sorting		all	all	all	
	Scribe and break wafers	Pressure and time	B3	E1	A7; B2	
(4) (5) (8) Perform and Header	Die attach	Temperature	B1, 2	E5	B4	A1, 2, 3 4, 5; B1, 2, 3
(3) (24) Internal Leads	Wire bond	Time and temperature	A1, 2	B	B1	
	100% Visual (precap) Inspection	Inspector training and vision		B		
	Wash and bake	Cleanliness		A1, 2	A2, 4	
(1) Can	Final seal	N_2 atmosphere, pressure, and heat		A2; C	A2, 4, 5	
	Final seal inspection	Inspector training and vision				A
	Fine and gross leak test					
	Date code devices					
	High temperature storage	Time and temperature				
	High temperature reverse bias (HTRB)					
	Temperature cycling					
	Electrical classification					
	100% screening to customer requirements (optional)					
	Mark, pack, and ship					B4, 5

NOTE: For items (1) through (23) see Figure 18-7

Figure 18-8. JFET (N-Channel) - Typical Assembly Flow with Related Problem Codes

JUNCTION FIELD-EFFECT TRANSISTORS

FAILURE ANALYSIS TECHNIQUES

General. Failure analysis is performed to establish remedies for the cause of component failure. It is used to define changes (where required) in component application criteria and/or installation and testing procedures. Very often it reveals subtle modifications in component manufacturing materials and processes and/or screening that can enhance application capability of the component. Failure analysis findings can show the need for redesign (improvement in materials, processes, and controls), and, most important, proper part application.

Predominant Failures. Misapplication, whether caused by a marginal design or the improper application of power during use, is the greatest cause of junction field-effect transistor failure.

Burn marks, melted leads, unusual discoloration, massive cracks with burning and/or discoloration are the usual indications of misapplication. Misapplication can also occur in the mounting of the transistor. Indications of improper mounting application would be corrosion of external leads, cracking of the lead-to-header seal resulting in destruction of the hermetic seal, and shorting of external leads to the package.

Dissection Precautions. Grinding and polishing, if not performed in small increments, can easily pass through the failed area without detecting its presence.

Failure Analysis Flow.. The failure analysis flow which follows provides for maximum nondestructive evaluation of the failed part prior to decapping and subsequent dissection.

Relationship to Failures. Where it is relevant, each step of the failure analysis procedure (Figure 18-9) is related to one of the four major problem areas and their causes by a coding system which is defined on the foldout in the Appendix. Thus, one experiencing a specific type of failure can identify those steps in the failure analysis most likely to reveal the problem.

NOTE: 1. Record all operations and photograph all anomalies during the failure analysis procedure.

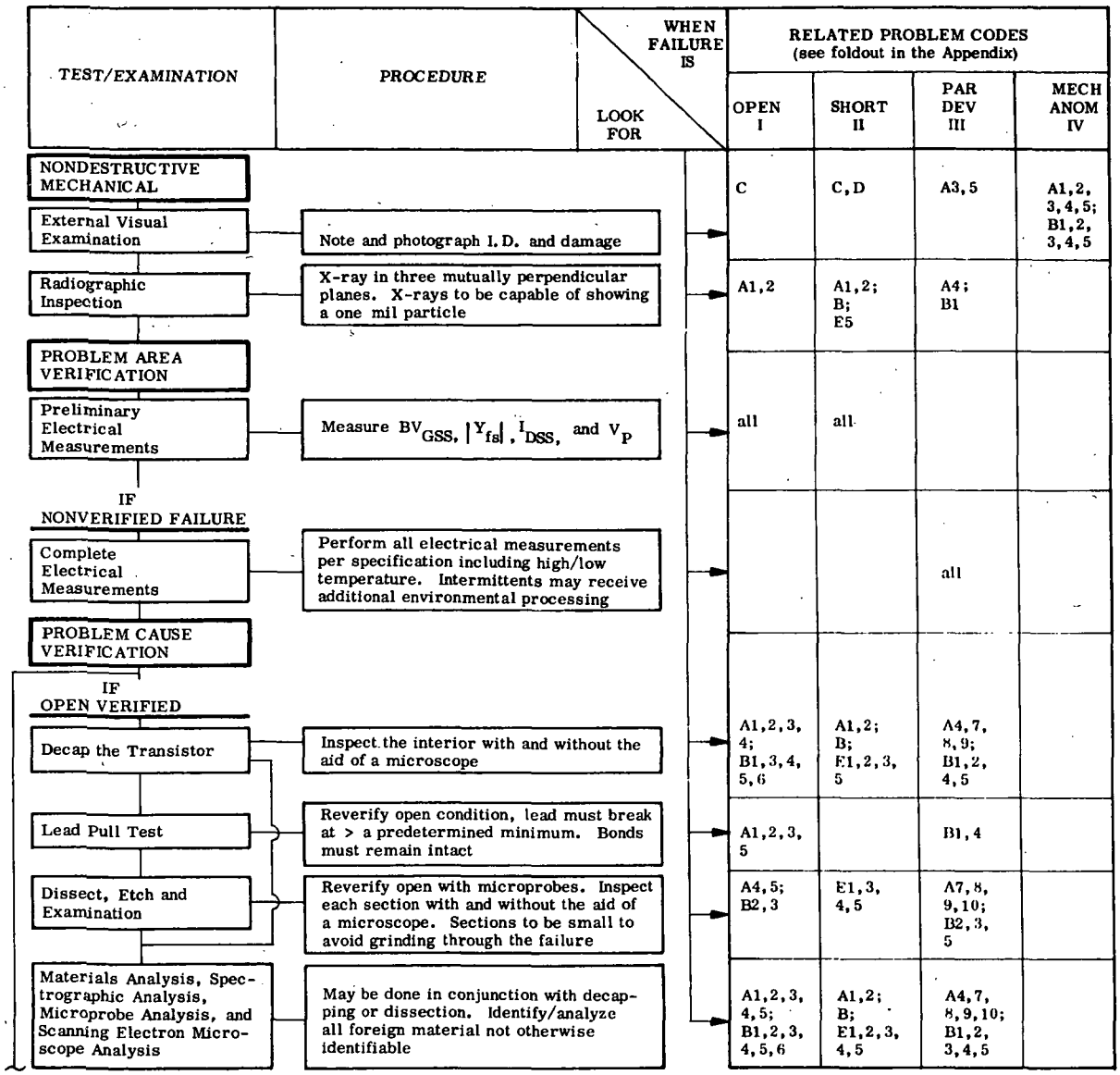


Figure 18-9. JFET (N-Channel) - Typical Failure Analysis Flow with Related Problem Codes

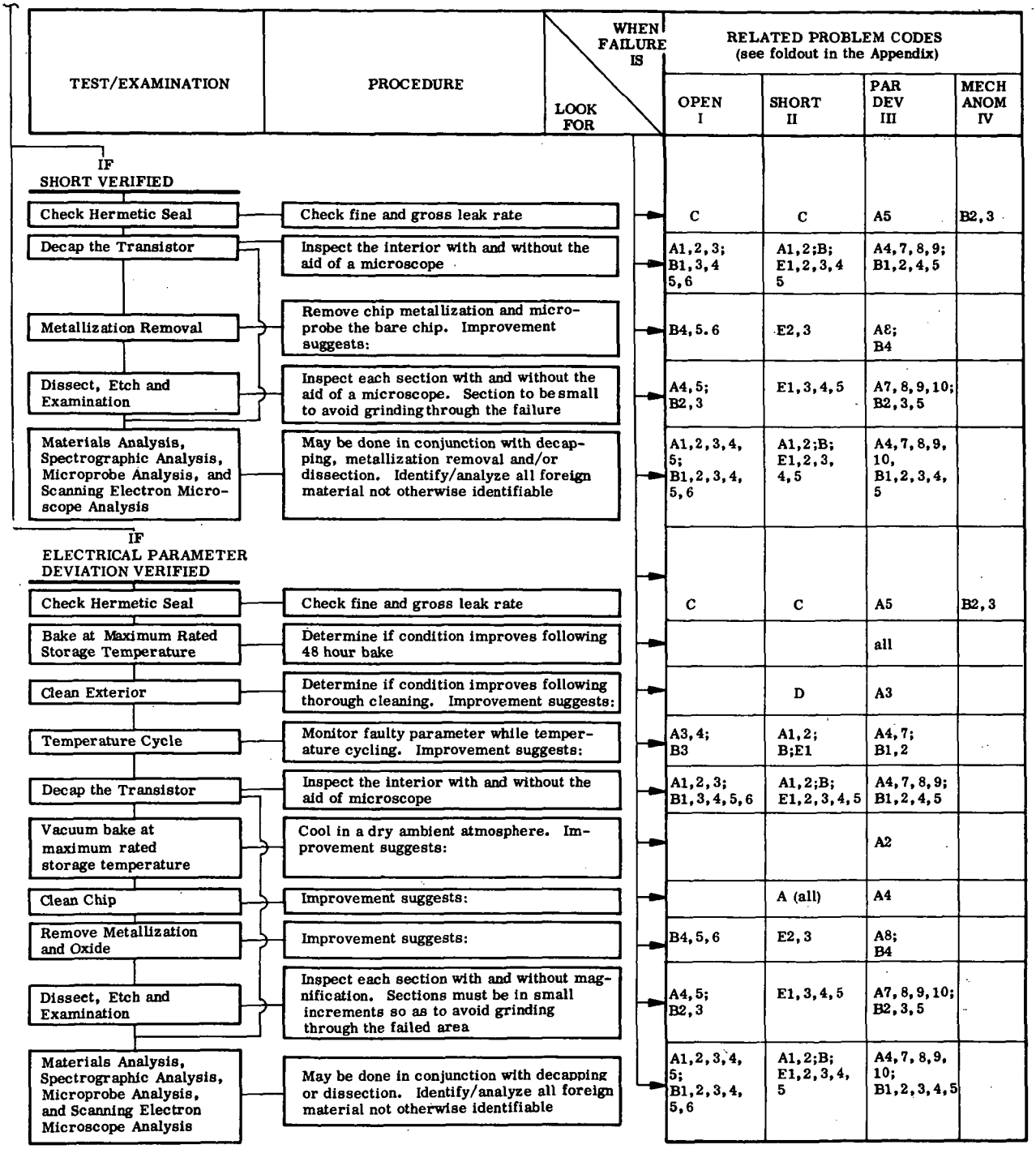


Figure 18-9. JFET (N-Channel) - Typical Failure Analysis Flow with Related Problem Codes

ALERT SUMMARIES

Summaries of ALERT reports issued against Transistors are shown below. They are listed according to problem area - most frequent to least frequent occurences. The "ALERT ITEM NO." (first column) references each summary back to the "Problem Area/Cause and Suggested Action" table.

The ALERT reports are not categorized according to transistor types since almost all of them concern bipolar transistors.

TRANSISTORS

ALERT[1] ITEM NO./ GIDEP NO.	PROBLEM AREA/ Cause	PROBLEM DESCRIPTION	PROBLEM ANALYSIS
1 K2-70-01, 01A	OPEN Lifted bonds	Five transistors failed acceptance testing.	Lifted lead bonds on chip as result of poor lead bonding process at part supplier.
2 MSFC-69-10, 10A, 10B, 10C, 10D	OPEN Lifted bonds	Timer was not timing out during tests.	Transistor was open between base and emitter. Lead wire had fractured at the heel of the thermo-compression wedge bond to the chip where there was a reduction in cross sectional area caused by bonding tool. Switching caused heating and cooling which flexed wire at point of reduced cross sectional area resulting in failure from fatigue.
3 MSFC-69-08	OPEN Lifted bonds	Cracking and separation of bond wire at the heel of the bond.	Excessive bonding pressure and distortion of the bond is primary cause. Failure rate is accelerated by power cycling.
4 GSFC 6-1-66	OPEN Lifted bonds	Transistor failed to operate after an epoxying operation during fabrication.	Failure analysis revealed bar geometry of transistor chip, which is not considered suitable for spacecraft application due to bonding problems. Device should have had teardrop geometry die.
5 E9-71-02	OPEN Lifted bonds	Box level loss of output was traced to a transistor.	Failure mechanism was cracked gold/aluminum intermetallic at the die.
6 B2-71-03, G4-71-02, 02A	OPEN Lifted bonds	Part failed thermal cycle testing at the transmitter assembly level.	Analysis verified an open emitter bond at the die resulting from thermal stresses induced by incomplete cure of polyimide protective coating, expansion and contraction of the coating during testing, or a combination of the two.
7 B2-71-01, 01A	OPEN Lifted bonds	During engineering developments test, eleven transistors failed.	Analysis showed lifted ball bonds on one or both leads and the presence of gold-aluminum intermetallics ("purple plague") on all failed devices.
8 K9-72-05	OPEN Lifted bonds	Devices showed intermittent opens.	Examination revealed under bonding of the base chip bond, necking of emitter post bond, and intermetallic growth around the emitter bond.

TRANSISTORS

ALERT[1] ITEM NO./ GIDEP NO.	PROBLEM AREA/ Cause	PROBLEM DESCRIPTION	PROBLEM ANALYSIS
9 MSFC-71-14, 14A	OPEN Lifted bonds	Bond failures of small signal transistors using 1-mil diameter aluminum lead wire thermocompression wedge and ultrasonic bonds have been experienced.	Mechanism observed is cracking and separation of the bonded wire at the heel of the bond. Excessive bonding pressure, inadequate strain relief, and distortion of the bond seem to be the primary causes. Failure rate is accelerated by power cycling.
10 MSFC-71-07	OPEN Lifted bonds	During electrical testing of a roll torquer board assembly a discrepancy was traced to a transistor.	Upon decapping an emitter bond was found to be lifted and examination revealed appearance of under-bonding.
11 E9-71-01	OPEN Lifted bonds	During test of uninstalled transistors, three devices failed gate-to-source voltage matching.	Delidding revealed either lifting or insufficient bonding of 1-mil aluminum leads to gold plated posts.
12 JPL 10-27-66, Add 11-15-66	OPEN Bad solder connection	During qualification testing of transistors, two devices showed open collector post to case and 60 were classified as poor workmanship and/or potential failures because of poor construction in the arc of the collector post to case connection.	Part made by drilling hole in case and soldering collector post in place. Poor soldering technique and oxide formation between post and case made the parts unacceptable.
13 MSFC-72-01	OPEN Broken bond	During qualification life test, the temperature control unit of the orbital workshop waste management system failed after approximately 17,000 cycles. Investigation revealed a failed transistor.	Failure analysis revealed that both emitter bonds had horizontal cracks along the full length and width of the bonds. The wires had sheared horizontally at the wire bond interface and had moved away from the bonding pad leaving part of the bonded wires adhering to the pads.
14 D7-A-72-12	OPEN Poor crimp connection	Two failures on upstage GCU due to intermittent operation of transistors.	Intermittent collector termination and intermittent base termination, both failures attributed to poor crimp connections.

TRANSISTORS

ALERT[1] ITEM NO./ GIDEP NO.	PROBLEM AREA/ Cause	PROBLEM DESCRIPTION	PROBLEM ANALYSIS
15 GSFC-69-08	OPEN Separation of metallization from chip	Devices failed to turn-on in board level tests because of open circuits in transistors	Examination of the bonds showed that they failed at the chip-metallization interface. The device manufacturer stated that the fault lay in the metallization system, which had inferior adhesion qualities.
16 MSFC-69-01, 01A	OPEN Separation of metallization from chip	Relay redundancy test of flight control computer showed out of tolerance condition. Problem was isolated to a transistor.	Test of h_{FE} at 200 μA showed intermittency. Tapping the transistor or allowing it to cool restored the device to normal operation. Sectioning of 53 transistors revealed 19 with tab bonding problems due to separation of metallization from chip.
17 G4-69-02, G4-69-03	OPEN Corrosion of metallization	"Delidding" inspection revealed corrosion of bonding pads and lifted bonds.	Microprobe analysis revealed the presence of chlorine. The chlorine, derived from trichloroethylene (TCE) used in cleaning process, combined with water, used in a special cleaning process, forms hydrochloric acid. The acid reacts with the aluminum and is regenerated by additional water. The process continues until the water or aluminum is used up.
18 GSFC-70-08	OPEN Corrosion of metallization	Transistors failed during operation of a data transfer switch.	Erosion of base metallization stripes resulting in electrically open base circuits. This was attributed to chemical attack by moisture.
19 MSC-69-02	OPEN Loose internal heat sink	Excessive noise level noted during vibration testing of antenna electronic box	Slight movement of internal heat sink during vibration caused intermittent condition in collector circuit of transistor.
20 K9-71-19	OPEN Loose internal heat sink	During incoming screening, several defects were noted in a NPN isolated collector transistor.	Eighteen devices become catastrophic failures because the isolating piece of ceramic had lifted from the header during 20 kg acceleration. In addition, X-ray revealed evidence of poor workmanship such as shorts between top of metallized ceramic and case, loose material, bent posts, burrs, and metallization running down the side of the ceramic isolating disk.
21 GSFC-69-01	OPEN Poor glass-to-metal seal	One transistor was found to exhibit a high base-to-emitter resistance during testing of spacecraft	Internal examination showed that all three post leads could be rotated in their seals. In addition, the post bonds showed improper resistance welding techniques

TRANSISTORS

ALERT[1] ITEM NO./ GIDEP NO.	PROBLEM AREA/ Cause	PROBLEM DESCRIPTION	PROBLEM ANALYSIS
22 CJ-68-01	OPEN Open in metallization path	I.F. amplifier failed on four different occasions	Microscopic examination revealed break in metallization path to emitter. Geometry of metallization of one batch of transistors from which failed parts came, differed from geometry of other batch examined.
23 MSFC 10-18-65	SHORT Conductive contamination	Four transistors failed during check-out of instrument unit.	Two transistors failed due to human error. One of the two remaining units was found to contain loose particles of solder. Dynamic X-ray of 35 additional units showed 3 units containing loose particles and 13 containing weld splash.
24 MSC-70-01	SHORT Conductive contamination	Failure of LM VHF transceiver during vibration testing	Metallic particles were found within the package. Due to .0005 inch separation of base-to-emitter metallization, any conductive particle of this size or larger could cause intermittency or catastrophic failure.
25 G3-69-01 Add 9-26-69	SHORT Conductive contamination	Intermittent collector-to-base shorts while testing collector-to-base breakdown voltage and tapping the case	The manufacturer stated that the problem was the result of improperly processed can lids from their vendor.
26 LeRC 10-6-66	SHORT Conductive contamination	One part failed short, collector-to-base at equipment level. Two parts failed intermittent during tap test of parts from stock.	Stretching of TO-5 can with temporary tooling to facilitate inclusion of a thermal slug caused entrapment of metallic particles.
27 MSFC-67-02	SHORT Conductive contamination	Intermittent failures occurred during vibration of memory modules having flat-pak transistors installed	Seven failures caused by particle contamination; three failures caused by drooping (slack) leads.
28 MSC-69-07	SHORT Conductive contamination	Collector-to-base short during low temperature operation	Failure analysis revealed that the cause of failure was a 3-way combination of shallow lead departure angle (result of change to aluminum ultrasonic bonding process), a conductive particle, and a tilted header (a new nailhead header). The conductive particle was the only component which was not part of a new process.

TRANSISTORS

ALERT[1] ITEM NO./ GIDEP NO.	PROBLEM AREA/ Cause	PROBLEM DESCRIPTION	PROBLEM ANALYSIS
29 MSFC-65-03	SHORT Conductive contamination	NPN transistors were shorted	Delidding of cans revealed nickel particles inside four of five transistors. The manufacturer reported that their can cleaning process had been changed and that the old process was at fault.
30 GSFC 8-18-67	SHORT Conductive contamination	Intermittent drain-to-gate shorts during monitored vibration of a MOS FET transistor	Spectrographic analysis of the contamination showed their composition to consist of iron alloy, manganese, nickel, copper, and sodium. The source of the contamination was determined to be the "flat pack" package.
31 K9-72-03	SHORT Conductive contamination	Devices showed intermittent shorts.	Dissection revealed loose extraneous gold wire, loose silicon particles, and metal particles. These caused bridging which resulted in electrical shorts. Much of the contamination did not show up on X-ray.
32 E2-71-01	SHORT Conductive contamination	The Hycon Lunar Topographic Camera experienced a shutter failure while photographing the lunar surface. Failure traced to a low power PNP transistor.	After decapping a piece of foreign material 0.130 inch long and 0.008 inch in diameter was observed laying on the header. This particle was not detected by X-ray.
33 MSFC-71-06	SHORT Conductive contamination	Power transistors built in isolated stud packages allow weld spatter during sealing operation.	Splashes of metal particles caused by the cap welding operation stick on the header or under the isolated pedestal, become loose during vibration tests, and may cause intermittent or permanent shorting of the device.
34 MSC 1-27-65	SHORT (1) Build-up of tolerances between header post and underside of can (2) Excessive slack in internal wires	Shorts to the case (1) or chip (2) (collector) by the emitter and/or base internal posts (1) and/or wires (2)	Package (TO-46, TO-47, TO-51) tolerances from one transistor supplier allow emitter and/or base post on header to short to underside of can. The second supplier's parts failed due to excessive slack in internal leads.
35 MSFC-68-02, 02A	SHORT Tin whisker	Tin whisker shorted the case to the transistor element	A tin whisker had grown from the tin plated copper alloy case to the germanium alloy transistor chip.
36 J5-70-04, 04A	ELECTRICAL PARAMETER DEVIATION Channeling	Abnormally high failure rate during high temperature reverse bias testing.	High reject rate due to lack of channel stop protection

TRANSISTORS

ALERT[1] ITEM NO./ GIDEP NO.	PROBLEM AREA/ Cause	PROBLEM DESCRIPTION	PROBLEM ANALYSIS
37 J5-69-02	ELECTRICAL PARAMETER DEVIATION Channeling	Fourteen of seventeen lots had high post burn-in reject rates.	High rejection rate attributed to lack of channel stop protection.
38 MSC-68-06	ELECTRICAL PARAMETER DEVIATION Channeling	System failure during acceptance testing was caused by (I_{CEO}) electrical leakage in excess of one milliampere.	Failure analysis showed the failure to be the result of a channeling defect. The manufacturer stated that high failure rates had been experienced with this lot of transistors.
39 ARC-70-01, 01A	ELECTRICAL PARAMETER DEVIATION Channeling	20 to 70% of JANTX2N930 and JANTX2N2920 transistors subjected to HTRB testing had substantial degradation in h_{FE} and increase in I_{CBO}.	High reject rate as a result of HTRB testing was due to a lack of channel stop protection.
40 K9-71-15	ELECTRICAL PARAMETER DEVIATION Channeling	A large number of subsystem failures involving transistors having high collector to base leakage.	Cause of failure is surface inversion. A metallized guard ring has been incorporated for this device family.
41 LeRC 12-1-65	ELECTRICAL PARAMETER DEVIATION Moisture in package (dew point problem)	I_{CBO} failures under low temperature reverse bias operation.	Moisture was entrapped in the packages during the final seal operation causing a dew point problem.
42 MSFC-66-01	ELECTRICAL PARAMETER DEVIATION Moisture in package (dew point problem)	Mesa type transistors exhibited high collector to base leakage at low temperatures (≈ -35°F)	Analysis showed that suspect parts had excessive moisture in the can which condensed at low temperatures. This condensation formed across the exposed collector base junction of the mesa constructed chips causing excessive collector base leakage.
43 JPL 3-23-66	ELECTRICAL PARAMETER DEVIATION Partial bond	During an evaluation/ qualification test, some of the parts exhibited high V_{BE}(sat) and V_{CE}(sat) of from 5 to 7 volts.	Exposure to high temperature storage at greater than 150°C caused partial bond separation within the gold metallization.

TRANSISTORS

ALERT[1] ITEM NO./ GIDEP NO.	PROBLEM AREA/ Cause	PROBLEM DESCRIPTION	PROBLEM ANALYSIS
44 H1-A-72-08	ELECTRICAL PARAMETER DEVIATION Cracked chip	During post storage check-out of a Saturn instrument unit, three coolant pump failures occurred which were determined to have been caused by excessive leakage current.	Failure analysis of 10 devices disclosed cracked dies, exposed junctions, and lifted metallization. The devices were mesa construction with varnish passivation.
45 WS-68-01	ELECTRICAL PARAMETER DEVIATION Defective hermetic seal	Transistors in TO-70 package failed at equipment level.	Moisture found inside package due to defective hermetic seals. TO-70 package has poor history due to seal problems. Part supplier has discontinued the use of this package.
46 L9-70-02	ELECTRICAL PARAMETER DEVIATION Secondary breakdown	Device was unable to meet data sheet requirements when tested with an automatic tester	Base emitter junctions were overstressed when measuring BV_{CEO} due to the line capacitance of the test setup and secondary breakdown characteristics of the transistor. Specification was changed to read breakdown voltage or test current whichever is reached first.
47 K4-70-01	ELECTRICAL PARAMETER DEVIATION Cracked glass	Degradation of performance subsequent to simulation of high voltage arcing condition at equipment level.	Analysis showed cracks entering through header glass, offset emitter lead attachment, and chip damage. Actual cause of failure not conclusively determined to be any of the aforementioned defects.
48 MSC-10-26-64	ELECTRICAL PARAMETER DEVIATION Contamination	Loss of hermeticity	Use of diagonals or nonshearing devices to remove index tab from the package may cause damage to can-to-header weld. Transistor eventually fails from contamination.
49 GSFC-71-03, 03A	ELECTRICAL PARAMETER DEVIATION Contamination	Transistors purchased as commercial parts exhibited extremely unstable condition in beta.	Manufacturer developed new process involving extra clean wafer fabrication techniques and the use of a silicon nitride passivation layer being placed over the planar passivation surface. A glassivation surface is then placed over the silicon nitride to protect from mechanical damage.
50 JS-68-02	MECHANICAL ANOMALY Contamination	Uneven solder flow, pin holes and bare spots on transistor leads.	Analysis was not performed, as vendor stated that government QAR representative had witnessed and approved lot tests.

TRANSISTORS

ALERT[1] ITEM NO./ GIDEP NO.	PROBLEM AREA/ Cause	PROBLEM DESCRIPTION	PROBLEM ANALYSIS
51 E9-68-01	MECHANICAL ANOMALY Notched leads	Leads cracked or broke off during installation and/or system high level random vibration qualification test.	Header etching process, used by the header manufacturer to remove oxide from the Kovar portions, caused notching of leads.
52 GSFC 5-11-67	MECHANICAL ANOMALY Corrosion and embrittlement	Lead of transistor broke off during assembly in equipment.	Examination of 642 transistors revealed 49 badly corroded units and 156 others showing corrosion. Parts manufacturer stated that the pre-plating change cycle had been too short.
53 ARC-72-02	MECHANICAL ANOMALY Cracked packages	Six quad transistors were found to have cracks in the ceramic at point of lead entrance into package.	It was determined that packages were breaking during a combination clinch/lead-cut operation.

NOTE:
1. Where no ALERT number (GIDEP) exists, the originator and date are shown.

APPENDIX A

This foldout is required to be used with Figures 16-3 (p 16-17, 16-18), 16-4 (p 16-19, 16-20), 16-5 (p 16-22, 16-23), 16-7 (p 16-28, 16-29), and 16-8 (p 16-31, 16-32).

PROBLEM CODES AND DEFINITIONS		
PROBLEM CODE		DEFINITIONS
AREA	CAUSE	
I		OPEN
	A	Inadequate Bonds
	1	Lifted bond
	2	Misplaced bond
	3	Excessive crimp
	4	Displaced "S" bend ribbon
	5	Inadequate bonding material
	B	Chip Associated Discontinuities
	1	Chip lifted
	2	Excessive voids in chip bonding material
	3	Cracked chip
II		SHORT
	A	Conductive Contamination (internal)
	1	Loose solder balls
	2	Loose chips of silicon
	3	Loose pieces of weld splash
	B	Lack of Hermetic Seal
	C	Conductive Contamination (external)
	D	Chip Associated Shorts
	1	Cracks in chip
	2	Metallization defects (bridging)
	3	Oxide faults (pinholes under metallization)
	4	Diffusion anomalies (spikes)
	5	Excessive chip bonding material build-up
III		ELECTRICAL PARAMETER DEVIATION
	A	High Electrical Leakage
	1	Contamination (external)
	2	Contamination (internal)
	3	Loss of hermetic seal
	4	Cracks or flaws in chip
	5	Oxide faults
	6	Diffusion defects (spikes, etc.)
	7	Improper alloying (irregularities)
	B	High Forward Voltage Drop
	1	Contact problems (bonds)
	2	Cracks or flaws in chip
	3	Voids between chip and header
	4	Metallization irregularities
	5	Diffusion anomalies
IV		MECHANICAL ANOMALY
	A	Lead Anomaly
	1	Poor plating (peeling, corroded, cracked, etc.)
	2	Damaged leads (nicks, cuts, scrapes, etc.)
	3	Defective welds
	4	Improper material
	5	Misalignment
	B	Case Anomaly
	1	Improper dimensions
	2	Cracked (nonhermetic)
	3	Defective case to lead seals
	4	Improper marking (polarity, p/n, etc.)
	5	Defective case paint (peels, lifts, blisters, etc.)

Figure 16-9. Problem Codes and Definitions

This foldout is required to be used with Figures 16-3 (p 16-17, 16-18), 16-4 (p 16-19, 16-20), 16-5 (p 16-22, 16-23), 16-7 (p 16-28, 16-29), and 16-8 (p 16-31, 16-32).

PROBLEM CODES AND DEFINITIONS		
PROBLEM CODE		DEFINITIONS
AREA	CAUSE	
I		OPEN
	A	Inadequate Bonds
	1	Lifted bond
	2	Misplaced bond
	3	Excessive crimp
	4	Displaced "S" bend ribbon
	5	Inadequate bonding material
	B	Chip Associated Discontinuities
	1	Chip lifted
	2	Excessive voids in chip bonding material
	3	Cracked chip
II		SHORT
	A	Conductive Contamination (internal)
	1	Loose solder balls
	2	Loose chips of silicon
	3	Loose pieces of weld splash
	B	Lack of Hermetic Seal
	C	Conductive Contamination (external)
	D	Chip Associated Shorts
	1	Cracks in chip
	2	Metallization defects (bridging)
	3	Oxide faults (pinholes under metallization)
	4	Diffusion anomalies (spikes)
	5	Excessive chip bonding material build-up
III		ELECTRICAL PARAMETER DEVIATION
	A	High Electrical Leakage
	1	Contamination (external)
	2	Contamination (internal)
	3	Loss of hermetic seal
	4	Cracks or flaws in chip
	5	Oxide faults
	6	Diffusion defects (spikes, etc.)
	7	Improper alloying (irregularities)
	B	High Forward Voltage Drop
	1	Contact problems (bonds)
	2	Cracks or flaws in chip
	3	Voids between chip and header
	4	Metallization irregularities
	5	Diffusion anomalies
IV		MECHANICAL ANOMALY
	A	Lead Anomaly
	1	Poor plating (peeling, corroded, cracked, etc.)
	2	Damaged leads (nicks, cuts, scrapes, etc.)
	3	Defective welds
	4	Improper material
	5	Misalignment
	B	Case Anomaly
	1	Improper dimensions
	2	Cracked (nonhermetic)
	3	Defective case to lead seals
	4	Improper marking (polarity, p/n, etc.)
	5	Defective case paint (peels, lifts, blisters, etc.)

Figure 16-9. Problem Codes and Definitions

This foldout table is required to be used with Figures 17-2 (p 17-21, 17-22), 17-4 (p 17-27, 17-28), 17-6 (p 17-34), and 17-7 (p 17-36).

PROBLEM CODES AND DEFINITIONS		
PROBLEM CODE		
AREA	CAUSE	DEFINITION
I		OPEN
	A	Die Metallization
	1	Microcracks at window cutouts
	2	Scratches across metallization stripes or pads
	3	Voids
	4	Incorrect/insufficient alloying
	5	Formation of insulating layer under metallization at cutouts due to faulty oxide removal
	6	Peeling, lifting, or flaking metal
	7	Mask misalignment
	8	Masking defect
	9	Corrosion
	B	Wiring/Bonding
	1	Lifted bond
	2	Cracked bond wire at heel of bond
	3	Broken bond wire, or nicked or necked-down wire
	4	Corroded wire
	5	Misbond - insufficient pressure or temperature/ excessive pressure or temperature
	6	Missing bonds or jumpers
	7	Plague (intermetallics)
	8	Incorrect bond sizes
	9	Misplaced bonds
	C	Chip or Substrate
	1	Cracked chip or substrate
	2	Lifted chip or substrate
	3	Lifted molytab(s)
	4	Diffusion defect: bad mask, contamination, incorrect, etc.
	5	Thin film defect: contact, scratch, omissions, lifting, peeling, voids, and corrosion
	6	Thick film defects: design error, silk screening, scratches, voids, omissions, contacts, and contamination
	7	Oxide defects

Figure 17-8. Problem Codes and Definitions

This foldout table is required to be used with Figures 17-2 (p 17-21, 17-22), 17-4 (p 17-27, 17-28), 17-6 (p 17-34), and 17-7 (p 17-36).

PROBLEM CODES AND DEFINITIONS		
PROBLEM CODE		
AREA	CAUSE	DEFINITION
II		SHORT
	A	Chip
	1	Smeared metallization
	2	Unetched metallization
	3	Lack of/or too thin oxide insulation
	4	Pinholes
	5	Mask(s) misalignment: diffusion masks, metallization masks overlapping
	6	Diffusion shorts due to faulty masks
	7	Particulate contamination embedded during diffusion
	8	Chemical contamination as result of faulty cleaning, rinsing, etc.
	9	Metallic or conductive particle short due to extraneous material
	10	Metallization pads placed too close to chip edge
	11	Chip edge chipouts exposing bare silicon to metallization scribing
	12	Excess flow of eutectic during die attach
	13	Short due to moisture or faulty hermetic seal - contamination
	14	Junction punch-through overstress
	B	Wiring
	1	Leads too long
	2	Lead dressing - too close to chip edge or adjacent chip or wire, or crossed over
	3	Sagging leads
	4	Leads in contact with package lid
	5	Bond tails too long
	6	Improper bond sizes causing adjacent shorts
	7	Improperly terminated leads
	8	Extraneous and or loose wires or bonds
	C	Substrates
	1	Smeared or scratched thin or thick film depositions
	2	Improperly deposited metallization patterns, e.g., misalignments
	3	Conductive contamination from inks or chemicals
	4	Shorts due to bonding agents, whether eutectic or conductive epoxies
	5	Extraneous interconnect wires or ribbons
	6	Misplaced bonds
	7	Extraneous particulate matter - bond melt, lid solder melt, or silicon chipouts, wire slivers or contamination

Figure 17-8. Problem Codes and Definitions

This foldout table is required to be used with Figures 17-2 (p 17-21, 17-22), 17-4 (p 17-27, 17-28), 17-6 (p 17-34), and 17-7 (p 17-36).

PROBLEM CODES AND DEFINITIONS		
PROBLEM CODE		
AREA	CAUSE	DEFINITION
II (Cont)	D	Package
	1	Eutectic lid solder melt in contact with package leads
	2	Package lead misaligned in package causing package to lead short
	3	Loss of hermetic seal
	4	Short due to external contamination
III		OPERATIONAL DEGRADATION
	A	Surface Inversion N to P or Vice Versa
	B	Surface Channeling
	C	High Leakage
	D	Loss of Beta
	E	Oversensitivity to Voltage Variation
	F	Oversensitivity to Temperature Variation
	G	Die Misorientation
	H	Design Change
	I	Design Deficiency
	J	Sequence of Power Application
	K	Misapplication of Device
	L	Electrostatic Discharge in MOS Devices
IV		MECHANICAL ANOMALY
	A	Marking or Identification (Misidentification or Illegibility)
	B	Mislocation of Index Mark/Tab
	C	Damage to Package
	D	Damage to Package Leads or Lead to Package Seals
	E	Loss of Hermeticity
	F	X-ray Anomalies
	G	Incorrect Package
	H	Missing Leads
	I	Dimensional Errors

Figure 17-8. Problem Codes and Definitions

This foldout table is required to be used with Figures 18-2 (p 18-18), 18-3 (p 18-20, 18-21), 18-5 (p 18-26, 18-27), 18-6 (p 18-29, 18-30), 18-8 (p 18-35, 18-36), and 18-9 (p 18-38, 18-39).

PROBLEM CODES AND DEFINITIONS

PROBLEM CODE		
AREA	CAUSE	DEFINITION
I		OPEN
	A	Inadequate Bonds
	1	Lifted and broken bonds
	2	Misplaced bond
	3	Poor crimp
	4	Loose heat sink
	5	Inadequate bonding material
	B	Chip Associated Discontinuities
	1	Lifted chip
	2	Excessive voids in chip bonding material
	3	Cracked chip
	4	Separation of metallization from chip
	5	Corrosion of metallization
	6	Open in metallization path
	C	Defective Hermetic Seal
II		SHORT
	A	Conductive Contamination (Internal)
	1	Loose solder balls
	2	Loose package material
	B	Drooping Leads
	C	Defective Hermetic Seal
	D	Conductive Contamination (External)
	E	Chip Associated Shorts
	1	Cracked chip
	2	Metallization defects (bridging)
	3	Oxide faults (pinholes under metallization)
	4	Diffusion anomalies (spikes)
	5	Excessive chip bonding material build-up
III		ELECTRICAL PARAMETER DEVIATION
	A	High Electrical Leakage
	1	Channeling
	2	Dew point problem (moisture in package)
	3	Contamination (external)
	4	Contamination (internal)
	5	Defective hermetic seal
	6	Secondary breakdown
	7	Cracks or flaws in chip
	8	Oxide faults
	9	Diffusion defects (spikes, pipes, etc.)
	10	Improper alloying (irregularities)
	11	Wandering threshold
	B	High Voltage Drop
	1	Bond problems
	2	Cracks or flaws in chip
	3	Voids between chip and header
	4	Metallization irregularities
	5	Diffusion anomalies
IV		MECHANICAL ANOMALY
	A	Lead Anomaly
	1	Poor plating (peeling, corroded, cracked, etc.)
	2	Damaged leads (nicks, cuts, scrapes, etc.)
	3	Defective welds
	4	Improper material
	5	Misalignment
	B	Case Anomaly
	1	Improper dimensions
	2	Cracked (nonhermetic)
	3	Defective case to lead seals
	4	Improper marking (part number, type, etc.)
	5	Defective marking paint (peels, lifts, blisters, etc.)

Figure 18-10. Problem Codes and Definitions

APPENDIX B
INTERCONNECTING OF HYBRID MICROELECTRONIC ASSEMBLIES AND DEVICES

B

CONTENTS

INTERCONNECTING OF HYBRID MICROELECTRONIC ASSEMBLIES AND DEVICES

INTRODUCTION

CONDUCTIVE FILMS

Conductive films of both Au (gold) and Al (aluminum) are vacuum deposited onto suitable substrate materials to form circuit interconnection paths, and when so deposited are identified as thin films. In addition, conductive films of gold, silver, platinum-gold, palladium-gold, and other materials are screen printed and fired onto suitable substrate materials. Such films are identified as thick films. Substrate material is usually aluminum oxide, Al_2O_3.

Hybrid Microcircuits. In hybrid microcircuits such films provide the major current paths between discrete devices, active and passive elements, and other functional devices that make up the complete hybrid. To complete the circuit it is necessary to add fine wires between the terminal areas of the devices and the deposited circuit traces. It may also be necessary to add wiring between the internal package terminal areas and the deposited terminal areas on the circuit or dev..es.

Beam Lead and Flip Chip Devices. Exceptions to these requirements are beam lead and flip chip devices. Such devices do not require the addition of wires, as the deposited circuit traces are designed to terminate at the bonding interface of the beam leads or flip chip bumps.

BOND RELIABILITY

Gold Thermal-Compression Ball Bonding. Gold thermal-compression ball bonding was the first method used in the semiconductor and hybrid industry to provide the interconnects mentioned above. However, severe bond failures often occurred since all of the semiconductor devices employed aluminum metallization. The heat required during thermal-compression bonding initiated the formation of aluminum-silicon-gold intermetallics in the bonded interface, known as "purple plague". Various solutions are available today to eliminate this problem, including moly-gold metallization and the use of a silicon nitride layer beneath the aluminum.

Aluminum and Gold Ultrasonic Bonding. Both aluminum and gold ultrasonic bonding equipment have been developed which produce no significant heat during the scrubbing process, and hence no danger of purple plague, at least from the bonding process. It should be mentioned, however, that purple plague can, and has been known to, exist even with the use of ultrasonic bonding of aluminum-silicon-gold systems. This is the result of heat subsequent to bonding, usually resulting from package sealing or lead soldering. For this reason a monometallic system is very desirable. Since wire bonds are usually the weakest link in a microelectronic circuit, continuing research to eliminate the wire interconnects led to the development of beam lead and flip chip devices.

Beam Lead and Flip Chip Devices. Beam lead devices are produced by vacuum deposition of gold, followed by heavy electroplating of gold. Selective back etching of the wafer produces individual dice with the gold beams extending beyond the silicon. Various flip chip configurations have been used employing vacuum deposition, plating, soldering, etc. The inherent problem with flip chip technology, with respect to hybrids, results from the considerably different coefficient of thermal expansion of silicon and the alumina substrate. Temperature cycling causes failures at the bond interface. There is also the problem of visual inspection of the bond, which is not possible. Beam lead devices do not suffer from either of these problems, since the gold beams are relatively long and compliant and can be visually inspected at the bond inte face.

These beam lead devices are becoming more readily available, but the system engineer would be hard pressed, currently, to design a complex system with off-the-shelf devices. The problem is economic rather than technical, at least for the bipolar devices. Some current MOS devices might require redesign to avoid degradation or damage during beam lead processing. It is safe to predict more widespread use of beam lead devices, especially for military and space applications, where reliability is more important than initial cost. Studies show that at least an order of magnitude increase in reliability should be experienced by use of beam lead technology.

Studies further show that complex hybrids, employing six or more beam lead devices, should actually be more cost effective than conventional chip and wire technology due to increased yield and opportunity for rework. A defective beam lead device may be removed and replaced without substrate metallization damage.

DIE BONDING

EUTECTIC DIE BONDING

General Considerations

Eutectic die bonding is a means of physically attaching active and passive devices to a thick or thin film circuit. These bonds physically fix the elements to the using circuit and provide for both thermal and electrical conduction, remaining firm up to the eutectic temperature of the alloy used.

Workstage. Basic to this bonding method is a heated workstage. The heat applied to this workstage is thermostatically regulated to close tolerances. In addition, the workstage must be tooled to firmly hold the carrier, substrate, or package onto which the dies are to be eutectically bonded. This holding action usually is accomplished by means of a vacuum hole of appropriate size in the workstage through which a vacuum is drawn. The carrier, substrate, or package is placed over this hole in the heated workstage and properly positioned and oriented to receive the die, and the vacuum is turned on. The effectiveness of such a means of holding the work solidly depends on smooth, flat, parallel mating surfaces between the workstage and the substrate or package. Rough, dirty, or uneven contacting surfaces will not permit the vacuum to hold the base to which the dies are to be bonded.

Clamping. Mechanical clamping of the work is another means of tooling that has been employed to hold the base to which the devices are to be eutectically bonded. However, such a device is of little or no use when the base for the devices is less than one half inch square. Overlapping clamp jaws can interfere with die bonding, particularly at or near the edge of the circuit carrying base. Such a situation makes necessary the use of vacuum holding workstages.

Oxide Inhibition. In addition, a flow of dry nitrogen gas onto the device during eutectic bonding is required to prevent severe oxide formation. Such oxides inhibit the die bonds, rendering them weak and electrically inferior.

Usage. Eutectic bonding is generally used because strong, high temperature bonds are formed through an alloying between the gold metallization on the carrier and the silicon of which most dies are composed. Many manufacturers provide a gold backing on their devices to assist in forming this bond. Ultraclean silicon will alloy with thin or thick film gold without the need of this gold backing; however, the addition of the gold film to the back of the die assures the user of a contaminant free silicon surface. Gold alloys well with tin, germanium, or silicon. These three materials are used as preforms to assist in the eutectic die bonding and package sealing process. Table B-1 provides data on these materials. Die bonding to thick or thin film gold does not necessarily require a preform if the die is provided with an ample gold backing.

TABLE B-1
GOLD-BASED EUTECTIC ALLOYS

Alloy	Ratio	Trace Dopant[1] and Properties	Temperature(°C)	
			Liquid	Solid
Gold-Tin	80 Au/20 Sn	This alloy is not normally doped. Used for lid seals	280	280
Gold-Germanium	88 Au/12 Ge	Boron — P Antimony — N	356	356
Gold-Silicon	94 Au/6 Si	Boron — P Antimony — N	370	370

NOTE: 1. Although not normally needed, dopants may be added to preform alloys to enhance the electrical polarity properties of the collector interface with substrate circuitry. Dopant polarity must be the same as collector polarity. Gold is basically neutral and can be used in both N and P doping situations.

Temperature Requirements. In order to establish a good electrical/mechanical bond between the die and the bonding pad, the temperature of the interface between the bottom of the die and the top of the die bonding pad area must be raised from 20 to 50°C above the melting point of the gold alloys in this interface. This additional temperature requirement above the melting point of the eutectic gold alloy is necessary because of the heat sinking characteristics of the carrier, substrate, and die. The nitrogen gas flowing over the whole bond area causes more loss of heat. Thus, in reality, devices that are to be eutectically bonded will experience temperatures up to 420°C, or perhaps even higher depending on the size of the substrate and the number of devices to be mounted. If many dies are to be eutectically bonded to the same substrate or carrier, extended time at temperature may be detrimental to the devices to the point of undesirable parametric changes.

Silicon Bleed-Out. Yet another problem can arise when multiple dies are to be eutectically bonded to thin or thick film circuits. This is silicon bleed-out onto the gold film. After the initial eutectic alloying between the die and the gold film, the gold continues to draw the silicon from the die as long as it is exposed to the eutectic bonding temperatures. If left on the heated workstage long enough the silicon alloys with all the gold it contacts. This creates wire bonding problems with aluminum wires, and also limits the amount of die replacement, or rework, that can be performed on those bonding pad areas.

Eutectic Machine Die Bonding

One die bonding method that may help to relieve the parametric change problems previously mentioned is to use machine die bonders equipped with thermostatically controlled, heated die collets. Such collets permit workstage temperature reduction to a point of minimal thermal effects on the devices, while still providing suitable bonding heat to the bond interface. Also, thermal shock to the device is reduced by using heated die collets.

Die Collet. The die collet is provided with a center vacuum hole to pick up and hold the die until pressure contact with the substrate occurs. (If a preform is employed, it may be placed on the bonding area prior to die attach using a vacuum pickup tool or tweezers). Once a predetermined pressure is reached, the die collet vacuum is cut off and the die is mechanically scrubbed into the bonding pad under controlled pressure and controlled time interval. After the scrub time, the die collet automatically returns above the work area ready for the next die pickup.

Spot Heating. Spot heating is employed by at least one manufacturer of die bonders in addition to heated die collets. Focused infrared energy heats the substrate or package from the bottom in the area where the die is to be attached. This technique allows dies already attached to remain at a much lower temperature than would be the case if a conventional heated stage was employed.

Other Techniques. Other techniques employed to reduce the high temperature exposure time include semiautomatic die pickup and multiple rotating collets to accomodate different die sizes on the same circuit. It should be mentioned that manufacturers of nonhybrid circuits do not encounter the same problems of high temperature exposure, since generally only one device is being attached to the header. While many MOS devices are sensitive to die attach temperatures, most modern silicon bipolar devices are not degraded by exposure to one die attach cycle, even without heated collets.

Advantages. Advantages of eutectic machine die bonding are:

1. Automatic vacuum die pickup prevents loss of die through mishandling.
2. Preheated die collets reduce thermal shock to sensitive devices.
3. Heat, pressure, and scrub times are programmable.
4. Mechanical die pickup and placement eliminates operator burns on exposed heat column.

Disadvantages. Disadvantages of eutectic machine die bonding are:

1. Equipment is very expensive.
2. The technique requires vacuum die collet tips for each different size of die or device. Several spare die collets are required for each size of die since they oxidize very quickly creating pickup problems. Oxide chips from tips may also flake off thereby creating a never ending precap inspection problem.

3. Development work is required to determine optimum heat, pressure, and scrub time schedules for each device size.

4. Machine bonding requires square cut dies to prevent chipping and cracking of dies by the die collets. Dies must be nearly perfect for machine die bonding. Uneven edges and nonsquare corners may result in improperly placed or poorly bonded dies requiring replacement. Such replacement could result in all work to that point being scrapped if the bonding pad metallization is damaged or removed when the die comes off.

5. Preforms, when used, must be placed on the bonding pad manually.

Eutectic Manual Die Bonding

A second method of die bonding in common use is the tweezer bond. In this method the die is picked up by the edges, using tweezers, and manually scrubbed into the die bonding pad. This, of course, is done on a preheated substrate and requires excellent manual dexterity and care on the part of the operator. The scrubbing action under light pressure causes the alloyed gold to flow, and a shiny, dark appearance around the base periphery of the die tells the operator that eutectic flow is occurring. Pressure on the tweezers is carefully relaxed and the device and its carrier circuit are then removed to cool and to await the next assembly operation.

Advantages. Advantages of eutectic tweezer die bonding are:

1. Equipment is low in cost.

2. An imperfectly broken die may be used, if otherwise acceptable.

3. A well trained operator may actually exceed the die attach rate of all but the most rapid machines.

Disadvantages. Disadvantages of eutectic tweezer die bonding are:

1. This method requires great patience and care on the part of the operator.

2. The heated workstage is a constant burn hazard for the operator's hands.

3. The devices must be exposed to higher temperatures since all of the heat is being supplied from the workstage.

EPOXY DIE BONDING

Epoxy die bonding is a means of adhesively attaching semiconductor and passive devices to a thin or thick film conductor through the use of soft, thixotropic pastes. Such adhesive bonds physically fix component circuit elements to the using circuit or carrier when they are properly mixed and cured. Selective use of these epoxies provides either thermal or electrical conduction, or both if required. However, these bonds will not survive continuous service above 275°C, and 125°C appears to be the maximum temperature for some of these epoxies. Table B-2 lists the important characteristics of such epoxies, both conductive and nonconductive.

TABLE B-2

BONDING EPOXIES - DIE AND SUBSTRATE

Name	Volume Resistivity (cm^{-1})	Operating Temp (°C)	Cure Data	Forms	Use[1]	Conductor
DAG-413	0.001	200	10 min @ 260°C	Paste	IC, C, R, substrate	Yes
Epotek H-20	0.0003	125	20 min @ 120°C	Paste	IC, C, R, substrate	Yes
Uniset-409	0.009	150	10 min @ 160°C	Paste	IC, C, R, substrate	Yes
Eccobond 58-C	0.0001	200	8 hr @ 125°C	Paste	IC, C, R, substrate	Yes
Monobond-Conducting	0.001	175	30 min @ 95°C	Paste	IC, C, R, substrate	Yes
Ohmex-AG	0.0001	275	15 hr @ 160°C	Paste	IC, C, R, substrate	Yes
Eccobond 24	10^{14}	250	8 hr @ room temp	Clear epoxy	IC, & S/S only	No
Allabond-Clear	10^{16}	200	4 hr @ room temp	Clear epoxy	IC, & S/S only	No

NOTE: 1. IC — integrated circuit; C — capacitor; R — resistors; S/S — substrate

Usage. The use of epoxy for die and substrate bonding is gaining favor in many of the industries fabricating and assembling microelectronic devices. Its use has been recognized by NASA in document MSFC-85MD3926, Design and Quality Standards for Custom Hybrid Microcircuits, dated November 13, 1972. MSFC is currently conducting an evaluation of the use of conductive epoxies in high reliability hybrid microcircuits.

Advantages. A review of the applicability of epoxies for die and substrate bonding shows the following advantages:

1. Epoxies are easy to use and rework.
2. A minimum of operator training time is required.
3. Units can be wire bonded for electrical check-out after a short, partial cure. This feature allows quick, nondestructive replacement in completed hybrid assemblies of defective devices. This is ordinarily not possible with eutectically bonded devices.
4. Damage to original film surfaces is minimal, even during rework.
5. Machines are available to pick up die and automatically dispense epoxy.

6. Epoxy impregnated fiberglas preforms are available for a variety of applications, including substrate attach and package sealing.

7. Cure temperature is much lower than eutectic attach temperature.

Disadvantages. Disadvantages of epoxy die bonding are:

1. Maximum operating temperature is currently limited to about 275°C, although some newer systems may operate above this temperature. Note from Table B-2 that some epoxies are limited to only 125°C.

2. Incomplete curing may occur under the centers of large devices (about 0.120 by 0.120 inch) and large substrates (0.250 by 0.250 inch and larger). This factor can cause device-substrate or substrate-package separation under high vacuum conditions due to outgassing of the uncured epoxy. Use of a vacuum oven during the cure cycle should reduce or eliminate this problem.

WIRE BONDING

GENERAL

Wire bonding is a process in which wires are added to a hybrid microcircuit assembly to complete the current carrying paths. These wires must be added to most semiconductor devices as well as many types of packages.

THERMAL-COMPRESSION BONDING

Ball Formation. Thermal-compression (TC) bonding uses pure gold wire to effect the interconnections. The gold wire is fed downward from its spindle mounted spool through a tube leading into a vertically mounted capillary bonding tool. A ball is then formed on the end of the wire extending below the end of the capillary by passing a controlled hydrogen flame across the gold wire.

Bond Formations. After a gold ball is formed, the first bond site is manipulated to a point directly under the tip and ball. The gold wire is floating loosely in the capillary bonding tip and, as the tip is lowered to the first bond site, the wire retracts into the tip until the ball contacts the bonding face of the tip. Both the ball and wire are now lowered onto the bonding site. Continued downward motion applies a preset pressure to the gold ball, deforming it and forming a diffusion type bond.

After the first bond is formed, and after a preset period of time, the bonding tool is raised with the wire continuing to feed freely through the bonding tool. The tip rises directly above the first bond site and, due to the shape of the end of the bonding tool, the wire can be fed out in any direction to approach the second bonding site. Experience suggests that generous loops will provide the best wire strengths. The wire should not be strained by stretching it tight when feeding out wire during travel to the second bond area. After the bonding tool is positioned over the second bond site with properly looped wire, the capillary is again lowered and the second terminating bond is formed. This second bond is not a ball bond as was the first, but is called a wedge bond because of its shape. The wedge shape facilitates the removal of the wire tail as the gold wire is thin and weak at the narrow, pinched edge of the wedge.

After a preset period of time, the bonding tool is again released and allowed to rise. At this point, the hydrogen flame cuts through the wire forming a new ball for the next bonding cycle.

Temperature Requirements. In most thermal-compression bonding both the workstage and capillary are heated continuously. With conventional bonding machines the workstage temperature ranges from 275°C to 400°C, depending on the assembly mass and bonding pad metal. Pulse bonders are now available which provide a heat pulse to the capillary only during the bonding operation. Many bonding operations may be performed at room temperature, although workstage heaters are provided if needed. Such bonders were developed for extremely heat sensitive devices, as well as for the hybrid industry. The obvious advantage is to greatly reduce the temperature to which all the devices in the hybrid circuit are subjected to during bonding.

Advantages. The advantages of thermal-compression bonding are:

1. Very strong bonds are formed in any direction; the wire usually breaks, rather than the bond.
2. Missed bonds can be replaced on the original bonding site.

Disadvantages. Disadvantages of TC bonding are:

1. The die must be heated to temperatures ranging from 250°C to 400°C for good, strong bonds, unless pulse bonding equipment is available.
2. This method utilizes gold wire which may result in purple plague, as discussed earlier.
3. Bonding pad areas of at least 4 mils square are required for 1 mil wire due to ball size. Also, the ball size increases as it is flattened under the pressure of the bonding tip. It may expand to six times the original wire size.

ULTRASONIC BONDING

General Considerations

Wire interconnections, using ultrasonic equipment, may be performed in two ways. In one, either gold or aluminum wire may be used. Both bonds are wedge bonds, and this method is called ultrasonic wire bonding. In the other, only gold wire may be used. The first bond is a ball bond, and the second is a wedge bond. The second method is known as ultrasonic ball bonding. Before distinguishing between wire bonding and ball bonding, a discussion of the principles of the ultrasonic bonding process will be given.

Since the ultrasonic bond is primarily a surface-diffusion bond, a discussion of metallic surfaces is necessary.

Surface Irregularities. The finest, most carefully polished metal surfaces exhibit irregularities (after all polishing compounds are removed) of between 150 and 250 atomic diameters in peak-to-valley vertical distances. As soon as such a specimen is exposed to the normal atmosphere, reaction with oxygen occurs and oxides of the base metal begin to form. In the case of aluminum, for example, the oxide would be aluminum oxide.

Oxides. These oxides are actually useful in ultrasonic bonding. By bringing together two such surfaces, and using a suitable pressure, the oxides can be made to fracture and expose the underlying metal. Introduction of a scrubbing motion to the wire while pressure is maintained breaks up the oxides, and they act as a scrubbing agent for the underlying base metals. As the oxides are scrubbed away, the base metals come together. The high asperities of the base metals, in scrubbing together under pressure, become flatter and wider, while at the same time the oxides are broken up and dispersed to the edges of the scrubbed area. Due to the surface nature of the base metal some oxides become trapped in the metal valeys. Oxide entrapments are not significant unless they contain corrosive contaminants. Such bonds, in many instances, are stronger than the parent metals and quite often exhibit grain boundary failures under testing. It should be noted that pure gold does not oxidize. Therefore, relatively longer scrub times, at higher power and pressure, are required to break down the oxides it contacts and to form a good bond.

Contaminants. In the normal process of handling semiconductor devices airborne contaminants, such as moisture and oily vapors, are deposited on all surfaces. The human breath carries many corrosive, oily vapors and thus provides a constant source of trouble for very sensitive microcircuits. Hands carry oil soluble saline films that, when in contact with delicate thin films of integrated circuits, are extremely corrosive. Not only are these films corrosive in nature, they also serve as surfaces lubricants and, if not removed, greatly inhibit the ultrasonic scrubbing action previously described. The integrity of such ultrasonic bonds becomes questionable. Other contaminants are photoresist films used at nearly every step in the fabrication of semiconductor devices. Such films must be completely removed to achieve good contact with the metallized surfaces. Residual films of photoresist are often difficult to detect, and the character of these chemicals can change severely if they are not properly stored and used.

Cleaning. To achieve a reliable ultrasonic bond, the cleaning and handling processes for all materials used in the semiconductor fabrication process must be well documented and followed precisely. Prior to bonding, the assembly must be cleaned to remove any airborne or operator induced contaminants. Cleaning should take place within two to three hours of the time the device is to be wire bonded. Bonding wire and the tools it contacts should be cleaned with Freon type solvents before being installed on the bonder. Once the metals to be joined are cleaned, good metallurgical bonds are produced.

Ultrasonic Wire Bonding

Equipment. The component assemblies of equipment are essentially the same as those used for ultrasonic ball bonding. The heart of either system is the power supply and matched frequency transducer-coupler assembly. Major differences are the bonding tools, method of applying pressure to the bonding tip, and the termination method.

Tooling. The bonding tool itself, and its configuration, are the aspects of tooling of most concern. The ultrasonic bonding tool has seen a transition from a simple wedge type to a very complex bonding tip. Several finishes on the face of the tip that contacts the wire are available, including flat, grooved, and concave.

If all contacting surfaces are parallel, the simple flat face would be ideal. Unfortunately, contact surface parallelism is unusual in thick or thin films due to the substrate. On uneven, nonlevel surfaces, the flat faced tip permits the wire to slide sideways, and sometimes completely out from under it, during ultrasonic scrubbing. When this occurs, the mass of wire under the tip changes resulting in substandard bonds. For this reason the flat faced tip is not recommended.

The grooved tool has a one-half mil groove transverse to the centerline axis of the wire. On a 1 mil wire the groove rolls a one-half mil wave of metal to and fro as the tool vibrates ultrasonically. This can create intergranular stresses leading to lower than average bond strength. Because of this, experience has shown this type of tool to be undesirable with wire of less than 2 mil diameter.

The concave tool has a shallow groove parallel to the centerline axis of the wire, usually 0.3 mils deep with a radius of 12 mils. This groove assists in keeping the wire centered under the tip which is especially useful when bonding to rough, uneven surfaces such as those found in thick films. It also helps to contain the sideward spread of the wire during the bonding process. Another feature of this type of tip face is that it produces more consistently uniform wire bonds than either the transverse grooved or flat faced tip. This concavity also tends to relieve the sharp (less than 0.0003 inch) radius of the tip heel where most wire breaks occur. Experience has shown this type of tip to be desirable for use with wire of 0.7 to 1.8 mil diameter.

Important considerations in selecting the appropriate ultrasonic bonding tip are:

1. Wire size and type.
2. Bond area available.
3. Bond size desired.
4. Bond strength required.

Taking these items in order, the wire size and type usually are dictated by the current carrying requirements that the interconnect wire is to meet. For example, a 1 mil wire of 99.99 percent gold will burn out at about 0.750A; a 1 mil wire of 99.99 percent aluminum will burn out at about 0.38A; and a 1 mil wire of 1 percent silicon-aluminum alloy will burn out at about 0.48A. (See Figures B-1, B-2, and B-3.) Obviously, the wire size and material will be determined by design engineering. A conservative maximum current would be one quarter of the burn out value.

Bond area is determined either from manufacturer data or from optical measurements. This area is the over-all size of the bonding pad or pads on semiconductors and circuit films. Those bond areas vary quite widely from device to device and from manufacturer to manufacturer. Bonding pads may be as small as 2 mils square requiring wire no larger than 1 mil and great care in bond placement.

Bond size is a combination of bond length, bond width, and wire size. For a given wire size, the bond size is largely determined by the size and shape of the bonding tool face. The length of the bond is approximately equal to the face length, but the width depends more on the shape of the face. As discussed previously, the concave face tends to contain the sidewise spread of the wire.

Bond strength required is related to the wire size and the environment the completed circuit will be subjected to. Factors that influence bond strength include alloy, temper, elongation, bonding tip face, surface contamination and surface texture. MIL-STD-883 (ref 34) contains testing methods and minimum bond strength requirements.

Bonding Pressure. Bonding pressure in ultrasonic wire bonding is pressure applied through the use of dead weights, the position of which can be manually varied.

By moving the weight away from the pivot point increasing pressure is applied to the bonding wedge. Moving the weight towards the pivot decreases the pressure on the bonding wedge.

The actual location of the weights, with regard to the pivot point, is determined by the equipment manufacturer. The extra weight afforded by the wire holding and clamping accessories forward of the pivot point also affects the method and location of weight adjustments.

Termination. Termination method in ultrasonic wire bonding involves correctly sequenced wire clamping and clamp movement cycles. The clamp performs two functions:

1. It either opens or closes on the wire to allow it to reel off freely, or to hold it firmly.
2. While closed it remains stationary to hold the wire, or by cam actuation it moves backward to break the wire, then forward to refeed it.

Advantages. The advantages of ultrasonic wire bonding are:

1. No heat is required, nor is appreciable heat generated during bonding.
2. Both aluminum and gold wire may be used. Aluminum is cheaper if the wire will handle the current.
3. Using thin film aluminum substrate metallization it is possible to produce a monometallic interconnect system and eliminate problems associated with intermetallics.

Disadvantages. The disadvantages of ultrasonic wire bonding are:

1. Bond strength is less than obtainable in the gold thermal-compression bonding; the bond will generally fail at the heel rather than breaking the wire. With aluminum wire even less bond strength is obtainable.
2. The current carrying ability of aluminum wire is considerably less than gold.
3. Bonding is permitted only in one direction. The second bond must be directly behind the first bond to properly position the wire under the tip.
4. Clear area in the vicinity of the bonding site must be greater than required for TC bonding since the tool is larger.

Ultrasonic Ball Bonding

Equipment. Equipment used in the ultrasonic ball bonding is essentially the same as that for ultrasonic wire bonding. Differences between the two techniques lie in tooling, pressure application, and termination methods.

Comparison to Thermal-Compression Bonding. Ultrasonic ball bonding is similar to thermal-compression bonding as follows:

1. Both require gold wire.
2. The first bond of each method uses a gold ball.
3. The second bond of each method is a wedge bond.
4. Both methods use a hydrogen flame to aid in the termination process.

The differences are that ultrasonic energy is used to deform and scrub the gold wire into the bonding area for the ultrasonic ball bond process. Thermal energy provided by a heated workstage and heated wire bonding tool is used to deform and press the gold wire into the bonding area for the thermal-compression bonding process. A stream of dry nitrogen gas is directed over the bond area in the thermal-compression process but is not required in the ultrasonic bonding process since the chip remains at essentially room temperature.

This method of interconnection is used:

1. When no heat can be used to attach interconnection wires.
2. When it is physically impossible to gain access to the required bonding area with an ultrasonic wire bonding tip.
3. When otherwise required by detail specifications.

Tooling. As with the thermal-compression wire bonding tip the gold wire feeds through the hollow capillary from a spool mounted above and over the tip. The ultrasonic ball bonding tip is normally manufactured with a 30° taper, as is the thermal-compression bonding tip. Ultrasonic ball bonding like thermal-compression bonding permits bonding in any direction without rotating the work. This is due to the symmetrical configuration of the tool tip.

Wire and Pad Size. As with ultrasonic wire bonding the wire size is determined by the circuit requirements although it is usually 1 mil gold wire. Bond area available for bonding was previously discussed under ultrasonic wire bonding.

Bond Size. Bond size is from two to six times the wire diameter. However, the size of the gold ball should be very closely controlled. This is made possible by varying the size of the hydrogen flame, flame off speed, flame overtravel, and bonding tip height above flame after second bond is made. The ideal size of the ball prior to bonding is two wire diameters. Surface conditions on the die might require a slightly larger ball, a determination to be made during bonding schedule development.

Bond Strength. Bond strength desired is that of the parent metal if attainable. Without an additional step, ultrasonic ball bonds will usually break at the second bond which is a wedge. A second ball bond may be placed directly over the wedge bond for greater strength. This second bond is then terminated on the same bonding pad. With the additional bond, the interconnect becomes a double ball bond and the wire rather than the bond will usually break when tested.

Bonding Pressure. Bonding pressure of both the first and second bonds in gold ball bonding may have different pressure loads. This is so because of the unique way in which adjustable spring loads are imposed on the transducer-coupler assembly. The pressure spring for the first bond works in a horizontal direction against the transducer. Most of the transducer-coupler assembly weight is forward of the transducer pivot point or toward the bonding tip. While in this first bond position, the second bond pressure spring (which is vertically attached to the cam follower) is held away from a stop pin on the transducer. This allows only that weight, or pressure, on the bonding tip that is imposed by the first bond pressure spring. As the bonding machine cycles to the second bond position the cam follower lever is allowed to rise against the stop pin, thereby imposing its pressure on the bonding tip. In the ultrasonic ball bonding process high gram pressure (90 to 120 grams) is needed to cut through the gold wire to form the wedge (second) bond. As the gold wire is actually cut through in the wedge bond termination it is easier to pull the cut through wire residue from the second bond point without disturbing the bond.

Termination. Termination is made by proper sequencing of the bonding tool and wire clamps as in the case of ultrasonic wire bonding. The purpose of this sequence is to have minimum drag on the wire during the stringing and looping cycles of wire bonding. The wire clamps are closed in the reset position (with gold ball against capillary face). From reset to first search the wire clamps remain closed. As the capillary drops to the first bond position the wire clamps open. The clamps remain open until the capillary rises about 90 mils above the second bond position, at which time they will close and rise with the capillary assembly, thus pulling the tail. The wire clamps remain closed until the capillary has reached the reset position and the flame off torch forms a new ball. At this time the clamps open and the spool rises pulling the gold ball against the capillary face. The clamps close again and the machine is at the end of its cycle.

Advantages. The advantages of ultrasonic ball bonding are:

1. Room temperature bonding.
2. By use of a double ball system a bond may be made that is stronger than the wire.
3. Bonding may be made in any position depending on the tool shape.
4. Since the tool is smaller than that required for ultrasonic wire bonding the bonds may be made in restricted areas.

Disadvantages. The disadvantages of ultrasonic ball bonding are:

1. Gold wire must be used.
2. If a double ball system is used bonding costs are increased since more bonds are made.

BEAM LEAD BONDING

Two methods are in use for beam lead bonding. The earliest method, and by far the most popular in industry, is the so-called wobble bonding. A later development known as compliant bonding is also utilized to some extent.

WOBBLE BONDING

Bonder Operation. Wobble bonding employs a tool somewhat the shape of a die attach collet. Instead of a scrubbing motion the tool literally wobbles about its vertical axis during bonding so that each beam on the device is bonded sequentially. Common practice is to make two revolutions to ensure that all beams are bonded. The interconnect is basically a thermal-compression bond since both the work holder and tool have heaters, and pressure is applied to the tool during bonding. Bonding may be accomplished with a cold substrate and heated tool, a cold tool and heated substrate, or with both heated.

Beam lead bonders utilize a partially surfaced mirror so that the face of the device may be viewed by the operator (beam lead devices are bonded face down) while simultaneously viewing the metallization pattern on the substrate. The tool utilizes a vacuum hole to allow the device to be picked up and held until placed on the metallization. When the beams are aligned optically with the metallization pattern, a switch is activated by the operator to cause the tool to contact the substrate and bond the device. The tool rises automatically at the end of the bonding cycle.

Film. Beam lead bonding may be made to both thin and thick film gold. Thick film platinum-gold or palladium-gold work equally well.

Substrate Flatness. One matter of concern is substrate flatness. An economic advantage of thick film processing is the ability to work with as-fired substrates which are not known for their flatness. If a sufficiently warped substrate is utilized, the chance that one or more bonds will not receive sufficient pressure is heightened. This can be found by visual inspection and repaired with a simple single bond machine. Such rework is time consuming and generally undesirable.

COMPLIANT BONDING

Bonder Operation. In order to accommodate less than ideal substrates the compliant bonder was developed. This bonder places a soft metal washer over the beams prior to bonding. The thought here is that the bonding forces will be better distributed even if the substrate surface in the area being bonded is somewhat out of parallel with the work holder, or if the metallization thickness is not constant at all bonding fingers. Introduction of the compliant washer somewhat complicates the machine and increases its cost. The washer is expended in making the bond and a new one used for the next device. The tool may wobble or simply come straight down on the washer. Washers must be available for all device sizes used.

ETCHED DEVICE

As mentioned previously, the beam lead device is etched out, not scribed out, so the problems encountered with less than perfectly scribed dice simply do not exist.

CHIP REMOVAL

If a chip is defective it may be removed with a sharp tool, tweezers, or a small machine designed to hold the package or substrate while a tool is positioned and moved to scrape the chip from the metallization. If one or more beams break from the chip and continue to adhere to the metallization these beams simply become part of the next bond.

ADVANTAGES OF BEAM LEAD BONDING

1. Beam lead devices exhibit at least an order of magnitude higher reliability.

2. Time required to completely bond the device is essentially independent of the number of beams, thus reducing bonding labor, especially for complex integrated circuits.

3. Rework is easily accomplished.

4. Bonding inspection is easily accomplished.

DISADVANTAGES OF BEAM LEAD BONDING

1. Many desirable device types are not as yet available in beam lead configuration.

2. Some current MOS devices may be degraded or damaged during beam lead formation, thus eliminating them as candidates for this technology.

3. Bonding machines are expensive although possessing a high production capability.

4. Devices are more expensive than conventional chips, even when the labor to attach both types is taken into consideration. This may not be the case for complex hybrids due to the increased yields and rework capability.

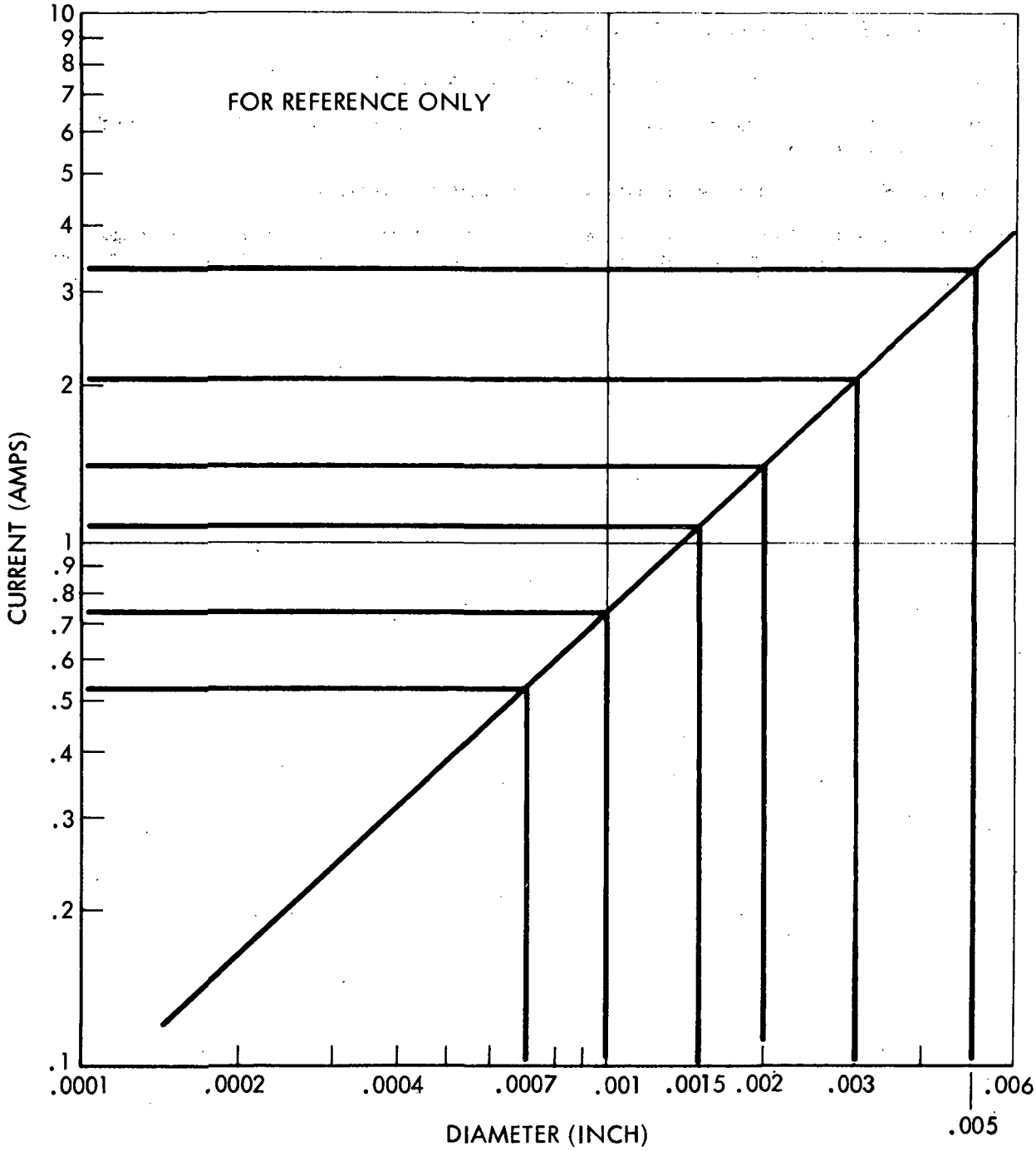


Figure B-1. 99.99% Gold Wire - Burn Out Current vs Diameter

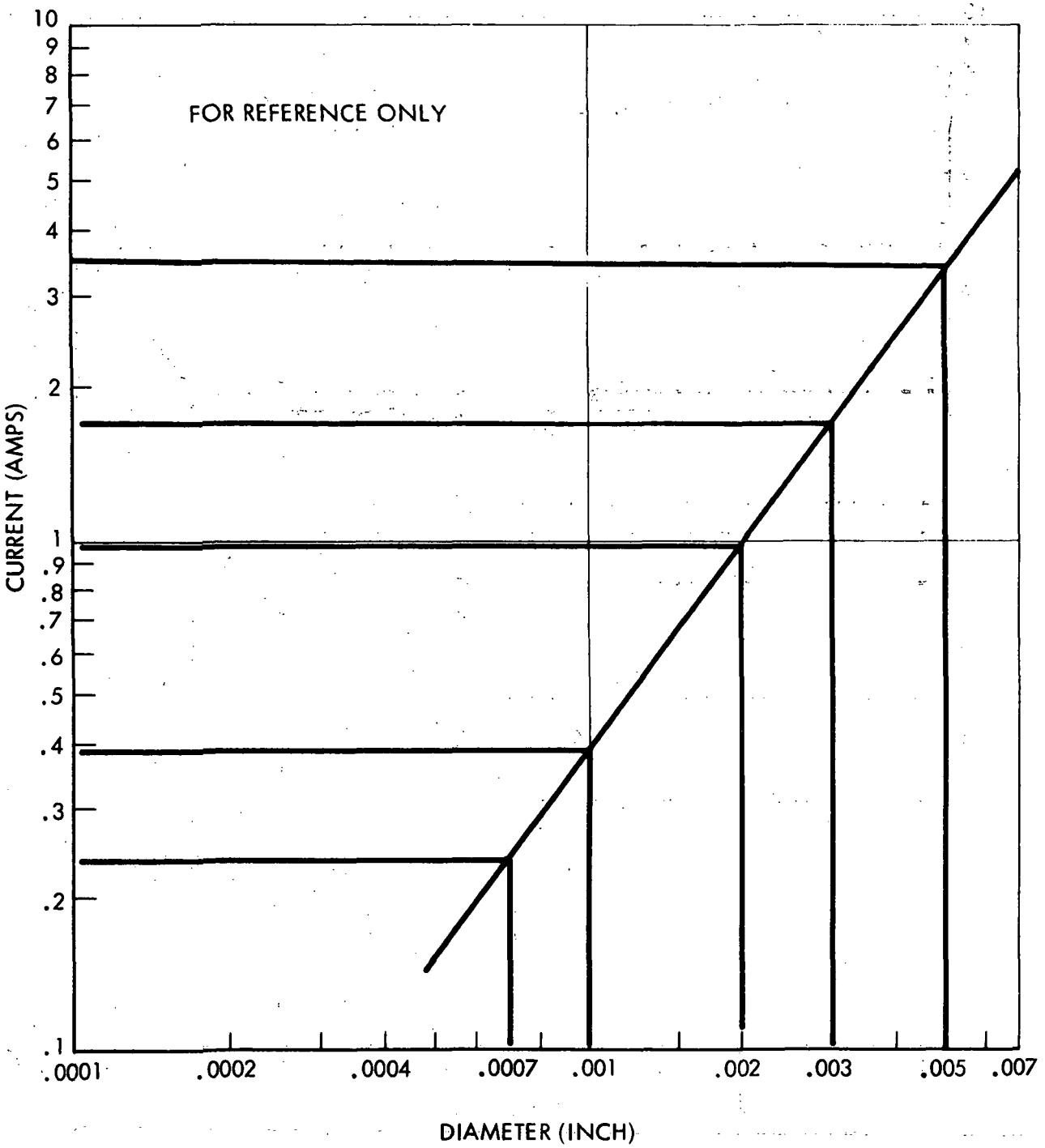


Figure B-2. 99.99% Aluminum Wire - Burn Out Current vs Diameter

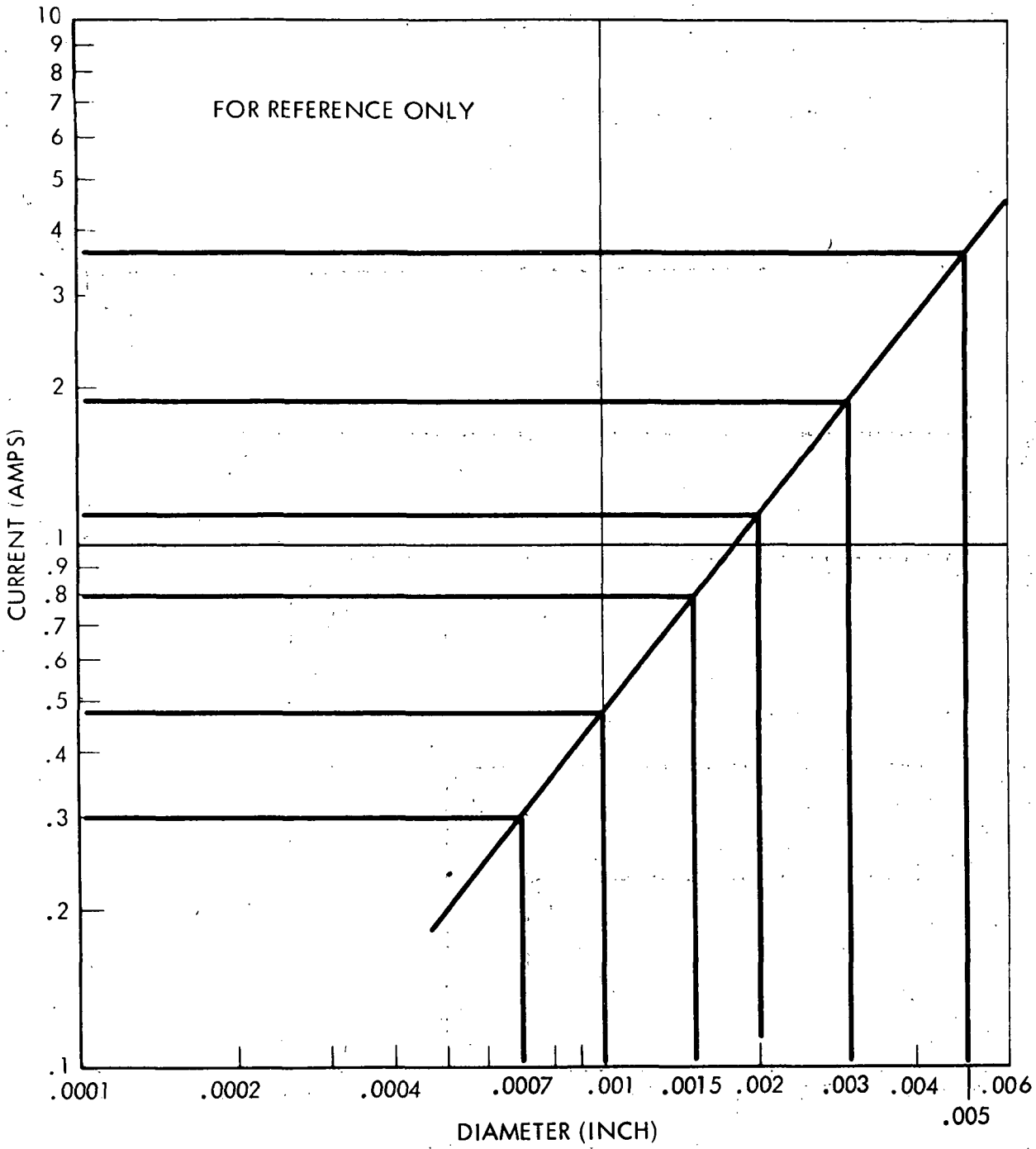


Figure B-3. 1% Silicon-Aluminum Wire - Burn Out Current vs Diameter

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KEYWORD INDEX

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