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HIGH PERFORMANCE DC-DC CONVERSION WITH VOLTAGE MULTIPLIERS

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ABSTRACT

The voltage multipliers using capacitors and diodes first developed by Cockcroft and Walton in 1932 were reexamined in terms of state of the art fast switching transistors and diodes, and high energy density capacitors. Because of component improvements, the voltage multiplier, used without a transformer, now appears superior in weight to systems now in use for dc-dc conversion. An experimental 100-watt 1000-volt dc-dc converter operating at 100 kHz was built, with a component weight of about 1 kg/kW. Calculated and measured values of output voltage and efficiency agreed within experimental error.

INTRODUCTION

Voltage multiplier power supplies for high voltage dc generation have been in use for many years. Cockcroft and Walton (1) built an 800 kV supply in 1932 for an ion accelerator application, and through the years their circuit has had many applications (2,3,4) with some analysis (1,4,5). Usually, these supplies have operated in an earth-type environment, where weight and efficiency are of secondary concern. Until recently the voltage multiplier was not considered seriously for space type high efficiency low weight applications. Within the last few years, however, substantial improvements have been made in lightweight capacitors, and in fast switching diodes and transistors. It now appears that, because of the major improvements in these power electronic components, that the voltage multiplier method of dc power conversion is superior in weight and efficiency for some applications to the more conventional transformer-rectifier system.

The body of this report will consist of two major parts. The first part will outline the basic circuit analysis, and the second will describe the construction and test results on a 100-watt 1000-volt dc-dc converter.

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THEORY OF OPERATION

General Description

Figure 1 shows a dc-dc converter using a transistor chopper and a capacitor diode voltage multiplier. Although two voltages V_{1i} and V_{2i} are shown, they will be assumed to be equal and equal to V_i for simplicity. The extension to unequal voltages can easily be made if necessary. A typical mode of operation, equivalent to $V_{1i} = V_{2i} = V_i$ is the use of a bridge of four switches, and only one power supply.

The switch operates at a frequency f, so that the voltage at the left terminal of C_N is alternately at $-V_i$ and $+V_i$ f times per second. Since C_N charges to V_i volts, the voltage at the junction of the capacitors C_{N-2} and C_{N-4} alternates between $2V_i$ and $4V_i$. In general, the voltage at the junction between C_{2j+2} and C_{2j} varies over a $2V_i$ range.

Thus the voltages at the junction points in the upper (even numbered) string of capacitors are square waves of voltage of amplitude V_i riding on top of a dc voltage which depends on the location in the chain. For the lower, or load string of capacitor (odd numbered values $C_1 \cdots C_{N-1}$) the voltage across each capacitor is $2V_i$, and across the entire ladder is NV_i, where N is the number of capacitors or diodes in the multiplier chain. Thus this converter may be thought of as a dc voltage transformer, with the load voltage V_L given by

$$V_L = NV_i \qquad (1)$$

The load current i_L is less than the source current i_s also by the ratio N.

$$i_L = \frac{i_s}{N} \qquad (2)$$

As will be seen later, both of these equations will need to be corrected for losses. It will be seen, however, that for a high efficiency system these corrections will be small.

The load output power P_L which will be derived later, is given by

$$P_L = 8\eta^2 f C_u V_i^2 r_L \qquad (3)$$

where

η overall efficiency

r_L calculated CDVM load ripple (actual ripple is about three to four times calculated ripple)

C_u capacitance of each unit capacitor

Capacitor Weight

In a space type power supply, minimum weight is of great importance. Since most of the weight in a capacitor diode voltage multiplier is in the capacitors, a rough preliminary estimate of weight can be made by considering capacitor weight only. The capacitor weight for each unit (C_1, C_2. . .C_N in fig. 1) is given by

$$W_u = \frac{\frac{1}{2} C_u (2V_i)^2}{k} \qquad (4)$$

where k is the energy density of the capacitor in joules/gm. Combining (eq. (3)) and (eq. (4)) with total weight $W = NW_u$ gives

$$\frac{W}{P_L} = \frac{N}{4\eta^2 f k r_L} \qquad (5)$$

For $0.8 < \eta < 1.0$, and N between 5 and 20 times multiplication, using k 0.01 joule/gm, $f = 10^5$ Hz, and for a ripple of 0.01

$$0.1 < \frac{W}{P_L} < 0.8 \quad \text{kg/kW}$$

This is small compared to components weight of even the most advanced converter (6), where a W/P_L of components of about 2.5 kg/kW was achieved.

Derivation of Current Equations

Although equation (2) gives an approximate value for the source current in terms of the load, for careful design and also for the calculation of efficiency, two kinds of leakage current should be considered. The first, reverse biased diode leakage current is normally in the microampere range for good semiconductor diodes and can be neglected in comparison with the diode forward or load currents, which are of the order of tenths to tens of amperes.

The second leakage current is that due to reverse biased junction capacitance charging, which cannot be neglected. This current, i_{JD}, is given by

$$i_{JD} = 2C_{JD}V_i f \qquad (6)$$

for each diode. If care is not taken to minimize C_{JD}, at frequencies of the order of 10^5 Hz, total current leakages from this cause may be of the order of 10 milliamperes and cannot be neglected. Similarly, the junction capacitance (C_{JT}) charging current of the two transistors must be considered. This section will develop an expression for the

currents in the capacitor diode voltage multiplier taking these two currents into account.

The current equation at the junction of C_1 and R_L for the case of odd diodes conducting is

$$\frac{-dq_1}{dt} + i_1 = i_L \qquad (7)$$

Similar equation can be written for all current modes. If these current equations are integrated to give equations of the type

$$-\Delta Q_1 + \frac{\langle i_1 \rangle}{2f} = \frac{\langle i_L \rangle}{2f} \qquad (8)$$

and the condition that

ΔQ_1 (even diodes "on")

$$= -\Delta Q_1 \text{ (odd diodes "on")} \qquad (9)$$

one obtains for the current from the voltage supply V_i

$$\langle i \rangle_{source} = N \langle i_L \rangle + 2C_\ell V_i f \qquad (10)$$

where the brackets indicate an average over a half cycle, and where:

$$C_\ell = C_{JT1} + C_{JT2} + NC_{JD} \qquad (11)$$

C_{JT1} output capacitance of NPN transistor

C_{JT2} output capacitance of PNP transistor

C_{JD} reverse bias diode junction capacitance

V_i input voltage

N number of capacitors or diodes in multiplier (8)

f operating frequency

The leakage capacitance charging term $2C_\ell V_i f$ may be several percent of the source (input) current and be one of the major sources of power loss in high efficiency dc-dc converters.

The current equations given above have been for average currents. It must be emphasized that the equality of the two average currents (say $\langle i_1 \rangle$ and $\langle i_2 \rangle$) does not in any way infer their equality at any given time. In fact, $i_2 = 0$ always when $i_1 > 0$ and vice versa. Similarly, $i_3(t) \neq i_1(t)$ although both i_3 and i_1 may be greater than zero at the same time. The detailed solution of $i(t)$ for the different diodes, or $q(t)$ for the different capacitors is not necessary for the determination of needed design parameters like output voltage, output ripple, and efficiency, and will not be given in this paper. In general, the $i_j(t)$ experimentally show a half cycle wave form of the type

$$i(t) = A \sqrt{\frac{C}{L}} e^{-Rt/2L} \sin \frac{t}{\sqrt{LC}} \qquad (12)$$

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where R is of the order of a few hundredths of an ohm and L is a few tenths of a microhenry for the 100-watt, 1000-volt, x8 multiplier supply described below.

Derivation of Output Ripple and Output Power Equations

The output ripple is a needed engineering design result when a capacitor diode voltage multiplier (CDVM) is used in a dc-dc converter. The load ripple is also a parameter in the efficiency and in the CDVM power output. This section will do the ripple derivation. The load ripple r_L is

$$r_L = \frac{V_{Lmax.} - V_{Lmin.}}{\langle V_L \rangle} \tag{13}$$

over a cycle of length $1/f$.

The total ΔV_L is equal to:

$$\Delta V_L = \frac{\Delta Q_1}{C_1} + \frac{\Delta Q_3}{C_3} + \ldots \frac{\Delta Q_{N-1}}{C_{N-1}} \tag{14}$$

It can be shown that

$$\Delta Q_1 = \frac{\langle i_L \rangle}{2f} + \frac{\langle i_{JD1} \rangle}{2f} \tag{15}$$

$$\Delta Q_3 = \frac{2\langle i_L \rangle}{2f} + \frac{\langle i_{JD3} \rangle}{2f} + \frac{\langle i_{JD2} \rangle}{2f} + \frac{\langle i_{JD1} \rangle}{2f} \tag{16}$$

$$\Delta Q_{N-1} = \frac{(N-1)\langle i_L \rangle}{2f} + \langle i_{JDN-1} \rangle + \ldots \frac{\langle i_{JD1} \rangle}{2f} \tag{17}$$

For the case of $C_1 = C_2 = \ldots C_N = C_u$

$$\Delta V_L = \frac{1}{2fC_u} \left[\langle i_L \rangle (1 + 3 + 5 \ldots N - 1) + \langle i_{JDN-1} \rangle + 2\langle i_{JDN-3} \rangle + \ldots \frac{N}{2} \langle i_{JD1} \rangle \right] \tag{18}$$

For identical diodes, i.e.,

$$i_{JD1} = i_{JD2} \ldots i_{JDN} \tag{19}$$

$$\Delta V_L = \frac{N^2 \langle i_L \rangle}{8 C_u f} \left(1 + \frac{\langle i_{JD} \rangle}{\langle i_L \rangle} \right) \tag{20}$$

Since i_{JD} is normally much less than $\langle i_L \rangle$, and since the ripple is a small change in the output voltage, one can write

$$\Delta V_L \approx \frac{N^2 \langle i_L \rangle}{8 C_u f} \tag{21}$$

within a few percent.

The ripple then is given by

$$r_L = \frac{N^2 \langle i_L \rangle}{8 C_u f V_L} \tag{22}$$

This may be written in terms of the output power P_L

$$r_L = \frac{N^2 P_\ell}{8 C_u f V_L^2} \tag{23}$$

The more exact expression for the load ripple r_L is

$$r_L = \frac{N^2 P_L}{8 C_u f V_L^2} \left(1 + \frac{\langle i_{JD} \rangle}{\langle i_L \rangle} \right) \tag{24}$$

and the power P_L can be written as

$$P_L = \frac{8 C_u f V_L^2 r_L}{N^2 \left(1 + \frac{\langle i_{JD} \rangle}{\langle i_L \rangle} \right)} \tag{25}$$

or within a few percent

$$P_L = \frac{8 C_u f V_L^2 r_L}{N^2} \tag{26}$$

By examination, it is apparent that output power depends directly on C_u, f, and r_L. Also, since $V_L/N \approx V_i$, output power depends on V_i as the second power. As is seen later under experimental results, a source of ripple other than as calculated for the CDVM exists. The quantity r_L in equation (26) is the calculated CDVM ripple.

Derivation of Efficiency and Output Voltage Equations

The efficiency of a CDVM dc-dc converter may be determined by calculating the individual losses in the process of one capacitor being charged from another and then adding these together for all the charge sharing processes in the CDVM and for the capacitor and diode capacitance charging losses. Both the energy lost during charge transfer, and the amount of energy transferred, are of importance. In order to calculate these quantities, only initial and final voltages were considered; losses and final energy transfer tend to be independent of current levels during charging and of voltage drops across stray inductances, lead resistances, and forward biased diode resistance.

Consider the charge transfer from a capacitor C_1 charged to a voltage V_{10} which charges a capacitor C_2 initially at a voltage V_{20} through a series resistance and/or inductance. The energy lost, E_ℓ for this transfer is

$$E_\ell = \frac{C_1 + C_2}{2 C_1 C_2} (\Delta Q)^2 \tag{27}$$

or

$$E_\ell = \frac{C_1 C_2}{2(C_1 + C_2)} (V_{10} - V_{20})^2 \tag{28}$$

If these losses are summed over all the capacitors in the voltage multiplier, and the result multi-

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plied by the frequency f to obtain the power loss

$$P_{\ell_{CDVM}} = \frac{1}{12fC_u} (\langle i_L \rangle + 2C_i V_i f)^2 N \left(N^2 + \frac{1}{2} \right) \quad (29)$$

Knowing the power loss, it is possible to compute the output voltage from the power balance equation.

$$P_{in} = P_\ell + P_L \quad (30)$$

where P_ℓ includes both the CDVM loss and the junction charging losses of the transistors. Thus

$$V_i(N\langle i_L \rangle + 2V_i fC_\ell) = \frac{1}{12fC_u} (\langle i_L \rangle + \langle i_{JD} \rangle)^2 N \left(N^2 + \frac{1}{2} \right)$$

$$+ C_\ell(2V_i)^2 f + V_L \langle i_L \rangle \quad (31)$$

This can be written in terms of load power P_L to obtain

$$V_L^2 \left[1 + \frac{2V_i^2 fC_\ell}{P_L} + \frac{(i_{JD})^2}{12fC_u} \frac{N\left(N^2 + \frac{1}{2} \right)}{P_L} \right]$$

$$+ V_L \left[-V_L N + 2 \frac{\langle i_{JD} \rangle}{12fC_u} N\left(N^2 + \frac{1}{2} \right) \right]$$

$$+ \frac{P_L}{12fC_u} N\left(N^2 + \frac{1}{2} \right) = 0 \quad (32)$$

The dominant terms in the above equation are

$$V_L^2 - V_L N V_i = 0$$

which gives

$$V_L \approx N V_i$$

This is equation (1).

The most exact equation for V_L may be obtained by solving the quadratic equation, and this solution may be needed for some cases.

This can be simplified, without losing significant accuracy in most cases, by ignoring the terms in i_{JD} and $\langle i_{JD} \rangle^2$ and dropping products of relatively small terms. The result is

$$V_L = \frac{N V_i \left[1 - \frac{P_\ell \left(N^2 + \frac{1}{2} \right)}{12fC_u N V_i^2} \right]}{\left(1 - \frac{2V_i^2 fC_\ell}{P_L} \right)} \quad (33)$$

This expression is accurate as long as $P_L > 2V_i fC_\ell$ so that the terms in parentheses are only a few percent different from unity. The efficiency may be derived from the V_L and i_s equations from the expression

$$\eta = \frac{i_L V_L}{i_s V_i} \quad (34)$$

using

$$i_s = N i_L + 2C_\ell V_i f$$

This efficiency is approximately

$$\eta = \frac{1 - \frac{P_\ell \left(N^2 + \frac{1}{2} \right)}{12fC_u N V_i^2}}{\left(1 + \frac{2fC_\ell V_i^2}{P_\ell} \right)^2} \quad (35)$$

EXPERIMENTAL RESULTS

Description of Experimental Converter

An experimental converter was built to operate at a nominal 100-watt output range. It was through the building and operation of the converter that the above design equations were developed, through a combination of experimental measurements and analytical studies. For example, the major loss, that due to reverse biased junction capacitance charging in the diodes and transistors was discovered through experimental measurements. The analysis given above was then developed consistent with the experimental results. This converter was built to locate losses, to guide theoretical analysis, and in general to aid in the development of transformerless, low loss, lightweight converters as a class. It is not meant to be a dc-dc converter to fill a particular application, but as part of an overall program which leads to the goal of improved, lightweight high efficiency space type converters, where high voltage dc is required. Therefore, the logic, protection, and drive details are not included, but must be developed as required for specific applications.

The operating frequency, which was obtained from a signal generator, was a nominal 100 kHz, although the frequency was varied from about 50 to 200 kHz. The "on" time of the signal generator was variable, and was adjusted to avoid both transistors conducting at the same time due to junction charges storage effects. The signal generator was capacitively coupled to the switching transistor bases since the two transistors were floated above ground potential by the input voltages V_{1i} or V_{2i}. For most of the work V_{1i} and V_{2i} were equal and were about 130 volts. The transistors were fast power devices, with turnon times of 200 nanoseconds, storage times of 2 microseconds, and turnoff times of also about 200 nanoseconds. The rated operating current for the NPN transistor (type SVT 350-5) was 5A, with a standoff voltage of 350 volts and an output capacitance of 350 pF. Two pnp transistors (type 2N6213) were paralleled to obtain sufficient current rating. Each transistor rating was 2A, with a standoff voltage of 400 volts and an output capacitance of 200 pF. The turnon, storage, and turnoff times were the same as the NPN transistor. The diodes

used were fast power devices, with a reverse time of about 100 nanoseconds, a current rating of 3A, and a junction capacitance at operating voltage of about 25 pF.

Each capacitance in the voltage multiplier (C_1, C_2. . .C_N) consisted of three series 2.2-microfarad 100-volt capacitors, giving a composite rating for C_1, C_2. . .C_N of 0.7 microfarad. The individual capacitors were high energy density (0.01 j/g) ceramic devices.

Measured Results

The nominal output of the voltage multiplier built was eight times the input voltage, modified by losses as shown above. Table I compares measured and calculated output voltages over a range of input voltages (and output power) for a fixed load resistance.

Table II compares calculated with measured output voltages for a fixed input voltage but with variable output load resistance. From these two tables, it is seen that the measured and calculated voltages agree fairly well, for the higher voltage inputs and, that the voltage multiplication ratio is a few percent under the zero power level of eight times.

Table III shows the efficiency as a function of output power. The overall efficiency was measured directly in dc terms by taking the ratio of the product of the dc output current and voltage to the input dc current and voltage at each power level. The nominal input voltage was 130 volts, with an operating frequency of 100 kHz. Again the calculated results agree reasonably well with the measured values. Accuracy of the measured results was about ±2 percent. The primary losses were calculated to be a junction capacitance charging loss. This was verified by the addition of a 0.001 microfarad capacitance in parallel with the output transistors and measuring the resulting decrease in efficiency.

Table IV shows the ripple as a function of output power, comparing measured and calculated values. As expected, the ripple increases with output power. No filter was used. At 100 kHz, only a minimal filter would be necessary to reduce the output ripple to a much lower value. The ripple as experimentally measured was three to four times larger than calculated. The cause of this excess ripple was not determined, but is thought to be due to resonant charging of the CDVM capacitors through stray lead inductances.

Measurement of Component Weights

A list of the components used and their weights for the nominal 100-watt experimental converter is given in Table V. This is equivalent to 1.15 kg per kW (2.5 lb/kW).

CONCLUSIONS

A preliminary investigation of the voltage multiplier, driven by a transistor chopper without a transformer, was made using both experimental and analytical methods. This concept appears extremely promising for the development of very lightweight, high-efficiency dc-dc conversion.

Agreement between experimental results and calculations was fairly good except for ripple. Experimentally, it was found that the primary losses were in the charging of transistor and diode junction capacitors, and in the charging of the voltage multiplier capacitors from one another. It was also found experimentally that the capacitor charging currents in the voltage multiplier network followed a resonant charging time dependence, and the charging rates were determined by the product of multiplier capacitance and the stray inductance.

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TABLE I. - COMPARISON OF MEASURED AND CALCULATED VOLTAGE OUTPUT VERSUS VOLTAGE INPUT FOR FIXED LOAD RESISTANCE

Volts input	Watts output	Volts output measured	Volts output calculated
80	32	620	586
90	39	685	660
100	48	760	733
110	57	830	806
120	68	900	880
130	78	970	953
140	90	1040	1027

TABLE II. - COMPARISON OF MEASURED AND
CALCULATED OUTPUT VOLTAGE VERSUS OUTPUT POWER

Output power watts	Output voltage measured	Output voltage calculated	Voltage multiplication ratio
50	1001	947	7.8
65	987	952	7.7
79	970	953	7.6
92	957	957	7.6
99	946	949	7.5

TABLE III. - COMPARISON OF
CALCULATED AND MEASURED
EFFICIENCIES AS A FUNCTION
OF OUTPUT POWER

Power output watts	Measured efficiency	Calculated efficiency
41	0.86	0.83
51	.83	.86
53	.85	.86
55	.86	.86
66	.85	.88
72	.86	.88
76	.85	.88
86	.85	.88
91	.79	.89
104	.82	.88

TABLE IV. - COMPARISON OF MEASURED AND
CALCULATED OUTPUT VOLTAGE RIPPLE AS
A FUNCTION OF OUTPUT POWER

Power output watts	Output voltage	Measured output ripple (PTP)	Calculated output ripple (PTP)
42	1010	1.6%	0.5%
51	1122	1.8	.5
53	1135	1.8	.5
55	1007	2.4	.6
66	1103	2.5	.6
72	1048	2.8	.8
76	1012	2.8	.7
86	1029	3.4	.9
91	915	3.4	1.2
104	978	3.5	1.2

TABLE V. - WEIGHT OF
COMPONENTS IN EXPERIMENTAL
100-WATT DC-DC CONVERTER

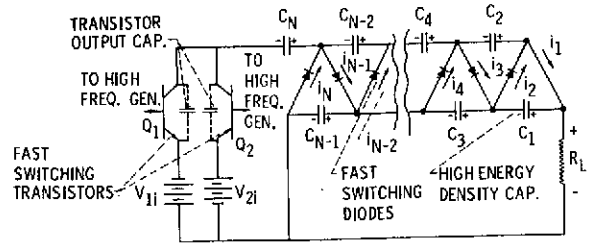| Component	Weight, g
Capacitors	70
Diodes	8
Power transistors	23
Miscellaneous	14
Total	115

Figure 1. - Transformerless capacitor diode voltage multiplier DC - DC converter. Either V_{1i} or V_{2i} can be zero or chosen arbitrarily within component ratings.