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ANALOG SIGNAL TO DISCRETE TIME INTERVAL CONVERTER (ASDTIC)

by

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ABSTRACT

An electronic control system for nondissipative d.c. power converters is presented which improves (1) **the routinely attainable** static output voltage accuracy to the order of **+.1 % for ambient** temperatures from -55 to 100° C and (2) the dynamic **stability by** utilizing approximately one tenth of the feedback gain needed otherwise.

Performance is due to a functional philosophy of "deterministic pulse modulation". based on pulse area control and to an autocompensated signal processing principle. The system can be implemented with commercially available unselected components. The system serves as a multipurpose functional block and is being used on a number of significant Government programs.

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I. INTRODUCTION.

1. Historical Background.

The presented system was developed in the Power Systems Laboratory of the Electronic Research Center, NASA, Cambridge, Massachusetts during the years 1966 and 1967 by the author [1] (see also Appendix B to this Report). Its development builds on previous work [2, 3]. After completion of development and testing of the then new ASDTIC system (Ch. VI) support of industry was engaged to transform it into a microminiaturized form [4]. The microminiaturized ASDTIC performed equally well (Ch. VI) and was first used in NASA programs.

The ASDTIC research program was transferred in July 1970 to the Lewis Research Center, NASA, Cleveland, Ohio. Work on its further development was continued in its laboratories and continues to be supported by industry. A set of three different types of ASDTIC controlled d.c. power converters was fabricated and is now being evaluated in the Power Electronics Branch of the Lewis Laboratories and at other NASA Centers. Cooperation with the U.S. Electronics Command, Ft. Monmouth, N.J., and with the FAA led to development programs which are utilizing ASDTIC control systems in d.c. power converters.

2. Content.

An electronic control system is described that governs the operation of d.c. converters which employ nondissipative pulse modulation techniques

for scaling and stabilization of d.c. voltage or current.

The system is compatible with most known d.c. power converter circuits and is intended to serve as a multipurpose functional block for design and construction of these systems.

A control system was devised that improves

- a. the readily attainable static stability of d.c. power converters by ~~approximately~~ one order of magnitude, from + 1 percent output voltage ~~tolerance to~~ + 0.1 percent.
- b. ~~the dynamic~~ behavior of these power converters appreciably, based on a ~~reduction~~ of the needed feedback gain by approximately one order of magnitude, and yet achieves an improved static stability.

The principles of nondissipative d.c. power conversion are reviewed in Chapter II. The therewith associated processes and objectives are described and the general terminology is defined.

The significant properties of the pulse modulated d.c. converter with conventional feedback control are reviewed and discussed in Chapter III. The compatibility of static with dynamic stability of this converter is investigated and the therewith associated limitations indicated.

Characteristics and commonalities of various pulse modulation systems are treated and analyzed in Chapter IV. The concept of pulse area control is introduced and shown to govern equally the known pulse width (PW) and pulse frequency (PF) modulation processes used for power conversion and control. The response of this type of converters to steady state variations and to continued and sporadic disturbances of the source voltage is analyzed; the capability of this deterministic pulse modulation process (DPM) to suppress the referred to variations and disturbances during open loop operation in the conventional sense is presented with quanti-

tative indication of effectiveness and limitations.

The material presented in Chapter IV includes the response of linear networks to recurrent and specifically programmed pulses. This process is mathematically formulated as the response of linear filters to periodic or aperiodic trains of uniform or ~~nonuniform~~ impulses. Formation of these pulses is governed by (1) the desired filter response and (2) the source voltage variations and disturbances. A process of synthesis is applied to arrive at general rules that govern the pulse forming process. The presented material is accordingly related to the concerned aspects of system and network theory.

The theory throughout Chapter IV is presented in engineering terms using intuition and plausibility arguments to introduce the significant system aspects. The existing rigorous mathematical basis was deleted as being beyond the scope of this presentation. Readers concerned, primarily, with circuit design aspects of the presented control system can omit this material and proceed to Chapter V.

One application of DPM processes for stabilization of d.c. power is introduced in Chapter V. The system concepts evolved in the preceding chapter are reformulated and translated into functional concepts. A signal converter is defined which (1) accepts analog signals emanating from the electronic power switch of the power converter's pulse modulator and which (2) translates these analog signals into discrete time intervals, such that the pulse forming electronic power switch is turned on and off to satisfy the intended power control purpose. Interaction of this analog signal to discrete time interval converter (ASDTIC) with the electronics of PW, PF and PW-PF modulated d.c. power converters is presented, including the interaction of the pulse modulation process with the therewith associated linear, passive, time invariant low pass filter.

Addition of conventional feedback techniques to remove residual errors of the output voltage is outlined. So called, "quasi DPM processes" are described which are used for dynamic stabilization of Type I feedback systems which integrate the feedback error. Finally, a brief outline of the dynamic stability problem is given; treatment of this topic is restricted to indication of the advantages of a comparatively small gain of the feedback amplifier, if any.

The embodiment of the functional mechanisms of DPM control as evolved in Chapter V into an electronic network is presented in Chapter VI. The functional objectives are stated. The electronic control system is implemented with application of a principle of autocompensation; it reduces and removes the errors caused by the electronic control mechanism itself by letting each component counteract the error it causes.

The significant sources of residual errors are indicated. Test results of ASDTICs in discrete component and thick film hybrid form are presented showing a tolerance of performance of ± 100 parts per million over the ambient temperature range from -55 to 100° C.

The conclusions presented in Chapter VII compare program goals with results and include recommendations for further work in this area. This includes an extension of the present frequency range of ASDTIC beyond 50 kHz and yet further improvement of the dynamic characteristics which ASDTIC imparts to d.c. power converters.

II. PRINCIPLES OF NONDISSIPATIVE D.C. POWER CONVERSION.

1. D.C. Power Conversion.

The purpose of the d.c. converter is to:

- scale the magnitude of the time varying unipolar voltage $e(t)$ of a source of electric energy as illustrated in figure 1(a) and/or to
- stabilize the resulting output voltage $e_o(t)$ to remain within prescribed limits, illustrated in figure 1(b)

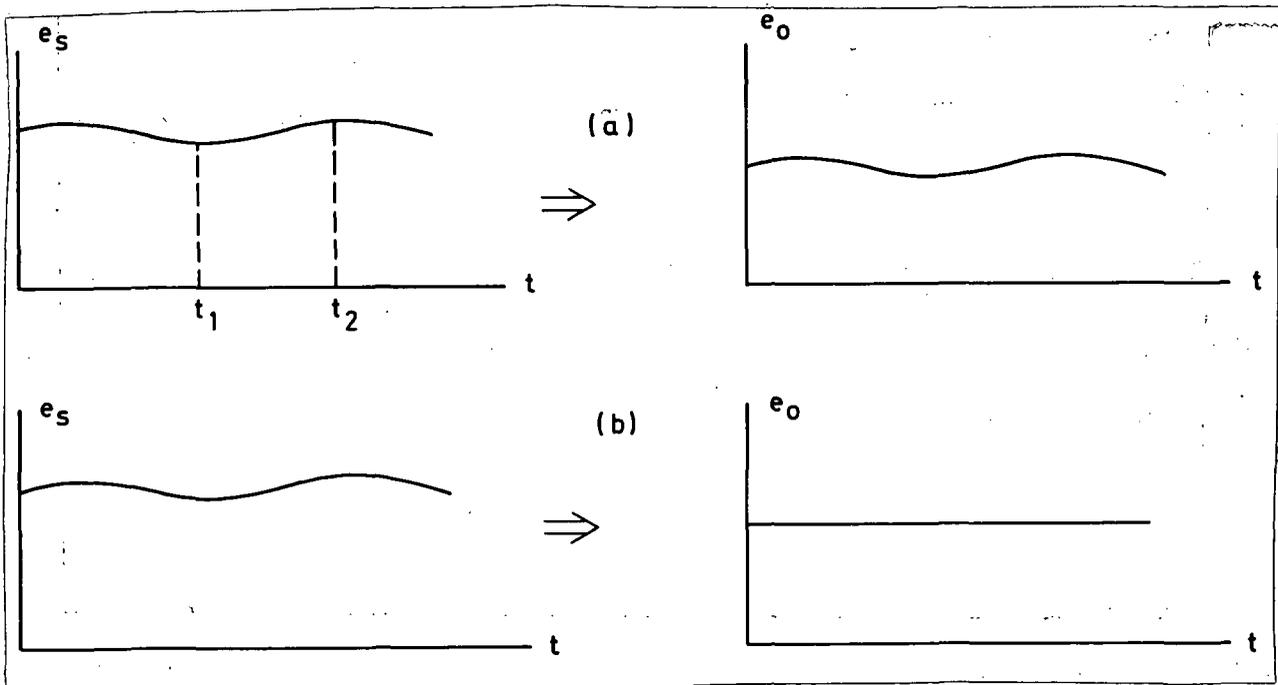


Figure 1.

Transformation of source voltage $e_s(t_1) \neq e_s(t_2)$: (a) scaling, $e_s/e_o = \text{constant for any } t$, (b) $e_o = \text{constant for any } t$.

The following discussion applies, in principle, equally to scaling and stabilization of unipolar currents, commonly referred to as d.c.; appropriate modifications of arguments will have to be introduced for that purpose. Application of the described technology for control of unipolar currents is illustrated in chapter IV; the following presentation is, at first, restricted to voltage scaling and, in particular to, stabilization.

All low case letters which follow express functions of time, such as $e_s(t)$; symbol t in parathesis will be deleted, in general, unless characterization of time dependence of a function is emphasized. Some low case letters, such as k, l, m, n are often used as indices. All time invariant quantities are symbolized by capital letters.

The d.c. power conversion process can be characterized by the transformation of one function, e_s , to another e_o . The transformed quantities

$$e_s(t) \rightarrow e_o \quad (2.1)$$

are defined

$$e_s = e_{dc} + e_{ac} \quad (2.2)$$

$$e_o = v_o + v_{os} + v_F \quad (2.3)$$

and

e_{dc}, v_o = slowly and irregularly varying d.c. voltages of different magnitude

e_{ac}, v_{os} = recurrent variations of e_s and e_o respectively
(such as line ripple and the resulting system response)

v_F = system response to internal converter (pulse modulation) processes

$E_s = \frac{1}{2}(e_{s \max} + e_{s \min})$, the nominal d.c. input voltage

$V_o = \frac{1}{2}(e_{o \max} + e_{o \min})$, the nominal d.c. output voltage

Voltage maxima and minima are specified design limits.

Statements (2.2) and (2.3) are rewritten, respectively, as

$$e_s = e_{dc} + \sum_{n=1}^{\infty} E_{sn} \sin(n\omega_s t + \phi_{sn}) \quad (2.4)$$

$$e_o = v_o + \sum_{n=1}^{\infty} V_{osn} \sin(n\omega_s t + \psi_{sn}) + \sum_{m=1}^{\infty} V_{oFm} \sin(m\omega_F t + \psi_{Fm}) \quad (2.5)$$

The second term in (2.4) is usually referred to as the "line ripple", except for temporary disturbances. Its first harmonic dominates the system behavior, as will be clarified further on. This expression is therefore often written as

$$e_s = E_{DC} + E_{s1} \sin \omega_s t \quad (2.6)$$

where E_{DC} is a "constant value" of $e_{dc}(t)$ at a given time.

The above defined input voltage e_s and its common aspects is illustrated in figure 2.

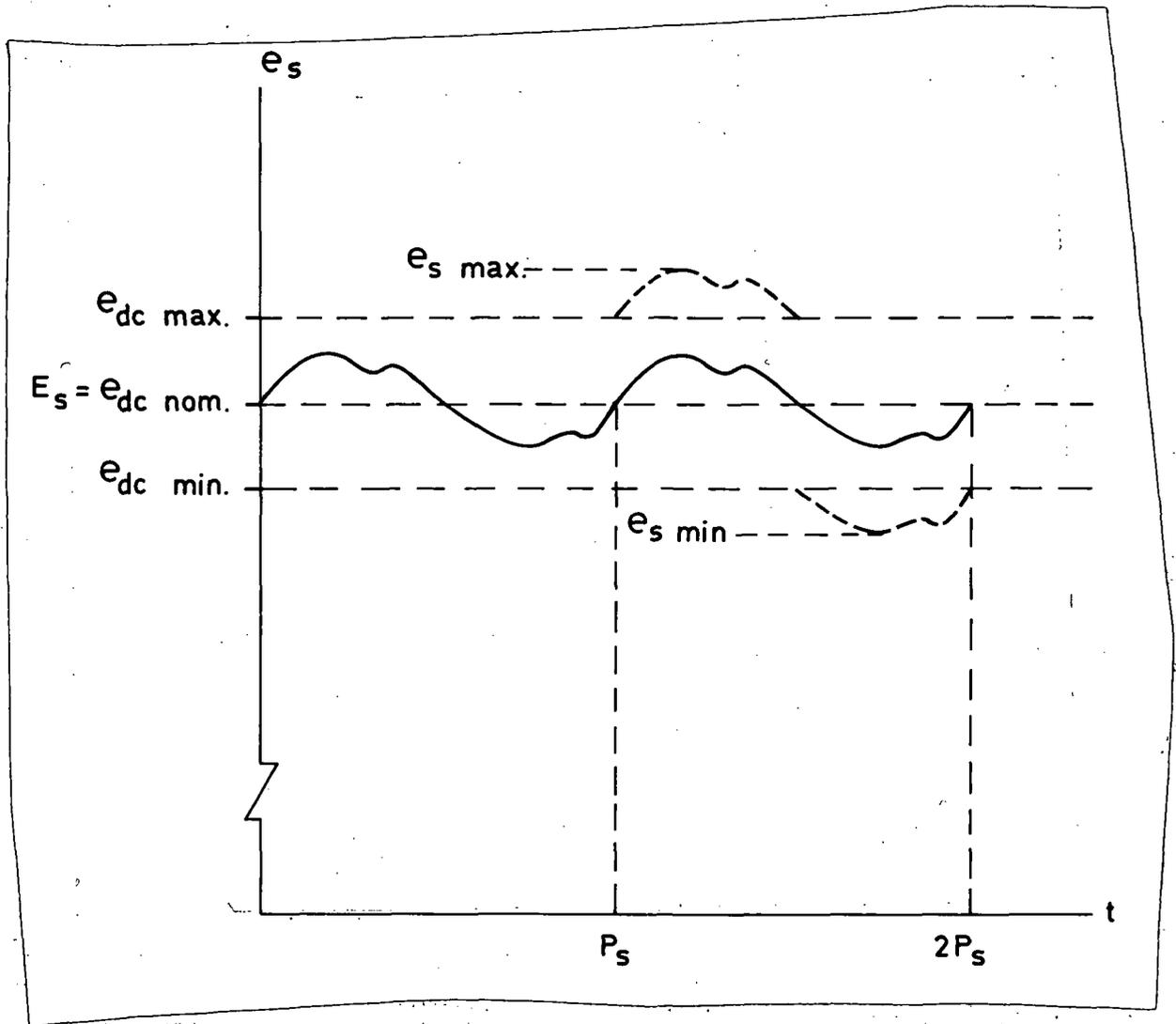


Figure 2.

Voltage e_s of the source of electric energy consisting of a unipolar component e_{dc} and a periodically varying component e_{ac} with nonzero average content.

Relation (2.5) is often written as

$$e_o = v_o + V_{os1} \sin(\omega_s t + \psi_{s1}) + V_{of1} \sin(\omega_F t + \psi_{F1}) \quad (2.7)$$

with indication of the first harmonic components only, which yields useful results for engineering purposes in many cases. These simplifications are used to facilitate the analysis of the d.c. converter systems with respect to its steady state behavior, and may have to be considered for other purposes.

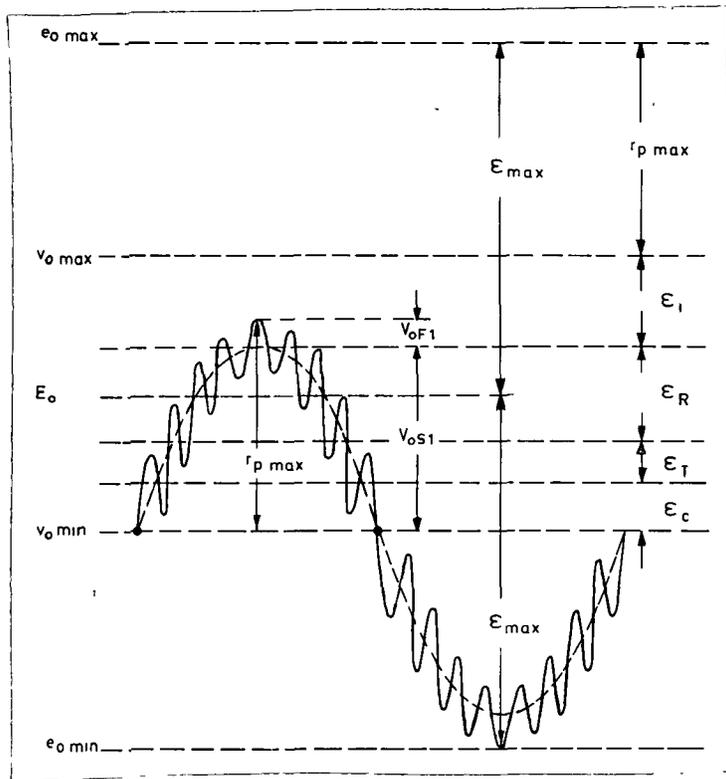


Figure 3.

Effects which cause errors in the output voltage of feedback controlled d.c. power converters.

Relation (2.7) and the significance of the individual symbols are illustrated in figure 3. The maximum value of the composite ripple

$$r_{p \max} = V_{os1} + V_{or1}$$

$$v_o = E_o + \sum \epsilon_p \quad (2.8)$$

where the ϵ_p are defined as maximum deviations of v_o from its maximal value $v_{o\max}$, due to

ϵ_R variations of load current i_o operating on the **apparent converter resistance**

$$R_s = \frac{e_o(\text{at } i_o \text{ min}) - e_o(\text{at } i_o \text{ max})}{i_o \text{ max} - i_o \text{ min}} \quad \left| \quad e_s = E_s$$

ϵ_T variations of power component characteristics caused by changes of operating temperature and by aging

ϵ_c limitations of accuracy of the electronic control system caused by intrinsic limitations of its functional mechanism, by temperature effects and aging of control electronics.

2. Non-Dissipative D.C. Conversion Processes.

Methods of pulse modulation have been used for non-dissipative d.c. to d.c. conversion for many years. They replaced the formerly used dissipative type series regulator which is now almost exclusively restricted to low power level (10 Watt) converters and regulators for the supply

of electric energy to various electronic systems.

The application of these methods is motivated by the necessity to avoid the generation and concentration of appreciable quantities of heat and the associated problems of heat disposal, and utilize the prime source of electric energy, such as solar, electrochemical or other power in the most cost effective manner.

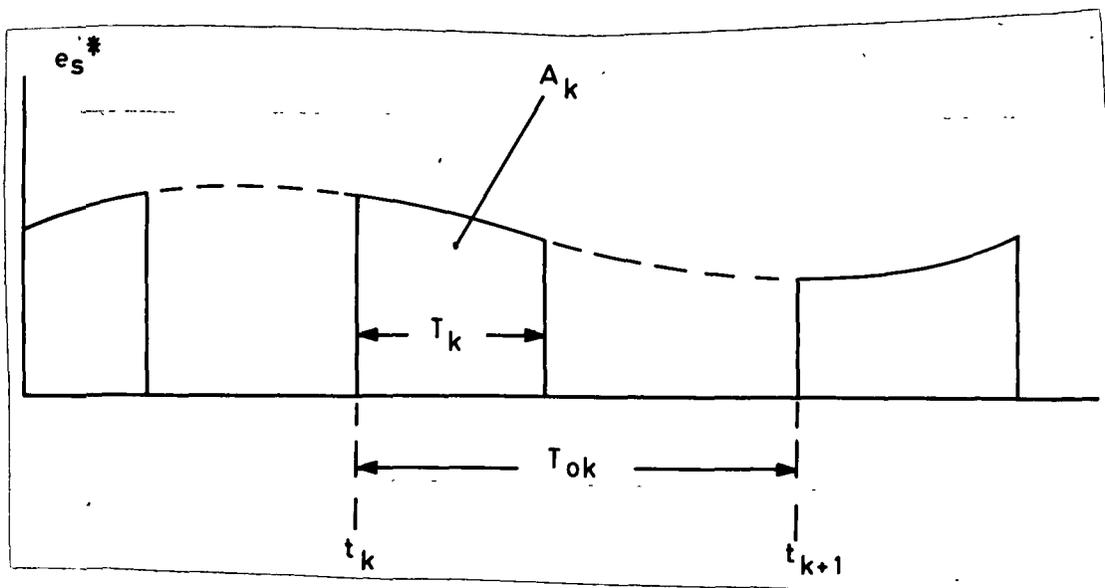


Figure 4.

Pulse train e_s^* derived by sampling of source voltage e_s .

Pulse modulation is a nominally non-dissipative process which transforms a voltage e_s into a pulse train (see figure 4).

$$e_s^* = \sum_{k=1}^{\infty} g_k(t) \quad (2.9)$$

where

$$g_k(t) = \begin{cases} e_s & \text{for } t_k < t < t_k + T_k \\ 0 & \text{everywhere else} \end{cases}$$

$$t_k = \sum_{m=1}^{k-1} T_{om} \quad T_{om} \neq T_{om+1} \quad (2.10)$$

The symbol \neq means: "not necessarily unequal". The volt-second integral of the k th pulse is indicated by the symbol A_k and defined by (4.3). A pulse train e_s^* as indicated in (2.9) and (2.10) is symbolically illustrated in figure 5(a) with $de_s/dt = 0$ for simplicity of graphic presentation.

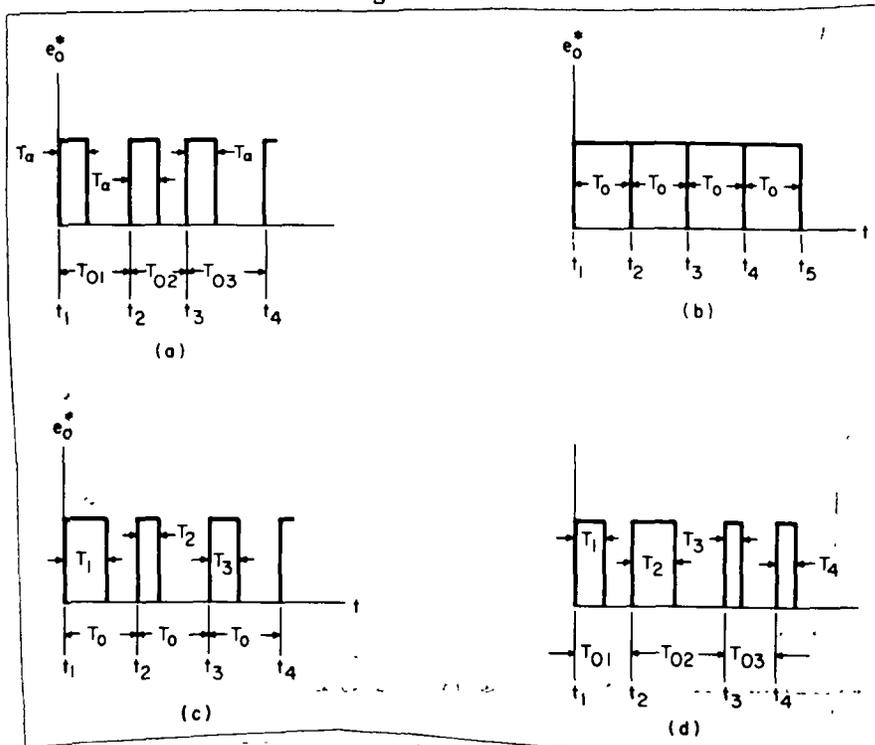


Figure 5.

Forms of pulse modulation frequently used in power processing: (a) pulse frequency modulated (PFM) rectangular wave, (b) rectified square wave, (c) pulse width modulated (PWM) rectangular wave, and (d) mixed PWM-PFM rectangular wave.

The pulse width

$$T_k \doteq T_{k+1} \doteq T \quad (2.11)$$

is not necessarily, but can be presumed to be equal unless otherwise indicated. If (2.11) holds then e_s^* represents a frequency modulated pulse train (PFM).

Figure 5(b) illustrates a succession of adjacent rectangular pulses which result from rectification of the output voltage waveform of a "square wave" inverter. This process is used for scaling only since $T_k = T_{k+1} = T_{ok} = T_{ok+1} = T_o$.

. If

$$t_k = kT_o \quad (2.12)$$

where

$$T_o = T_{ok} = T_{ok+1} \quad (2.13)$$

and

$$T_k \neq T_{k+1} \neq T \quad (2.14)$$

as illustrated in figure 5(a) then (2.9) and (2.12) through (2.14) represent a width modulated pulse train (PWM).

Likewise if (2.8) through (2.10) and (2.14) hold, then the pulse train

is both pulse width and pulse frequency modulated (PW-PFM). Such a pulse train is indicated in figure 5(d).

Table I. Methods of Pulse Modulation for Processing of Power.

Modus Operandi	Square Wave	PWM	PFM PWM-PFM	$T_m = T_n$ $T_m \neq T_n$) $T_{om} \neq T_{on}$
Time Intervals T_k, T_{ok}, t_k ***	$t_k = (k-1)T_o$ $T_k = T_o$	$t_k = (k-1)T_o$ $0 < T_k/T_o < 1$	$t_k = \sum_{j=1}^k T_{oj}$ $0 < T_k/T_{ok} < 1$	
Degrees of Freedom of Control	None	1	PFM 1 PWM-PFM 2	
$k=1,2,3, \text{ to } n$	In Process of Inversion $e_s^*(t_k) = \begin{cases} > 0 \text{ for odd } k \\ < 0 \text{ for even } k \end{cases}$			

*** T_k = pulse width, T_{ok} = pulse interval, and t_k = instant of pulse initiation.

The degree of freedom relates to the functions that can be performed by certain pulse modulation processes:

None Square Wave. Evidently there is no way of altering the envelope of the pulse train if they form a continuous signal consisting of adjacent blocks.

1 PWM. The envelope of the train of periodically repeating pulses can be shaped by varying the width of the individual pulses.

PFM. The same can be achieved by varying the intervals of pulses with equal areas A_k .

2 PWM-PFM. The envelope of this aperiodical train of nonuniform pulses can be shaped by varying the pulse width or their repetition rate or both. However, in addition to the requirement to form an envelope one can impose one more constraint on the modulation process since either of its features (PWM or PFM) by itself can satisfy this requirement. A second constraint can originate from a component limitation such as the saturation of magnetic core materials contained in network components.

The significant characteristics of pulse modulation processes are summarized in Table I.

If one uses the nominal values E_s and E_o for input and output voltage of a chopper and it is desired that

$$E_o = k_r e_r \quad (2.15)$$

where

$$e_r = \text{a reference voltage with property } de_r/dt = 0$$

then it is necessary that

$$k_r e_r T_{ok} = E_s T_{sk} \quad (2.16)$$

This relation suffices for steady state conditions and after idealization of the concerned network with its associated voltage wave forms.

One of the simplest d.c. converters which uses pulse modulation techniques is the series chopper as illustrated in figure 6. Only the power circuit is shown. The associated critical waveforms are indicated below in an idealized form for simplicity of presentation. The train e_s^* would, in reality, not have flat tops on the individual pulses.

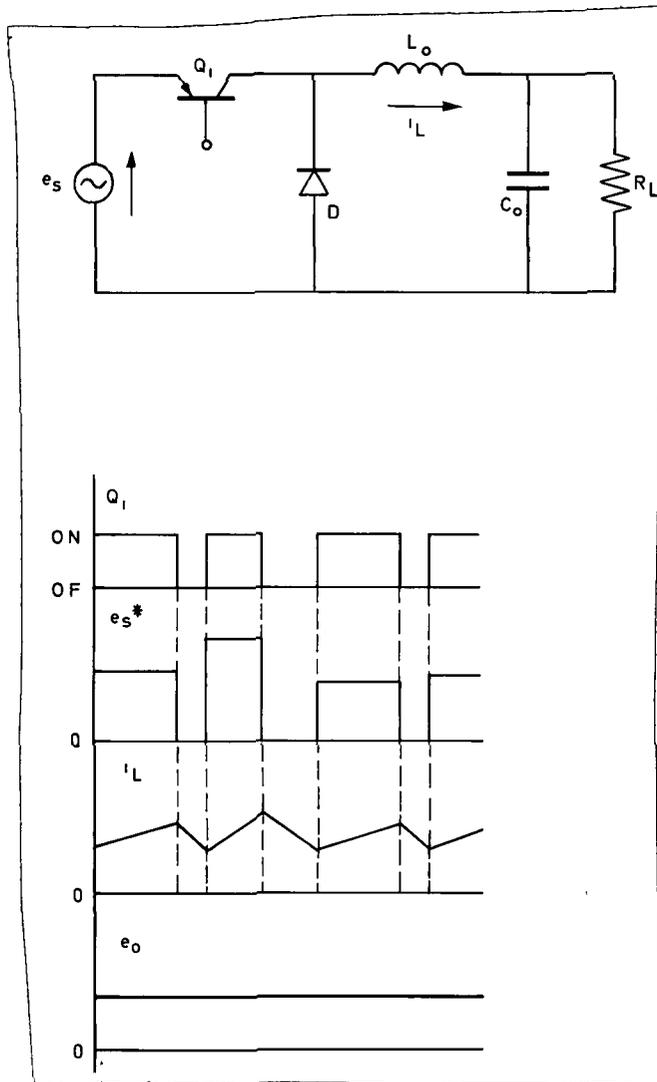


Figure 6.

Common series chopper and the associated critical waveforms.

- (b) Overshoots caused by delay between the demand of energy supply to the load and the surplus of energy stored in inductive elements anywhere in the power supply or power processing system. These overshoots occur at:
 - i. The start of the system
 - ii. Following sudden load changes
- (c) Load voltage regulation (deviation) caused by a variation in load current with limited steady state error correction capability of the converter control system.
- (d) Undershoot caused by suddenly increased current demand of the load.
- (e) Break down caused by an excessive current demand of the load, such as a short circuit current, and due to:
 - i. Inability of the source to supply the demanded energy
 - ii. Protective measures taken by the power processor.
- (f) Rise time of output voltage of converter.
- (g) Settling time of the system.

Another significant embodiment operating on the same principle is the parallel inverter illustrated in figure 8. This system is, in essence, a two sided chopper which operates through a transformer and a rectifier into the same output filter as that of the chopper. The filters of both discussed systems "see" at their respective input terminals the same type of pulse train enter.

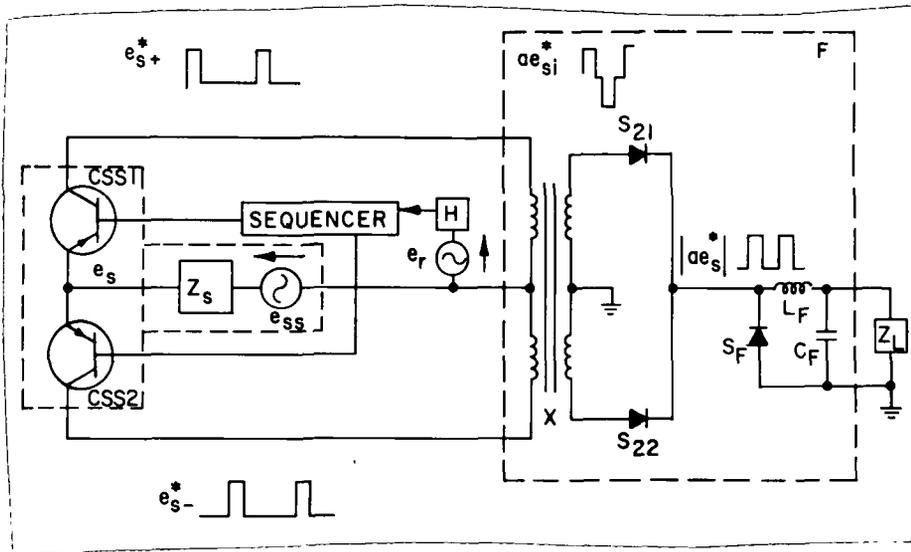


Figure 8.

Diagram of power pulse modulator incorporating inversion process.

The above advantages of pulse modulation cited under this section are counterbalanced by newly introduced problems, such as: (a) an increase in the complexity of control, (b) a substantial increase in the significance of parasitic effects in fast switching power circuits causing new types of stresses on components and compounding the problems of system and circuit analysis, and (c) the occurrence of dynamic phenomena, such as inadequate insensitivity of the systems to steady state or transient disturbances in the primary supply of electric energy, the effects of inadequate and time varying component characteristics on the accuracy of the pulse modulation processes, and the limitation of attainable accuracy of system output control without compromising its needed reaction capability.

Above all, the needed system analysis becomes cumbersome because of

the introduction of techniques that could be characterized by (d) non-uniform sampling processes, such as modulation of the width of trains of periodically reoccurring pulses (PWM), (e) aperiodic sampling processes such as modulation of intervals between pulses of equal width (PFM) and (f) a concurrent combination of the PFM-PFM processes, as indicated before.

The difficulties of analysis with inadequate methods are further compounded by the fact that the actual power pulses do not correspond to the intended control signal, as illustrated in figure 9.

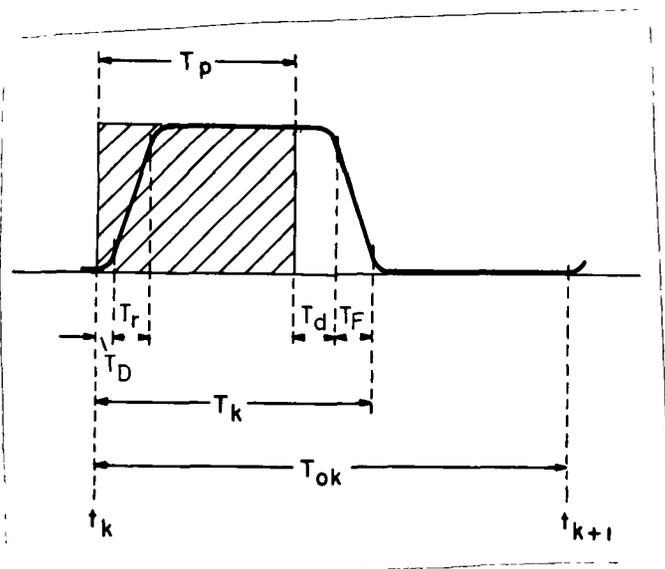


Figure 9.

Preprogrammed (shaded area) and actual pulse.

The preprogrammed "flat top" pulse intended in the time $t_k \leq t \leq t_k + T_p$ and indicated by the shaded area is implemented in the illustrated form in the time interval $t_k \leq t \leq t_k + T_p + T_d + T_f$. Reconciliation of the

discrepancy between the intended and the actual power pulse is attempted by application of feedback techniques, however, at the expense of at least two critical elements consisting of: (1) the addition of gain to the feedback amplifier and thus increasing the hazard of unfavorable dynamic system behavior and (2) an inadequate dynamic response capability due to the need for iterative adjustments to changing operating conditions where each iteration is delayed by the time constants of the system output filter. The block diagram of a representative pulse modulator with type 0 feedback control is indicated in figure 10 for clarification of the discussion.

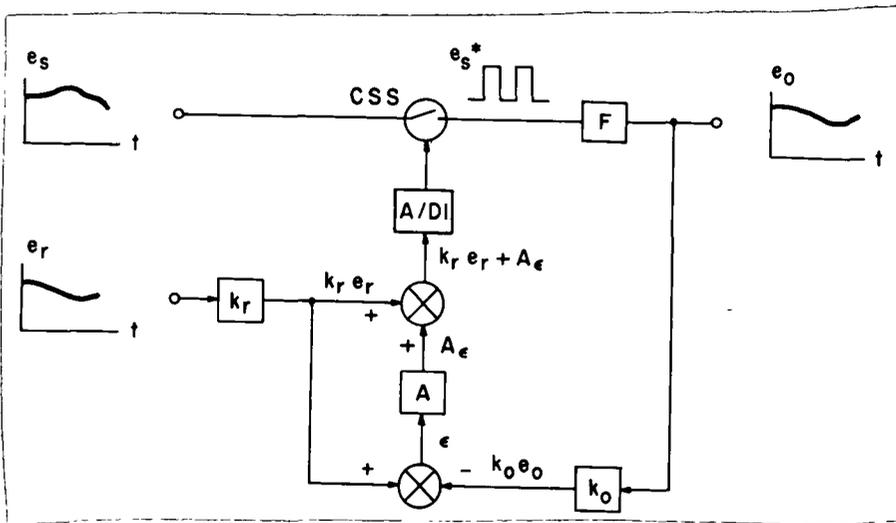


Figure 10.

Block diagram of pulse modulator with type 0 feedback control mechanism.

Each correction on the individual pulses of the pulse train e_s^* has to travel over a finite (and appreciable) time interval through low pass

filter F before influencing the feedback network and causing one of the iterations in response to a disturbance as referred to above.

The adverse effects of this time consuming procedure of adjustment are self evident. They compound the inherently existing dynamic stability problem of these systems.

It is, in conclusion, pointed out that almost any feedback system with purely passive load can be "stabilized" by unrestricted application of damping in form of (RC) delays of the feedback signal. However, this occurs at the expense of the reaction capability of the system. The impairment of this capability is, usually, incompatible with the intended use of the system, which as a rule does not energize a purely resistive and time invariant load.

3. Objectives.

Reconciliation of the ~~apparently conflicting~~ characteristics of adequate static and ~~dynamic behavior~~ respectively was the motivation for the development of an alternative method of pulse modulation control.

The primary objective is to eliminate the time delay caused by the output filter when processing signal e_s^* for purpose of its transformation to e_o . This signal e_o should be available undelayed when e_s^* is being formed.

A secondary objective is to utilize the actual pulse waveforms as discussed with reference to figure 10 as information for the control process rather than to pretend the existence of fictitious ideal rectangular pulses for purpose of implementing actual control functions.

III. THE D.C. CONVERTER WITH CONVENTIONAL FEEDBACK CONTROL.

The current state of the art of d.c. converter control is discussed first to provide a reference system for the presentation of more advanced control concepts and technology.

1. Principles of Control.

The filter of an electronic d.c. converter, such as a series chopper illustrated in figure 6 is, usually, designed to attenuate the harmonic content caused by the chopping process

$$e_s^* = a_0 + \sum_{m=1}^{\infty} a_m \sin(m\omega_F \tau + \psi_{Fm}) \quad (3.1)$$

to remain within acceptable and specified limits, as indicated with reference to (2.3) and illustrated in figure 3. The conventional chopper and its control system is illustrated in figure 11. Its "equivalent" presentation in form of a conventional control system is shown in figure 12. The chopping function is simulated by introducing $e_{sac}^* = e_s^* - e_{sav}^*$ as disturbance $D(\tau)$ into the shown port. The low frequency component e_{ac} of e_s is considered to be zero for purpose of this consideration.

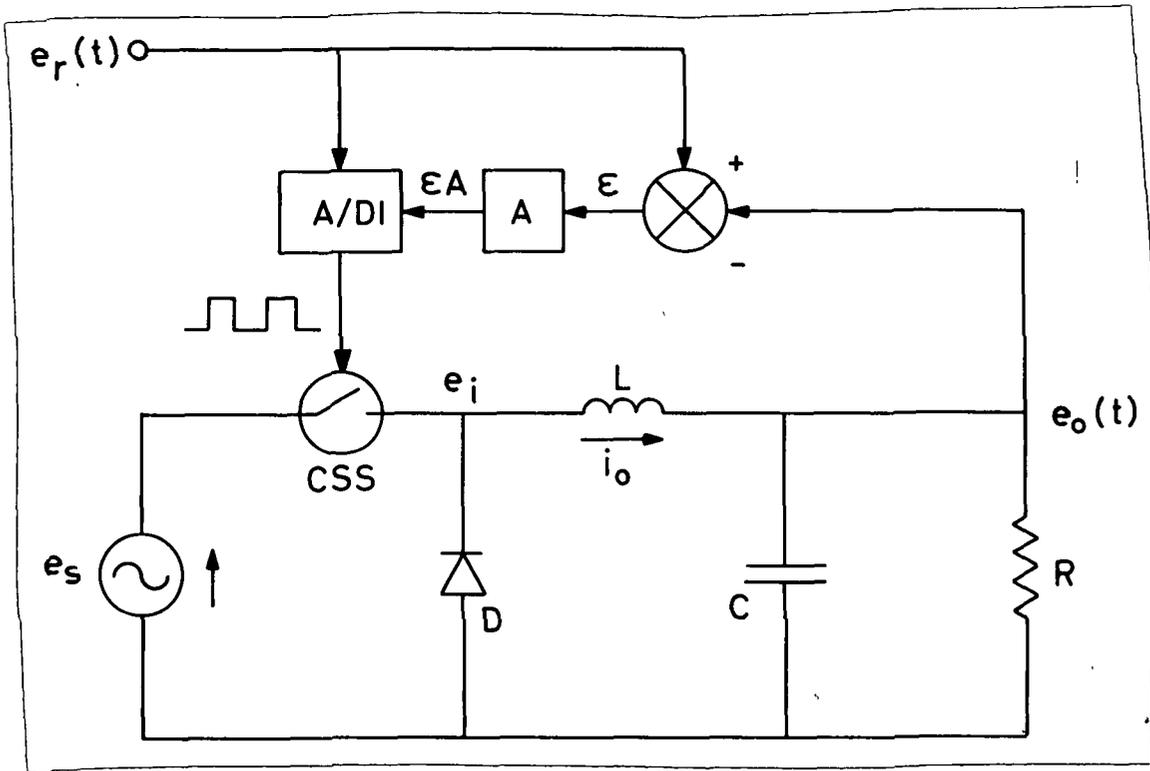


Figure 11.

Symbolic diagram of series chopper regulator and its control mechanism.

The attenuation a_{Fm} of the m th harmonic component of e_s^* by such a filter within a feedback controlled chopper system illustrated in figure 11 is given by (see figure 13).

$$a_{Fm} = (m\omega_F/\omega_0)^2 \left\{ \left| (1 + A)(\omega_0/m\omega_F)^2 - 1 \right|^{\frac{2}{3}} + \left| 2\xi\omega_0/m\omega_F \right|^2 \right\}^{\frac{1}{2}} \quad (3.2)$$

where

$\omega_F = 2\pi f_F$ and f_F is the pulse (chopping) frequency

$\omega_0 = 1/\sqrt{LC}$ being the undamped resonant filter frequency

$\xi = \sqrt{L/C}/2R$ being the damping constant of the load terminated filter

A = gain of the feedback loop

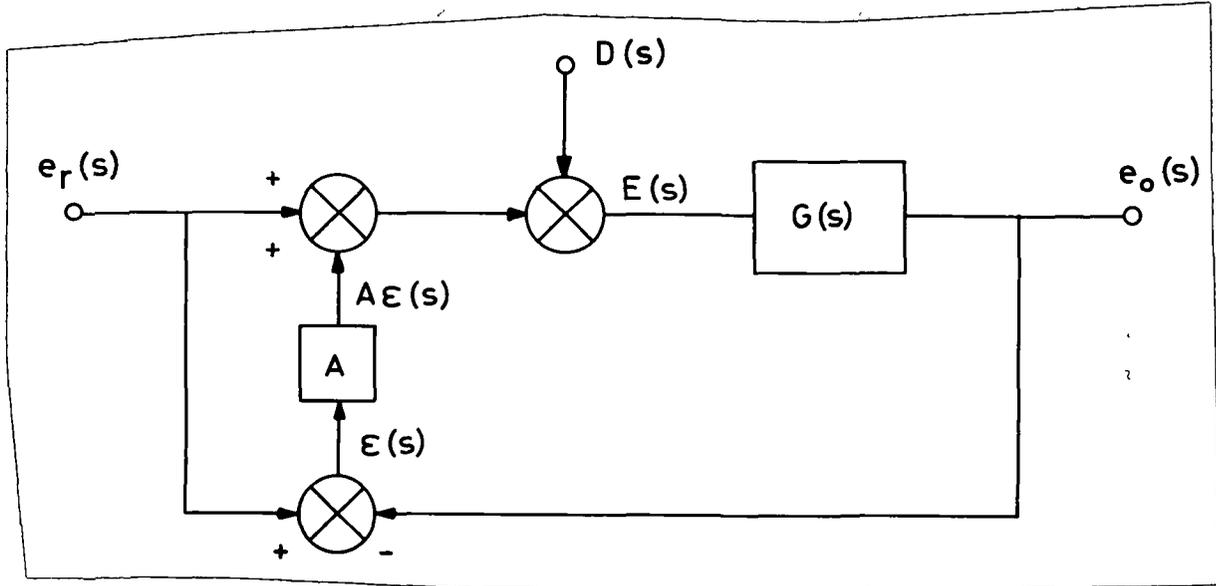


Figure 12.

Symbolic diagram of d.c. feedback converter with "Disturbance" $D(t)$:

Since $a_2 < a_1$ in (3.1) for any usual "duty cycle" T_k/T_{ok} and a_{Fm} increases roughly with the square of $m = 1, 2, \dots$, it follows that the first high frequency (f_F) harmonic component of e_s^* dominates the magnitude of the hf ripple of e_o as indicated in (2.7).

The amplitude V_{oF} of the hf ripple of e_o is, therefore,

$$V_{oF} \approx V_{oF1} = a_1/a_{F1}$$

The magnitude of the transfer function of the same chopper feedback

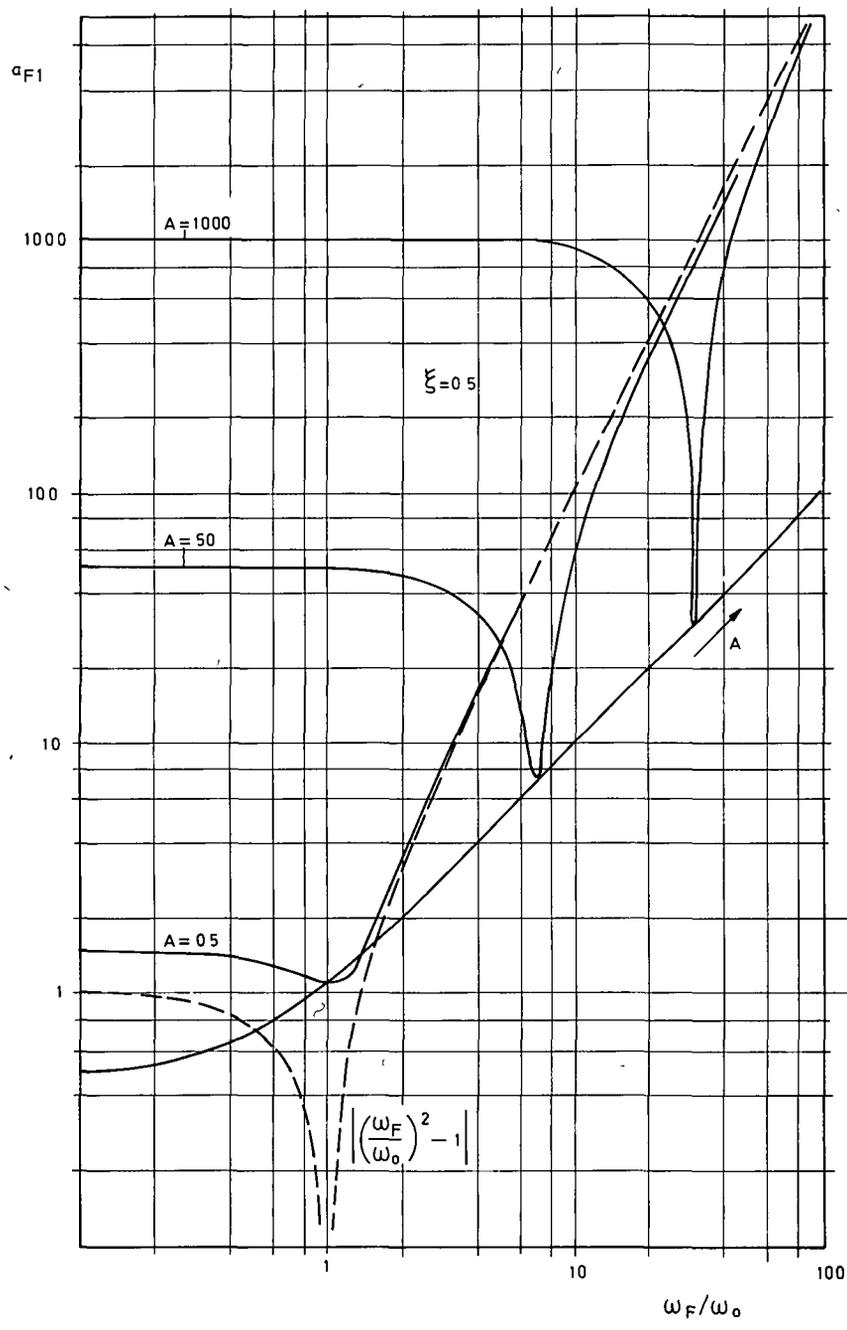


Figure 13.
 Attenuation of the first harmonic component of the
 chopping waveforms $D(t)$.

system is given by

$$\frac{1}{a_{F1}} = \frac{(\omega_o/\omega_F)^2}{\{ |(1+A)(\omega_o/\omega_F)^2 - 1|^2 + |2\xi\omega_o/\omega_F|^2 \}^{1/2}} \quad (3.3)$$

It is seen that this relation increases appreciably and indicates instability unless

$$(1+A)(\omega_o/\omega_F)^2 \ll 1 \quad (3.4)$$

which puts a limit on A for a given ω_o/ω_F . Peaking of $1/a_{F1}$ can be also avoided if $(1+A)(\omega_o/\omega_F)^2 \gg 1$ such as 2 or more. It can be shown, that an undesirable condition involving the phase shift of v_F would occur. The inequality (3.4) imposes, therefore, the indicated restriction. Both, ω_o is limited by size, weight and efficiency of filter components, and ω_F is limited by an efficient operation of the switching electronic components.

The attenuation a_{sn} of the low frequency harmonic content e_{ac} of e_s stated in (2.2) by the same system, and for analogous reasons, especially, that of first harmonic component indicated in (2.6) is given with good approximation by

$$a_{s1} = E_{s1}/V_{os1} \approx A \quad (3.5)$$

The capability of the system to suppress a low frequency (line) ripple is limited by the bounds imposed upon A by the effects of the chopping operation as evident in (3.4). Such a system can, therefore, not per-

form well the suppression of a low frequency harmonic content of e_s unless a high ratio ω_F/ω_0 is used, which in turn is bounded by physical limitations. An analogous argument applies for the system response to the low frequency content of step changes in the source voltage e_s . High frequency, f_{hf} , disturbances of e_s will be attenuated by the system following relation (3.2) when ω_F is replaced by ω_{hf} .

2. Limitations.

The significant physical limitations of the conventional feedback controlled d.c. converter originate in:

- a. the discrepancy between the signal which is being applied to the electronic power switch (CSS) and the resulting pulse voltage. This is illustrated in figure 9 in a semi-idealized form, and presented resembling to its real appearance in figure 14.

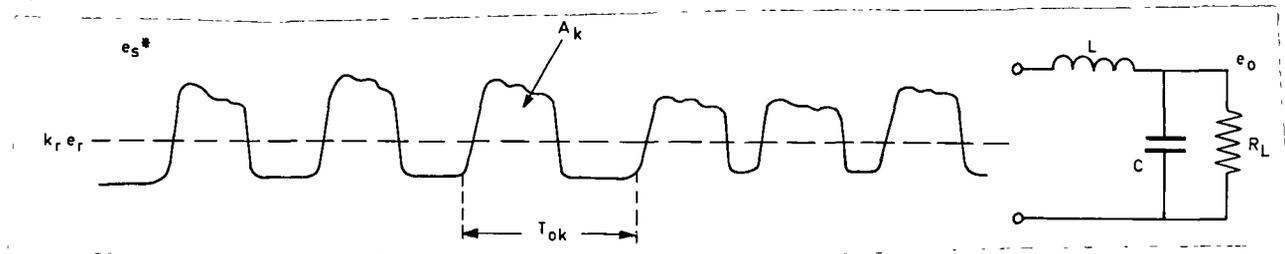


Figure 14.

Irregularly shaped form of actual pulse train e_s^* with property $A_k/T_{ok} = k_r e_r$, entering converter output filter.

- b. the need to engage the feedback control systems to reduce all errors ϵ_p in output voltage e_o illustrated in and discussed with reference to figure 3; the largest possible feedback gain A is required for that purpose.

- c. the risk of subharmonic oscillations (instability) if the feedback loop gain A is enlarged beyond the limitations imposed by (3.4), and the therefore
- d. enforced tolerance of variation of the system output voltage e_o from its nominal value E_o or
- e. the slow down of the reaction capability of the system below the various modes of subharmonic oscillation frequencies if a large feedback gain A is required, which compounds the problems of reaction to step changes in source voltage and loading.

Application of feedback stabilization techniques leads, in general, only to modest improvements of the system's dynamic behavior. It is difficult to move two complex conjugate poles ~~in the complex plane~~ to the left, by introduction of poles ~~and zeros on the~~ real axis, thus by use of "lead-lag" feedback networks. ~~Tuning out of poles~~ by superposition of zeros and creation of ~~new~~ poles further to the left in the complex plane is possible by use of bridged T filters [5]. The effectiveness of this approach is limited by the temperature dependence of filter components, especially the capacitors; the system becomes easily untuned and its dynamic behavior deteriorates accordingly.

IV. DEFINITION AND DESIGN EQUATIONS FOR THE USE OF DETERMINISTIC PULSE MODULATION (DPM) TECHNIQUES.

A method was devised which forms a train of actual power pulses in a specific manner: when impressed upon a non-dissipative low pass filter, than the output of that filter will behave in a predetermined manner without a need in principle to utilize the filter output signal for application of corrective measures. This method distinguishes itself from the conventional forms of pulse modulation, where a pulse of nominal width is programmed and this width is then modified by a feedback signal consisting of the amplified error ϵ between the reference signal e_r and the output voltage e_o . The designation of the presented method as deterministic pulse modulation is derived from this distinction.

The method applied for the purpose under consideration, its targets of achievements, and its limitations will be described in a qualitative manner. Sufficient information on quantitative results will be provided to allow the treatment of technical mechanisms which embody a functional philosophy governed by this method. A detailed quantitative treatment of the material under this chapter IV is not presented as explained under I.2.

A reconciliation of the requirements of (2.16) related to "well behaved" rectangular flat top pulses with the type of pulses shown in figure 14 is achieved if:

$$k_r e_r T_{ok} = \int_{t_k}^{t_{k+1}} e_s^* dt \quad (4.1)$$

The question arises: if in the time interval $t_k < t < t_{k+1}$

$$e_s^* \neq e_s$$

as is the case in actual power electronics converters, and if

$$de_s/dt \neq 0 \quad \text{at times or at all times}$$

what is the effect on e_o defined in (2.3)? Or rephrased: What pulse modulation process has to be applied to transform the source voltage e_s as defined by (2.2) via an actual pulse train e_s^* as shown in figure 14 and with the limitations indicated in figure 9, into a converter output voltage e_o defined by (2.3) and illustrated in figure 2, within the limitations associated therewith?

1. The Objectives of DPM.

These objectives are stated as:

- a. "generation of a pulse train $e_s^*(t)$ derived from a source voltage e_s in such a manner that all harmonic coefficients E_{sn} of e_s indicated in (2.4) and with order number $n < n_c$ are reduced in magnitude below a prescribed level; the order number n_c corresponds to the cut off frequency of the filter which accepts the pulse train."

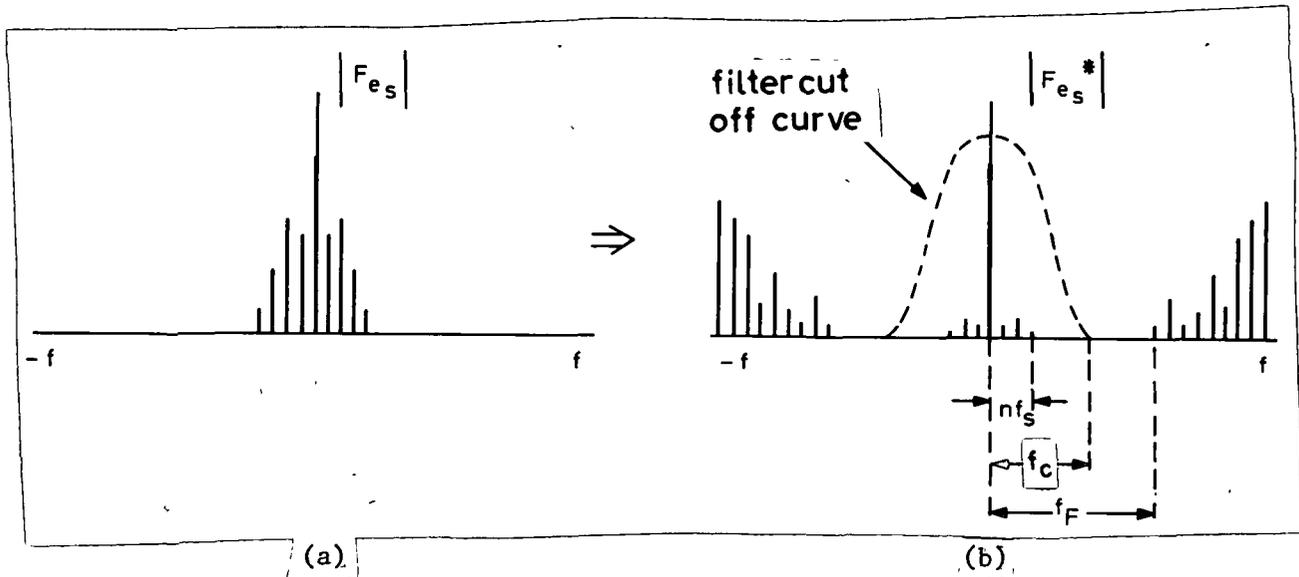


Figure 15.

Frequency spectrum of (a) source voltage e_s ; (b) samples e_s^* of figure 14. The vertical scale of line frequency spectra should be assumed to be logarithmic.

This intended purpose is illustrated (see figure 15) in form of the frequency spectrum of e_s and that of the therefrom derived train of pulses e_s^* . The spectral lines of e_s indicating the magnitude of the harmonic coefficients with frequency $nf_s < n_c f_s = f_c$ are reduced by the pulse modulation process itself before the pulse train e_s^* enters the low pass filter as illustrated in figure 14. The filter then removes the high frequency components of e_s^* with order number $n > n_c$; it follows that only the in size reduced remnants of the original frequency components of the source voltage e_s appear as components of the system output voltage e_o .

b. a continued retention of a constant average value of e_s^* as stated with (2.4) under all static and dynamic conditions of converter systems operation.

The underlying principles of this transformation $e_s \rightarrow e_o$ are discussed in the following section.

2. The Harmonic Content of a Train of Samples (Pulses).

If a function e_s with the frequency spectrums $|F_{e_s}|$ as shown in figure 16(a) is uniformly and periodically sampled with a sampling frequency f_F , then its frequency spectrum will repeat itself indefinitely in frequency intervals f_F as indicated in figure 16(b) [6].

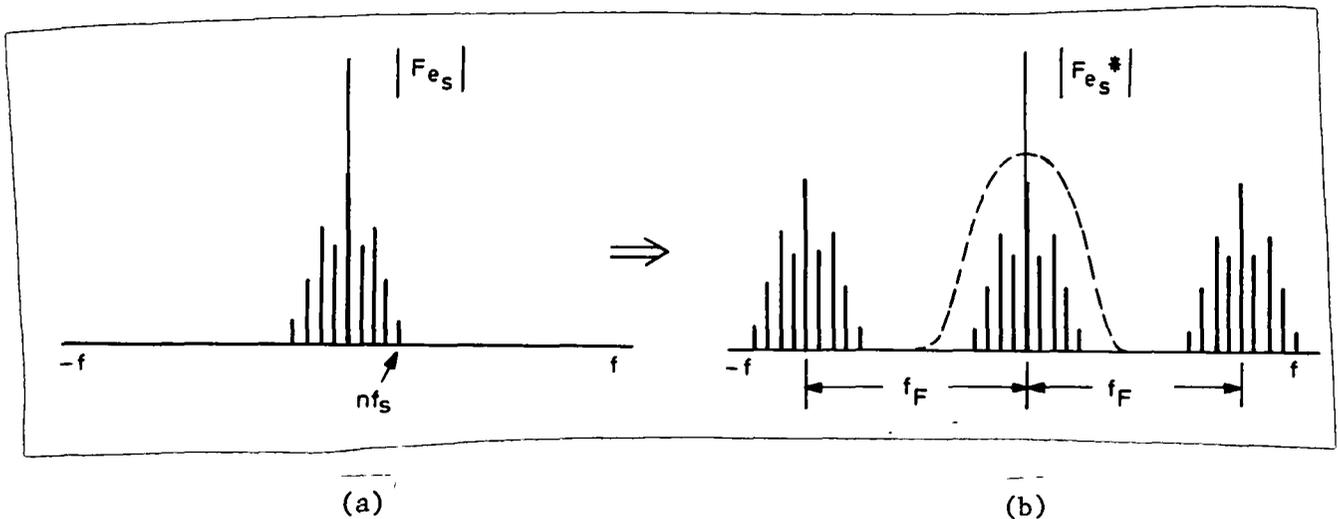


Figure 16.

Frequency spectra $|F_{e_s}|$ of the source voltage e_s and $|F_{e_s}^*|$ of a train of uniform and periodic samples thereof.

If, however, (the Fourier transformable) function e_s as illustrated in figure 17 is sampled in a nonuniform and/or aperiodic way, then the frequency spectrum of the ensuing train of samples within the limited band $-f_c < f < f_c$ is altered and neither the original spectrum of e_s nor that of e_s^* repeats itself at any frequency interval of the spectrum. There are spectral lines located outside the indicated band

limits, as illustrated in figure 15(b); they are of little significance for the intended transformation, since they are cut off by the low pass filter indicated by a dotted line in same figure.

Pulse width modulation such as discussed with reference to figure 5(c) can be characterized as a nonuniform periodic sampling process. Such a process is illustrated in figure 17. This is, however, an idealized

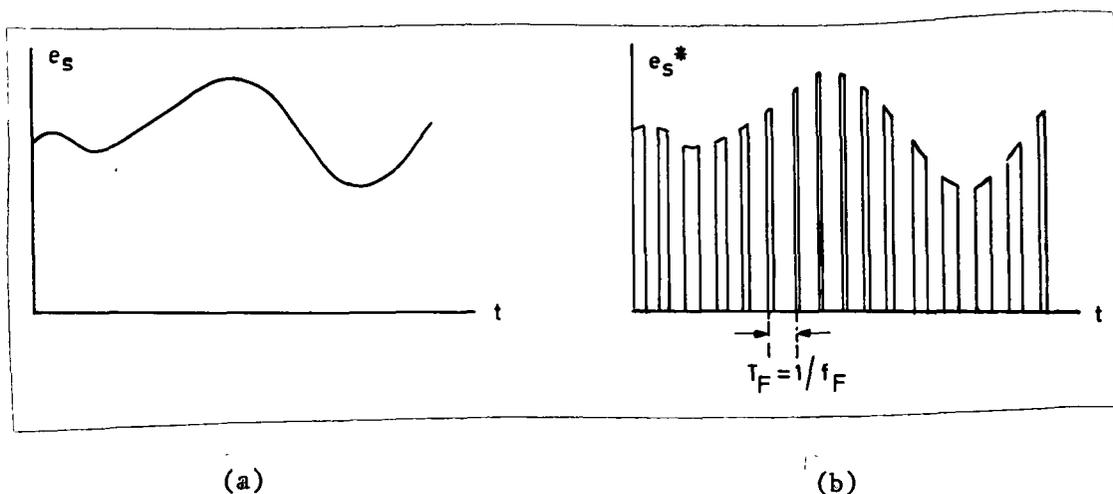


Figure 17.

Source voltage e_s and the therefrom derived train e_s^* in width modulated pulses.

presentation as is recalled from study of figure 14. The argument will be made that although the energy for generation of the secondary voltage source e_o is derived from the source of electric energy with voltage e_s , it is not necessary that $e_s^*(k) = e_s(t_k < t < t_k + T_k)$ in order to satisfy relation (4.1). In other words $e_s^*(t)$ which derives its voltage from e_s need not have any resemblance to e_s as long as it fulfills other requirements such that the prescribed transformation of $|F_{e_s}| < |F_{e_s^*}|$

is attained for every line of the spectrum within the band limit $-f_c < f < f_c$ governed by the low pass filter.

The preceding statement is discussed with reference to figure 18. Several pulses of a train e_s^* are shown, with individually different form, shape and pulse areas A_k , and apparently, derived from an

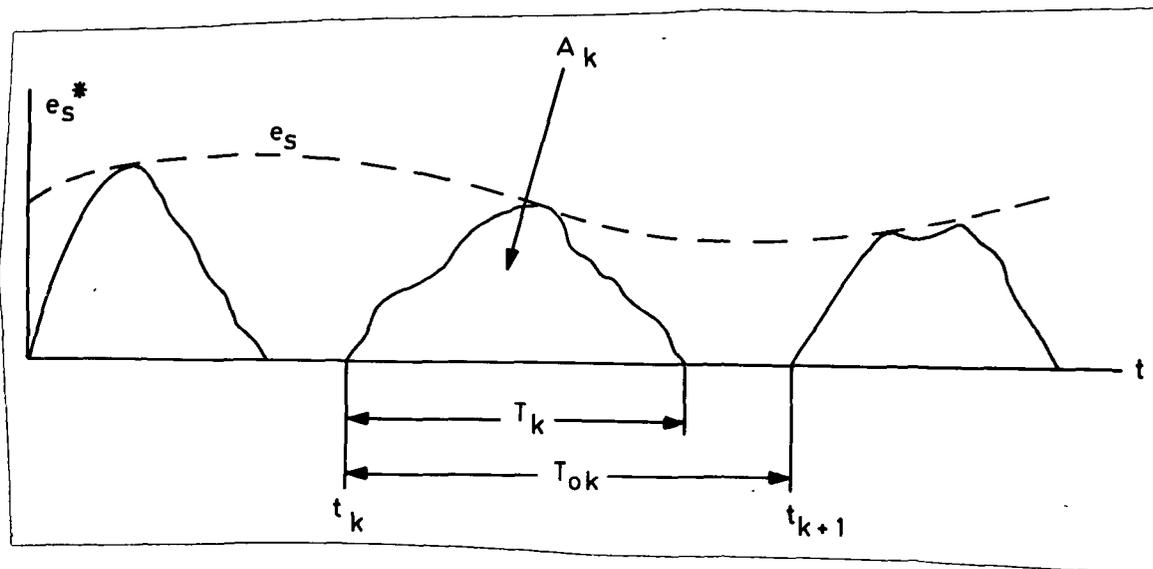


Figure 18.

Irregularly shaped samples e_s^* of source voltage function e_s .

envelope e_s . A number of characteristics of this pulse train are significant. The pulse train e_s^* contains frequency components related to:

- its average value (zero frequency component) according to relation (4.1);
- its envelope e_s ;
- its sampling frequency f_F , or of its sampling frequency band $f_{F \max} - f_{F \min}$, if frequency modulated;

d. the shape and the location of the individual pulses.

The frequency components indicated under c. and d. are, apparently, of no practical interest because they are outside the filter cut off band limit. However, the shape of the individual pulses is entirely irrelevant, as long as (4.1) is satisfied, which in turn satisfies a. above. This means that from that point of view these pulses could have - mathematically speaking - any shape including rectangular shapes or that of impulses. This last form is very convenient for mathematical operations and is therefore chosen to discuss the transformation of the frequency components emanating from the source voltage e_s to conform to the limitation specified for e_o , concurrent with satisfaction of (4.1).

It is consistent with the preceding statement d. that a train of rectangular pulses e_i^* shown in figure 19 can replace the pulse train e_s^* shown in figure 18 as long as the respective individual pulse areas A_k and the thereto relate pulse intervals T_{ok} are equal in magnitude with those illustrated in figure 18.

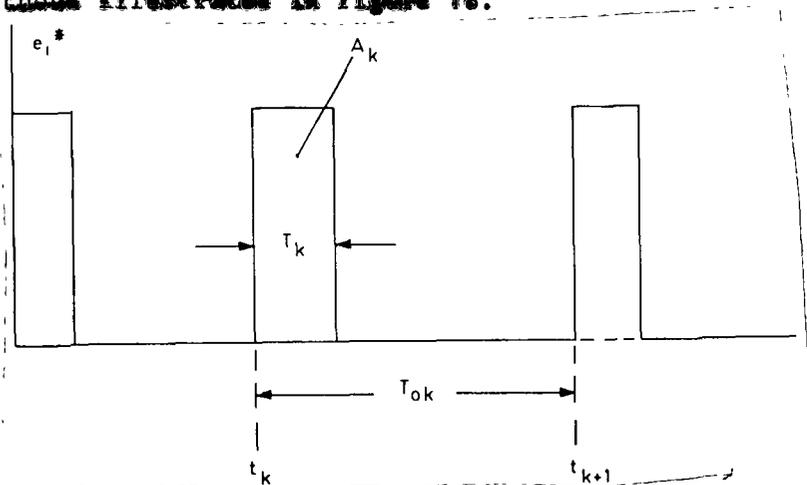


Figure 19.

Rectangular pulses e_i^* with band limited ($-f_c < f < f_c$) frequency spectrum that is identical with e_s^* shown in figure 18.

It was implied above that the effects caused by the sampling frequency f_F lie outside the filter cut off limit. This interpretation of statement c. has only limited validity. There are two types of effects caused by the sampling process that should be distinguished. These are the effects caused by:

- c1. the mechanics of sampling and the therewith associated harmonic components with frequency $f > f_c$, and
- c2. the sampling mode and rate which reflect themselves into the harmonic components with frequency $f < f_c$, even though the pulse train satisfies the requirements of (4.1).

The first statement c1. is self evident for $f_F > f_c$.
The last statement c2. is further clarified.

First, the objectives of the sampling process are recalled with reference to the discussion associated with figure 3. These objectives can be restated in the idealized form that the individual volt-second areas B_k of the system output voltage e_o in the time intervals T_{ok} should have the property

$$E_o = B_k / T_{ok} = A_k / T_{ok} \quad (4.2)$$

with the tacit assumption that

$$A_k = \int_{\tau_k}^{\tau_{k+1}} e_s^* dt \quad (4.3)$$

and (4.1) is satisfied for every closed time interval T_{ok} . The areas B_k are required to have (1) the appropriate average value and (2) a

harmonic content that falls within the limits discussed with reference to figure 3. A sketch of areas B_k within intervals T_{ok} is shown in figure 20 with some exaggeration of the indicated harmonic content for purpose of illustration.

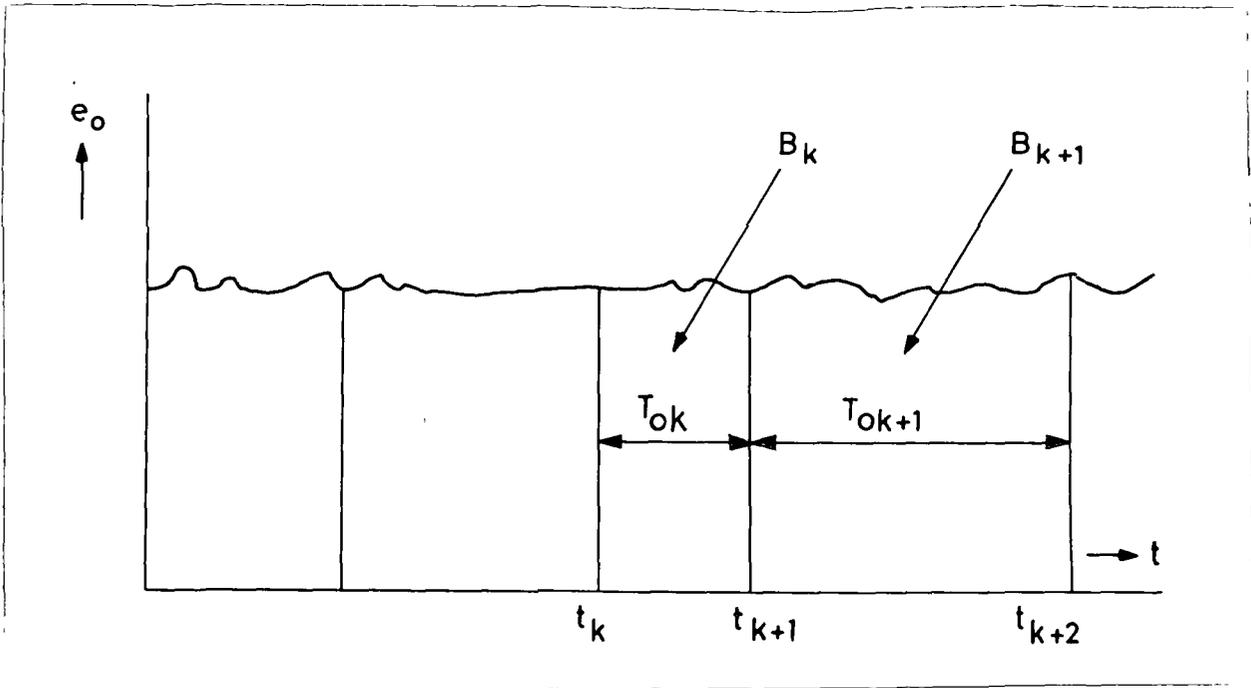


Figure 20.

Output voltage e_o at filter termination with $B_k/T_{ok} = B_{k+1}/T_{ok+1}$.

For purpose of the following argument it is assumed that the system output filter does not attenuate the harmonic components of e_s^* with frequency $f < f_c$. The mechanism by which the sampling process transforms the frequency spectrum of the sampled function e_s is discussed next.

3. The Spectral Transformation Process.

The transformation

$$e_s(t) \rightarrow e_o \quad (2.1)$$

is accomplished by sampling e_s in such a manner that

- (a) (4.1) be satisfied over every closed time interval T_{ok} , and
- (b) all low frequency harmonic component $V_{osn} \sin(n\omega_s t + \psi_{sn})$ in (2.5) fall within the limit discussed with reference to figure 3.

Attainment of condition (a) appears, at least in principle, plausible. Condition (b) would require, that all V_{osn} fall within these limits, preferably, approaching zero.

The necessary requirements for attainment of these conditions will be stated, and the quantitative results given without proof, as cited in I.2.

A normalized source voltage function

$$e_{i1} = 1 + m_i \sin \theta \quad (4.4)$$

and the therefrom derived train of samples

$$e_{i1}^*(\beta) = \sum_{k=1}^{\infty} Q e_{i1}(\beta_k) \delta(t - t_k) \quad (4.5)$$

as illustrated in figure 21 are considered first. Q is an arbitrary con-

stant and will be defined further on.

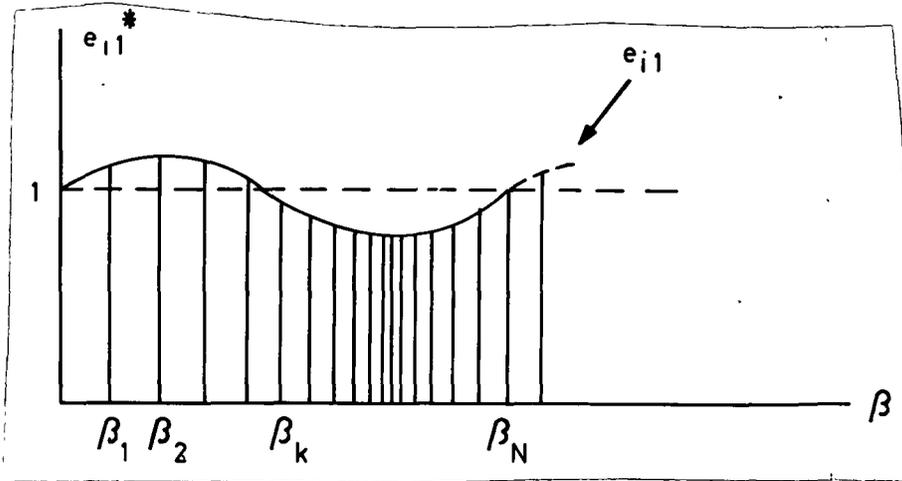


Figure 21.

Pulse frequency mode sampled function e_{i1} .

The index 1 of e_{i1} indicates that only the first harmonic component of a function e_i containing a number of such harmonic components is being considered. The ensuing results can be expanded to cover the other harmonic components of that function by application of the principle of superposition.

Function e_{i1} , as defined in (4.4) is normalized to (1) an average value of unity, (2) a first harmonic frequency of $1/2\pi$ and (3) a modulation index $m_i \ll 1$. A modulation index $m_i > 0.5$ would not address itself in a meaningful way to the technical problem at hand. The results are, of course, applicable to any problem of that kind.

a. An Aperiodic Uniform Sampling Process (PFM).

A number of N samples is chosen for each normalized time period of

2π seconds. The samples succeed each other in time intervals $\Delta\beta_k$ such that

$$\beta_k = \sum_{j=1}^{k-1} \Delta\beta_j$$

analogous to (2.10). Pulse train (4.5) can be rewritten in form of an ordinary complex Fourier series

$$e_{i1}^*(\beta) = \sum_{n=-\infty}^{\infty} c_{in}^* e^{jn\beta} \quad (4.6)$$

where the

$$c_{in}^* = \frac{Q}{2\pi} \int_0^{2\pi} e_{i1}^* e^{-jn\beta} d\beta \quad (4.7)$$

It is the objective to choose all time intervals β_k for $k = 1, 2, \dots, N$ in such a manner that all c_{in}^* approach zero for $n \neq 0$, and $c_{i0}^* = 1$. All c_{in}^* with $n \neq 0$ should be at least small enough to meet the required characteristic discussed with reference to figure 3. Constant Q is chosen so that $c_{i0}^* = 1$.

The problem as stated in the preceding paragraph is further elucidated by performing the integration (4.7), using (4.5), resulting in

$$2\pi c_{in}^* = Q \{ e_{i1}(\beta_1) e^{-jn\beta_1} + e_{i1}(\beta_2) e^{-jn\beta_2} + \dots + e_{i1}(\beta_N) e^{-jn\beta_N} \} \quad (4.8)$$

since $e_{i1}^*(\beta_k) > 0$ at instant β_k only.

Letting

$$A_k = Q e_{i1}(\beta_k) \quad (4.9)$$

leads (for $n = 1$) to

$$2\pi c_{i1}^* = A_1 e^{-j\beta_1} + A_2 e^{-j\beta_2} + \dots + A_k e^{-j\beta_k} + \dots + A_N e^{-j\beta_N} \quad (4.10)$$

Relation (4.10) can be represented in vector form as illustrated in figure 22, where $m_i = E_i$. The objective stated with relation (4.7)

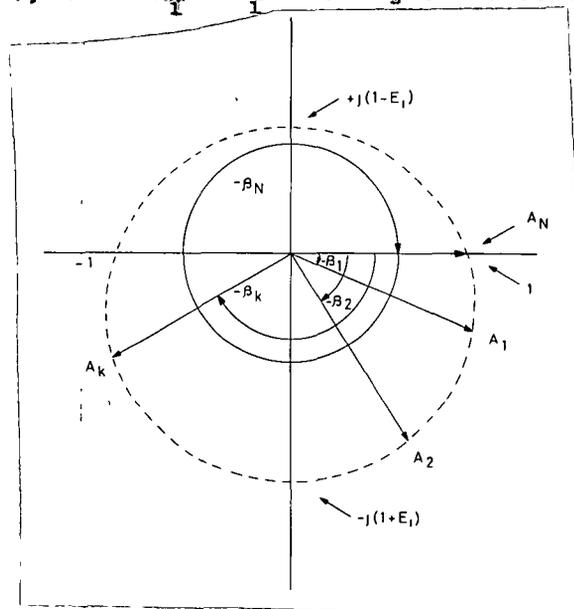


Figure 22.

Vectorial presentation of samples e_{i1}^* shown in figure 21.

requires that the sum of the projections of all vectors A_k on the horizontal and on the vertical axes, respectively, be zero; this objective requires furthermore that the same be true if all angles β_k be doubled, tripled, and so on for $n = 2, 3, \dots$, according to (4.8), whereby the associated A_k remain unaltered in magnitude and the origin be encircled n times by β_N .

A number of N transcendental equations can be formed from (4.8) to calculate the N angles β_k to meet concurrently the stated objectives.

It can be shown (as referred to under I.2.) that a solution of the stated problem exists, requiring that

$$\frac{A_k}{\Delta\beta_k} = \frac{A_{k+1}}{\Delta\beta_{k+1}} \quad (4.11)$$

and that under these conditions the first harmonic component in form of the modulation index $m_i = E_i$ is attenuated by

$$a_{d1} \approx N/\pi \quad (4.12)$$

It can be shown, furthermore, that the higher harmonics of

$$e_{in}^* = 1 + \sum_{n=1}^{n_c} E_{in} \sin(n\beta + \psi_n) \quad (4.13)$$

are attenuated through the described sampling process by

$$a_{dn} = N/\pi n \quad (4.14)$$

The diminishing attenuation a_{dn} of the harmonic coefficients in (4.13) with increasing n is offset by the, usually, even faster decrease of the magnitude of harmonic coefficients of a Fourier transformable function which may describe the source voltage e_s in its normalized form e_{in} . Primary attention is therefore given to the attenuation a_{d1} of the first harmonic component E_{i1} .

Examples of the effectiveness of this process of pulse modulation are presented in a number of graphs which follow. Figure 23 illustrates the frequency spectrum of the periodically sampled function $e_{in} = e_{i1}$ as defined in (4.4), the magnitude of spectral lines being indicated by $|F_{e_{i1}}^*|$. In this case is $c_{i1} = c_{i1}^*$, the c 's being the first harmonic coefficients of e_{i1} and e_{i1}^* , respectively. The following figure 24 shows the frequency spectrum $|F_{e_{i1}^*}|$ of an aperiodical train of samples generated in accordance with (4.8) and (4.11). It is seen that the first harmonic component of e_{i1} with relative magnitude $m_i = 0.1$ was reduced in accordance with (4.12); yet other spectral lines of appreciable magnitude were generated at the order number of frequencies $n = f/f_s = 50$. The indices p and a refer to periodic and aperiodic sampling processes, respectively. The subscript n of e_{in} signifies the normalization of the function.

The advantage of the described process demonstrates itself in form of a frequency shift of the required filter cut off boundary, which was moved from $f_{cp} < f_s$ to $f_{ca}/f_s \approx 40$. If it is, furthermore, realized that the cut off frequency of a simple LC filter as indicated in figure 15(b) decreases with the square of the order number n of the spectral lines, then one significant aspect of the effectiveness of the applied powerful tool reveals itself distinctly; the requirements for a filter to attenuate low frequency line disturbances (line ripple) are, therewith, drastically reduced in electrical

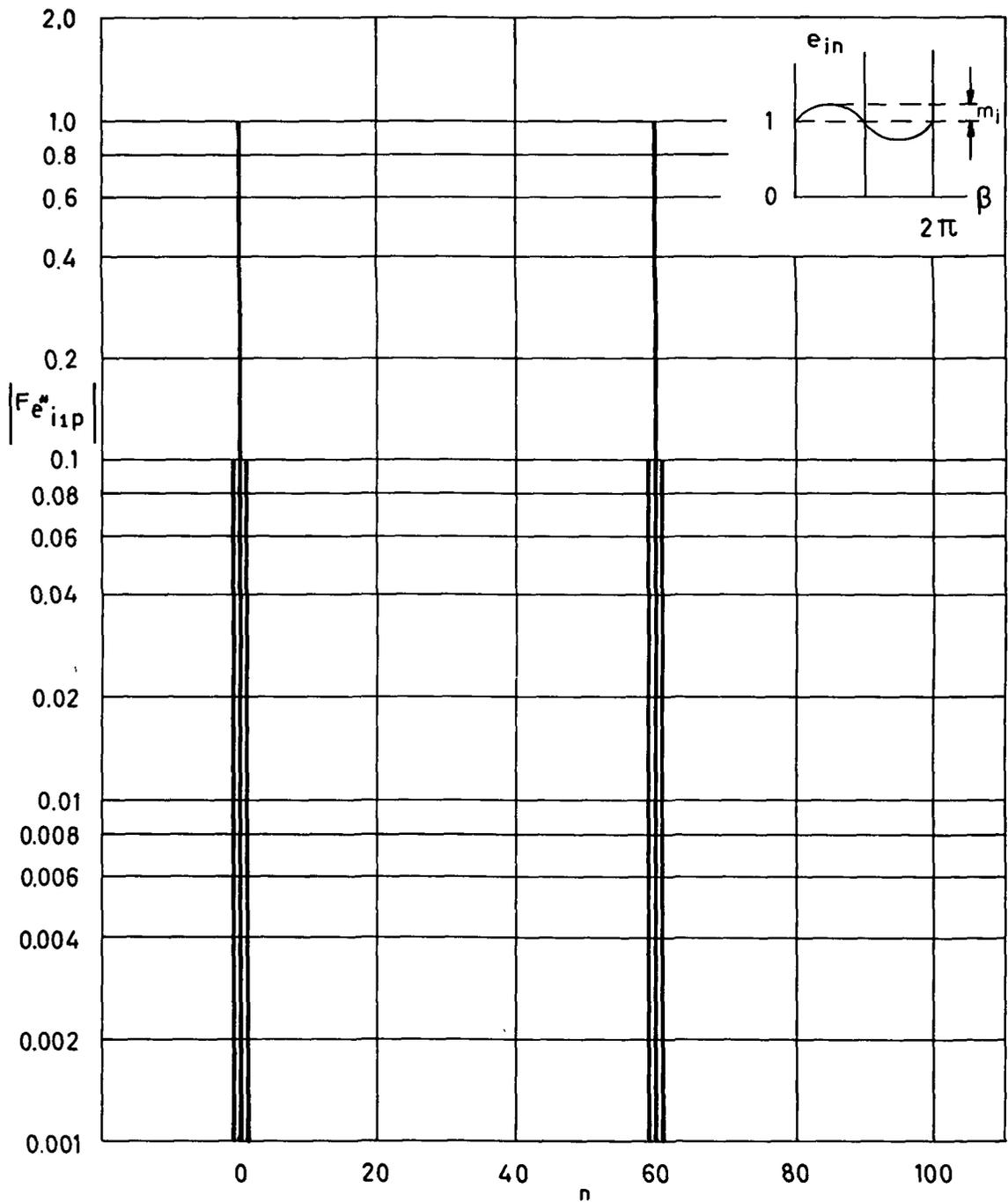


Figure 23.

Frequency spectrum of the periodically sampled function shown above;

$m_i = 0.1$.

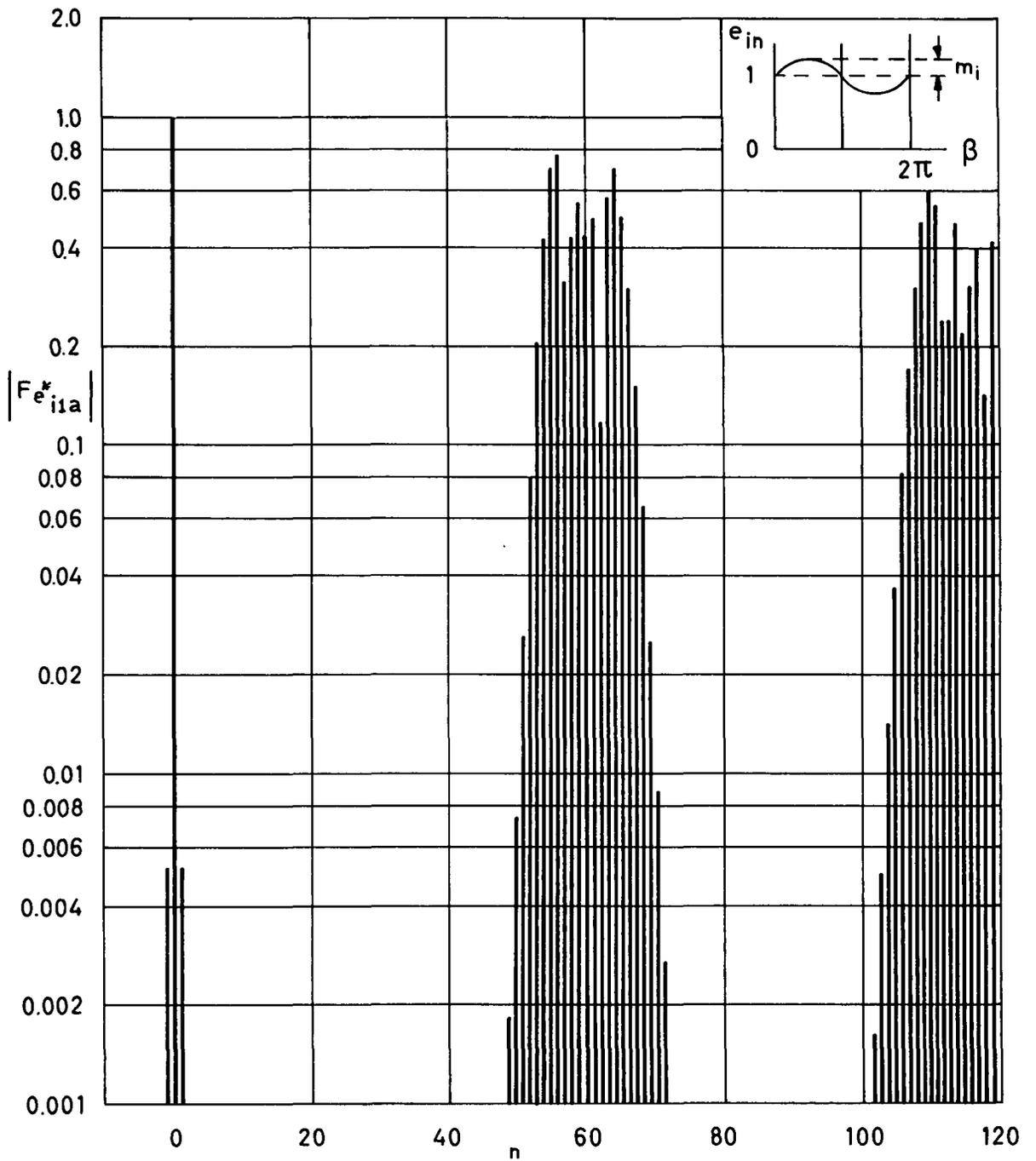


Figure 24.

Frequency spectrum of the aperiodically sampled function shown above;
 $m_i = 0.1$, $N = 60$.

values and, therefore, both in weight and in size.

The significance of the described process is rooted in the fact that the band limited ($-f_c < f < f_c$) spectral content of the original source voltage function e_s is transformed by the sampling process itself before even entering the low pass filter. This filter removes only the high frequency components caused by the mechanics of the sampling (pulse modulation) process as referred to under cl. above.

A further insight into the effectiveness of this process is gained by analysis of another wave form with a more extended harmonic content, such as

$$e_{in} = 1 + (-1)^h g(\beta) \quad (4.15)$$

where

$$g(\beta) = \begin{cases} m_i & \text{for } \pi h < \beta < \pi(h + 1) \\ 0 & \text{everywhere else} \end{cases}$$

and

$$h = 0, 1, 2, \dots$$

$$2h = k = 0, 1, 2; \text{ each } k \text{ is related to one cycle of } e_{in}.$$

The frequency spectrum of the periodically taken uniform samples of this function is shown in figure 25. The same function is then sampled in an aperiodic manner ($N = 500$) such as discussed with

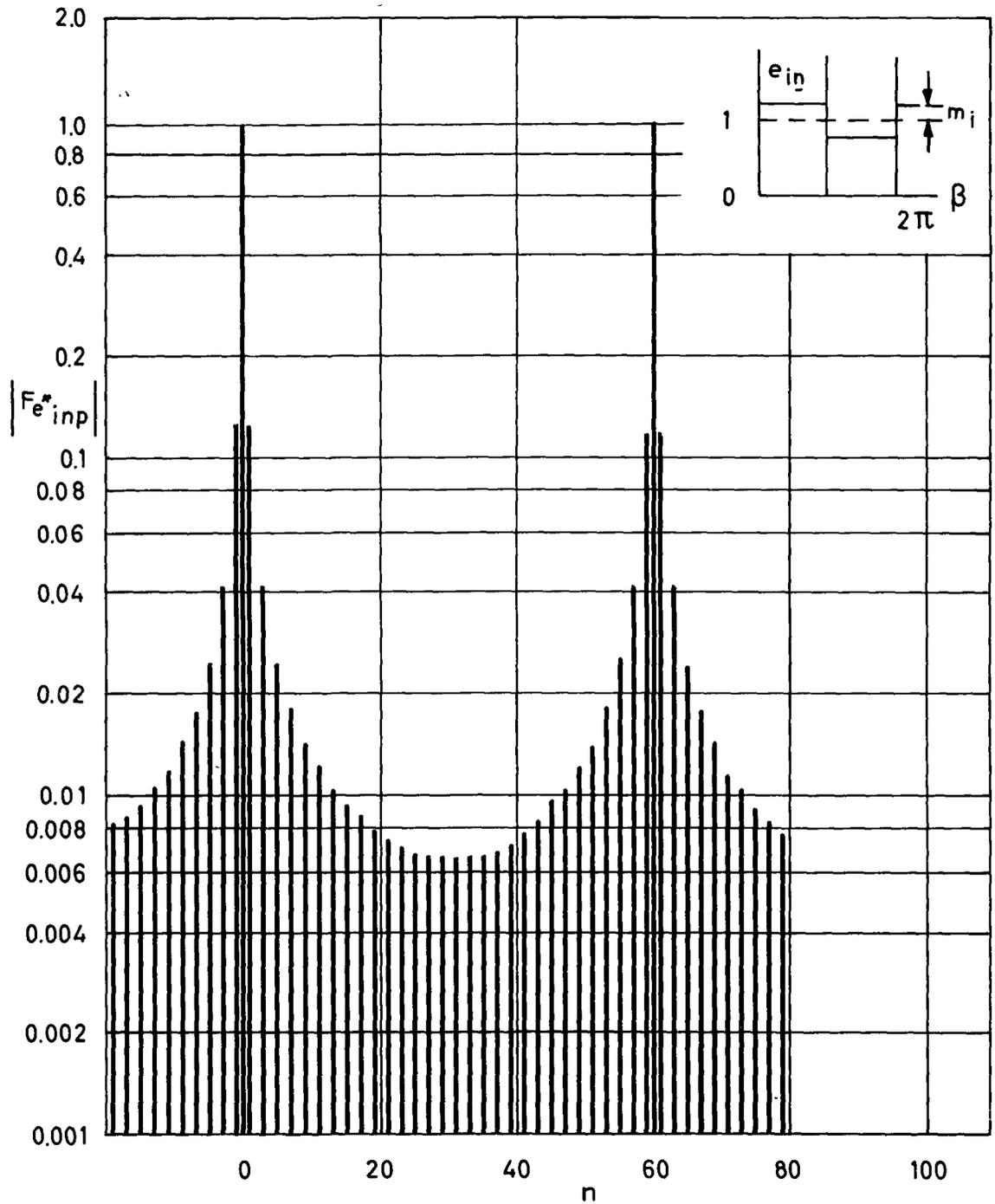


Figure 25.

Frequency spectrum of the periodically sampled function above; $m_i = 0.1$, $N = 60$.

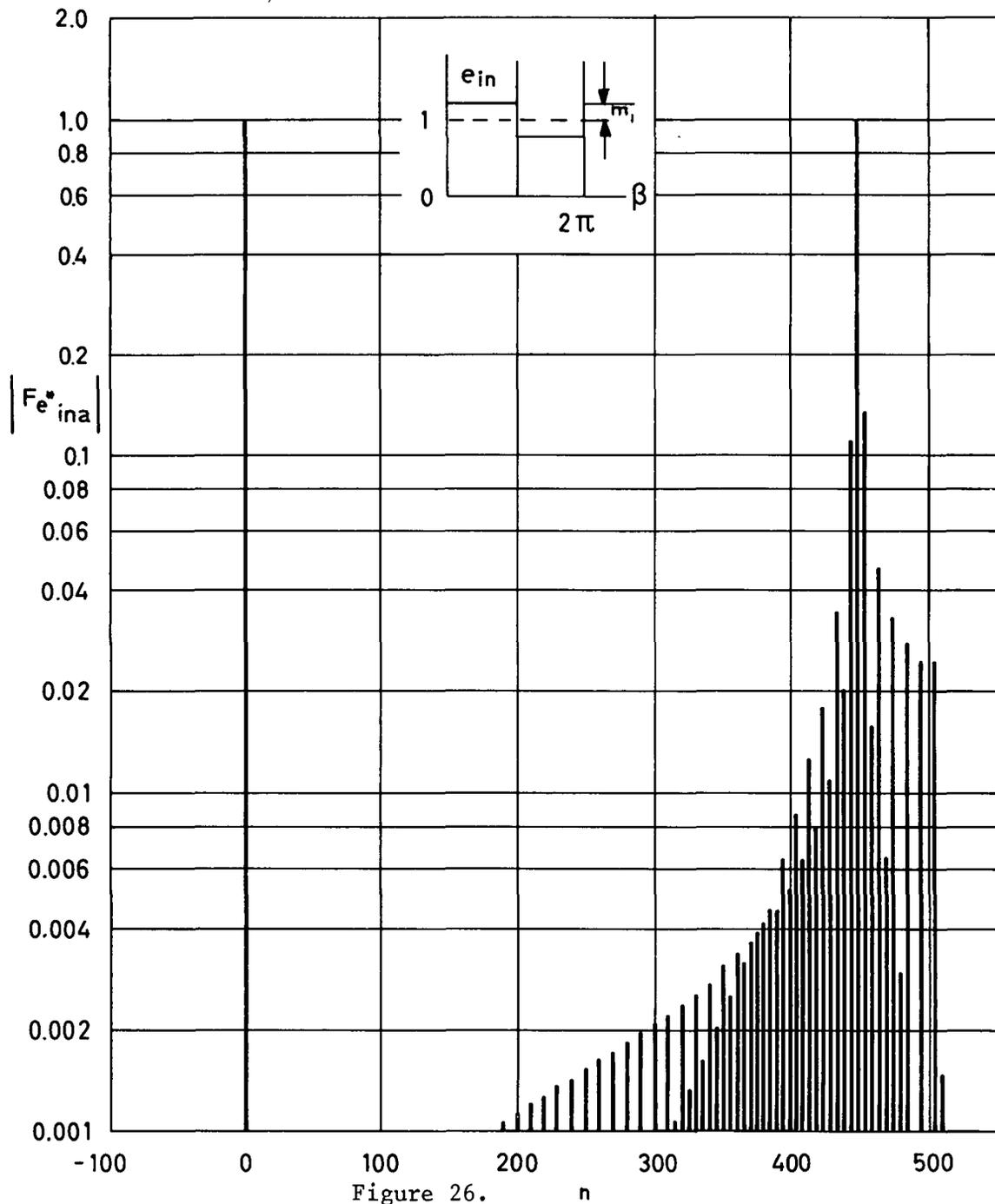


Figure 26.

Frequency spectrum of the aperiodically sampled function shown above;
 $m_i = 0.1$, $N = 500$.

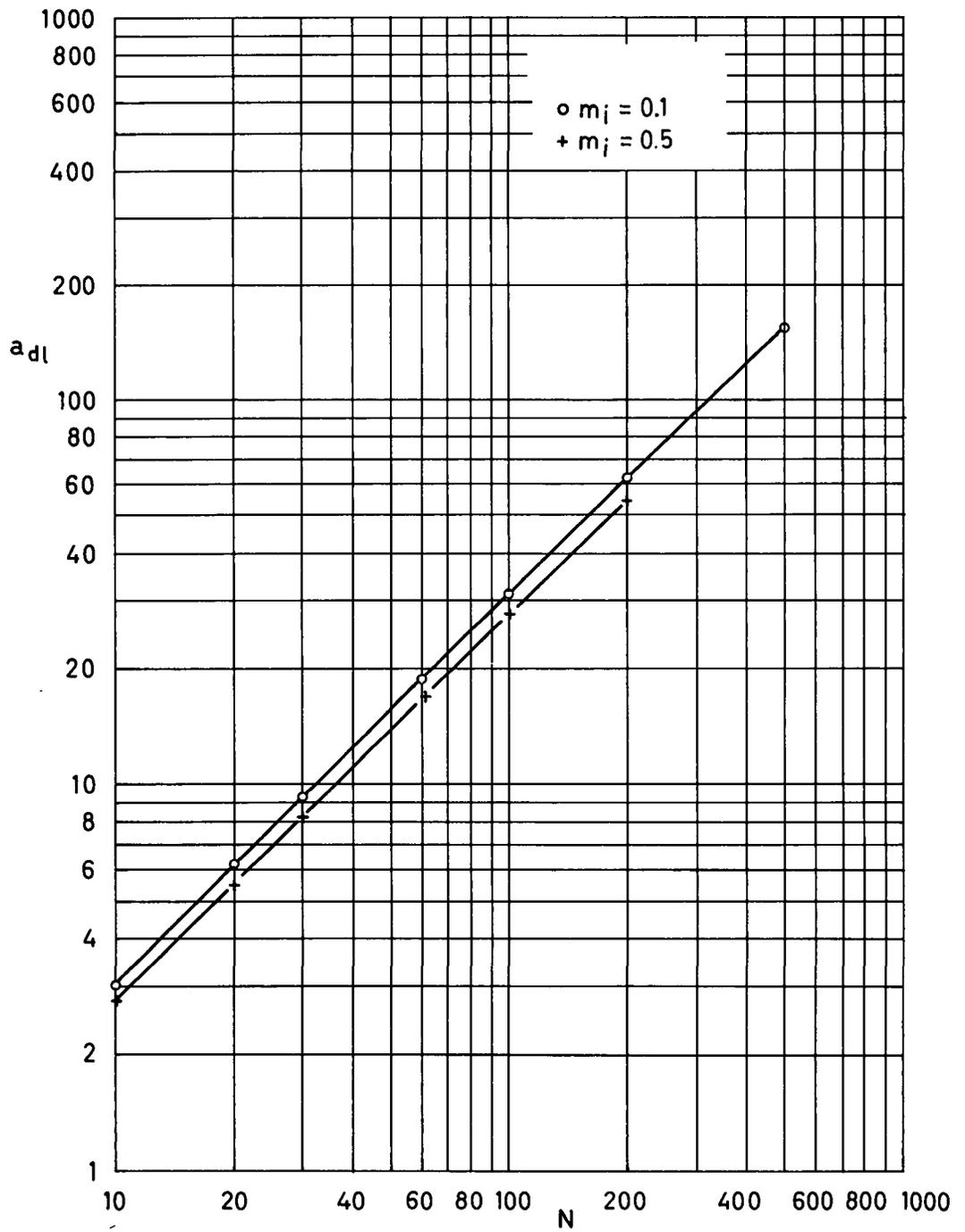


Figure 27.

Attenuation a_{d1} of the first spectral line of the frequency spectrum of the function $e_{in} = 1 + m_i \sin \beta$ by an aperiodic sampling process.

reference to figure 24 ($N = 60$), but this time with a higher relative sampling frequency. The result is shown in figure 26.

It is seen that the spectral lines with order number $n < 180$ have all but disappeared, which is due to the high sampling rate as indicated by (4.12) and (4.14).

The attenuation a_{d1} of the first spectral line of e_{in} as defined in (4.4) as a function of the number N of samples per period is shown in figure 27.

It is seen that relation (4.12) holds for a given modulation index m and for the various N . A change of a_{d1} occurs when the modulation index increases to 0.5 as seen on the same graph, although this new value of a_{d1} remains linearly proportional to N . An investigation of the effects of the modulation index m_i shows that the attenuation a_{d1} of the first harmonic coefficient of e_{in} remains proportional to N once the appropriate factor for the given modulation index is established.

The results of this investigation are shown in figure 28 where a_{d1} is related to m_i .

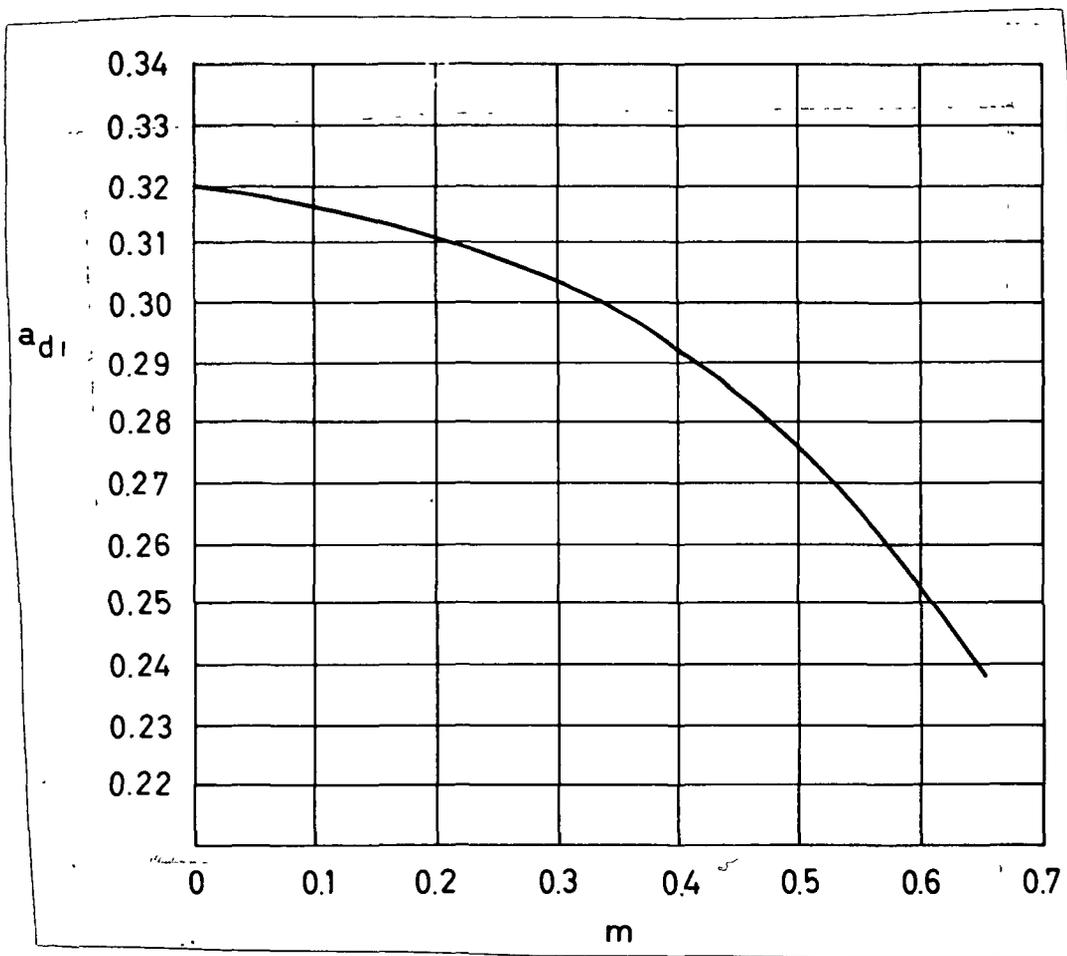


Figure 28.

Attenuation per sample a_{d1} for the first spectral line of the frequency spectrum of the function $e_{in} = 1 + m \cdot \sin \beta$ by an aperiodic sampling process.

It follows that once the frequency spectrum of the source voltage function e_s is known one can choose the sampling rate in such a manner that the band limited frequency spectrum of e_o will have a specific and predictable content. The designation of this pro-

cess as deterministic pulse modulation is based on this property of the described process.

b. A Nonuniform Periodic Sampling Process (PWM).

The spectral transformation can be also implemented by application of a pulse width modulation process, described in the discussion with reference to figure 5.

The mathematical treatment of this process can be carried out by describing it in form of a nonuniform periodic sampling process. Similar and analogous reasoning is applied for that purpose, consistent with the arguments presented in the initial phase of this chapter; these were used to justify the mathematical treatment of a process of pulse frequency modulation by way of uniform and aperiodic sampling.

Analysis shows (referred to under I.2.) that the first harmonic component can be, ideally, completely suppressed with application of that process. The ensuing vector diagram can be viewed to be similar with the one depicted in figure 22 indicating the intrinsic mechanics of a uniform and aperiodic sampling process which lead to the ensuing effects as illustrated in figures 24 and 26 through 28. However, the new vector diagram, applicable to PWM would contain a set of individually weighed vectors A_k which are spaced with equal angles in the complex plane $nk\Delta\beta = n2\pi k/N$. The time intervals $\Delta\beta$ between samples are uniform and given by

$$\Delta\beta = 2\pi/N \quad (4.16)$$

The vectors A_k follow the same (broken curve) contour $e_{i1}(\beta)$,

however, with weights signifying the respective pulse width such that an analogous effect is achieved as pursued with the process of aperiodic uniform sampling (PFM), namely to let constant Q introduced with (4.7) assume a value such that

i.

$$\frac{Q}{2\pi} \sum_{k=1}^N e_{i1}^*(\beta) = \frac{1}{2\pi} \sum_{k=1}^N A_k = 1$$

ii. all sums of the projections of the vectors A_k on the horizontal and on the vertical axes approach zero for any n , except for $n = 0$.

The n th Fourier coefficient c_{in}^* of e_{in} as defined by (4.7) and (4.13) in a general manner is given in this case by:

$$c_{in}^* = \frac{1}{2\pi} \sum_{k=1}^N A_k e^{-jn2\pi k/N} \quad (4.17)$$

For reasons of symmetry it is possible to weigh the vectors A_k which are equally spaced in time with intervals $\Delta\beta$ in such a manner that ii. above can be, indeed, satisfied for $n=1$, not only by way of approximation, but completely.

The technical effectiveness of this process is, however, curtailed by the inadequacies of physical electronic switches, as discussed with reference to figure 9.

The complete removal of the first harmonic component of e_{in} as indicated above is, in theory, only possible if the number of N samples fits exactly into one normalized period 2π . This is, in turn, predicated on the requirement stated in (4.16). It will be

seen in chapter V that once the electronic control mechanism is established, then a satisfaction that $N\Delta\beta = 2\pi$ for each cycle would require an almost prohibitive electronic complexity. Fortunately, nature is gracious and strict satisfaction of neither of the theoretical requirements is necessary in order to obtain engineering results well within acceptable limits.

Preference could be given to PWM over PFM in cases where suppression of the first harmonic component of e_s is of paramount importance, provided that physical limitations of the power electronic mechanisms and certain system stability considerations are compatible with that approach.

c. A Nonuniform and Aperiodic Sampling Process (PWM-PFM).

The spectral transformation discussed in this chapter can be implemented by combining the two described processes of pulse width and pulse frequency modulation to one composite process (PW-PFM) as discussed with reference to figure 5(d) in chapter II. The combination of these two processes has several advantages:

- c1. The attenuation of the first harmonic component of $e_{in}(\beta)$ can be improved over the results given for PFM with relation (4.12) and discussed with reference to figures 24, and 26 through 28.
- c2. The improvement cited under c1. above can be implemented under mitigation of the restrictions imposed on the attenuation of higher order harmonics by application of PWM, as indicated under IV.3.b. above. In other words: a reduction of the band limited $(-f_c < f < f_c)$ spectral lines of e_s shown in figure 15

by at least the measure indicated by (4.14) is possible, concurrent with the above cited (c1.) improvement.

- c3. A second degree of freedom inherent in this method of pulse modulation, described in the discussion with reference to figure 5(d) and summarized in Table I can be used to:
- i. Overcome a physical limitation of the power electronics system such as the saturation limit of a magnetic device (transformer) containing a saturable core material, or the inadequency of electronic switching devices illustrated in figures 9 and 14, or
 - ii. Satisfy dynamic system stability requirements concurrent with satisfaction of the static system stability requirements, meaning that control of the system output voltage regulation remain within the limits of tolerance indicated and discussed with reference to figure 3. One of two degrees of freedom of the composite PW-PFM process is used, respectively and independently, in support of the objectives of static and of dynamic system stability, as referred to under this letter ii.

A disadvantage of the composite PW-PFM system is that the power converter cannot be synchronized to an external periodic signal because it contains the frequency modulated element. This limitation restricts its use to so called "free running" systems, where the internal frequency of operation is irrelevant.

The question of whether it is necessary at all to synchronize the internal workings of a d.c. converter is in itself a controversial one. Yet, the indicated technical restriction of the PW-PFM remains an inherent property of that, otherwise, advan-

tageous system.

The material was, so far, largely discussed in terms of normalized quantities such as the voltage e_{i1} , containing only one single harmonic component with coefficient E_{i1} , a voltage e_{in} containing an infinite number of harmonic components with coefficients E_{sn} , the time β in radians and the normalized frequency of $1/2\pi$ Hz. All results stated in normalized form are equally applicable to the analogous common values of source voltage e_s , its harmonic coefficients E_{sn} and any common source voltage frequency $f_s = \omega_s/2\pi$ Hz.

The significant results indicating the attenuation a_{dn} of the n th harmonic coefficient E_{sn} of a source function e_s which is chopped into N pulses per period $P_s = 1/f_s$ for a given mode of pulse modulation, remain unaltered. They are directly applicable to any related engineering problem at hand.

The results of this chapter are for convenience summarized in Table II below.

Table II.

Attenuation a_{dn} of Spectral Lines by Way of Pulse Modulation at the Input Terminals of the Output Filter for $m_i \ll 1^*$

	a_{d1}	$a_{dn} \quad n > 1$
PFM	$\sim N/\pi$	$\sim N/\pi n$
PWM	$> N/\pi$	$< N/\pi n$
PW-PFM	$> N/\pi$	$\sim N/\pi n$

$m_i = E_{sl} / E_s$ where e_s is the periodic content of the source voltage e_s and E_s is its nominal value as stated with (2.2) and the therewith associated definitions.

N = number of pulses per period $P_s = 1/f_s$ of the fundamental frequency f_s of e_s ; the number f_{Fav} of pulses per second is Nf_s .

*for other values of $m < 0.65$ see figure 28.

4. Spectral Transformation of Aperiodic Source Functions.

So far, two significant aspects of transformation of the function $e_s \rightarrow E_o$ stated by (2.1) have been considered with the objectives to

- 1a. scale and stabilize a d.c. voltage e_s by means of time ratio T_k / T_{ok} control of a pulse train e_s^* derived from e_s
- 2a. remove the low frequency harmonic components contained in e_s

It was assumed that

$$e_s(\tau_k) = e_s(t + kP_s)$$

with

$$k = 1, 2, \dots$$

No time restriction was imposed on the magnitude of P_s . It appears that the reasoning used for analysis should be independent of the magnitude of the period P_s , even if that period

$$P_s \rightarrow \infty$$

The fundamental frequency f_s would indeed become smaller and smaller, but by the same token would the number N of pulses per period increase for given $T_{ok \min} < T_{ok} < T_{ok \max}$. The attenuation a_{d1} of the first harmonic component E_{s1} remains given by (4.12) and will therefore **increase with the number N of pulses per "period" of e_s , whatever the length of the period P_s . The length of P_s remains finite for any practical system and the analysis will hold for that reason.**

It can be shown that the results summarized in Table II will hold also, if the number N of samples (pulses) per period P_s increase without limit.

The attenuation of the spectral lines under discussion will then take place even if $P_s \rightarrow \infty$ and $f_s \rightarrow 0$; nevertheless, they remain finite in magnitude because of physical limitations.

One classical case in **which the aperiodicity of the source function becomes significant is that of the occurrence of a step in e_s , as illustrated in figure 29. The high frequency content contained in**

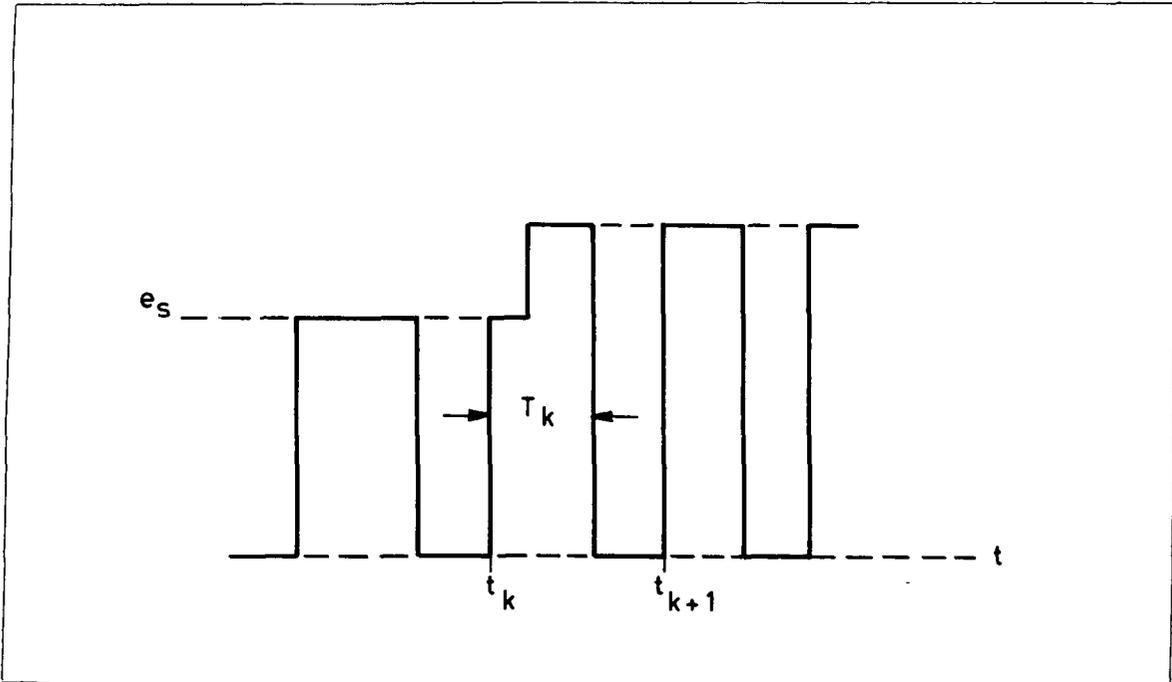


Figure 29.

Pulse modulation of the source voltage e_s at the occurrence of a step in e_s .

the step of e_s which occurs in the interval $t_k < t < t_k + T_k$ is never "seen" by the low pass filter which accepts the pulse train, because the pulse behaves according to the requirements of (4.1); its peculiar shape is entirely irrelevant under these conditions as stated under and discussed with reference to IV.2.d.

One aspect that gains significance is the low frequency content in the step, which is the classical cause for over- and undershoots in the output voltage e_o . It is one of the fortunate properties of the described pulse modulation systems that the harmonic components with frequency f_F that may be generated by the step in e_s and which lie outside the filter cut off frequency, and which will not be removed as part of a "peculiar" pulse shape as indicated above, will be suppressed by the filter. Those harmonic components with frequency f_s that lie inside the frequency band limit

$(-f_c < f < f_c)$ of the filter will be suppressed by the modulation process itself as described throughout this chapter. The location of the various spectral lines and the associated groups of frequency components are indicated in figure 30 for convenience.

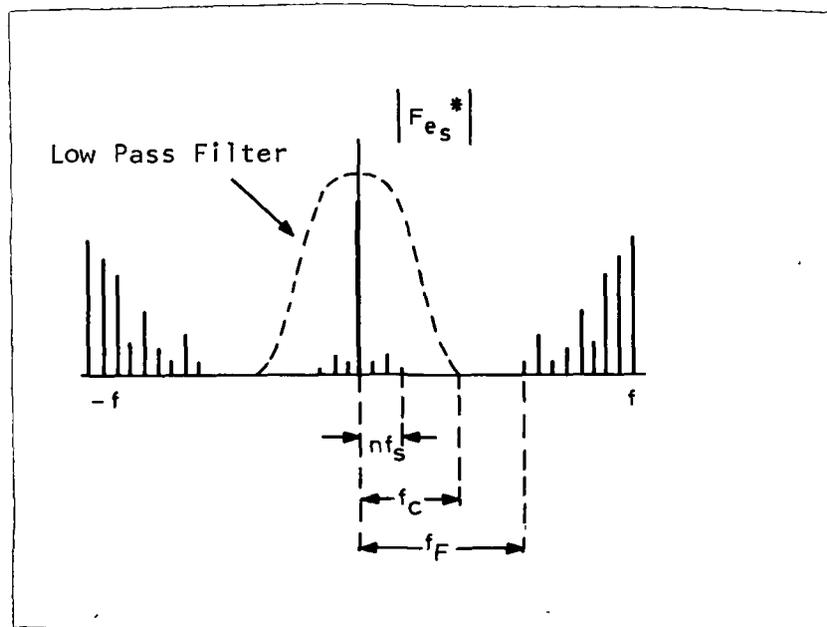


Figure 30.

Illustration of frequency ranges: f_s of the sampled function, f_o the natural filter frequency, f_F the sampling (pulse frequency).

Physical limitations of the power apparatus may impair the indicated advantages of the described pulse modulation systems, especially the distributed shunt capacitance of the filter series inductor and the series inductance and resistance of the shunt capacitor. Appropriate design can mitigate these effects and will be indicated in the following chapters.

5. Design Requirements for Power System Control.

A control system which implements the pulse modulation processes that were described in this chapter will acquire information on the size and shape, or more specifically the area A_k of each individual pulse which enters the low pass filter. This system will, in principle be of the form shown in figure 31.

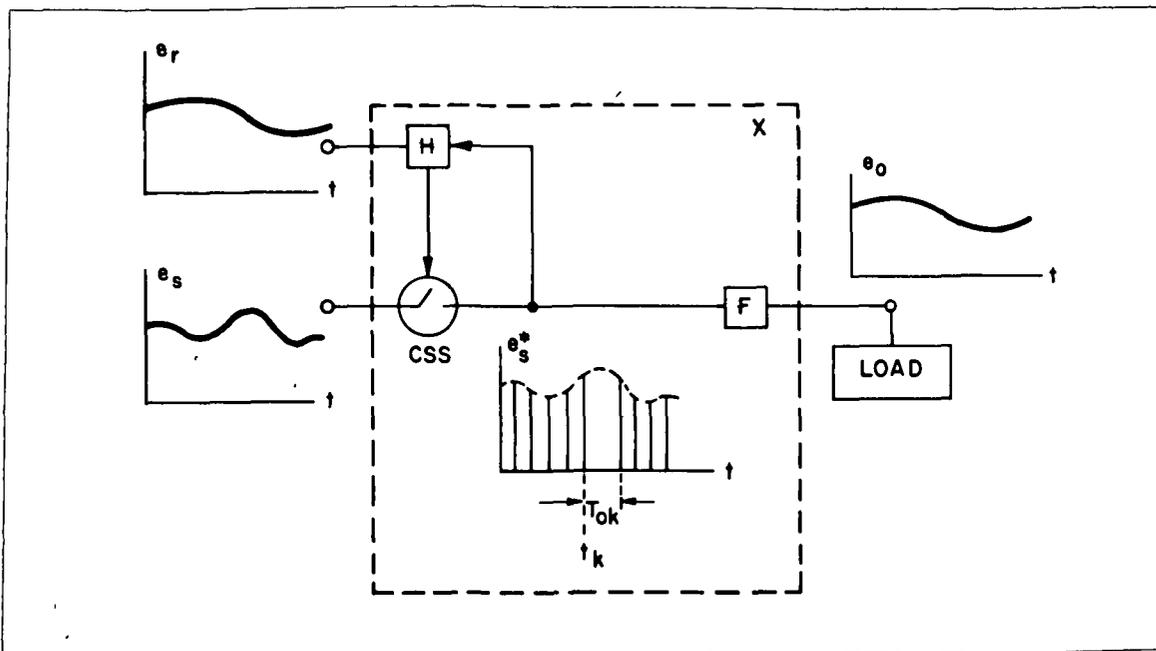


Figure 31.

Electronic system for nondissipative conversion of $e_s \rightarrow e_o$.

The k th pulse $e_s^*(k)$ is "observed" by control block H during the process of its formation and compared with the requirements of the control signal e_r , which is here sketched as a curve for purpose of generality. Block H governs the controlled sampling switch CSS and operates it in such a way, based on signals e_r and e_s^* for $t_k < t < t_{k+1}$ that relation (4.1) is satisfied for each of the

individual intervals. Satisfaction of (4.1) is requisite to any of the previously discussed forms of deterministic pulse modulation; the specific form depends on the internal mechanism of block H; it will be discussed in more detail in the following chapter.

The significant aspect of the symbolic diagram shown in figure 31 is the fact that the pulses are being formed in the presence and under the influence of the control signal e_r and of the pulse itself there and then, and without delay by any filter.

If block H can, indeed, operate switch CSS in the described manner, then the needed minimum interval frequency of operation of a planned d.c. power converter to reduce the harmonic content of e_s stated in (2.4) to be confined within the required limits stated in (2.5), can be determined by selection of the appropriate number N of pulses from Table II.

- a. Attenuation of the harmonic content caused by the internal chopping process.

The high frequency content of e_o caused by the pulse modulation process is contained by a second order (LC) low pass filter within specified limits for a given case by letting

$$a_m / V_{oFm} = a_{Fm} \approx (m\omega_F / \omega_o)^2 \quad (4.18)$$

where

a_m = the coefficient of the mth harmonic frequency component of e_s^* caused by the lowest chopping rate

v_{oFm} = the maximum allowable filter response to this mth harmonic component, as specified

a_{Fm} = the attenuation of the mth harmonic component a_m of e_s^* by the filter without application of an external feedback loop

$\omega_F = 2\pi f_F$, where f_F is the lowest frequency component caused by the chopping process

$\omega_o = 1/\sqrt{LC}$, being the natural undamped resonant frequency of the second order LC filter

m = the order number of the harmonic component under consideration

To calculate the harmonic coefficient a_m defined in and by the discussion with reference to (3.1), it is convenient to normalize numerator and denominator of the ratio stated in (4.18) for convenience without causing any change in its meaning or magnitude. This ratio is rewritten

$$a_{mn}/V_{oFmn} = \frac{a_m/a_o}{V_{oFm}/E_o} = a_{Fm} \quad (4.19)$$

where index n indicates a normalization.

If $a_o \approx E_o$ as in the case of a simple chopper as illustrated in figure 11, then (4.19) is reduced to (4.18). If a transformer effect causes a ratio $a_o/E_o \neq 1$ then (4.19) becomes more meaningful since it expresses the desired ripple attenuation in terms of a fraction, as specified in most cases.

The relative (normalized) magnitude of the mth harmonic a_{mn} of

e_s^* caused by the chopping process is given by

$$a_{mn} = \frac{2\sqrt{2}}{m\pi} \{1 - (-1)^m \cos m\gamma\}^{\frac{1}{2}} \quad (4.20)$$

where

$$\gamma = \pi(2d - 1)$$

and

d = the smallest or the largest steady state duty cycle T_k/T_{ok} of the planned pulse train e_s^* , whichever would cause the largest a_{mn}

In most cases it suffices to consider the first harmonic component only, which results in

$$a_{1n} = \frac{2\sqrt{2}}{\pi} \{1 + \cos\gamma\}^{\frac{1}{2}} \quad (4.21)$$

For the approximation of a "standard" duty cycle $d = 0.5$, is

$$a_{1n} \left[\begin{array}{l} = 4/\pi \\ \gamma = 0 \end{array} \right] \quad (4.22)$$

If it is specified that V_{of1}/E_o be less than p percent then

$$a_{Fm} > 10^2 \frac{2\sqrt{2}}{p\pi} \{1 - (-1)^m \cos m\gamma\}^{\frac{1}{2}} \quad (4.23)$$

and

$$a_{F1} \left| \begin{array}{l} > 4 \cdot 10^2 / \pi p \\ d = 0.5 \end{array} \right. \quad (4.24)$$

The undamped natural frequency ω_0 of the filter is then readily calculated from (4.19), whichever expression is used to calculate the needed attenuation of the high frequency harmonic components with the minimum fundamental frequency $f_{F \min}$.

b. Requirements for d.c. output voltage error confinement.

The material contained in this chapter and its significance for the output voltage e_o can be reviewed qualitatively in connection with a reinspection of figure 3., which is here reproduced for convenience.

- b1. The high frequency ripple consisting primarily of the first harmonic component with amplitude V_{oF1} of an open loop DPM system will not differ significantly from that of an ordinary feedback controlled d.c. power converter (OFECDIC), provided (3.4) is satisfied. The term "open loop" is used to indicate that no signal is being fed back from the output terminals of the converter system to affect in any manner the pulse modulation process.
- b2. The low frequency component of e_s is reduced by the open loop DPM system according to the relations indicated in Table II under IV.3.c. unlike the case of the OFECDIC system which requires a gain A in the feedback loop for that purpose. The effectiveness of the DPM systems low frequency ripple reduction

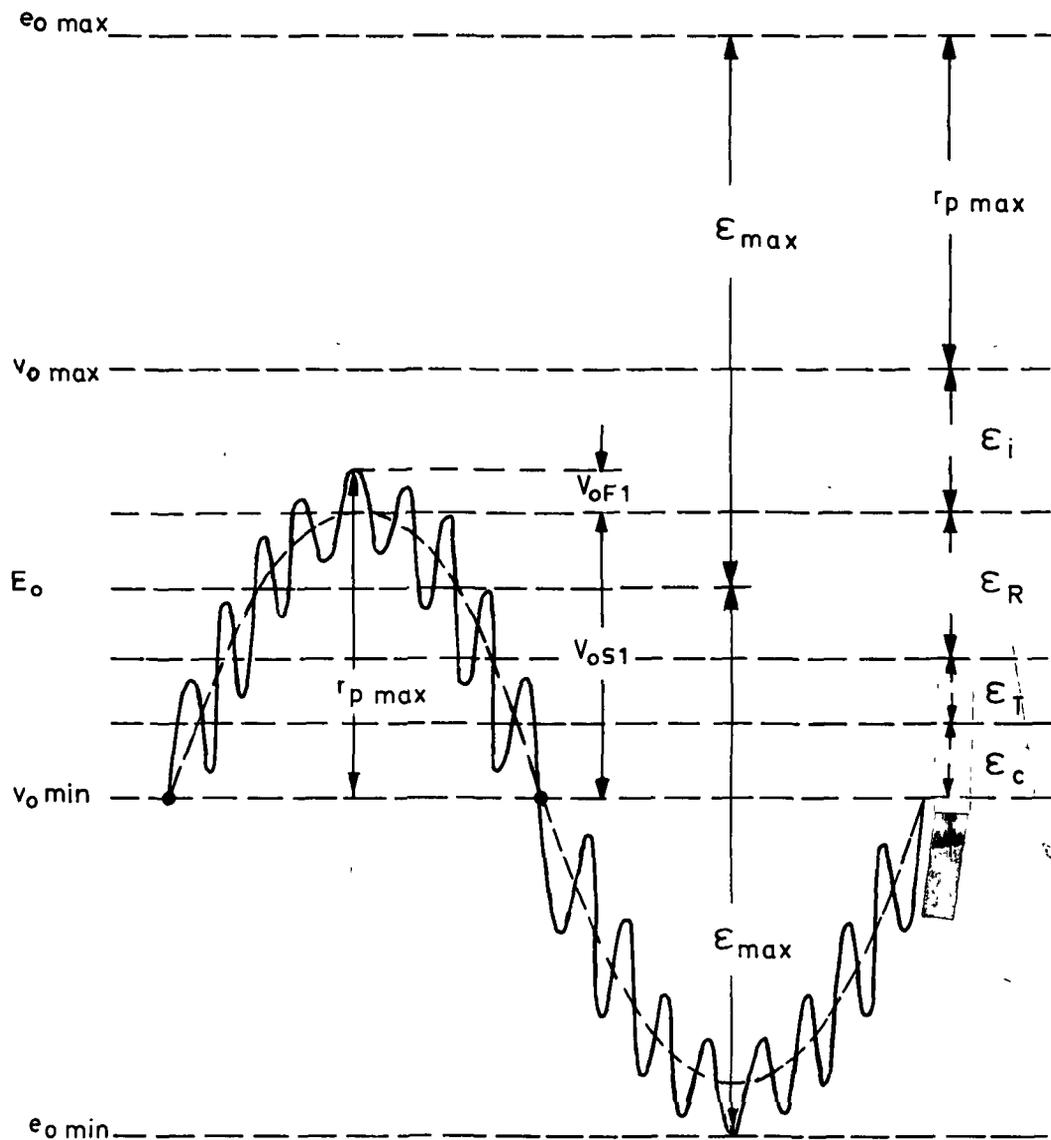


Figure 3.

Effects which cause errors in the output voltage of feedback controlled d.c. power converters.

depends on the number N of pulses per period P_s and is limited by the practicality of high frequency chopping operation in the light of system efficiency and reliability.

- b3. All output voltage level errors ϵ_i which are due to variations of the input voltage level indicated by e_{dc} in (2.2) are eliminated by adjustment of the average value of the pulse train e_s^* entering the low pass filter, stated in (4.17). The d.c. error component ϵ_i indicated in figure 2 is therewith reduced to zero.
- b4. Error components ϵ_R and ϵ_T caused by effects that precede the input terminals of the output filter in the sense of power flow are, likewise, eliminated by virtue of (4.17) which governs the pulse train actually entering that filter. This comprises most of the causes of ϵ_R and ϵ_T error components in a converter.

However, a residual cause of errors ϵ_R and ϵ_T is located in the resistive components of the output filter inductor and the wiring between input filter terminals and the load. The effect of this resistive component can be estimated from the specified or chosen design efficiency of the output filter inductor, and if applicable, the resistance of the (ground) power return wire. See figure 32.

If a relative power loss of $1 - \eta_2$ at full load is designed into the output filter inductor ~~then the~~ ensuing no load--full load voltage variation, is determined.

The error ϵ_{RL} caused by the series resistance R_ℓ of the induc-

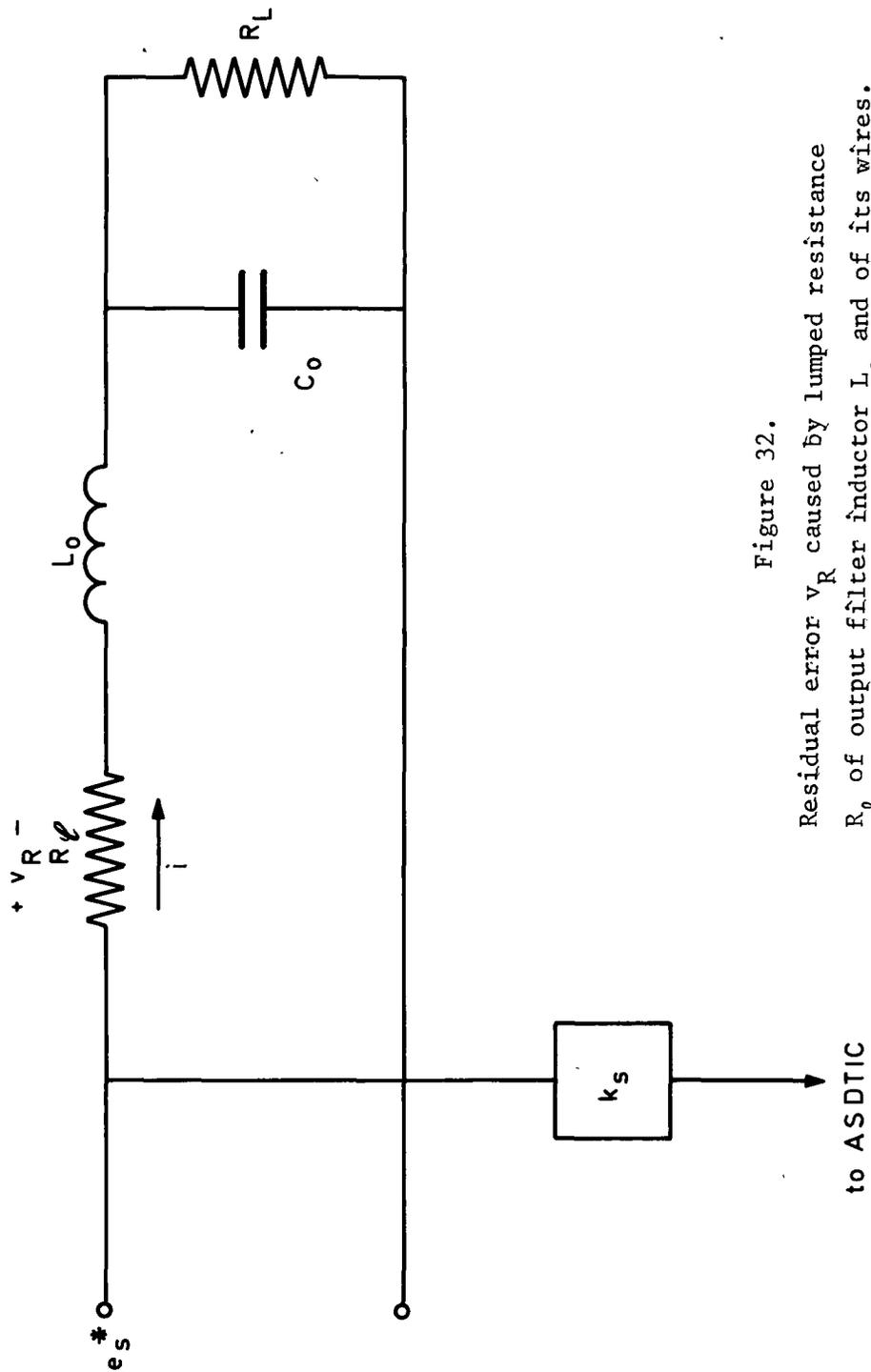


Figure 32.

Residual error v_R caused by lumped resistance R_ϕ of output filter inductor L_0 and of its wires.

tor is given by the ratio

$$\epsilon_{RL}/E_o = \rho_i^2 R_\ell/R_L \quad (4.25)$$

identifying the cause of ϵ_{RL} as the effect of a resistive voltage divider. At no load is $R_L \rightarrow \infty$ and $\epsilon_{RL} \rightarrow 0$. Symbol ρ_i signifies the current form factor i_{rms}/i_{av} as defined in the literature [6]. When R_L assumes its smallest value $R_{Lf.l.}$ at full load then is

$$1 - \eta_\ell = \rho_i^2 R_\ell/R_{Lf.l.} = \epsilon_{RL \max}/E_o \quad (4.26)$$

which shows that the maximum relative "no load - full load" error caused by the inductor is identical with the relative power loss in that inductor.

If, for instance, $1 - \eta = 0.02$ and the nominal output voltage E_o is "centered" about its average value 0.01 then the relative error $\epsilon_{RL}/2E_o$ caused by the resistance R_ℓ of the inductor will be + 1 %. Powerful tools will be shown further on to remove this residual error which is not eliminated by the pulse modulation methods in the discussed form.

The efficiency η_ℓ of the inductor at full load can be calculated at the highest wire temperature. The effect ϵ_{TL} concerning the inductor alone is then included. It is, again, only a small fraction of the former ϵ_T of the OFECDIC system because the pulse train e_s^* removes the effects caused by variations of temperature in all components preceding the formation of that

pulse train.

One significant effect caused by changing ambient temperature is the voltage variation of the voltage reference source, usually a Zener diode which at times is temperature compensated. This voltage variation cannot be remedied by any known electronic mechanism. Fortunately the error caused by the reference voltage source is usually small compared to the other temperature caused errors of the OFECDIC systems.

- b5. The effect ϵ_c of variations in the accuracy of the control system can be all but eliminated by devising the concerned electronics in an appropriate manner which applies a principle of autocompensation; this principle will be treated further on. The error $\epsilon_c \rightarrow 0$ under these conditions.

c. Summary of system design requirements.

The system characteristics which result from the application of a deterministic pulse modulation process are compared to conventional feedback methods; they are summarized in Table III. The index D has been added to the d.c. error indices ϵ_p to indicate the association of these terms with the discussed DPM method; suffixes F have been added to the indices of the errors ϵ_p associated with conventional feedback systems.

Table III.

D.C. Error Indicators ϵ_{pD} Found in Open Loop DPM Systems and Related to the Same Errors ϵ_{pF} of OFECDIC Systems.

	Remark
$\epsilon_{iD} \rightarrow 0$	Feed forward effect
$\epsilon_{RD} \rightarrow k_i \epsilon_{iRF}$	$k_i \ll 1$ Inductor resistance only
$\epsilon_{TD} \rightarrow k_T \epsilon_{TRF}$	$k_T \ll 1$ Reference Zener diode and inductor resistance only
$\epsilon_{cD} \rightarrow k_c \epsilon_{cF}$	$k_c \ll 1$ Autocompensation reduces this error component by at least one order of magnitude
$E_{s1} \rightarrow V_{os1} = E_{s1} v/M$	<u>Attenuation attained without conventional feedback loop; A = 0.</u>
$V_{oF1D} = V_{oF1F}$	No change in h.f. ripple, provided $A(\omega_o/\omega_F)^2 \ll 1$

An examination of Table III indicates that the open loop results of the DPM system are comparable with the closed loop results of the OFECDIC system. If one attaches quantities to the improvement, then the advantages of the DPM system become even more obvious.

- c1. The DPM system can attain an open loop static system stability that is comparable to the same stability of an OFECDIC system. If an outer loop were added to the DPM system, then the magnitude of the feedback gain A would be at least one order of magnitude smaller in order to attain an equal d.c. accuracy.

- c2. Alone the fact of a smaller feedback gain A, if any, makes the dynamic behavior of the DPM system superior to the OFECDIC systems, not counting the aspects of prevention of source voltage noise penetration into the system and its output voltage.

V. APPLICATION OF DPM PROCESS.

The process of deterministic pulse modulation was, originally, conceived to control the power flow into second order filters as customary with a larger class of d.c. converters. These comprise d.c. choppers in form of so called "buck" or "boost" regulators, and systems containing parallel or series inverters, followed by rectifiers and second order (LC) filters.

During work on the application of DPM processes it became apparent that they could be used with advantage to control other types of d.c. converters including those terminating in first order filters. This includes "fly back or energy ladling" circuits, also referred to a series inductor converters or to series capacitor converters.

Control of the named systems by DPM processes is introduced, and the significant aspects are discussed.

1. Concepts of Control.

The pulse train e_s^* entering a low pass filter such as illustrated in figure 14 is being fed into an electronic control system. Signal e_s^* is sensed by establishing a connection to the input terminal of the output filter; it is being attenuated by a factor k_s and then ~~enters~~ enters the control system. This is symbolically indicated in figure 33.

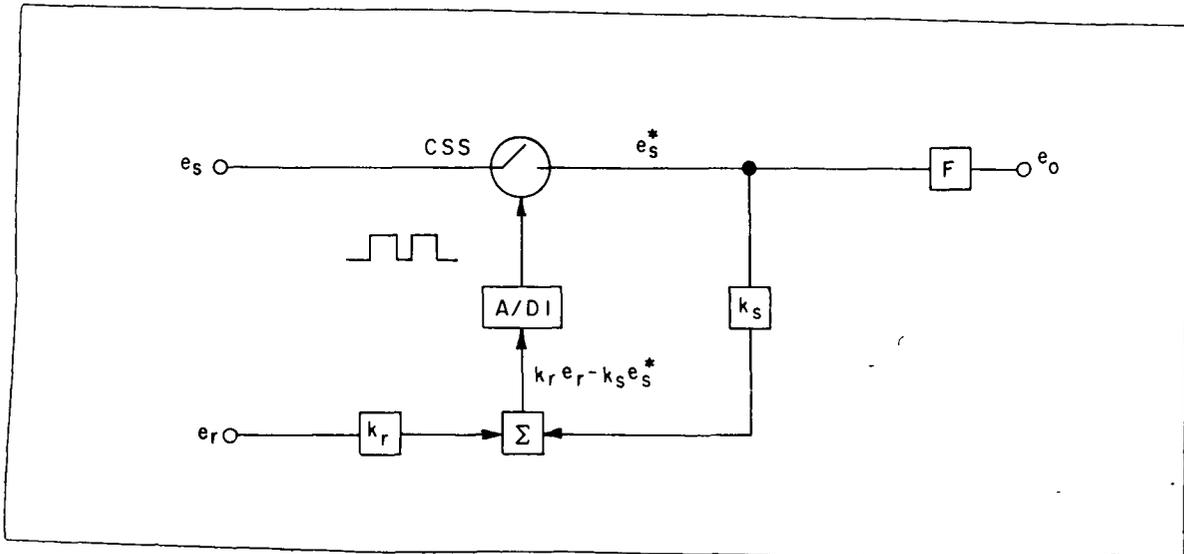


Figure 33.

Symbolic diagram of DPM controlled d.c. converter.

Another signal fed to the electronic control system is that of a d.c. reference source e_r , attenuated by a factor k_r . These two signals are added algebraically to form the sum

$$x(t) = k_s e_s^* - k_r e_r \quad (5.1)$$

This sum is fed into an analog (signal) to discrete (time) interval A/DI converter which transforms this information into an unbroken succession of alternating discrete time interval 0|0|..... signals; this A/DI converter governs the controlled sampling switch CSS in such a manner that it is closed during a one (1) position, and opened during a zero (0) position of the DI signal (see figure 33.).

It is emphasised that this DI signal is not a digital signal in the currently accepted sense of electrical engineering language. Digital signals are assumed to be clock driven and to occupy a succession of periodic time intervals. This DI signal does consist of a succession of 0101.... values, but the time spaces of this succession vary according to the intended pulse time ratio T_k/T_{ok} prominently used throughout the treatment of the presented methods and contained in relations (2.16) and (4.11). The time pattern of this signal can contain periodic elements such as a fixed time interval from one 1 to the next 1 for PWM; but the width of 1's and 0's will vary. PFM and PW-PFM processes do not introduce any periodic elements into the DI signal. It is, therefore, referred to as a DI signal rather than a digital signal.

It depends on the programming of the DI converter whether the system will operate in the PWM, PFM or PW-PFM mode.

Purpose of the DI converter is to implement the pulse modulation methods described throughout this work and summarized in Table I to achieve the results listed in Tables II and III. One of the primary requisites to achieve these results is satisfaction of (4.1) which can be put into a more rigorous form:

$$k_r \int_{t_k}^{t_{k+1}} e_r dt = k_s \int_{t_k}^{t_{k+1}} e_s^* dt$$

This relation is, certainly satisfied if

$$\int_{t_k}^{t_{k+1}} (k_r e_r - k_s e_s^*) dt = 0 \quad (5.2)$$

It is concluded that if (5.2) holds for each individual time interval $T_{ok} = t_{k+1} - t_k$, then the ensuing pulse modulation process will materialize all results listed in the tables cited above, which summarize the reasoning and discussions associated with the individual goals in terms of intended effects.

Relation (5.2) does not impose any restriction on the shape of the individual pulses $e_s^*(k)$, nor does it rely on a process of iteratively improving approximation for purpose of its eventual satisfaction. It states the requisite condition that has to be satisfied unconditionally over each closed interval T_{ok} .

The DPM system derives from compliance with the just stated requirement its favorable properties which will become apparent as the technical significance of the more fundamental considerations contained in the preceding material will unfold.

One of the striking aspects contained in (5.2) is the fact that, if satisfied, there will be a zero system's error. This fact typifies the PDM method as a Type I control system [7] up to the input terminals of the output filter. The steady state error ϵ_s of such a system is zero, because it integrates the error over an extended time. Its integral

$$\int_0^{\infty} \epsilon_s dt < M \tag{5.3}$$

where M is a very finite quantity. Type I control systems suffer usually from stability problems, unlike the DPM system which enjoys a static and dynamic stability exceeding that of conventional Type I

and Type 0 systems. The aspects of dynamic stability can be quantitatively formulated based on rigorous analysis. This analysis is not presented here, as exceeding the scope of this work.

Reduction of the residual error caused by the resistance R_λ of the inductor under varying load conditions will be discussed further on.

a. Application of DPM Techniques for PFM.

The block diagram of an electronic control system H as illustrated in figure 31 which contains the A/DI converter applied for PFM control of a d.c. converter and incorporates the DPM concept is shown in figure 34.

Signals e_s^* and e_r are derived from a system as indicated in figures 31 through 33. The cited symbolic diagrams of parts or entire d.c. converter systems can represent any chopper illustrated in figure 11 or any type of inverter-converter which would work into a second order filter. The algebraic sum indicated in (5.1) is formed and fed into an integrator. A signal $x(t)$ is being formed which is identical with $k_s e_s^*$ except that its average value is reduced by $k_r e_r$ as a result of the cited algebraic sum formation defined by (5.1). This is shown in figure 35, which illustrates the voltage waveforms associated with the system depicted as block diagram in figure 34. Signal x enters the indicated integrator and an integral

$$y(t) = y(t_k) - \int_{t_k}^t (k_s e_s^* - k_r e_r) dt \quad (5.4)$$

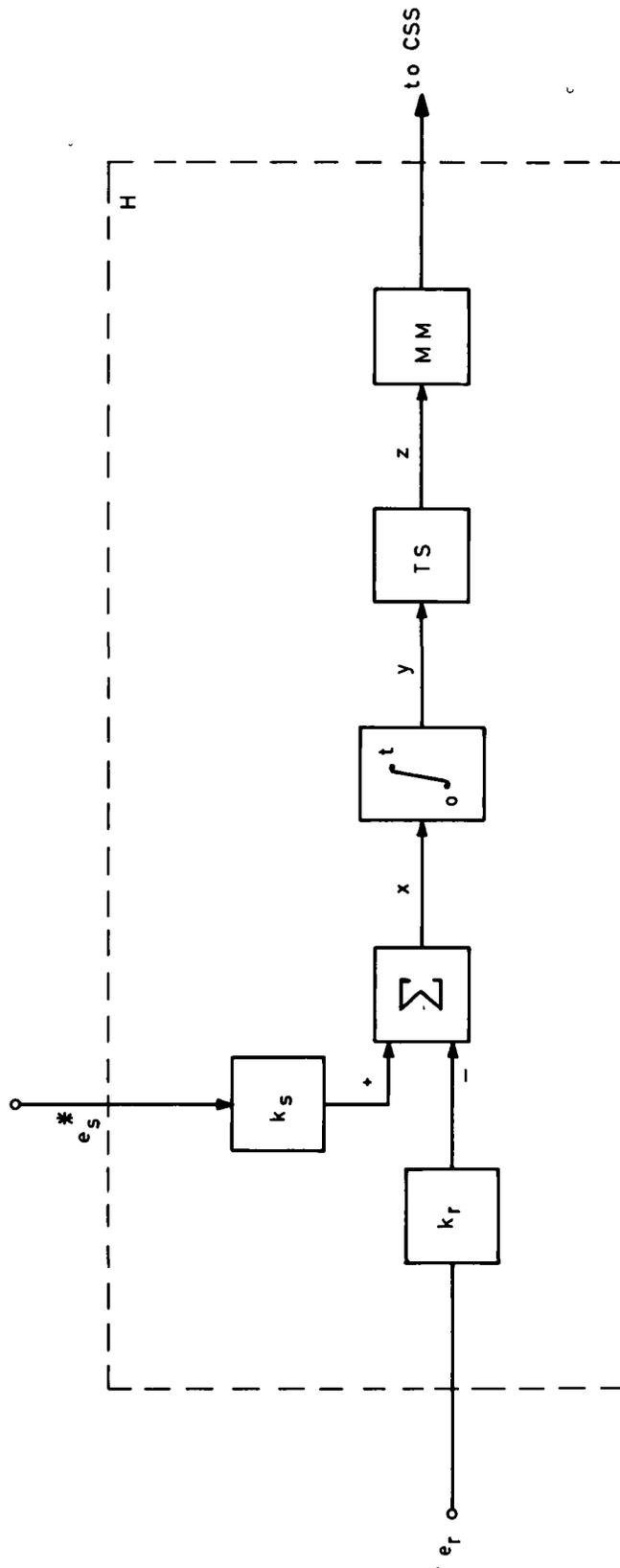


Figure 34.

Block diagram of analog signal to discrete time interval converter ASDTIC for pulse frequency modulation.

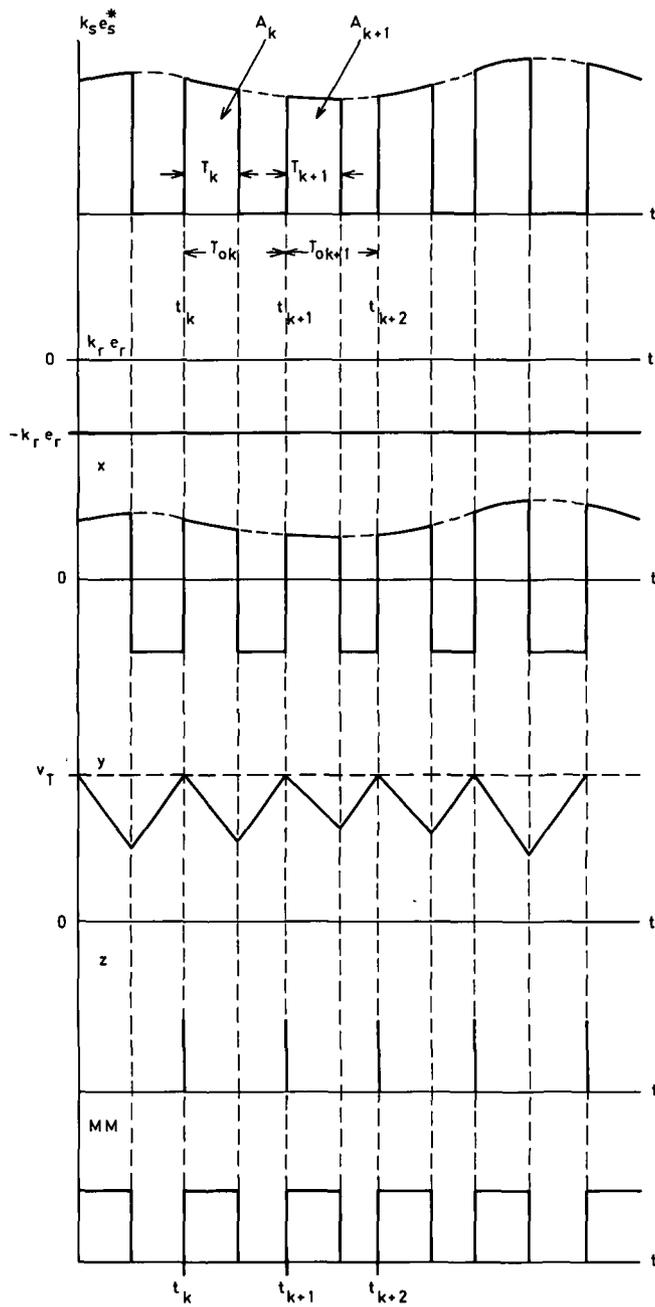


Figure 35.

PFM forming process of ASDTIC and the signal flow associated with its block diagram shown in figure 34.

results. Attention is given to the fact that e_s^* is at time $t_k < t < t_k + T_k$ not a definite pulse $e_s^*(k)$ with a given shape, width or area A_k . It is a pulse which is in the state of generation by the power electronics system following initiation at time t_k and whose shape is determined by parameters that depend on the physical disposition of the system. These parameters include, the value of e_s for $t_k < t < t_k + T_k$, the specific system load with the associated dynamic conditions at that time, the time varying "lumped parameter" characteristics of the concerned components, and the associated parasitic effects.

Pulses

$$e_s^*(k) \neq e_s^*(k+1) \quad (5.5)$$

for the reasons given above. It follows that

$$A_k \neq A_{k+1} \quad (5.6)$$

The electronic system would be physically unable to generate equalities for (5.5) and (5.6), even if it were so desired. Fortunately, this is not at all necessary. The pulses $e^*(k)$ come similar in form as preprogrammed (figure 9), but in actuality unpredictably different "as they please" and as indicated in figure 14.

The voltage waveforms shown in figure 35 are idealized for purpose of clarity of presentation. Pulse train e_s^* assumes, in reality, a form which resembles the one shown in figure

14. Likewise will other voltage waveforms be deformed accordingly.

It is recalled for completeness of presentation that for PFM

$$T_{ok} \neq T_{ok+1}, \quad (2.10)$$

$$T_k \doteq T_{k+1} \quad (2.11)$$

and that

$$\frac{A_k}{T_{ok}} = \frac{A_{k+1}}{T_{ok+1}} \quad (4.11m)^*$$

The integration signal y has the following characteristics

$$dy(k)/dt = dy(k+1)/dt \quad \text{for} \quad dy(k)/dt > 0 \quad (5.7)$$

and

$$dy(k)/dt \neq dy(k+1)/dt \quad \text{for} \quad dy(k)/dt < 0 \quad (5.8)$$

This integration signal starts at time t_k from an initial condition

$$y(t_k) = v_T \quad (5.9)$$

where v_T is a reference voltage which is compared to $y(t)$ by a high gain discriminator. This voltage discriminator fulfills the

*m = modified, using different symbols; otherwise unaltered.

function of a threshold sensor ~~which~~ which emits a signal $z(t_k)$; this signal z triggers a ~~measurable~~ multivibrator MM, which then by virtue of its intrinsic characteristic emits a continuous succession of 1010... signals in response to each trigger $z(t_k)$ that energize the controlled sampling switch CSS.

Evidently $y(t)$ returns to the same initial condition v_T at any instant t_k at the initiation of each cycle. It follows that (5.2) is indeed satisfied if

$$v_T(t_k) = v_T(t_{k+1}) \quad (5.10)$$

However, there is no guarantee that this be absolutely true in any physical system. The relative error ϵ_x that would be caused by variations of v_T will be shown to be irrelevant for all practical purposes (Chapter VI).

The indicated sequence of events is caused by signals e_s^* and e_r which operate on the electronic control system and which in turn form the pulse train e_s^* ~~by way~~ of gross approximation of the conditions imposed ~~by (2.10) and (2.11)~~, yet satisfying accurately the requirement (5.2) ~~and otherwise~~ with the unconditional compliance with (4.11m).

The objectives of the pulse modulation process as presented throughout this work and as discussed with reference to (5.2) are attained accordingly. The validity of this statement depends solely on the ability of the electronic control system to perform its task as described and is independent of all distortions, delays, regulation characteristics and parasitic effects rooted

in the power electronics system. So far, however, with exception of the resistive element R_ℓ incorporated in the series inductor of the output filter.

b. Pulse Width Modulation with Use of DPM.

Pulse width modulation is implemented by application of the same principles stated in this chapter preceding the material under letter a. above. However, the electronic mechanization of the DI block within H used for PFM and shown in figure 33 is altered to fit the purpose.

A diagram of block H (fig. 31) and suited for PWM is shown in figure 36. Its mode of operation is discussed with reference to the associated waveforms shown in figure 37.

A clock pulse emanating at time kT_o from any suitable source such as an astable multivibrator AM (shown) or from a counted down crystal oscillator, or from an external synchronization signal, triggers the bistable multivibrator BM "on", meaning from its previous state zero (0) to one (1). The controlled sampling switch CSS is closed in this process and the kth pulse $e_s^*(k)$ starts to be formed. Signals $k e_{s_s}^*$ and $k e_{r_r}$ are added (5.1) and the ensuing signal x is integrated forming signal y. Threshold sensor TS emits a trigger pulse z, whenever $y = v_T$ at time $kT_o + T_k$. This trigger pulse z turns the bistable multivibrator BM "off" to change its state from one (1) to zero (0) and switch CSS is opened. Pulse $e_s^*(k)$ is then completed.

If (5.10) holds true, then (5.2) is satisfied. It follows that for

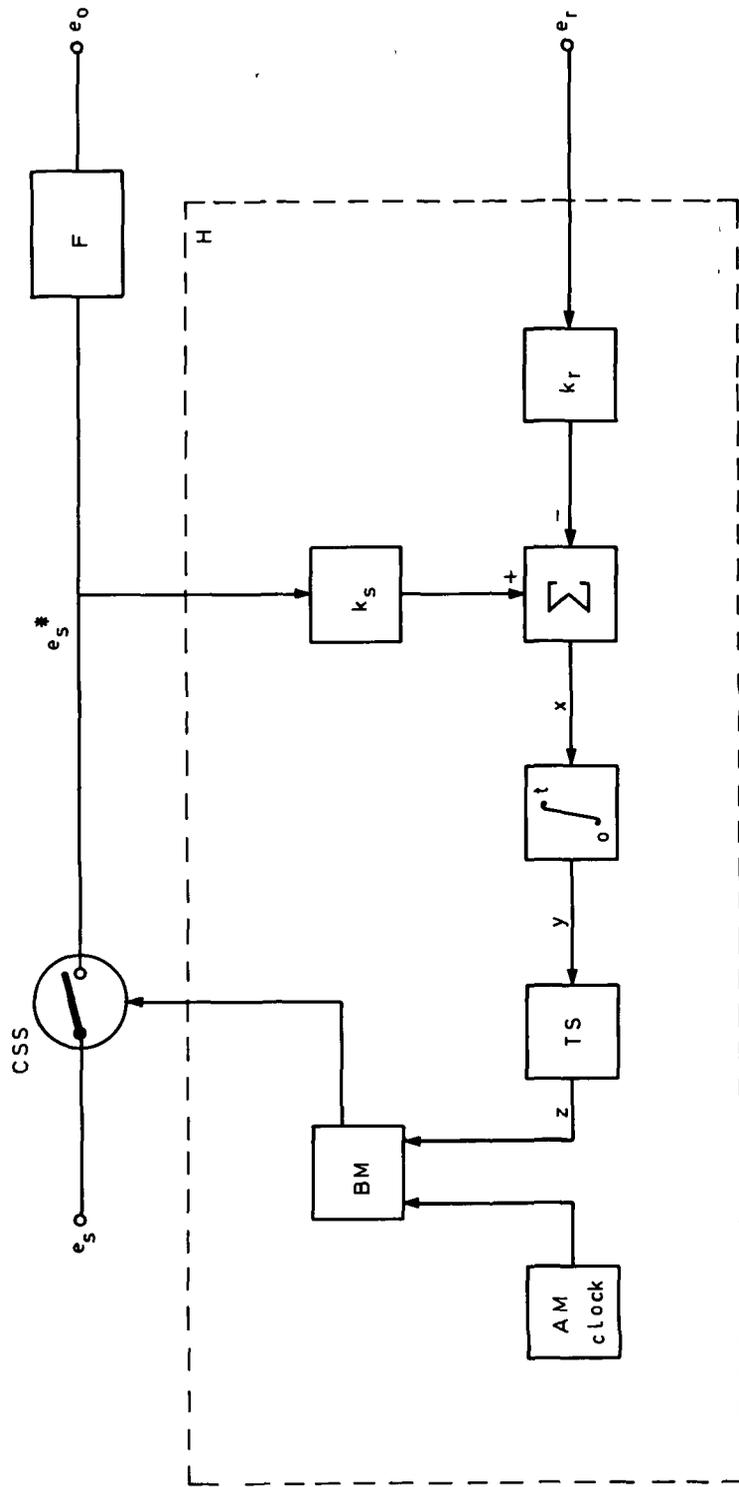


Figure 36. Block diagram of ASDTIC for pulse width modulation (PWM) and its integration with a symbolically indicated converter system.

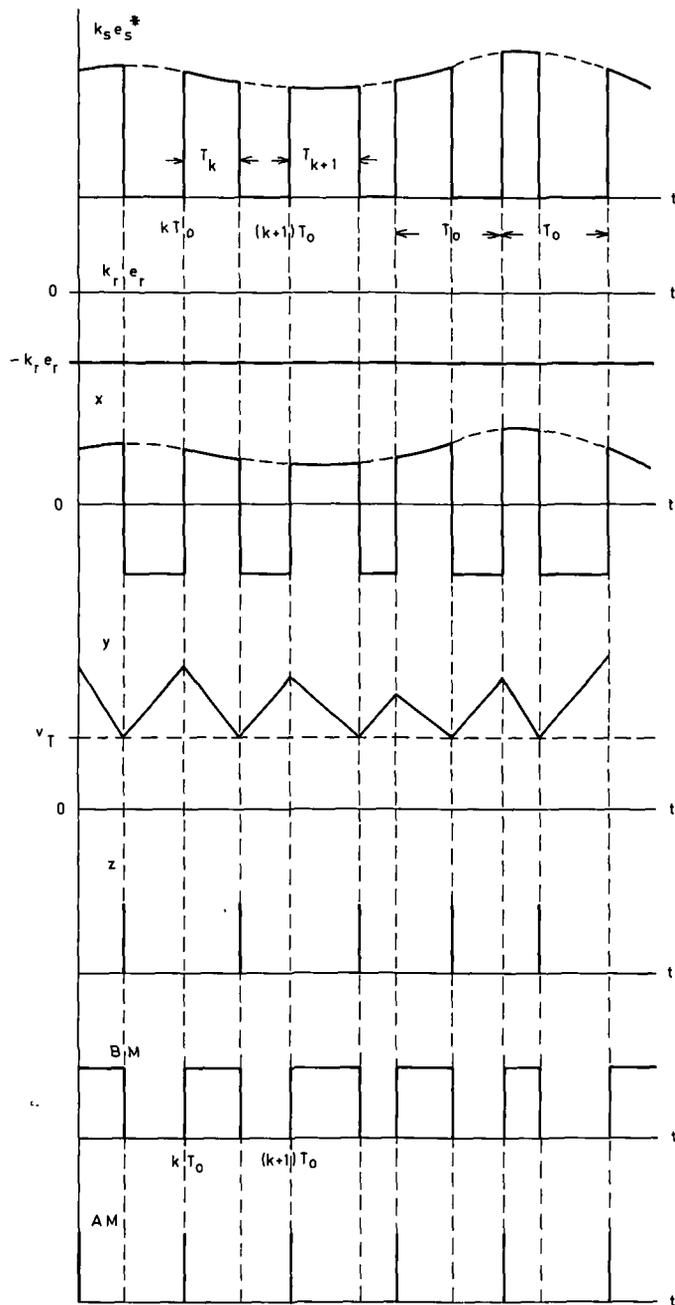


Figure 37.

PWM process of ASDTIC and its signal flow associated with its block diagram in figure 36.

$$t_k = kT_o \quad (2.12)$$

and

$$T_{ok} = T_{ok+1} = T_o, \quad (2.13)$$

but

$$T_k \neq T_{k+1} \quad (2.14)$$

yet

$$\frac{A_k}{T_o} = \frac{A_{k+1}}{T_o} \quad (4.11m)$$

even though all quantities involved, and in particular $e_s^*(k)$, T_k and T_{k+1} are by no means precisely defined or predictable. The mere fact that (5.10) guarantees the validity of (5.2) suffices to satisfy (4.11m). The objectives of DPM processes are, again, secured as discussed at the end of the material under letter a. above.

The integration signal y has the same properties as stated with (5.7) and (5.8).

Attention is directed to an unobtrusive but **significant subtlety**. Pulse $e_s^*(k)$ does not terminate at the instant $t_k + T_k = kT_o + T_k$ because of physical limitations of the **electronic switch** performing the function of the CSS, and of the therewith associated circuit. Signal y will therefore over- (under)shoot the thres-

hold level v_T towards a new level v_T' which may, again, be time invariant as a whole, but could vary from pulse to pulse according to changes in supply line voltage, including a supply line ripple, loading and other external or internal effects. The, possibly, therewith associated dynamic effects are obvious.

An analogous process of PWM can be achieved if the functions of the clock signal and a signal z which govern the state of PM are interchanged. The threshold signal z will then initiate the individual pulses $e_s^*(k)$ and the clock signal will cause its termination. The functional inaccuracies, referred to in the previous paragraph, are eliminated, accordingly; an improved insensitivity against the described effects can be expected.

c. DPM for PW-PFM Processes.

The process of composite PW-PFM is illustrated in figure 5(d). It is used to advantage whenever a second degree of freedom to control the pulse modulation process becomes necessary or desirable. This mode of operation has also another valuable property: the controlled system remains for all practical purpose and within the limits of the intended frequency band, almost unconditionally stable.

This process can be mechanized by replacing the clock signal operating on BM shown in figure 36 by another signal derived from converter operation. The classical example is the warning signal of impending saturation of a transformer core, such as transformer X of the pulse modulated parallel inverter indicated in figure 8. Detection of impending transformer saturation is described in the literature [8, 9, 10, 11].

The ensuing signal flow is similar with the one discussed with reference to figure 37, except that the trigger signals shown under AM are not equally spaced but depend on the characteristics of the functional mechanics that generate these signals.

It follows that:

$$T_{ok} \neq T_{ok+1} \quad (2.10)$$

$$T_k \neq T_{k+1} \quad (2.14)$$

but,

$$\frac{A_k}{T_{ok}} = \frac{A_{k+1}}{T_{ok+1}} \quad (4.11m)$$

still guarantees the equality (5.1) based on the necessary satisfaction of (5.2). The therewith associated considerations were discussed under letter a. above.

d. Choice of the Mode of Operation:

Choice between the modes of pulse modulation indicated in figures 5 (a) through (d) depends, primarily, on external constraints.

d1. System synchronization with an external signal which is

d1a. periodic, requires application of PWM

d1b. aperiodic, requires application of PW-PFM

- d2. Minimization of the output filter in the absence of constraints d1. points to use of PW-PFM
- d3. Simplicity of control electronics can be achieved by application of PFM, provided constraints d1. and d2. are absent.

These general guidelines for the choice of systems are, furthermore, restricted by stability considerations including the cases of quasi DPM processes.

Certain significant functional concepts for use of DPM processes to control d.c. converters have been indicated. Their effect has been related to the requirements stated in chapters II and III, and the relations developed in chapter IV to meet these requirements. Limitations imposed by stability considerations will be briefly outlined under letter 5. of this chapter. Significant physical limitations are indicated in chapter VI.

2. Interaction with the Second Order Low Pass (LC) Filter.

The attenuation of low frequency components with order number $n < n_c$ of the source voltage function e_s caused by the process of deterministic pulse modulation is summarized in Table III and further elaborated on, in the therewith associated discussion. The open loop attenuation of the effects of the pulse modulation mechanism (h.f. components) is given by (4.18) through (4.20) with further expansion in (4.21) through (4.24).

The relative regulation effect ϵ_{RL} caused by the resistive element R_2 contained in the output filter inductance L_0 is quantized

in (4.25) and related to the filter inductor efficiency η_L in (4.26). Means for its mitigation will be indicated under number 3. of this chapter.

An important consideration is the magnitude of the high frequency components and their effect on the system stability. One of the significant effects of a high ratio ω_F/ω_o is, indeed, the mitigation of that h.f. output ripple, which enhances system stability.

The normalized harmonic coefficients a_{mn} caused by the chopping "disturbance" decrease with a ratio

$$a_m/a_1 = 1/m \quad (5.11)$$

as indicated in and discussed with reference to (4.20).

In view of (4.18) will therefore

$$V_{o1}/V_{oFm} \approx m^3 \quad (5.12)$$

which puts the significance of the first harmonic component of v_F defined in (2.3) once more in evidence.

3. Addition of Conventional Feedback Techniques.

There are several prominent reasons to want to add conventional feedback techniques to a d.c. converter system governed by deterministic pulse modulation techniques.

One is to reduce the relative output voltage error caused by resistance R_o of the filter inductor and, possibly, of other connecting wires. Related to this reasoning is the meeting of requirements for remote control which "extend" the resistive voltage drop effect beyond the terminals of the output filter capacitor C_o .

Another is the need to improve the dynamic characteristics of the system, especially when exposed to sudden load changes.

Figure 38 shows the symbolic diagram of a DPM controlled d.c. converter as shown in figure 33 to which an other feedback loop has been added. This "outer" feedback loop reduces the relative

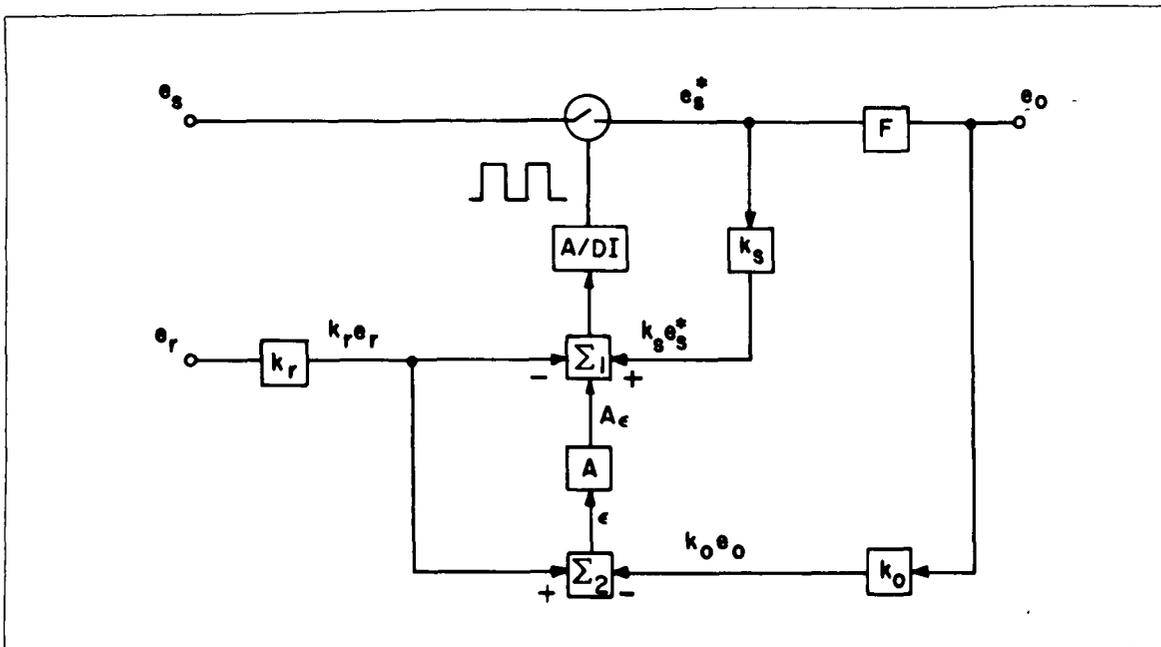


Figure 38.

Symbolic diagram of DPM controlled d.c. converter with added conventional "outer" feedback loop.

steady state error indicated in (2.26) and caused through the voltage drop v_R over R_ρ illustrated in figure 32, by a factor $|A + 1|$ such that the remaining relative system error

$$\epsilon_{RLA}/E_o = \frac{\epsilon_{RL}}{E_o(A + 1)} = \frac{1 - \eta_\rho}{A + 1} \quad (5.13)$$

where

$A > 1$ being the gain of the feedback loop.

The contribution to the output voltage error caused by the **physical limitations of the control electronics** is designated by ϵ_{ce} . Its effect is reduced by the factor $A + 1$ if an "outer" feedback loop is applied. There is no known way to correct an error ϵ_{cr} caused by variations of the reference source voltage e_r .

The cumulative effect of relative "d.c." output voltage errors

$$\epsilon_{o \max}/E_o = \left\{ \sum_1^P \epsilon_{pA} \right\} / 2E_o \quad (5.14)$$

in analogy with (2.8) where

$$\epsilon_{o \max} = \frac{1}{2}(v_{o \max} - v_{o \min}) \quad (5.15)$$

being the maximum deviation from the average level of output voltage and the individual error components

$$\Sigma \epsilon_{pA} = 2\epsilon_{o \max} = \epsilon_{RLA} + \epsilon_{ce} \quad (5.16)$$

The first component is defined by (5.13), the last one is due to inaccuracies of the electronic control system itself and will be elaborated on in chapter VI.

No other contributing effects than these cited above causing static errors in the output voltage e_o are apparent.

The area of static errors will be given further attention in chapter VI with reference to the discussion of experimentally obtained and recorded results.

The needed feedback gain A to attain a certain $\epsilon_{o \max}/E_o$ as defined in (5.16) can be expressed in an explicit form as:

$$A = \frac{1 - \eta_l + \epsilon_{ce}/E_o}{2\epsilon_{o \max}/E_o} - 1 \quad (5.17)$$

It was indicated previously in the discussion with reference to relation (4.26) that an "open loop" DPM controlled system with a 2 percent power loss in the inductor of its output filter would have a ± 1 percent output voltage variation only. No significance was then attached to the voltage variation ϵ_{cr} of the reference source and to the effects ϵ_{ce} of the control electronics network.

It is added that a fairly well compensated reference source will not vary by more than 0.001 % per $^{\circ}\text{C}$ temperature variation, in the average, and thus not more than 0.1 percent over a temperature range of 100°C which includes the room temperature.

It is, further, assumed at this time that for a given system

$$\epsilon_{ce} \ll \epsilon_{cr} \quad (5.18)$$

such as $\epsilon_{ce}/E_o \approx 2 \cdot 10^{-4}$ and $\epsilon_{cr}/E_o \approx 10^{-3}$ as indicated above. For these values and for $\eta_\ell = 0.98$ is according to (5.17)

$$A \approx 9 \quad (5.19)$$

in order that $\epsilon_{o \max}/E_o \approx 0.1$ percent, all other possible variations of external influences and changes in component characteristics included. This is an extremely modest feedback gain, considering the achieved accuracy. More will be said in section 5 about the effects of the feedback loop.

4. Effects of Quasi DPM Processes.

The DPM processes were primarily developed to control the power flow into second order filters, as stated at the outset of this chapter and as evident from the applied philosophy of control developed throughout chapter IV. It so happens, that this control system can be also applied to control the power flow into first order filters.

A customary LC low pass filter is meant here to be of second order if its characteristics can be described by a second order differential equation and if the energy storage capability of the constituting L_o and C_o , respectively, are comparable under full load conditions. A type 0 feedback system is commonly used to control a chopper system incorporating such a filter.

It is here for completeness briefly indicated that a pulse modulated parallel inverter-converter shown in figure 8 can be considered as being nothing else but a double ended chopper that feeds in that sense a second order filter through a transformer-rectifier. This type converter is also widely used for concurrent voltage scaling and stabilization. It provides, furthermore ohmic isolation between its input and its output terminals.

A low pass filter is defined here to be the first order if its characteristics can be described by a second or higher order differential equation but the energy storage capability of one single element utilized at full load systems operation exceeds that of each of the others by approximately one order of magnitude.

These conditions are found in converter systems in which electric energy is conveyed intentionally in discrete quantities to a capacitor C_o which maintains a relatively invariant voltage e_o at the systems output terminals.

a. The Series Inductor Converter.

A system that works according to that principle is illustrated in figure 39 in form of the series inductor d.c. converter, also often referred to as "fly back" or "energy ladling" circuit. A split inductor SI with polarity of windings as indicated by dots is "charged" with energy by closing the controlled sampling switch CSS. Current i_1 increases during time T_{k1} up to a given maximum value, when CSS is opened. The inductor terminals reverse polarities and the formerly back biased diode in the secondary circuit conducts current i_2 toward capacitor C_F and the load. This capa-

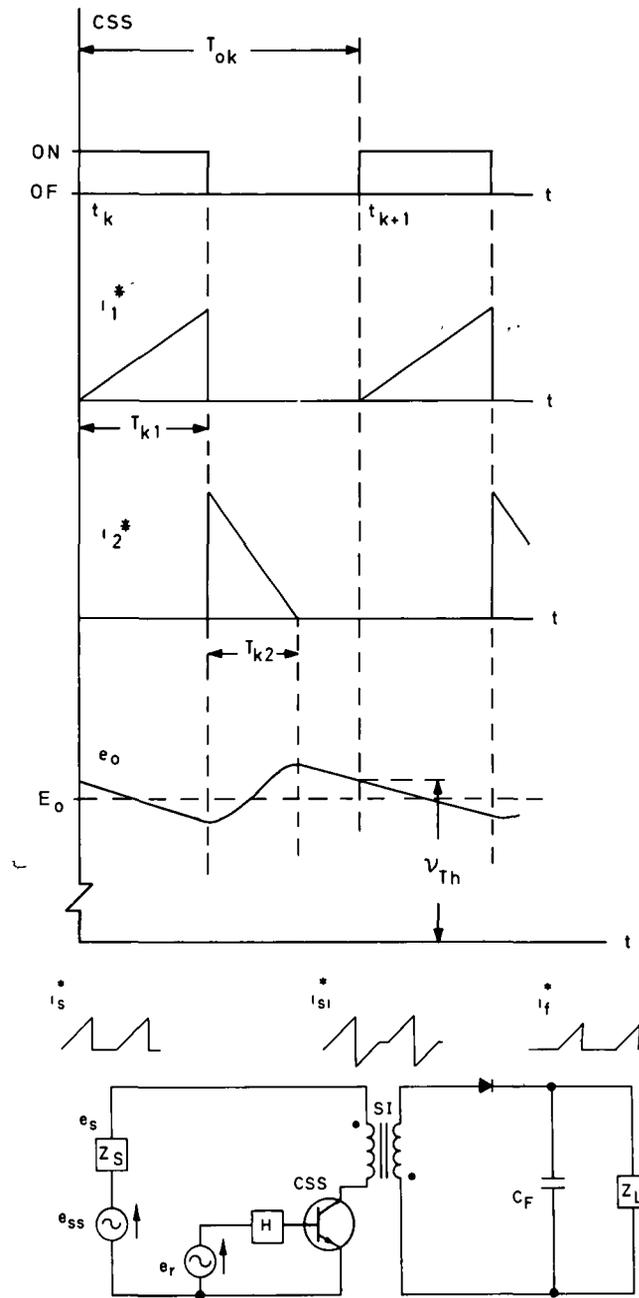


Figure 39.

Series inductor d.c. converter and its characteristic waveforms.

citor is large enough that the output voltage e_o vary only moderately during this operation. The ensuing output voltage is shown in the lowest curve, with its ripple exaggerated for purpose of clarity of presentation. When the output voltage decays from its maximum and reaches a threshold value v_{Th} , then the control system calls for another pulse and "charging" of split inductor SI by means of current i_1 is reinitiated. The split inductor derives its name from the fact at no time do the two windings carry current simultaneously which would create counteracting magnetomotive forces, a necessary requisite for transformer operation.

The just described type of control operation is often referred to as a "ripple regulator". Indeed, it is a regulator system and not a type 0 feedback system. The regulator distinguishes itself from the feedback system in that it calls for a resupply of energy for a given condition of its operational state. ~~This call for energy is independent of the magnitude of output voltage deficiency and no measure at all for an oversupply.~~

The regulator system is therefore clearly distinguished from ordinary feedback systems [7]. The energy storage capability of inductor SI is necessarily much smaller than that of capacitor C_F and its current i_2 has rather the form of a triangle with a negatively inclined hypotenuse, than to indicate remotely a resonance with capacitor C_F .

Such a regulator system possesses, necessarily, favorable dynamic characteristics. An over- or undershoot of the output voltage e_o is for all practical purposes impossible within the limitations of intended operation and beyond negligible output voltage ripple

variations caused by loading effects. These properties provide it with a high dynamic stability.

A signal which would be suited to acquire information on the volt-seconds per second that enter the output filter is not readily apparent. The system appears, therefore per se not suited for application of the DPM method. The system characteristics that are obtainable with that process make it, however, attractive to apply this method: for one that possibility to ~~get an exact~~ average voltage under all conditions of loading, not readily attainable otherwise; and then the zero steady state error availability, not to speak of hopes for improved dynamic characteristics.

A substitute is used for the missing signal referred to in the preceding paragraph [12]. The applied method of control is in principle identical with the one used to control a series capacitor converter by the DPM method. Therefore, the description of this method is continued in the next sections for that type of converter.

b. The DPM Controlled Series Capacitor Inverter-Converter.

A symbolic diagram of this converter and of the associated significant waveforms are illustrated in figures 40 and 41, respectively. This system can be controlled by a "ripple regulator system" just as the previously discussed series inductor d.c. converter; it is likewise suited for DPM control. The controllable - frequency modulated - series capacitor inverter-converter was first introduced with a second order filter in the secondary circuit [2, 3, 13, 14]. The forerunner of the DPM system was

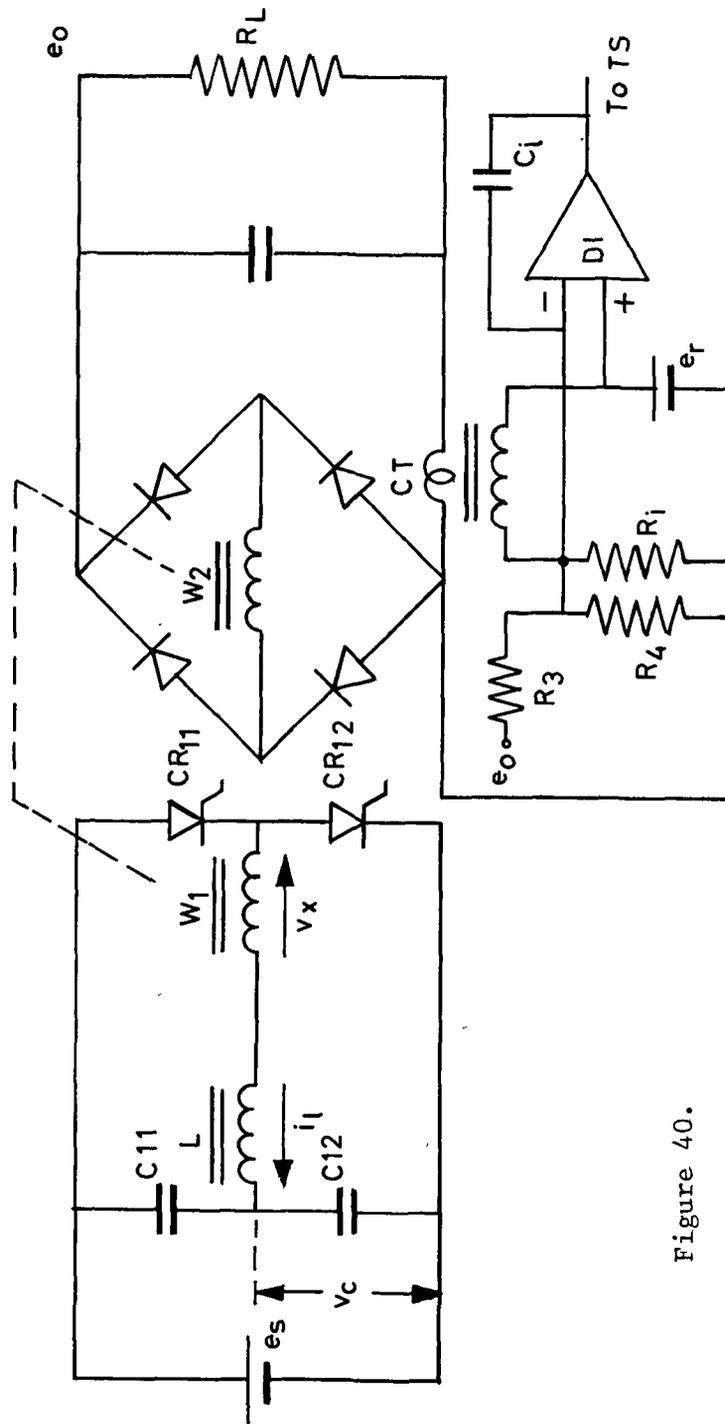


Figure 40.

Symbolic diagram of the load insensitive, controllable series capacitor inverter-converter with PDM control.

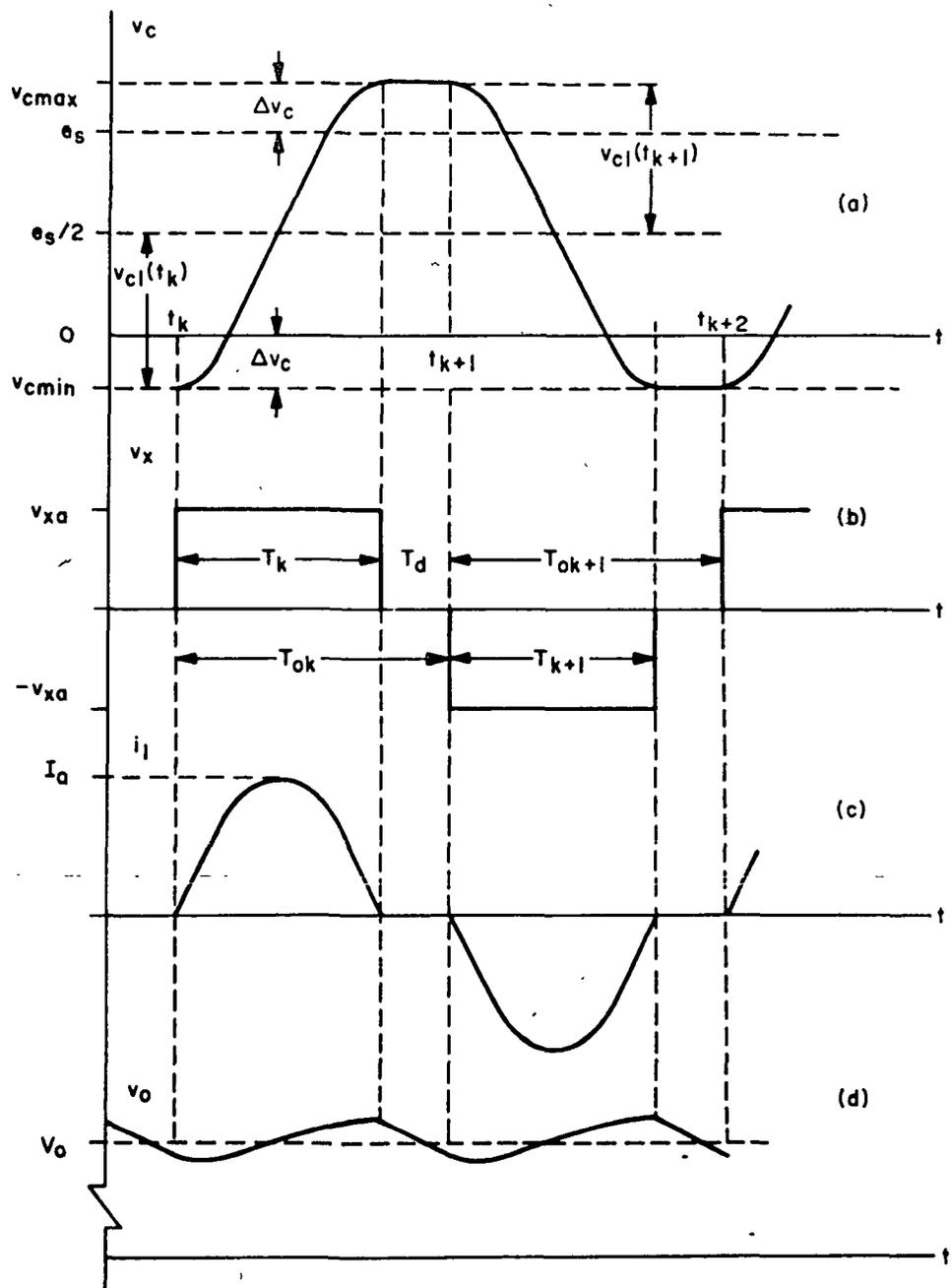


Figure 41.

Characteristic voltage and current waveforms of the load insensitive, controllable series capacitor converter.

used for its control. The inability of that system to operate under open circuit conditions, as all second order filter terminated systems do, led to the development of the illustrated system that would operate under open circuit conditions [15].

This system is operated through its inner control loop (see figure 38) as a current is sensed by current transformer CT and fed in considerably reduced magnitude into the integrating capacitor C_i (figure 40). This can be done with or without the interposition of a series resistor in the loop formed by the secondary winding of CT and the operational amplifier. The transformer operates as a current source into the "low impedance" point at the minus entry to the operational amplifier. The average voltage of that point is, necessarily, almost equal to the reference voltage e_r . All advantages of dynamic system behavior apply here analogously to the described cases of secondary voltage sources, but the output voltage e_o would remain undetermined. This is remedied by feeding the attenuated output voltage through a divider formed by resistors R_3 and R_4 to the operational amplifier, thus establishing a definite output voltage level using a stable Type I system.

The details of this technique will become more evident, after discussion of the physical aspects of the electronics which implement the DPM system. An amplifier which would limit the feedback signal can be used instead of the R_3, R_4 divider for better starting conditions.

At this time it is sufficient to say that DPM is used in the absence of a suitable signal, to operate the system as a controlled current source, and then to ascribe to the same system

a definite output voltage by application of direct outer loop feedback. The designation "quasi" DPM processes is used to describe this type of operation.

5. Dynamic **Stability** Aspects of DPM Systems.

One of the significant motivations for the development of DPM controlled d.c. converters was the desire to improve the dynamic characteristics of these systems, concurrent with their static stability (II.3). The powerful tool devised for that purpose is the process which forms the pulse train based on undelayed information available at the output filter input terminals to secure to a large extent, both, favorable static and dynamic characteristics as described throughout this presentation.

The advantage gained with this process is twofold:

- a. The pulse train $e_s^*(t)$ is shaped precisely at the spot of its formation and without relying on a process of successive convergence due to the delay time caused by the low pass filter, and
- b. A substantially lower feedback gain A is needed, if at all, to attain a required degree of static stability. This is, primarily, due to the mitigation and elimination of a number of effects requiring correction by feedback action in conventional systems, and due to PDM's tolerance of a Type 1 error integrating system without impairment of dynamic system stability (see number 3. above).

However, for all practical purposes, only the PW-PFM system is not

susceptible to subharmonic oscillations when controlling the input to a second order filter. Instabilities which manifest themselves in the form of subharmonic oscillations do occur in DPM controlled PWM and PFM systems under certain conditions which will be further described; they are characterized by a recurrent sequence of pulses that are too wide and too narrow for the PDM system. Yet the cumulative effect of two successive pulses is still in compliance with relations (5.1) and (5.2); the second relation is modified to read:

$$\int_{t_k}^{t_{k+2}} (k_r e_r - k_s e_s^*) dt = 0 \quad (5.20)$$

which is valid for PWM and PFM under conditions to be defined further on.

The static stability of the systems remains unimpaired. However, the h.f. ripple attenuation capability of the output filter is reduced by a factor $2^2 = 4$ and a certain unrest is introduced into the system which may affect its dynamic characteristics adversely.

One characteristic by which the indicated subharmonic oscillations can be recognized is the output waveform $y(t)$ of the integrator of the DPM system, as discussed with reference to figures 35 and 37. The subharmonic oscillation causes an alteration of the previously depicted waveforms and is indicated in figure 42. It is seen that a

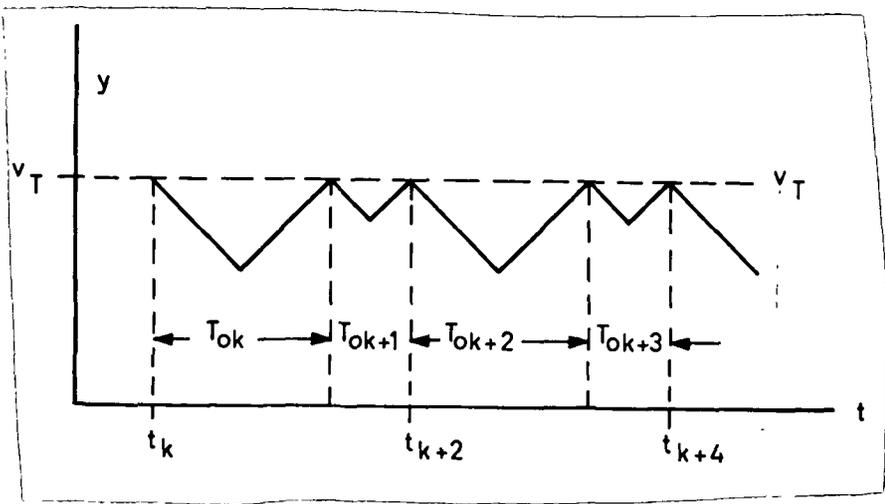


Figure 42.

Integrator output signal $y(t)$ during subharmonic oscillations of DPM systems. $T_{ok} = T_{ok+2} \neq T_{ok+1} = T_{ok+3}$.

pattern of unequal time intervals T_{ok} repeats itself regularly in pairs, while the intervals $t_{k+2} - t_k$ remain alike, with the tacit assumption that everything else remains equal for the sake of argument.

It can be shown that a DPM controlled d.c. converter will not develop subharmonic oscillations in the mode of

$$\text{PWM} \quad \text{if} \quad d_{ss} > 0.5$$

$$\text{PFM} \quad \text{if} \quad d_{ss} < 0.5 \tag{5.21}$$

$$\text{PW-PFM} \quad \text{for any} \quad d_{ss}$$

where

$$d_{ss} = \left. \text{the steady state duty cycle } T_k/T_{ok} \right|_{ss}$$

Many applications for d.c. converters ~~do not require~~ a steady state range for d_{ss} that approaches or ~~exceeds~~ 0.5; ~~they can~~ be used in these cases without alterations. Evidently, ~~one will~~ use the PW-PFM systems wherever compatible with externally imposed constraints, as listed under letter l.d. above.

The subharmonic oscillations under discussion can be avoided by injection of extraneous functions with zero average value into the signal flow discussed under l.a. and b. above. This could consist of a ramp function $r(t)$ where

$$\frac{1}{T_o} \int_{kT_o}^{(k+1)T_o} r dt = 0 \quad (5.22)$$

which is added to $k_r e_r$ or to $k_s e_s^*$ respectively [16]. This procedure is, in general, successful although the cause-effect relationship has not been analytically formulated. Injection of the signal and the therewith associated effects, especially under conditions of dynamic operation, can affect the functional mechanism of the DPM system, unless comprehensive precautionary measures are taken.

It is emphasized that the problem of subharmonic oscillations is characteristic to open loop operation of PWM and PDM systems under the conditions indicated under (5.21). It is, of course, found in the same systems, after "outer" loop feedback control is added as indicated under number 3 above.

The solution of the problem of subharmonic oscillations for PWM systems of the DPM type for any d_{ss} remains one of the desirable goals of further development.

Outer loop feedback control added to DPM systems leads to stability limitations which are comparable with those formed in conventional OFECDIC systems. The magnitude of the problem is considerably reduced, because only a fraction of the otherwise needed feedback gain A is required to obtain comparable results.

A comprehensive study into the feedback controlled DPM system, using PWM was carried out [17]. A sample of the results is shown in figure 43. The ratio $\omega_E/\omega_O = 50$, defined with reference to (3.2), governs the data shown in that figure, which are otherwise self explanatory. Symbol ξ designates the damping ratio of the output filter. The solid curves toward the right of the diagram indicate the "isotopes" of amplitudes of the steady state oscillations of the system; they are shown as far as they were discernible from other output voltage effects, such as the ripple caused by the internal converter mechanism. The smallest indicated amplitude is marked with 0.0003 or 0.03 percent, well within, usually, acceptable limits. These curves with increasing amplitudes give the impression of a topological ridge that builds up toward the right of the graph, and quite rightly so, since it is "forbidden territory" where increasing steady state oscillations indicate decreasing dynamic stability.

A brief review of the material under number 3. above indicates that a gain of approximately 10 in an outer feedback loop may suffice generously for most practical applications. It is seen from the graph shown in figure 43 that an appreciable distance

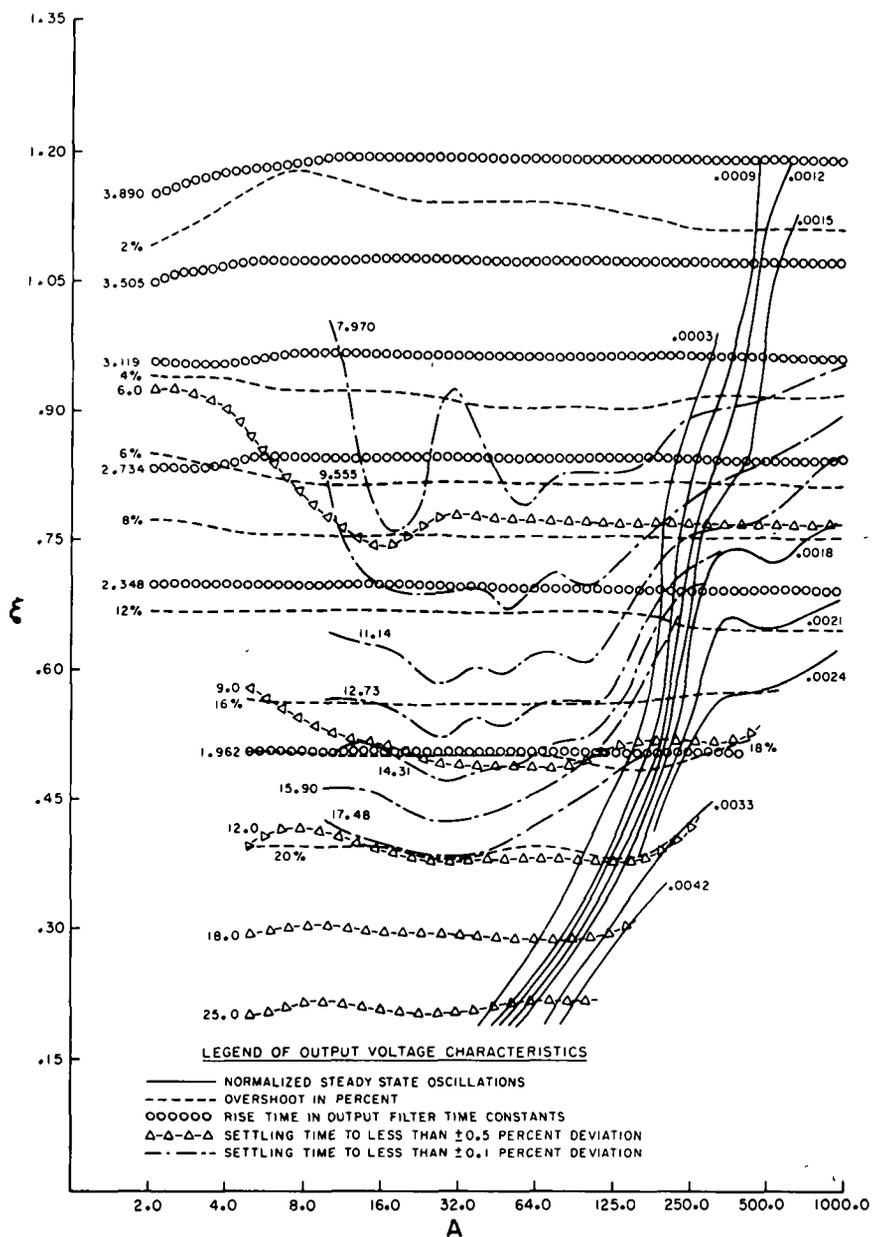


Figure 43.

Dynamic characteristics of DPM controlled d.c. converter for a ratio $\omega_F/\omega_O = 50$.

can be maintained from the "mountain ridge" for any damping coefficient for a gain $A = 10$. It is added that the "isotopes" of oscillations move to the right for increasing ω_F/ω_O , which is, in general, more common in modern d.c. converters.

A comprehensive treatment of this area, including a "design procedure for stable pulse modulated d.c. converters" could be carried out, based largely on an existing knowledge.

The designer of DPM system will, in general, find that the problem of devising a stable converter is greatly reduced compared to OFECDIC systems, because of the relative smallness of the required feedback gain.

The dynamic stability of first order systems, discussed under number 4. above is considerably more favorable than the one of second order systems. This is simply so because (a) no continuously closed LC circuit exists that could oscillate and (b) the intermittently connected L's and C's are connected during time intervals that are much shorter than their resonant period. They are nearly always stable when controlled in a regulator mode.

Use of a Type I error integrating system with these converters is solely possible because of the stabilizing effect of the current source control by the PDM mechanism.

Comprehensive analytical studies should be undertaken: to shed light on this area beyond classical engineering considerations, to provide the designer with tangible tools for the construction of systems with known margins of dynamic stability, or to prove unconditional stability.

VI. ELECTRONIC EMBODIMENT OF DPM CONTROL.

The electronics which implement the control philosophy of d.c. converters governed by DPM Techniques are presented throughout this chapter.

1. Functional Objectives.

An electronic control system for pulse modulated d.c. power converters is devised that satisfies:

- a. the requirements stated in (5.2) and can thereby attain the performance characteristics listed in Tables II and III.
- b. the necessary dynamic characteristics including source-load isolation as discussed under sections IV.4 and V.5.
- c. the requirement of time invariant performance of the control electronics. This includes, especially, a far going independence of the control electronics from the variations of the characteristics of its own components due to aging and changes in environmental conditions.
- d. the need for versatility for application to a wide variety of d.c. converter systems with various internal functional mechanisms.

Application of the principle of deterministic pulse modulation to a number of systems was explained throughout this presentation. It is recognized that the block diagrams indicating the various control systems contained largely the same elements.

An electronic control system that contains these common elements

and that could be programmed for these various purposes was devised. Its intrinsic functional mechanism, its properties and limitations are discussed in the following.

The primary objective is to clarify its functions and to relate them to the underlying principles presented in the preceding chapters. It is, furthermore, intended to provide engineering information for the design of PDM control systems and to identify areas of criticality that can exert a significant influence on the successful operation of the control system. A considerable amount of information on specific engineering aspects is described elsewhere [12].

2. The Analog Signal to Discrete Time Interval Converter (ASDTIC).

The results of mathematical analysis outlined in chapter IV in conjunction with the functional requirements described in chapter V formed the basis of a process of synthesis which resulted in the embodiment of an electronic control system, now known under the acronym ASDTIC.

The ASDTIC system which is one embodiment of control electronics for DPM applications to d.c. converters is discussed with reference to its operation within a PFM system. This discussion covers all essential aspects of this type control system. The various control configurations are obtained by rearrangement of certain functional blocks and appropriate interface elements. Figure 44 illustrates an ASDTIC system in its elementary form, yet containing all essential functions.

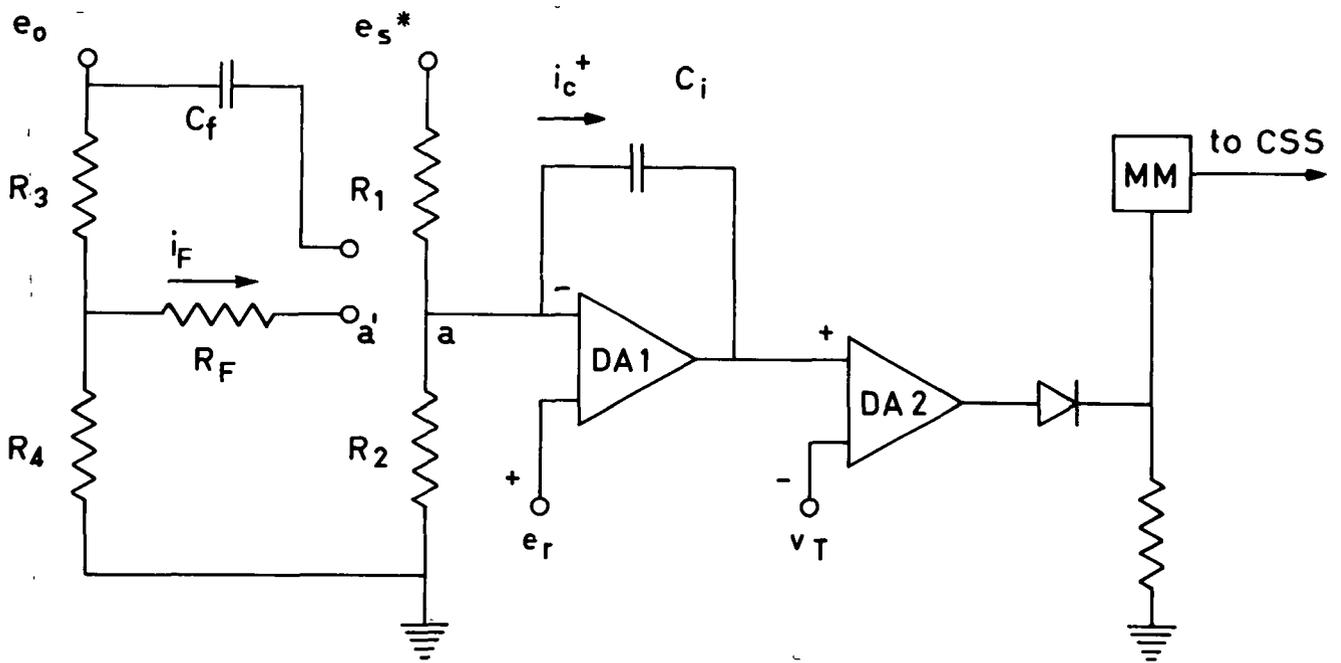


Figure 44.

Block and circuit diagram of the basic ASDTIC system.

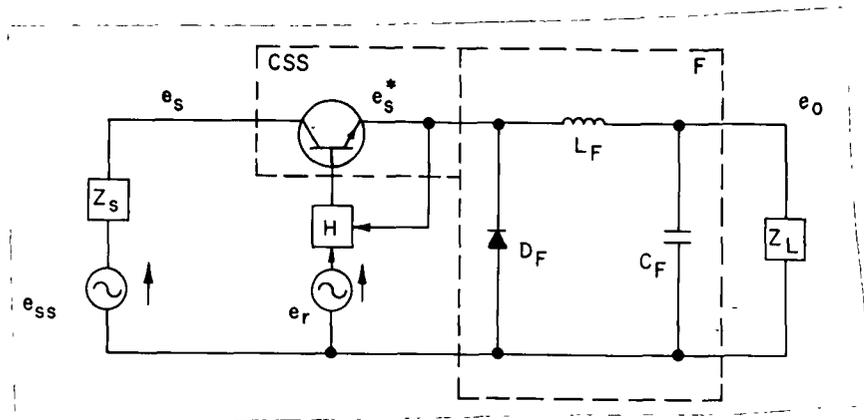


Figure 45.

ASDTIC controlled series chopper d.c. converter.

a. The Functional Mechanism.

The ASDTIC control system as shown in figure 44 and, possibly, augmented by a buffer to drive the controlled sampling switch CSS constitutes the control block H shown to govern a common series chopper illustrated in figure 45. Operation of the d.c. converter as a whole, and specifically that of ASDTIC will be discussed with reference to these two figures.

Signal e_s^* is fed through the voltage divider consisting of resistors R_1 and R_2 into the one terminal of the operational amplifier consisting of the differential amplifier DA1 and the integrating capacitor C_i . Signal e_r is connected to the other terminal of the

same operational amplifier. This amplifier serves thus concurrently as summer and as integrator as symbolically shown in figures 34 and 35; $R_2/(R_1 + R_2) = k_s$, being the attenuation constant used in (5.1). The threshold sensor is implemented by the differential amplifier DA2, which compares signal y emanating from the integrator (operational amplifier) with the threshold voltage level v_T . Threshold sensor DA2 emits a positive signal when $y > v_T$ and triggers the monostable multivibrator MM, which in turn emits a one (1) signal with duration T_k as indicated in (2.11). This signal closes the controlled sampling switch and a new pulse $e_s^*(k)$ is initiated.

A current i_c^+ will flow at that time t_k into capacitor C_i with magnitude

$$i_c^+ = (e_s - E_e)/R_1 \quad e_{s \min} < e_s < e_{s \max} \quad (6.1)$$

where

$$R = R_1 R_2 / (R_1 + R_2) \quad (6.2)$$

This current will cease when the monostable multivibrator MM releases CSS after its inherent pulse time T_k . Inductor L_F of the second order filter shown in figure 45 to which the upper terminal of resistor R_1 is connected will reverse its formerly positive polarity as soon as the pulse $e_s^*(k)$ ceases since $L_F di/dt < 0$ for CSS open with direction of current flow assumed toward capacitor C_F . The voltage at the input terminal of the low pass filter will fall until diode D_F is forward biased and closes the circuit consisting of itself, inductor L_F and the parallel combination C_F and Z_L .

Integrator capacitor C_i will during this conducting state of D_F discharge with a current

$$i_c^- = e_r/R \quad (6.3)$$

The input terminal of DA1 to which the capacitor C_i is connected is a "low impedance point" which does not change its potential perceptibly $|18|$. The current i_c^- will continue to flow from the capacitor C_i until the output voltage y of the operational amplifier has risen to $y > v_T$ and MM starts a new cycle.

Under conditions of cyclic stability must

$$T_k i_c^+ = (T_{ok} - T_k) i_c^- \quad (6.4)$$

or $y(t)$ would not return recurrently to the trigger level v_T . It is, of course, assumed that the current needed to operate DA1 - such as a FET differential input voltage - is so small that it is entirely negligible.

A nominal input voltage E_s as defined with reference to (2.3) is used here in place of e_s^* for clarity of presentation of the computation process. This input voltage is related to the nominal output voltage by

$$E_s T_k / T_{ok} = E_o \quad (6.5)$$

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Relation (6.1) is rewritten in the form

$$R_1 = (e_s - E_o) i_c^+ \quad e_s = E_s \quad (6.6)$$

and

$$R_2 = \frac{e_r R_1}{E_o - e_r} \quad (6.7)$$

The capacitor

$$C = \frac{e_r T_k}{\Delta y R} \quad (6.8)$$

where

$$\Delta y = y_{\max} - y_{\min} \quad (6.9)$$

as arbitrarily chosen between approximately one to several volts (see figures 35 and 37).

b. Effects of Physical Limitations.

A further requisite that (6.4) may hold is the virtual absence of a capacitor leakage current. Such a leakage current is always present, even in the best capacitor. It is desirable to keep i_c at least at a magnitude of approximately 20 μ a to minimize the effects of parasitic phenomena. A leakage current will be relatively balanced if the output terminal of DA1 is approximately balanced with respect

to the reference voltage level e_r . Small enough leakage currents may be entirely irrelevant.

It was indicated that one of the significant requirements to satisfy (5.2) on which the success of the ASDTIC system hinges is to satisfy concurrently (5.10). The validity of this expectation will be now investigated. The relative error ϵ_x that would be caused in terms of fractions in (5.2) is given by

$$\epsilon_x = \frac{|v_T(t_{k+1}) - v_T(t_k)| T_{ok}/\Delta t}{\frac{k}{T_{ok}} \int_{t_k}^{t_{k+1}} e_r dt} \quad (6.10)$$

where

Δt = the time over which a monotonic drift
 $\Delta v_T = v_T(\Delta t) - v_T(0)$ is recorded, such as caused
 by a monotonic change in ambient temperature

Relation (6.10) can be simplified if it is assumed that $k_r e_r$ remain constant during the interval Δt in order to examine the effect ϵ_x caused by the control electronics, excluding the contributing aspects emanating from the reference source e_r . Relation (6.10) then becomes

$$\epsilon_x = \frac{\Delta v_T T_{ok}/\Delta t}{k_r e_r} \quad (6.11)$$

where

$$\Delta v_T = v_T(t_{k+1}) - v_T(t_k)$$

If v_T has a nominal value of, say, 10 volts and would drift monotonically by 0.1 percent over a time interval of 10 minutes due to a monotonic change in ambient temperature; and if the effective reference voltage were $k_r e_r = 6$ Volts and the converter were to operate at an internal frequency of 10 kHz, then

$$\epsilon_x = 10^{-9}/396 \approx 2.5 \cdot 10^{-12}$$

It can be appreciated that even if v_T were to vary by one percent over seconds, a quite unfavorable assumption, then ϵ_x would still amount only to a few parts per million.

It is noticed in review that the change in v_T per cyclic interval T_{ok} determines the error ϵ_x and that even appreciable changes of v_T over finite time intervals would be negligible compared to other effects.

It is recognized, however, that periodic signals superimposed on v_T such as a 120 Hz ripple caused by a rectified a.c. supply line could have an effect on the performance of ASDTIC and introduce a comparable line ripple disturbance in the converter system output if the ripple signal on v_T were to carry such a ripple. Threshold level v_T should, therefore, be kept free of appreciable periodic disturbances, although a d.c. drift would have virtually no effect at all on the accuracy of an ASDTIC controlled d.c. converter system.

Another significant aspect of ASDTIC is the fact that all time delays in operating the threshold sensor TS, triggering the monostable multivibrator MM, turning on and turning off switch CSS can not cause an error in the system's static stability because

$$\int_{t_k}^{t_{k+1}} (k_r e_r - k_s e_s^*) dt < \epsilon_x \quad (6.12)$$

using (5.2) at its worst. The cyclic error ϵ_x defined by (6.10) and (6.11) is here extended to include all varying functional errors of the system; it amounts to fractions of one part of a million of e_r if any reasonable and by no means extensive precautions are taken. These could include the use of a voltage divider (v_T) with resistors made of similar material and stabilizing the control electronics supply voltage roughly by means of a simple series regulator. The fact that (5.2) and (5.10) are being satisfied, removes all errors caused by any mechanism in ASDTIC since the integrals of the scaled reference voltage $k_r e_r$ and of the scaled pulse train $k_s e_s^*$ must be and remain equal over every individual cycle and over any indefinite length of time. This fact guarantees unconditional static stability of the control system itself, and over appreciable and critical parts (CSS) of the power electronics system.

In order to improve the system's response to sudden load changes, it can be of advantage to add "steps" into the integration process of the operational amplifier. This is accomplished by feeding current from the converter output terminal with voltage e_o through a

feedback capacitor C_f directly to point "a". The otherwise ensuing normal integration process is sped up in form of a voltage jump on the integrating capacitor C_i and appears to have beneficial effects on the system behavior [16].

c. The "Outer" Feedback Loop.

The application of an "outer" feedback loop for further improvement of the system performance was indicated in V.2. The feedback effect is implemented by injecting a positive or negative current into point "a" at the junction of resistors R_1 and R_2 with the operational amplifier. The effect of a positive current i_F which is added to i_c , but which is, in general, unidirectional for a given cycle is that the total positive capacitor current

$$i_{ct}^+ = i_c^+ + i_F^+ \quad (6.13)$$

is now larger than the current caused by e_s^+ and current i_c^- becomes smaller than e_r/R as indicated in (6.3). The effect is that the integrator "sees" both e_s^* and e_r in modified magnitudes and the ampere-seconds balance indicated by (6.4) remains true with the appropriate substitutions of i_{ct}^+ and i_{ct}^- for i_c^+ and i_c^- , respectively, in order to achieve the intended feedback effect.

One way to inject such a current i_F into a point "a", is to attach a voltage divider consisting of resistors R_3 and R_4 to the converter system output terminals.

The ratio of these resistors is chosen so that

$$E_o R_4 / (R_3 + R_4) = e_r \quad (6.14)$$

No current i_F will flow through resistor R_F shown in figure 44 under these conditions if the right hand terminal a' of that resistor is tied to point "a".

The current i_o through resistors R_3 and R_4 is then chosen to be much greater than current i_F through resistor R_F , which is

$$i_F \approx \epsilon e_r / R_F \quad (6.15)$$

where

$$\epsilon = |e_o - E_o| / E_o \quad (6.16)$$

The feedback gain A is given by

$$A = \frac{i_F T_{ok} / E}{i_c + T_k} \quad (6.17)$$

Resistor R_F is then calculated by

$$R_F = \frac{e_s}{E_o} \frac{R_1}{A} \frac{e_r}{e_s - E_o} \quad e_s = E_s \quad (6.18)$$

Resistor R_F can be deleted completely if the appropriate Thevenin equivalent is used in calculating resistors R_3 and R_4 ; and so can resistor R_2 be combined with R_4 . In practice it is preferred to use separate resistors for purpose of circuit check out.

If it is desired to delete resistor R_F , then

$$R_3' = \frac{R_1}{A} \frac{e_s}{e_s - E_0} \quad (6.19)$$

and

$$R_4' = \frac{e_r}{E_0 - e_r} \frac{R_1}{A} \frac{e_s}{e_s - E_0} \quad (6.20)$$

The junction a' of R_3' is then directly connected to point "a".

The critical aspects for accuracy are:

- c1. A high quality reference source e_r in form of a temperature compensated Zener diode.
- c2. A good quality differential amplifier AD1 with minimum variation of the "zero" input voltage differential.
- c3. A high quality integrating capacitor C_i , such as the types made with mica dielectric materials.
- c4. Equal temperature tracking of resistor combinations R_1 and R_2 , and R_3 and R_4 , respectively.

All other component and material properties are of secondary importance.

For high feedback gains $A > 10$ it may be necessary to limit the current i_F derived by divider R_3, R_4 from capacitor C_i during the starting phase of the system.

The reason for this precaution is the necessity to get the input terminal "a" of DA1 into a position where its voltage approaches e_r to get the system operating. Standard "artifices" consisting of "pull up" transistors, delaying capacitors and diodes that are cut off eventually can be used for that purpose. The choice of such mechanisms rests with the designer.

A convenient technique to facilitate start up is to interpose between the junction of resistors R_3 and R_4 and resistor R_F an amplifier with unity gain, but with almost "perfect" tracking of input and output voltage. This amplifier serves as an impedance transformer. But above all it should have a current limiting output circuit, which could supply or accept no more than approximately thirty percent of the nominal value of i_c . Such an amplifier will facilitate the starting process, since it will permit initiation of systems operation. The feedback resistor is under these conditions given by (6.18).

The dynamic behavior of a DPM system with "outer" loop feedback as indicated in figure 43, with use of the characteristics of an amplifier is described in section V.5.

3. The Principle of Autocompensation.

The concept of an electronic mechanism was devised which eliminates the effects of most of the error causing phenomena in the control network.

It was indicated under 2.b. above that the system corrects its own errors due to the bounded nature of integral (5.20), which in fact amount to fractions of a part per million, although the cumulative

error of the control system itself is considerably larger when considered over an appreciable temperature range.

There is yet another aspect which strenghtens the static stability of this control system: Once signals $k_{s s}^* e_s$ and $k_{r r} e_r$ have entered the operational amplifier terminals (DA1), they are both being processed concurrently by the same components and enduring the same delays, distortions and whatever may happen to them until the final signal 0101.... emerges carrying its control information in form of analog discrete time intervals.

It will be, therefore, of little significance whether the total resistance of the voltage divider consisting of R_1 and R_2 varies with time or with temperature, whether C_i changes its value or whether v_T varies, since the integration path RC_i (6.2) is the same for charging and discharging capacitor C_i ; the amplitudes of the triangles in figures 34 and 36 may vary, but not the ratios T_k/T_{ok} as they would if the signals were processed separately. Such is, indeed, the case when an amplified feedback error signal is compared with a ramp function, as is usually the case; these two signals are then processed by different components with different variation of characteristics due to ageing and temperature and processed by different mechanisms with their individual idiosyncrasies.

It is, primarily, due to the facts that $\epsilon_x \rightarrow 0$ in (5.20) and that the compared signals are processed concurrently by the same mechanisms, that ASDTLC performs with a degree of accuracy, which is unusual for any electronic system (see section 5. of this chapter). This principle of autocompensation was first applied to magnetic amplifiers [19, 20] and later extended to electronic control systems.

4. Critical Design Aspects.

A number of significant critical design areas were outlined under 2.b. above. Several practical physical limitations are added.

One of the most cumbersome areas of physical electronics is the resistive voltage divider, especially when it should be adjustable and would carry high frequency components (MHz) of pulse signals with repetition rates in the order of tens of kHz. The first requirement is the use of uniform resistive material throughout such a divider, including the potentiometer needed for adjustment. Then follows the noninductivity of the resistors. A temperature stability is, fortunately, not necessary in this case; it is, however, desirable to choose resistors with dissipation ratings that are proportional to the actually dissipated electric energy, to enhance the development of comparable resistor temperatures.

Another source of errors can be found in the input current to the operational amplifier as indicated under 2.b. Variation of each $I_{c\ min}^+$ = 20 μ a over an extended temperature range can amount to an error of 0.01 percent, an appreciable error for a system with excellence of performance.

The electronic control system is presently limited by a maximum operating frequency of 50 kHz. It should be realized that the harmonic content of the voltage waveforms in and outside ASDTIC include frequency components reaching into the MHz range which gain significance, when measured against the high standards of accuracy of the system. Further development of electronic circuits, possibly, paired with improved functional concepts will be necessary to overcome the indicated limitation.

5. Test Results.

An experimental breadboard of a DPM controlled d.c. power converter was built in 1967 in the laboratories of the Electronics Research Center, NASA Cambridge, Mass. from unselected commercially available components and tested (see Appendix B). The results are shown in figure 46. The voltage v_z of a precision Zener reference diode with

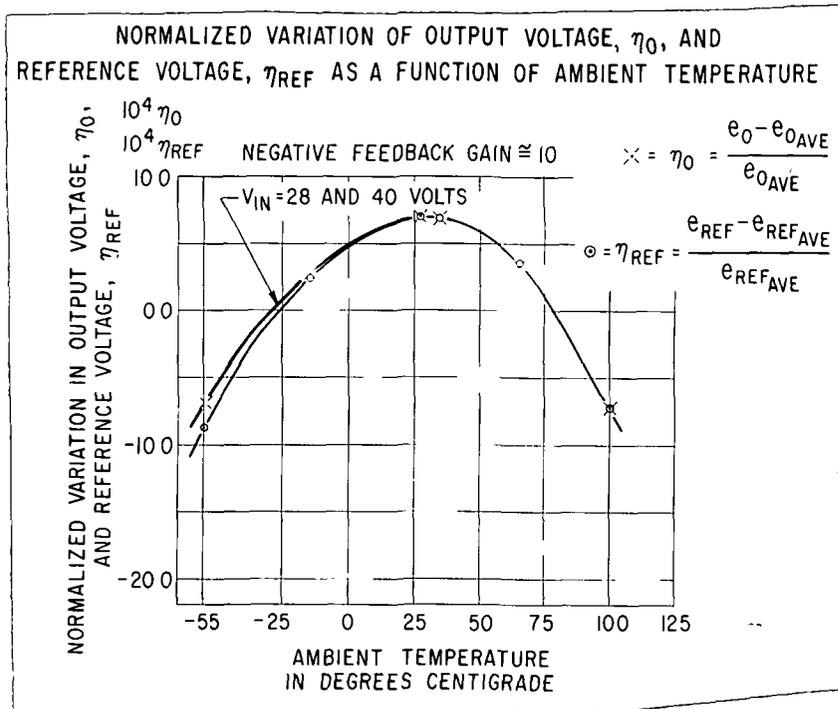


Figure 46.

Normalized variation of output voltage η_0 and reference voltage η_{REF} as a function of ambient temperature.

a temperature coefficient of 0.001 %/°C was measured over the ambient temperature range from -55 to +100 °C. The results were normalized in the indicated form as

$$\eta_{REF} = \frac{e_{REF} - e_{REFAVE}}{e_{REFAVE}}$$

where

$$e_{REF} = e_r \text{ used throughout this presentation}$$

and

$$e_{REF_{AVE}} = \text{the average value of } e_{REF}.$$

The output voltage e_o of the system was measured over the same temperature range; the results were normalized in a similar form, as indicated in figure 46. The results are recorded in units of $10^4 \eta_o$ or in 100 parts per million (ppm) for each indicated unit. The total variation of the maximum of the normalized reference source amounts to approximately 0.17 percent over the indicated temperature range. The curve indicating the normalized system output voltage voltages, expressed in equal units, coincides with the curve of the reference source, except at its left low temperature end where it follows it closely. No distinction between the results for an input voltage E_s of 28 and 40 Volts is apparent on that graph. It means that the output voltage variations due to a change in input voltage by approximately 40 percent were for a given temperature and loading not clearly discernible.

The absolute accuracy of the ASDTIC system was, therefore, more closely investigated, holding the reference voltage e_r constant (outside the environmental chamber) and then recording the variations in output voltage e_o of the converter system over the same ambient temperature range. The results are shown in figure 47. The indicated functions are here similar with those shown in figure 46.

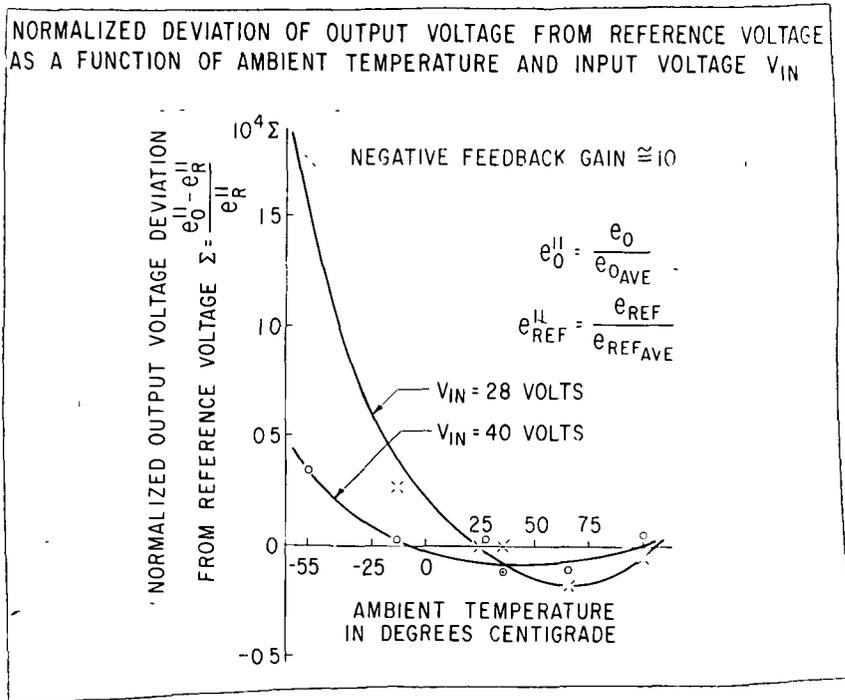


Figure 47.

Normalized deviation of output voltage from reference voltage as a function of ambient temperature and input voltage v_{in} .

The units are expressed in 100 ppm. A difference between the response to 28 and 40 Volts is now clearly discernible. The shown voltage variations are within a tolerance of ± 100 ppm. The larger variation at an input voltage of 28 V at low temperature resulted, primarily, from an appreciable base current variation of the DAI from 10 na at room temperature to 50 na at -55° C which caused more "damage" for larger T_k/T_{ok} at the low input voltage than for smaller T_k/T_{ok} at the higher input voltage.

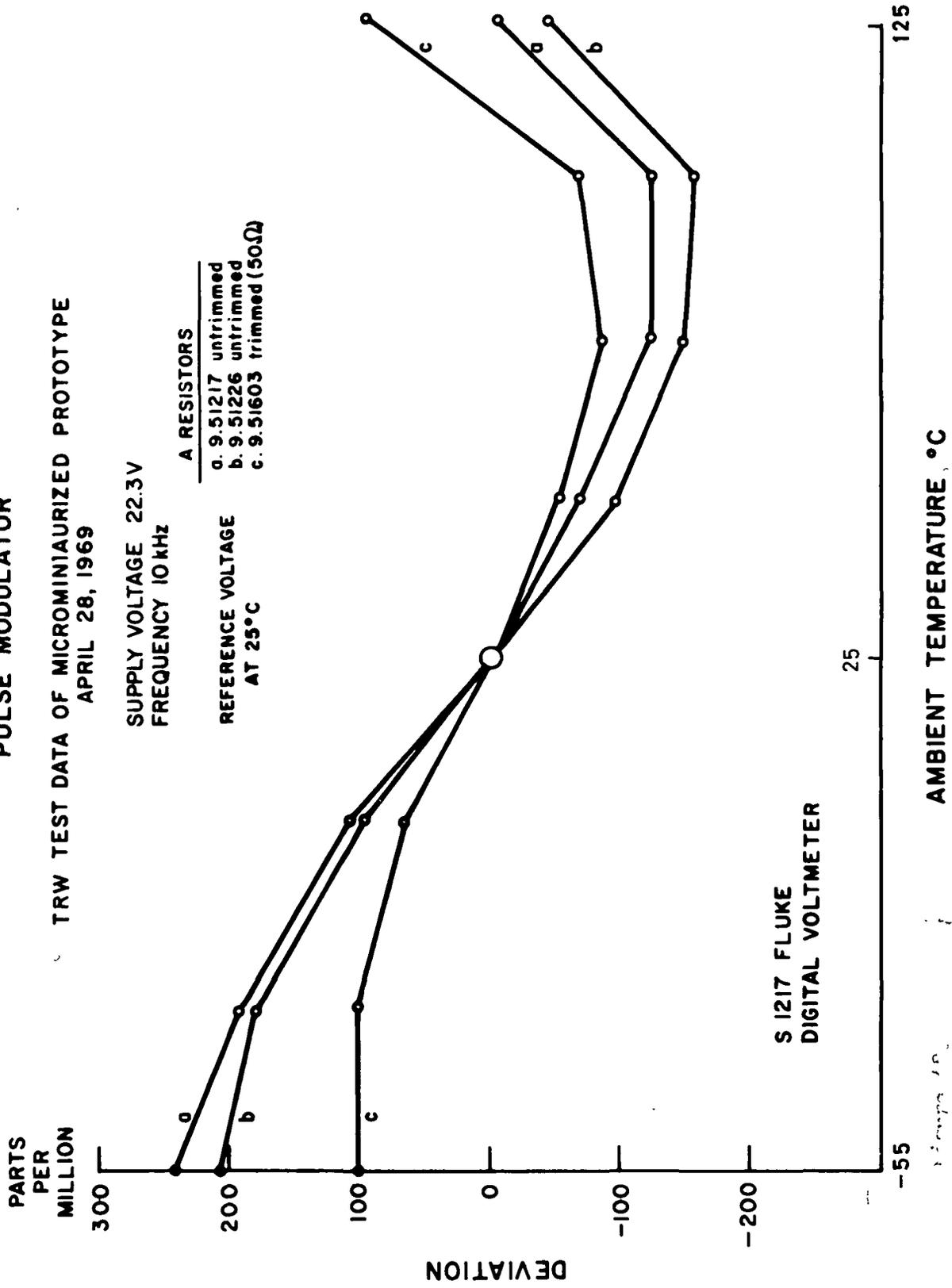
The ASDTIC system was subsequently microminiaturized in hybrid thick film form [4]. The resulting flat pack contains the essential ASDTIC functions: the operational amplifier, threshold sensors

for positive and for negative trigger levels, a feedback amplifier and a regulated internal power supply. External terminals allow tailoring of the functional block to the various applications by selecting the R_1 , R_2 divider, the integrating capacitor C_i , the R_3 , R_4 feedback divider and the feedback gain determining resistor R_F .

The test results of the microminiaturized flat pack are shown in figure 48. The flatpacks were provided with trimming resistors that could be burned out by external action for improvement of performance. The results are shown for the same unit before and after trimming; they are consistent with the results obtained with unselected discrete components, shown in figure 47.

ACCURACY OF ASDIC CONTROLLED
PULSE MODULATOR

Figure 48.



Accuracy of ASDIC Controlled Pulse Modulator

VII. CONCLUSIONS.

The analog signal to discrete time interval converter effort has achieved some of its goals. It has provided a functional block for the control of pulse modulated d.c. power convertors that can operate many of the currently used converters and provide them concurrently with considerably improved static and dynamic characteristics.

It has brought output voltage tolerances of 0.1 percent within the realm of common design, where 1 % was the accepted common standard before, and it provides unparalleled dynamic isolation from input voltage step or pulse disturbances (60 db). Through these properties it has found its use throughout U.S. Government programs carried out for NASA, DoD (U.S. Army, USAF) and DoT (FAA) in discrete part or in microminiaturized form.

Further improvements appear desirable: (1) to remove the barrier of subharmonic oscillations of PWM systems for $d_{ss} < 0.5$ (V.5), (2) to provide one functionally homogeneous system for bipolar operation with unequivocally determined (no dead band) conditions during zero cross over and reconciliation of mutual bipolar history, and (3) to increase the useful frequency range from the present 50 kHz to, at least, 100 kHz in anticipation of forthcoming faster and efficient converters.

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APPENDIX A.

Design Example of Converter System and ASDTIC Interface.

1. Statement of Problem.

a. Description of Process. ,

A resistive load R_L is to be energized from a secondary voltage source. The voltage e_o of this source is required to vary within close tolerances, as specified.

The prime energy is derived from one phase of an ordinary 60 Hz generator with appreciable variations of its voltage e_{acs} .

The process of voltage waveform transformation and the used complementary techniques are illustrated in figure A.1. The voltage e_{acs} of a.c. power, derived from the single phase supply line is first scaled by a transformer, then processed by a full wave rectifier, and subsequently smoothed by an "input filter" (IF). This input filter is so dimensioned as to cause a relatively high a.c. ripple content in its output voltage e_s . Filter IF is intentionally underdesigned for purpose of keeping its physical weight and size low, yet to provide it with an acceptable efficiency of power processing.

The converter-regulator which succeeds filter IF processes the power emanating from this filter with voltage e_s . Its pulse modulator performs a sampling process which decreases the low frequency components of order number n contained in e_s with coefficients E_{sn} (see 2.4) in such a manner that each harmonic component of e_s^* of

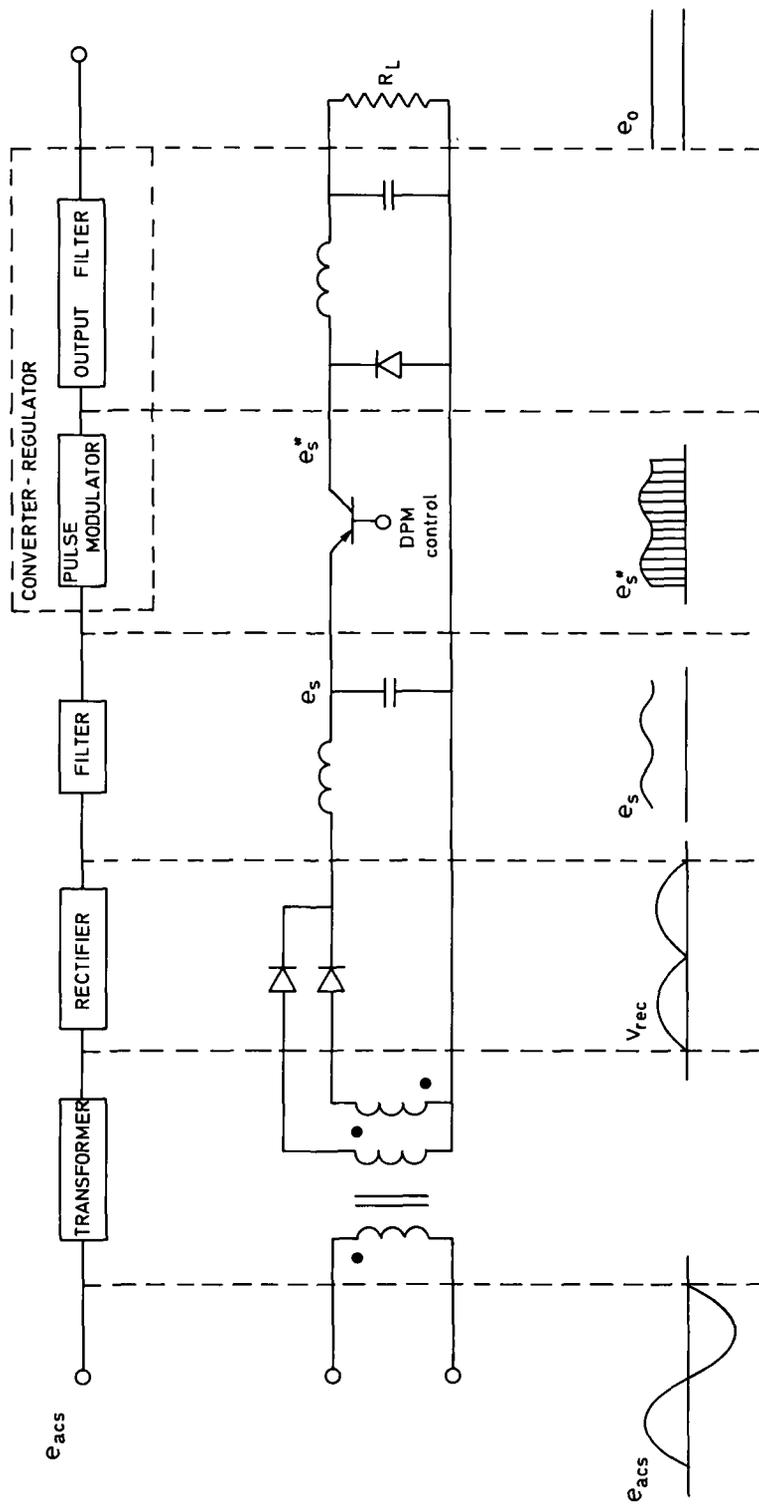


Figure A.1.
Transformer rectifier filter regulator system.

the same order number n is reduced at least to a prescribed level (discussed with reference to figure 15). Or, that the cumulative rms content of e_s^* for any frequency component with order number $n < n_c$ be confined to the given specifications of e_o . The output filter OF will have to reduce only the harmonic content of e_s^* which is caused by the sampling process itself at frequencies $f_{F \max} > f_F > f_{F \min} \gg n_c f_s$ where f_s is the fundamental frequency of e_s .

The result of this power processing method is the reduction of the size of filter IF by a factor a_d which signifies the attenuation of the harmonic content of e_s by the pulse modulation process. Application of this process is necessitated by the required control of voltage e_o . Attenuation of the E_{sn} and a drastic reduction of If is obtained by adding an additional task to the modulation process at no expense of physical weight and size of power processing efficiency.

b. Specifications.

b.1. Input voltage.

$$v_{\text{rec nom.}} = 32\{1 + 2[(1/3) \cos 2\pi 120t - (1/(3.5)) \cos 4\pi 120t - (1/(5.7)) \cos 6\pi 120t + \dots]\}$$

$$\text{Average: } e_{dc} = 32 + 6 \text{ V.d.c.}$$

Continuous

harmonic

$$\text{content: } e_{ac} = 10 \% \text{ rms of } e_{dc} \quad 120 < n f_s < 360$$

$v_{\text{rec nom}}$ is the nominal rectified source voltage e_{acs}

b.2. Output voltage.

Average: $v_o = 20(1 \pm 001)$ V.d.c.

Continuous

harmonic

content: $v_{os} = 0.00025 E_o$ rms $120 < nf_s < 360$

$$v_F = 0.00018 E_o \text{ rms}$$

Absolute maximum steady state instantaneous output voltage variation:

$$10^2 |e_o/E_o - 1|_{\text{max}} < 0.175 \text{ percent}$$

b.3. Output current: 2 to 10 Ampere average.

b.4. Ohmic isolation between input and output terminals not required.

b.5. Operating ambient temperature range -55 to 100° C.

2. System Design.

A pulse frequency modulated chopper system is designed to derive electric energy with a voltage e_s as indicated in figure A.1. This chopper will convert voltage e_s into an output voltage e_o with maximum variations

as required by the specifications under letter 1.b.2. and consistent with the other output power requirements.

The lowest chopping frequency $f_{F \min}$ with which the specifications can be met is established first. This chopping frequency is determined by the needed attenuation to reduce the low frequency harmonic content of e_s according to (4.14) to fit within the tolerances given for v_{os} in the specifications.

Voltage e_s has the average content e_{dc} as specified. Its harmonic content e_{ac} caused by the first three harmonic components of v_{rec} is indicated with 10 percent.

Voltage v_{rec} is related to e_{acs} by [6]

$$v_{rec} = \frac{2E_{acs}}{\pi} + \frac{4E_{acs}}{\pi} \left\{ \frac{\cos 2\omega_s t}{3} - \frac{\cos 4\omega_s t}{3.5} + \frac{\cos 6\omega_s t}{5.7} - \dots \right\} \quad (A.1)$$

The relative magnitude of the individual harmonic coefficients is listed as

$$1, 1/5, 3/35 \quad (A.2)$$

The second order input filter IF will attenuate the individual harmonic components of v_{rec} proportionally to the square of the order number n of their frequencies (3.2); n being 1, 2, and 3 in this case. The relative magnitude of these harmonic coefficients of e_s attenuated by IF is given by

$$1, 1/20, 1/105$$

Their relative contribution to the rms content of e_s is indicated by calculating the composite rms content of e_s in a conventional manner:

$$e_{ac \text{ rms}} = 0.1 E_s = \frac{E_{s1}}{\sqrt{2}} \{1 + (1/20)^2 + (1/105)^2\}^{\frac{1}{2}} \quad (A.3)$$

Relation (A.3) reveals that the contributions of the harmonic components with order number higher than 1 is approximately 1/1000.

This harmonic content of e_s will be even further reduced by the ASDTIC controlled pulse modulation process according to relation (4.14). Again, if E_{s1} is reduced by the pulse modulation process to a specific magnitude V_{os1} , then the relative magnitudes of the first three harmonic frequency components will follow (4.14) and be given by

$$1, 2/(20), 3/105 \quad (A.4)$$

such that proper interpretation of (A.3) and (A.4) and the specifications under 1.b.2. yields that

$$v_{os \text{ rms}} = 0.00025 E_o = \frac{V_{os1}}{\sqrt{2}} \{1 + (1/10)^2 + (1/35)^2\}^{\frac{1}{2}} \quad (A.5)$$

The relative significance of the harmonic components for $n > 1$ has increased, but their cumulative effect is still near 5/1000; it will be seen, further on, that an error of $\frac{1}{2}$ % becomes irrelevant for the accuracy of the design process itself.

It follows from the statements contained under 1.b.1. and 1.b.2. that

$$e_{ac} = 0.1 e_{dc} \text{ rms} \quad (\text{A.6})$$

and that

$$v_{os} = 0.00025 E_o \text{ rms} \quad (\text{A.7})$$

respectively require that the first harmonic coefficient E_{s1} of e_{ac} be attenuated by way of the pulse modulation process by a factor

$$a_T = 10/0.025 = 400 \quad (\text{A.8})$$

with allowance of another $\frac{1}{2}$ % of that number to account for the second harmonic component. The filter IF is designed to meet the requirements of (A.6); this design is not considered part of the problem at hand; relation (A.6) is simply postulated for purpose of this treatment.

The total attenuation a_{T1} of the first harmonic component of e_s is found by forming the product

$$a_{T1} = a_{s1} a_{d1} (A + 1) \approx 402 \quad (\text{A.9})$$

where

a_{s1} = attenuation of E_{s1} by the low pass converter output filter;

assumed is in this case that $a_{s1} = 1$ (no attenuation)

$$a_{d1} = N/\pi \text{ defined by (4.12)}$$

A = amplification of the converter's error feedback signal

The gain A of the feedback error signal ϵ is determined from its contribution to the static stability of the converter system expressed in terms of $|v_o - E_o|_{\max}$. This is preceded by evaluation of the other factors affecting the converter's static stability, being the error ϵ_{cen} of the electronic control system itself and the relative error $\Delta e_{r \max} / e_r = \epsilon_{\text{crn}}$ of the systems reference voltage source.

The maximum absolute relative ϵ_{cen} error of the electronic ASDTIC control system

$$|\epsilon_{\text{cen}}| = 0.0001 \quad (\text{A.9})$$

as indicated in figures 47 and 48.

A compensated Zener reference diode with a temperature coefficient of 0.0003 %/°C for the indicated temperature range centered around 25° C, is used for this design. The maximum relative deviation ϵ_{crn} of this voltage reference device from its value in percent is then

$$10^2 \epsilon_{\text{crn}} = 10^2 (0.0003) (100 - 25) = 0.0225 \text{ percent} \quad (\text{A.10})$$

The maximum relative steady state d.c. error ϵ_{v_o} of the output voltage e_o

$$\epsilon_{v_o}/E_o = |v_o/E_o - 1|_{\max} = \epsilon_{cen} + \epsilon_{crn} + v_{R_\ell \max} / 2(A + 1)E_o \quad (A.11)$$

as indicated with (A.9), (A.10), (4.26) and the therewith associated discussions. Relation (4.26) is introduced here in accordance with the discussion with reference to figure 32. It is assumed that the power loss in the inductor L_o is 2 % of the total power output (200 W) of the converter when fully loaded. The output voltage e_o would vary by 2 % between full load and no load conditions. This total error v_{R_ℓ} over the loading range of the converter which is due to the inductor resistance R_ℓ is halved after "centering" of v_o with respect to E_o , as discussed with reference to (4.26). The relative maximum "centered" normalized error due to R_ℓ ,

$$\epsilon_{R_\ell n} = v_{R_\ell \max} / 2E_o = 0.01.$$

In a closed loop feedback system with gain A is

$$v_{R_\ell \max} / 2(A + 1)E_o = \epsilon_{v_o} / E_o - \epsilon_{cen} - \epsilon_{crn} \quad (A.12)$$

or

$$\begin{aligned} \epsilon_{R_\ell n} / (1 + A) &= 0.001 - 0.0001 - 0.000225 \\ &= 0.000675 \end{aligned} \quad (A.13)$$

It follows that

$$A + 1 = \frac{\epsilon R_{\ell} n}{0.000675} = \frac{0.01}{0.000675}$$

and

$$A \approx 14 \tag{A.14}$$

With $a_{s1} = 1$ defined under (A.9) is

$$a_{d1} = a_{T1} / (A + 1) = 402 / 15 \approx 27 \tag{A.15}$$

The lowest pulse frequency $f_{F \min}$ is given by

$$f_{F \min} = N \cdot f_s \tag{A.16}$$

N being the number of pulses per period P_s with frequency f_s .
Use of (A.15) and (4.12) to solve (A.16) shows that

$$f_{F \min} = \pi a_{d1} f_s \tag{A.17}$$

and thus

$$f_{F \min} = (3.14)(27)(120) \approx 10,250 \tag{A.18}$$

pulses per second (pps). The lowest average pulse frequency of a PFM system occurs at the highest input voltage and at the lowest

load (2A); in this case when $e_{dc} = 38$ V. The highest pulse frequency $f_{F \max}$ occurs at the lowest input voltage and the highest load (10 A). If it is assumed that the system develops a series voltage drop differential of 5 % of the nominal output voltage E_o between lowest and highest loading, then it is necessary to increase the pulse frequency to a maximum

$$f_{F \max} = f_{F \min} (e_{dc \max} / e_{dc \min}) (1.05) \quad (A.19)$$

yielding

$$f_{F \max} = 10,250 (38/26) (1.05) \approx 15,700 \text{ pps} \quad (A.20)$$

In conclusion it is summarized that the 10 % source ripple is contained within the prescribed limits of 0.025 % rms of the d.c. output voltage and this d.c. voltage is stabilized within 0.1 % if (1) the converter is equipped with a maximum pulse frequency of 15,700 pps and an outer loop feedback gain $A = 14$. Reference is made to figures 2 and 3 and Table 3, and to the discussion with reference to these figures for elucidation of the treatment of this problem.

The lowest pulse frequency $f_{F \min}$ imposes in conjunction with the required processing of the first harmonic component of e_s an upper limit on the undamped frequency f_o of the system output filter. It is necessary that

$$\frac{a_1/a_o}{V_{oF1}/E_o} < (\omega_F/\omega_o)^2 \{ |(A+1)(\omega_o/\omega_F)^2 - 1|^2 + (2\xi\omega_o/\omega_F)^2 \}^{1/2} \quad (A.21)$$

with $\omega_F = \omega_{F \min}$. This is consistent with (3.1) through (3.3) and (4.19)

including the associated discussions.

The effect of the term under the one half power sign is neglected at first to arrive at a zero order approximation:

$$\omega_o < \omega_F \min \left\{ \frac{a_1/a_o}{V_{oF1}/E_o} \right\}^{-\frac{1}{2}} \quad (\text{A.22})$$

or

$$\omega_o < 2\pi 10,250 \left\{ (4/\pi)/0.00025 \right\}^{-\frac{1}{2}}$$

$$\omega_o < 2\pi 144 \approx 904 \quad (\text{A.23})$$

using the worst case expressed by $\gamma = 0$ in (4.20).

The ratio

$$\omega_F \min / \omega_o \approx 71 \quad (\text{A.24})$$

accordingly.

Introduction of the calculated value for ω_F/ω_o into (A.21) verifies the assumed neglect of the factor with the half power factor. The values of the components L_o and C_o are readily calculated from (A.24) and another design requirement such as inductor current continuity for the containment of ohmic losses [6] or any other requirement at the designers option.

The various converter output voltage components which cause deviations from its nominal value E_o are summarized for clarity in Table A.1.

Table A.1. List of Output Voltage Error Components.

(a) D.C. voltage level variations:

$$10^2 \epsilon_{R_l} = 0.066 \text{ percent}$$

$$10^2 \epsilon_{\text{cen}} = 0.01 \text{ percent}$$

$$\underline{10^2 \epsilon_{\text{crn}} = 0.024 \text{ percent}}$$

$$10^2 \Delta v_{o \text{ max}} / E_o = 0.1 \text{ percent}$$

(b) Harmonic content

i. rms values:

$$10^2 v_{os} / E_o = 0.025 \text{ percent rms}$$

$$10^2 v_F / E_o = 0.018 \text{ percent rms}$$

ii. amplitudes:

$$10^2 |v_{os \text{ ampl}}|/E_o = 0.038 \text{ percent}$$

$$10^2 |v_{F \text{ ampl}}|/E_o = 0.025 \text{ percent}$$

(c) Summary

$$10^2 \{ |\Delta v_o \text{ max}| + |v_{os \text{ ampl}}| + |v_{F \text{ ampl}}| \} / E_o = 0.163 \text{ percent}$$

3. ASDTIC Interface Design.

The value of the significant interface components with ASDTIC, namely R_1 , R_2 , R_3 and R_4 is established next. The minimum integrator capacitor current i_c that will be large enough as not to be appreciably affected by parasitic (leakage) currents, dominates these considerations. The lowest positive capacitor current

$$i_{c \text{ min}}^+ = (e_s^* - E_o)/R_1 \quad \left| \begin{array}{l} e_s^* \\ e_s \text{ min} \end{array} \right.$$

The positive capacitor current i_c^+ is at a minimum for the lowest value of e_s . This value

$$e_{s \text{ min}} = e_{dc \text{ min}} (1 - E_{s1}/e_{dc \text{ min}}) - v_{ce} \quad (\text{A.25})$$

where $v_{ce} = 1.2$ is the assumed voltage drop of the electronic switch during conduction. In numbers is

$$e_{s \min} = 26(1 - 0.1\sqrt{2}/26) - 1.2 \approx 21.1 \text{ V} \quad (\text{A.26})$$

The lowest positive integrator capacitor current is calculated from (6.1) and (A.26):

$$i_{c \min}^+ = 1.1 \text{ } \mu\text{a for each } 10^6 \text{ ohm of } R_1 \quad (\text{A.27})$$

From practice it has been learned that $i_{c \min}^+ \gtrsim 20 \text{ } \mu\text{a}$ is adequate to obscure the effects of leakage currents. The observed performance characteristics of ASDTIC contained in figure 46 has been obtained with a minimum current of that magnitude. This empirical experience is used to calculate

$$R_1 = \frac{1.1}{20} 10^6 = 55 \cdot 10^3 \text{ ohm} \quad (\text{A.28})$$

A resistor

$$R_1 = 62 \cdot 10^3 \text{ ohm} \quad (\text{A.29})$$

is chosen for this purpose for a current $i_{c \min}^+$ of slightly less than $20 \text{ } \mu\text{a}$. Resistor

$$R_2 = (8/(20 - 8))(62 \cdot 10^3) = 41.3 \cdot 10^3 \text{ ohm} \quad (\text{A.30})$$

according to (6.7), assuming $e_r = 8 \text{ Volt}$. This value of R_2 may have to be provided in exact magnitude unless e_r is adjustable by way of a resistive divider.

Capacitor current i_c^- is calculated from (6.3) using (A.29) and (A.30):

$$i_c^- = 8/(25 \cdot 10^3) \approx 320 \mu a \quad (A.31)$$

for $e_s^* = 0$. In actuality is $e_s^* < 0$ at the time when the "free wheeling" diode shown in figure 45 conducts the current i of inductor L_o . However, the integrator "sees" then the correct filter input voltage.

The nominal positive capacitor current

$$i_{c \text{ nom}}^+ = (32 - 20)/(62 \cdot 10^3) = 193 \mu a \quad (A.32)$$

The feedback resistors are calculated from (6.19) and (6.20) respectively

$$R_3' = \frac{62 \cdot 10^3}{14} \frac{32}{32 - 20} = 11.8 \cdot 10^3 \text{ ohm} \quad (A.33)$$

$$R_4' = \frac{8}{20 - 8} \frac{62 \cdot 10^3}{14} \frac{32}{32 - 20} = 7.9 \cdot 10^3 \text{ ohm} \quad (A.34)$$

Appropriate provisions have to be taken to prevent the feedback voltage divider to load down the integrator mechanism during the starting phase. The designer can use any of the common circuit techniques available for that purpose with special attention devoted to the prevention of leakage currents that would vary with temperature or with ageing of components.

The most effective manner to secure starting of the system with feedback in place is to mechanise it such that the sampling switch CSS remains closed for

$$e_o \frac{R_4}{R_3 + R_4} \ll e_r \quad (\text{A.35})$$

Voltage e_o then builds up from zero to some value which reduces this inequality (A.35) to an extent where converter operation can gradually start.

4. Comparison with Conventional Feedback Design.

An analogous systems design process as presented under section 2. above for the problem stated in section 1. is now carried out for a converter regulator with conventional feedback control (see figure 10).

For purpose of comparison of results it is assumed that both systems:

- a. meet the same specifications in each of their individual requirements.
- b. employ the same pulse modulation philosophy, PFM with the same maximum frequency $f_{F \text{ max}}$, which constitutes one of the critical physical limitations for any of the two systems.
- c. employ control systems:

- i. which are constructed of unselected commercially available components.
 - ii. whose circuits do not incorporate special techniques for the compensation of temperature effects.
- d. employ the same quality voltage reference source.

The accuracy of a conventional control system as described under 4.b. and c. above over the required temperature range is estimated with a maximum static stability of 0.02 percent. This appears as a favorable assumption, if for no other reason than the lack of application of a principle of autocompensation (VI.3) in the signal processing mechanism.

The errors ϵ_p which signify the deviations $v_{o \max} - v_{o \min}$ due to individual causes are defined in and discussed with reference to figure 3, Table III, and relation (5.15). These errors are normalized with respect to E_o and "centered" about E_o for purpose of the following treatment. The normalized (centered) error

$$\epsilon_{pn} = \pm \epsilon_p / 2E_o \quad (\text{A.36})$$

These "centered" errors will be used with the positive sign only for worst case analysis. The maximum normalized deviation of v_o from E_o is given by the summ

$$\Sigma_{pn} = \epsilon_{in} + \epsilon_{Rn} + \epsilon_{Tn} + \epsilon_{crn} + \epsilon_{cen} \quad (\text{A.37})$$

The specifications require under 1.b.2. that $\Sigma_{pn} \leq 0.001$. It was assumed above that $\epsilon_{cen} = 0.0002$; a normalized error $\epsilon_{crn} = \Delta e_{r \max} / e_r = 0.000225$ is indicated in relation (A.10) for analysis of the DPM system. The sum of the first three terms on the right hand side of (A.38) is found to be

$$\epsilon_{in} + \epsilon_{Rn} + \epsilon_{Tn} = 0.0001 - 0.000255 - 0.0002 = 0.000575 \quad (A.38)$$

The cause of each of the error components on the left hand side of (A.38) is considered next for purpose of finding a feedback gain A which will reduce their sum to the limit given by (A.38).

Error ϵ_i is caused by variations of the input voltage e_s ; its maximum total variation is expressed by

$$\begin{aligned} e_{s \max} - e_{s \min} &= 38(1 + 0.1\sqrt{2}) - 26(1 - 0.1\sqrt{2}) \\ &= 43.39 - 22.31 = 21.08 \text{ V} \end{aligned} \quad (A.39)$$

using the given specifications under 1.b.1. This system needs the capability to process all the recurrent variations of e_s including the excursions of the low frequency ripple symbolized by e_{ac} . It processes these variations as a "slowly varying d.c." which is a prerequisite for its functional capability to suppress or mitigate this harmonic content through the effectiveness of its feedback loop.

Errors ϵ_R and ϵ_T are due to the varying average voltage drops caused by the ohmic resistance of the converter between source and load. These effects have been assumed to cause a cumulative maximum

relative voltage drop of 7 % in the DPM system as expressed by relation (A.12) and (A.19). This is related to the respective output voltage error components by

$$A \cdot 10^2 (\epsilon_R + \epsilon_T) / E_O = 7 \text{ percent} \quad (\text{A.40})$$

since the feedback gain A will reduce the 7 % error to the allowable levels for $\epsilon_R + \epsilon_T$. Relations (A.39) and (A.40) are normalized and centered with respect to their average values in the form

$$\epsilon_{in} + \epsilon_{Rn} + \epsilon_{Tn} = (e_{s \max} - e_{s \min}) / 2AE_s + (\epsilon_R + \epsilon_T) / 2E_O \quad (\text{A.41})$$

This is reexpressed in numbers using (A.38) through (A.41) by

$$\epsilon_{in} + \epsilon_{Rn} + \epsilon_{Tn} = 21.08/64A + 0.035/A = 0.000575 \quad (\text{A.42})$$

Solving (A.42) yields

$$A = 0.365/0.000575 = 635 \quad (\text{A.43})$$

A feedback gain indicated in (A.43) will guarantee that

$(v_{O \max} - v_{O \min}) / 2E_O \leq 0.1 \%$ as required by the specifications under 1.b.2.

The lowest pulse frequency

$$f_{F \min} = f_{F \max} (e_{s \min} / e_{s \max}) / (1.07) \quad (\text{A.44})$$

The last factor in (A.44) signifies the contribution of (A.40)

to the required range since the series voltage drops expressed by (A.40) increase the effective input voltage ratio as viewed from the system's output terminals.

The requirement of equal $f_{F \max}$ stated under 4.b. and use of (A.39) leads to a numerical expression for (A.44) in the form

$$f_{F \min} = 15,700 (22.31/43.39)/(1.07) = 7,540 \text{ pps} \quad (\text{A.45})$$

The needed attenuation $a_{F1} = (a_1/a_o)/(V_{oF1}/E_o)$ of the relative magnitude of the first harmonic coefficient a_1/a_o caused by the chopping process requires satisfaction of relation (A.21). The second term under the half power sign is, again, initially neglected and reasoned that

$$\omega_{F \min}/\omega_o > (a_{F1} + A + 1)^{\frac{1}{2}} \quad (\text{A.46})$$

It follows from use of (A.43), (A.45), (A.46) and the last factor above relation (A.23) that

$$f_o < \frac{f_{F \min}}{(a_{F1} + A + 1)^{\frac{1}{2}}} = \frac{7,450}{(5.080 + 635)^{\frac{1}{2}}} \approx 100 \quad (\text{A.47})$$

The same value a_{F1} was used in the DPM case to contain the output voltage ripple v_{oF} within specified limits.

The frequency ratio

$$f_{F \min}/f_o \approx 76 \quad (\text{A.48})$$

A recheck of (A.21), using the numerical values contained in (A.45), (A.47), (A.48) and assuming that $\xi \approx 1$, confirms the validity of (A.46) and the therefrom derived results.

The relative low frequency content of e_o is restricted to

$$V_{os}/E_o \approx \frac{E_{s1}/E_s}{A} = \frac{0.141}{635} = 0.0222 \cdot 10^{-2} \quad (\text{A.49})$$

as indicated by (3.5). It is thus well within specifications. The critical condition for calculation of A was in this case the attainment of the required d.c. output voltage control accuracy.

Both systems studied in this Appendix have shown to meet the specifications of the example problem.

A comparison between selected critical functional aspects of the DPM and the conventional system follows next:

Symbol	DPM	Conventional	
A	14	635	
f_o	144	100	Hz

The LC product of an L type filter used, predominantly, in d.c. power supplies increases with the square of decreasing f_o since $(2\pi f_o)^2 = 1/LC$. It follows that the filter of the conventional

feedback controlled system will be $(144/100)^2 \approx 2$ times heavier than that of the DPM controlled system, everything else being equal.

The disparity of the needed feedback gains 635 vs. 14 entails more serious considerations. This increased gain is the cause for lowering the resonant filter frequency f_0 in order that its attenuation capability in the presence of A , indicated by (3.3) be maintained. But, the most important effect of the increased feedback gain is exerted on the system's dynamic behavior. This is discussed with reference to figure 43.

The feedback gain $A = 14$ associated with the DPM control system can be thought of as generating a vertical line on the graph in figure 43. which ends on the respective value indicated on the abscissa.

The significance of the individual curves is defined in and discussed with reference to figure 43. The vertical $A = 14$ is at a comfortable distance from the solid lines which indicate ~~unstable~~ system oscillations. The respective relative ~~amplitudes~~ $\sqrt{2V_0}/E_0$ are given in absolute values. A relative ~~step~~ ~~gradient~~ of 0.0003 or 0.03 % from line to line can be interpreted ~~moving~~ from right to left. The last line to the left of the group indicating a total amplitude of 0.03 % eliminates three such steps and points to a complete cessation of the unstable area which lies securely to the right of it. The system employing a feedback gain $A = 14$ will thus remain securely stable.

A choice of dynamic characteristics such as rise time, overshoot, ~~and settling~~ times is possible by selecting one point on the ver-

tical line $A = 14$. This point determines the loaded filter's damping factor ξ . Once ξ is chosen, then the second condition for determination of the filter component L_o and C_o as discussed under (A.24) is given. The results of this determination are unique for a given load R_L . This method can be used for design of d.c. converters with unequivocally predictable dynamic characteristics.

Application of a feedback gain $A = 635$ **for the given frequency** ratio $f_{F \min} / f_o$ appears to be marginally **feasible, at best**. A high degree of damping of the filter appears necessary for that purpose which leads to the expectation of a system with a sluggish response capability as often found in practice.

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SEPTEMBER 1968

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TITLE: Electronic Analog Signal to Discrete Time Interval Converter
(ASDIC)

NASA Work Unit: 120-33-08-11-25

Responsible Individual: F. C. Schwarz

OBJECTIVE:

Establishment of an electronic circuit technique that converts analog electrical signals into a succession of discrete time intervals according to a specific conversion philosophy. Control of pulse modulation mechanism in pertinent power systems. Variance in the characteristics of integrators, including ferromagnetic integrators - saturable reactors - should be substantially reduced by use of readily reproducible miniaturized electronic circuits. Improvement of accuracies by at least one or two orders of magnitude at higher frequencies of operation and considerable cost reduction are expected.

APPROACH:

The voltage waveform of a signal under consideration will be transformed into an analogous and linearly proportional current waveform. A capacitor will accumulate the latter in form of charge, or ampere-seconds; the time needed to charge the capacitor to a reference level is used to control the pulse forming switch. The nonlinear characteristics of circuit components including those due to temperature variations and aging will be used by way of autocompensation to counter balance the nonlinear effects within the circuit that are due to the characteristics of these components.

PROGRESS:

The objective of this program is to devise an electronic intergrator to be used wherever conversion of analog to digital signals is required, in particular for the purpose of transmission of an analog signal by use of pulse modulation and subsequent detection. Integrators of this kind are well known in the art, in particular the saturable magnetic reactors. This nonlinear inductive device is extensively described in the pertinent literature. These reactors do not appear well suited for high frequency applications because of apparent parasitic circuit parameters associated with wire wound electromagnetic devices that gain necessarily in significance when integration over shorter time intervals is required. Electronic integrators - usually RC integrators - are widely used. The volt-seconds of a sample of a function are converted to a corresponding time interval in the application under consideration. This process is, however, largely dependent on the invariance of component characteristics due to variations in environmental conditions, including ambient temperature and aging of components. It is the purpose of this program to devise

an integrator as discussed so far, but with the distinction of maintaining its accuracy of expected operation notwithstanding variations in its components characteristics, and variations of applied voltage waveforms and supply voltages within practical limits.

A circuit philosophy was developed that will vary the time base of its cyclic operation concurrent with the effects on the processing of signals that are due to variations of the characteristics of components included in this network. The read out of information from this network occurs against the same time varying time base. The former referred to effects of variations of components characteristics are in this way undone and the read out information is obtained as if the components had maintained their characteristics in an invariant form. It is this novel functional mechanism that distinguishes this approach from other networks of this kind which operate against preprogrammed time bases and are therefore, unable to cope with variations in the characteristics of their components. It is emphasized that this network philosophy utilizes the time variant characteristic of the same component to undo the effect of its own variation in characteristics rather than to call for compensation of these effects of its own variation in characteristics rather than to call for compensation of these effects by another component.

This circuit has been breadboarded and tested. It yielded remarkable accuracies of response over an ambient temperature range from -55 to 100°C, when operated in conjunction with the DC to DC converter. The deviations of the normalized output voltage from its average were recorded in the order of 10 parts per million of the variations of the normalized input voltage over the entire temperature range as indicated above. Review of limitations of instrumentation will be undertaken for purpose of consolidation of results. The normalized output voltage tracks the normalized reference voltage to a tolerance of less than .02% over the entire temperature range as indicated above. This indicates that DC power supplies with substantially higher accuracies than presently available could be devised when utilizing this novel method of control, provided better reference sources can be made available. A detailed treatment of the functional mechanism of this new network is contained in the ERC Invention Disclosure "Autocompensated Electronic Integrator" of February 21, 1967. Figs. 1-4 summarize test data.

A functional block diagram of the regulatory part of the control system is indicated in Figure 5 identifying the individual elements of operation. The elements shown within the dotted line are presently being reduced to microminiaturized form by an industrial contractor. A multi-purpose control system for power supplies that utilizes the network under consideration and could be applied to electric power converters employing either pulse width or pulse frequency modulator or so-called fly-back circuits has been devised. It consists of the network indicated in Figure 1 and another network that accepts, processes and finally channels the appropriate signals to the respective power circuit. The latter network, being called the "peripheral network" is

presently being hardened up and should enter the phase of microminiaturization during FY '69. Both networks and certain critical discrete components will be included in one electromagnetically shielded box with appropriate terminals for admission and transfer of signals. This complete network should make it possible to operate any of the pulse modulated power systems indicated before and reduce the cost of such power supply design considerably. It should also free the power engineer from the unfamiliar task of designing delicate and accurate analog and digital pulse circuitry for the purpose of control.

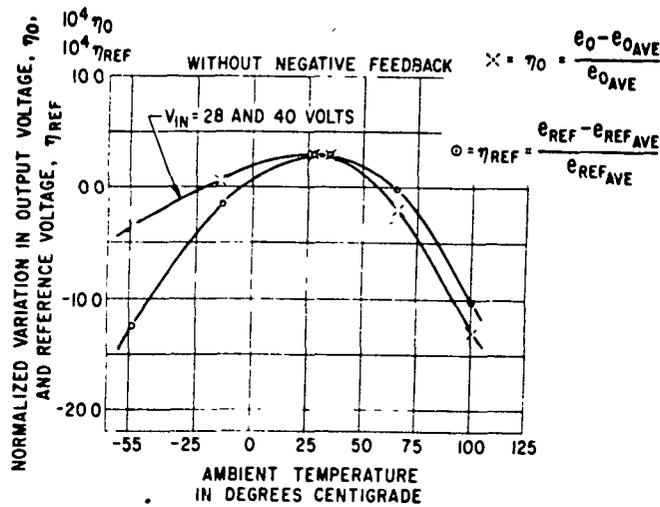


Figure 1.- Normalized variation of output voltage, η_0 , and reference voltage, η_{REF} as a function of ambient temperature

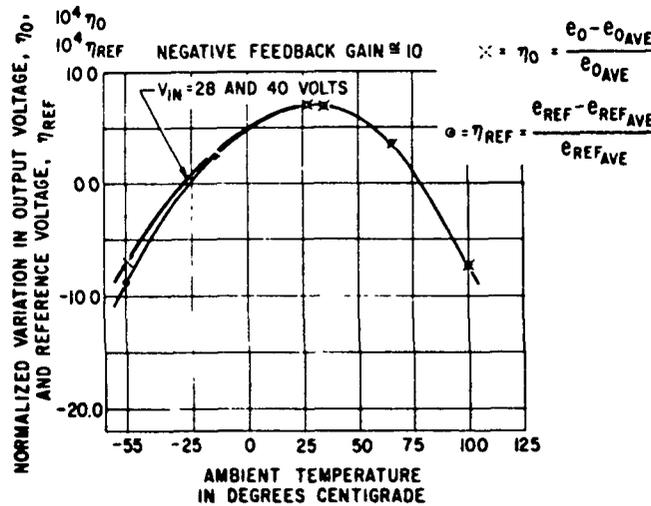


Figure 2.- Normalized variation of output voltage, η_0 , and reference voltage, η_{REF} as a function of ambient temperature

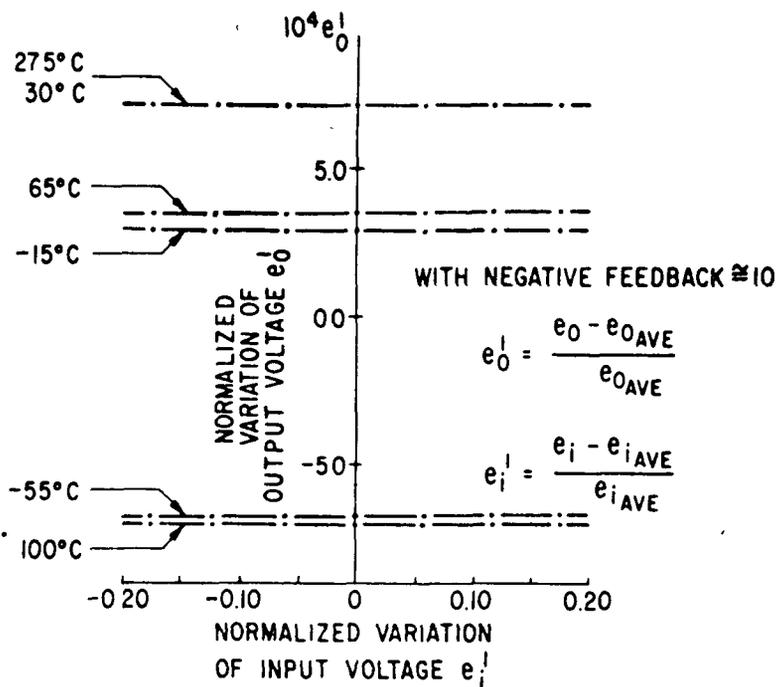


Figure 3.- Normalized deviation of output voltage e_0^I as a function of the normalized deviation of input voltage e_i^I and ambient temperature

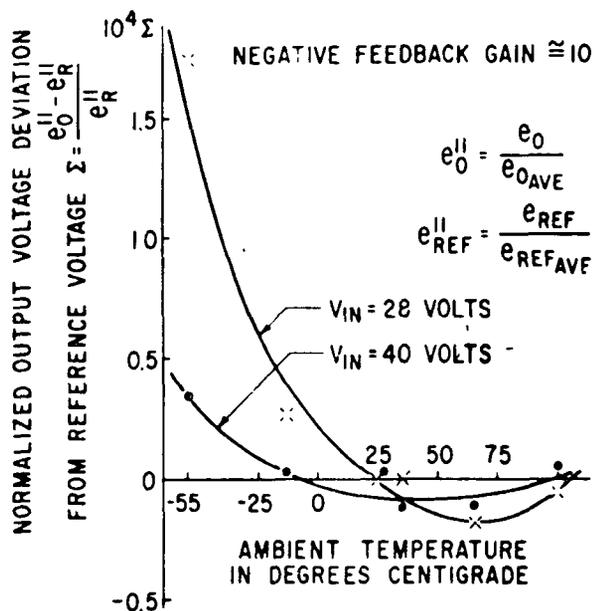


Figure 4.- Normalized deviation of output voltage from reference voltage as a function of ambient temperature and input voltage V_{IN}

APPENDIX C. Definition of Symbols.

Symbol	Definition
A	amplification of the feedback error signal $\epsilon = k_r e_r - k_o e_o$
a_{dn}	attenuation of the nth harmonic component with amplitude E_{sn} contained in the low frequency content e_{ac} of the source voltage e_s
A/DI	analog to discrete interval converter
A_k	area of the kth pulse in volt-seconds or ampere-seconds
a_{Fm}	attenuation of the mth harmonic coefficient a_m by the converter's low pass filter
a_m	mth harmonic coefficient of the pulse train e_s^* solely due to the mechanics of the sampling or pulse modulation process
$\underline{a_{mn}}$	a_m normalized with respect to the average value of e_s^* in terms of a_o
AM	astable multivibrator
a_o	average value of the pulse train e_s^* over the time interval (period) P_s of e_s
$\underline{a_{ln}}$	first harmonic component of the chopped waveform normalized for: $m_i = 0$; $T_k = T_{k+1}$; $T_{ok} = T_{ok+1}$
BM	bistable multivibrator

Symbol	Definition
B_k	volt-seconds (or ampere-seconds) area of output voltage e_o for $t_k < t < t_{k+1}$
β	angle in radians; equal to time in seconds for normalized voltage e_{i1}
$\Delta\beta$	time invariant, normalized time intervals with duration $2\pi/N$
β_k	sum of all normalized intervals $\Delta\beta_m$ for $m = 1, 2, \dots, k - 1$
$\Delta\beta_k$	kth normalized time interval $\beta_{k+1} - \beta_k$
CCS	controlled sampling switch
c_{in}^*	nth complex harmonic coefficient of the function e_{i1}^*
C_o	capacitance of low pass output filter
d	ratio T_k/T_{ok} , or "duty cycle" of pulse modulation process
d_{ss}	steady state "duty cycle" d
DA	differential amplifier
e_{ac}	recurrent variations of the source voltage e_s with zero average component in the steady state
e_{dc}	slowly and irregularly varying d.c. voltage component of source of electric energy
e_{in}	normalized voltage of source of electric energy e_s/E_s
e_{in}^*	train of samples derived from e_{in}

Symbol	Definition
E_{in}	amplitude of the nth harmonic component of e_{in}
e_{i1}	normalized voltage of source of electric energy including the fundamental component
e_{i1}^*	train of samples derived from e_{i1}
e_o	output voltage of the d.c. converter
E_o	nominal value of e_o
e_{omax}	absolute steady state maximum value of e_o
e_{omin}	absolute steady state minimum value of e_o
e_r	reference voltage of d.c. converter
Δe_r	maximum variation of reference voltage
$e_r(T)$	voltage of reference source as function of its operating temperature
e_s	voltage of source of electric energy
e_s^*	train of samples derived from e_s
e_{smax}	absolute maximum steady state value of e_s
e_{smin}	absolute minimum steady state value of e_s
e_{sav}^*	average value of e_s^*
e_{sac}^*	$e_s^* - e_{sav}^*$
E_s	nominal value of e_s

Symbol	Definition
E_{sn}	nth harmonic coefficient of e_{ac}
ϵ	feedback error signal
ϵ_c	maximum variation of e_o due to physical limitations of the governing electronic control system
ϵ_{ce}	variation of output voltage e_o due to variations in the control electronics
ϵ_{cr}	variation of output voltage e_o due to variations e_r
ϵ_i	maximum variation of e_o in response to the maximum variation of e_{dc}
ϵ_{max}	absolute maximum steady state deviation of voltage e_o from its nominal value E_o
ϵ_p	maximum variation of voltage e_o due to individual causes characterized by the subscripts $p = c, i, R, T$, respectively to
ϵ_{pD}	d.c. error indicators in open loop DPM converter
ϵ_{pF}	d.c. error indicators for open loop conventional feedback controlled converters
ϵ_R	maximum variation of e_o due to maximum loading of converter
ϵ_{RL}	output voltage error component caused by resistive voltage drop in L_o (maximum)
ϵ_{RLA}	remaining maximum error of DPM controlled system after addition of "outer" feedback loop with feedback error amplification A

Symbol	Definition
ϵ_s	steady state system error
ϵ_T	maximum variation of e_o due to cumulative effects of ambient temperature on converter power system components
ϵ_{TL}	output voltage error component caused by temperature effects on R
ϵ_x	output voltage error caused by drift of v_T
η_l	efficiency of output filter inductor L_o
f	frequency
f_{hf}	high frequency in the harmonic content of sporadic disturbances of the source voltage e_s
F	time invariant, passive, linear low pass filter
f_c	filter cut off frequency
f_{cp}	filter cut off frequency for the periodically sampled function e_{in}
f_{ca}	filter cut off frequency for the aperiodically sampled function e_{in}
$ F_{e_{inp}}^* $	magnitudes of the spectral lines of a periodically sampled normalized function e_{in}
$ F_{e_{ina}}^* $	magnitudes of the spectral lines of an aperiodically sampled function e_{in}
f_F	pulse or sampling frequency

Symbol	Definition
F_h	spectral lines of the Fourier expansion of a function h
f_o	undamped frequency of the converter's output filter
f_p	constant pulse or sampling frequency
f_s	fundamental frequency of component e_{ac} being a part of the source voltage e_s
f_{sn}	frequency of the n th harmonic component of e_{ac}
f_1	fundamental frequency of the Fourier expansion of a periodic function
ϕ_n	phase angle of the n th harmonic component of e_{ac}
g_k	time function describing the k th pulse
γ	asymmetry of square wave with period 2π in radians
H	control signal processing function
i	current in output filter inductor L_o
I_a	amplitude of current in series resonant circuit of series capacitor converter
i_{av}	average current
i_{rms}	r.m.s. current
i_c^-	current flowing out of integrating capacitor
i_c^+	current flowing into integrating capacitor
i_{ct}^+	total positive capacitor current

Symbol	Definition
i_F	feedback current
i_l	resonant current in series capacitor converter
k_p	k_i, k_T, k_c ; constants relating errors ϵ_{pD} to same errors ϵ_{pF}
k_o	time invaring attenuation of e_o for control operation
k_r	time invaring attenuation of reference voltage e_r for control operation
k_s	time invaring attenuation of e_s^* for control operation
m	index assuming the value of succeeding integers; often used as order number for frequency components of a function
M	an arbitrary constant of finite value
m_i	modulation index of e_{i1}
MM	monostable multivibrator
n	index assuming the value of succeeding integers with limits as indicated; often used as order number for frequency components of a function
N	number of samples or pulses per period $P_s = 1/f_s$ of the fundamental harmonic component of e_s
n_c	order number of the harmonic component $n_c f_s$ of the Fourier expansion with fundamental frequency f_s where $n_c f_s = f_c$ being the cut off frequency of a filter
ω_F	fundamental radial frequency of the effects of the pulse modulation process itself

Symbol	Definition
ω_s	fundamental radial frequency of the source voltage component e_{ac}
ω_{hf}	radial frequency of f_{hf}
ω_o	undamped resonant frequency of the converter's low pass filter
p	percent
PFM	pulse frequency modulation
PF-PWM	mixed pulse frequency - pulse width modulation
P_s	period of the fundamental frequency component of e_{ac} , a part of e_s
PWM	pulse width modulation
ψ_{Fm}	phase angle of the mth harmonic component of v_F
ψ_{sn}	phase angle of the nth harmonic component of the converter's response to the nth component of e_{ac}
Q	a constant such that $Q \sum_{k=1}^N e_{i1}(\beta_k) \delta(t - t_k) = 1$
r	ramp function
R	parallel combination of R_1 and R_2
R_F	feedback resistor
R_l	resistive component of output inductor L_o

Symbol	Definition
R_L	resistance of converter load
R_L f.l.	R_L at full load
R_1, R_2	resistors of voltage divider at input to integrator
R_3, R_4	resistors of voltage divider providing voltage feedback signal
R'_3, R'_4	Thevenin's equivalent of voltage divider R_3, R_4 feeding resistor R_F
ρ_i	current form factor i_{rms}/i_{av}
s	number of error components
t	time in seconds
T	constant width of idealized pulse (PFM)
T_k	width of kth idealized pulse
T_D	delay time between pulse turn on signal and attainment of 10 % of the nominal pulse height
T_F	pulse fall time from 90 to 10 % of its height
T_{ir}	intrapulse time
t_k	sum of all time intervals T_{om} for $m = 1, 2, \dots, k - 1$
T_0	constant time base
T_{ok}	time base of kth pulse
T_r	pulse rise time from 10 to 90 % of its height

Symbol	Definition
T_d	delay time between pulse turn off signal and its decay from 90 % of its height
TS	threshold detector
v_{ax}	transformer voltage amplitude
v_c	capacitor voltage (series converter)
Δv_c	$v_{cmax} - E_s$; $- v_{cmin}$ (series capacitor converter)
v_F	a.c. component of converter system response to internal pulse modulation process
v_o	slowly and irregularly varying d.c. voltage component at converter output terminals
V_{oFm}	mth harmonic coefficient of v_F
V_{oFmn}	V_{oFm} normalized with respect to E_o
v_{os}	converter response to a.c. source voltage component e_{ac}
V_{osn}	nth harmonic component of v_{os}
$v_{R, L}$	v oltage drop in the resistive component R of the output f ilter inductor L_o
v_T	threshold voltage
v_x	transformer voltage (series capacitor converter)
x	feedback error of d.c. converter
X	non-linear active filter

Symbol	Definition
ξ	damping constant of the converter's load terminated low pass filter
y	output signal of electronic integrator in control system
Δy	peak to peak value of y
z	output signal of threshold detector

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