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UNIVERSAL COMPUTER TEST STAND

(RECOMMENDED COMPUTER TEST REQUIREMENTS REPORT)

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UNIVERSAL COMPUTER TEST STAND

(Recommended Computer Test Requirements)

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ABSTRACT

RECOMMENDED COMPUTER TEST REQUIREMENTS

The objective of this report is to investigate techniques which would be used to characterize aerospace computers with the Space Shuttle application as end usage.

The first section surveys the system level digital problems which have been encountered and documented in several Aerospace Companies. Tests were then devised by these companies to discover the system problems prior to vehicle installation.

From the large cross-section of tests, an optimum set is recommended. The report demonstrates that this set has a high probability of discovering documented system level digital problems within laboratory environments.

The second section defines a baseline hardware, software system which is required as a laboratory tool to test aerospace computers.

The third section surveys the GSE equipment candidates and recommends the Unified Test Equipment (UTE) as the laboratory system to be considered for the computer test set.

The fourth section of the report contains hardware and software baselines and additions necessary to interface the UTE to aerospace computers for test purposes.

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I. SYSTEM PROBLEM AND TEST METHOD SURVEY

A. INTRODUCTION

The purpose of this study is to arrive at an optimal set of tests to be specified for the Universal Computer Test Stand (UCTS). The tests are to be optimized from a standpoint of test effectiveness, cost and efficiency to uncover digital system problems not normally found in subsystem quality testing.

To achieve this objective, the following guidelines were used:

- Discover and document actual digital system problems
- Compile a list of tests to uncover those documented problems
- Optimize and coorelate test and problem data

Digital Problem Survey. This survey was implemented to learn what types of system problems were found throughout the aerospace industry. This gave the survey team an opportunity to document the problems and to have a documented baseline from which to choose system tests.

Test Compilation. The tests to detect the problems surveyed were also documented during the "Problem Survey". A large list (37 individual tests) was generated which, if all were implemented on any tester, would require a large amount of time and money.

Optimization and Data Correlation. To reduce the test and problem data to a usable economical form, an optimization technique was used. The Optimization technique which was used was implemented with various weighted criteria and analyzed with a test criterion function equation.*

*Woodson, T.T. Introduction to Engineering Design, pp 202-235; 1966; McGraw Hill Inc.

B. STUDY IMPLEMENTATION

To achieve the study objective it first became necessary to find and document those problems encountered in computer installations. With this completed, it was possible to generate a test list from the survey comprised of various tests designed to uncover the documented problems. It is impractical to design a test for each problem individually. However, by grouping problems of similar nature (i.e. EMI, grounding), tests can be developed to cover a problem category. Thus, there was a need to group problems into categories. At this point the list of problems was divided into categories. The problem categories were compared to the test groups to find an optimal set of tests. A test weighting criteria was established to eliminate the least effective tests. Considerations for the test weighting criteria includes the following:

- Cost
- Test Effectiveness
- Problem Severity

Cost - Cost is considered because it will have a direct impact on UCTS hardware cost and test time. Tests which require hours of test time or large quantities of hardware should have low priority considerations.

Test Effectiveness - This criteria is rated against each of the nine problem categories to determine how well the test uncovers the particular problem category. For instance, a test which is only meant for EMI will not be effective against a hardware type problem such as a broken connector pin.

Problem Severity - This criteria considers the severity of the problem in terms of four problem weighting criteria: difficulty of isolation, frequency of occurrence, mission criticality, and safety criticality.

The following example shows the reasoning that made it necessary to consider problem severity. If, for example, Test 1 covers only problem Category A and Test 2 (same cost as 1) covers only problem Category B and each test covers their problem category equally well, which test is better? If problems in Category A are more critical (severe) then Test 1 should be rated higher.

With these three criteria selected, a method was derived to incorporate them into a meaningful test rating figure for each test. These rating figures will then permit the selection of an optimal set of tests.

C. GENERAL

The following summary will detail the implementation of the test study. The summary is divided into five major sections.

(1) System Problem Survey and Analysis

(2) Compilation of System Test and Analysis

(3) Baseline Tests

(4) Conclusions

(5) Recommendations

(1) System Problem Survey and Analysis

This section includes system problems not normally found during Acceptance Tests, but found during system integration. The problems were categorized into nine (9) groups. The groups were then analyzed and weighted against each other to determine the degree of severity for each group. The degree of severity is on a scale of 0 to 24 where 24 indicates a most severe problem and 0 would be the least severe.

The severity of problem group was used as an input to determine the optimal group of tests.

(2) Compilation of System Test and Analysis

This section consists of a test list and the analysis of that list. Each test was given an efficiency rating from 0 to 1 for each problem category. A test that was judged to be very effective in uncovering a type of problem was given a high efficiency rating (near 1) for that problem category.

Considering the efficiency rating, problem severity, and cost, a list of highly efficient tests are recommended for the purposes of evaluating Space Shuttle candidate computers.

(3) Baseline Tests

This section contains a list of functional tests which were deemed a minimum requirement to gain insight into the performance of each candidate computer.

(4) Conclusions

The results of the problem and test survey are presented including the recommended optimum test list and the minimum baseline tests to be performed.

(5) Recommendations

A recommended list of tests and procedures are presented in this section.

D. PROBLEM SURVEY AND ANALYSIS

1. Introduction

This section includes the list of System integration problems which were compiled from several sources categorized and weighted as to severity.

2. Background

The main purpose of the UCTS is to detect problems generally not found until the computer is installed and operational. It is therefore felt that the purpose of the UCTS is to find those problems that have previously gone undetected through qualification tests, but were then found during system integration testing. This background led to the different weighting factors which were assigned to the problem analysis criteria.

3. Object

The object of this survey is to obtain from several sources, information which pertains to system problems not normally detected during final factory Acceptance Testing. Data was obtained from several sources within the General Electric Company, from Grumman Aerospace Corporation and from Apollo History documents. Listed below are the various sources from which digital system problem data was obtained:

a. General Electric, Aerospace Electronics Systems Dept., Utica, NY

b. General Electric, Ordnance Systems Division, Pittsfield, Mass.

c. General Electric, Space Systems Operation, Valley Forge, Penna.

d. General Electric, Apollo Ground Support Dept., Houston, Texas

e. Grumman Aerospace Corporation, Bethpage, Long Island, N.Y.

f. Apollo Problem History Report, compiled by Draper Laboratories at Massachusetts Institute of Technology.

Due to the nature of the information gathered from the above sources, the specific programs cannot be revealed. Appendix A contains a complete list of the problems surveyed.

4. Results of Survey

Table 1 shows the results of the problem survey. It is shown that the various problems fit into categories with four (4) to eight (8) individual different problems in each category. These categories are listed below:

Design	Memory	Hardware
EMI	Noise	
Grounding	Power	
I/O	Software	

Within each category there are two subcategories which describe the problem symptom and the eventual cause of the problem. These two categories were used to analyze the problem severity and will be discussed below. It was found that after obtaining data from more than two of the above sources, the problems started to repeat. For instance,the problem symptom of "computational errors" under the category of NOISE was documented twice by the survey team as shown in Table 1 by the two in parenthesis (2).

Once a large percentage of individual problems exhibited similar characteristics, it became meaningless to continue the survey.

5. Analysis of Data

5.1 Introduction

The data as previously noted was divided into nine categories. An individual problem, however, because of its complex nature might appear in more than one category. An example of this is the "computer stoppage" symptom which appears in the Design, EMI, Noise Power, software and hardware.

Several problems were classed in more than one category. An example of this is the case ground to signal ground isolation problem. This was categorized both in EMI and Grounding. As a result, a circled number appears next to this problem. A circled number next to a problem indicates that this problem is categorized elsewhere in Table 1.

Once the entries were categorized, it was necessary to determine which category of problems was more severe than others so that these values could also be used for test organization. In order to determine this, a problem severity concept was adopted using the following criteria:

- Difficulty of Isolation
- Frequency of Occurrence
- Mission Critical
- Safety Critical

Weights were assigned to each of the above criteria based on the importance of each with respect to the objective of the study. The study objective as pointed out above is to find the optimal test which will be the most cost effective to test the most severe problems.

5.2 Weighting Philosophy

Those problems that are most difficult (and therefore expensive) to find are the problems that will obtain the most attention by the UCTS. For this reason, the first (of a final four) problem weighting criterion was developed. This criterion, termed Difficulty of Isolation (DI) was given a maximum rating of 10. If a problem was hard to isolate, it would receive a DI of 10, if not so difficult, such as a broken wire, the DI might be 2.

It was felt that emphasis should be given to problems that occurred often within any one category. This frequency of occurrence concept should be closely tied to difficulty to isolation as it is only those problems that are difficult to isolate that are going to be well documented and, as a result, covered in the problem survey. The Frequency of Occurrence (FO) criterion was developed to handle this concept and was assigned a lesser maximum value of 8. (Not quite as important a criterion as DI but still an important factor in the determination of relative problem category "importance").

What if two problem categories are rated equal after DI and FO determinations? There were two criteria that were developed to be deciding factors in such close cases. If a problem is determined to be safety critical or critical to mission completion, it should contribute to the severity of the problem.

In the case of the UCTS, safety criticality or mission criticality of problems should not be a major consideration in problem severity because it is assumed that those problems which the UCTS is responsible for finding are problems that would have been eventually found (after computer installation but before the actual mission).

For all these problems that would have been found before the actual mission, the question of safety and mission becomes academic, for those problems are assumed to be solved before the mission and then do not exist during the mission.

For this reason, these two criteria were rated low (not severe) compared to DI and FO. Safety criticality (SC) was assigned a

maximum of 4 and mission criticality assigned a maximum of 2; safety being of greater importance than mission, assuming manned flights.

5.3 Problem Weighting

All individual problems within each category were then assigned a value for DI (from 0 to 10), SC (from 0 to 4) and MC (from 0 to 2). From these values an average DI, SC and MC was derived for each problem category.

The problem category weight then became the sum of the category's average DI, average SC, average MC and FO. Where the category FO was the ratio of the number of problems in the category to the maximum number of problems in any category, multiplied by the maximum number of problems in any category, multiplied by the maximum scale rating for FO (8).

The equation used to determine average DI, average SC, average MC and FO are as follows:

Difficulty of Isolation
$$DI_j = \sum_{i=1}^{N_j} \frac{\{DI_{ij} \{(0-10)\}\}}{N_j} \quad (1)$$

Frequency of Occurrence
$$FO_j = \frac{8}{N_{max}} \cdot N_j \quad (2)$$

Safety Critical
$$SC_j \quad \frac{1}{N_j} \cdot \sum_{i=1}^{N_j} \{SC_{ij} \{(0-4)\}\} \quad (3)$$

Mission Critical
$$MC_j = \frac{1}{N_j} \cdot \sum_{i=1}^{N_j} \{MC_{ij} (0-2)\} \quad (4)$$

Where the subscript j indicates the jth category (i.e. EMI), Nj indicates the number of problems in the jth category and N_{max} is the maximum number of problems in a single category. DI_j, FO_j, SC_j and MC_j are the difficulty of isolation, frequency of occurrence safety criticality and mission criticaltiy, respectively of the problem category and DI_{ij}, FO_{ij}, SC_{ij} and MC_{ij} are the ith problem in the jth

category for each parameter. The expression (a-b) represents the phrase " on a scale of a to b."

The results of weighting and summing are shown in Table II. The weighting was a committee effort of hardware digital engineers and the results shown represent a consensus of opinion of those engineering.

5.4 Results of Weighting

Table II indicates that several categories contain critical problem areas (EMI, Power and noise). The total severity of weighting for these three categories ranges from 16.7 to 17.7.

The next most severe problem categories are shown to be design, grounding, memory and software with a range of 13.7 to 14.9.

The least severe problem categories are the I/O, and hardware with weighting of 11.4 and 7 respectively. The results of the problem category weighting have no real meaning until it is used in the test effectiveness analysis.

E. COMPILATION OF SYSTEM TEST AND ANALYSIS

1. Introduction

This section contains system tests used by manufacturers which were surveyed in Section D-3 of this study to uncover system integration problems found after in-plant subsystem acceptance tests had been completed. Also contained herein are various tests which are used to assure that the digital equipment meets design specifications.

2. Background

As pointed out previously, this study concerns itself with test practices of digital equipment manufacturers. Since the Military Standards are well documented, this section of the study concentrates on tests which the surveyed manufacturers have imposed upon themselves which are in addition to or parallel with

those documented in the Military Standards. These tests were necessary to uncover those documented problems and to test specifications unique to each manufacturers digital equipment.

3. Object

The object of this study is to compile a list of system tests and analyze those tests. An optimum set of efficient tests will be generated as a minimum set of tests to be used by the UCTS.

4. Results of Survey

The survey resulted in a comprehensive list of tests which were used by different manufacturers to uncover the documented problems listed in Table I of this report. These tests are listed in Appendix B of this report.

5. Analysis of Data

5.1 Introduction

The first step in the test analysis was to judge the effectiveness of each test in uncovering problems in each problem category. Evaluations were also made in regard to relative test expense. Overall test effectiveness was then evaluated on the basis of test efficiency, problem category weighting, and test cost considerations. An optimized list of tests was then compiled by combining overall test effectiveness with a mathematical technioue designed to compensate for overlapping test coverage (redundancy considerations).

5.2 Weighting Philosophy

As previously stated, the objective is to optimize the test list for UCTS operation. In order to do this, an analysis of test quality was made. It is important that the judgment be made on the lowest feasible level in order to make the judgment as objective as possible.

5.2 <u>Test Weighting</u>

All tests were judged on the same criterion. Each test was assigned an efficincy rating (E) for each of the nine problem categories based on a scale from 0 to 1. A test would be analyzed in each problem area by making judgment as to how well that test could bring about the discovery of computer problems in that category. The more "efficient" (capable) a test was in detecting problems in a particular problem category, the higher (closer to 1) its efficiency rating (E) would be for that category. For example, a test designed specifically for power problem detection would have a high E for the power category but probably would have a low E for the memory category because of its inability to detect a memory failure of the computer.

After assigning an efficiency rating to each test for every problem category (nine ratings per test), each test was given a cost factor (I) based on 0 to 1. A test deemed relatively expensive would have a high I (near 1) while an inexpensive test would have a low I.

5.4 <u>Overall Test Effectiveness</u>

A basis was formulated from which overall test effectiveness could be made. Effectivness variables included, problem weights, cost factors and efficiency ratings of each test for every problem category.

A criterion function was developed to handle these test parameters in a meaningful way.

The criterion function (CF) developed was:

$$CF_i = \frac{\sum_{j=1}^{9} W_j E_{ij}}{1 + I_i} \qquad (5)$$

Where CF_i = Criterion function of Test #i

I_i = Cost factor of Test #i

W_j = Problem weight of problem category #j

E_{ij} = efficiency rating for test #i on problem category #j

This function favorably ranks inexpensive tests which efficiently detect a broad range of problem categories. When tests become more expensive, or less effective in detection of problems, or less effective in their detection of a wide variety of problems; their criterion function (overall test effectiveness) drops accordingly. This particular CF gave appropriate significance of each test parameter to the total evaluation of the test in question.

Cost factors, efficiency ratings, and CF's are tabulated in matrix form for each test (Table III). This matrix also includes the partial products $W_j E_{ij}$ for each test in each problem category.

5.5 Redundancy Considerations

5.5.1 Purpose

Results of Table III indicate that Test #1 (Transient Radiation) is the best overall test that was analyzed. Test #2 has the second largest CF but this should not necessarily mean that Test #2 is the second best overall test.

There were many of the proposed tests which would uncover the same type of problems. Therefore, these tests would overlap their problem solving abilities. To avoid recommending different tests that have redundant problem solving abilities, a technique was developed to decrease intra-test redundancy.

As an exaggerated example, assume that the first test selected (highest CF) detected all noise and power problems (E_{power} = E_{noise} = 1.00) but not other type (all other E's = 0). Also assume that the test with the second largest CF and E_{power} = E_{noise} = 1.00 with all other E's = 0. It is obvious that with the best test implemented, the test with the second highest CF adds nothing to the problem detection ability of the first test. It is necessary for optimization to consider and remove the redundancy between tests already selected and tests still being analyzed.

5.5.2 Redundancy Technique

After the first matrix was completed (Table III) which contains weights for overall test effectivness for each test, Test #1 was selected as the best test. The efficiency ratings of Test #1 were then used as a percentage of problem coverage for each respective problem category.

The efficiency ratings of all remaining tests were then retabulated (to the nearest hundreth) taking problem coverage by previously selected tests into account. New ratings become:

$$E'_{ij} = E_{ij} (1 - E_{j\ Total}) \quad (6)$$

where E'_{ij} = new adjusted efficiency rating for Test #i on problem category #j

E_{ij} = original efficiency rating (from first matrix)

E_{jTotal} = total problem coverage.

This is the sum of the test efficiency ratings of all previously selected tests for problem category j. The test efficiency ratings used are the ones tabulated for the test at the time it was selected.

5.6 Finalized Analysis Procedure

The first matrix was established as previously indicated (see Table III). Test #1 had the highest CF. The efficiency ratings of this test then became the total problem coverage (E_{jTotal}). New efficiency ratings were then used (as in first matrix) to form a second matrix to select the second best test. See Table IV for second matrix.

The highest CF on this matrix was Test #3. The efficiency ratings of Test #3 used in this second matrix (Round #2) were then added to the total problem coverage to form the new total problem coverage to be used in Matrix #3 (Round #3). This was continued until all problem categories had a high rate of being detected.

5.7 Analysis of Results

Table V is a table of results derived from the matrix analysis. Each test number appears with its rank after each round of matrices. The tests were ranked after each matrix (round) completion

according to their CF's. Ranks went from 0 to 36 with 0 rank given to the highest CF (Test #1). After a test was selected, its rank was frozen in subsequent rounds. This enables quick examinations to be made from one round to another to detect test rank shifts due to redundancy compensations.

Notice that between Rounds 1 and 2 there is considerable shifts in rank, especially in the tests with low rank numbers. For example, Test number 8 was ranked 3 after the first round, but dropped to a rank of 6 after the second round.

Generally, in the first few rounds, numberous rank changes took place. This was due to the fact that the first few tests selected caused significant changes in new problem coverage percentage for the succeeding matrix. Table VI shows the problem coverage percentages in each problem area after each round was completed. Notice how drastically these percentages change over the first few rounds while by the 5th or 6th rounds, percentage changes were comparatively minor.

This trend explains why rank changes from the 5th to the 6th rounds were minor; and as a result of these facts, we propose to let the ranks of the 6th round stand as a test order criterion for the tests suggested in this report. This list provides a basis on which an optimum test set can be proposed.

5.8 Results of Redundancy Considerations

After six "rounds" of redundancy matrix manipulation, six tests were selected as the best overall tests to detect the documented problems. The following shows the accumulated test effectiveness

for the problem categories: Design (58%); EMI (91%); Grounding (60%); I/O (66%); Memory (81%); Noise (88%); Power (77%); Software (28%); and Hardware (81%). These test effectiveness ratings express an anticipated percentage of problem discovery in the various problem areas. Thus, after the selection of the best six tests, the problem area of software is still relatively neglected. In order to add significant coverage to this problem area, Test #2 (ranked eighth) must be included. This will increase software coverage about 50%.

This indicates that an optimum set of tests include the tests ranked one to eight. These eight tests provide a maximum (approximately 73% coverage) problem coverage for such a limited number of tests.

F. BASELINE TESTS

1. General

The following set of tests are recommended as a minimum to evaluate the performance of a candidate computer. It is suggested that the following tests be performed to obtain computer performance baseline.

The tests are divided into three sub-classes, each designed to test a particular test article function.

The sub-classes are:

Primitive Diagnostic Tests
Computer Functional Tests
Simulated Space Shuttle Environment Tests

2. Primitive Diagnostic Tests consist of six tests designed to discover that part of the computer hardware which may have failed during evaluation testing:

The Primitive Tests include:

- Memory Test
- I/O Test
- Arithmetic Test
- External Interrupt Test
- Address Modification Test
- Complex Instruction Test

a. <u>Memory Test</u>

The memory test will consist of writing into and reading from memory through the Direct Memory Access (DMA) port. The test will include putting through simple data words at a reasonably slow rate. If the read data differs from the written data, it can be assumed that the memory is not functioning properly.

b. <u>I/O Test</u>

This test involves an I/O transaction through the program controlled input-output port with memory interaction optional. This test is designed to ascertain health of the logic and software involved in I/O transactions.

c. <u>Arithemtic Test</u>

This test will ascertain the health of the arithmetic unit by requiring execution of some elementary arithmetic functions such as add or subtract.

d. <u>External Interrupt Test</u>

This test will ascertain the health of the interrupt logic and software and will be accomplished by sending external interrupts from the UCTS to the Test article.

e. Address Modification

This tests the ability of the software and hardware to modify addresses as specified by the manufacturers literature. This test involves all the hardware previously mentioned plus additional registers and control logic for working storage and control respectively. This will also help ascertain the effectivity of the illegal modification traps.

f. Complex Instructions

Once it has been established from the above tests that the computer can execute individual simple instructions and can modify addresses, then the health of the remainder of the machine can be diagnosed by requiring it to do complex instructions (i.e., floating point divide, etc).

3. Computer functional tests are designed to ascertain the performance of the candidate computer in comparison to the manufacturer's specifications. These tests measure accuracy and execution time of certain tasks listed below:

Computational Ability
Time Class of Instructions
Matrix Manipulation
Logical Ability
I/O Efficiency
I/O - DMA Efficiency
Memory Exerciser
Code Conversion
Math Routines

a. Computational Ability

This test involves high Central Processor Unit (CPU) usage over a relatively long time span (minutes). This

test is designed to test the computational ability of the machine and catch any timing problems that tend to build-up after several minutes of operation.

b. Time Class of Instruction

In order for the computer user to get a working feeling for the speed of his machine, some elementary timing measurements must be taken. The goal of this test is to time a class of instructions such a general register, transfer and bit manipulation. The machine would repeat that instruction several times. Measurements of speed of each instruction would be accomplished by taking the total time for repeated instruction execution and dividing that time by the number of instruction executions. This test should be done with several individual instruction classes.

c. Matrix Manipulation

An evaluation technique which requires high computational ability and many other features such as shift and bit manipulation is contained in a matrix manipulation program. This test will time the matrix program process and measure its accuracy.

d. Logical Ability

This test is designed to ascertain the ability of candidate computer to perform shifting tasks, incrementing, list manipulation and general overhead functions. Time and accuracy of this program execution will be the measurement criteria.

e. I/O Efficiency

A critical parameter from subsystem integration point of view is the through-put of the machine at the program controlled I/O port. This test is designed to evaluate that parameter by presenting information at the I/O port. the data will be presented at a constant frequency and the test article will be programmed to run at maximum I/O frequency. By monitoring the data accepted by the test article, the true maximum I/O rates can be ascertained. Appendix D contains an explanation of this method along with reasons for its use.

f. DMA Efficiency

This test is performed in the same manner as in 3(e) except the computer port now being exercised is the DMA.

g. I/O-DMA Efficiency

This test involves exercising both I/O and DMA ports simultaneously at a changed frequency to ascertain the ability of the computer to handle heavy throu put loads on both ports.

h. Memory Exerciser

This test is designed to detect memory problems such as "bit creep" and memory noise in the mainframe memory whether core or plated wire. The memory is exercised at a high rate with a worse case "noise" pattern for the purposes of uncovering missing or changing bit problems which may occur under worse case noise conditions.

i. <u>Code Convert</u>

NASA expressed a need for conversion of fixed to floating point and back to fixed as part of the Space Shuttle Requirement. This test is designed to measure the performance of each individual computer to perform the conversion task. The test is designed to measure the accuracy and time involved to accomplish the conversion.

j. <u>Math Routines</u>

For computers such as guidance and navigation computers, certain mathematical subroutines must be executed. These include but are not limited to sine, cosine, arctan and square root. This test will require the execution of these functions with speed and accuracy as measurement criterion.

4. <u>Simulated Space Shuttle Environment Tests</u>

This series of tests will be used to ascertain the effectiveness of the candidate machine to handle space shuttle type programs. These tests are listed below:

Round Robin Evaluation
Concurrent Jobs

a. <u>Round Robin</u>

The round robin in the space shuttle vehicle takes advantage of at least two pieces of hardware, the computer and an external data acquisition unit. The data acquisition unit is continually polling all subsystem sensors. When changes larger than a programmed delta occur in the sensor status, the result is stored in a change stack. The change stack contains both the sensor address and change data.

The computer software system takes advantage of the rotating "change" stack with a software pointer, pointing to the location of the hardware pointer. The contents of the hardware pointer specifies the address of the last variable to be written in the stack. This data contained in the stack is then transferred into main memory and properly acted upon.

In simulation, the UCTS computer inputs data into the change stack through the DMA port. The frequency at which the list is updated is increased at controlled increments. The number of words which are fed to the change list are counted by a hardware counter.

The test computer then reads a hardware counter and the data between the location of the hardware pointer through the last address to be written in.

Data is checked, sent back to the candidate computer at a higher rate, being counted by a hardware counter until overload occurs.

If the hardware counter indicates more word transfers than the stack is capable of handling, an overload condition results. This point is then recorded as the saturation point of the round robin program.

This test measures the ability of the candidate computer to handle high data rate changes under simulated space shuttle conditions.

b. Concurrent Jobs

This test involves the round robin evaluation coupled with simultaneous mathematical routine execution, code conversions and I/O, DMA transactions. Data for computer evaluation includes time and accuracy of intermediate results as well as final results.

G. CONCLUSIONS

1. Introduction

The results of the study showed that a set of optimum tests were generated to effectively detect those document system type problems.

In addition, a baseline set of tests are recommended as a minimum to assure functional candidate computer capabilities.

2. Base Line Tests

The following lists the base line tests:

Primitive Diagnostic Tests

Memory
I/O Test
Arithmetic
External Interrupt
Address Modification
Complex Instruction

Computer Functional Tests

Computational Ability
Time Class of Instructions
Matrix Manipulation
Logical Ability
I/O Efficiency
I/O - DMA Efficiency
Memory Exerciser
Code Conversion
Math Routines

Simulated Space Shuttle Tests

Round Robin
Concurrent Jobs

3. Recommended Test Set to Detect documented System Problems:

Test	Test #
Transient Radiation	1
Inadvertant Power Transient	3
Line Impulses	2
Random Interrupt	9
Voltage and Ground Wire Check	6
Electrostatic Discharge Test	8
Power Line Pulses	4
Maximum Interrupt Speed	26

Descriptions of these tests are included in the Test Methods Survey (Appendix B).

4. Survey Method Effectiveness

The survey should not be considered a final word in testing, but should be used as a base for test development.

H. RECOMMENDATIONS

It is recommended that in order to completely test a candidate computer for space shuttle applications, the following procedure be adopted in order to compile sufficient, meaningful data.

1. Recommended Test Procedure.

   a. Implement all tests explained in G-2 of this report. Do these tests in a quiet (noiseless) room temperature atmosphere to obtain computer baseline data.

   b. Repeat 4.1.1 under each of the conditions specified in G-3 of this report. This will give the computer user a complete set of data from which space shuttle operation can be predicted. This will also give the user a detailed analysis of which environmental condition causes difficulty with the computer operation.

TABLE I

SURVEY OF SYSTEM DIFFICULTIES DETECTED AFTER NORMAL ACCEPTANCE

DESIGN		EMI		GROUNDING	
CAUSE	SYMPTOM	CAUSE	SYMPTOM	CAUSE	SYMPTOM
1. Out of spec pulse	System failure	1. Unknown	System lock-up	1. Caseground signal ground isolation (8)	Computational errors during RF testing
2. Marginal components	Computer stoppage	2. Case gnd signal gnd isolation (8)	Computational errors during RF testing	2. Multipoint ground system	Computational errors
3. Timing problem	Computer stoppage	3. Bad memory bits caused by transients (2)	Various system failures	3. Removing ground connector induced signal transients (3) (2)	Bad memory and register data
4. Peripheral on/off caused extraneous pulses stored in buffer. 1	Erroneous initial data	4. Transients due to connector separation (intentional) (3) (2)	Bad memory and register data		
5. Multiple I/O processing deficiency	Jump I/O channel doesn't always execute	6. EMI in power supply	Bad computer bits		
6. Priority interrupt lock-up	Highest priority interrupt hogs computer if no "1" level is achieved				
7. Priority interrupt lock-up (10)	Inadequate burst I/O capability				

TABLE I (continued)

I/O		MEMORY		NOISE	
CAUSE	SYMPTOM	CAUSE	SYMPTOM	CAUSE	SYMPTOM
1. Rapid I/O Transactions	Reduced processor speed	1. Bad bits (2)	Various system failures	1. unterminated signal connector pins (2)	Computational errors
2. Rapid interrupt sequence	Reduced processor speed	2. Low temperature bit creep	Bad memory data	3. Adjacent signal crosstalk	split pulses
3. Peripheral on/off caused extraneous pulses stored in buffers 1	Erroneous initial data	3. Ambient temp. bit creep	Bad memory data	4. Adjacent signal crosstalk	bad data
4. Design failure (10)	Inadequate burst I/O capability	4. Adjacent word disturbance	Bad memory data	5. Excessive Cable length	Bad transmitted data
				6. Signal Transients induced by cable separation (2)	Bad data
				8. Relay Noise	Computer Stoppage

Table 1 (continued)

POWER		SOFTWARE		HARDWARE	
CAUSE	SYMPTOM	CAUSE	SYMPTOM	CAUSE	SYMPTOM
1. Power transient	Clock sync modulation	1. Improper Instruction Sequence (2)	Computer stoppage	1. Bad connector	Various System Failures
2. Bad memory bits due to power up and down (3)	Various system failures	3. Programming errors	Computer Stoppage	2. Bad cables	Computer stoppage
		4. Language selection	Reduced processing speed	Note: Failure to test immediately after power-on ignores numerous faults.	
5. Low prime power	Computer Stoppage	5. Software error	Computer acts on non-legal code		
6. Low prime power	Intermittent failures				
7. EMI in power supply	Bad computer bits				
8. Power interrupt recycle different for different equipment	Bad computer bits				

TABLE II - **PROBLEM CATEGORY WEIGHTING** (based on Difficulty of Isolation, Safety Criticality, Mission Criticality and Frequency of Occurrence)

PB #	DESIGN			EMI			GROUNDING			I/O			MEMORY			NOISE			POWER			SOFTWARE			HARDWARE		
	DI	SC	MC	DI	SC	MC	DI	SC	MC	DI	SC	MC	DI	SC	MC	DI	SC	MC	DI	SC	MC	DI	SC	MC	DI	SC	MC
1	6	2	0	10	2	0	5	2	1	5	2	1	7	4	2	6	2	1	4	1	1	8	2	0	3	2	0
2	9	3	1	8	2	1	6	3	1	5	2	1	6	3	1	6	2	1	6	3	1	8	2	1	3	2	0
3	7	3	1	6	3	1	7	3	1	6	2	.5	6	3	1	8	4	2	6	3	1	4	2	1			
4	6	2	0	7	2	2	7	3	1	3	2	0	6	3	1	8	3	1	6	3	1	5	1	0			
5	3	2	1	7	2	2										3	2	1	3	2	1	7	1.5	0			
6	3	2	1	7	2	0										5	3	1	3	2	1						
7	2.5	1	0													5	3	1	7	3	1						
8																5	3	1	7	2	1						
AVE.	5.2	2.1	.6	7.5	2.2	1	6.25	2.75	1	4.8	2	.6	6.3	3.3	1.3	5.8	2.8	1.1	5.3	2.4	1	6.4	1.7	.4	3	2	0
FO	7			6			4			4			4			8			8			5			2		
WEIGHT	14.9			16.7			14			11.4			14.9			17.7			16.7			13.5			7		

TABLE III - ROUND 1 - TEST PREFERABILITY

NAME	TEST #	PROBLEM WEIGHT (W) / COST FACTOR	DESIGN 14.9		EMI 16.7		GROUNDING 14		I/O 11.4		MEMORY 14.9		NOISE 17.7	
			E	WE	E	WE	E	WE	E	WE	E	WE	E	WE
Transient Radiation	1	1.1	.1	1.49	.7	11.69	.2	2.80	.0	.0	.3	4.47	.6	10.62
EMI-Electrical Field Susceptibility	35	1.3	.1	1.49	.2	3.34	.2	2.80	.2	2.28	.2	2.98	.2	3.54
Mag. Field Radiated Susceptibility	38	1.3	.1	1.49	.2	3.34	.1	1.40	.1	1.14	.1	1.49	.1	1.77
EMI Mag. Field Susceptibility	34	1.2	.1	1.49	.1	1.67	.1	1.40	.1	1.14	.1	1.49	.1	1.77
EMI Audio & RF Susceptibility	37	1.2	.1	1.49	.2	3.34	0	0	.1	1.14	.1	1.49	.2	3.54
Line Impulses	2	1.2	.1	1.49	.4	6.68	.1	1.40	.2	2.28	.3	4.47	.4	7.08
EMI Transient (spike) on power lines	36	1.4	.1	1.49	.1	1.67	0	0	.1	1.14	.1	1.49	.1	1.77
Inadvertant Power Transient	3	1.6	.2	2.98	.1	1.67	.1	1.40	.2	2.28	.2	2.98	.1	1.77
Power Line Pulses	4	1.6	.1	1.49	.2	3.34	.1	1.40	.1	1.14	.2	2.98	.2	3.54
Cable Bundle	5	1.4	0	0	.3	5.01	.1	1.40	.1	1.14	.2	2.98	.3	5.31
Voltage & Ground Wire Check	6	1.1	.1	1.49	.1	1.67	.3	4.20	0	0	.1	1.49	.1	1.77
Oscillator Check	7	1.5	.2	2.98	0	0	0	0	.1	1.14	0	0	0	0
Electrostatic Discharge	8	1.2	.1	1.49	.3	5.01	.1	1.40	.1	1.14	.2	2.98	.3	5.31
Spike on Ground	14	1.2	.1	1.49	.2	3.34	.2	2.80	.1	1.14	.1	1.49	.1	1.77
Random Interrupt	9	1.3	.2	2.98	0	0	0	0	.4	4.56	.3	4.47	0	0
Temp. variation vs Moisture	10	1.0	.2	2.98	0	0	0	0	0	0	0	0	0	0
Overtemperature Response	11	1.2	.1	1.49	0	0	0	0	.1	1.14	.1	1.49	0	0
Three Phase Unbalance	12	1.5	.1	1.49	0	0	0	0	.1	1.14	.1	1.49	0	0
Power Transients & Switch Toggles	13	1.2	.1	1.49	.1	1.67	.1	1.40	.1	1.14	.1	1.49	.1	1.77
Max. Interrupt Speed	26	1.5	.2	2.98	0	0	0	0	.3	3.42	.1	1.49	0	0
EMI-Input/Output Threshold	28	1.7	.1	1.49	.3	5.01	.2	2.80	.2	2.28	0	0	.3	5.31
EMI-Emissions from Computer (time)	29	1.3	.1	1.49	.2	3.34	.1	1.40	0	0	0	0	0	0
EMI-Emissions from Computer (Freq.)	30	1.7	.1	1.49	.2	3.34	.1	1.40	0	0	0	0	0	0
EMI - Static Residual,Resultant Fields	31	1.2	0	0	.2	3.34	.1	1.40	0	0	0	0	.1	1.77
EMI-E Field from Computer	33	1.5	.1	1.49	.2	3.34	.1	1.40	0	0	0	0	.2	3.54
Mag. Field Radiated Emissions	39	1.3	.1	1.49	.1	1.67	0	0	0	0	0	0	.1	1.77
RF Susceptibility on Power Lines	40	1.2	.1	1.49	.1	1.67	0	0	0	0	0	0	.1	1.77
Echo Check	42	1.2	0	0	0	0	0	0	.2	2.73	.6	8.94	0	0
Power Interrupt	43	1.8	0	0	0	0	0	0	0	0	.1	1.49	0	0
Circuit Protect on Test Connectors	44	1.1	.1	1.49	0	0	.1	1.40	0	0	0	0	0	0
Memory Sum Check	45	1.6	0	0	0	0	0	0	.2	2.28	.4	5.96	0	0
Memory Protect Verification	46	1.2	0	0	0	0	0	0	.1	1.14	.1	1.49	0	0
I/O Speed & Buffering	47	1.2	.1	1.49	0	0	0	0	.3	3.42	0	0	0	0
Random Bit word generator	48	1.2	.1	1.49	0	0	0	0	0	0	.1	1.49	0	0

TABLE III - ROUND 1 (continued)

NAME	TEST #	POWER 16.7 E	POWER 16.7 WE	SOFTWARE 13.5 E	SOFTWARE 13.5 WE	HARDWARE 7 E	HARDWARE 7 WE	WE	CF	RANK
Transient Radiation	1	.2	3.34	0	0	0	0	34.41	31.282	1
EMI-Electrical Field Susceptibility	35	0	0	0	0	.1	.70	17.13	13.176	6
Mag. Field Radiated Susceptibility	38	0	0	0	0	0	0	10.63	8.176	17
EMI Mag. Field Susceptibility	34	0	0	0	0	.1	.70	9.66	8.050	18
EMI Audio & RF Susceptibility	37	.2	3.34	0	0	0	0	14.34	11.950	11
Line Impulses	2	.1	1.67	0	0	0	0	25.07	20.892	2
EMI Transient (spike) on power lines	36	.2	3.34	0	0	.1	.70	11.60	8.286	16
Inadvertant Power Transient	3	.6	10.02	.1	1.35	.1	.70	25.15	15.719	4
Power Line Pulses	4	.5	8.35	.1	1.35	.1	.70	24.29	15.182	5
Cable Bundle	5	.1	1.67	0	0	.1	.70	18.21	13.007	8
Voltage & Ground Wire Check	6	.1	1.67	0	0	.3	2.10	14.39	13.082	7
Oscillator Check	7	0	0	0	0	.1	.70	4.82	3.213	34
Electrostatic Discharge	8	.1	1.67	0	0	.1	.70	19.70	16.416	3
Spike on Ground	14	.1	1.67	0	0	.1	.70	14.40	12.000	10
Random Interrupt	9	0	0	.2	2.70	.2	1.40	16.11	12.392	9
Temp. variation vs. Moisture	10	.1	1.67	0	0	.2	1.40	6.05	6.05	24
Overtemperature Response	11	.1	1.67	.1	1.35	.1	.70	7.84	6.533	23
Three Phase Unbalance	12	.1	1.67	0	0	.1	.70	6.49	4.327	28
Power Transients & Switch Toggles	13	.2	3.34	0	0	.1	.70	13.00	10.833	-12
Max. Interrupt Speed	26	0	0	.3	4.05	.2	1.40	13.34	8.893	15
EMI Input/Output Threshold	28	0	0	0	0	.1	.70	17.59	10.347	13
EMI-Emissions from Computer (time)	29	.1	.167	0	0	.1	.70	8.60	6.615	22
EMI-Emissions from Computer (Freq.)	30	.1	1.67	0	0	.1	.70	8.60	5.508	26
EMI - Static Residual, Resultant Fields	31	.1	1.67	0	0	0	0	8.18	6.816	21
EMI-E field from computer	33	0	0	0	0	.1	.70	10.47	6.980	19
Mag. Field Radiated Emissions	39	0	0	0	0	0	0	4.93	3.792	33
RF Susceptibility on Power lines	40	.2	3.34	0	0	0	0	8.27	6.891	20
Echo Check	42	0	0	0	0	0	0	11.22	9.350	14
Power Interrupt	43	.3	5.01	.1	1.35	0	0	7.85	4.361	27
Circuit Protect on Test Connectors	44	0	0	0	0	.2	1.40	4.29	3.900	32
Memory Sum Check	45	0	0	0	0	0	0	8.24	5.150	25
Memory Protect Verification	46	.1	1.67	0	0	.1	.70	5.00	4.167	30
I/O Speed & Buffering	47	0	0	0	0	0	0	4.91	4.092	31
Random bit word generator	48	0	0	.1	1.35	.1	.70	5.03	4.192	29

TABLE IV - ROUND 2 - TEST PREFERABILITY

NAME	TEST #	PROBLEM WEIGHT(W)	DESIGN 14.9		EMI 16.7		GROUNDING 14		I/O 11.4		MEMORY 14.9		NOISE 17.7	
		I COST FACTOR	E	WE	E	WE	E	WE	E	WE	E	WE	E	WE
Transient Radiation			.1		.7		.2		0		.3		.6	
EMI-Electrical Susceptibility	35	1.3	.09	1.34	[illegible]	1.00	.16	2.24	.2	2.28	.14	2.08	.08	1.42
Mag. Field Radiated Susceptibility	38	1.3	.09	1.34	[illegible]	1.00	.08	1.12	.1	1.14	.07	1.04	.04	.71
EMI Mag. Field Susceptibility	34	1.2	.09	1.34	.03	.50	.08	1.12	.1	1.14	.07	1.04	.04	.71
EMI Audio & RF Susceptibility	37	1.2	.09	1.34	.06	1.0	0	0	.1	1.14	.07	1.04	.08	1.42
Line Impulses	2	1.2	.09	1.34	.12	2.0	.08	1.12	.2	2.28	.21	3.12	.16	2.85
EMI Transient (spike) on power lines	36	1.4	.09	1.34	.03	.50	0	0	.1	1.14	.07	1.04	.04	.71
Inadvertant Power Transient	3	1.6	.18	2.68	.03	.50	.08	1.12	.2	2.28	.14	2.08	.04	.71
Power Line Pulses	4	1.6	.09	1.34	.06	1.00	.08	1.12	.1	1.14	.14	2.08	.08	1.42
Cable Bundle	5	1.4	0	0	.09	1.50	.08	1.12	.1	1.14	.14	2.08	.12	2.14
Voltage & Ground Wire Check	6	1.1	.09	1.34	.03	.50	.24	3.36	0	0	.07	1.04	.04	.71
Oscillator Check	7	1.5	.18	2.68	0	0	0	0	.1	1.14	0	0	0	0
Electrostatic Discharge	8	1.2	.09	1.34	.09	1.50	.08	1.12	.1	1.14	.14	2.08	.12	2.14
Spike on Ground	14	1.2	.09	1.34	.06	1.00	.16	2.24	.1	1.14	.07	1.04	.04	.71
Random Interrupt	9	1.3	.18	2.68	0	0	0	0	.4	4.56	.21	3.12	0	0
Temp. variation vs Moisture	10	1.0	.18	2.68	0	0	0	0	0	0	0	0	0	0
Overtemperature Response	11	1.2	.18	2.68	0	0	0	0	.1	1.14	.07	1.04	0	0
Three Phase Unbalance	12	1.5	.09	1.34	0	0	0	0	.1	1.14	.07	1.04	0	0
Power Transients & Switch Toggles	13	1.2	.09	1.34	.03	.50	.08	1.12	.1	1.14	.07	1.04	.04	.71
Max. Interrupt Speed	26	1.5	.18	2.68	0	0	0	0	.3	3.42	.07	1.04	0	0
EMI-Input/Output Threshold	28	1.7	.09	1.34	.09	1.50	.16	2.24	.2	2.28	0	0	.12	2.14
EMI-Emissions from Computer (time)	29	1.3	.09	1.34	.06	1.00	.08	1.12	0	0	0	0	0	0
EMI- Emissions from Computer (Freq)	30	1.7	.09	1.34	.06	1.00	.08	1.12	0	0	0	0	0	0
EMI - Static Residual, Resultant Fields	31	1.2	0	0	.06	1.00	.08	1.12	0	0	0	0	.04	.71
EMI-E Field from Computer	33	1.5	.09	1.34	.06	1.00	.08	1.12	0	0	0	0	.08	1.42
Mag. Field Radiated Emissions	39	1.3	.09	1.34	.03	.50	0	0	0	0	0	0	.04	.71
RF Susceptibility on Power Lines	40	1.2	.09	1.34	.03	.50	0	0	0	0	0	0	.04	.71
Echo Check	42	1.2	0	0	0	0	0	0	.2	2.28	.42	6.26	0	0
Power Interrupt	43	1.8	0	0	0	0	0	0	0	0	.07	1.04	0	0
Circuit Protect on Test Connectors	44	1.1	.09	1.34	0	0	.08	1.12	0	0	0	0	0	0
Memory Sum Check	45	1.6	0	0	0	0	0	0	.2	2.28	.28	4.17	0	0
Memory Protect Verification	46	1.2	0	0	0	0	0	0	.1	1.14	.07	1.04	0	0
I/O Speed & Buffering	47	1.2	.09	1.34	0	0	0	0	.3	3.42	0	0	0	0
Random Bit Word Generater	48	1.2	.09	1.34	0	0	0	0	0	0	.07	1.04	0	0

TABLE IV - ROUND 2 (continued)

NAME	TEST #	POWER 16.7 E	POWER 16.7 WE	SOFTWARE 13.5 E	SOFTWARE 13.5 WE	HARDWARE 7 E	HARDWARE 7 WE	WE	CF	RANK
Transient Radiation	1	.2		0		0	E_{Total}			1
EMI-Electrical Field Susceptibility	35	0	0	0	0	.1	.7	11.06	8.508	8
Mag. Field Radiated Susceptibility	38	0	0	0	0	0	0	6.35	4.885	20
EMI Mag. Field Susceptibility	34	0	0	0	0	.1	.7	6.55	5.458	18
EMI Audio & RF Susceptibility	37	.16	2.68	0	0	0	0	8.62	7.183	12
Line Impulses	2	.08	1.34	0	0	0	0	14.05	11.708	3
EMI Transient (spike) on power lines	36	.16	2.68	0	0	.1	.7	8.11	5.793	17
Inadvertant Power Transient	3	.48	8.07	.1	1.35	.1	.7	19.49	12.181	2
Power Line Pulses	4	.40	6.73	.1	1.35	.1	.7	16.88	10.550	5
Cable Bundle	5	.08	1.34	0	0	.1	.7	10.02	7.157	13
Voltage & Ground Wire Check	6	.08	1.34	0	0	.3	2.1	10.39	9.445	7
Oscillator Check	7	0	0	0	0	.1	.7	4.52	3.013	33
Electrostatic Discharge	8	.08	1.34	0	0	.1	.7	11.36	9.467	6
Spike on Ground	14	.08	1.34	0	0	.1	.7	9.51	7.925	10
Random Interrupt	9	0	0	.2	2.70	.2	1.4	14.46	11.123	4
Temp. Variation vs. Moisture	10	.08	1.34	0	0	.2	1.4	5.42	5.42	19
Overtemperature Response	11	.08	1.34	.1	1.35	.1	.7	8.25	6.875	15
Three Phase Unbalance	12	.08	1.34	0	0	.1	.7	5.56	3.707	26
Power Transients & Switch Toggles	13	.16	2.68	0	0	.1	.7	9.23	7.692	11
Max. Interrupt Speed	26	0	0	.3	4.05	.2	1.4	2.59	8.393	9
EMI Input/Output Threshold	28	0	0	0	0	.1	.7	10.20	6.000	16
EMI-Emissions from Computer (time)	29	.08	1.34	0	0	.1	.7	5.50	4.231	22
EMI-Emissions from Computer (Freq.)	30	.08	1.34	0	0	.1	.7	5.50	3.235	32
EMI-Static Residual, Resultant Fields	31	.08	1.34	0	0	0	0	4.17	3.475	31
EMI-E field from computer	33	0	0	0	0	.1	.7	5.58	3.720	25
Mag. Field Radiated Emissions	39	0	0	0	0	0	0	2.55	1.962	34
RF Susceptibility on Power lines	40	.16	2.68	0	0	0	0	5.23	4.358	21
Echo Check	42	0	0	0	0	0	0	8.54	7.117	14
Power Interrupt	43	.24	4.03	.1	1.35	0	0	6.42	3.567	28
Circuit Protect on Test Connectors	44	0	0	0	0	.2	1.4	3.86	3.509	30
Memory Sum Check	45	0	0	0	0	0	0	6.45	4.031	23
Memory Protect Verification	46	.08	1.34	0	0	.1	.7	4.22	3.517	29
I/O Speed and Buffering	47	0	0	0	0	0	0	4.76	3.967	24
Random bit word generator	48	0	0	.1	1.35	.1	.7	4.43	3.692	27

TABLE V - TEST PREFERABILITY RESULTS AFTER 6 ROUNDS

TEST #	RANK AFTER ROUND #					
	1	2	3	4	5	6
1	*1	1	1	1	1	1
35	6	8	7	9	9	9
38	17	20	18	20	20	19
34	18	18	17	16	16	16
37	11	12	16	17	15	15
2	2	3	*3	3	3	3
36	16	17	19	19	19	20
3	4	*2	2	2	2	2
4	5	5	8	7	6	7
5	8	13	11	13	12	11
6	7	7	5	5	*5	5
7	34	33	32	29	30	30
8	3	6	6	8	7	*6
14	10	10	10	10	10	10
9	9	4	4	*4	4	4
10	24	19	20	18	17	17
11	23	15	15	12	13	13
12	28	26	29	26	28	29
13	12	11	13	11	11	12
26	15	9	9	6	8	8
28	13	16	14	14	14	14
29	22	22	23	23	21	21
30	26	32	30	30	27	28
31	21	31	28	32	26	26
33	19	25	22	25	23	22
39	33	34	34	34	34	34
40	20	21	27	28	25	25
42	14	14	12	15	18	18
43	27	28	33	33	31	31
44	32	30	26	21	22	23
45	25	23	21	27	33	33
46	30	29	31	31	32	32
47	31	24	24	24	29	27
48	29	27	25	22	24	24

* Indicates test selected in a specific round

Indicates test previously selected

TABLE VI

EFFICIENCY RATING ACCUMULATION

AFTER ROUND #	DESIGN	EM	GND	I/O	MEMORY	NOISE	POWER	SOFT.	HARD.
1	.1	.7	.2	0	.3	.6	.2	0	0
2	.28	.73	.28	.2	.44	.64	.68	.1	.1
3	.35	.85	.35	.36	.62	.78	.71	.1	.1
4	.48	.85	.35	.62	.73	.78	.71	.28	.28
5	.53	.87	.55	.62	.76	.80	.74	.28	.50
6	.58	.91	.60	.66	.81	.88	.77	.28	.55

II. UCTS BASELINE SYSTEM DEFINITION

A. INTRODUCTION

The UCTS system philosophy is to develop a machine which is capable of testing aerospace computers which eventually will be integrated into the space shuttle system. Presently the environment and operational characteristics of the space shuttle are not well defined. The candidate aerospace computers are also, in some cases to date, not well defined. The development of the computer tester, then, is dependent upon the accuracy of the interface specification available to GE/AESD during the design phase.

Specifications for such a machine with these constraints calls for a highly flexible, easily operated and low cost GSE machine. See Figure II-1 which is the block diagram of the proposed UCTS.

B. SYSTEM FLEXIBILITY

As a minimum, the tester (UCTS) must have the following flexibility features:

- Programmability
- Modular Software
- Flexible Peripheral Devices

1. Programmability

The UCTS should, as a minimum, be able to perform the functions recommended in the problem test survey report. It is anticipated, however, that when testing actually beings, additions and modifications to the recommended test functions will be required. This, then, requires that changes to the test functions can be made with minimum difficulty and maximum cost efficiency.

A way to make the machine flexible is to make it programmable. Programmability directs one into the area of computers. Since there is a choice of many mini-computers available in today's market at relatively low cost, a mini computer with satisfactory peripheral interface ability is recommended.

One then looks at the programmability of the computer to assess its flexibility in software and hardware.

2. Modular Software

The goal here is to design software modules which are independent entities but can be interfaced one to another. If changes are needed from the basic program philosophy, the user then does not have to rewrite the total operational program, but rather, just make modification to those affected modules. Modular software is software which is partitioned in such a manner that maximum changes cause minimum cost. The baseline UCTS software modules are shown in Figure II-2.

2.1 Interface Language

This is the language that is needed to interface the user to the machine and the machine back to the user. This language is necessary so that ease of machine operation can be maintained and operator errors can be minimized.

2.2 Up Link

This software module is designed to transmit commands and data from the UCTS computer to the test article and the test article interface.

2.3 Down Link

This software module is designed to receive information from the test article and test article interface.

2.4 I/O Routine

This software module communicates between the up link, down link and peripherals for the purposes of inputting and outputting data to peripheral devices.

2.5 Error Processor for UUT (Unit Under Test)

The error processor communicates to the UCTS user that there are operational problems in the UUT. (test article).

2.6 Fault Processor for UCTS

This module processes and isolates faults which may occur in the tester system.

2.7 Self Test

This module contains test and diagnostic programs which are used to test the health of the tester electronics and diagnose any failures.

3. Flexible Interface Devices

Flexible interface devices shall be chosen such that major changes in test procedure or test philosophy can be handled with a minimum of hardware modifications. Such devices include keyboard, card reader, or magnetic tape inputs and printer or hard copy output as a minimum. Devices such as operator's panel input (code in binary) paper tape etc., have serious flexibility limitations as input devices. Output devices such as binary lights, nixie tubes or CRT also exhibit limitations because, for instance, they allow no permanent record and in the case of binary light are difficult to interpret.

C. EASE OF OPERATION

1. General

In order for the UCTS to be useful as a test vehicle, the user must be able to grasp its operation and interface to it with minimum of training. Once trained, the user should be able to use his tools effectively without difficulty or constant retraining. This then necessitates a requirement for a man-machine language which is easily usable and does not need constant debug. This also means that the hardware with which the operator interfaces also is easily used.

As a minimum, the machine shall contain the following features to be easily operated:

- Man-Machine Interface
- Input Device
- Output Device
- Well Defined Test Article Interface

a. Man-Machine Interface

This item was discussed in Section B, Item 2.1.

b. Input Devices

This covers the area of both man-machine interface and the data input interface.

For ease of operation, at a minimum, the input device should be a keyboard accompanied by the associate software conversion (described in Section B, Item 2.1). Other items which would help in overall functionalmodifications would be a card reader. This device allows the operator to modify his test program very easily by modifying only those affected cards.

In the area of data and program storage, a preliminary estimate of total necessary memory is 8K. Most mini-computers are equipped with at least 8K of mainframe memory and some with expansion capability.

If, as more detailed definition of test functions become available it is found that additional memory is necessary, expansion of the mainframe as well as disc or magnetic tape should be considered.

c. Output Device

The output devices could consist of a multitude of devices from binary readout lights to line printers. Obviously the binary lights are the most cost effective approach in terms of hardware cost. From the standpoint of user ease and errorless permanent record-keeping, however, the printer is the best choice and is recommended herein. Another device which makes the machine easily used is a CRT display. This device is not necessary for ease of operation but would help in troubleshooting and test modifications.

d. Clean Test Article Interfaces

Probably the area in which trouble occurs most frequently when a tester such as UCTS is being specified, is the area of test article interface. This area should be carefully considered as the tester is being designed. Since the UCTS is to test at least four 32 bit aerospace computers, four separate interfaces should be built, one for each test article. These interfaces shall be so well defined that there would be no requirements for modifications necessary to interface any of the four test articles.

D. GSE MINIMUM REQUIREMENTS

To maintain a cost effective design, a search for operating, in-place equipment must be made. Once the equipment is located, a study into the requirements necessary to modify that equipment for computer testing must be made. Considerations as to availability, ease of use, flexibility should also be made.

The search for GSE equipment then centers around the following:

Low cost with flexibility and operational ease.

1. Low Cost

The general specifications outlined in the flexibility and ease of operation area are expensive unless the equipment is in place and operational. Modification of the existing equipment is quite cost effective if the changes are minor and a good understanding of the equipment is made at the outset.

In order to keep low cost, therefore, there are two choices (1) compromise on the previous specific actions and live with less than stated minimums or (2) use existing hardware that closely matches those stated specifications. Both alternatives should be explored.

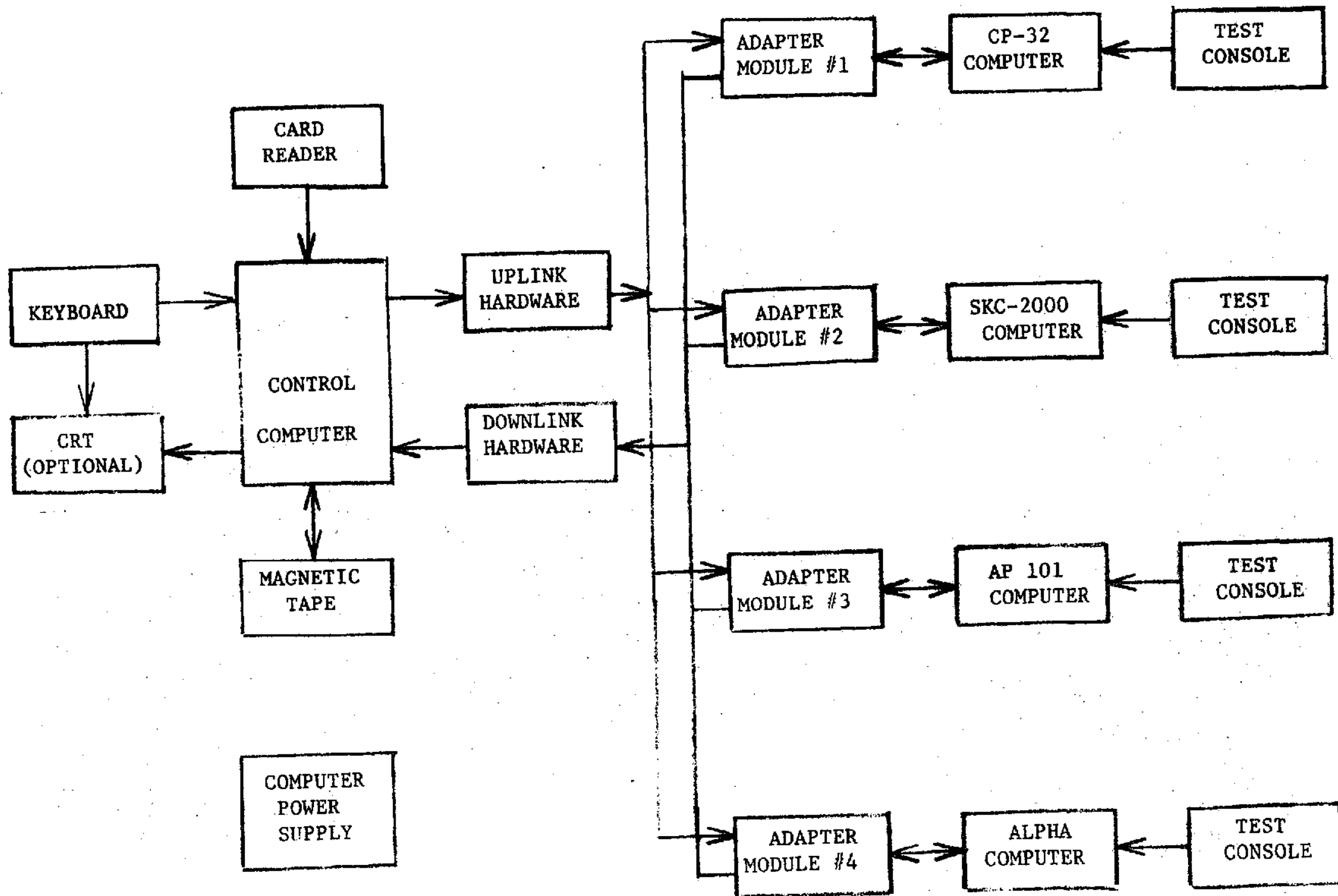
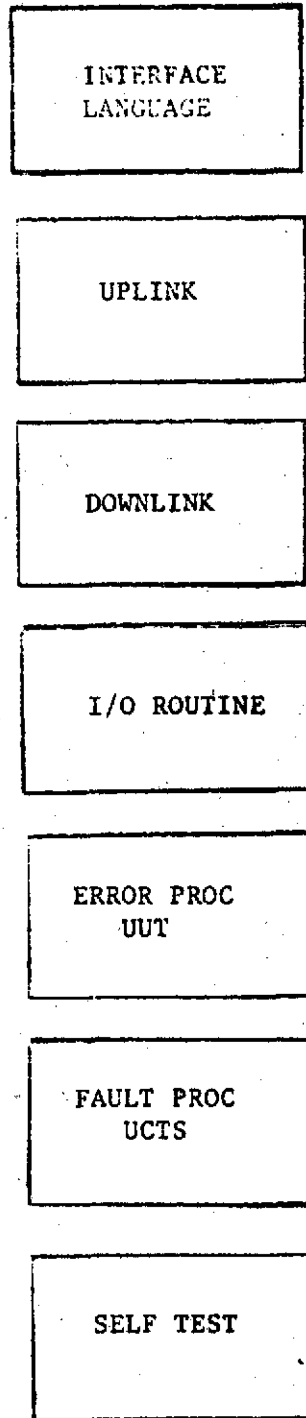


FIGURE II-1. UCTS SYSTEM BLOCK DIAGRAM



SOFTWARE MODULES FOR UCTS MINI COMPUTER

FIGURE II-2

III. SYSTEM TRADEOFF

A survey of GSE which would be available at NASA-MSC to be used for UCTS includes the following:

NOVA Model 1200
DDP-516
PDP-11
4PI-EP
UTE

A. NOVA 1200

The NOVA 1200 is a mini-computer made by Data General, several of which are available at NASA.

The use of the NOVA as a candidate for the UCTS computer deserves the following considerations:

1. Advantages

1.1 Low cost since it is available at NASA - MSC.

1.2 Programmable

2. Disadvantages

2.1 No modular test software written.

2.2 All interfaces to the test article including interface control must be designed.

2.3 No man-machine interface software written.

2.4 Limited input device capability, teletypewriter only.

2.5 Limited output devices, interfaced to a teletypewriter only.

2.6 The machine is unfamiliar to both NASA and GE personnel, which means extra expense would be incurred to learn the machine.

3. Recommendations

Because of the overwhelming diadvantages of the use of the NOVA processor in UCTS, the NOVA was mutually rejected by both GE-AESD and NASA-MSC during the 9/20 to 9/22/72 visit.

B. DDP-516

The DDP-516 is a mini-computer made by Honeywell, one of which is available at NASA-MSC. The use of the DDP-516 as a candidate processor for the UCTS computer deserves the following considerations:

1. Advantages

   1.1 Low cost since it is available at NASA-MSC.

   1.2 Machine familiarity with the personnel at GE-AESD.

   1.3 Programmable

2. Disadvantages

   2.1 No modular software written for testing computers.

   2.2 All interfaces to the test article including interface control must be designed.

   2.3 No man machine interface software written.

   2.4 No available peripherals interfaced to computer.

   2.5 There is only one machine and the availability is in question.

3. Recommendation

   Because of the overwhelming disadvantages, the use of the DDP-516 has been rejected as a possible candidate for use in UCTS.

C. PDP-11

The PDP-11 is a computer made by Digital Equipment Corporation and will be supplied with the SKC 2000 Singer Kearfott Aerospace Computer and be used as a peripheral interface. Careful consideration then must be given for the use of the PDP-11 in the UCTS baseline system.

1. Advantages

   1.1 Programmable

1.2 Interface to peripherals both input and output devices is designed and built. Software is also written to control the device.

1.3 Interface to one of the candidate computers, namely the SKC-2000 is complete and working.

2. Disadvantages

2.1 No modular test software has been written including man-machine interface language which limits flexibility

2.2 Questionable availability of the PDP-11 for use in the UCTS in the time period of interest (from January to June 1973).

3. Recommendations

The PDP-11 was rejected as a candidate computer to be used in UCTS because of lack of resident test software and questionable availability.

This hardware could, however, be used as a back-up if an emergency causes reselection. However, this would significantly increase software costs.

D. 4PI-EP

This computer made by IBM is presently working in a test setup at NASA-MSC. It has limited peripherals, written test software and is well known to NASA and GE personnel. The following careful considerations were made on the 4PI-EP as a possible candidate for UCTS.

1. Advantages

1.1 Programmable.

1.2 The 4PI-EP has modular test software written, but must be modified in order to be usable for UCTS.

1.3 There is some interface control logic built and working for the present test configuration, different however than the UCTS configuration.

1.4 There is a limited set of man-machine software written but must be modified for the UCTS applications.

1.5 The input and output peripheral devices, including controllers, are sufficient for the UCTS project.

2. Disadvantages

2.1 The availability of the 4PI-EP is in question for the time period of interest (January to June 1973).

2.2 Even thought the 4PI-EP has much software written and is very familiar to NASA and GE, it was felt that the machine, in general, was difficult to use and was generally unreliable. Past history has proven that this machine and its peripherals require more than average maintanence.

3. Recommendations

The 4PI-EP was rejected as a possible candidate for use in UCTS because of the question of availability and the past unreliable operational performance record.

E. UTE (Unified Test Equipment)

This equipment is more than a computer and peripheral, it is a working hardware-software test system designed to check aerospace Line Replaceable Units (LRU's). The UTE is designed with modular software and hardware with flexibility and ease of operation as prime considerations. The UTE system deserves the following considerations:

1. Advantages

1.1 The UTE has modular software written, most of which is working. The modules consist of an executive software module called Basic Operating System Software (BOSS).

Within this executive supervisor there are the following sub-modules:

Interface - including up link and down link
System Control
Operators Interface (Interface Language)
Display

1.2 Programmability

The UTE has a META 4 computer in which BOSS resides which is obviously programmable. In addition, both the commands to the test article and the responses from the test article are routed through programmable peripheral processors.

1.3 Interface Modules

The UTE contains the following interface modules:

Two keyboard-CRT consoles
Two magnetic Tape Transports
One disc storage
Line Printer
Distribution Multiplexer

1.4 Man-Machine Software

Man-machine software is part of the BOSS executive program which interprets the keyboard inputs. An assembler is also available.

1.5 Input Devices

The input devices for each of operation include two keyboard CRT consoles. One for control display and the other for data display.

In addition, discs and magnetic tapes are supplied for data base input or storage and program storage.

1.6 Output Devices

The UTE has the capability for interfacing to a line printer or CRT image copier. The UTE also has software necessary to properly format output information so that interpretation is made with ease.

1.7 Test Article Interface

The test article will be interfaced through a Acquisition Command Module (ACM). As a baseline, the interface will be through the 32 bit parallel bus lines of the command formatter sequencer and response formatter which are contained within the ACM. It is assumed that a minimum amount of interface electronics will be necessary to connect the test articles to UTE.

1.8 Low Cost

If UTE were selected as the system for testing computers under the UCTS project, total cost can be held to a minimum. Since all basic test and peripheral interface software is in place, only modifications thereof are necessary to specifically test computers. The hardware, including peripheral controllers and programmable test article interfaces are in place.

Additions to the hardware for testing computers include individual computer interfaces, power supply for the computers and air cooling equipment. This then decreases the need for major design effort of new test hardware and necessary software which decreases overall cost.

Cost efficiency can then be gained by using the UTE system as the major portion of the computer test project.

1.9 The machine is very familiar to GE as well as NASA personnel and documentation is excellent.

2. Disadvantages

The UTE schedule for testing other LRU's may interfere with the computer test effort. A mutual GE/NASA agreement was made that NASA would build a schedule such that the UTE could be used for both computer testing and other LRU testing.

3. Recommendations

Because of the overwhelming advantages of UTE and its close correlation to the system goals, the selection of UTE as baseline hardware to be used for UCTS is recommended. If problems arise, the PDP-11 system shall be used in a back-up situation.

IV. SYSTEM DESCRIPTION

A. INTROUDCTION

The use of Unified Test Equipment (UTE) as the prime hardware for the UCTS project involves hardware and software additions. This section describes the tester system, emphasizing areas in which hardware, software modifications and/or additions are required.

1.0 HARDWARE APPROACH

The UTE hardware system is shown in Figure IV-1. As shown, this system is modular which makes additions and modifications relatively easy. It has been determined that the best place to interface to the UTE for the purposes of testing computers is at The Acquisition Command Module (ACM); specifically, at the output of the Data/Command Distributor (DCD) and the input to the Input Data Multiplexer Router (IDMR) as shown in Figure IV-2. At this location, adapter modules are interfaced to the UTE in the current CTTB configuration for the purposes of interfacing to serial data buses.

According to the UTE documentation, there are provisions made to attach up to eight adapter modules in the current configuration. There are currently two adapter module channels committed, which leaves six for other test functions. Appendix E contains a brief description of the UTE hardware.

Therefore, GE/AESD proposes to design and build new Computer Adapter Modules (CAM), for the purposes of computer test. A CAM will be necessary for each different airborne computer that is scheduled for test.

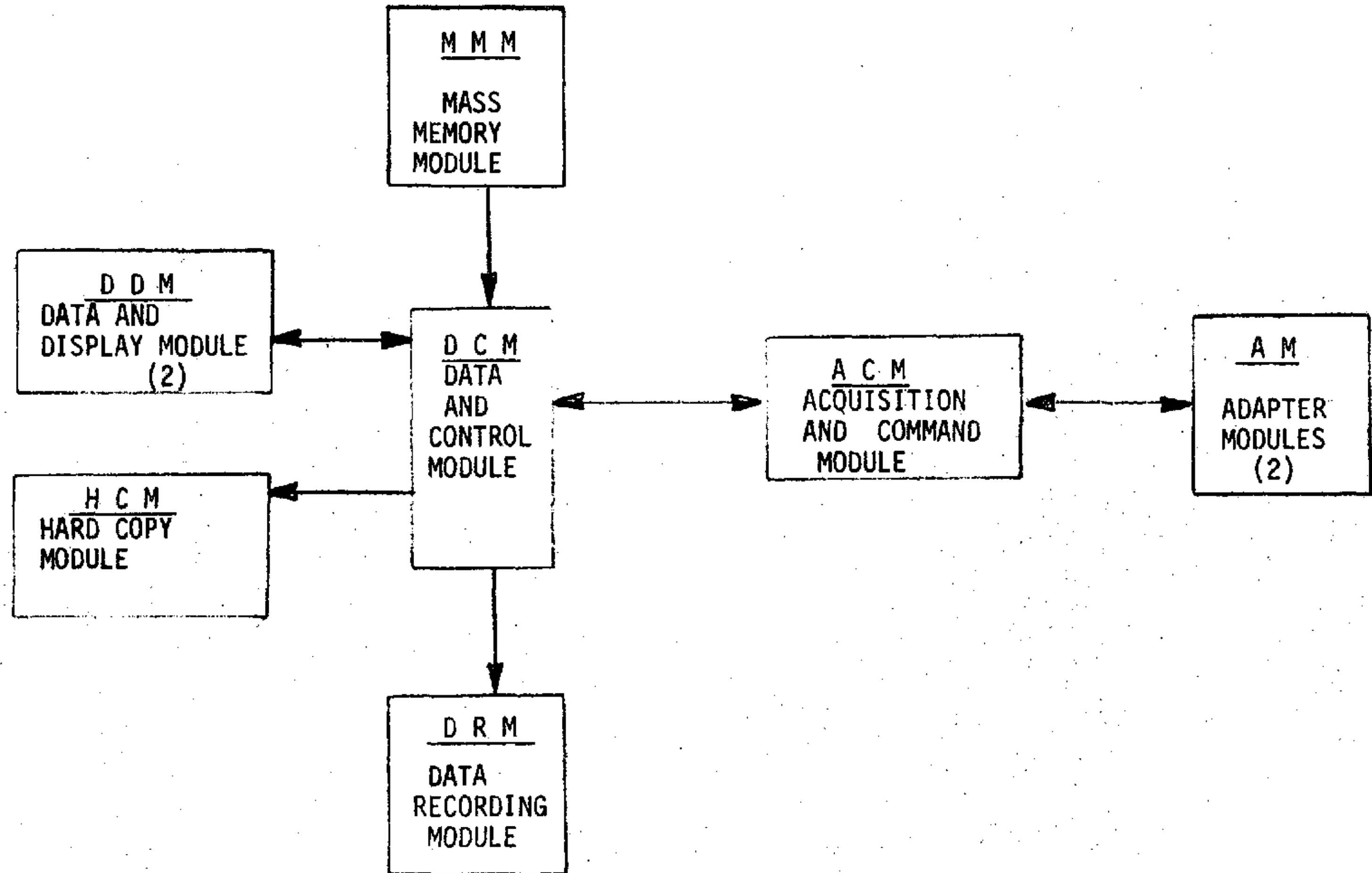


FIGURE IV-1. UTE IN CTTB CONFIGURATION

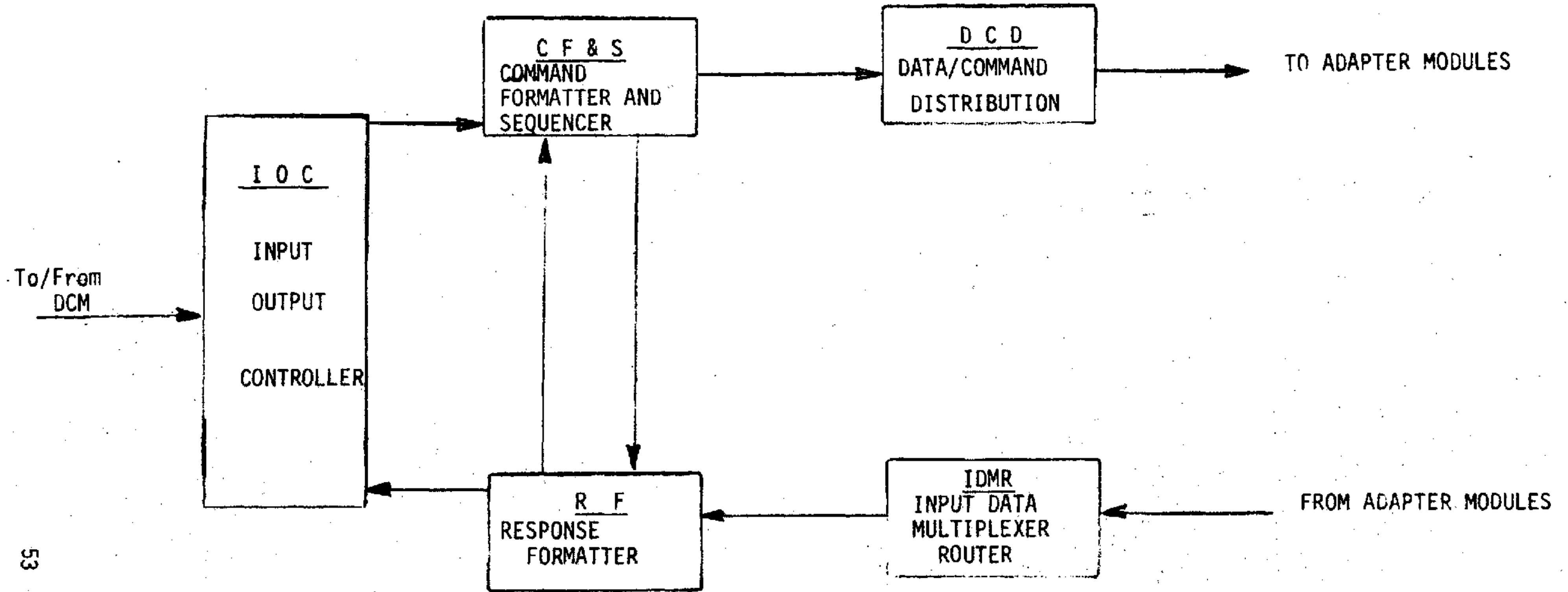


FIGURE IV-2. ACM BLOCK DIAGRAM

BASIC OPERATING SYSTEM SUPERVISOR (BOSS)

THE BOSS ENCOMPASSES ALL SOFTWARE NECESSARY FOR HARDWARE INTERFACE, SYSTEM CONTROL, OPERATOR INTERFACE, DISPLAY PROCESSING, JOB CONTROL AND FILE MANAGEMENT

ACM

ACM INCLUDES ALL SOFTWARE REQUIRED FOR THE UTILIZATION OF THE RESPONSE FORMATTER (RF) AND THE COMMAND FORMAT AND SEQUENCER (CF&S)

TEST OPERATOR SYSTEM (TOS)

TOS INCLUDES ALL SOFTWARE REQUIRED FOR THE IMPLEMENTATION OF AN INTERPRETATIVE TEST LANGUAGE (ITL) CAPABILITY WHEN APPLIED TO A REAL TIME OPERATING SYSTEM.

SELF EVALUATION SYSTEM (SES)

SES INCLUDES ALL SOFTWARE REQUIRED FOR A SYSTEM ORIENTED CHECK OF HARDWARE DEVICE OPERATIONAL STATUS

FIGURE IV-3. UTE SOFTWARE MODULES

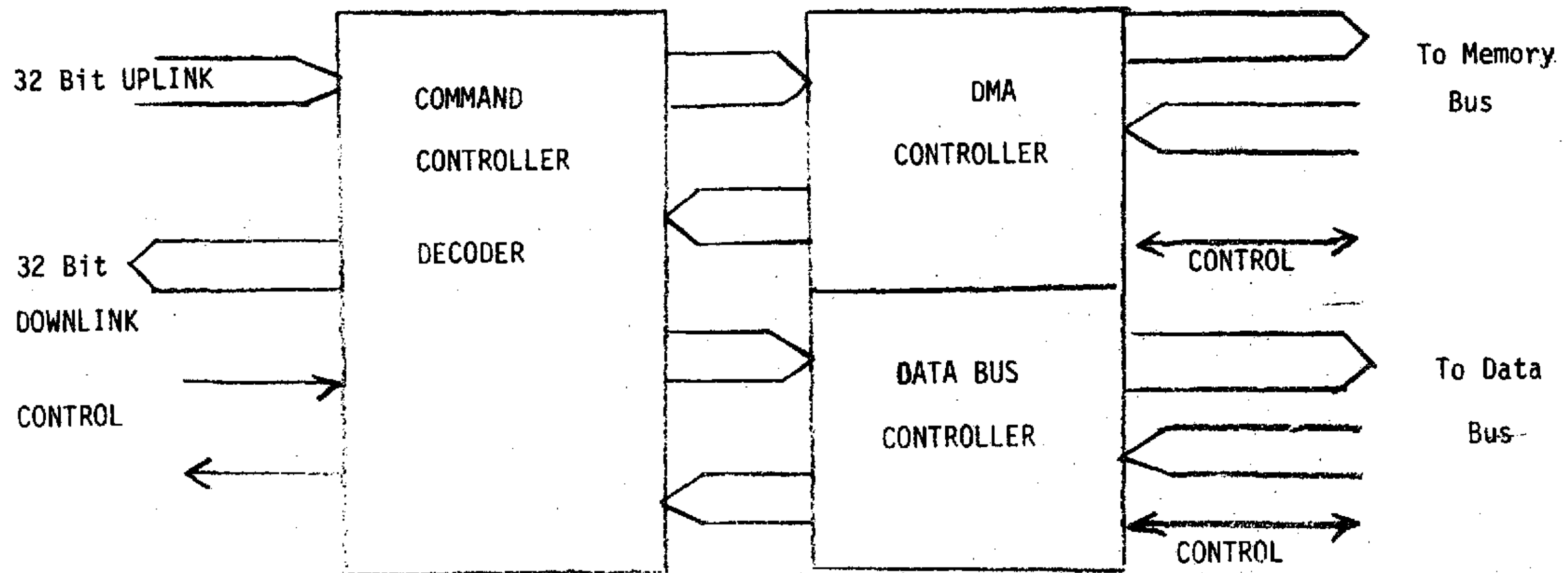


FIGURE IV-4. COMPUTER ADAPTER MODULE BLOCK DIAGRAM

1.1 Software Approach

Figure IV-3 shows the software modules currently implemented in the DCM and ACM modules. The computer test function requires additional test programs to be generated.

The possible areas of software which may be affected include ACM and TOS and SES, each of which must be added to and/or modified for the purposes of computer testing. Appendix F contains a brief description of the present UTE software.

B. HARDWARE DESCRIPTION

1.0 COMPUTER ADAPTER MODULE (CAM)

The CAM is illustrated in Figure IV-4. The CAM will consist of a Command Controller Decoder (CCD), a Direct Memory Access Controller (DMAC) and a Data Bus Controller (DBC).

The CAM is designed to properly control the signal interfaces shown in Figure IV-5. (GE - GEMIC - CP-32 interface is shown).

1.1 Command Controller Decoder (CCD)

The function of the CCD is to interface the ACM to the DMAC and DBC. The CCD accepts commands and data from the Data/Command Distributor (DCD) and properly routes them to the DMAC or DBC. In addition, the CCD receives commands and data from the DMAC or DBC. In addition, the CCD receives commands and data from the DMAC or DBC and properly routes them to the IDMR or I/O controller.

The CCD also keeps track of the direction of data flow, the type of data that is flowing and processes fault and error signals.

Figure IV-6 is a block diagram of the CCD.

FIGURE IV-5.

CP-32 ADAPTER MODULE

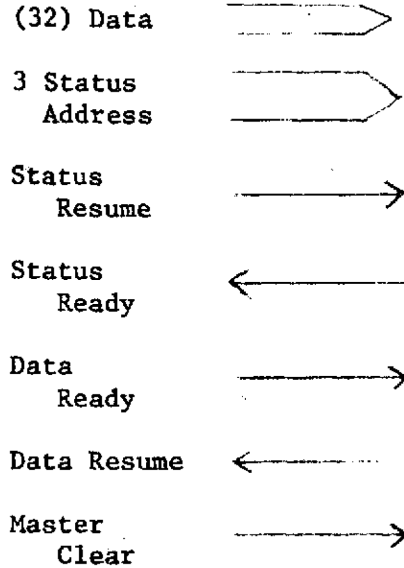
(GE-GEMIC 1)
(CP-32)

SIGNAL INTERFACES

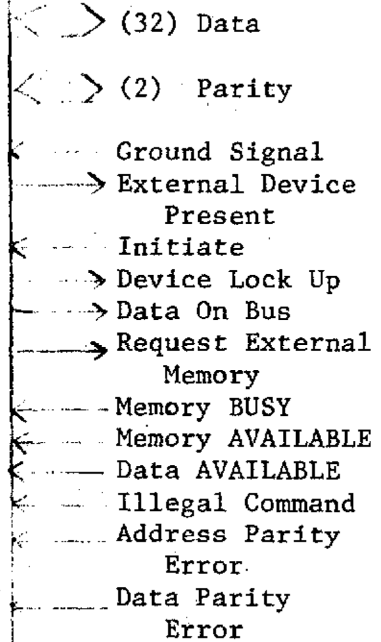
TESTER INTERFACE

TEST ARTICLE INTERFACE

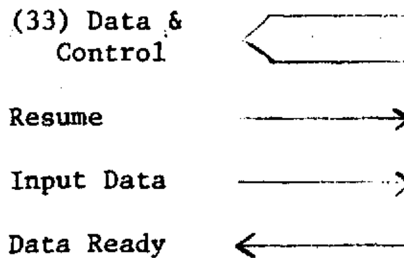
COMMAND DISTRIBUTOR PORT



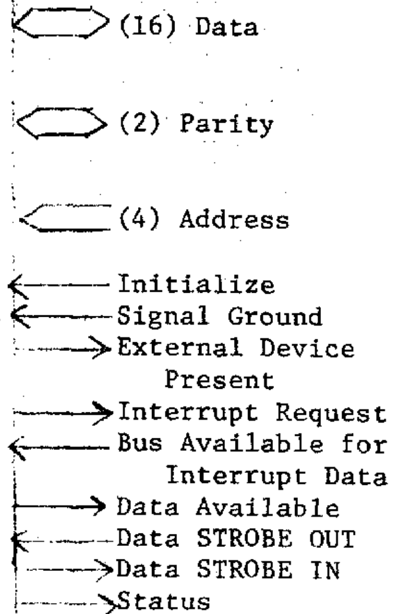
DMA PORT



INPUT DATA MULTIPLEXER ROUTER PORT



PUT TAKE PORT



1.1.1 CCD Features

- Appropriate "Handshaking" with ACM
- Data Routing
- ACM Interrupt Capability
- CAM Timing
- IDMR Formatting

1.1.2 System Concept

The CCD shown in Figure IV-6 is the hardware controlling function which assures that the proper test equipment/test article communication is maintained.

The CCD is able to recognize codes from the ACM to route test data and commands to either the DMAC or the DMC.

The CCD is able to recognize codes from the ACM to route test data and commands to either the DMAC or the DMC.

The CCD then is able (after recognizing the proper ACM code) to set up the modes in the DMAC or DBC for implementing the various test article functions.

The CCD will set up switching necessary to read from the various timers, comparators and fault indicators in the CAM and notify the ACM through interrupt capability of test article errors.

The data returning from the test article is routed by the CCD to the IDMR and proper ACM control is maintained. The data to the IDMR requires specific formatting which is done by special CCD hardware.

1.1.3 CCD Hardware Details

1.1.3.1 ACM Control

This module accepts and generates all signals necessary to accomplish data transfer across the ACM to/from CAM interface.

Inputted ACM control signals are interpreted and transferred to the CONTROL FORMATTER for the purposes of properly routing data and control to the DMAC or DBC.

Control signals are generated from the ACM CONTROL for the purposes of inputting data and test article status.

1.1.3.2 Control Formatter

This module takes command controls from DBC, DMAC or "ACM CONTROL" modules and transforms them into the control format recognizable to the device intended to receive that control (i.e., DBC or DMAC).

1.1.3.3 Word Formatter

This logic takes 32 bit ACM words, 29 of which can be used for data and formats them into a 32 bit data word necessary for DBC or DMAC. It also takes 32 bit data words from DBC or DMAC and puts the word into the necessary format for IDMR with proper control bits added. The control for this module comes from the "CONTROL FORMATTER".

1.1.3.4 DMAC Control

Control is transferred to this block of logic when DMA testing is in progress. This block controls all functions necessary to accomplish the various types of DMA.

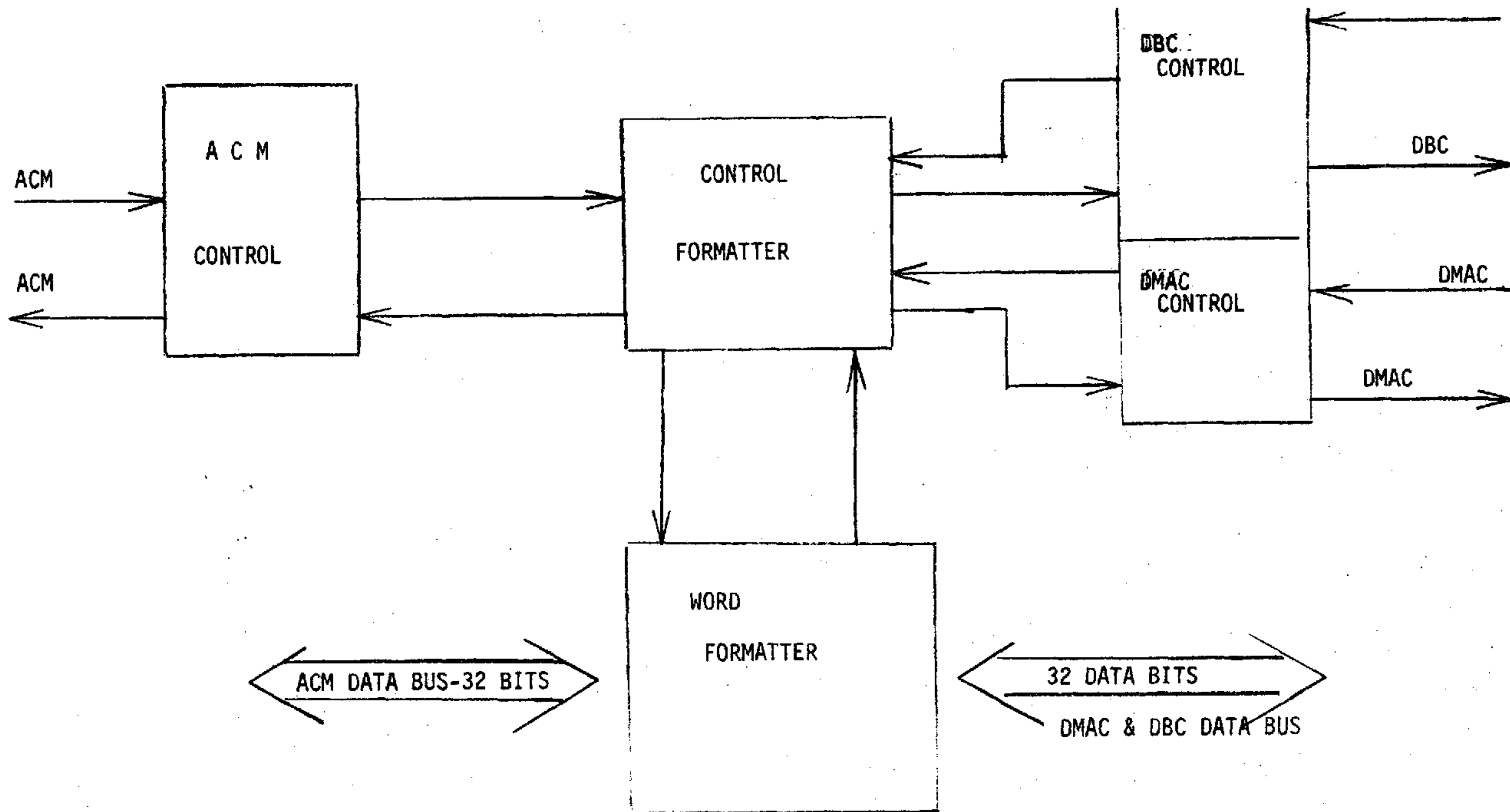
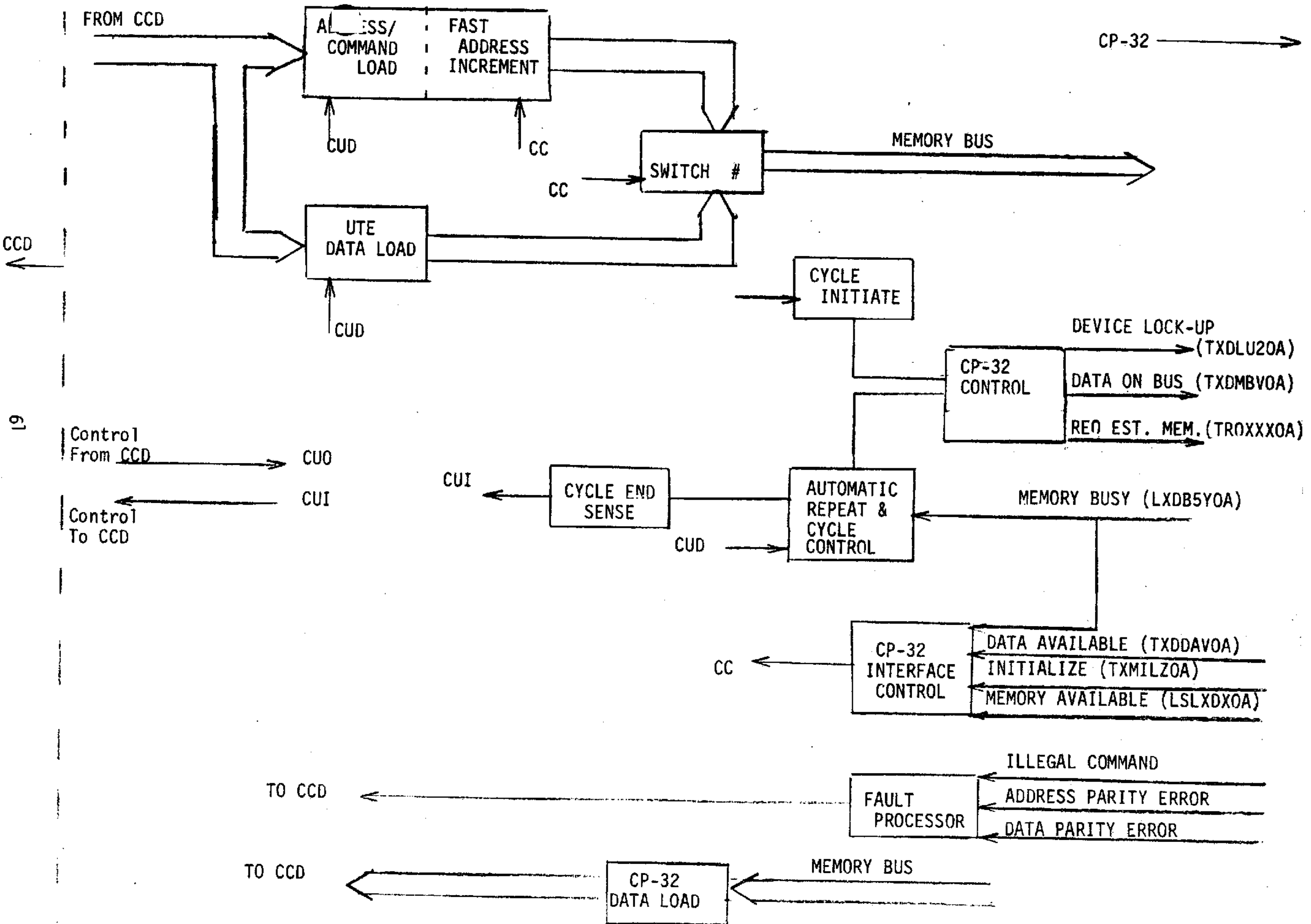


FIGURE IV-6. CCD BLOCK DIAGRAM



DIRECT MEMORY ACCESS CONTROLLER FOR GE GEMIC CP-32 - FIGURE IV-7.

1.2 Direct Memory Access Controller (DMAC)

The DMAC is custom designed logic to externally control the test articles mainframe memory, and also to interface with the CCD. Each test article requires a custom designed DMAC.

Figure IV-7 is a block diagram of a DMA controller which is being designed as part of CAM for GE GEMIC I CP-32 Computer.

1.2.1 DMAC Features

The DMAC has the following features:

. Write into memory (any address)
. Read from memory (any address)
. Increase the rate at which data is presented
. Check and generate parity
. Check for illegal commands
. Load rotating list (for Round Robin)
. Increment address
. Word Count
. Required test article "handshaking" control circuitry

1.2.2 System Concept

The DMAC, briefly, is necessary logic to provide proper communication between the CCD and the test article's memory bus. The DMAC contains only minimum hardware necessary to do the communication function with minimum data processing capability.

Because ACM speeds are slower than the test article's speeds, speed-up logic is necessary as part of DMAC so that data and addresses are available at the test article interface when necessary. The speed-up circuitry is designed independent of the ACM speed but is directly controlled by the test article interface through the "CP-32 COMMAND MODULE", "AUTO, REPEAT &

CYCLE CONTROL," "ADDRESS/COMMAND LOAD" register and "FAST ADDRESS INCREMENT."

The DMAC properly activates the test article's memory with address and commands to the memory bus, through the "UTE DATA LOAD" registers or the "ADDRESS COMMAND LOAD", FAST ADDRESS INCREMENT" module. The data is then read back through the "CP-32 DATA LOAD" register. Proper data processing including comparison is done in the ACM.

All control signals from CCD and the test article are generated and received in the remaining modules in Figure IV-7.

The following discussion presents details of each module considered in Figure IV-7.

1.2.3 DMAC Hardware Details

1.2.3.1 Address/Command Load

A register that loads and stores CP-32 DMA address and command bits. Parity is also generated for the 32 bit word.

1.2.3.2 Fast Address Increment

This section of the Address/Command load is used when the test article DMA is run at its highest capable speed. It provides new consecutive DMA addresses at a rate equal to the test article's DMA speed. This is done by incrementing an address register after each DMA cycle.

1.2.3.3 UTE Data Load

A register that loads and stores the test article's DMA input data. Parity is also generated for the 32 bit word in this module.

Hardware is present to insure data will not be read from the register by the test article when new data is being strobed into that register from the CCD.

1.2.3.4 Switch Z

Switch Z determines 32 bit flow to test article from either an address/command register or the data register. Switch Z is under CP-32 interface control.

1.2.3.5 CP-32 Control

This control module sends the necessary levels required for DMA transactions to the test article. The input to this control is sent from two sources "CYCLE INITIATE" and "AUTOMATIC REPEAT & CYCLE CONTROL".

The hardware in this module contains necessary one-shots, registers, latches and level sensors necessary to accomplish the above tasks.

1.2.3.6 Cycle Initiate

This module sends a pulse requesting a DMA cycle. This circuitry is CCD interface control fed.

1.2.3.7 Automatic Repeat & Cycle Control

This module generates the necessary test article "handshaking" pulses and levels needed for a complete DMA cycle. This block also contains a counter that can be used to call for repeated DMA cycles up to 1000 test article cycles.

1.2.3.8 Cycle End Sense

This module detects the end of a series of DMA cycles caused by the high speed repeat. This sense is triggered when the counter in the "AUTOMATIC REPEAT" module times out. This cycle end sense notifies the CCD of the end of this event.

1.2.3.9 Fault Processor

The logic herein detects unexpected test article fault levels (illegal command, parity error) and transmits this information to the CCD.

If a fault is expected (intentionally send bad parity) the fault processor will acknowledge this expected response by not sending any fault notification to the CCD when the test article indicates this parity fault.

1.2.3.10 CP-32 Data Load

This register loads and stores data sent from CP-32. Data is sent to the CCD upon request. This block is controlled by the "CP-32 INTERFACE CONTROL" module.

1.3 Data Bus Controller (DBC)

This block of circuitry is intended to interface the CCD with the program controlled input-output port of the test article. This port accesses the CPU of the test article.

The port on the GE-GEMIC-1 CP-32 which is interfaced is called the PUT/TAKE port which consists of a bi-directional party line type 16 bit bus. All proper "handshaking", bus direction, interrupts, channel address commands and controls must be activated and tested by the DBC. The DBC is shown in Figure IV-8.

1.3.1 Features

The features of the DBC include the following:

- Supply data to test article
- Take data from test article
- Generate and check parity
- Interrupt at variable speed while program is running
- Word comparison
- Word Count

Fig.IV-8 is a block diagram of the DBC which is currently being designed for the GE-GEMIC 1 - CP-32 Aerospace Computer.

1.3.2 System Concept

The DBC is designed to operate in three modes for the purposes of testing different test article functions. These modes are:

- Data Input and Output
- Interrupt
- Polled

1.3.2.1 Data Input and Output Mode

In this mode data, addressing commands and controls are transferred across the test article interface at relatively slow rates. This is done to test the accuracy of the I/O and make sure all functions are operating normally. The transfer can be initiated either by the tester or the test article. Implementation of the transfer can be initiated from the ACM interrupt or test article polling.

1.3.2.2 Interrupt

To observe the reaction of the test article while doing a resident program to external interrupts, special hardware is included in the DBC.

The hardware has the capability of changing the rate of interrupts so that program interrupt I/O efficiency of the test article can be observed.

The approach here is to run a resident program in the

test article, interrupt the CPU at various rates to do trivial I/O tasks. When the I/O transaction becomes inaccurate as seen by the "COMPARATOR" or when the resident program shows deterioration (accuracy or time), the test article will be termed "saturated".

1.3.2.3 Polled Mode

The polled mode allows the test article to input data and store it at its maximum rate. During this test mode the maximum speed at which test article I/O transactions can be made is measured. This test mode is similar to the method used in the DMAC controller when measuring maximum memory speed.

1.3.3 DBC Hardware Details

1.3.3.1 Load Data or Increment Address

This module loads either a data word or the interrupt and address words onto the 16 bit data (PUT/TAKE) bus. A bit set determines which word type has been sent by the CCD. Control, including data word content, is under ACM control.

1.3.3.2 Fast Interrupt of Address

This logic is used when the I/O port is operated at high speed. It provides new interrupt register words at a rate equal to the test article of a CP-32 interrupt I/O cycle. This is done by incrementing an interrupt register after each interrupt cycle.

1.3.3.3 Fast Data

This module is used when maximum I/O transactions exist when the CPU is being interrupted. It is initially loaded by the ACM and is reloaded following each interrupt I/O cycle with the data from"CP-32 Data" module. Control for this section comes from both the ACM and the test article.

1.3.3.4 Switch

This multiplexer puts interrupt and address words or data words onto the data bus in proper order at the proper time. The switch also selects the "INTERRUPT MODE" or "DATA I/O MODE" bus loading by switching "FAST DATA" and "FAST INTERRUPT and ADDRESS" blocks or the "LOAD DATA" and "INCREMENT ADDRESS" onto the data bus. Switching control is from either ACM or test article.

1.3.3.5 Normal Interrupt Request

This block sends an interrupt request to the test article. This request is sent when a particular bit is set in the interrupt/address register of the "LOAD DATA" or "INTERRUPT/ADDRESS" block.

1.3.3.6 Cycled Interrupt Request

This module sends a repetition of interrupt requests at timed intervals. This maintains a rapid interrupt I/O mode for a specific number of cycles determined by a counter in this request block. Request control is provided by both the ACM and the CP-32.

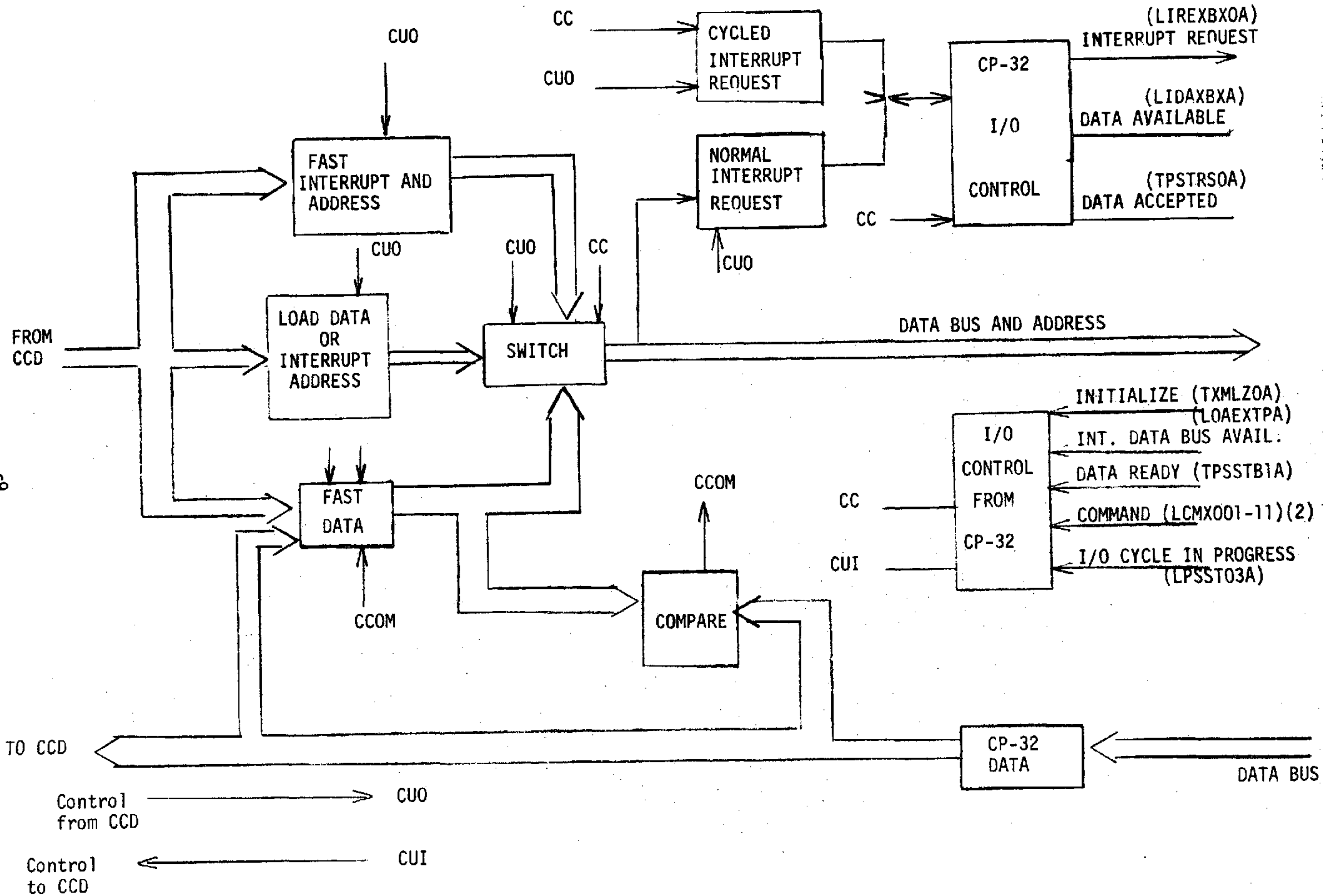


FIGURE IV-8. DATA BUS CONTROLLER

1.3.3.8 Comparator

This device is used in the "high speed" interrupt I/O mode. In this mode, the CP-32 is interrupted and asked to take a data word. This word is to be manipulated inside the test article and then outputted on a PUT cycle to "CP-32 DATA" block. The comparator will check the inputted data word to see if the CP-32 has correctly completed its I/O routine. If so, the comparator will allow the word in "CP-32 DATA" block to be strobed into the "FAST DATA" block providing a new data word for the CP-32 to act upon in the next interrupt I/O cycle.

1.4 Power Supply Additions

In addition to signal interface circuitry, the UTE must be modified to prime power to the test article.

The test article is either powered by 28 volts D.C. or 115 V.A.C. at 400 cycles. (Power testing is in Appendix G).

It is required that the power supply be programmable so that voltage profiles and power interrupts may be created.

1.4.1 Voltage Profiles

Programmability should be provided so that prime power may be varied as a minimum 10% above or below the nominal input voltage specifications. Further programmability should be considered to adjust the voltage magnitudes in accordance with the Apollo fuel cell profiles.

1.4.2 Power Transients and Interrupts

Power transients and interrupts are critical parameters in computer operations. The power supply should have the capability of being interrupted over a wide range of pulse widths so that the test article power transient characteristice can be established. If it is necessary to introduce transients on the lines by implementing short narrow voltage pulses, then additional hardware will be required. This hardware should be designed to inject voltage pulses into the primary power cable at various amplitudes and durations.

1.5 Cooling Hardware

Cooling hardware should be implemented with a forced air system of sufficient capacity to cool the test articles. Manually movable valves should be provided to decrease air flow so that the effect of temperature change on computer operation can be observed.

Thermosensors shall be strategically placed on the test article so that temperature versus computer operation can be correlated. (Appendix H shows a thermo-testing system).

C. SOFTWARE

1.0 SOFTWARE APPROACH

The use of Unified Test Equipment (UTE) software provides modular software functions which will fulfill the major requirement of the UCTS Program. The UCTS will make full use of UTE Test Language (UTETL) to execute tests on the test article. A brief description of the UTE software and UTETL is

1.0 Software Approach (continued)

included in Appendix F. Figure IV-3 shows the Software currently implemented for the DCM and ACM modules.

1.1 Software Modification

Some modifications in existing software of the Test Operating System (TOS) will be required for processing of responses in the DCM. Special Routines that cannot be handled by UTETL will be a combination of Test Language and Assembly language programs. Modification in the ACM software will involve the microprograms of the Command Formatter and Sequencer (CF&S) and the Response Formatter (RF). Routines to adapt the hardware interface changes and Computer Adapter Module (CAM) for Test Language control will be implemented with assembly language.

1.2 Software Additions

For the purpose of computer testing, new test procedures will need to be written using UTETL. These procedures will activate the test article's Diagnostic Test Routines provided with the candidate computer and handle responses necessary to conduct Diagnostic Test, record status, provide reporting and test data logging.

APPENDIX A

PROBLEM REPORTS

PROBLEM SURVEY

PROBLEM: Bad Connectors

DESCRIPTION: Bad connectors account for a large percentage of field problems.

SOLUTION: Evaluate connectors for human engineering factors.

SOURCE OF INFO: Grumman

DATE OF INFO: 9/7/72

* * *

PROBLEM: Out of Spec Pulse

DESCRIPTION: A system interface pulse was out of spec and did not allow proper system operation. The factory test equipment could not detect faulty pulse.

SOLUTION: Make design change to
1. Prime Equipment
2. Test Equipment

SOURCE OF INFO: G.E. Utica

DATE OF INFO: 8/30/72

* * *

PROBLEM: Computer "Lock-Up"

DESCRIPTION: The lock-up was characterized by an ignoring of all input stimuli.

SOLUTION: The only known cure was to remove computer from craft and correct via a Computer Test Set in the G.N.&C. lab. Later findings showed that large EM disturbances could cause and also cure "lock-ups".

SOURCE OF INFO: Apollo Program Computer print-out Computer Vol. IV.

DATE OF INFO: June 20, 1972

PROBLEM: Case Ground Signal Ground Isolation

DESCRIPTION: RF transient testing by induced electrostatic discharges (spark test) showed that computer signal ground to computer case isolation was detrimental. Distributed capacity between wiring and the case was large, providing return paths for transient currents between power lines and case. This made computer sensitive to spark type transients, even though it was insensitive to transients between power lines.

SOLUTION: Computer signal ground and case were connected at multiple points.

SOURCE OF INFO: Apollo Program Computer print-out Computer Vol. IV

DATE OF INFO: 6/20/72

* * *

PROBLEM: Multipoint Ground System

DESCRIPTION: During factory system checkout erroneous information was present on signal lines to test equipment in a multi-grounded system.

SOLUTION: Get rid of multiground system and replace with good design practice single point ground system.

SOURCE OF INFO: G.E. Utica

DATE OF INFO: 8/30/72

* * *

PROBLEM: Rapid I/O Transactions

DESCRIPTION: Speed of processor was decreased by up to 50% when rapid I/O transactions are required.

SOURCE OF INFO: G.E. Houston

DATE OF INFO: 8/15/72

PROBLEM: Rapid Interrupt Sequence

DESCRIPTION: In hardware system test the computer's program was messed up by too many interrupts. The simulated flight test (which was the factory final acceptance test) did not check this function.

SOLUTION:
1. Major computer design change
2. Limit the frequency of interrupts
3. Modify in-house testing to detect problem

SOURCE OF INFO: GE Pittsfield

DATE OF INFO: 8/22/72

* * *

PROBLEM: Turn-on & Shut-Down

DESCRIPTION: When the uplink equipment was turned on or in some cases when turned off, the equipment would emit one or more pulses. These pulses would remain in the AGC register and would cause the first data transmission to be in error.

SOLUTION: Register must be cleared before transmission

SOURCE OF INFO: Apollo Program computer print-out R-700 Computer Vol. IV

DATE OF INFO: 6/20/72

* * *

PROBLEM: Adjacent Signal Cross Talk

DESCRIPTION: Occasional errors in reading radar data.

SOLUTION: An AGC hardware/software interaction was resulting in a split radar sync pulse output. The timing of a clear and restore action in channel 13 due to a write instruction was partially synchronized with the timing strobe for the sync pulse output. This resulted in possible split pulse generation for the sync pulse. This was solved in software by preventing channel output use during radar data reading. A hardware design change could also have solved this problem.

SOURCE OF INFO: Apollo Program computer print-out R-700 Computer Vol. IV

DATE OF INFO: 6/20/72

PROBLEM: Interference Problem (Interface)

DESCRIPTION: While updating contents of memory, the computer would reject or interrupt transmissions, from the ground and signal uplink alarms.

SOLUTION: The alarms resulted from noise on the umbilical input lines, used during prelaunch checkout. A radio telemetry/GSE control was added to eliminate noise pickup after launch.

SOURCE OF INFO: Apollo Program Computer print-out R-700 Computer Vol. IV

DATE OF INFO: 6/20/72

* * *

PROBLEM: Computer Stoppage

DESCRIPTION: The Digital Geo-Ballistic Computer suffered from an abnormal number of computer "stoppages". These stoppages were defined as computer malfunctions which prevented execution of required operations at "high speed". No obvious reasons for the malfunctions were noticed and no corrective action on the part of the operator was required to resume normal operation. By manually restarting the computer the same faulty indications would not occur and normal operations would resume.

Causes for Failure:

1. Majority of stoppages due to improper instruction being read out or written in.
2. Low output voltage introducing logic failure.
3. Marginal components render entire computer marginal in operation.
4. Program Errors

SOLUTION:

1. Noise on control delays (due to excess negative voltage on the clock oscillator output) was reduced by clamping the clock module.
2. New cables with larger flex life (10,000 flexes)
3. Five timing changes were made to the memory cycle timing and procurement specifications were changed on a number of modules to tighten their propagation time.

DATE OF INFO: 5/5/67

PROBLEM: Inadequate Burst I/O Capability

DESCRIPTION: 100K words per second burst I/O transfer rate through CPU required by Equipment Specification. Production equipment achieves only 60K to 65K words per second transfer rate.

SOLUTION: Not yet determined--so far work around and suffer.

DATE OF INFO: 8/14/72

COMMENTS: This is qualified production computer with no deviation on this item and over 100 production computers have been delivered. It would be interesting to learn if original qual test was inadequate or whether subsequent design change ECP was inadequately incorporated. This is design deficiency.

* * *

PROBLEM: Memory

DESCRIPTION: 90% of computer problems are bad memory bits from various causes including EMI. Usually occur during power up and power down.

SOLUTION: Check like crazy during power up and down.

SOURCE OF INFO: Grumman

DATE OF INFO: 9/7/72

* * *

PROBLEM: Bit Creep Effects at Low Temperature

DESCRIPTION: Bit location changes were evident only at low temperature in the PWM test.

SOLUTION: Change layout of PWM system.

Tighten quality control of PW.

SOURCE OF INFO: G.E., Pittsfield

DATE OF INFO: 8/22/72

PROBLEM: Bit Creep in PWM at Ambient Temperature

DESCRIPTION: After many memory cycles there was a tendency for bits to change either in state of location thus "creep".

SOLUTION: Better quality control of the wire.

Change layout of PWM.

SOURCE OF INFO: G.E., Pittsfield

DATE OF INFO: 8/22/72

* * *

PROBLEM: Adjacent Word Disturb

DESCRIPTION: Adjacent words were being jumbled when the write cycle took place in the biax memory.

SOLUTION: Software restore.

Leave blank spaces in memory.

SOURCE OF INFO: G.E., Utica

DATE OF INFO: 8/30/72

* * *

PROBLEM: Unterminated Signal Connector Pin

DESCRIPTION: Logical input wires used for testing became unterminated when in spacecraft configuration. This provides coupling internal to the computer between high level system mode interface signals and computer logic.

SOLUTION: A special test connector cover was designed which grounded these test signal inputs preventing coupling.

SOURCE OF INFO: Apollo Program Computer print-out Computer Vol. IV

DATE OF INFO: 6/20/72

PROBLEM: Adjacent Signal Cross Talk

DESCRIPTION: Analysis of erroneous information indicated adjacent line interference.

SOLUTION: Double shielded signal lines.

SOURCE OF INFO: G.E., Utica

DATE OF INFO: 8/30/72

* * *

PROBLEM: Long Cables

DESCRIPTION: Long cable (50ft.) was used for part of system checkout. Erroneous data was pronounced on signal lines.

SOLUTION: Single point ground.

Double shielded signal lines.

SOURCE OF INFO: G.E., Utica

DATE OF INFO: 8/30/72

* * *

PROBLEM: Signal Transients Induced by Cable Separation

DESCRIPTION: Transients were seen on the signal lines as the ground unibical was removed which caused system errors.

SOLUTION: System factory testing did not check this condition, only found in final hardware testing.

Introduce simulated noise spikes on lines during factory checkout.

SOURCE OF INFO: G.E., Pittsfield

DATE OF INFO: 8/22/72

PROBLEM: Power Transient Problem

DESCRIPTION: When the computer was switched between standby and operate, a power transient internal to the computer would modulate the clock sync signals to the spacecraft. This modification would sometimes cause down telemetry to drop out of sync for about 1 sec.

SOURCE OF INFO: Apollo Program Computer print-out Computer Vol IV

DATE OF INFO: 6/20/72

* * *

PROBLEM: Lost Memory Bits Due to Power Up and Down

DESCRIPTION: When tech switched computer on and off repeatedly, memory bits were lost.

SOLUTION: Capacitor controlling shutdown sequence did not completely discharge when fast switched. Guarantee discharge during shut off period or change shutdown logic.

SOURCE OF INFO: Grumman

DATE OF INFO: 9/7/72

* * *

PROBLEM: Low Prime Power

DESCRIPTION: Random failures were observed with no apparent cause.

SOLUTION: Investigation showed that the prime power was low due to power line drop.

SOURCE OF INFO: G.E., Pittsfield

DATE OF INFO: 8/22/72

PROBLEM: Equipment would not work for 5 min. after turn on, after being soaked in cold at -65°C for 2 hours.

DESCRIPTION: It was found that the equipment failed or worked erroneously within the first 5 minutes after cold soak. This failure was first discovered on the vehicle by accident.

SOLUTION: There was a temperature sensitive op amp that caused the problem.

Look at operation of system in factory during warm up.

SOURCE OF INFO: G.E., Pittsfield

DATE OF INFO: 8/22/72

* * *

PROBLEM: Erroneous Data During Warm up.

DESCRIPTION: During the first 5 to 10 minutes of operation, the system appeared to fail.

SOLUTION: It was found that the test equipment had a 20 minute warm up cycle required. The test equipment and prime equipment were both turned on together, not allowing proper test equipment warm up.

SOURCE OF INFO: G.E., Utica

DATE OF INFO: 8/22/72

* * *

PROBLEM: Power Supply EMI

DESCRIPTION: EMI originating within the computer power supply caused bits to be intermittently added or deleted within the computer.

SOLUTION: Redesign the power supply to eliminate and adequately attenuate the P/S EMI.

DATE OF INFO: 8/21/72

PROBLEM: Power interrupts recycle different for different equipment

DESCRIPTION: When a primary power transient occurs, the primary computer and interfacing equipments all go through individually controlled power interrupt cycles. However, the interval start and end times for each equipment occurs at different times. Thus, garbage information can get into the computer.

SOLUTION: So far, to live with it and suffer.

DATE OF INFO: 8/21/72

COMMENTS: This is avionics system problem, but has major impact on computer application.

* * *

PROBLEM: Language Selection

DESCRIPTION: It was found that (HOL) will directly affect processor speed if language and hardware are not compatible.

SOLUTION: Choose compatible language

SOURCE OF INFO: G.E., Houston

DATE OF INFO: 8/15/72

* * *

PROBLEM: Computer Stoppage

DESCRIPTION: Computer stopped (4 PI EP computer)
Analysis: A specific sequence of instructions stalled the computer.

SOLUTION: Design change had to be implemented in the hardware.

SOURCE OF INFO: G.E., Houston

DATE OF INFO: 8/15/72

PROBLEM: Priority Interrupt Lockup

DESCRIPTION: When highest priority interrupt signal fails to yield a "1" level, entire computer is totally "hogged" locking out all other computation functions. Lesser priority interrupt signals have same problem to lesser degree.

SOLUTION: Change design of I/O circuit so that computer does not respond to the interrupt until the trailing edge of the interrupt pulse has occurred.

DATE OF INFO: 8/14/72

COMMENTS: First implementation was poor design.

* * *

PROBLEM: Multiple I/O Processing Deficiency

DESCRIPTION: The computer has a JUMP I/O CHANNEL instruction. This instruction refuses to execute under most specified allowable conditions.

SOLUTION: Design change is planned. In meantime work around and suffer.

DATE OF INFO: 8/21/72

COMMENTS: This is computer design deficiency.

* * *

PROBLEM: Interface Equipment Cable Disconnect

DESCRIPTION: When computer is operating and interconnecting cable is disconnected, computer I/O register stages individually and semi-randomly go to a "1" or "0" state. This permits "garbage" information to get into the computer which could propagate with undesirable results.

SOLUTION: Work around solution of leaving all equipments connected when power is ON except in special controlled cases.

DATE OF INFO: 8/14/72

COMMENTS: This is a result of specification deficiency--both system and computer specification.

PROBLEM:	Non-Legal Code Acceptance
DESCRIPTION:	Computer sometimes carries out undesired action on non-legal code rather than rejecting or trapping it.
SOLUTION:	Do not know if problem fixed or not.
DATE OF INFO:	8/14/72
COMMENTS:	Design deficiency

APPENDIX B

TEST METHODS SURVEY

TEST METHODS SURVEY

TEST #1: TRANSIENT RADIATION

DESCRIPTION: Transient Radiative Susceptibility.

The test shall be performed in accordance with Figure 7. The relay used shall be MS25271 or equivalent. No suppression shall be applied to the relay. The relay circuit shall be unshielded wire tightly coupled (taped) to, and in parallel with, the equipment power leads and signal leads, and tightly looped about the units of the equipment comprising the test sample. The test shall be performed twice, first with the DPDT switch in position B and then A. The tests shall be run for a period of at least 5 minutes in each switch position. If the unit is susceptible, each threshold of susceptibility shall be determined by moving the relay circuit wire away from the bundle or case.

ELEMENTS TESTED: TRANSIENT RADIATIVE SUSCEPTIBILITY

SOURCE OF INFO: Grumman Aerospace Corporation

DATE OF INFO: 2/10/72

COMMENTS: See sketch (Figure 7)

TEST #35: EMI ELECTRIC FIELD SUSCEPTIBILITY

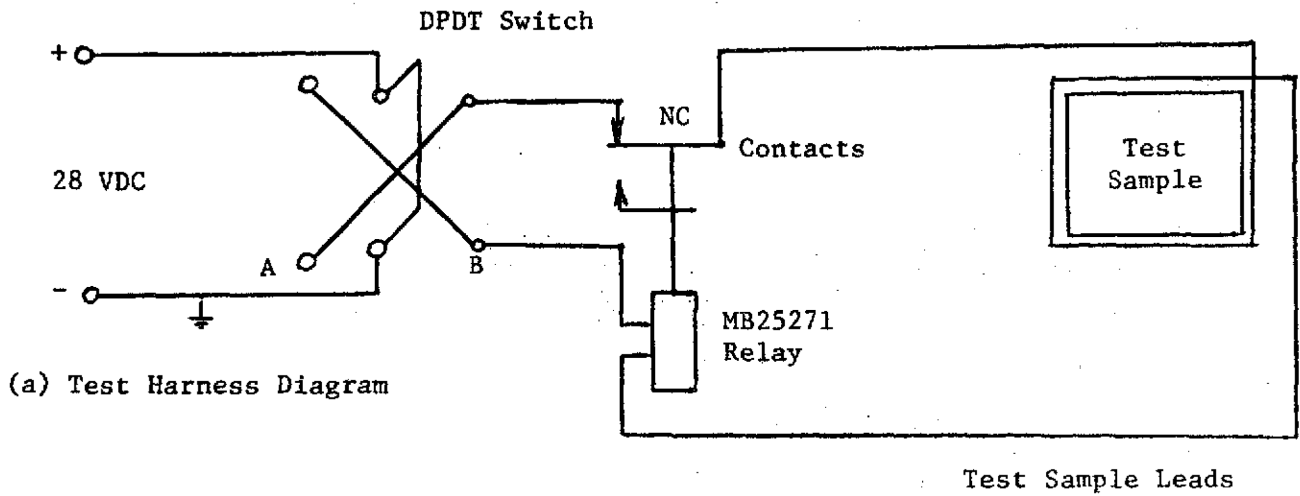
DESCRIPTION: Operation of the computer in a specified E field without malfunction.

REASON: Measure the unit's level of RF radiated susceptibility over broad frequency range.

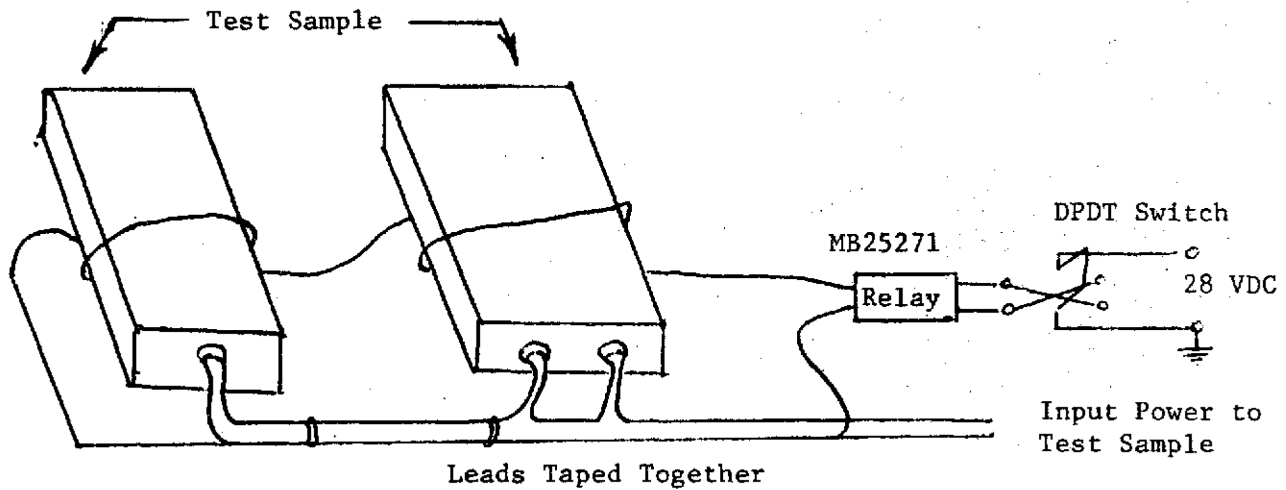
ELEMENTS TESTED: Circuit susceptibility - case shielding and cable shielding.

SOURCE OF INFO: MIL-STD-461 and other recent EMI specs for equipment.

COMMENTS: Shielded room is necessary.



(a) Test Harness Diagram



(b) Test hookup

FIGURE 7

TRANSIENT RADIATED INTERFERENCE SUSCEPTIBILITY

TEST METHODS SURVEY

TEST #38: MAGNETIC FIELD RADIATED SUSCEPTIBILITY

DESCRIPTION: Subject the computer to AC magnetic fields (30 Hz to 30 KHz).

REASON: Establish susceptibility relative to spec limit.

ELEMENTS TESTED: Magnetic devices.

SOURCE OF INFO: MIL-STD-461 and 462

DATE OF INFO: Current

TEST #34: EMI MAGNETIC FIELD SUSCEPTIBILITY

DESCRIPTION: Operation of the computer in a DC or low frequence AC (or pulsed) magnetic field without malfunction.

REASON: A test of the susceptibility of magnetic components to stray fields present on spacecraft or aircraft.

ELEMENTS TESTED: Magnetic memory and inductors.

COMMENTS: There are several variations of this test.

TEST #37: EMI - AUDIO AND RF SUSCEPTIBILITY ON PRIMARY POWER LINES (30 HZ to ?)

DESCRIPTION: Couple audio and RF sine wave signals to input power lines at specified levels.

REASON: Measure susceptibility level per spec limit.

ELEMENTS TESTED: Power line filtering
Power supply regulation and high frequency isolation.

SOURCE OF INFO: MIL-STD-461 and other recent EMI equipment specs.

TEST #2: LINE IMPULSES

DESCRIPTION: All lines (excluding power lines). Impulses of 0.001 volt-seconds, at a rate of at least 3 different rates indicative of the most susceptible rates shall be injected into each line of the equipment. The test shall be performed 3 times for various volt-second combinations: Vmax, times t min, V times 2 t min, and V times 4 min. The maximum voltage shall be limited to a value consistent with the maximum line voltage plus the maximum excursion permitted on the line.

ELEMENTS TESTED: Susceptibility to line impulses.

SOURCE OF INFO: Grumman Aerospace Corp.

DATE OF INFO: 10/2/72

- -

TEST #36: EMI - TRANSIENT (SPIKE) SUSCEPTIBILITY ON PRIMARY POWER LINES

DESCRIPTION: Super-impose voltage spike onto power lines at specified level without malfunction of computer.

ELEMENTS TESTED: Power line filtering
Power supply regulation and high frequency decoupling.

SOURCE OF INFO: MIL-STD-461 and other recent EMI equipment specs.

- -

TEST #3: INADVERTENT POWER TRANSIENT

DESCRIPTION: Inadvertent Power Transient Susceptibility

Circuits required to remain in a known state or predetermined initial state as a result of power drop out or power turn off shall demonstrate their required circuit-state configuration as a result of an inadvertent power failure. This inadvertent condition shall be simulated by manually cycling each AC and DC power input (circuit breaker) a minimum of five times at approximately 2 second intervals.

ELEMENTS TESTED: Susceptibility to inadvertent power transients.

SOURCE OF INFO: Grumman Aerospace Corp.

DATE OF INFO: 2/10/72

TEST METHODS SURVEY

TEST #4: POWER LINE PULSES

DESCRIPTION: Power Lines

Pulses, 50 volt amplitude both positive and negative polarity, shall be injected into each AC and DC power lead at a pulse repetition rate of 10 pps minimum for a period of at least 5 minutes for each pulse polarity. The characteristics of the transient pulse, as measured by an oscilloscope across the input terminal of the test sample (while the test sample is operating) shall follow a typical waveshape. Series or parallel injection shall be used. Line stabilization networks shall be removed during these tests. If the equipment is susceptible, each threshold of susceptibility shall be determined by decreasing the pulse amplitude.

ELEMENTS TESTED: Power line pulse susceptibility

SOURCE OF INFO: Grumman Aerospace Corp.

DATE OF INFO: 2/10/72

TEST #5: CABLE BUNDLE TEST

DESCRIPTION: Two insulated, unshielded wires are taped to the cable bundle 90° apart. Apply 20 amp AC @ 400 Hz to each wire one at a time. If unit is susceptible, determine each threshold of susceptibility by two methods: 1. decrease current; 2. carry wire away from bundle.

ELEMENTS TESTED: EMI susceptibility of cable bundle.

ELEMENTS NOT TESTED: System EMI

SOURCE OF INFO: Grumman Aerospace Corp.

DATE OF INFO: 2/10/72

COMMENTS: See Sketch #8.

TEST #6: Voltage and Ground Wire Check

DESCRIPTION: Resistance measurements are made

(a) to see that signal ground is isolated from signal ground

(b) to see that there are no shorts between voltage and signal ground.

REASON: To assure power and ground wiring is proper.

ELEMENTS TESTED: Power and ground connections at I/O connectors.

ELEMENTS NOT TESTED: No operational sequences.

SOURCE OF INFO: GE/Utica

DATE OF INFO: 8/30/72

- -

TEST #7: OSCILLATOR CHECK IN FIELD

DESCRIPTION: Triple redundant oscillator is checked with special test equipment in field by checking each channel then the voted result.

Crystal and electronic component drift including crystal oven was evident over weeks of shelf life.

ELEMENTS TESTED: Triple redundant oscillator.

ELEMENTS NOT TESTED: Remaining system

DATE OF INFO: 8/30/72

COMMENTS: This field test assures that the system will be accurate during the mission.

SOURCE OF INFO: GE/Utica

TEST #8: ELECTROSTATIC DISCHARGE TEST

DESCRIPTION: Equipment subjected to an electrostatic field produced by discharging a 50 ufd capacitor, changes to 10K volts. when applied between equipment case and ground.

ELEMENTS TESTED: Electrostatic Discharge Susceptibility

SOURCE OF INFO: Grumman Aerospace Corporation

DATE OF INFO: 2/10/72

COMMENTS: Grumman suggests testing twice on each face of case.

* * * * * * * * * * * *

TEST #14: SPIKE ON GROUND

DESCRIPTION: Induce capacitor spike on ground line during operation and note results.

Check susceptibility to AC discharges.

ELEMENTS TESTED: All Grounds

ELEMENTS NOT TESTED: Only Grounds on I/O

SOURCE OF INFO: Grumman Aerospace Corporation

DATE OF INFO: 9/7/72

TEST #9: RANDOM INTERRUPT

DESCRIPTION: Randomly vary frequency of interrupts while operating extensive instruction set to increase probability of causing interrupt malfunction.

REASON: To verify that occurrence of interrupt on any instruction does not cause malfunction.

ELEMENTS TESTED: CPU interrupt hardware and interrupt software.

ELEMENTS NOT TESTED: Memory speed

SOURCE OF INFO: GE/Pittsfield

DATE OF INFO: 8/22/72

- -

TEST #10: TEMP VARIATION VERSUS MOISTURE TEST

DESCRIPTION: Power is left on during the controlled cooling of the unit.

To assure that moisture due to condensation, as temperature changes, does not affect the system operation.

ELEMENTS TESTED: Power supply shorting during temperature variation.

ELEMENTS NOT TESTED: Operational hardware as it was not exercised.

SOURCE OF INFO: GE/Utica

DATE OF INFO: 8/30/72

- -

TEST #11: OVER TEMPERATURE RESPONSE

DESCRIPTION: Check response of computer for orderly shutdown to overtemp.

REASON: Many computers just quit in overtemp. mode.

ELEMENTS TESTED: Power supply and overtemp protect.

SOURCE OF INFO: Grumman

DATE OF INFO: 9/7/72

TEST METHODS SURVEY

TEST #12: THREE PHASE UNBALANCE

DESCRIPTION: Check operation of computer with unbalanced three phase input.

REASON: Found some computers power monitor did not respond to 3 phase unbalance.

ELEMENTS TESTED: Power supply - shutdown logic.

SOURCE OF INFO: Grumman Aerospace Corporation

DATE OF INFO: 9/7/72

* * * * * * * * * * * * * *

TEST #13: POWER SUPPLY TRANSIENTS AND SWITCH TOGGLES

DESCRIPTION: Evaluate computer response to various transients and verify operation if ON/OFF switch is switched 3-10 times.

REASON: Found computers used capacitor for shutdown and switching did not allow them to discharge and lost memory bits resulted. Some computers are too sensitive to transients, other not sensitive enough.

ELEMENTS TESTED: Power supply, memory, shut-down logic.

ELEMENTS NOT TESTED: General Logic of CPU

SOURCE OF INFO: Grumman Aerospace Corporation

Date of INFO: 9/7/72

TEST #26: MAXIMUM INTERRUPT SPEED

DESCRIPTION: Increase frequency of interrupts as computer is performing program until computer can no longer handle main program.

REASON: This allows the computer's speed under interrupt conditions to be evaluated at the same time the interrupt system efficiency is evaluated.

ELEMENTS TESTED: Logic hardware, interrupt hardware, logic speed, interrupt speed, interrupt efficiency.

SOURCE OF INFO: GE/Pittsfield

DATE OF INFO: 8/22/72

COMMENTS: Suggested as a possible test idea if typical operating system simulated.

TEST #28: EMI - SUSCEPTIBILITY THRESHOLD OF COMPUTER INPUT AND OUTPUT CHANNELS

DESCRIPTION: CW, CW-AM modulated, CW-pulsed modulated , video pulses and spikes are coupled to selected input and output circuits and their amplitude is increased until a failure occurs.

REASON: If the susceptibility level of these circuits is known, then system integration people would know how much noise or pick-up could be allowed in the system.

ELEMENTS TESTED: Common mode and other forms of rejection of undesired serials. Susceptibility of circuits, frequency response, etc.

SOURCE OF INFO: This information is required by MIL-STD-6051D for integration of space and aircraft electronic equipment.

DATE OF INFO: Recent (1972)

COMMENTS: The test normally requires a large quantity of test equipment items to cover large free range and several modulations (30 Hz to 1 GHz). Coupling of the signals to data lines, telemetry lines etc. without changing their characteristics is not simple. Usually requires active coupling circuits.

TEST #29: EMI - CONDUCTED EMISSIONS FROM THE COMPUTER (TIME DOMAIN MEASUREMENT)

DESCRIPTION: A measurement of noise or unnecessary signals on computer interface lines that could cause interference elsewhere in a system. The measurement could be made in the time domain with voltmeters or oscilloscope.

REASON: If this is known, it can be compared to the interface susceptibility threshold levels for other equipment in the system and interference problems revealed.

SOURCE OF INFO: Required for MIL-STD-6051D System Compatibility Specification

DATE OF INFO: Recent (1972)

COMMENTS: Measurement of computer generated signals only requires isolation from other peripheral equipment or circuits. Measurements in the time domain results in limited information when a conglomeration of signals is being considered. (Peak values only). Time domain measurements are simple compared to most frequency domain measurements. They are one shot with wide bandwidth device.

TEST #30: EMI - CONDUCTED EMISSIONS FROM THE COMPUTER (FREQUENCY DOMAIN MEASUREMENT)

DESCRIPTION: A measurement of noise or unnecessary signals on computer interface lines that could cause interference elsewhere in a system. The measurement would be made with a receiver with a restricted band width scanned over the frequency range of interest.

REASON: These measurements could be used for system integration planning or directly compared with MIL-Specs for equipment requirements.

ELEMENTS TESTED: Data lines - power lines, etc.

ELEMENTS NOT TESTED: Lines internal to the computer.

SOURCE OF INFO: MIL-STD-461 and others

DATE OF INFO: recent (1972)

COMMENTS: Test requires special and expensive equipment but is necessary to check to MIL-STD for computers.

TEST #31: EMI - STATIC, RESIDUAL OR RESULTANT MAGNETIC FIELD EMISSION OR MAGNETIC DIPOLE MOMENT OF THE COMPUTER

DESCRIPTION: This is a measurement of the resultant magnetic field at a point or points of all the magnetic sources within the computer. Magnetic dipole moment or torque on the unit by reactions with an external magnetic field can be calculated from this measurement.

REASON: Used for control of spacecraft position.

ELEMENTS TESTED: Magnetic devices and material within the computer - power on and off.

SOURCE OF INFO: This is a NASA requirement used on GEOS and others.

DATE OF INFO: Recent (1972)

COMMENTS: Magnetometer and area of low mag field int necessary.

TEST #33: EMI- E FIELD RADIATED EMISSIONS FROM THE COMPUTER

DESCRIPTION: A field intensity measurement taken a short distance from the unit (1 meter) over a frequency range of interest.

REASON: Evaluation of radiated fields which could cause interference in a system.

ELEMENTS TESTED: Shielding of enclosure and cables.

SOURCE OF INFO: Current Mil Specs.

COMMENTS: Impossible to perform without shielded room.

TEST #39: MAGNETIC FIELD (AC) RADIATED EMISSION

DESCRIPTION: Measurement of computer generated magnetic fields (38 H_Z to 30 KH_Z) with 100P sensor and volt meter and or tunned receiver.

REASON: To check field against MIL-SPEC-limit.

ELEMENTS TESTED: Magnetic devices.

SOURCE OF INFO: MIL-STD-461 and 462

DATE OF INFO: Current (1972)

TEST #40: RF CONDUCTED SUSCEPTIBILITY ON POWER LINES

DESCRIPTION: Capacitor couple RF (30 HZ to 400 HZ) to the computer primary power lines.

REASON: To establish the susceptibility of the unit relative to a MIL-spec level.

ELEMENTS TESTED: Power supply and input filtering.

SOURCE OF INFO: MIL-STD-461 and 462

DATE OF INFO: Current (1972)

COMMENTS: Requires signal of about 1 volt into low Z of power supply.

TEST METHODS SURVEY

TEST #42: ECHO CHECK

DESCRIPTION: Reads input data from I/O into memory and then reads it back to external device via CPU. Can be run via DMA channel.

REASON: Checks I/O and Memory cricuits for proper operation and checks CPU transfer operations if DMA not used.

ELEMENTS TESTED: I/O operation, memory, CPU control and transfer logic.

ELEMENTS NOT TESTED: CPU logical, shifting or arithmetical operation; very little software.

SOURCE OF INFO: GE/Pittsfield

DATE OF INFO: 8/22/72

COMMENTS: Easily implemented as part of other tests. Too expensive on complete memory test but verifies cperation of control.

TEST #43:	POWER INTERRUPT
DESCRIPTION:	Power is interrupted from prime power supply to specs. Wider than field system spec.
REASON:	To assure that field operation under narrower specs will be proper when power is interrupted.
ELEMENTS TESTED:	Power converter power storage capability under worse than system conditions.
ELEMENTS NOT TESTED:	All other Hardware.
SOURCE OF INFO:	GE/Utica
DATE OF INFO:	8/30/72

TEST #44:	CIRCUIT PROTECTION ON TEST CONNECTORS
DESCRIPTION:	Resistance measurements are made on the test point connector between the test points and ground.
REASON:	To assure that the test point circuit protection resistors are correct and in place.
ELEMENTS TESTED:	Test connectors and protective resistors.
ELEMENTS NOT TESTED:	All other system functions.
SOURCE OF INFO:	GE/Utica
DATE OF INFO:	8/30/72

TEST #45:	MEMORY SUM CHECK
DESCRIPTION:	Check sum of outputs from memory after loading memory or from ROMS.
REASON:	To verify operation of memory read/write circuits, memory, and address circuits.
ELEMENTS TESTED:	Memory (ROM, RAM, P.W, CORE) addressing logic, read/write logic, control ckts.
ELEMENTS NOT TESTED:	CPU logic, software
SOURCE OF INFO:	GE/Pittsfield
DATE OF INFO:	8/22/72
COMMENTS:	Appears to be limited to small memory systems.

TEST #46: MEMORY PROTECT VERIFICATION

DESCRIPTION: Verify that memory protect operates under all conditions.

REASON: Some memory protects failed under extremes.

ELEMENTS TESTED: Memory and protect logic.

SOURCE OF INFO: Grumman

DATE OF INFO: 9/7/72

TEST #47 I/O SPEED AND BUFFERING

DESCRIPTION: Check that no timing glitches exist between I/O inputs and CPU. Check speed of I/O versus operation.

REASON: Some I/O's improperly buffered or buffered make too slow.

ELEMENTS TESTED: I/O

SOURCE OF INFO: GE/SSO, Valley Forge

DATE OF INFO: 9/8/72

TEST #48 RANDOM BIT WORD GENERATOR PARITY CHECK

DESCRIPTION: The random words and parity are generated by random bit generator and computer checked for number of parity errors.

REASON: To check parity circuitry

ELEMENTS TESTED: Memory, Parity circuits

ELEMENTS NOT TESTED: Logic, control logic, addressing logic.

DATE OF INFO: 9/7/72

COMMENTS: A better alternative would seem to be to generate both correct and incorrect words and vary operation.

Note: Assume even sets bit

WORD	PARITY	CORRECT
E	0	No
0	0	Yes
E	1	Yes
0	1	No

Expect 50% non-function.

APPENDIX C

CANDIDATE SUBROUTINE REQUIREMENTS SPECIFICATION

APPENDIX C

CANDIDATE SUBROUTINE REQUIREMENTS SPECIFICATION

C.1.0 INTRODUCTION

Typical specifications which would be presented to the computer manufacturer for the purposes of writing resident test software is presented herein.

The following specifications are presented:

- Memory Access and Crosstalk exerciser
- Time Class of Instructions
- Convert to Engineering Units

Also presented in this section are specifications for the resident operating system that is necessary to interlink and dispatch the proper test programs.

C.2.0 MEMORY ACCESS AND CROSSTALK TEST

2.1 Identification

Memory access and crosstalk exerciser.

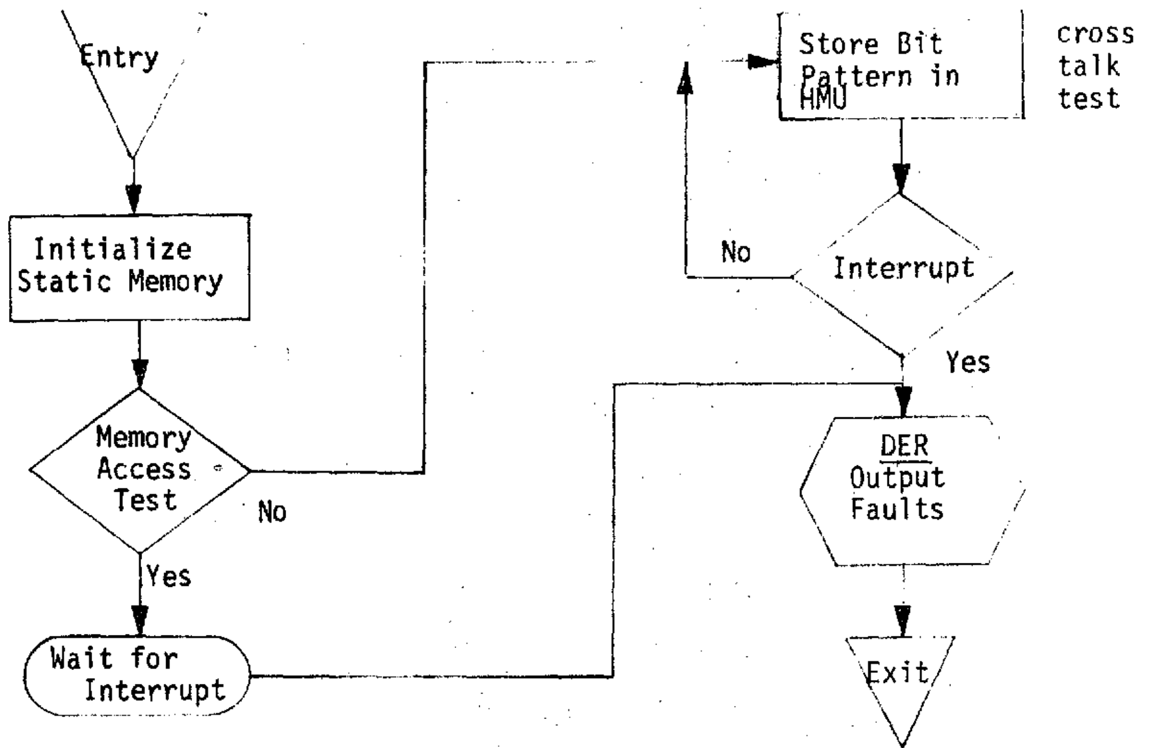
2.2 Purpose

This subroutine tests the CPU memory access time, and the effects of partitioned high memory utilization on adjacent memory (bit creep). This test will also be used to determine the effect of memory access time variations.

2.3 Program Requirements

Input parameters will be used to determine initial values and areas of memory to be tested. A Direct Memory Access (DMA) will allow an external device to access memory at controllable rates.

2.4 Flow Chart



2.5 Detailed Functional Requirements

2.5.1 Data Input

Parametric data supplied as control statements is stored in the Resident Job List by the Supervisor prior to a run. This data will, for the crosstalk test, consist of initial memory values and the area of memory to be partitioned as high memory utilization (HMU) and the area of memory to remain static.

2.5.1.1 Cross Test Data Format

No. of Bytes
Subroutine Number
Concurrency FLG
Initial Value
Test Value
Start Address HMU
Ending Address HMU
Start Address Static
Ending Address Static

Parametric data for memory access time test will be an initial value for static memory and the area of memory to be declared as static memory.

2.5.1.2 Access Time Test Data Format

No. of Bytes
Subroutine No.
Concurrency FLG
Initial Value
Start Address
Ending Address

2.5.2 Data Processing

The area of memory specified in the parameters data is initialized to the desired value. For the memory access time test, the computer is placed in a wait state. At this time, the direct memory access testing device is activated. When the external DMA test is completed, the specified area of memory is checked for values different than the initial values. Failures can also be noted by "scoping" the memory base.

The high memory utilization test constantly stores in the area of memory of HMU a bit pattern specified until interrupted. The area of memory declared as static is checked for values different than the initial values.

2.5.3 Data Output

All static memory addresses that changed in value are placed in the output area. The initial value along with the faulted values are placed in the output area.

2.5.3.1 Data Format

Subroutine No.
No. of Words
Initial Value
Fault Address
Bit Address
Fault Address
Bit Address

C.3.0 TIMING TEST

3.1 Identification

Time Classes of instructions.

3.2 Purpose

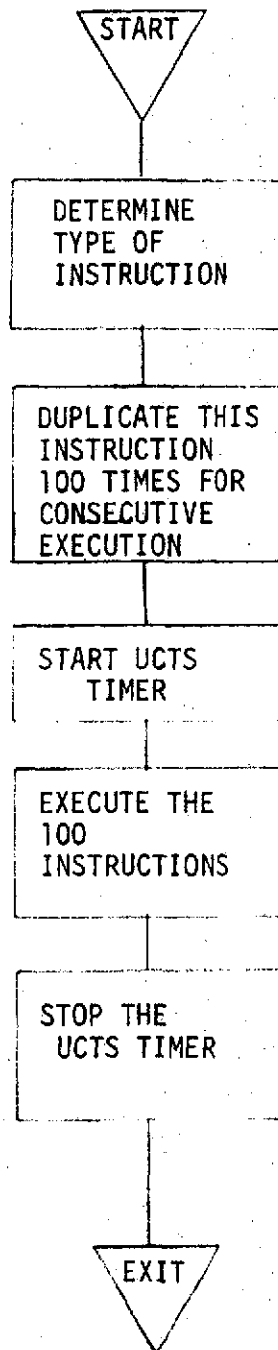
This program will demonstrate the CPU's speed for executing certain instructions. It will be required to do this with and without cycle stealing interference in the main frame memory. This test will be used to verify the manufacturer published specifications for instruction execution time.

3.3 Program Requirements

This subroutine will use the provided parameters to construct a series of instructions in its own machine language. This series of instructions will be executed while the UCTS timer is running so that accurate measurements of instruction timing can be obtained.

3.4 Summary Flow

INSTRUCTION EXECUTION PROGRAM



3.5 Detailed Functional Requirements

3.5.1 Data Input

The data input will be a parameter telling the candidate computer what type of instruction to do. (i.e., as full word add, a full word multiply, etc.)

Data Format

No. of Bytes
Subroutine No.
Concurrency
Instruction No.

3.5.2 Data Processing

The instruction number will be used to determine what type of instruction to execute. It should be used as an index to a table that contains the actual machine code for the appropriate instruction in the computer under test. The instruction to be tested should then be picked from the table and should be stored in 100 consecutive locations. A command should then be sent to the UCTS to start the timer after which the 100 duplicate instructions should be executed. After the 100 instructions are executed, a command should be sent to stop the UCTS timer.

3.5.3 Output

Commands should be sent to the UCTS to start and stop its elapsed timer.

C.4.0 CONVERSION TEST

4.1 Identification

Convert to Engineering Units.

4.2 Purpose

This subroutine demonstrates the CPU ability to convert fixed point data (representative of Spacecraft PCM data) to Engineering Units. It also (as an option) converts the Engineering unit value to a BCD code suitable for display.

4.3 Program Requirements

This subroutine will, when called, act upon the resident parameters previously read in to obtain data and calibration values to perform the Engineering unit conversions. The conversion from raw data for those measurements that are to be processed as engineering units is by linear interpolation. This is accomplished by using precomputed calibration data points y0, Y1, --- yn.

Data ranges in this program are as follows:

a. The largest absolute value that will be used is 9999.

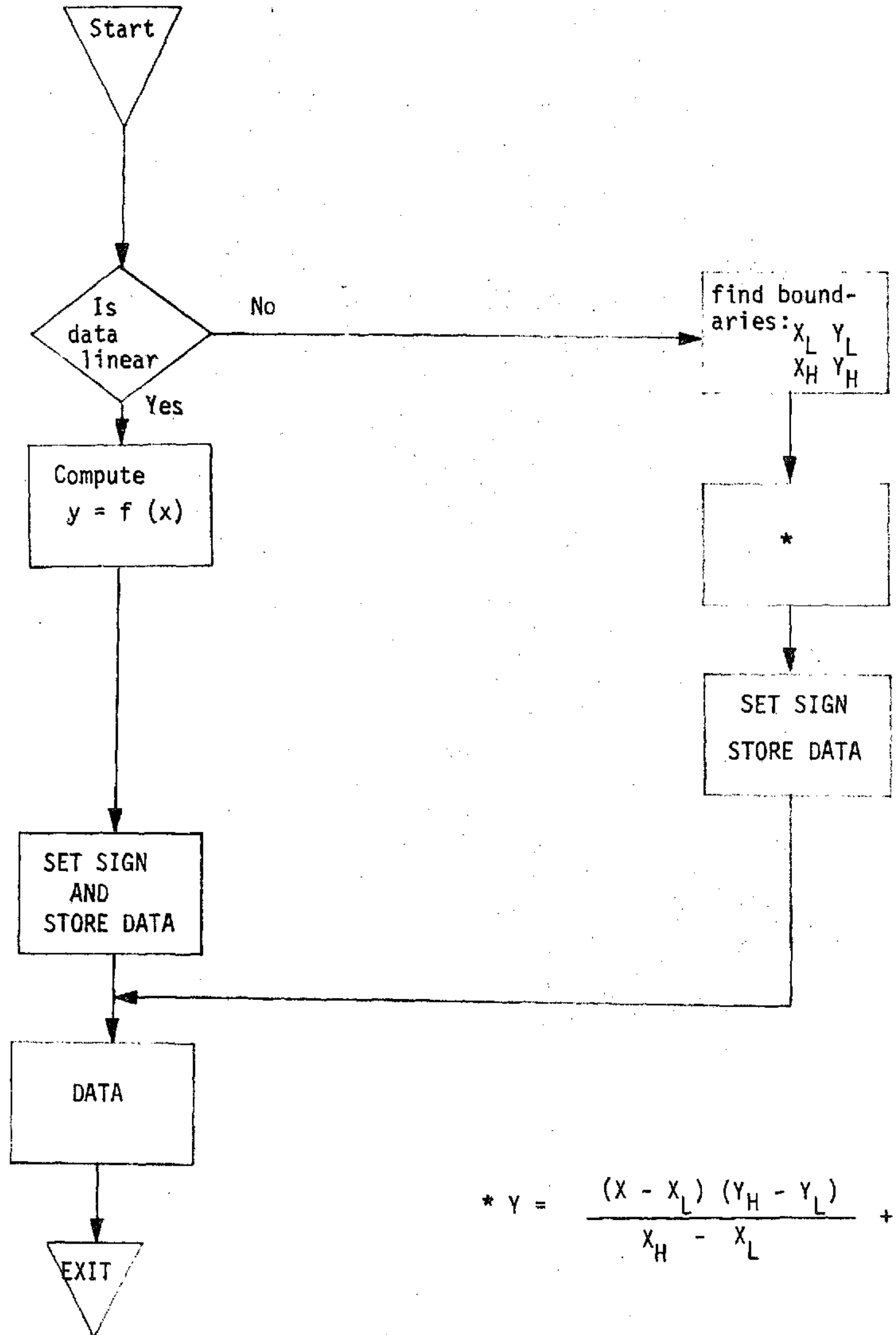
b. The maximum output value is also 9999.

c. All values must be considered whole values, therefore all scaling is done prior to the input of the values.

d. The PCM data or raw data is an 8 bit count value.

4.4 Summary Flow

Convert Subroutine



$$* \; Y = \frac{(X - X_L)(Y_H - Y_L)}{X_H - X_L} + Y_L$$

4.5 Detailed Functional Requirements

4.5.1 Data Input

The raw data and calibration data will be previously stored in the resident job list as parameters. The subroutine when called should use a register that points to this data.

a. Data Format

NO OF BYTES

Subroutine No.

Concurrency

Raw Data

x_o

y_o

x_1

y_1

x_2

y_2

x_n

y_n

4.5.2 Data Processing

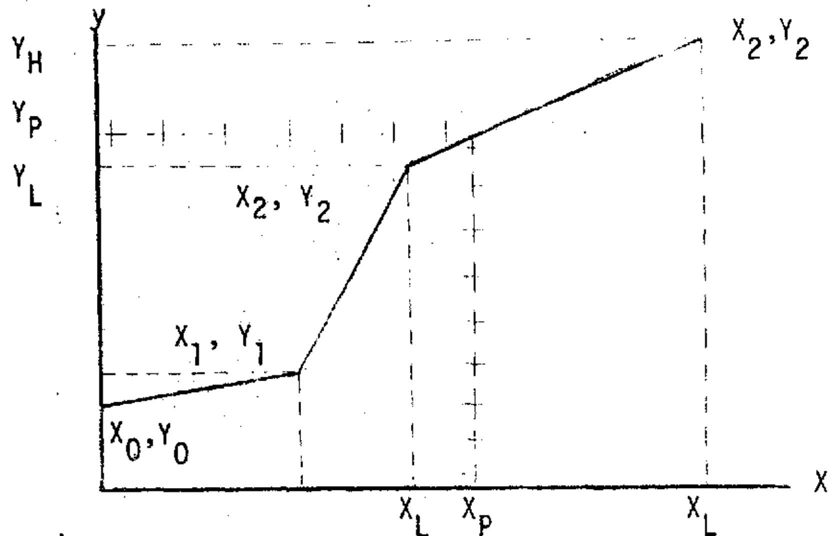
The conversion is done by a linear interpolation between two points, for linear equations these are the end points. Equations that are not linear are broken into segments. Each of these segments are considered to be linear.

Let X be used to represent raw data (bit counts) and Y, the converted values (engineering units). If X_p is the current value to be converted, then the resultant output is Y_p. The two stored end points are found (X_H and X_L) such that $X_H > X_p > X_L$ and also, the values Y_H and Y_L that corresponds to $Y_H = f(X_H)$ and $Y_L = f(X_L)$.

$X_H = Y_H$

$X_p = Y_p$

$X_L = Y_L$



Then by standard ratio:

$$\frac{X_p - X_L}{X_H - X_L} = \frac{Y_p - Y_L}{Y_H - Y_L}$$

and solving for Y_p

$$Y_p = \frac{X_p - X_L}{X_H - X_L} \cdot (Y_H - Y_L) + Y_L$$

4.5.3 Output - The converted BCD values are stored sequentially in the output area along with the subroutine identification number.

<u>Data Format</u>

Subroutine No.
No. Word
BCD Sign $(\pm)$
First BCD Digit
Second BCD Digit
Third BCD Digit
Fourth BCD Digit

4.6 Special Conditions

1. Data Scaling - The calibration data will be an integer scaled to represent an Engineering unit value that corresponds to a X value as shown on the input data format. The range of the calibration data is ± 9999, negative numbers are in two complement form.

C.5.0 OPERATING SYSTEM

5.1 Identification

Operation System Requirements

5.2 Purpose

The operating system will be designed to call resident test subroutines that evaluate the CPU capabilities.

5.3 Program Requirements

The operating system will consist of the following modules: a *minimum* Supervisor, Resident Test Subroutines, Job Dispatcher, and Data Exchange Routine.

5.3.1 Supervisor

A minimum interface to the operating system is required to initiate I/O and respond to interrupts. The supervisor will also contain a self-loading loader that can be initiated by the hardware IPL procedure. The IPL will load all modules including test routines to be made resident during a run. After IPL has been accomplished, the supervisor will initialize all functions necessary to begin operation. It will then pass control to the Data Exchange routine to read in job and parameter data to make a resident job list (RJL) in main storage.

5.3.2 Resident Test Subroutines

The computer will have "n" resident test subroutines which are callable by a job number from the Resident Job List (RJL) by the Job Dispatcher. The following is a list of subroutines and assigned call numbers:

Call Number	Subroutine
01	Interrupt Reaction
02	I/O Codes I/O Work
03	Memory Test (Read, Write)
04	Arithmetic Test
05	Address Modifications
06	Complex Instructions
07	Computational Program (High CPU Utility)
08	Time class of instructions
09	Matrix Program
10	Housekeeping (Logical ability), (Bit manipulation)
11	I/O, DMA, Efficiency
12	Memory Exerciser (bit creep, speed)
13	Engineering Units conversion
14	Math Routines
15	Round Robin evaluation
16	Concurrent jobs (13, 14, 15, 11)

5.3.3 Job Dispatcher

This routine calls the test routines based on the RJL generated by the supervisor. It interprets job numbers to the test subroutine as a call for execution, and provides a pointer to the data and parameters to be used. Test data can be supplied within the RJL or by use of an I/O function to evaluate concurrent operation.

5.3.4 Data Exchange Routine

This routine provides for data exchanges between the test routine. Functions performed by this routine are:

a. Read in user supplied control cards containing subroutines names and parameters.

b. Convert subroutine name to a test subroutine call number.

c. Provide parameter pointers for test routine.

d. Store response (results) from test routines.

e. Start/Stop flag (interrupts) to trigger CPU into starting on a resident test routine.

5.3.5 Summary Functional Sequence

After IPL has been completed, the supervisor reads in control statements and generates a Resident Job List that is used when a start processing command is issued. Resident Test Subroutines are called based on data contained in this list. Data is transferred to/from the CPU by the Data Exchange Routine.

5.4 Detailed Functional Requirements

5.4.1 Data Input

The supervisor generates the Resident Test List (RTL) making an entry for each control statement. The RTL format is shown in Figure 1.

5.4.2 Data Processing

When a start processing command is issued, the CPU's control is transferred from the supervisor to the Job Dispatcher Routine (JDR). The start command causes the Job Dispatcher Routine (JDR) to call a Resident Test Subroutine (RTS) based on the call number contained in the list.

As the RTS completes a job, it has the Data Exchange Routine (DER) place the results along with an identification number (RTS call number) in an output area. The JDR continues calling RTS until a delimiter is encountered at which time the CPU sets the stop flag. Each time the DER is called to place results in the output area, a mark flag is set so that steps in a test may be timed.

No. of Bytes/Entry Subroutine Call no. Concurrency Flag Parameter 1 " 2 " " N
No. of Bytes/Entry Subroutines call no. concurrency flag Parameter 1 " 2 " " N
No. Parameter N
End of List Flag

One Entry

Entry

FIGURE 1. FORMAT OF RESIDENT JOB LIST

The concurrency flag if set indicates that the next job in the RTL is to be executed along with the current job. Usually this should be an I/O operation or a mutually exclusive job that can be cone in parallel. An example of a concurrent operation would be an I/O operation flagged as concurrent and for example, an Engineering units subroutine responding to data supplied by the I/O operation. A fixed number "n" Engineering units jobs could be done for each I/O operation.

5.4.3 Data Output

The Data Exchange Routine (DER) is used to place results in an output list as shown in Figure 2. Each time a result is placed in this list a mark flag is set by the DER. The mark flag can be used to time intermediate results or verify concurrent operations.

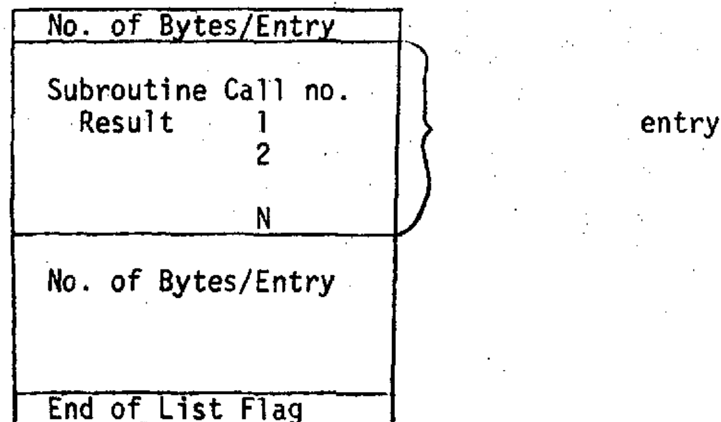


FIGURE 2. FORMAT OF RESPONSE LIST

APPENDIX D

CYCLE RATIO TEST METHOD

(Suggested Method for Determining I/O and DMA Speeds)

CYCLE RATIO TEST METHOD

Suggested Method for Determining I/O and DMA Speeds

A. INTRODUCTION

This method is suggested as a means of determining I/O and DMA speeds of a test article, without varying input data frequency from the tester, (Unified Test Equipment (UTE)).

1.0 CYCLE RATIO TEST METHOD ADVANTAGES

- The rate at which the UTE outputs commands and data does not have to be supplied at high speeds
- The UTE command and data rate does not have to be variable
- There is no requirement for special hardware to generate data words at high cycling rates

2.0 ASSUMPTIONS

- UTE data output (parallel word) rate can be operated at speeds which are some fraction of the slowest expected test article interface rate
- The UTE data rate can be maintained accurately and is known
- New data can be supplied to the UTE - test article interface at the same time data is being read from the interface by the test article

B. INTERFACING CONCEPT

One design configuration that will meet design requirements for feeding data to the test article for the Cycle Ratio Test appears in Figure 1.

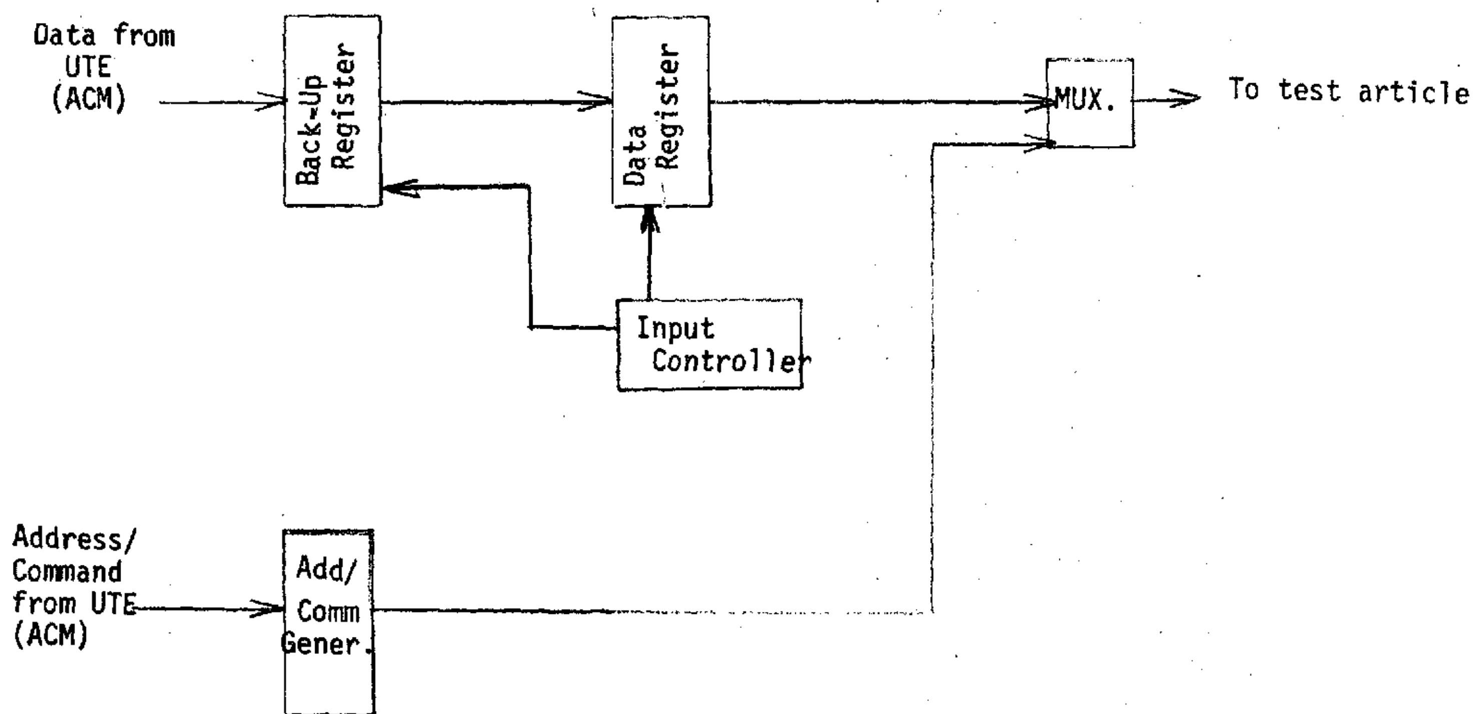


FIGURE 1. INTERFACE CONFIGURATION

1.0 System Concept

When the UTE is ready to supply new data, it will be stored immediately in the Back-Up Register. As soon as the test article has finished reading a data word from the Data Register, the Input Controller will strobe the new data from the Data Back-Up Register to the Data Register.

This assures that new data can be supplied to the UTE- Test article interface at the same time data is being read from the interface by the test article. This requirement is necessary if both the UTE and Test Article are allowed to cycle independent of one another.

The address/Command Generator is needed to generate new address locations for the data word read in each test article I/O or DMA cycle and is controlled by the test article time cycle.

2.0 Cycle Timing

Figure 2 shows a typical cycle timing sequence. The UTE is being cycled at a slower rate than is the test article. Note that the LOAD DATA REGISTER pulse does occur after the first trailing edge of a test article cycle following the trailing edge of a UTE cycle.

The numbers within the test article positive pulse indicates a typical word which is transferred to the test article during that I/O or DMA cycle. A change in number indicates a word content change.

Within each UTE cycle envelope (T) the number of test article cycles receiving the same data word varies by one and only one integer as shown by the circled numbers in Figure 2. This variance of one integer must always be true if the UTE and test article cycle times remain relatively constant.

C. ANALYSIS

1. If the test article cycles ar a rate P times faster than the UTE cycles, the ratio of the number of test article cycles to the number of UTE

cycles equals P exactly. This only occurs, however, after the number of cycles approaches infinity.

By computing the ratio after a finite number of cycles, an error exists between the true cycle ratio and the computer cycle ratio. This is because there is no way of tracing a part of a cycle and thus the ratio must be expressed as a ratio of integers. An expression for maximum error was derived to insure a known accuracy of a ratio computed after a finite number of cycles. The expression predicts an error of about .1% if 1000 test article DMA or I/O cycles are used in the ratio computation.

2. Derivation

The worst case error would be possible if the ratio (P) were to be exact during a UTE cycle previous to the last UTE cycle included in a ratio computation.

Let X = No. of UTE cycles when ratio became exact.

Then, X + 1 = No. of UTE cycles used in ratio computation.

Let Y = No. of UTE cycles recording a high integer number of test article cycles.

X + 1 - Y = No. of UTE cycles recording low integer number of test article cycles.

W = Actual low integer number of test article cycles.

W + 1 = Actual high integer number of test article cycles.

Z = Exact ratio of test article cycles to UTE cycles

Let N = No. of test article cycles completed within the (X+1) cycles.

Z(X + 1) is the number of test article cycles that should appear in (X + 1) UTE cycles.

This can be a non-integer number, thus:

$Z\ (X + 1) = N + d$ where N = number of test article cycles
d is a number between -1 and 1

As the value $Z\ (X + 1)$ can be a non-integer, and N must be an integer number of cycles; a fraction d must be added to N to make the equality $Z\ (X+1) = N + d$. Maximum error will occur when the value of d approaches +1 or -1. In such a case, the value of N is one full integer away from making the calculated ratio $\frac{N}{X+1}$ approach Z.

Thus for worst error

$$Z\ (X+1) = N \pm 1$$

2.1 Low Integer # of Test Cycles

If the last envelope (T) at X+1, contained a low integer number of test article cycles, then worst error case would be

$$Z\ (X+1) = N + 1$$

The true average Z can be expressed

$$Z = \frac{Y(W+1) + (X-Y)(W)}{X} \qquad (1)$$

The apparent average A can be expressed

$$A = \frac{Y(W+1) + (X+1 - Y)(W)}{X + 1} \qquad (2)$$

This apparent average will be lower than the true average by an error of:

$$E/100 = \frac{Z-A}{Z} \qquad (3)$$

Subtracting (1) and (2) into equation (3).

$$E/100\ Z = \frac{Y(W+1) + (X-Y)W}{X} - \frac{Y(W+1) + (X+1=Y)W}{X + 1}$$

$$E/100\ Z = \frac{YW + Y + XW - YW}{X} - \frac{YW + Y\ XW + W - YW}{X + 1}$$

$$E/100\ Z = W + Y/X - W - \frac{Y}{X+1} = \frac{Y}{X} - \frac{Y}{X+1} = \frac{XY + Y - XY}{X(X+1)}$$

$$E/100\ Z = \frac{Y}{X(X+1)}$$

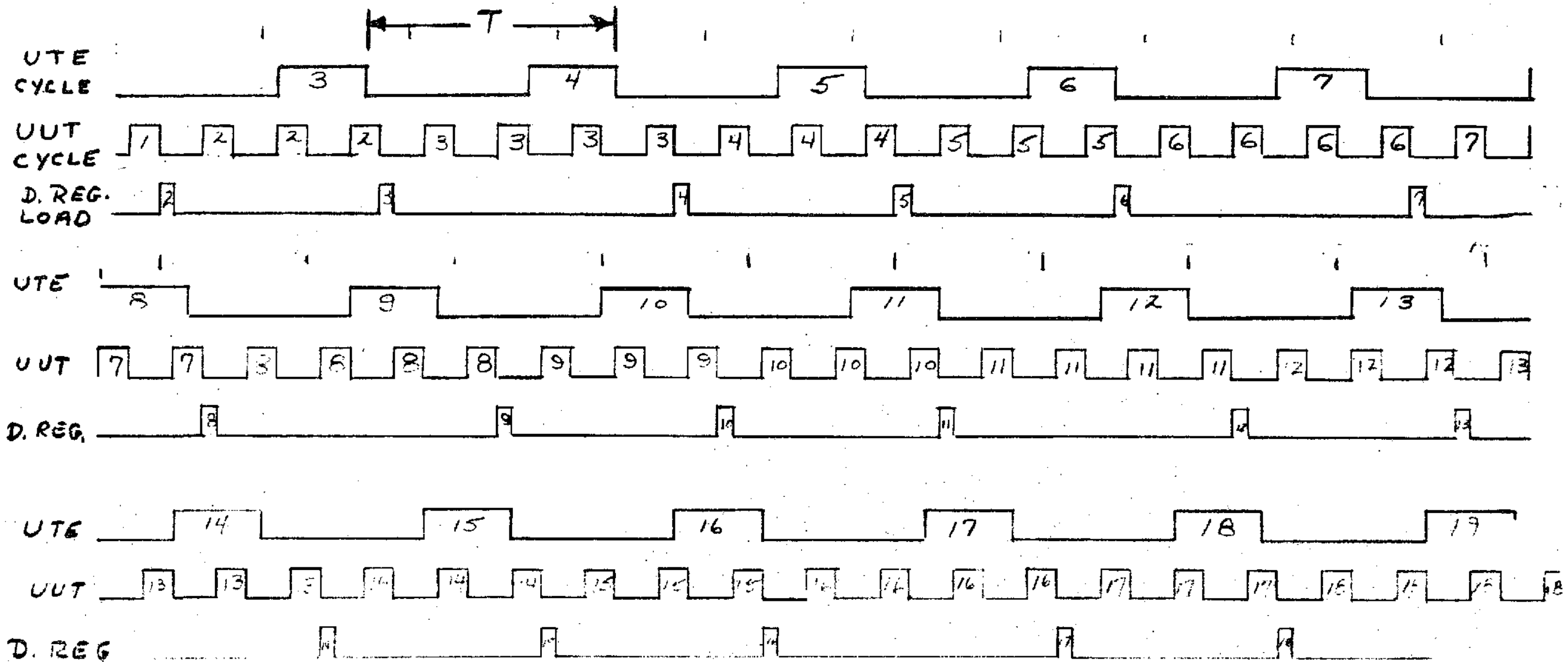


FIGURE 2 CYCLE TIMING

T = ENVELOPE WIDTH IS FALLING EDGE OF ONE UTE CYCLE TO THE FALLING EDGE OF THE NEXT

$$E/100 = \frac{Y}{X[(X+1)Z]}$$

but $(X+1)Z = N+1$

Therefore $E/100 = \frac{Y}{X(N+1)}$

The highest value Y/X can reach is 1, thus the largest error in this case is:

$$E/100 = \frac{1}{N+1} \tag{4}$$

and, A can be lower than the true ratio by $\frac{Z}{N+1}$ at most.

2.2 High Integer # of Test Cycles

If the last envelope T at X+1, contained a high number of test article cycles, then the worst case error would be

$A(X+1) = N - 1$

The true average Z can be expressed

$$Z_H = \frac{(Y-1)(N+1) + (X+1-Y)(W)}{X} \tag{5}$$

The apparent average A_H can be expressed

$$A_H = A = \frac{Y(W+1) + (X+1-Y)W}{X+1} \tag{6}$$

This apparent average will be higher than the true average by an error of:

$$E_H/100 = \frac{A-Z}{Z} \tag{7}$$

Substituting (5) and (6) into equation (7):

$$E_H/100Z = \frac{Y(W+1) + (X+1 - Y)W}{X+1} - \frac{(Y-1)(W+1) + (X+1-Y)(W)}{X}$$

$$E_H/100\ Z = \frac{YW + Y + XW + W - YW}{X + 1} - \frac{YW + Y - W - 1 + WX + W - YW}{X}$$

$$E_H/100\ Z = \frac{Y}{X+1} + W - W - \frac{Y-1}{X} = \frac{XY - XY + X - Y + 1}{X(X+1)}$$

$$E_H/100 = \frac{(X+1 - Y)}{X\ [Z(X+1)]}$$

but $Z(X+1) = N-1$

Therefore $E_H/100 = \frac{(X+1-Y)}{X(N-1)}$

$(X+1-Y)$ is the number of low integer UTE cycles, so if the last integer was high, the largest value of $\frac{X+1-Y}{X}$ (worst case error) is 1.

Thus the largest error in this case is:

$$E_H/100 = \frac{1}{N-1} \tag{8}$$

and A can be higher than the true ratio by $\frac{Z}{N-1}$ at most.

Thus:

$$Z - \frac{Z}{N-1} \leq A \leq Z + \frac{Z}{N+1} \tag{9}$$

Thus a computed cycle ratio would have a maximum error of about .1% by using 1000 test article DMA or I/O cycles, as $E_H = 100 \frac{1}{N-1} \approx 100 \frac{1}{N} = .1\%$ max. error.

D. SIMULATED CYCLE RATIO EXAMPLES

A computer program was written to show the errors possible in using the Cycle Ratio Test.

The computer ratio may depend not only on the number of cycles involved but also upon how the test article and UTE cycles were synchronized during the test. Thus the ratio computed when the UTE and test article cycles start simultaneously (Delta Offset = 0) may be different than the ratio computed when the two cycles do not begin simultaneously.

Delta offset is the part of a test article cycle between the beginning of the first UTE cycle and the first test article cycle.

For each Delta Offset, four values are printed:

1. UUT cycles indicates the number of test article cycles used in completing the cycle Ratio Test.
2. UTE cycles indicate the number of UTE cycles used in completing the Cycle Ratio Test.
3. Ave indicates the cycle ratio $\left(A = \frac{\#UUT\ cycles}{\#UTE\ cycles}\right)$ which should approach the actual ratio (Z).
4. % Error is the percent error of the cycle ratio (Ave.) to actual ratio (Z) thus % error = $100^* \frac{Z-A}{Z}$.

Inputs to the program are:

1. The number of test article cycles. The program may use extra test article cycles to complete the last UTE cycle.
2. The actual ratio of UTE cycle length/test article cycle length.

If N is the number of test article cycles, maximum error can occur if (1) $\frac{N-1}{ratio}$ is slightly less than an integer (2) $\frac{N+1}{ratio}$ is slightly greater than an integer.

Case (1) is true because a possibility exists of getting an extra test article cycle under an ideal condition causing the computed A to be larger than the actual ratio. The error should be $100\left(\frac{1}{N-1}\right)$

1.0 Simulated Low Integer # of Cycles

As an example let N = 10

$\frac{N-1}{ratio}$ is slightly less than an integer (I)

Let I = 8

Thus ratio is slightly greater than $\frac{N-1}{8} = \frac{9}{9} = 1.125$

Thus let ratio = 1.125001

The ratio A should have a max error of $\frac{100}{9}$ = 11.1111% and A should be larger than the actual ratio by this error margin.

Figure 3 is a computer run of the above mentioned ratios illustrating error at a point near N-1.

B= NO. OF UUT CYCLES
Y= UTE CYCLE LENGTH / UUT CYCLE LENGTH
B=
?10
UUT CYCLE TIME TEST FOR 10 SAMPLES
Y=
?1.125001
RATIO= 1.125001

DELTA OFFSET	UUT CYCLES	UTE CYCLES	AVE	% ERROR
0	10	8	1.25	-11.11101
.05	11	9	1.222222	-8.641878
.1	11	9	1.222222	-8.641878
.15	10	9	1.111111	1.234656
.2	10	9	1.111111	1.234656
.25	10	9	1.111111	1.234656
.3	10	9	1.111111	1.234656
.35	10	9	1.111111	1.234656
.4	10	9	1.111111	1.234656
.45	10	9	1.111111	1.234656
.5	10	9	1.111111	1.234656
.55	10	9	1.111111	1.234656
.6	10	9	1.111111	1.234656
.65	10	9	1.111111	1.234656
.7	10	9	1.111111	1.234656
.75	10	9	1.111111	1.234656
.8	10	9	1.111111	1.234656
.85	10	9	1.111111	1.234656
.9	10	9	1.111111	1.234656
.95	10	9	1.111111	1.234656
.9999999	10	9	1.111111	1.234656

FIGURE 3 - Computer Run to Illustrate Error at N-1

MM GE RECOMM GE RECOMM GE

2.0 High Integer Number of Test Cycles

Case (2) is true because a possibility exists of getting one less test article cycle under ideal conditions causing the computed A to be samller than the actual ratio. The error should be 100 $\left(\frac{1}{N + 1}\right)$

Using the same example as above

$N = 10$

$\frac{N + 1}{ratio}$ is slightly greater than I

Thus the ratio is slightly less than $\frac{N+1}{8} = \frac{11}{8} = 1.3750$

Thus let ratio = 1.374999

The ratio A should have a max error of $\frac{1}{11}$ = 9.0909%. and A should be smaller than the actual ratio by the error margin.

Figure 4 is a computer run of the above mentioned ratios illustrating error at a point near N + 1.

AM GE RECOMM GE RECOMM GE RE

```
B= NO. OF UUT CYCLES
  Y= UTE CYCLE LENGTH / UUT CYCLE LENGTH
B=
?10
  UUT CYCLE TIME TEST FOR   10 SAMPLES
Y=
?1.374999
    RATIO=  1.374999
```

DELTA OFFSET	UUT CYCLES	UTE CYCLES	AVE	% ERROR
0	10	7	1.428571	-3.896179
.05	10	7	1.428571	-3.896179
.1	10	7	1.428571	-3.896179
.15	10	7	1.428571	-3.896179
.2	10	7	1.42851	-3.896179
.25	10	7	1.428571	-3.896179
.3	10	7	1.428571	-3.896179
.35	10	7	1.428571	-3.896179
.4	10	7	1.428571	-3.896179
.45	10	7	1.428571	-3.896179
.5	10	7	1.428571	-3.896179
.55	10	7	1.428571	-3.896179
.6	10	7	1.428571	-3.896179
.65	11	8	1.375	-7.26093E-05
.7	11	8	1.375	-7.26093E-05
.75	11	8	1.375	-7.26093E-05
.8	11	8	1.375	-7.26093E-05
.85	11	8	1.375	-7.26093E-05
.9	11	8	1.375	-7.26093E-05
.95	11	8	1.375	-7.26093E-05
.9999999	10	8	1.25	9.090843

FIGURE 4. Computer Run to Illustrate Error at N + 1.

APPENDIX E

UTE HARDWARE DESCRIPTION

This appendix contains brief descriptions of the required UTE hardware modules necessary to perform UCTS functions.

Section A - Display and Control Modules

Section B - Acquisition and Command Module

Section C - Data Recording Module

Section D - Hard Copy Module

Section E - Data Display Module

Section F - Mass Memory Module

Section G - Program Preparation Peripherals

A. DISPLAY AND CONTROL MODULE (DCM)

The Display and Control Module is contained in a single console designed for use by one operator.

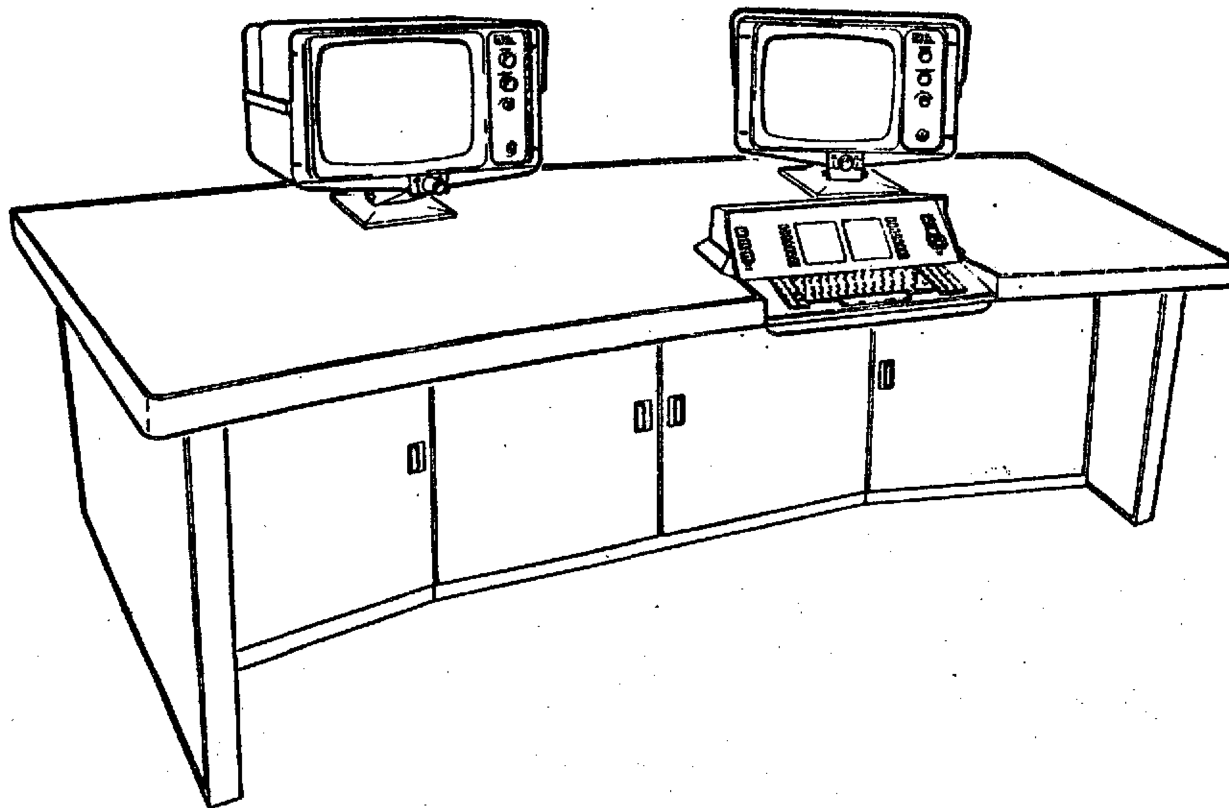
The Console appearance is similar to an executive office desk with 2 CRT's and a keyboard mounted on work surface as shown in Figure A-1. The DCM is a stand-alone unit mounted on casters with overall dimensions of 108" x 44" deep x 45" high.

The DCM consists of all elements shown in the block diagram in Figure A-2 plus power supplies.

Operator's entry is via a keyboard containing 16 variable-function keys, 15 special fixed-function keys, 10 control and editing keys, and a set of typewriter keys containing 32 graphic symbols in shifted mode. A legend display consisting of up to 10 alphanumeric characters can be programmed for each of the variable function keys.

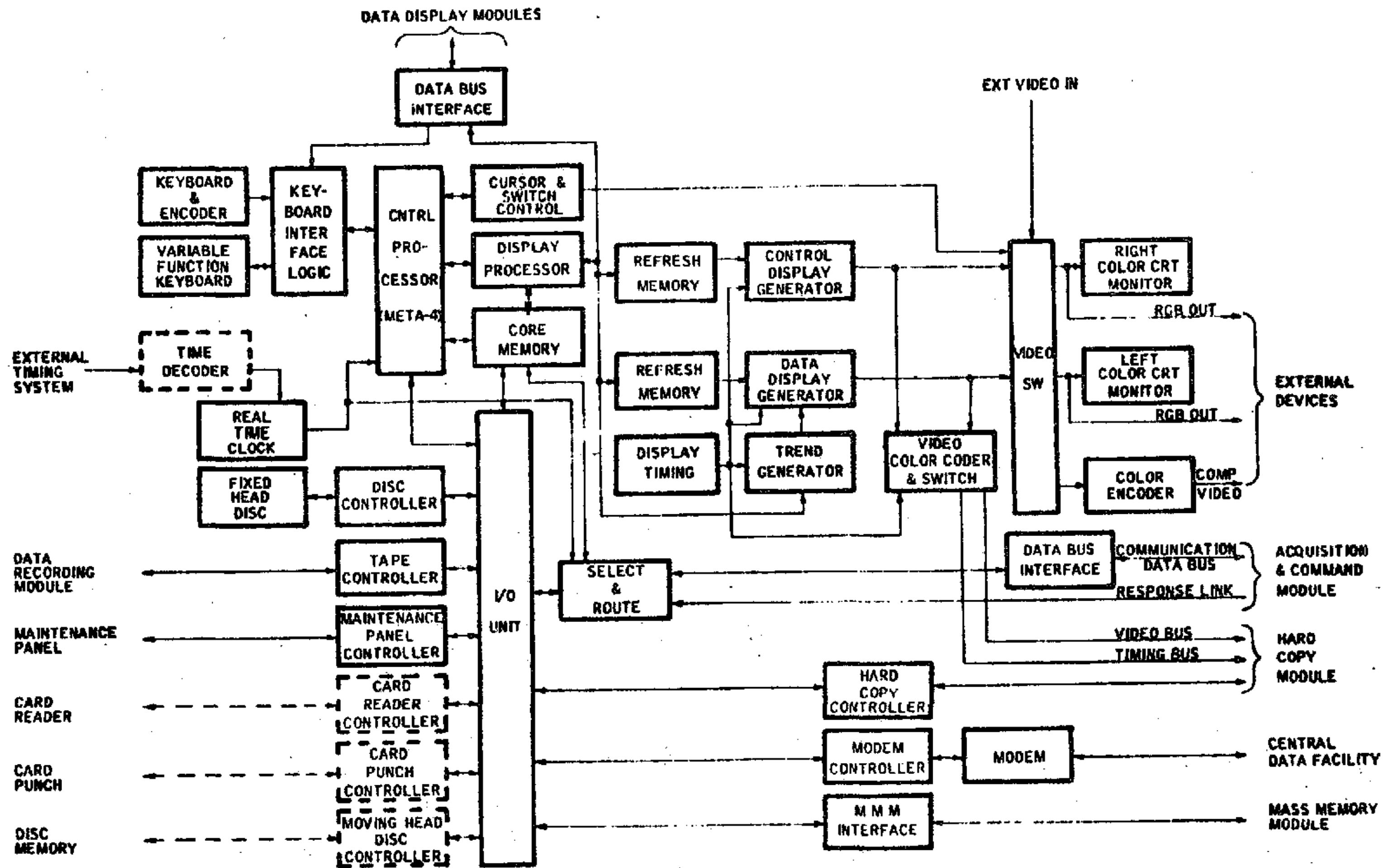
Two color TV Monitors (CRT's) are used for all information display. The Control Display (right CRT) provides alphanumeric, status, and event symbology plus a cursor. The Data Display (left CRT) provides alphanumeric, status, event meter bar, special graphics and trend symbology.

A repertoire of 64 alphanumeric characters can be displayed with up to 52 characters per line and 25 lines per page. Status or event data can be displayed with up to 5 annotated-patches per line. The meter-bar symbol including annotation and representation of the analog parameter state can be displayed on up to 25 lines. Up to 3 trend curves can be presented simultaneously with 256 points per curve and 128 possible levels for each point. 32 Special-graphic symbols can be used to construct pictorial diagrams. Color can be combined with all of the symbology to highlight



DISPLAY AND CONTROL MODULE

FIGURE A-1



DISPLAY AND CONTROL MODULE
BLOCK DIAGRAM
FIGURE A-2

significant characteristics such as data out-of-tolerance, change-of-state, or feature discrimination.

All parametric processing, for the two CRT's and up to 6 external Data Display Modules (DDM's), is performed by the Display Processor. The Display Processor transfers the processed data to a separate refresh memory associated with each display.

A Data Bus Interface provides 2-way communications with each of the DDM's.

The Control Processor performs overall executive control, data state determination, data-dependent operations, variable computation, sequential operations, file-management operations, display callup, program loading, recovery operation, and self-test functions. The Control processor is a 16-bit general-purpose machine with a 4K modifiable-ROM microprogram memory and an instruction cycle of less than 100 nanoseconds.

Primary Memory consists of 32K 16-bit words of core in 4 banks. Each bank has 4 ports and all banks can be simultaneously accessed. Secondary memory consists of a Fixed Head Disc with 374K 16-bit-word capacity.

An I/O unit provides both party-line I/O and direct-memory access for external device controllers in addition to the internal Fixed Head Disc and the Select & Route.

A real-time clock derives time in millisecs through days from the 60-cycle power line. Time is displayed to the operator on the control display.

Each DCM receives data from the Acquisition and Control Module (ACM) via the common 32-bit parallel response link. This data is sent to the Select & Route circuit for time-tagging and storage in core memory. In addition, critical data may be received from ACM via the serial data bus and the data bus I/F. The serial data bus, which is common to each DCM and ACM is also

used by the Select & Route when transferring program and command information to the ACM.

DCM controls the operation of the Hard Copy Module when a DCM or Data Display Module (DDM) operator requests hard copy of his display. DCM services the requests as received, stops updating the designated display, provides commands to switch coded-video on to the video bus, and controls printing.

A Mass Memory Interface is provided for transfer of information to and from the Mass Memory Module.

The Tape Controller provides for the transfer of data to and from the Data Recording Module. In addition, the Tape Controller provides for the control and sequencing of up to 4 tape drives.

A Card Reader Controller, a Card Punch Controller, and a Moving Head Disc Controller provide control of optional software preparation devices.

A Maintenance Panel Controller permits an external panel to be used in performing extensive H/W & S/W troubleshooting.

DCM will accept monochrome composite video for display on the left CRT. In addition, it will output a color composite video from either the Control or Data Display and RGB video is available from both displays.

Self-test features permit on-line detection of error and allow failure isolation to the line replaceable item.

Provisions for mounting facility intercom systems are included.

B. ACQUISITION AND COMMAND MODULE (ACM)

The Acquisition and Command Module performs data processing and command formatting and provides the primary interface with the test area.

All elements shown in block diagram in Figure B-1 plus power supplies are contained in two (2) standard cabinets with the following dimensions: 48" wide x 30" deep x 72" high.

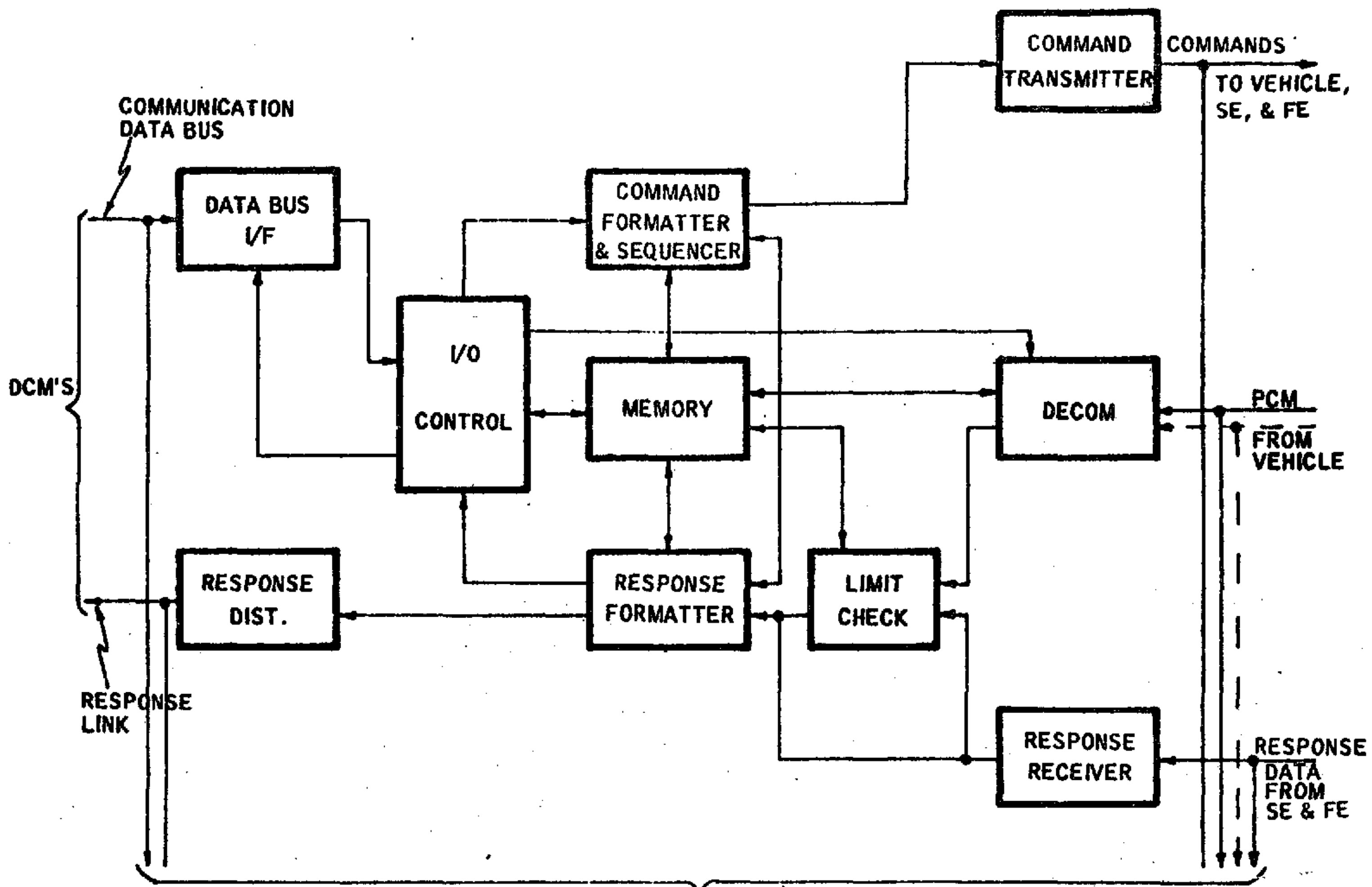
Communications, critical data, and program data are transferred between DCM and ACM via the communication data bus. All response data required for display, processing, or recording is sent to all DCM's via the open-ended parallel response link.

The Command Formatter & Sequencer is a special-purpose processor which can generate multiple command sequences with word length up to 32 bits and at a rate up to 40K-words/sec. The CFS can measure time intervals in 1-millisec increments. The CFS can request the Response Formatter to indicate receipt of selected measurements.

The Command Transmitter contains a parallel-to-serial converter, error-code generation, and line drivers for interface with the facility long-line transmission system.

Memory will be addressable to 65K words and will consist of multiported, independently accessible banks capable of being configured to provide dedicated portions of memory to the Decom, Limit Check, and Response Formatter. The memory has the capability of read-modify-write on a single access.

The Decom will accept PCM data words from the orbiter vehicle. It will tag measurements with a 16-bit identifier and the PCM format is programmable. The Decom will accept a redundant PCM input and automatically switch lines to recover from loss-of-synchronism due to a transmission error.



ALTERNATE ACM

ACQUISITION AND COMMAND MODULE

BLOCK DIAGRAM

FIGURE B-1

The Limit Checker accepts data up to 16 bits in length and performs fixed and floating-limit tests on the upper 8 bits. Four floating-limit apertures are selectable: 1, 2, 4 and 8 counts for 8-bit words (4, 8, 16 and 32 for 10-bit words). One of five states is determined by the fixed-limit test. Only non-redundant data is sent to the Response Formatter.

The Response Formatter is a special-purpose processor which reformats and tags data for DCM processing and recording. It can handle 32-bit words (16-bit data & 16-bit address) at rates up to 400K words/sec.

An alternate ACM can be operated in parallel in a passive-monitoring mode with the Response Link open. State-of-health is continually determined by both ACM's and reported to the Master DCM. When failure of the primary ACM is detected by the Master DCM, theoperator can initiate switchover and recovery on the alternate ACM.

Self-test features of the ACM permit a failure to be isolated to a Line Replaceable Unit.

C. DATA RECORDING MODULE (DRM)

The Data Recording Module provides the capability to store and retrieve data on magnetic tape. Two 1/2" Magnetic-Tape Drives are enclosed in a cabinet which is 24" wide x 30" deep x 72" high.

Each tape drive permits data to be recorded on 9 tracks (including parity) using 1600-cpi phase encoded or 900-cpi NRZI format. Automatic threading and vacuum columns reduce tape wear and maintenance. Use of 10 1/2" reels permits approximately 40 x 10^6 8-bit bytes of storage per tape at 1600 cpi. A tape speed of 125 ips results in a maximum recording rate of 200K-bytes/sec (8 bits + parity).

D. HARD COPY MODULE (HCM)

The Hard Copy Module provides high-contrast, permanent-copy paper output in three forms: CRT-image copy, line printer, and graphics.

The HCM containing printer, printer logic, paper cutter, and power supplies is contained in a console-type enclosure with dimensions: 27" wide x 32" deep x 30" high.

Copy is electrostatically reproduced in a dot-matrix format 10" wide on a 11" page width with programmable page length. Paper is automatically collated and made available for front access with printout rates up to one 8-1/2" x 11" page per second or 4800 lines per minute.

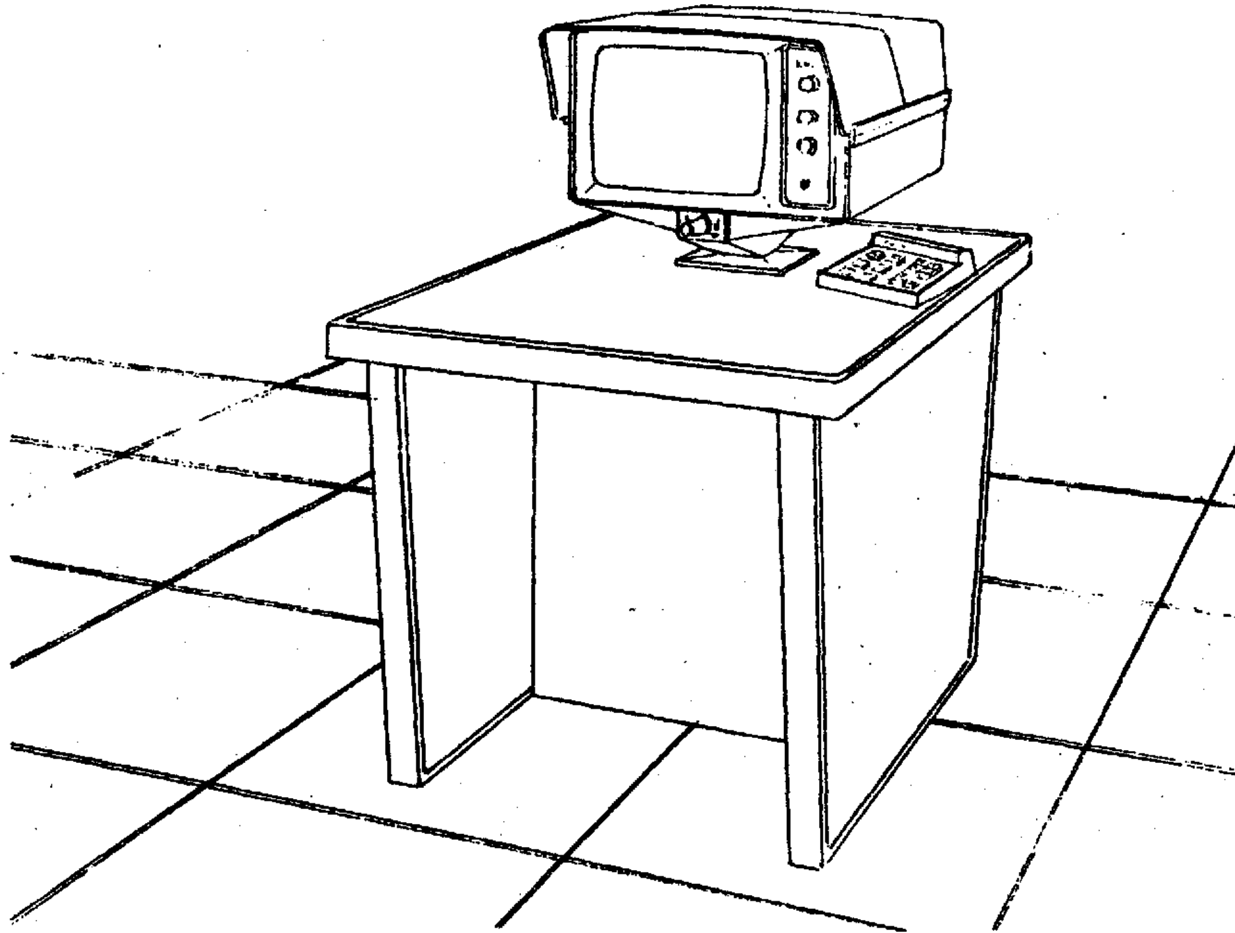
With a print resolution of 80-dots per inch the HCM contains sufficient buffering to convers 525 line TV (interlaced) scan rate to the print rate. In line-printer mode the alphanumeric format is 132 characters per line. In graphics mode each dot is printed selectively.

E. DATA DISPLAY MODULE (DDM)

The Data Display Module provides operator selection and display of all pages available within the host DCM.

The DDM which is shown in Figure E-1 is 24" wide x 30" deep x 45" high (including table). All elements shown in the block diagram in Figure E-2 plus power supplies are contained in the single enclosure which is mounted on casters for easy movement.

Page selection is performed using 10 fixed-function keys containing numerals 0 - 9. In addition, the keyboard contains keys for control functions such as: "hard-copy", "execute," "external-video," "backup," and "power-on/off". Any pages which can be displayed on DCM can also be displayed



DATA DISPLAY MODULE

FIGURE E-1

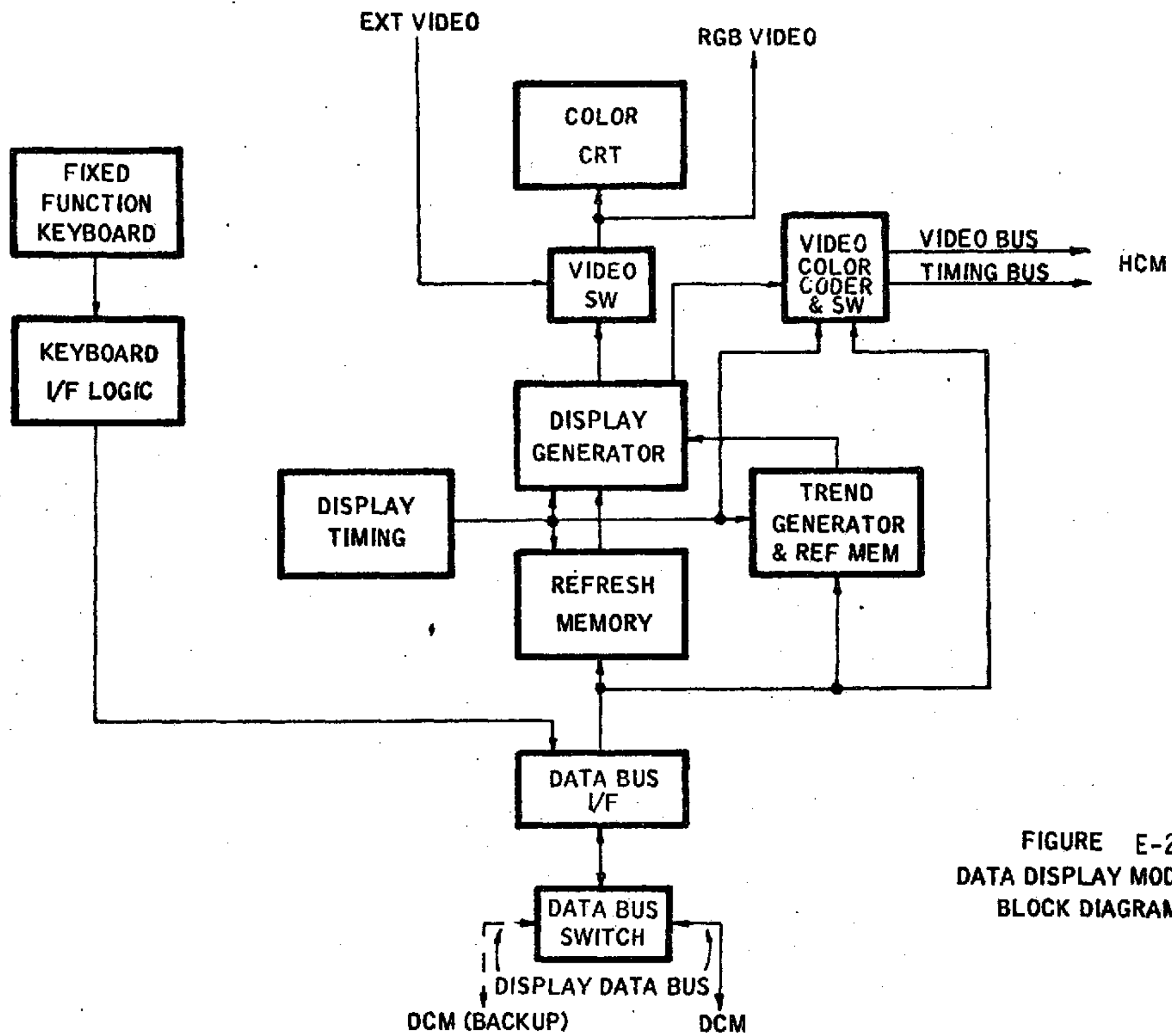


FIGURE E-2
DATA DISPLAY MODULE
BLOCK DIAGRAM

on a DDM. Communication and display data are transferred between DDM and DCM using a data bus. A Data Bus Switch permits the DDM to be readily connected to the backup DCM.

DDM contains a data-bus interface, refresh memory, trend generator, display generator, display timing, and color CRT interchangeable with that used in DCM.

A video switch enables DDM to accept monochrome composite-video for display. The video color coder and switch provides hard-copy compatible video and timing to the video and timing bus in response to an operator request via DCM control.

Provision for mounting facility intercom unit is provided.

F. MASS MEMORY MODULE (MMM)

The Mass Memory Module provides a shared-program and data-storage function for a UTE station.

The MMM, which consists of the elements shown in block diagram in Figure F1 is 30" wide x 30" deep x 72" high (approximately).

A moving-head disc drive which accepts a removable disc pack (IBM 2316 compatible) is used. The disc pack contains 11 discs with 20 surfaces usable. One disc pack provides 29 x 10^6 16-words of storage with a peak access rate of 156 K-words/sec.

DCM interface control provides switching andpriority requests for up to 8 DCM's. The disc-drive controller maintains head location and control for the disc drive.

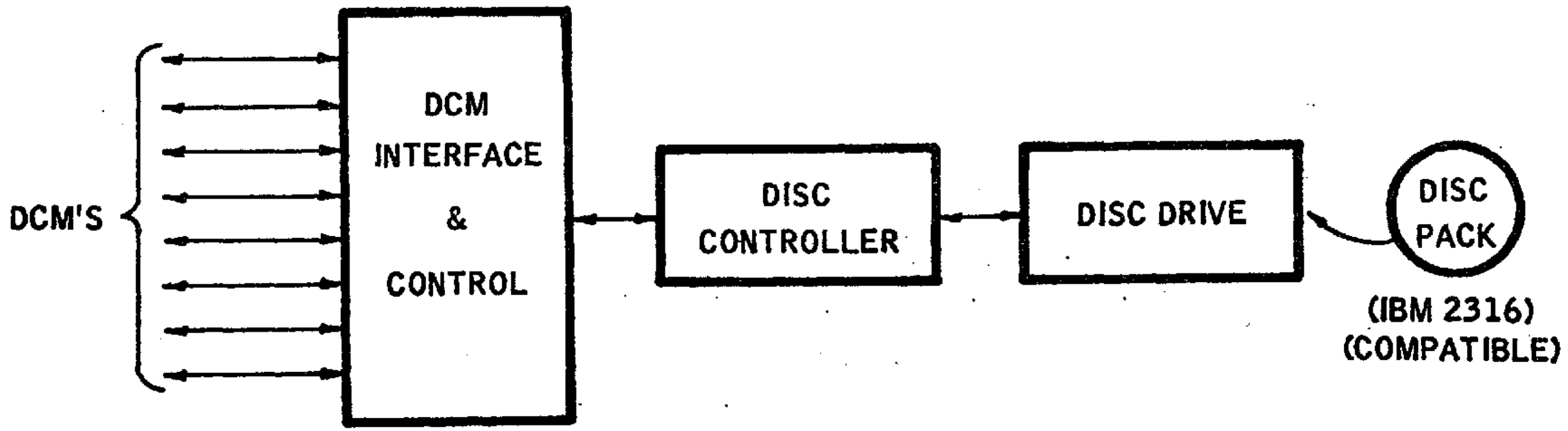


FIGURE F-1
MASS MEMORY MODULE
BLOCK DIAGRAM

G. PROGRAM PREPARATION PERIPHERALS

The following devices are used in the preparation of test programs:

(a) Disc Memory - provides for storage of up to 512 K 16-bit words on single removable disc. This unit is contained in a cabinet which is 24" wide x 30" deep x 72" high.

(b) Card Reader - permits standard 80-column cards to be input at rates up to 1000 cards per minute. The Card Reader is 24" wide x 30" deep x 45" high including a table.

(c) Card Punch - permits standard 80-column cards to be punched automatically under DCM control at rates up to 90 cards per minute. The card punch is 44" wide x 30" deep x 45" high.

APPENDIX F

UTE SOFTWARE DESCRIPTION

This appendix consists of three major sections concerning UTE Software.

Section A - Software Modules implemented in UTE.

Section B - Brief Description of UTE Test Language

Section C - Program Preparation and Verification of UTE Test Software

APPENDIX F

SECTION A. SOFTWARE MODULES IMPLEMENTED IN UTE

1.0 INTRODUCTION

UTE software consists of seven subsystems which operate under control of an overall system supervisor.

These subsystems are oriented toward the major functional areas of job control, file management, test-language compilation, test operations, and UTE self evaluation.

Overall system supervision is provided by the Basic Operating System Supervisor, or BOSS.

Since BOSS provides functions common to all subsystems, it is discussed first in the following description.

2.0 BASIC OPERATING SYSTEM SUPERVISOR (BOSS)

The BOSS provides executive control for time-shared multi-program operation; resource allocation for memory management; and a consistent software environment through interfaces for display control and processing, operator communication and peripheral Input/Output (I/O) control.

2.1 Executive Controls

Executive Control provides task scheduling by priority assignments. The types of scheduling available are as follows:

- Schedule execution at a specified time. The time base may be real (e.g., time-of-day or GMT) or relative (e.g., elapsed test time or countdown time).

2.1 EXECUTIVE CONTROLS (continued)

- Schedule execution after specified time delay. The time delay is specified in minutes, seconds and milliseconds.
- Schedule execution on receipt of specified responses.
- Schedule execution on an available time basis.

2.2 MEMORY MANAGEMENT

Memory management controls the transfer of programs, parameters, and test sequences from the console disc to core memory. There are three basic categories of core memory utilization:

- Basic load programs consisting of those system-supervision functions which require permanent core residency.
- Alternate resident programs which comprise the subsystem in use.
- Non-resident programs such as Load and Execute programs, test sequences, remote-device programs, or data-in-transit.

2.3 OPERATOR INTERFACES

The Operator interface provides the means for operator control of the UTE system activity.

Commands received via the fixed and variable-function keys are decoded and routed to (i.e., cause execution of) the assigned software functions.

Variable-function key assignments are dynamically specified by the subsystem in use.

Fixed-function keys are assigned to subprograms within the operator interface to provide control of display formats, trned generation, hard copy control, etc.

Also included is the interface to provide communication with the operator in a tutorial (question-answer) mode for obtaining variable information.

2.4 DISPLAY CONTROL AND PROCESSING

The subprograms comprising this program provide the interfaces for selecting display-page formats and the subsequent processing of data for display.

Processing capability includes the following display processors:

- Decimal-display analog values in engineering units
- Alphanumeric display of event states
- Scaling of analog values to meter-bar displays
- Coloring status or event patches as a function of the state of a variable
- Coloring graphics displays as a function of the state of the variable
- Scaling variables for display on a trend plot

2.5 I/O CONTROL

I/O Control consists of subprograms, one for each peripheral oevice, which provide a standard software interface for all other system software.

3.0 JOB CONTROL SUBSYSTEM (JCS)

Job control allows operator selection of: the subsystem, the activity within that subsystem, and any further sub-selection until the desired level of operation is obtained.

3.1 DECISION TREES

Selections are made using the variable keyboard. The initial selection will display function names analogous to the available software subsystems. (Since the user can specify the variable-function-key annotation, more meaningful names may be substituted for the subsystem names.)

Selection of a subsystem may, if applicable, cause the selection of activities (or programs) within that subsystem to be displayed. This process may be repeated for successive levels of decision, thus affecting a "Decision-Tree" of access.

3.2 OPERATOR IDENTIFICATIONS

The user may specify "Operator-ID" codes, which will be used to implement access security. This code is then applied as a "key", which in turn restricts the selections presented by the decision-tree.

Thus, the user may restrict access to any desired level.

3.3 UTILIZATION LOG

Job Control activity is recorded in the utilization log on the console disc. Entries into this log may be made by other subsystems. The capability is provided to present this information in the form of a utilization report.

The following, as a minimum, will be logged:

- Operator-identification and time.
- Decision-Tree Selections
- Self-evaluation activities and results
- Operator sign-off

4.0 FILE MANAGEMENT SUBSYSTEM (FMS)

The File Management Subsystem allows the operator to create, copy, edit, and manipulate files in the DCM. It also contains the interface with the Central Data Facility (CDF) and the Mass Memory Module (MMM). Thus, these two devices may be used as the source or the destination of the above files.

Subsets of the File Management Subsystem are available to other software subsystems to provide interfaces to the CDF and MMM.

4.1 DISC UTILIZATION

This is a special stand-alone program required to build a console disc from scratch. The Disc Initialization Program loads the disc from scratch. The Disc Initialization Programs loads the disc with basic BOSS resident load, (i.e., the program load on execution of an Initial Program load (IPL), the file-management programs, and those I/O routines necessary to complete the disc building).

The remainder of the files are then loaded to the disc by the file-management programs from the systems peripherals, including the CDF and MMM.

4.2 FILE MANIPULATION

Programs are provided which include, but are not limited to, the following functions:

- Addition of a file to the console disc from any source, including CDF, MMM, and Core Memory
- Replacement of a file on the console disc with a file from any source as above.
- Deletion of a file on the console disc with a file from any source as above
- Copy a file from the console disc to any destination, including CDF, MMM, and Core Memory
- Editing of test files, which includes addition, deletion, or insertion of logical records; text editing such as byte-string replacements; field manipulations; sequencing of logical records, with specification of sequence fields, starting value and increment.

4.3 CDF TERMINAL MODE OPERATION

This program provides the optional capability of using the DCM Control Display and Keyboard as a CDF terminal, using the standard Communications Language.

This provides the operator the capability of direct data transfers, between the console disc and the CDF.

5.0 TEST LANGUAGE COMPILER SUBSYSTEM (TLC)

The Test Language Compiler converts Test Language Programs, consisting of test-engineering-oriented statements (source statements), to a loadable-binary format executable by the Test Operating Subsystem.

5.1 INPUT TRANSLATOR

Test language source statements are input from the operator-designated device as character-mode records.

These records are checked for format, syntax, and semantics errors, then translated to an intermediate-binary format acceptable by the Element Compiler.

5.2 ELEMENT COMPILER

The Element Compiler converts the intermediate binary from the Input Translator, to the required series of object instructions that will perform the operations specified by each of the original source statements.

Storage cells are assigned for the variable names defined by the test writer, and references to these cells by the test program are converted to relative addresses.

Data-base information, obtained from the CDF, is used to correlate variable names assigned to real measurements and stimuli.

5.3 OUTPUT TRANSLATOR

The Output Translator completes the conversion by translating the object instructions, generated by the Element Compiler, to the specific instructions required for interpretation by the designated UTE unit.

The resultant binary information is output in the format required by the binary-load programs.

6.0 TEST OPERATING SUBSYSTEM (TOS)

The Test Operating Subsystem provides execution of Test Language Programs to check out a Test Article.

6.1 TEST OPERATING EXECUTIVE

The Test Operating Executive controls execution of Test Language Programs. It is functionally the same as the Test Debug Executive without the operator control of program-execution rate.

6.2 TEST ELEMENT OPERATORS

The element operators are discussed under the Test Language Program Debug Subsystem.

6.3 TEST SUMMARY LOG

The Test Operating Subsystem maintains a Test Summary Log file on the console disc. It will file the Operator-ID, the Test Program Selected, time-of-selection, and time of termination. The rest of the log will be determined by the Test Language Program as specified by the user. Examples of the type of information which may be filed are operator command entries, test bench-marks, test-completion status, and discrepancies.

6.4 PARAMETRIC DATA TAPE

Selected parametric-test-data, as specified by the test writer, will be filed on the Parametric-Data Tape. Data which may be filled includes both measurement and stimuli data plus time.

7.0 UTE SELF EVALUATION SUBSYSTEM (SES)

This subsystem provides on-site fault detection and isolation for UTE hardware. Operator interfaces are oriented to line repair disciplines.

7.1 OPERATIONAL READINESS PROGRAMS

These programs exercise the UTE modules, operationally, to verify system readiness prior to testing. Diagnostic capability is limited to fault detection at the module level.

7.2 MAINTENANCE PROGRAMS

Maintenance programs provide diagnostic testing of UTE modules for acceptance tests, periodic preventative maintenance, and fault isolation for on-site repair.

While the resolution of fault isolation is dependent on module complexity, it may be generally stated as not more than one hierarchical level above the LRI.

7.3 FAULT ISOLATION PROGRAMS

These programs provide fault isolation to the LRI for those modules whose complexity prohibits this resolution by Maintenance programs.

SECTION B. UTE TEST LANGUAGE (BRIEF DESCRIPTION)

1.0 INTRODUCTION

This is an introduction to the Unified Test Equipment Test Language (UTETL) to acquaint the reader with terms of the language. The intent is to help the reader better understand the manner in which the various parts of UTETL fit together.

The UTE Test Language is a compiler level language which gives engineers and other people who are not programmers the ability to generate software in the form of test programs.

2.0 STATEMENT

The smallest entity in the UTETL language is the "statement." A statement is a compiler instruction that causes several machine instructions to be executed. A test program is made up of the logical grouping of statements which perform the required tasks.

2.1 STATEMENT TYPES

UTETL statements are of two types:

- Name statements whose purpose is to establish a name for a parameter, entry point or activity.
- Step statements which perform tasks or describe an activity or part of an activity such as defining the colors associated with the states of a test article.

The reference manual (UTE # 0.5.0.0.7.0) refers to "blocks" which are sets of step statements between name statements. A name statement terminates the preceding block and starts a new one.

3.0 TEST PROGRAMS

A test program is made up of up to four separate sections. Each section performs a separate function and has its own set of allowable statements.

3.1 THE $SPECIFICATION SECTION

The first section, referred to as the $SPECIFICATION (The $ is silent or not silent as the user may choose - the $ added to the term "SPECIFICATION" emphasizes the fact that we are talking about SPECIFICATION section of a UTETL test program), specifies parameters and variables which are referenced in other sections of the test program.

The statements in the $SPECIFICATION section perform the following functions:

1. Assigns names to the following:
   - measurements
   - stimuli
   - computed analog values
   - computed discrete values
   - CRT message fields
2. Links the data base identification with the name assigned by the program.
3. Defines names for the various states associated with measurements, stimuli, computed analog values and computed discrete values.
4. Defines the colors associated with each of the defined states.
5. Defines whether to record significant changes in value or state of measurements and computed analog values and computed discrete states.
6. Provides branching capability based on the value of a computed analog or discrete value.
7. Performs the replacement function (A ← B read A is replaced by B).
8. Defines the number of characters in a message.
9. Allocates core.

3.2 THE $PROCEDURE SECTION

The $PROCEDURE (the $ is handled just like in the $SPECIFICATION as it is in the other two sections of the program) contains the main

program logic. As opposed to the $SPECIFICATION section whose instruction set specifies and describes, the instruction set of the $PROCEDURE section is made up of "executable" instructions which make things happen in the test articles. The $PROCEDURE section is analagous to the "main program" in other compiler languages.

The statements in the $PROCEDURE section perform the following functions:

1. Assigns names to the following: Control loops - groups of control logic
   Entry points - a location within a program which is the destination of a branch or transfer statement.
2. Initiates the execution of a program module, in the associated $TESTS section.
3. Terminates the execution of a program module.
4. Initiates the presentation of a complete page of CRT display information.
5. Links a Variable Function Key (VFK) with a module which executes when the VFK is depressed.
6. Negates a VFK program link.
7. Returns control to the monitor when appropriate.
8. Performs the replace function ($A \leftarrow B$ read A is replaced by B).
9. Provides branching capability based on a real or computed value.
10. Initiates the display of a message on a CRT.
11. Provides a pause in the execution of statements for a specified period of time.
12. Provides an unconditional branch.

3.3 THE $TEST SECTIONS

The $TESTS section statements are used to build small logic segments referred to as "modules". These modules are analogous to subroutines. The modules are caused to execute by being "called" by a statement in the associated $PROCEDURE section. When a module finishes executing it must return control back to the $procedure.

The statements in the $TESTS section perform the following functions:

1. Assigns names to the following:

   Control Loops - groups of control logic
   Entry Points - A location within a program which is the destination of a branch or transfer statement.

2. Stimulates the equipment associated with a test article.
3. Returns control from a module back to the calling program.
4. Performs the replace function (A ← B read A is replaced by B).
5. Provides branching capability based on a real or computed value.
6. Initiates the display of a message on a CRT.
7. Provides a pause in the execution of statements for a specified period of time.
8. Provides an unconditional branch.

3.4 THE $DISPLAY SECTION

The $DISPLAY section is concerned with setting up displays or portions of displays to be utilized by the $PROCEDURE or $TESTS sections of the test program. It should be noted that the $DISPLAY section cannot cause any part of a display to be presented.

The statements in the $DISPLAY section perform the following functions:

1. Assigns a name to a full display page.
2. Defines the parameters associated with the display of meter bars.
3. Defines the parameters associated with the display of event patches.
4. Defines the parameters associated with the display of horizontal and vertical bars.
5. Defines the text of a message.
6. Defines the position on the CRT face for a message.
7. Defines the format and position on the CRT face for display of a measured or computed value.

SECTION C. PROGRAM PREPARATION AND VERIFICATION

1.0 INTRODUCTION

The Program preparation and Verification (PPV) concept provides an economical approach to those activities associated with program preparation, compilation and verification. PPV utilizes system resources available at any UTE Test Station. Therefore, the functions performed achieve a high degree of mobility since any Test Station can be used for PPV. The PPV requires a minimum of on-line support from the Test Stations and is essentially a stand-alone system.

The PPV system provides for an efficient and flexible man-machine interface to perform all the activities necessary for program preparation, compilation, editing, verification, and distribution.

2.0 SYSTEM INTERFACES

The principle inputs to the Program Preparation and Verification system consist of:

- Test Programs from the Test Engineer.
- Test Program Library updates.
- Measurement/Stimuli Data Base Updates.
- Equipment Configuration Data Base from Test Stations.
- Verified Test Program Source, documents and schematics from the DSM.

Outputs from the PPV system include:

- Test Program System Load disc to the Test Station.
- Hard-copy listings to the Test Engineer.
- Updates of verified test Program Library.

. Card or tape copies of Test Program source.

. Verified Test Program source microfilm to DMS.

. Verification diagnostics to the Test Engineer.

3.0 PREPARATION, COMPILATION, EDITING, VERIFICATION & DISTRIBUTION

3.1 PREPARATION

Test programs are prepared for compilation at the PPV system. In preparing a Test Program the Test Engineer must establish the test requirements for the system being tested. He has access to the DSM for a source of verified information. With the aid of the information stored in the DSM, he is able to select verified Test Program Procedure and test sequences for insertion into his Test Program source. The Test Engineer prepares the Test Program source off-line on cards or tape. If the Test Engineer requires Test Programs from the Verified Test Program Library, he can obtain copies in card form for manual insertion into his source deck or by the use of the File Management Subsystem he can merge his source with the Test Program Library Source either on tape or in the MMM. The most economical method would be to merge source from card, tape, or disc into the Test Program source file on the MMM.

3.2 COMPILATION

Prior to compilation, the Test Language Compiler is brought into the main memory of the backup DCM from its fixed-head disc. The TLC is written in Fortran IV to assure machine independence. Any changes to the Test Language Compiler assumes the existence of a higher-level compiler (Fortran IV) resident on disc at the PPV system (compile the TL Compiler).

All inputs to the TL Compiler reside in the MMM. The Measurement/ Stimulus Data Base is updated perioically. The most current Test Station Equipment Data Base must be transferred to or updated at the PPV system. TL Compiler object (unverified) is stored in the MMM in the TP System Load file.

The contents of the TP System Load file consists of:

- Procedure Name and Status
- ACM Programs
- UTE Configuration Table
- Symbolic Reference Table
- Procedure Sequences
- Test Sequences
- Expanded TP Source Representation

The expanded TP source is listed on the PPV Hard Copy Module at compile time. The Test Engineer uses the TP listing for a first level of verification of TP syntax and semantics.

3.3 Editing

The Test Engineer reviews the compile-time errors and edits the Test Program from the backup DCM operators console. With the aid of the File Management Subsystem he is able to make insertions, corrections, and deletions to the expanded TP source representation stored in the unverified TP System Load File. In order for the Test Engineer to verify the TP display-pages and variable-function keys, he must initialize the unverified TP System Load into the backup DCM. Once he has verified the page format he can request a hard copy from the HCM. After all major revisions of the TP Source are made, the Test Engineer can recompile before proceeding into the final verification phase.

3.4 VERIFICATION

There are several levels of verification of Test Programs:

- TLP Compiler Level
- TP Logic Level
- Simulation and verification of Procedure and Test Sequences in the Test Operational Mode.

Verification at the first two levels is accomplished during the compile and edit phases. The final level of verification requires a minimum reconfiguration of the Test Station resources.

APPENDIX G

This appendix contains three sections covering the subject of prime power testing of digital equipment.

Section A. Testing D.C. Prime Power

Section B. Testing A.C. Prime Power

Section C. Commercially Available Test Equipment.

SECTION A - TESTING SYSTEMS REQUIRING D.C. PRIME POWER

1.0 INTRODUCTION

The following discussion relates to testing being done on Aerospace equipment being produced at the Aerospace Electronic Systems Department of the General Electric Company. Figure G-1 shows typical D.C. test circuitry.

2.0 TESTS PERFORMED

The following tests are performed to assure the quality of the test article. The failure of any of the following tests will be interpreted as a test article failure and necessary corrective action shall be taken.

2.1 High Voltage Test

A high voltage test is conducted (nominal voltage plus 10%) over a wide temperature. A failure of the test article to operate according to specification at any temperature will initiate test article corrective action.

2.2 Low Voltage Test

A low voltage test is conducted (nominal voltage minus 10%). The procedure and results are handled in a similar manner to that of 2.1.

2.3 Power Interrupt

A power interrupt test is conducted during the high and low voltage tests and at various temperatures. The test article must operate through a .5 second power interrupt at either high or low voltage. This test is implemented by single pulse interrupt and a

long waiting period before another and a burst of pulses up to 50% duty cycle.

A power interrupt of longer duration is also implemented to assure that the test article will properly shut down if power is interrupted for periods longer than 1 second. This test is also implemented with single and multiple interrupt bursts.

2.4 Transient Testing

Transient testing is done on various pulse width and amplitudes dependent upon the customer's specifications. The implementation includes a set of power switching devices which are controlled by programmable logic. The relays switch out the nominal prime power and switch in the transient amplitude for a controlled amount of time. The nominal power is then switched back to the test article. A typical power transient waveform is shown in Figure G-2.

It is noted in Figure G-2 that during the relay operating time the power goes toward ground. This is desirable in that it simulates the actual vehicle conditions.

SECTION B - TESTING SYSTEMS REQUIRING A.C. PRIME POWER

1.0 INTRODUCTION

Systems requiring A.C. power sources are tested similarly to the D.C. systems shown in Section A of this appendix. There are also additional tests performed.

2.0 ADDITIONAL TESTS

2.1 Frequency Variation Tests

The supply frequency is varied plus or minus 10% from nominal at room temperature only to assure that the input isolation transformer is wound correctly.

2.2 The sine wave distortion test is performed but only in the engineering laboratory to promote a design which will accept "bad" aircraft waveforms.

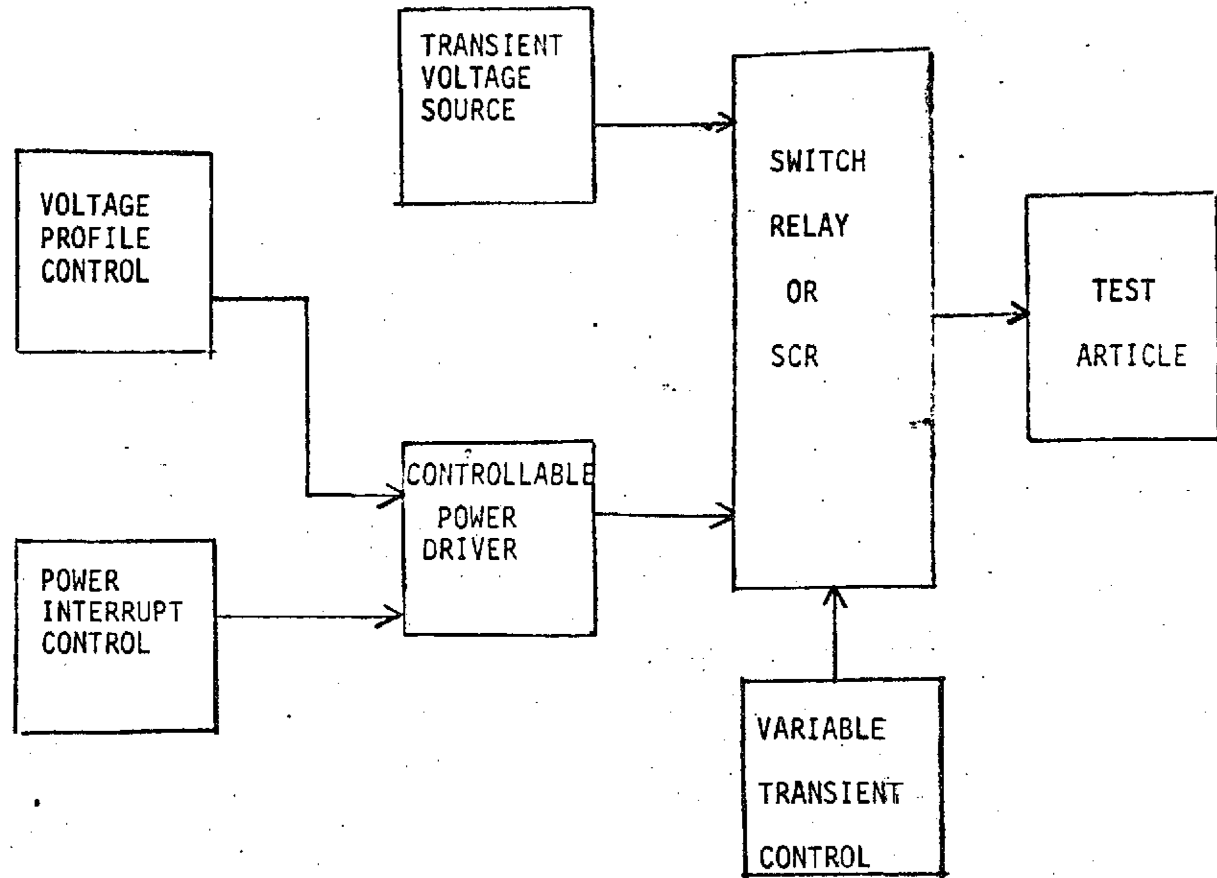
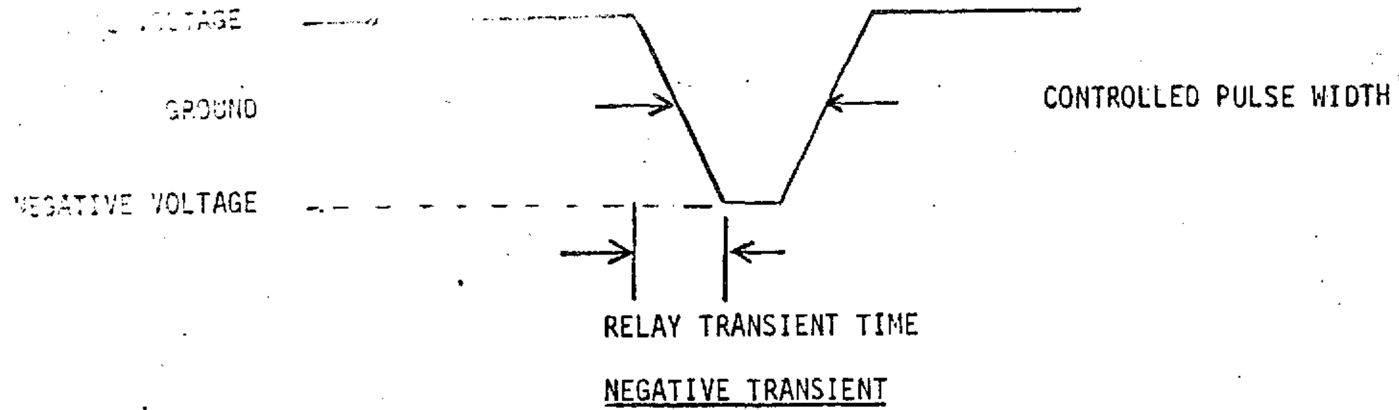


FIGURE G-1. TYPICAL D.C. POWER TEST CIRCUITRY



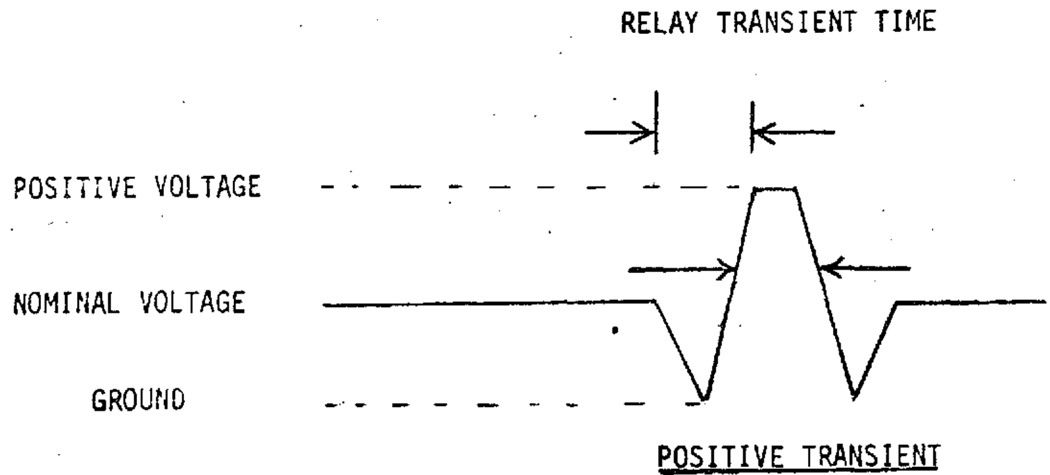


FIGURE G-2. POWER TRANSIENT WAVEFORMS

SECTION C - COMMERCIALLY AVAILABLE TEST EQUIPMENT

The following is a reproduction of commercially available typical A.C. test equipment.

The General Electric Company is by no means promoting the company shown, but rather, is showing the literature as a typical example of A.C. power test equipment which is commercially available.

ELGAR MODEL TG-704A
TRANSIENT GENERATOR OSCILLATOR MODULE

MODELS:			
	TG-704A-1	(single phase)	$1,995.00
	TG-704A-1D	(single phase with harmonic distortion)	$2,145.00
	TG-704A-3	(three phase)	$2,245.00
	TG-704A-3D	(three phase with harmonic distortion)	$2,495.00

SPECIFICATIONS:

OUTPUTS

FREQUENCY

RANGE (steady state)	300-500Hz, resolution 1Hz, and 45-70Hz, resolution 0.1Hz, push-button select
TRANSIENT MAGNITUDE	±100Hz max, (300-500Hz range) resolution 1Hz, and ±10Hz max, (45-70Hz) resolution 0.1Hz
TRANSIENT DURATION	0.015 - 15.0 seconds adjustable in 3 ranges
TRANSIENT RESPONSE	Double exponential filtered, [illegible]ms time constant

VOLTAGE (at output of associated power amplifier)

RANGE (steady state)	55-205 VRMS line to neutral, resolution 0.5 VRMS
CONFIGURATION	3-phase 4 wire wye, or single phase
TRANSIENT MAGNITUDE	±80 VRMS max, continuously adjustable, resolution 1 volt
TRANSIENT RESPONSE	Rise time less than 100 microseconds
TRANSIENT DURATION	0.015 - 15.0 seconds adjustable in 3 ranges
AMPLITUDE MODULATION	0-100% (requires external low frequency signal of 0-3 VRMS at rear panel BNC connector)
DROPOUT DURATION	0.015 - 15 seconds adjustable in 3 ranges
WAVEFORM	A. NORMAL - sine wave, less than 1% THD B. DISTORTED - (peaked or flattened waveform) 8% THD (Optional)

NOTE: Analog voltages directly proportional to voltages and frequency outputs available on MS connector on rear of instrument. Remote initiate inputs for both frequency and voltage transients also available in same MS connector.

INPUT	115 VRMS ±10% less than 100VA, 47-70Hz
SIZE	3½" H x 19" W x 16½" D (standard RETMA rack panel)
WEIGHT	20 pounds

(May 25, 1972)

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TG-704A-3D	(three phase with harmonic distortion)	$2,495.00

SPECIFICATIONS:

OUTPUTS

FREQUENCY

RANGE (steady state)	300-500Hz, resolution 1Hz, and 45-70Hz, resolution 0.1Hz, push-button select
TRANSIENT MAGNITUDE	±10CHz max, (300-500Hz range) resolution 1Hz, and ±10Hz max, (45-70Hz) resolution 0.1Hz
TRANSIENT DURATION	0.015 - 15.0 seconds adjustable in 3 ranges
TRANSIENT RESPONSE	Double exponential filtered, 33ms time constant

VOLTAGE (at output of associated power amplifier)

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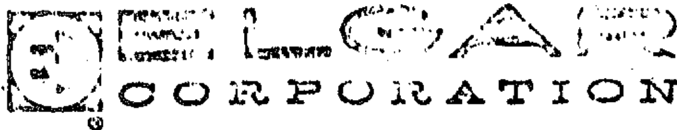

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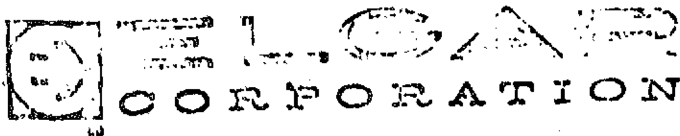

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(May 25, 1972)

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ELGAR CORPORATION

PRINCIPLES AND APPLICATIONS OF A.C. POWER SOURCES AND POWER SIMULATION SYSTEMS

1. INTRODUCTION

In 1965 Elgar Corporation was determined to find ways of fulfilling a vital need for highly controllable AC Power. We delivered our first solid state AC Line Conditioner. Since then we've developed AC Power Sources and Frequency Changers and UPS no-break AC power systems. . . and there's more to come. We're specialists in solutions to sophisticated AC power problems . . . that's our only business. Elgar products are playing vital roles in major defense programs as well as many unique applications in industry.

What we do is provide instruments that make it possible to obtain the kind of AC power needed by our customers . . . from conventional power lines. How we do it is described on the following pages. See for yourself.

2. THE NATURE OF AC LOADS

Before a discussion of Elgar's capabilities, we should be familiar with certain basic definitions relative to loads, power factor and VA which must be considered before the proper Elgar power source can be selected.

All AC loads can be classified as being resistive, capacitive or inductive. Depending upon which prevails, the amount of power drawn will vary from one load to the next even though the apparent current drain is the same. The difference is due to the power factor associated with different kinds of loads.

Power Factor (P.F.) is the ratio of watts or useful power output to the volt-ampere (VA) output. VA is the product of output volts and amperes and is a measure of the output capacity of a power source. More specifically, a VA rating is the vector sum of the watts and the reactive or useless power output. Thus, for an AC power source to have a meaningful specification, it must state how much current it can deliver to a stated range of P.F.

Power sources are rated on their total VA capability. Therefore, the following will help the power source user in determining what output capability his needs require.

(1) VA = voltage x amperes

Real power is measured in terms of W which is:

(2) W = VA x P.F.

(3) $\text{P.F.} = \dfrac{W}{VA}$

therefore:

(4) $VA = \dfrac{W}{\text{P.F.}}$

The P.F. is unity (1.0) for a pure resistive load and less than unity – either leading or lagging – for all other loads. In selecting power sources it is not sufficient to consider only P.F. Certain kinds of loads must also be considered due to the fact that they exhibit high starting currents or non-linearities.

3. CONSIDERATIONS PECULIAR TO CERTAIN LOADS

Elgar AC power sources are compatible with all types of loads, but some applications require correcting or tuning of the source for proper compatibility. Typical problem loads are as follows:

1. Single-phase motors
2. Synchronous motors
3. Transformers and variacs
4. Constant voltage transformers
5. S.C.R. and magnetic amplifier power supplies

The problem with these loads stems either from non-linearity in the loads or from high inrush currents required for their operation.

Almost all motors take 5 to 10 times full load current during starting. This type of load needs to be coordinated with other loads if the KVA rating of the source is to be compatible with the inrush current requirement, or provision must be made to start the motor from the line and then transfer over to the power source.

Single-phase motors of the capacitance-start type employing a built-in starting switch can cause voltage pulsations and motor oscillation if any single motorload rating exceeds 25% of the power source VA rating. For special requirements where a larger motor must be driven from the power source, it can be operated from the power line for a short period during starting and then switched to the output of the power source for continuous duty.

Many step-up or step-down transformers such as a variac may saturate and will therefore demand high input current. This characteristic is usually referred to as non-linearity and will in most cases cause a momentary overload of the power source. As a result, the power source will current limit and increase the harmonic content in the output of the source. In extreme cases it could cause the output voltage to go into oscillation. When large transformers are to be used on the output of the power source or line conditioners, it is recommended that these be of a design compatible with source characteristics or that the proper source be selected to be compatible with the transformer characteristics.

Loads that go into saturation in any portion of the operating range of input voltage, current or frequency are classed as non-linear loads. Typical of these loads are ferroresonant regulating transformers. Constant voltage transformers (CVT's) should be eliminated from power source loads wherever possible. Since the power source provides precisely regulated voltage, the need for a CVT is eliminated.

SCR and mag-amp power supplies employ phase-delayed switching which draws power from the AC source over only a portion of each cycle. This tends to increase the total harmonic distortion of the output waveform, and in some cases can cause voltage pulsations. If such a supply is less than 20 - 25% of the AC source rating, the output waveshape will generally be acceptable.

4. HOW TO DETERMINE TOTAL VA

The total VA load may consist of one or more smaller loads. If the load can be measured, the following steps should be taken to determine the total VA:

1. Measure:
   AC voltage with a voltmeter
   AC current with an ammeter
   AC power with a wattmeter
2. Compute:
   KVA and P.F. from formulas (1) & (3)

Inrush currents for loads such as motors can be measured with an ammeter at the instant the load is energized. For loads which have faster decaying inrush currents – such as solenoids, relays, incandescent lamps, transformers and power supplies -- an oscilloscope is required.

If the load cannot be measured, the following can be done. Check the nameplate on the equipment. These will usually give the voltage and either wattage or P.F. data. Knowing this, the previous formulas can again be used to determine the VA, and these may be added together for each of the loads. The average P.F. for dissimilar loads may be calculated by:

$$\text{Average P.F.} = \frac{\text{total W}}{\text{total VA}} \text{ (for all loads)}$$

5. COMBINED LEADING AND LAGGING P.F. LOADS

In some cases, the P.F. of the individual loads comprising the total will vary considerably. Adding the currents together in such a case will result in a current rating that is higher than would actually exist. Under those conditions where there is a combination of leading and lagging power factor loads, this difference can be significant. Therefore, the individual loads should not be added.

In some cases, the volt amperes reactive (VAR) is determined for each load or group of loads which have the same P.F. The following procedure should be followed to determine the total load:

1. Find VA for each load from previous equations.
2. Find W from previous equations.
3. Find VAR where:
   $VAR = VAR \sqrt{1 - (P.F.)^2}$
4. Find total VAR for all lagging P.F. loads and assign a negative sign.
5. Find total VAR for all leading P.F. loads and assign a positive sign.
6. Algebraically add these two totals.
7. The total VA can be found by using the following:
   $\text{Total VA} = \sqrt{W^2 + VAR^2}$
8. Knowing the total VA, the power factor for the load can be determined.

6. ELGAR AC SOURCES . . . SIMPLE & FLEXIBLE

To better understand the principle of Elgar AC power sources, think of them as a high power linear amplifier driven by an oscillator. More specifically, the basic power amplifier actually consists of a DC supply and a multistate amplifier with a multiple tap power output transformer. The output frequency is established by a plug-in oscillator. In simplified form, the power source operates as shown in Figure 1.

Although frequently classed as an instrument, Elgar power sources are actually power systems . . . made possible by their exceptional flexibility. Not only can they deliver a variety of voltages and frequencies at the output, but the phase can be controlled, enabling the user to interconnect the output of two or more power sources into 2-phase and either Delta or Wye, 3-phase configurations. This flexibility carries with it still another important benefit to the user. Since the many possible output variations from the power source are achieved either by a plug-in device or by external interconnection, a given power source — or group of sources — can serve one application today and an entirely different one tomorrow. The advantage, of course, lies in the ability to standardize on one group of equipment . . . confident in the knowledge that alternate equipment purchases will not be required to meet future needs. There is nothing to become obsolete with an Elgar power source.

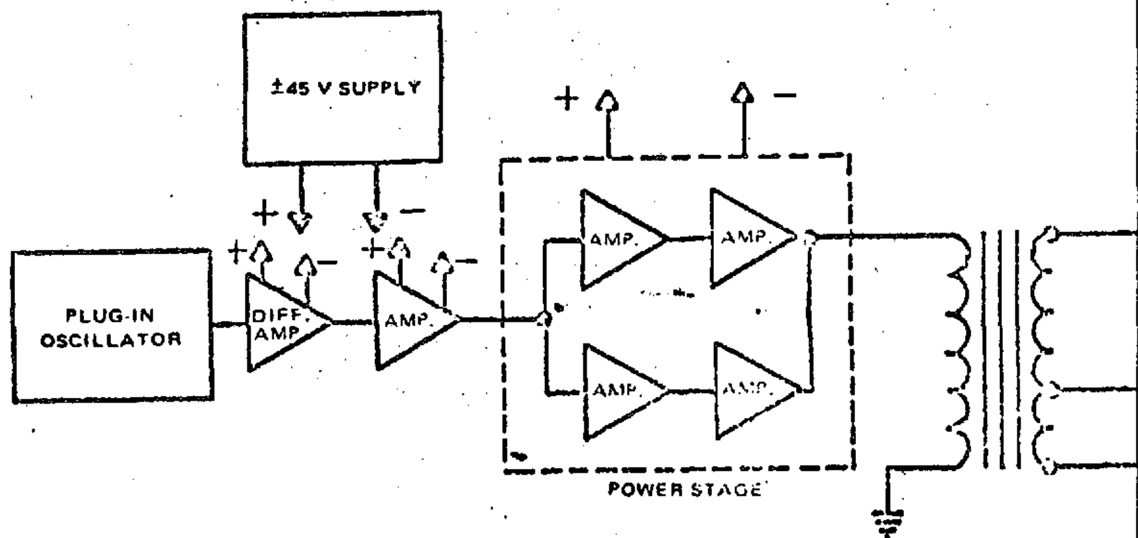


FIGURE 1. — Simplified Power Source Block Diagram

7. THE OUTPUT TRANSFORMER

The output transformer windings of the typical Elgar power source are shown in Figure 2. Each winding has a 32 and 130 volt tap. Within a given source, these two windings may be connected either in series or in parallel, depending upon the voltage output desired. The use of both windings of a given source — whether connected in series or in parallel — is required to achieve the full power output (VA rating). This does not prevent the user from isolating the two windings, however, and drawing one-half power from each for two different purposes.

When two or more power sources are interconnected either to gain greater power, multiple phase operation or for use in a complex system arrangement, the transformer windings from one source to the next must *never* be connected in parallel. Figure 3 shows the interconnection of two power sources capable of delivering a 260 volt output at twice the VA rating of a single unit. To achieve the same capability with a 130 volt output, the interconnection would be as shown in Figure 4. The maximum possible voltage output is derived by interconnecting as shown in Figure 5 and produces 520 volts. Similar techniques are also employed to achieve multiple phase operation. This will be discussed in a subsequent section of this document.

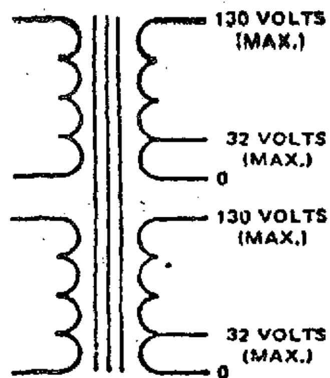


FIGURE 2. – Power Source Output Transformer Voltage Taps

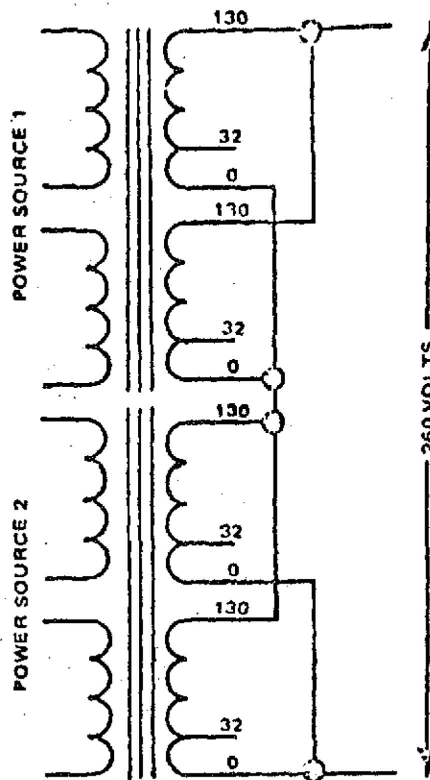


FIGURE 3. – Interconnection of Two Power Sources to Provide 260 Volts at Twice the Power of a Single Unit

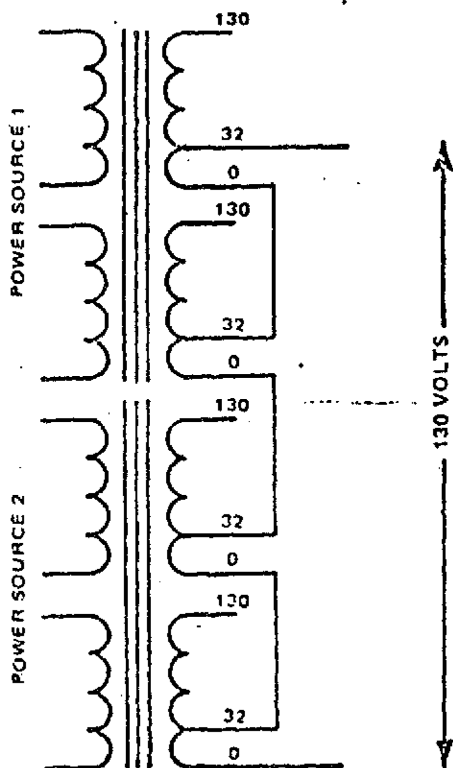


FIGURE 4. – Interconnection of Two Power Sources to Provide [illegible] Volts at Twice the Power of a Single Unit

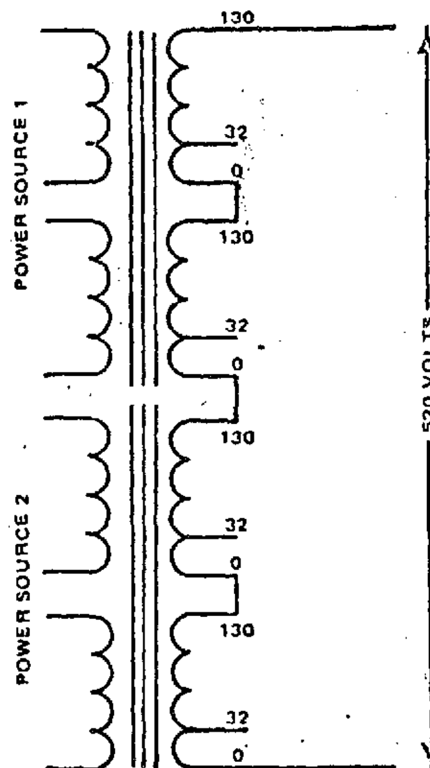


FIGURE 5. – Interconnection of Two Power Sources to Provide 520 Volts

8. FREQUENCY GENERATION TECHNIQUES

The output frequency of the power source is determined by the plug-in oscillator which drives the power amplifier. A variety of interchangeable versions are available, including 45Hz to 10KHz variable; narrow range variable; or fixed frequencies with accuracies to 0.0001%.

Depending upon the accuracy of frequency control desired, either of two methods of frequency generation is utilized. One method employs a modified phase shift oscillator. This technique is used in both the variable and fixed frequency plug-ins since it requires only a change of resistance to produce a change in frequency. External sync capability is also easily added to this group of oscillators. The other method uses a crystal oscillator and is primarily for fixed frequency, highly stable applications. The principle of operation here is to select a fundamental crystal frequency which can be divided down to the required output frequency. By utilizing these two methods of frequency generation, Elgar offers 30 standard plug-in oscillators and has produced many special oscillators as well.

The plug-in oscillator is capable of producing one, two or three-phase output sine waves. The single-phase signal generated within the oscillator is attenuated by the master power source front panel amplitude control. The output of the attenuator is then applied to an A-phase power amplifier and to a signal splitter which develops voltages equal in amplitude and opposite in phase. These signals are then applied to an all-pass phase shift network to form the leading and lagging signals. Control of the amount of lead or lag takes place in the phase-shift network by simply varying resistance in an RC circuit. This resistance variation is then ganged to that required for frequency variation, thereby maintaining a proper phase angle relationship between the two when variable frequency is required. All output signals for a one, two or three-phase configuration are generated in one plug-in oscillator located in the A-Phase power amplifier. It is not necessary to use an oscillator in the power amplifiers used in B and C phases.

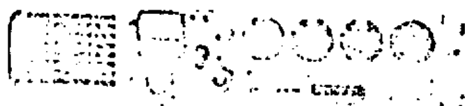
9. VOLTAGE VARIATION TECHNIQUES

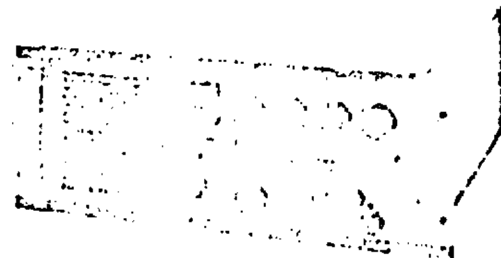
The single or multiple phase oscillator output is adjusted with the amplitude control on the front panel of the master power source. Each of the slave units is independently adjustable if desired. The oscillator produces a signal of approximately 3 volts RMS which will drive the power source to full rated output. A multi-scale front panel meter is permanently wired to one of the 130 volt windings of the output transformer and indicates a full scale reading of 130 volts – regardless of whether the power source output is interconnected for 32, 130 or 260 volts. Thus, the meter reading is multiplied by two for a 260 volt output, and divided by four for a 32 volt output.

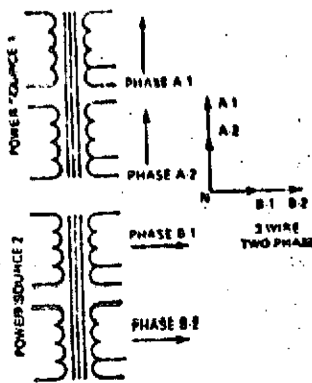
10. MULTIPLE PHASE OPERATION

Elgar AC power sources lend themselves to easy interconnection in a variety of multiple phase configurations. Two power sources may be interconnected for 2-phase or 3-phase operation. Figure 6 shows the phase relationships of the output windings of the two sources, interconnected to produce a 2-phase output. To obtain 3-phase power, the user has the option of interconnecting either two or three power sources. The determination of how many power amplifiers to use depends upon whether a 4-wire Wye or Phantom Wye or 3-wire Open Delta connection is desired. The Phantom Wye and Open Delta configurations utilize two power sources, thereby providing significant cost savings to the user. Although neither of these is a true Wye or Delta, the load cannot tell the difference. Use of the Phantom Wye mode of power source interconnection is limited, however, by the fact that a relatively (within 10%) balanced load is required in order to meet standard Elgar regulation specifications. The vector and output winding diagrams for these two modes of operation are shown in Figures 7 and 8.

A true Wye arrangement necessitates the use of either three power sources or a single unit with three power amplifiers designed to deliver only 3-phase power. The three unit approach is shown in Figure 9. It should be noted that this configuration does not require balanced loading for good regulation.







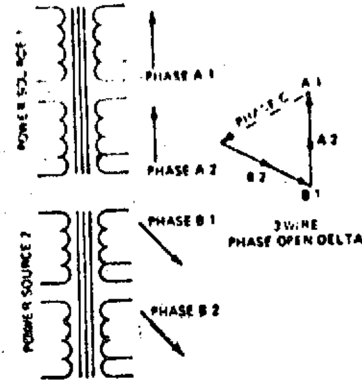
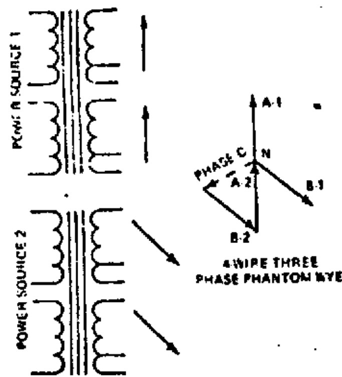


FIGURE 6. – Vector Addition from Two Power Sources Showing Method of Achieving 2-Phase Power

FIGURE 7. – Vector Addition from Two Power Sources Showing Method of Achieving 3-Phase Open Delta



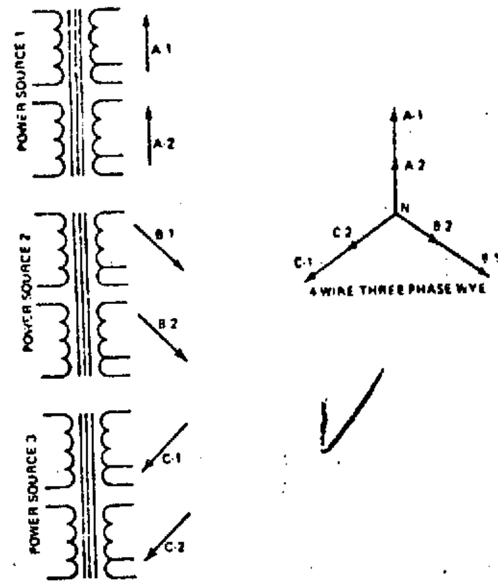


FIGURE 8. – Vector Addition from Two Power Sources Showing Method of Achieving 3-Phase Phantom Wye.

FIGURE 9. – Vector Addition From Three Power Sources Showing Method of Achieving 3-Phase Wye

11. POWER SYSTEM SIMULATORS

Because of the relative ease of control of the output frequency, amplitude and phase, Elgar AC power sources may be externally programmed either by a computer or by other digital commands. This capability enables avionics and other system designers to automatically "exercise" and test their end products under simulated power conditions. This capability has proved valuable for various industrial and commercial product manufacturers who have critical power requirements in the operation or test of their devices.

Elgar has a series of solid state decoder programmers which make possible power system simulation. They are designed for automatic programmed frequency, amplitude or phase angle selection as well as certain combinations of the three. They are available in one, two or three-phase configurations.

The basic decoder programmer accepts parallel BCD inputs in an 8421 code. By selection of options, either a TTL compatible voltage level or contact closure input can be provided. An additional option provides internal storage such that the decoder programmer may be operated in a time-share mode with a computer. The various input signals are then used to control amplitude, frequency or phase for either one, two or three-phase operation. The front panel of the decoder programmer also contains a series of manual controls accompanied by indicator lights. These enable the operator to [illegible] select amplitude, frequency or phase as well as have a visual indication of the programmed conditions, whether [illegible] of the two modes of operation is selectable by a front panel switch.

To protect the unit under test, various safety features are built into the decoder programmer. For example, units containing storage cannot change their programmed conditions until overlapping STROBE and SET commands have been received. This protects against accidental switching from remote to manual operation – thereby inserting an unwanted frequency, amplitude or phase angle condition. An added safety feature takes over in case of a momentary or prolonged power failure. Upon restoration of line voltage, the decoder programmer automatically sets itself for a zero voltage amplitude control and for a 400Hz frequency.

12. A FULL SPECTRUM OF APPLICATIONS

A few representative applications will demonstrate the exceptional flexibility and capability of Elgar power sources.

A somewhat simple application is shown in Figure 10. An Elgar Model 1503, 1500VA 3-phase AC source, was selected as a basis. Specifications called for the ability to program the output voltage amplitude from 0 to 130 volts (line-to-line or line-to-neutral) in 100 millivolt steps. It was also necessary to modulate the output amplitude at a 9Hz rate from 0 to 10% in 1% steps. In addition, it was necessary to program frequency from 45Hz to 5KHz in three ranges of from 45Hz to 100Hz in 0.1Hz steps, from 100Hz to 1KHz in 1Hz steps, and from 1KHz to 5KHz in 10Hz steps. All three of these capabilities were provided by a single Elgar three-phase decoder programmer. A final system requirement necessitated provision for switching the output configuration from Wye to Delta. To insure that the system output voltage agrees with the programmed value, remote sensing is also included at the system output.

A step up in complexity is represented by Figure 11. Because of need for individual control of amplitude for each phase, three Elgar Model 1001's (3000VA, 3-phase AC Source) were used as the basic power system. Amplitude programming of the three phases was handled by three identical decoder programmers which provided independent amplitude control and parallel amplitude modulation control. The range of output voltage variation was from 0 to 130 volts line-to-neutral in 100 millivolt steps. Amplitude modulation varied from 0 to 10% at a frequency of 9Hz. Each of the three decoder programmers could be activated independently of the other by the computer I/O device. In addition, a fourth decoder was provided in order to program the frequency of the system from 45Hz to 5KHz over the same three ranges as in the first application.

Figure 12 represents one of Elgar's more complex systems. The system has two independent modes of operation for the single-phase output which are independent of the three-phase output, plus complete amplitude and frequency control of the three-phase output. The system uses standard Elgar hardware. For the three-phase output, three Elgar Model 251's were selected. Two individually selectable voltage ranges, 0 to 130 and 0 to 260 volts, are provided. Either independent or simultaneous amplitude control of each phase of the three-phase output is also provided. A three-phase decoder programmer provides amplitude programming with 100 millivolt resolution over the selected voltage range plus frequency programming from 45Hz to 5KHz. The frequency resolution is the same as in the previous applications. Phase A is used as a reference phase in the decoder programmer controlling the phase of the single-phase power source. Phase programming is provided in 1° steps from 0 to 360°. The single-phase output is also controlled by a decoder programmer which programs amplitude and frequency with the same resolution as the three-phase output.

Another significant application involves the simulation of the AC power systems found on military aircraft. The performance of these systems is basically defined by Military Standard MIL-STD-704A. Elgar has developed a standard test generator, the Model TG-704A, which will simulate the wide variety of voltage transients, frequency transients, amplitude modulation and various types of harmonic distortion in accordance with MIL-STD-704A. The three-phase output of the TG-704A is used to drive any combinations of standard Elgar AC power sources to provide 115/200 volt, 3-phase 4-wire 400Hz power with the controlled aberrations at a power level determined by Elgar AC power source ratings. This provides for the first time a completely integrated MIL-STD-704A testing system built from readily available standard hardware at a nominal cost.

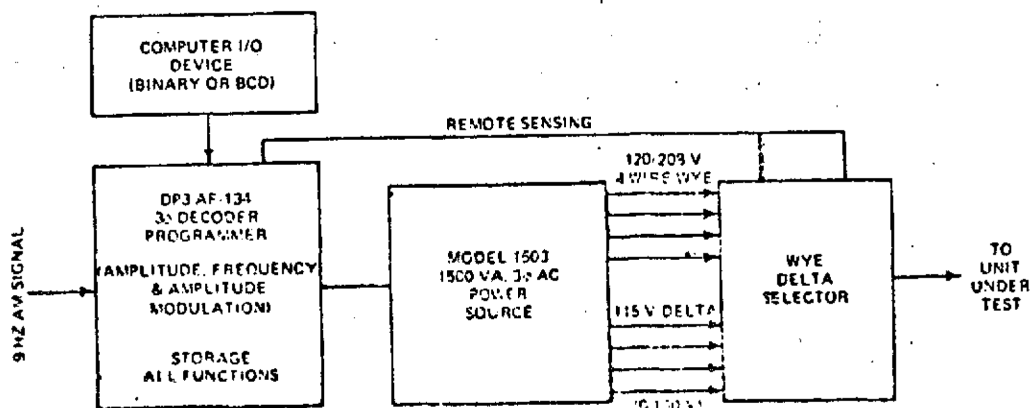


FIGURE 10. – Block Diagram of Simple Power Source System

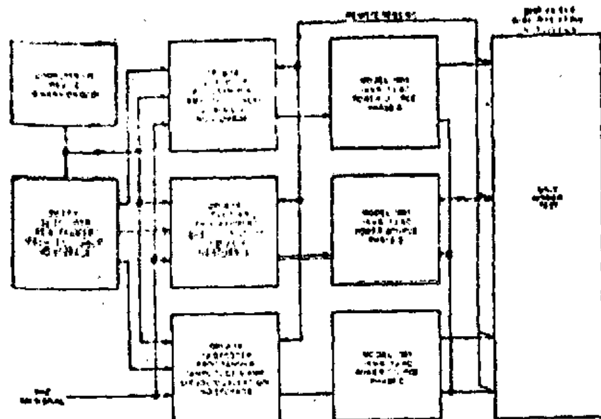


FIGURE 11. – Block Diagram of Multi-Programmer Three-Phase Power Source System

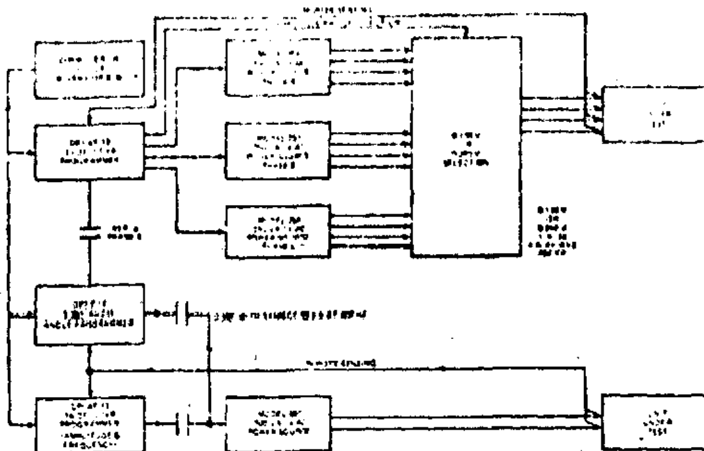


FIGURE 12. – Block Diagram of Complex Multi-programmed Three-phase and Single-phase Power Source System

13. A REPUTATION BUILT ON QUALITY

Elgar Corporation is expert in the control of AC power. That's our only business. We pride ourselves on producing the highest quality product for the lowest possible price. Take one look at any of our products and you'll quickly see a quality of construction that is unsurpassed. Front panels, side rails, top and bottom lids . . . all are fabricated of heavy gage steel . . designed to provide overall rigidity as well as adequate support for the internal components.

When it comes to components – with the exception of the specially designed output transformers – we use only "off-the-shelf" types available from one or more major suppliers. We also take extreme care in every aspect of the utilization of the components . . . including appropriate heat sinks . . . overload protection . . . oversized printed circuit boards . . . right down to the finest detail.

We also take great pride in the reliability of Elgar power sources. The power source itself will deliver a 10-year service life and a documented MTBF of 24,000 hours. That's nearly 2½ years of continuous operation or 12 years of normal service. This is Elgar quality . . . and we build it into every product we produce.

The quality doesn't stop with the components, however. The stated specifications on all Elgar power sources are conservatively rated on the basis of what they'll deliver where it counts . . . at the output. We see no logic in specifying our products on the basis of some internal capability which is greatly reduced by the time it reaches the output. An example is our decoder programmer. The specifications quoted are at the output and include those of the power source as well as the programmer. This user orientation of our specifications can also be found in our frequency range. We quote to 10KHz. Why go further when there's hardly an application that requires it?

The proof of the Elgar story does not come from us however . . . but from our customers. In over seven years of existence, we have served some of the leading Government agencies and corporations in the world . . . organizations who demand service and quality.

We suggest that you be the judge. We're prepared to prove this to you . . . in your laboratory or ours.

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APPENDIX H

THERMAL TEST SYSTEM

1.0 INTRODUCTION

The controlling thermal parameters in the performance of a forced air cooled computer are the supply temperature and the mass flow rate of the cooling air.

2.0 ANALYSIS

The limiting temperature of a device may be written in the form:

$$T_d = Ta + \Delta Ta + \Delta Tf + \Delta Tc \qquad (1)$$

where: Td = device malfunction

Ta = supply air temperature

Δ Ta = air temperature rise as air passes through the computer

Δ Tf = film temperature rise

ΔTc = chassis temperature rise to the device.

Each of these terms may be expressed explicitly as follows:

(1) Td = Cl, a constant

(2) Ta = variable

(3) ΔTa = q/mcp

where: q = heat dissipation, a constant

cp = specific heat of air, a constant

m = mass flow rate of air, a variable

thus,

ΔTa = C2/m, C2 a constant

(4) ΔTf = q/hA

where: q = as before

A = heat flow area of heat exchanger, a constant

h = convective film coefficient

$= f(Re)$

Re = Reynold's Number

$\propto m^n$

n = constant

thus,

$$Tf = C3/m^n$$

where C3 is taken to be approximately constant

(5) $Tc = C4$, approximately a constant

2.1 RESULTS

Substituting into equation (1) and using $C5 = C1 - C4$

$$C5 = Ta + C2/m + C3/m^n \quad (2)$$

A typical plot of equation 2 is shown in Figure H-1.

Figure H-2 shows a typical flow-pressure drop performance curve for a computer.

3.0 TEST PROCEDURE

The test procedure for obtaining data to construct such curves is illustrated in Figure H-3 and delineated below. The foregoing procedure is valid not only for a push-through air supply, but also for a draw-through supply, since the pressure measurements are reduced to standard density supply air.

3.1 Flow Pressure Measurements

3.1.1 Air is supplied to the computer by means of a blower. The flow is controlled by a valve and measured by a suitable flow meter and manometer.

3.1.2 Entering air temperature is established by an air conditioner. Entering and exhaust air temperatures are measured by means of thermocouples and a recorder.

3.1.3 The pressure loss across the computer is measured by means of static pressure taps in the ducting and a manometer.

3.1.4 Barometric measurements are taken in order to determine mass flow rate and to reduce the data to standard air density conditions.

3.2 Operating Procedure

3.2.1 The entering air temperature is fixed at a high mass flow rate and pressure temperature, and flow measurements taken after system temperature have reached steady state.

3.2.2 The computer is exercised through suitable electrical operations to determine if it is functioning satisfactorily.

3.2.3 The mass flow rate is reduced (holding the entering air temperature fixed) steady state reached and the electrical test operational repeated.

3.2.4 This procedure is repeated until some functional failure occurs in the computer. This defines a point on the curves in Figures H-1 and H-2.

3.2.5 The entering air temperature is changed and the whole procedure, 3.2.1 thru 3.2.4 repeated.

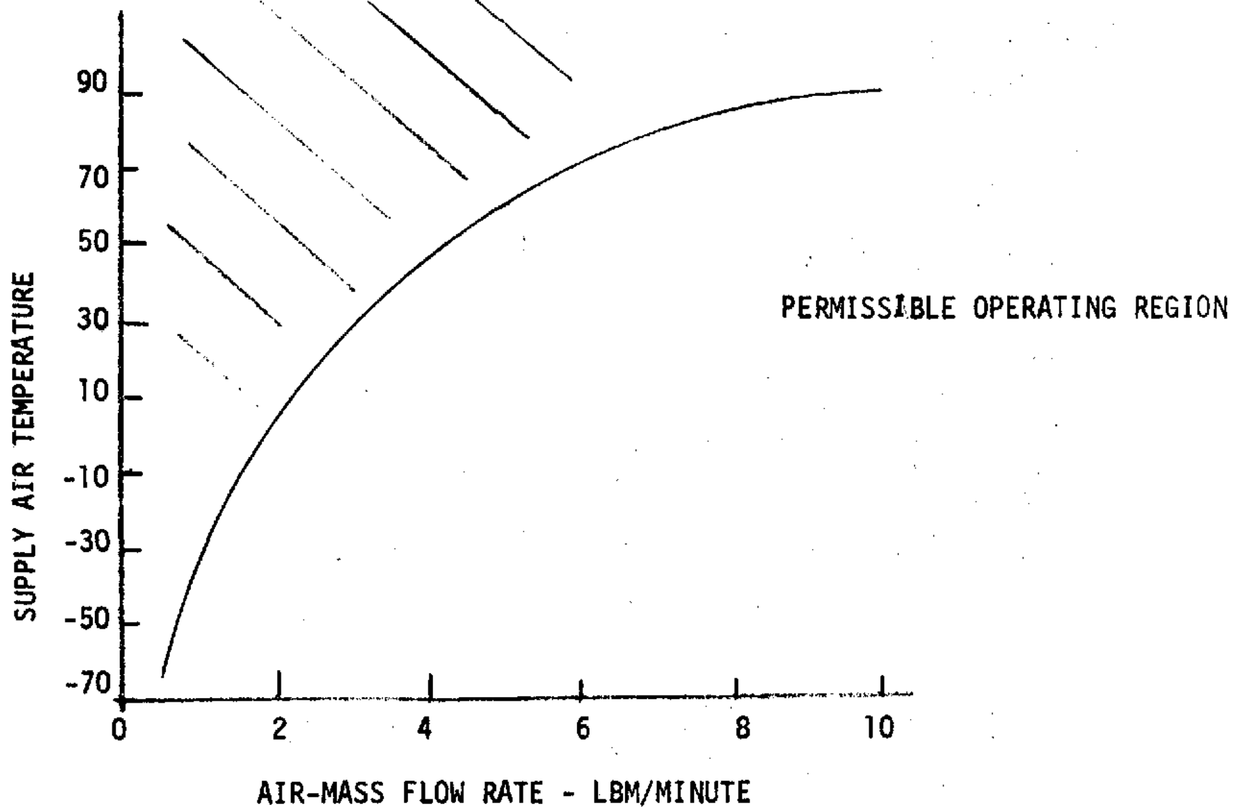
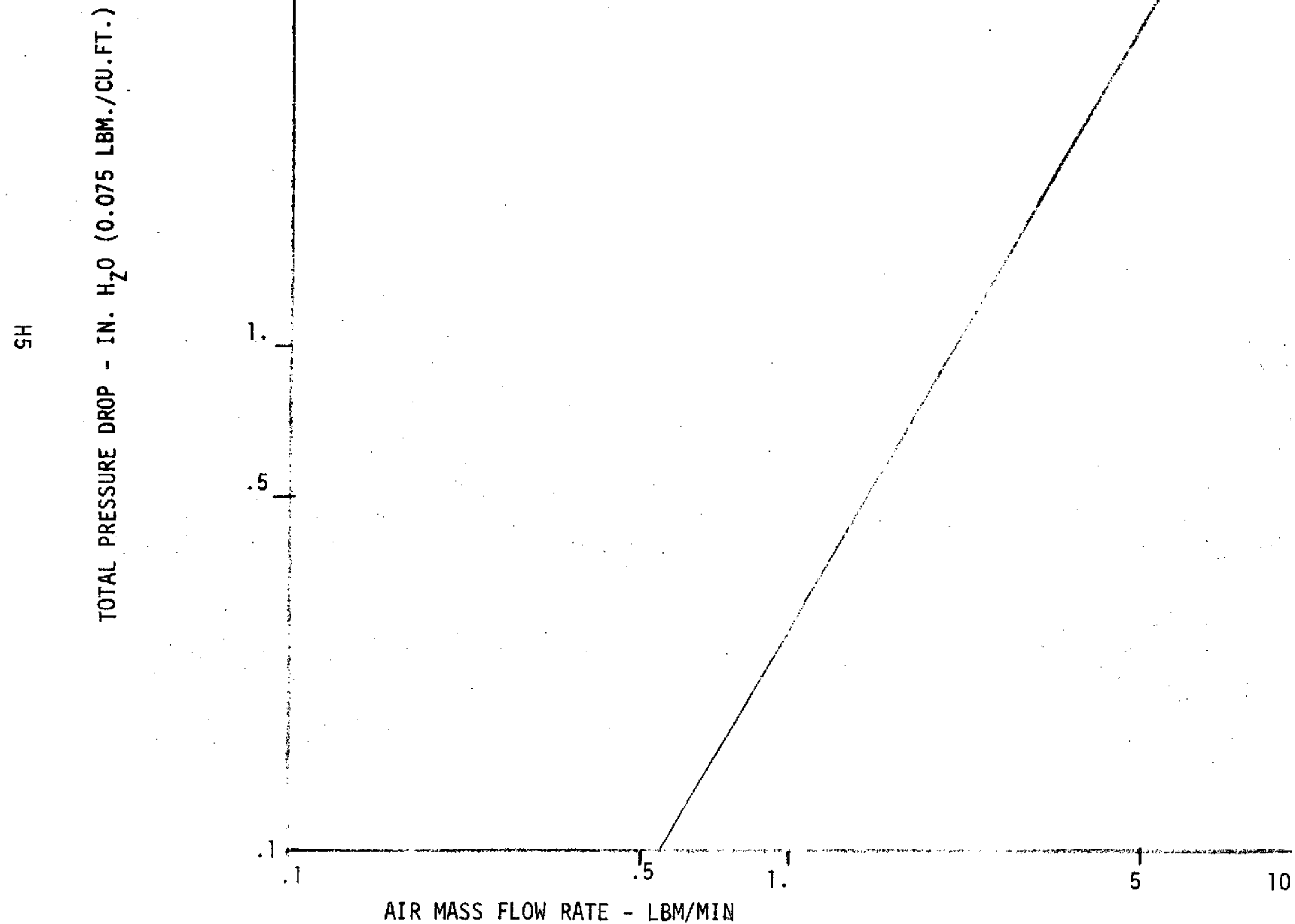


FIGURE H1 - PERMISSIBLE OPERATING CONDITIONS

FIGURE H-2 - TYPICAL FLOW PRESSURE DROP CHARACTERISTICS



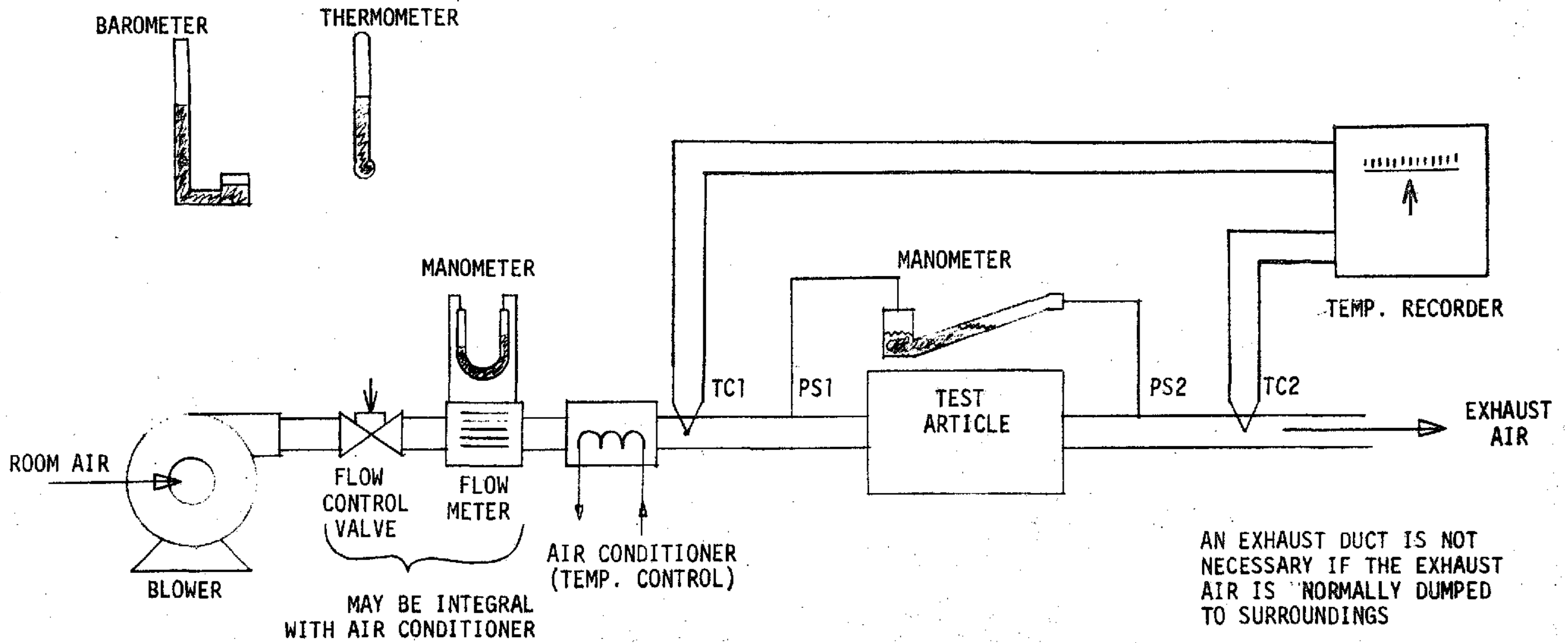


FIGURE H3. THERMAL TEST SETUP