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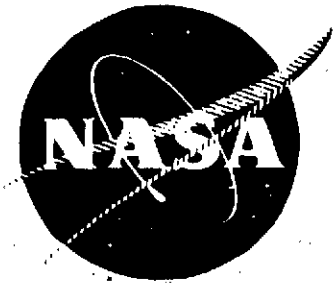

THE APPLICATION OF THE ANALOG SIGNAL TO DISCRETE TIME INTERVAL CONVERTER TO THE SIGNAL CONDITIONER POWER SUPPLIES

by

A. D. Schoenfeld and Y. Yu

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16. Abstract

The Analog Signal to Discrete Time Interval Converter (ASDTIC) microminiatruized module was utilized to control the signal conditioner power supplies. The multi-loop control provides outstanding static and dynamic performance characteristics greatly exceeding those generally associated with single-loop regulators.

Eight converter boards, each containing three independent dc to dc converter, were built, tested, and delivered to NASA/LeRC.

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FOREWORD

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1. SUMMARY

The application of the microminiaturized ASDTIC (Analog Signal to Discrete Time Interval Converter) to the signal conditioner power supplies is discussed in detail.

The ASDTIC, conceived originally within NASA, was utilized as the basic control element for three buck switching regulators, which resulted in uniformly superior static and dynamic performances. For example, a $\pm$0.05% output voltage regulation was achieved for an input change of 18V to 32V, a load change of open to full load (10W), and a temperature range of -55°C to 85°C.

A network to recover power-transistor switching loss was implemented to improve reliability, efficiency, and EMI control.

The successful application of the ASDTIC module has established the soundness of the ASDTIC control concept, and justified its further exploitation to utilize fully the inherent merits associated with the ASDTIC control.

2. INTRODUCTION

A nondissipatively-regulated dc to dc converter generally employs high-frequency switching for size and weight reduction. The oscillation is achieved by cyclically operating the power switch of the converter in its conduction state and its nonconduction state. Consequently, the converter control system must be able to accept analog signals emanating from the power circuit and the control reference, and to convert them into discrete time intervals in controlling the conduction and nonconduction of the power switch. The ratio of conduction time to a switching-frequency period is known as the power-switch duty cycle.

A classical duty-cycle control based exclusively on the sensing and amplification of the converter output-voltage error generally suffers certain inherent limitations. These limitations are basically caused by the LC output filter of the converter, which introduces poor dynamic response and potential instability into the converter operation.

The ever-increasing demands of space programs have served to promote considerable research effort toward the development of an electronic control system capable of improving the power-processor performance. One such system was conceived within a NASA Internal Research Program by Dr. F. Schwarz[1], [2]. The controlling element in the system is basically an Analog-Signal-to-Discrete-Time-Interval converter (ASDTIC). In addition to the feedback control loop sensing the dc output voltage, the ASDTIC incorporated a second loop sensing an ac waveform inherent in the converter operation. This waveform can be either the voltage across the output-filter inductor or the current in the output-filter capacitor. Using this two-loop control, converter stability is enhanced, and its performance characteristics are greatly improved.

The ASDTIC control concept was subsequently reduced to a microminiaturized thin-film hybrid under contract NAS12-2017, and documented[3,4].

This report describes the application of the microminiaturized ASDTIC module to a number of dc to dc converters. The packaged converters were used as signal-conditioner power supplies for the Brayton Cycle Space Power System. The power supplies consist of eight module frames, each of which contains three independent dc to dc chopper regulators; one 28V to 10V converter, one 28V to 5V converter, and one -28V to -10V converter. Each converter utilizes a microminiaturized ASDTIC module to achieve the desired regulating function. This report covers the design, development and fabrication of these converters. The work described here was performed from December 1969 to October 1970, under contract NAS12-2017, from NASA's Lewis Research Center.

The description starts with a converter block diagram, followed by a detailed discussion of each block in terms of the converter schematic. Breadboard performances are then presented to demonstrate the superb regulation accuracy obtained from the control loop. Packaging concepts including thermal consideration and component layout are discussed, and pictures of the fabricated power supply modules are given.

3. CONVERTER FUNCTIONAL BLOCK DIAGRAM

All three converters on each of the eight module frames have essentially the same block diagram shown in Figure 1. The dotted line shows the division between power and control circuit functions. These functions are summarized in Tables I and II, respectively.

TABLE I. POWER CIRCUIT FUNCTIONS

Blocks	
Input Filter	Its functions are: (1) to isolate the switching effect of the converter from the power bus, and (2) to absorb voltage transients on the bus.
Basic Power Configuration	Input Voltage E, transistor switch S, diode D, inductor L, capacitor C, and load R constitute the basic stepdown chopper regulator. By properly controlling the duty cycle of switch S, a constant load voltage V can be maintained against variations in E and R.
Energy Recovery Network	The network serves (1) to limit the inrush current during the short interval when S is turned on and D is in the process of recovering its blocking capability, thus improving efficiency and reliability, and (2) to reduce the switching spike at the converter output.
Voltage Booster	The need for this network is predicated by the off-nominal low input voltage specified for this particular converter. It adds a voltage in series with the converter input to ensure the proper operation of the converter control logic.

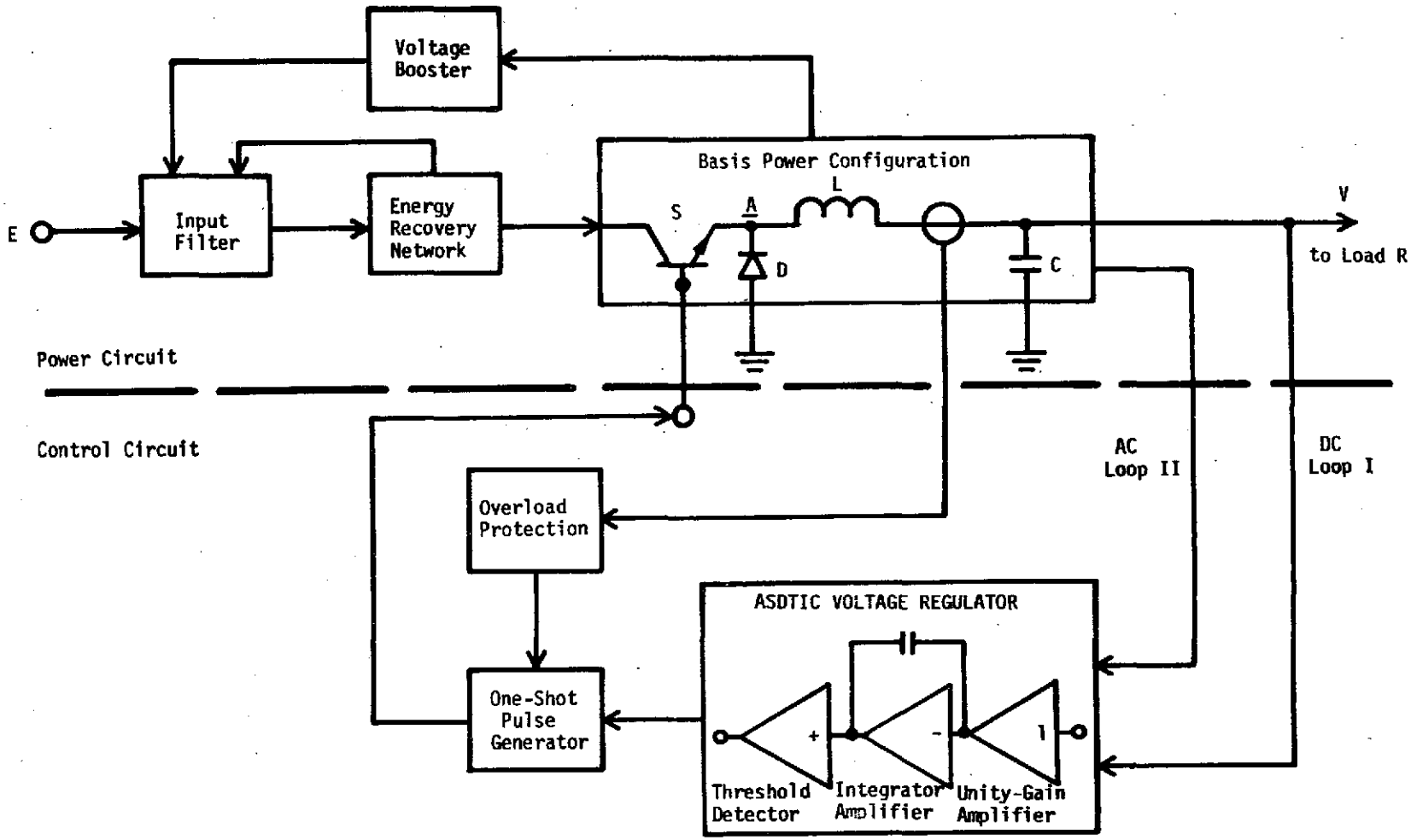


Figure 1. Converter Functional Block Diagram

TABLE II. CONTROL CIRCUIT FUNCTIONS

Blocks	Functions
ASDTIC Voltage Regulator	Starting from point A at the tip of diode D and tracing clockwise, the ac voltage across L and the dc voltage across C are separately sensed to become two input signals to the ASDTIC voltage regulator. The regulator processes the sensed signals, and provides the proper output to actuate a one-shot pulse generator for controlling the duty cycle of power switch S.
One-Shot Pulse Generator	It determines the conduction time of switch S as a function of the converter input voltage E. The time interval is initiated by the output pulse from the threshold detector within the microminiaturized ASDTIC voltage regulator.
Overload Protection	Overload protection is accomplished by sensing the inductor current. In the event of an overload, the combined function of the current sensor and the ASDTIC voltage regulator keeps S in switching-mode operation during current limiting; its duty cycle depends on the severity of the overload.

4. CONVERTER SCHEMATICS

The schematics for the three converters on each module frame are shown in Figure 2. From top to bottom, the converters are those providing a +10V output, a -10V output, and a +5V output. Detailed descriptions of all blocks, based on the given schematics, are given in the next section.

The accompanying parts list for Figure 2 is presented in the Appendix.

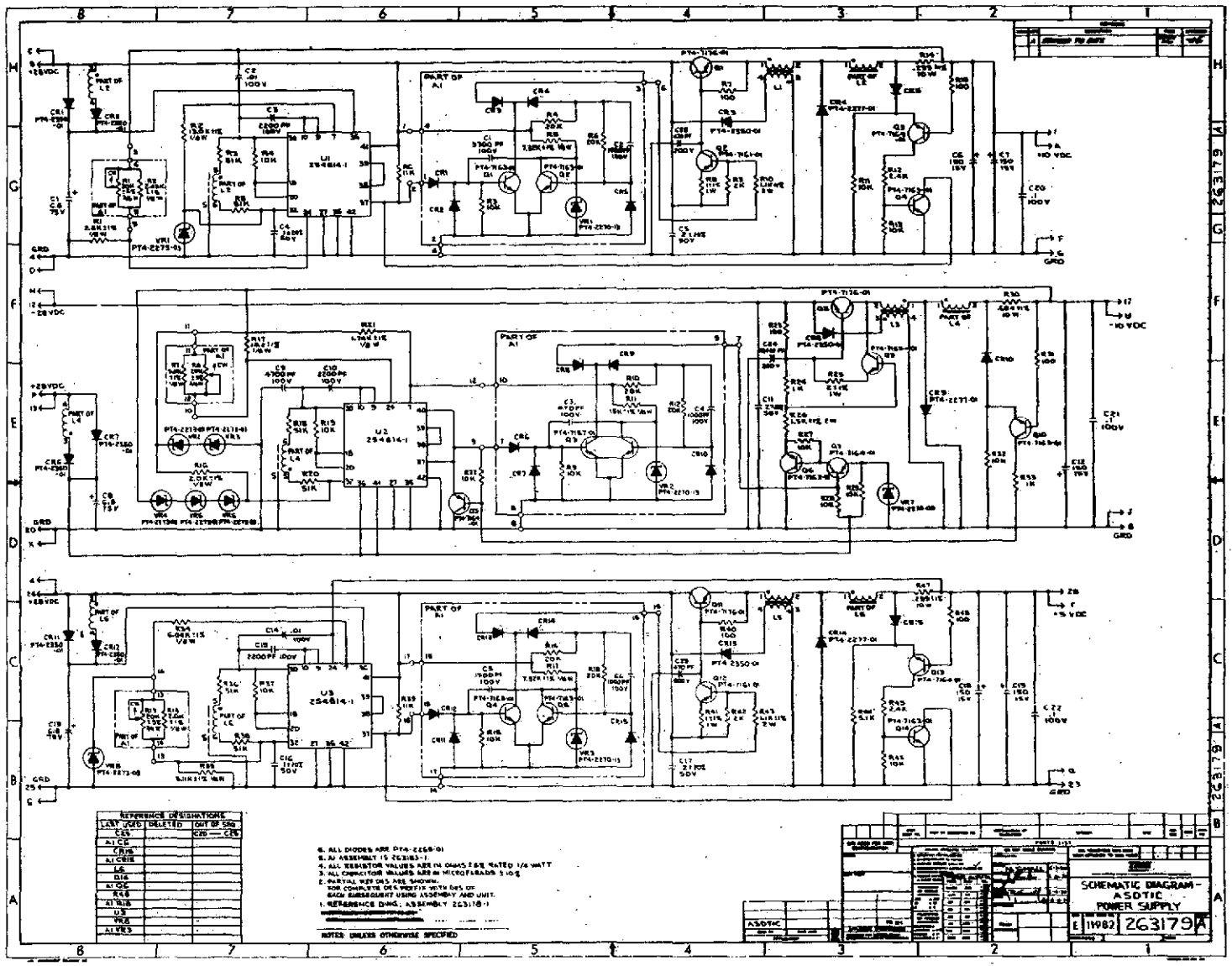


Figure 2. Schematic Diagram of the Signal-Conditioner Power Supply

5. DESCRIPTIONS OF POWER FUNCTIONAL BLOCKS

Due to the similarity among the three converters, the +10V converter will be used to describe circuit operations and designs associated with the functional blocks of all three converters.

5.1 INPUT FILTER

The input filter is physically located external to the fabricated converter module, and therefore is not shown in the schematic of Figure 2. The filter utilizes the two-stage configuration illustrated in Figure 3. The first stage containing L_A, R_A and C_A limits the resonant peaking of the entire filter. The second stage with L_B and C_B supplies most of the pulsed ac current required by the converter power switch. The combined function of both filter stages is to accomplish the two objectives stated in Table I.

5.2 BASIC POWER CONFIGURATION

Shown at the top of Figure 2, the +10V converter basic power configuration consists of power switch Q1, diode CR4, inductor L2, capacitors C6 and C7 in parallel, and the load. During the time when Q1 conducts, CR4 is back biased, input voltage E is supplied to the circuit containing inductor L2, capacitors C6 and C7, and the load. During the time when Q1 is off, CR4 becomes conducting to keep the current continuity in L2. The LC filter maintains essentially a dc voltage across the load.

Normal Operation

In steady-state, the net energy storage in L2 must be zero. Therefore,

$$(E - V)T_{on} = VT_{off}. \tag{1}$$

Equation (1) is equivalent to

$$ET_{on} = VT \tag{2}$$

where $T = T_{on} + T_{off}$.

By maintaing a constant product of ET_{on}, the converter having a regulated V would operate essentially at a constant frequency 1/T. This feature is utilized to its advantage in the power converters.

Light-Load Operations

The light-load condition is defined as that causing the current in L2 to become zero during each steady-state operating cycle, and to remain zero for an interval T'_{off}.

While equation (1) concerning zero net energy storage is still valid under this condition, the introduction of T'_{off} has caused a new switching period T' > T. The triangular input current averaged over a cycle is

$$I_{ave} = \frac{(E - V)T_{on}}{2L_2} \cdot \frac{T_{on}}{T'} \quad . \qquad (3)$$

Multiplied this current by input voltage E and converter efficiency e gives output power V^2/R, from which one obtains

$$T' = T_{on} + T_{off} + T'_{off} = \frac{EeRT^2_{on} \quad (E - V)}{2L_2V^2} \quad . \qquad (4)$$

Therefore, the lighter the load R and/or the smaller the inductance L2, the lower will be the operating frequency 1/T'.

Critical Load Resistance

The critical resistance, R_K, is defined as the particular light load at which the previously described T'_{off} emerges. Period T of (2) and T' of (4) are identical at this load, thus giving

$$R_K = \frac{2L_2V}{(E-V)eT_{on}} \qquad (5)$$

Notice that R_K increases with L2 and decreases with T_{on} and e.

In the signal-conditioner converters, L2 and T_{on} are so designed that, within the specified line and load variations, the converters never encounter a nonzero T'_{off}. However, all converters are capable of maintaining regulation at light loads. Indeed, each converter provides stable operation into no load without exceeding the required regulation limit.

Output Voltage Ripple

The current excursion through inductor L2 is given by

$$\Delta i = \frac{(E - V)T_{on}}{L_2} \quad . \tag{6}$$

The ripple voltage across C6 and C7 and the ripple current in them are generally in phase, suggesting that the ripple voltage is due largely to the equivalent series resistance R_c of the two paralleling capacitors. The equation for Vpp becomes

$$Vpp \cong R_c \Delta i = \frac{(E-V)T_{on}R_c}{L_2} \tag{7}$$

5.3 ENERGY-RECOVERY NETWORK

If no energy-recovery network were used, the finite recovery time associated with diode CR4 of Figure 2 would cause a sharp current pulse to pass through the source, Q1, and CR4 at the start of each T_{on} interval, causing peak power dissipation in Q1 and CR4. This sudden increase of current also induces RFI, which not only propagates to the regulator output, but in addition, it can cause other spacecraft electromagnetic compatibility problems.

For the regulator to meet the peak-peak noise specification, the networks composed of inductor L1 and diode CR3, shown in Figure 2, are used. During the on-time of Q1 and the recovery time of CR4, input voltage E is absorbed by reactor L1. Diode CR3 is reverse biased, and energy is stored in L1. The rate of the current increase at the beginning of T_{on}; the energy stored in it during T_{on} is returned to the source via diode CR3.

For the signal-conditioner converters, L1 is designed to be 12.5μH. At a maximum E of 32V, the rate of current increase is 32/12.5, or 2.56amp/μs. It therefore takes approximately 1μs for the turn-on current to rise from zero to the 2-amp average load-current level. By that time, diode D1 will have been fully recovered. The RFI associated with the turn-on of power switch Q1 is thus minimized. Pictures of output-voltage switching spike, with and without this suppression network, are given in Figure 4 to illustrate the utility of the network. The upper trace, representing the output-voltage ripple when no energy-recovery network was used, exhibits a considerably higher switching spike at the beginning of T_{on} interval as compared to the lower trace when the energy-recovery network was used. The higher switching spike of the upper trace is directly related to the sharper current rise previously described.

In addition to noise reduction, the network also improves the converter efficiency. For without choke L1, transistor switch Q1 would experience high dissipation due to the simultaneous high current and high voltage (i.e., essentially input voltage E) during the recovery time of diode CR4. However, the network enables most of this otherwise-lost energy to be conserved and returned to the power source.

5.4 VOLTAGE BOOSTER

The ASDTIC module requires a minimum bias supply of 22V. However, the input voltage E is only 18V during off-nominal operations. A winding N_{34}, shown schematically near the converter input, is therefore provided from output choke L2 to boost the supply voltage. This winding, along with the associated diodes CR1, CR2 and capacitor C1, are shown schematically in Figure 2. The phase relation between N_{12} and N_{34} of L2 is such that, in conjunction with input E and the peak charging of capacitor C1, a minimum of 22V is maintained for supplying the ASDTIC bias when E becomes 18V during off-nominal operations.

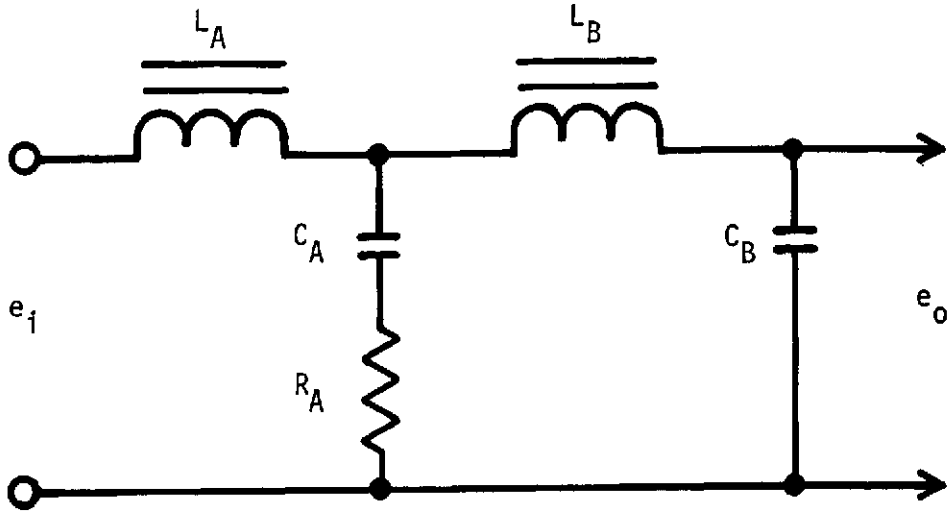
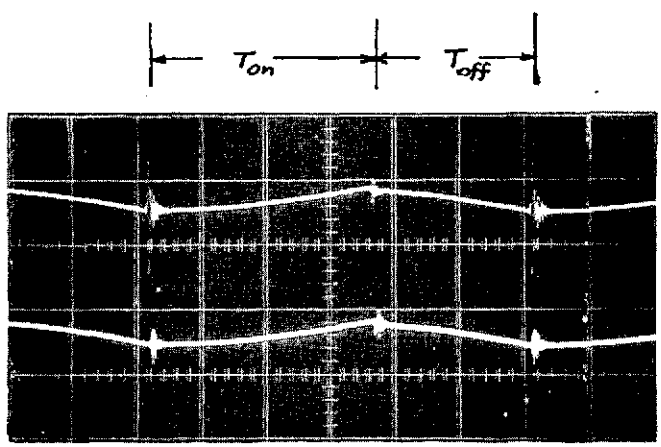


Figure 3. The Two-Stage Input Filter



Vertical: 20mV/Div.
Horizontal: 5μs/Div.

Figure 4. Converter Output-Voltage Switching Spike
(a) Without the Energy Recovery Network
(b) With the Energy Recovery Network

6. DESCRIPTIONS OF CONTROL FUNCTIONAL BLOCKS

The +10V converter shown in Figure 2 will again be used for control-circuit description.

6.1 ASDTIC VOLTAGE REGULATOR

The central component of the ASDTIC voltage regulator is the microminiaturized ASDTIC Module U1. Detail description of the thin-film module can be found in Reference [3]. The module, shown schematically in Figure 5, contains the following basic elements:

- Unity-Gain Amplifier
- Integrator Amplifier
- Threshold Detector
- Series Regulator

The first three elements are shown in the converter block diagram of Figure 1. The series regulator is used to provide a regulated bias voltage for the first three elements. The terminal numbers shown in Figure 5 correspond exactly with those of U1 in Figure 2.

Before entering the detail description of the ASDTIC voltage regulator in Figure 2, it is noted that the +10V converter components are packaged in two boards - a main board and a baby board. The baby board, Board A1, contains those components within the rectangular dotted enclosures of Figure 2. Thus, the R1 and Q1 on the main board, for example, are not to be confused with the R1 and Q1 on the baby board. With the packaging details being reserved in Section 8 to be presented later, the +10V ASDTIC voltage regulator processing control signals from a dc loop and an ac loop are now described.

The dc loop senses the load voltage. The voltage is divided down by R1 of the main board (near the converter input ground) and the parallel combination of R1 and R2 on board A1. The divided signal is fed to pin 24 of the ASDTIC, which is the input terminal of the unity-gain amplifier used for impedance-matching. The output

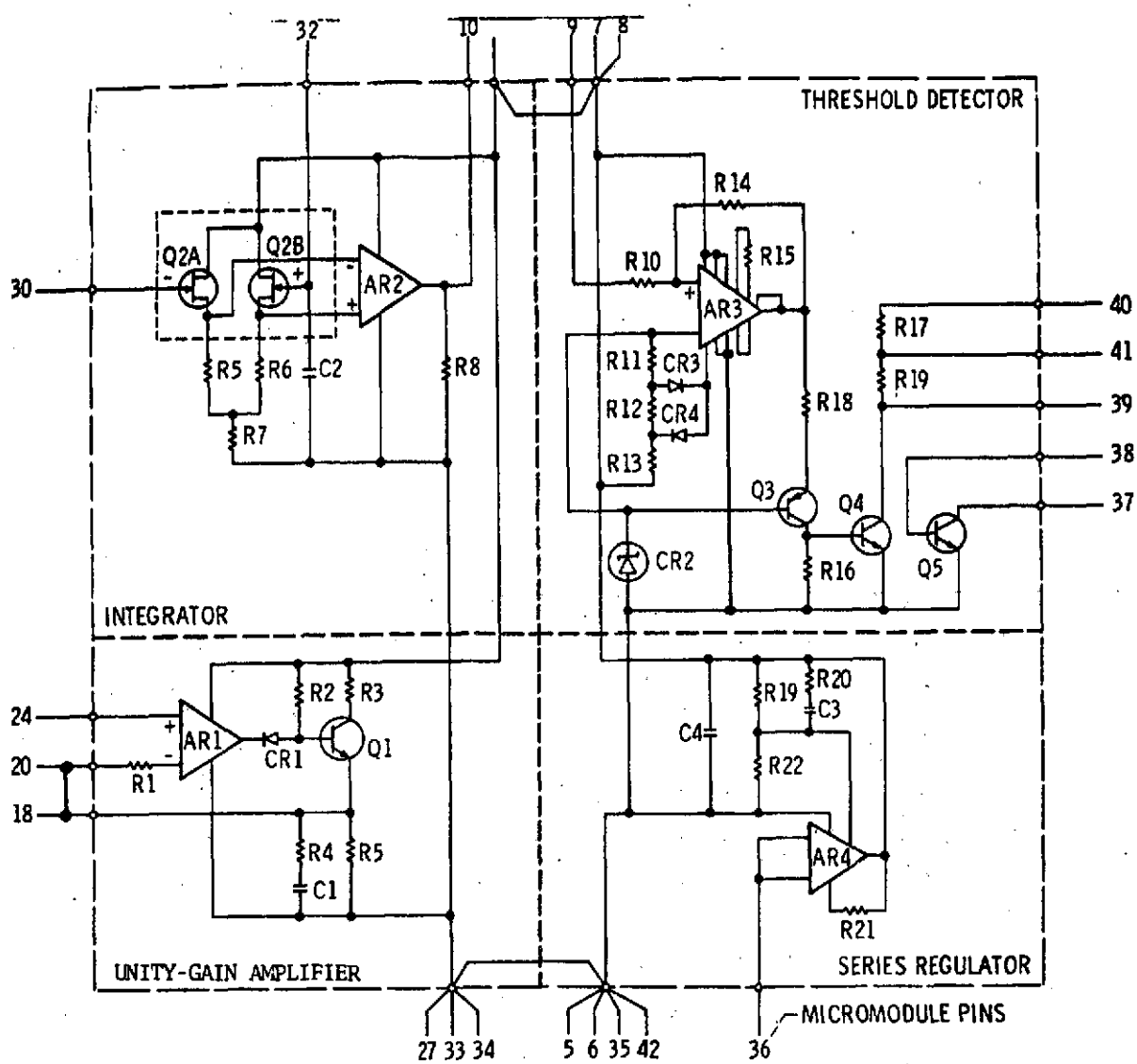


Figure 5. ASDTIC Module Schematic Diagram

from the unity-gain amplifier, derived from pin 18 and pin 20, connected in common, is fed to the "inverting" terminal of the integrator, pin 30, through a gain-controlling resistor R4.

The ac loop senses the instantaneous ac voltage across the inductor L2. Through gain-controlling resistors R3 and R5, the signal is fed differentially into the "inverting" and the "non-inverting" integrator terminals, pin 30 and pin 32. The algebraic sum of this ac signal and the dc output signal from the unity-gain amplifier are compared to reference VR1 applied to pin 32. The error is integrated by the integrating amplifier with time constant $C_3(R_3 + R_5)$, where C_3 is the feedback capacitor of the integrator amplifier connecting between pin 10 and pin 30.

The amplitude of the sensed ac inductor voltage is determined by the turns ratio N_{56}/N_{12} on L2. Its phase in relation to the integrator terminals is such that a ramp voltage with a positive or negative slope exists during the off or on time of power switch Q1. When the instantaneous value of the ascending ramp reaches an internal reference, E_T, of the threshold detector, the pulse output from the detector available at pin 37 will actuate the one-shot pulse generator through diode CR1 on board A1, which in turn controls the power transistor to conduct for a predetermined time interval T_{on}. During T_{on}, slope of the ramp voltage at the integrator output is negative. In steady-state operation, the positive excursion of the integrator output voltage during T_{off} is identical to its negative excursion during T_{on}.

It is noted that the ac loop ensures equal volt-seconds for the positive and negative half-cycle of the inductor voltage, thus securing zero net energy storage per cycle in the inductor during converter switching operation. Compared with the dc loop which senses the converter output voltage averaged by a low-frequency LC filter containing L2, C6 and C7, the control action of the ac is instantaneous.

To illustrate this fast action graphically, waveforms at several key points along the control-signal path are identified in Figure 6. Here, the converter input voltage is assumed to have a step increase, with the corresponding voltage across inductor L2 shown as E_L. The ascending integrator output ramp voltage E_I intersects the threshold level E_T to effect the threshold-detector output pulses E_{TD}. Each of these output pulses initiates a conduction interval T_{on} through the pulse generator represented by E_{PG}.

With the qualitative description of the ASDTIC voltage regulator now presented, attention is now drawn to two important integrator performance considerations - its output voltage waveform and a functional subtlety associated with its frequency response.

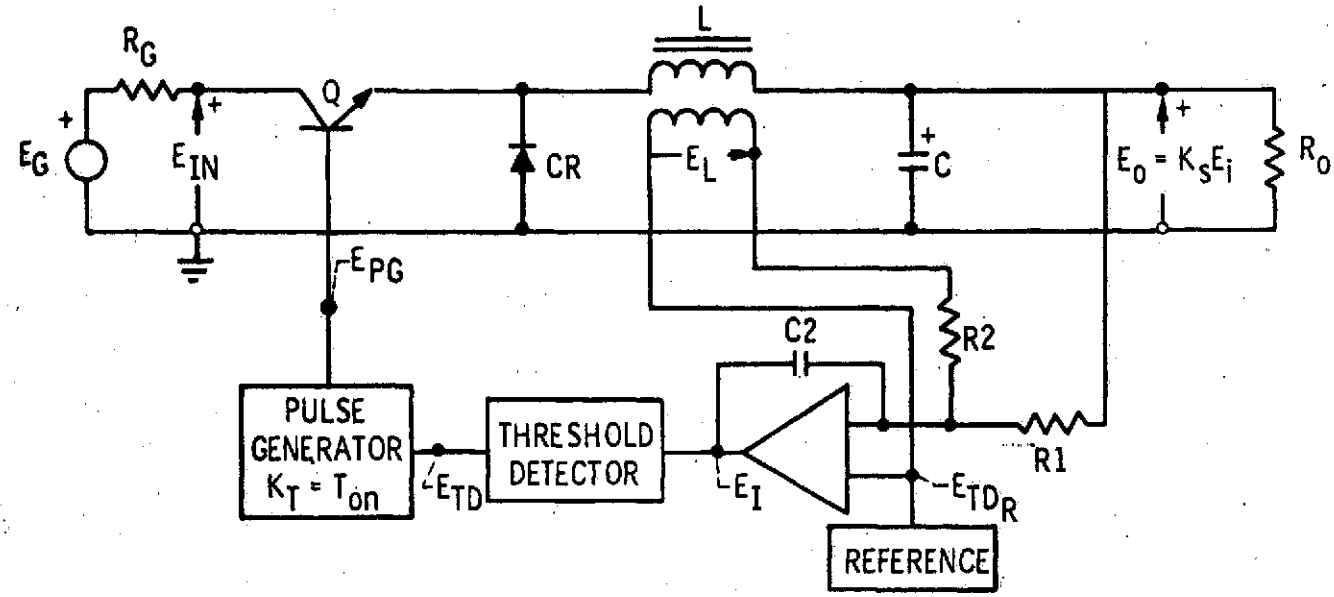
Integrator Output Waveform

For convenience, the inductor voltage E_L, and the integrator output E_I are given in Figures 7(A) and 7(B). The straight line in Figure 7(B) passing (T, e_T) with a slope $NV/(R3 + R5)C_3$ can be expressed as

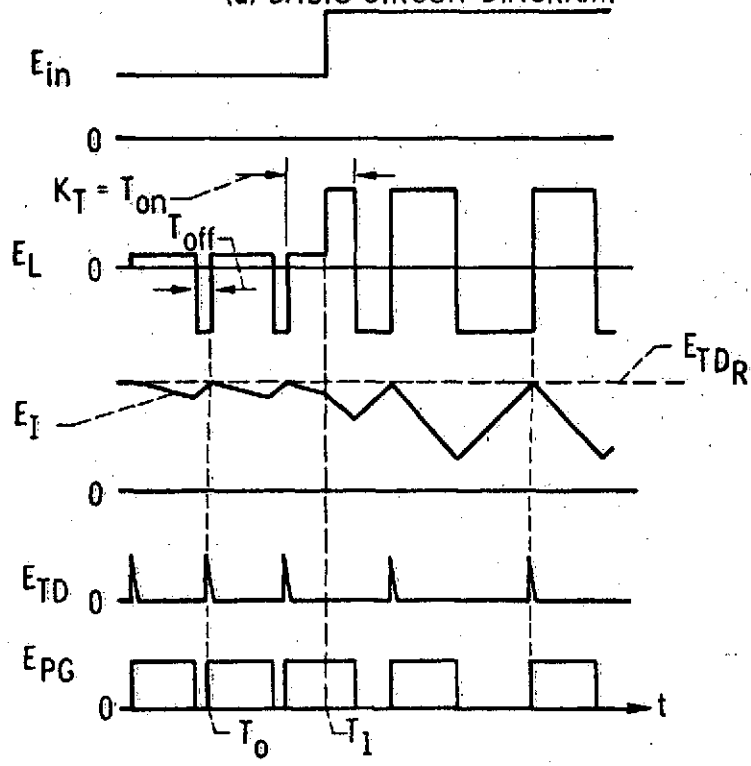
$$e = e_T - \frac{NV}{(R_3 + R_5)C_3} (T - t) \qquad (8)$$

where $N = (N_{56}/N_{12}$ on inductor L2) is the ac signal sensing ratio, and $T = (T_{on} + T_{off})$ is the converter switching period. Combining (2) and (8) at $t = T_{on}$ gives

$$e = e_T - \frac{NT_{on}}{(R_3 + R_5)C_3} (E\text{-}V) \qquad (9)$$



(a) BASIC CIRCUIT DIAGRAM.



TIME, μSEC

(b) WAVEFORMS.

Figure 6. Step-Down Chopper Regulator and ASDTIC Control Waveforms

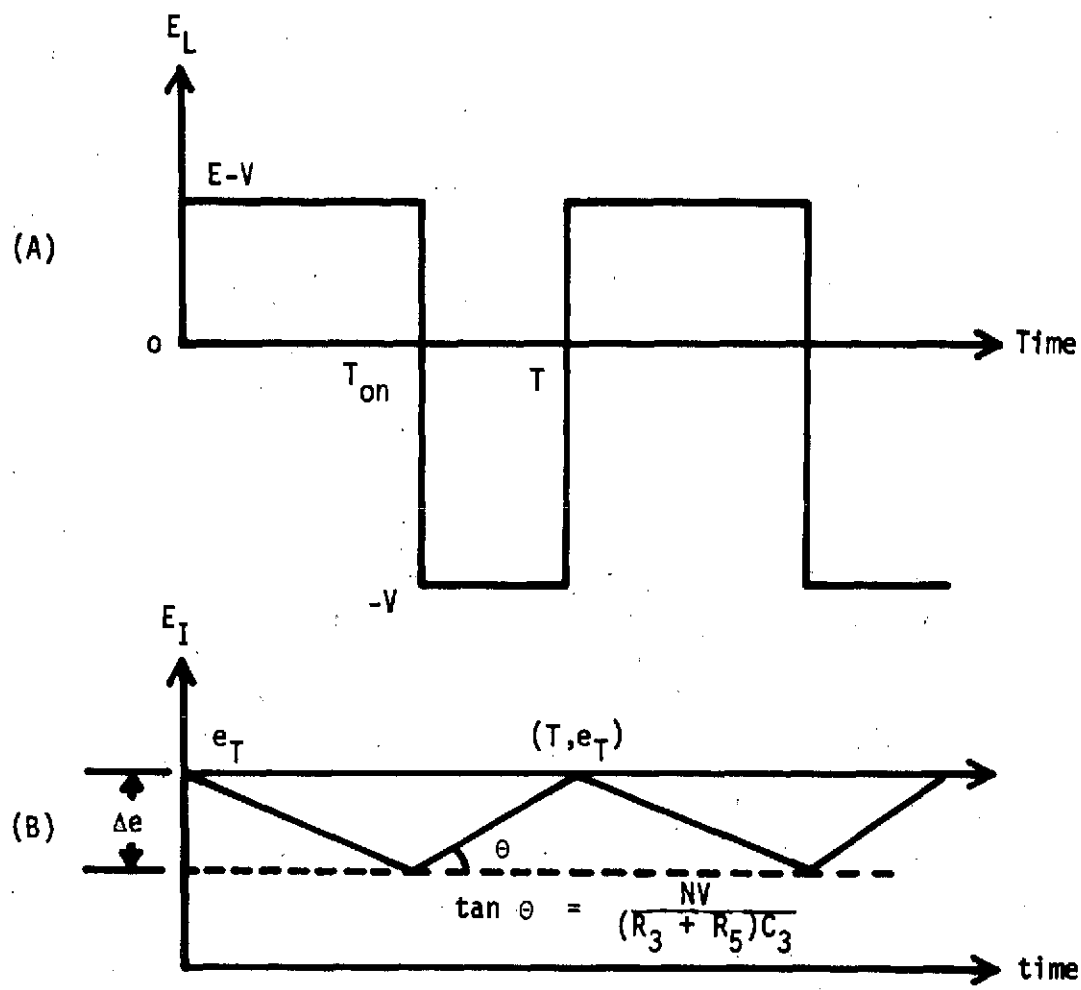


Figure 7. ASDTIC Integrator-Amplifier Output Voltage
(A) Inductor Voltage
(B) Integrator Output Voltage

Thus, the integrator output swing Δe of Figure 7(B) is

$$\Delta e = \frac{NT_{on}}{(R_3+R_5)\ C_3}\ (E-V) \qquad (10)$$

Equation (10) is used in designing Δe so that it is being limited to 2 volts, which is well within the threshold level e_T, thus always maintaining a linear regulator operation.

6.2 THE SIGNIFICANCE OF CAPACITOR C2 MAIN BOARD

As discussed previously, the ASDTIC regulator has two feedback loops; the dc loop sensing the load voltage, and the ac loop sensing the inductor voltage. These two loops tend to interact in such a way as to form an extremely underdamped second-order system at a particular frequency. Consequently, any transient line or load change would introduce to the regulator output a damped yet prolonged oscillation at that frequency, giving rather undesirable dynamic performances.

Mathematically, the frequency response of the ASDTIC regulator can be expressed as the following:

$$F(s) \cong \left[\frac{K}{1+SA}\right]\ \left[\frac{1}{1+SB+S^2C}\right]\ [1+SD+S^2E] \qquad (11)$$

The first bracket on the right-hand side of equation (11) is the frequency response of the integrator, with the numerator as its dc gain. The second bracket represents the characteristic of the output LC filter and the load. The third bracket illustrates the interaction between the dc loop and the ac loop.

Unlike the conventional second-order filter response in which the second-order equation in "s" appears in the denominator, this second-order interaction appears in the numerator. Plotted on a Bode diagram, this term introduces a negative-going valley, centered at frequency F, where F is a function of the filter as well as the control-circuit design. Specifically, F can be shown to be the following:

$$F \cong F_f \left(\frac{gR_{ac}}{NR_{dc}}\right)^{1/2} \qquad (12)$$

Here, F_f is the resonant frequency of the output LC filter, g is the dc voltage-divider ratio, R_{ac} is the ac loop gain-controlling resistance, R_{dc} is the dc loop gain-controlling resistance, and N2 the inductor-voltage sensing turns ratio. Corresponding to the +10V converter schematic,

$$g = \frac{(R_1)_{\text{on mainboard}}}{(R_1)_{\text{on mainboard}} + \left(\frac{R_1 R_2}{R_1 + R_2}\right)_{\text{on A1 board}}}$$

$$R_{ac} = R_3 + R_5$$

$$R_{dc} = R_4$$

and

$$N = N_{56}/N_{12} \text{ on L2.}$$

Depending on the damping value of "D" in the third bracket of equation (11), the negative-going valley can be of very high amplitude, causing significant gain reduction. A sudden disturbance in either the line or the load condition would cause the regulator output to engage in prolonged osillation, yielding undesirable line and load dynamic response and poor audio-susceptibility performance within a frequency band centered at F.

To mitigate this undesirable characteristic, capacitor C2 is used, connecting between the converter output and the integrator input (Pin 30 of ASDTIC module). This greatly increases the damping value of "D" in equation (11), thus reducing the amplitude of the negative-going valley and its detrimental consequence. The effect of C2 has been substantiated both mathematically and experimentally. In addition, the use of C2 allows stable converter steady-state operation to be maintained when load resistance increases beyond R_K, defined previously in equation (5).

6.3 ONE-SHOT PULSE GENERATOR

As shown in Figure 2, the pulse generator is located on the A1 board. To start with, the converter input voltage E drives a base current $E/(R_4 + R_6)$ to keep Q2 in conduction. Resister R3, on the other hand, keeps Q1 off. The Q1, Q2, R3, R4, and R6 here are those on board A1, and should not be confused with those on the main board.

When a positive pulse is applied to the base of Q1 through diode CR1, the sudden decrease of Q1 collector voltage causes Q2 to come out of saturation. The consequent current in C1 resulting from an increase in the collector voltage of Q2 regenerates itself rapidly until Q1 conducts and Q2 turns off and remains off. Transistor Q1 is kept in conduction by the current path composed of E, R5, and C1, and base-emitter junction of Q1. This state continues until C1 is charged to the zener breakdown voltage of VR1, when Q1 is suddenly deprived of its base drive and turns off, which, in turn, initiates the turn-on of Q2. Following the complete turn-on of Q2, the one-shot pulse generator is ready for another trigger pulse. The on time of Q1, which is concurrent with the conduction of CR3 (on board A1) and Q1 and Q2 on the main board, determines on-time T_{on} of the chopper-regulator power switch. To charge C1 through R5 from voltage E, the time required for V_{c1} to reach VR1 is:

$$T_{on} = R_5 C_1 \ln \left(\frac{E}{E - VR1} \right) . \qquad (13)$$

6.4 OVERLOAD PROTECTION

The overload protection is physically placed on the main board. Current in inductor L2 is sensed by R14. The voltage $i_{L2}R_{14}$ during normal operation is insufficient to turn on Q3 and Q4. The pulse generator therefore receives command pulses from the ASDTIC exclusively to control the cyclic on-off of power switch Q1 for as long as a regulated load voltage is maintained.

As load resistance diminishes during overload, the load-voltage regulation is eventually lost. The dc error applied to the ASDTIC is of such a phase relation that the output voltage from the threshold detector is high, thus always providing a signal for the one-shot to turn on the power

switch for the T_{on} interval defined by equation (13). At the start of and throughout the interval T_{on} when the instantaneous current of i_{L2} is increasing, the voltage drop $i_{L2}R_{14}$ is sufficiently high to keep Q3 and Q4 in conduction.

With the completion of T_{on}, inductor current i_{L2} decays through R_{14}, C6 and C7, and CR4. During the decay, Q3 and Q4 maintain conduction, thus clamping pin 37 of the micro-ASDTIC unit and inhibiting the one-shot from turning on the power switch. The decay continues until $i_{L2}R_{14}$ becomes small enough to allow Q3 (and therefore Q4) to turn off. Upon removal of this inhibition, the signal from ASDTIC immediately actuates the one-shot to start another T_{on}.

Consequently, the switching action is maintained in the event of an overload. The on-time T_{on} of the power switch is identical to that during normal operation without an overload. The T_{on} interval starts as soon as the decaying i_{L2} during T_{off} causes $i_{L2}R_{14}$ to become insufficient to keep Q4 in conduction. The length of T_{off} therefore depends on the load resistance during overload. The longest T_{off} occurs when the output is short circuited. Under this condition and neglecting the small voltage drop across R_{15}, the inductor current decays at a rate of $[V_{CR4} + V_{CR5} + (V_{Q3})_{BE}]/L_2$. Since the current excursion during T_{on} and T_{off} is equal to ET_{on}/L_2, the longest T_{off} is therefore:

$$(T_{off})_{max.} \cong \frac{ET_{on}}{V_{CR4} + V_{CR5} + (V_{Q3})_{BE}} \qquad (14)$$

7. BREADBOARD PERFORMANCES

The +5V, +10V, and -10V converters were breadboarded and tested. Their performance characteristics were similar due to the use of identical ASDTIC control. To illustrate this uniformly-high performance capability offered by the ASDTIC, the requirement versus capability of the +5V converter breadboard, using the microminiaturized ASDTIC, is presented in Table III.

TABLE III

REQUIREMENT VERSUS CAPABILITY
+5V SUPPLY USING MICROMINIATURIZED
ASDTIC CONTROL MODULE
Temperature Range -55°C to 85°C

	CHARACTERISTIC	REQUIREMENT	CAPABILITY
Nominal Operation E_i = 28 ±4V	Voltage Regulation (mV)	±50	±2.5
	Maximum Output Current (A)	2	2
	Minimum Output Current (A)	1	0
	Output Center of Nominal Voltage (V)	4.8-5.2	5.034-5.039
	Output Ripple (p-p) (mV)	100	30
	Output Noise (mV)	100	40
	Maximum Short-Circuited Current (A)	6	5.4
Off-Nominal Operation E_i = 28 ±10V	Voltage Regulation (mV)	±250	±3
	Output Center of Nominal Voltage (V)	4.6-5.4	5.033-5.039
	Output Ripple (mV)	200	30
	Output Noise (mV)	100	40

From Table III, the following conclusions can be drawn:

(1) The measured output-voltage regulation of $\pm 0.05\%$ is an order of magnitude better than that required throughout the specified line, load and temperature range, including off-nominal operations when E = 18V and at no load.

(2) During normal operation, the output ripple and the noise spike are both within the allowed limits, each being specified at 100mV. Also, their amplitudes do not increase during off-nominal operations.

(3) The short-circuited current for each supply is limited to 5.4A, which is less than the 6A allowed.

8. CONVERTER PACKAGING

A geometric layout was made to fit a +10V, a -10V, and a +5V supply into each of the eight module frames furnished by NASA/LeRC.

Each module frame contains three major packaging portions: (1) metal frame, (2) baby board, previously referred to as Board A1, and (3) sheet metal base.

To provide proper heat-sinking, power elements including power transistors, output filter chokes, current-sensor resistors, and power diodes, are placed on the metal frame. The frame is fastened mechanically to the external sheet metal base. Service to these components can be made readily without disassembling the frame and the PC board. Separate feeders were used for input and output ground leads to maintain a clean output voltage ripple.

A baby board, identified previously as board A1, containing three pulse generators and voltage-divider trim pots, is employed to relieve component congestion and to obtain easy accessibility for output-voltage adjustments. The baby board and the PC board are separated from either side of the metal frame by spacers. Their total height is within the specified space envelope.

All other circuit parts, including the microminiaturized ASDTIC's, are placed on the sheet metal base. While all circuit components are placed on one side of the PC board, the component density on the board has necessitated the use of printed circuits on both sides. In planning the printed circuits, considerable attention was given to the maintenance of relatively noise-free surroundings for all sensor leads, all load output leads, and all voltage references. The PC board is planned so that no element generating significant amount of heat exists in the vicinity of the microminiaturized ASDTIC.

A picture of a fabricated converter board containing the +10V, -10V, and +5V converters is shown in Figure 8, in which the power inductors, transistors, diodes, and current sensing resistors for the three corresponding converters are easily seen. Board A1, the baby board, is shown in the foreground. The three microminiaturized ASDTIC's are located on the sheet metal base under the baby board, and are therefore invisible in Figure 8. The converter module's sheet metal base, with the baby board removed, is shown in Figure 9. The three microminiaturized ASDTIC modules are clearly identified.

Performances of the packaged converter met all the specified requirements. The regulation is not as precise as that of the converter breadboard, due to (1) the finite printed-circuit resistance between the regulator sensing point and the actual packaged converter output terminals, and (2) the temperature coefficient of the trimming potentiometer for packaged converter output-voltage adjustment, which replaced the precision resistor used in the converter breadboard to avoid any test-select implementation.

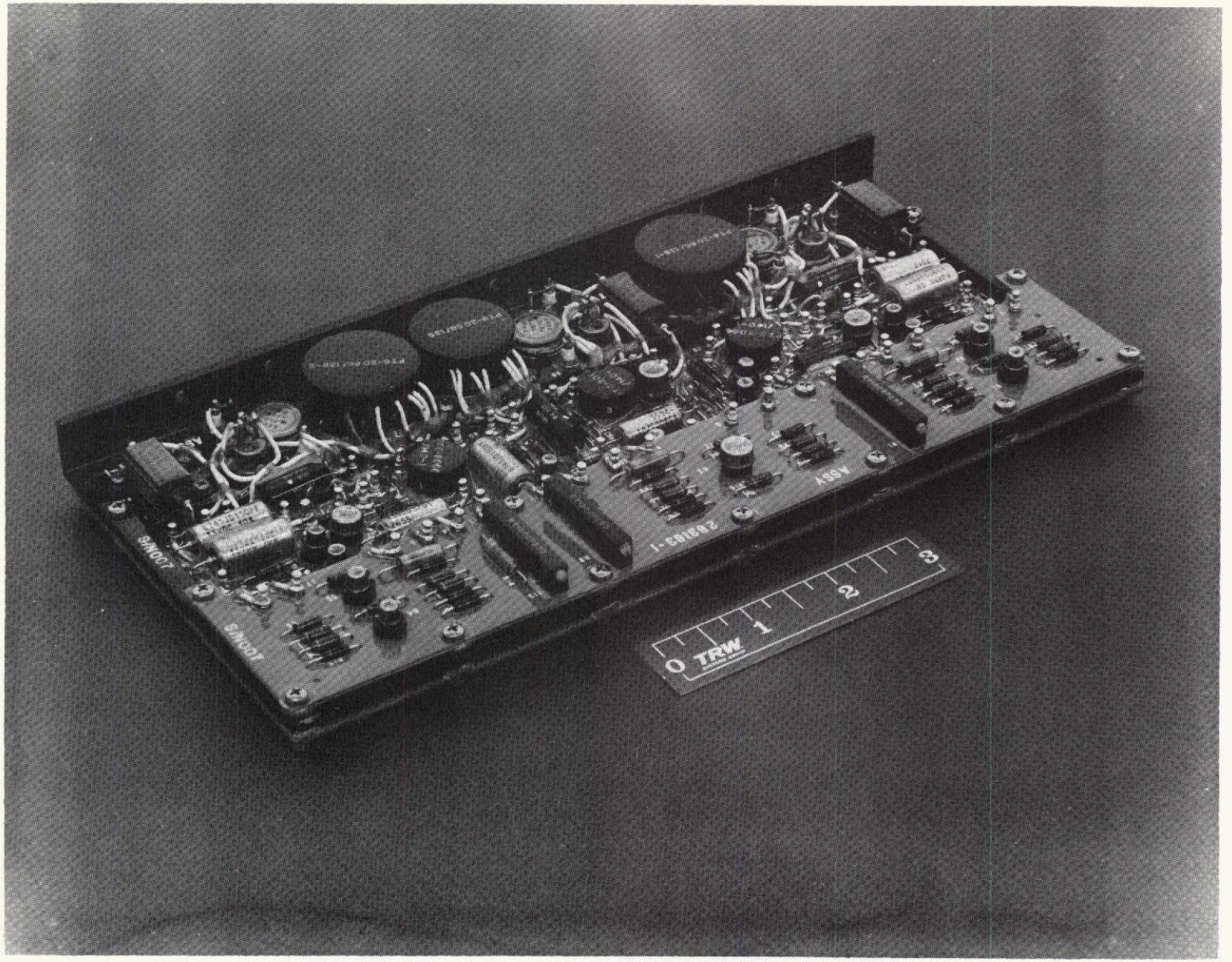


Figure 8. A Fabricated Signal-Conditioner Power Supply Board Containing Three Independent Converters

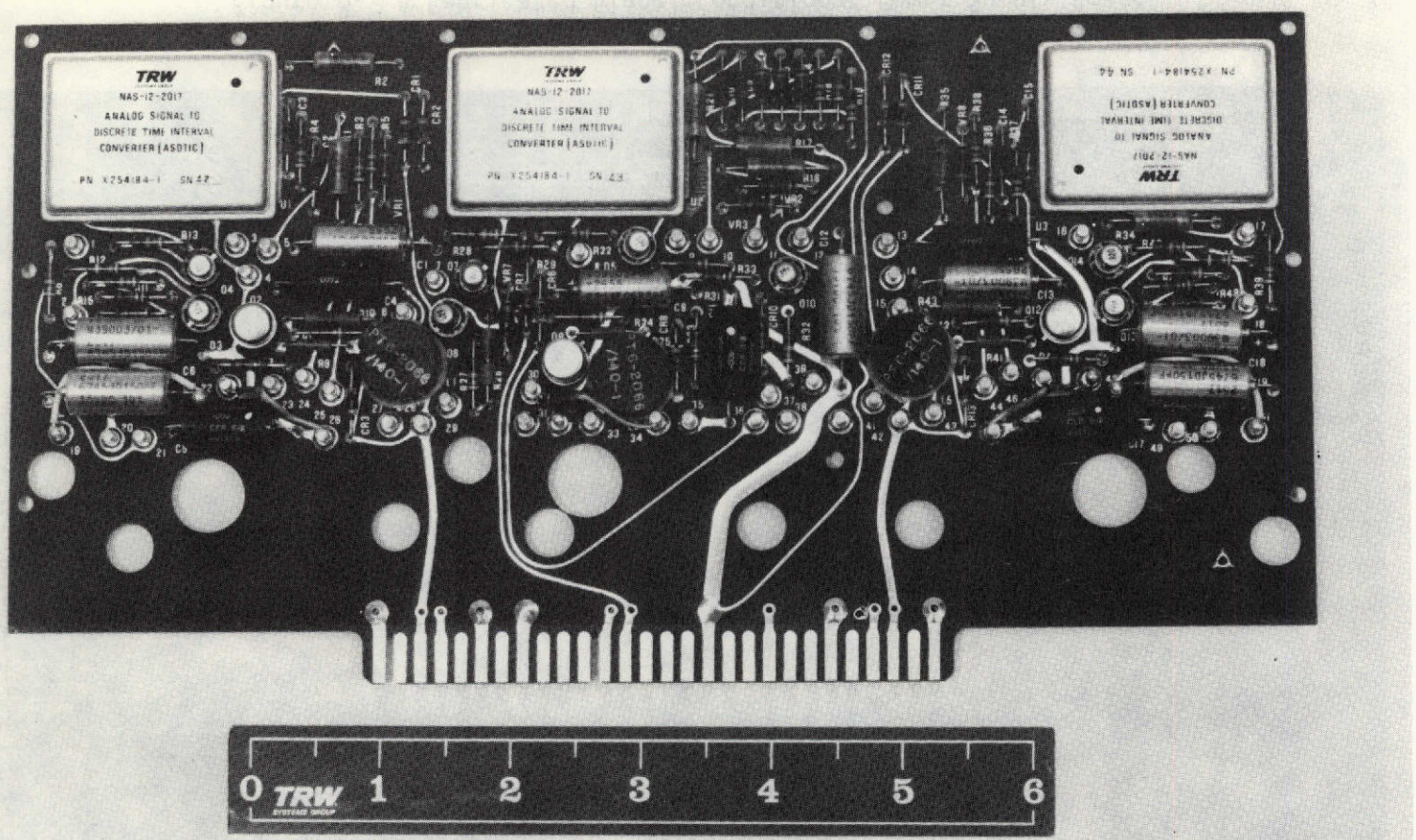


Figure 9. Converter Modules Sheet Metal Base
With the Baby Board Removed

9. CONCLUSIONS

The microminiaturized ASDTIC module was applied successfully to control three dc to dc converters of the signal conditioner power supplies within the Brayton Cycle electrical subsystem.

Eight converter boards, each containing three independent dc to dc converters, were built, tested, and delivered to NASA Lewis Research Center.

The successful application of the ASDTIC module resulted in superb static and dynamic performances of each converter. For example, a $\pm$0.05% output voltage regulation was achieved for an input change of 18V to 32V, a load change of open to full load (10W), and a temperature range of -55°C to +85°C.

The application not only substantiated the soundness of the two-loop ASDTIC control concept, but it also justified further exploitation with the objective of utilizing fully the inherent merits offered by the two-loop control as applied to converter regulators.

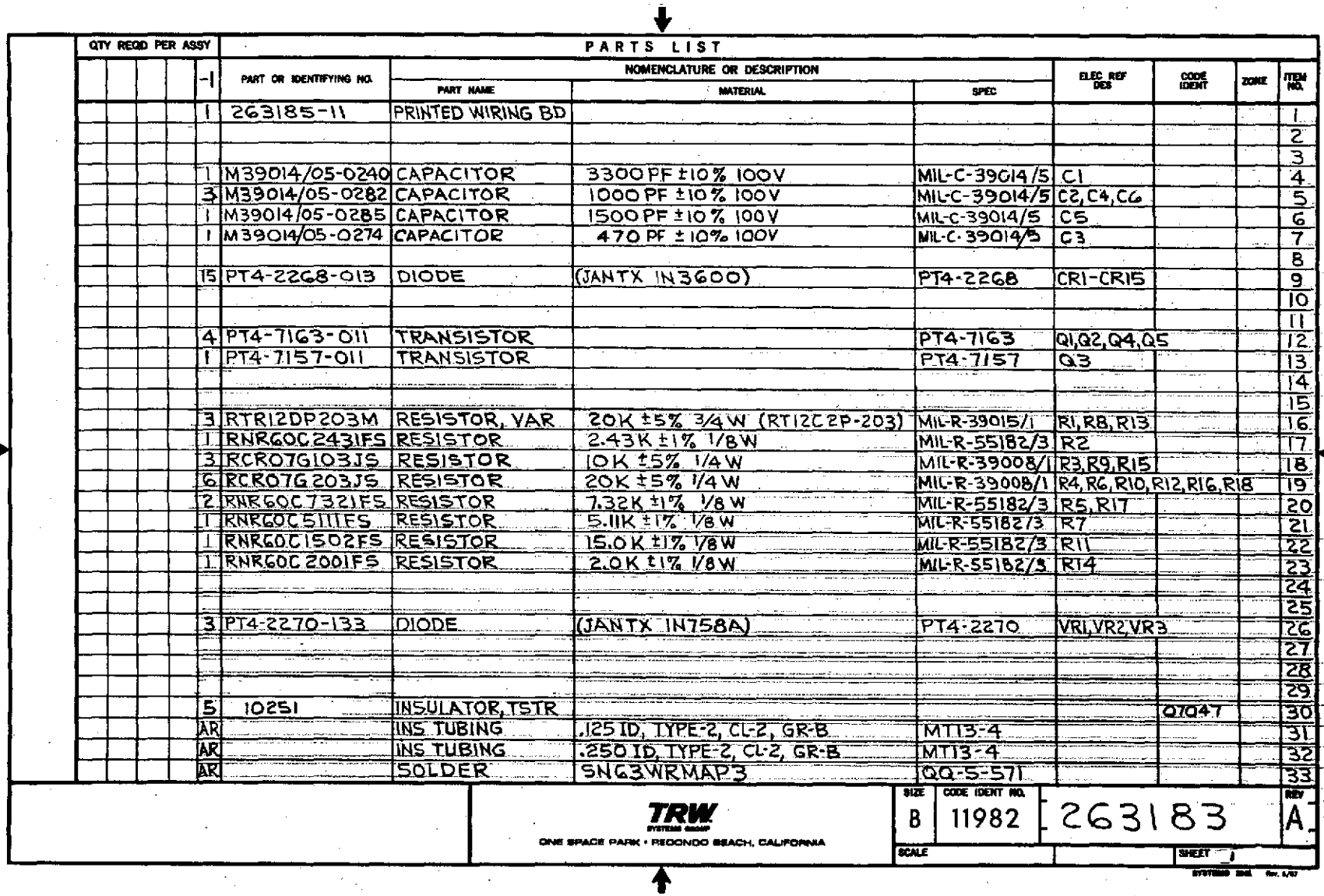
10. APPENDIX

Presented in this appendix is the parts list for the schematic diagram shown in Figure 2. The list on Page 31 describes those components located on the A1 board of Figure 2 (i.e., the baby board). All other power processor electrical parts are given on pages 32 and 33.

Certain semiconductors are described in terms of TRW's in-house parts designation. For convenient cross-reference, the equivalent generic number of these components are given below:

TRW Designation	Generic Equivalent
PT4 - 2273	1N4573A(-03A)
2277	PD9050
2350	UTR294
7157	2N2920
7161	2N3467
7163	2N2222A
7164	2N2907A
7165	2N2851
7176	2N2880

Figure 2. Parts List for A1 Board



PARTS LIST

QTY REQD PER ASSY -1	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION: PART NAME	MATERIAL	SPEC	ELEC REF DES	CODE IDENT	ZONE	ITEM NO.
1	263185-11	PRINTED WIRING BD						1
								2
								3
1	M39014/05-0240	CAPACITOR	3300 PF ±10% 100V	MIL-C-39014/5	C1			4
3	M39014/05-0282	CAPACITOR	1000 PF ±10% 100V	MIL-C-39014/5	C2, C4, C6			5
1	M39014/05-0285	CAPACITOR	1500 PF ±10% 100V	MIL-C-39014/5	C5			6
1	M39014/05-0274	CAPACITOR	470 PF ±10% 100V	MIL-C-39014/5	C3			7
								8
15	PT4-2268-013	DIODE	(JANTX 1N3600)	PT4-2268	CR1-CR15			9
								10
								11
4	PT4-7163-011	TRANSISTOR		PT4-7163	Q1, Q2, Q4, Q5			12
1	PT4-7157-011	TRANSISTOR		PT4-7157	Q3			13
								14
								15
3	RTR12DP203M	RESISTOR, VAR	20K ±5% 3/4 W (RT12C2P-203)	MIL-R-39015/1	R1, R8, R13			16
1	RNR60C2431FS	RESISTOR	2.43K ±1% 1/8 W	MIL-R-55182/3	R2			17
3	RCR07G103JS	RESISTOR	10K ±5% 1/4 W	MIL-R-39008/1	R3, R9, R15			18
6	RCR07G203JS	RESISTOR	20K ±5% 1/4 W	MIL-R-39008/1	R4, R6, R10, R12, R16, R18			19
2	RNR60C7321FS	RESISTOR	7.32K ±1% 1/8 W	MIL-R-55182/3	R5, R17			20
1	RNR60C5111FS	RESISTOR	5.11K ±1% 1/8 W	MIL-R-55182/3	R7			21
1	RNR60C1502FS	RESISTOR	15.0K ±1% 1/8 W	MIL-R-55182/3	R11			22
1	RNR60C2001FS	RESISTOR	2.0K ±1% 1/8 W	MIL-R-55182/3	R14			23
								24
								25
3	PT4-2270-133	DIODE	(JANTX 1N758A)	PT4-2270	VR1, VR2, VR3			26
								27
								28
								29
5	10251	INSULATOR, TSTR				07047		30
AR		INS TUBING	.125 ID, TYPE-2, CL-2, GR-B	MIL-I-23053/4				31
AR		INS TUBING	.250 ID, TYPE-2, CL-2, GR-B	MIL-I-23053/4				32
AR		SOLDER	SN63WRMAP3	QQ-S-571				33

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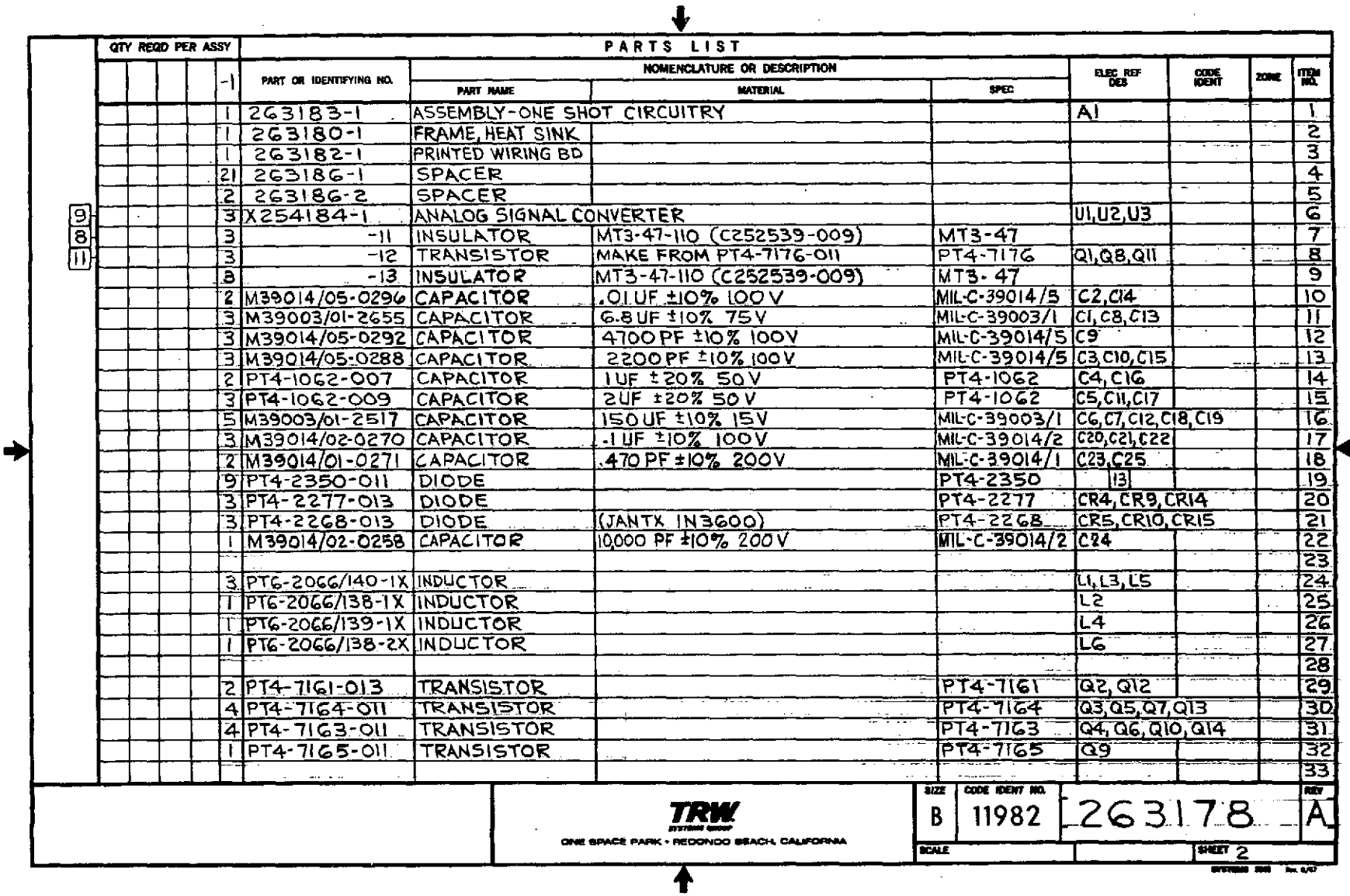

PARTS LIST

QTY REQD PER ASSY -1	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION: PART NAME	MATERIAL	SPEC	ELEC REF DES	CODE IDENT	ZONE	ITEM NO.
1	263183-1	ASSEMBLY-ONE SHOT CIRCUITRY			A1			1
1	263180-1	FRAME, HEAT SINK						2
1	263182-1	PRINTED WIRING BD						3
21	263186-1	SPACER						4
2	263186-2	SPACER						5
3	X254184-1	ANALOG SIGNAL CONVERTER			U1,U2,U3			6
3	-11	INSULATOR	MT3-47-110 (C252539-009)	MT3-47				7
3	-12	TRANSISTOR	MAKE FROM PT4-7176-011	PT4-7176	Q1,Q8,Q11			8
8	-13	INSULATOR	MT3-47-110 (C252539-009)	MT3-47				9
2	M39014/05-0296	CAPACITOR	.01 UF ±10% 100 V	MIL-C-39014/5	C2,C14			10
3	M39003/01-2655	CAPACITOR	6.8 UF ±10% 75V	MIL-C-39003/1	C1,C8,C13			11
3	M39014/05-0292	CAPACITOR	4700 PF ±10% 100V	MIL-C-39014/5	C9			12
3	M39014/05-0288	CAPACITOR	2200 PF ±10% 100 V	MIL-C-39014/5	C3,C10,C15			13
2	PT4-1062-007	CAPACITOR	1 UF ±20% 50 V	PT4-1062	C4,C16			14
3	PT4-1062-009	CAPACITOR	2 UF ±20% 50 V	PT4-1062	C5,C11,C17			15
5	M39003/01-2517	CAPACITOR	150 UF ±10% 15V	MIL-C-39003/1	C6,C7,C12,C18,C19			16
3	M39014/02-0270	CAPACITOR	.1 UF ±10% 100V	MIL-C-39014/2	C20,C21,C22			17
2	M39014/01-0271	CAPACITOR	.470 PF ±10% 200V	MIL-C-39014/1	C23,C25			18
9	PT4-2350-011	DIODE		PT4-2350	13			19
3	PT4-2277-013	DIODE		PT4-2277	CR4,CR9,CR14			20
3	PT4-2268-013	DIODE	(JANTX 1N3600)	PT4-2268	CR5,CR10,CR15			21
1	M39014/02-0258	CAPACITOR	10,000 PF ±10% 200V	MIL-C-39014/2	C24			22
								23
3	PT6-2066/140-1X	INDUCTOR			L1,L3,L5			24
1	PT6-2066/138-1X	INDUCTOR			L2			25
1	PT6-2066/139-1X	INDUCTOR			L4			26
1	PT6-2066/138-2X	INDUCTOR			L6			27
								28
2	PT4-7161-013	TRANSISTOR		PT4-7161	Q2,Q12			29
4	PT4-7164-011	TRANSISTOR		PT4-7164	Q3,Q5,Q7,Q13			30
4	PT4-7163-011	TRANSISTOR		PT4-7163	Q4,Q6,Q10,Q14			31
1	PT4-7165-011	TRANSISTOR		PT4-7165	Q9			32
								33

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Parts List for Figure 2. (A1 Board Not Included)

Parts List for Figure 2 (A1 Board Not Included) (Cont'd)

PARTS LIST

QTY REQD PER ASSY -1	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION: PART NAME	MATERIAL	SPEC	ELEC REF DES	CODE IDENT	ZONE	ITEM NO.
1	RNR60C2801FS	RESISTOR	2.8K ±1% 1/8W	MIL-R-55182/3	R1			34
1	RNR60C1302FS	RESISTOR	13.0K ±1% 1/8W	MIL-R-55182/3	R2			35
6	RCR07G513JS	RESISTOR	51K ±5% 1/4W	MIL-R-39008/1	R3,R5,R18,R20,R36,R38			36
10	RCR07G103JS	RESISTOR	10K ±5% 1/4W	MIL-R-39008/1	14			37
2	RCR07G113JS	RESISTOR	11K ±5% 1/4W	MIL-R-39008/1	R6, R39			38
6	RCR07G101JS	RESISTOR	100 OHM ±5% 1/4W	MIL-R-39008/1	R7,R15,R23,R31,R40,R48			39
2	RWR81S1R00FP	RESISTOR	1 OHM ±1% 1W (RW81U1R00F)	MIL-R-39007/9	R8, R41			40
2	RCR07G202JS	RESISTOR	2K ±5% 1/4W	MIL-R-39008/1	R9, R42			41
2	RWR80S1101FP	RESISTOR	1.1K ±1% 2W (RW80U1101F)	MIL-R-39007/8	R10, R43			42
2	RCR07G242JS	RESISTOR	2.4K ±5% 1/4	MIL-R-39008/1	R12, R45			43
2	RER65FR299P	RESISTOR	.299 OHM ±1% 10W (REG5GR299)	MIL-R-39009/1	R14, R47			44
1	RNR60C2001FS	RESISTOR	2.0K ±1% 1/8W	MIL-R-55182/3	R16			45
1	RNR60C1822FS	RESISTOR	18.2K ±1% 1/8W	MIL-R-55182/3	R17			46
1	RNR60C1741FS	RESISTOR	1.74K ±1% 1/8W	MIL-R-55182/3	R21			47
2	RCR07G102JS	RESISTOR	1K ±5% 1/4W	MIL-R-39008/1	R24, R33			48
1	RWR81S2R00FP	RESISTOR	2 OHM ±1% 1W (RW81U2R00F)	MIL-R-39007/9	R25			49
1	RWR80S1501FP	RESISTOR	1.5K ±1% 2W (RW80U1501F)	MIL-R-39007/8	R26			50
1	RCR07G153JS	RESISTOR	15K ±5% 1/4	MIL-R-39008/1	R29			51
1	RER65FR604P	RESISTOR	.604 OHM ±1% 10W (REG5GR604)	MIL-R-39009/1	R30			52
1	RNR60C6041FS	RESISTOR	6.04K ±1% 1/8W	MIL-R-55182/3	R34			53
1	RNR60C5111FS	RESISTOR	5.11K ±1% 1/8W	MIL-R-55182/3	R35			54
1	RCR07G512JS	RESISTOR	5.1K ±5% 1/4W	MIL-R-39008/1	R44			55
								56
								57
								58
								59
7	PT4-2273-031	DIODE		PT4-2273	VR1-VR6,VR8			60
1	PT4-2270-093	DIODE	(JANTX 1N754A)	PT4-2270	VR7			61
								62
								63
11	10251	INSULATOR				07047		64
6	1480C	TERMINAL				88245		65
								66

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11. REFERENCES

[1]. F. C. Schwarz, "Power Processing," NASA SP-244, 1971.

[2]. F. C. Schwarz, "Analog Signal to Discrete Time Interval Converter (ASDTIC)," U. S. Patent 3659184, 1972.

[3]. A. D. Schoenfeld and K. K. Schuegraf, "Design, Development and Fabrication of a Microminiaturized Electronic Analog Signal to Discrete Time Interval Converter," TRW Systems, NASA CR-120905, 1972.

[4]. V. R. Lalli and A. D. Schoenfeld, "ASDTIC Duty-Cycle Control for Power Converters," NASA TM x-68066.