2-8

BASIC MEMORY MODULE

FINAL REPORT

IBM

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FINAL REPORT

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TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

Section 1

INTRODUCTION AND SUMMARY

This report describes the construction and electrical characterization of the 4096 × 2-bit Basic Memory Module (BMM) designed and fabricated by IBM under Contract NAS8-30460. This module was developed for the Space Ultrareliable Modular Computer (SUMC) program. A separate report[1] presents the overall fault-tolerant memory organization recommended for using the BMMs in this application.

All contract requirements and performance goals for the BMM were met. Thirty-two modules were provided, along with a special card (described in Appendix A) that permits testing individual BMMs using conventional laboratory test equipment.

The module, described in detail in Section 2, uses four 2K × 1-bit N-channel FET, random-access memory (RAM) chips, called "array chips," and two sense amplifier chips, mounted and interconnected on a ceramic substrate. Figure 1-1 shows the module with its ceramic cover removed. In Appendix A, Figure A-1 shows the BMM with the cover in place.

Four 5% tolerance power supplies are required. At the module, the address, chip select, and array select lines require a 0-8.5 V MOS signal level. The data output, read-strobe, and write-enable lines operate at TTL levels.

Although the module is organized as 4096 × 2 bits, it can be used in a 8196 × 1-bit application with appropriate external connections, as shown in Figure 1-2. A 4096 × 1-bit organization can be obtained by depopulating chips.

Originally, only one dual sense-amplifier chip was planned, with each amplifier servicing a single output bit. It was subsequently determined that the dual sense amplifier chip of interest had on-chip wiring in the output stage that precluded the 8196 × 1-bit organization. Thus, it was necessary to use two of these sense amplifier chips with only one of the dual amplifiers actually connected and powered on each chip. This was the only change from the originally proposed BMM.

Table 1-1 summarizes the most important measured performance characteristics of the device for selected conditions. Only room temperature functional testing was required, but a rather comprehensive electrical characterization was actually performed. The results are presented in Section 3.

The memory and sense amplifier chips are standard IBM commercial devices, and the ceramic substrate and interconnection techniques are standard IBM commercial technology. Inherently then, the BMM has the advantages of a large chip production base, low cost, and an immense amount of relevant field experience to support its projection of high reliability.

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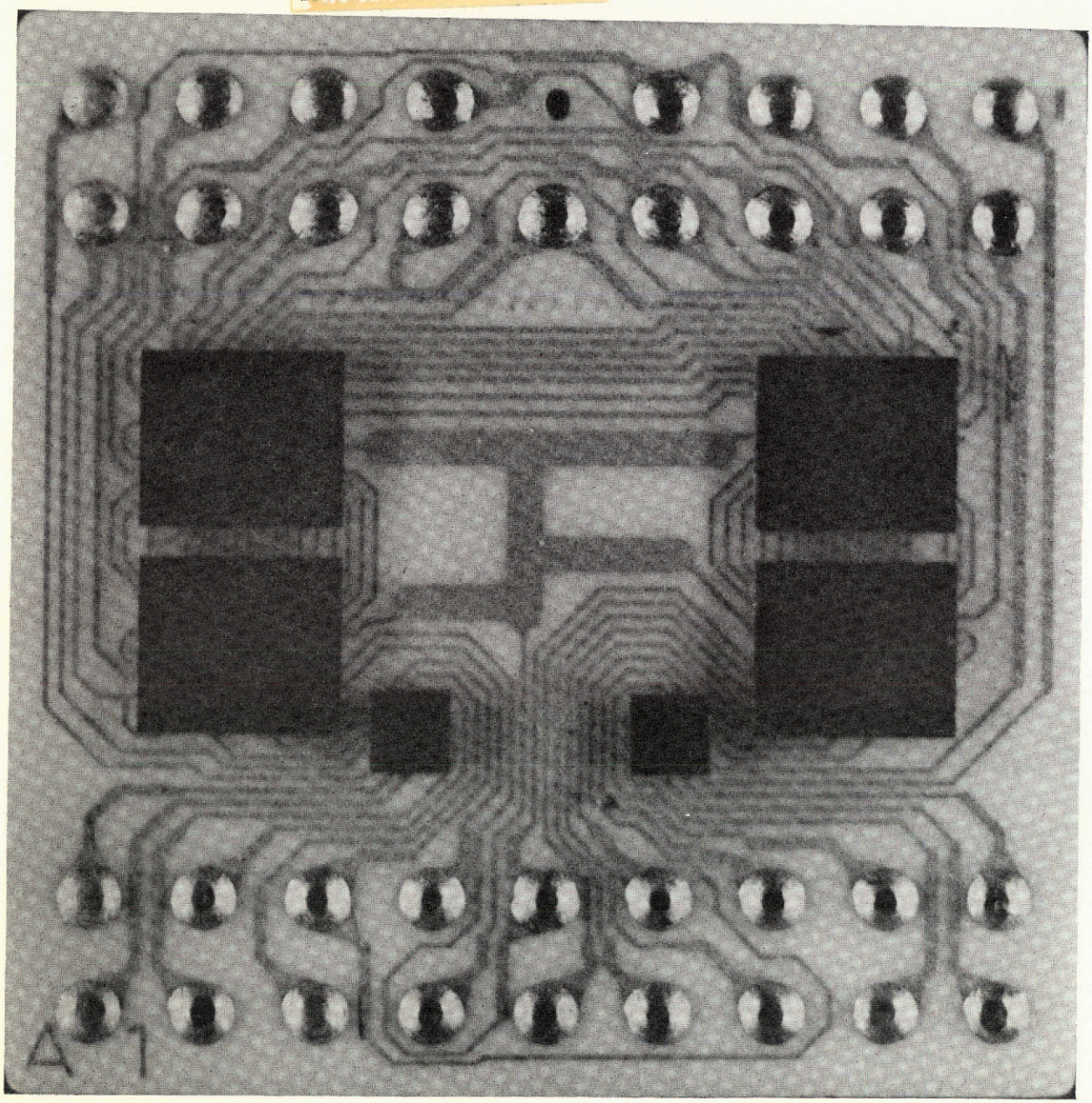
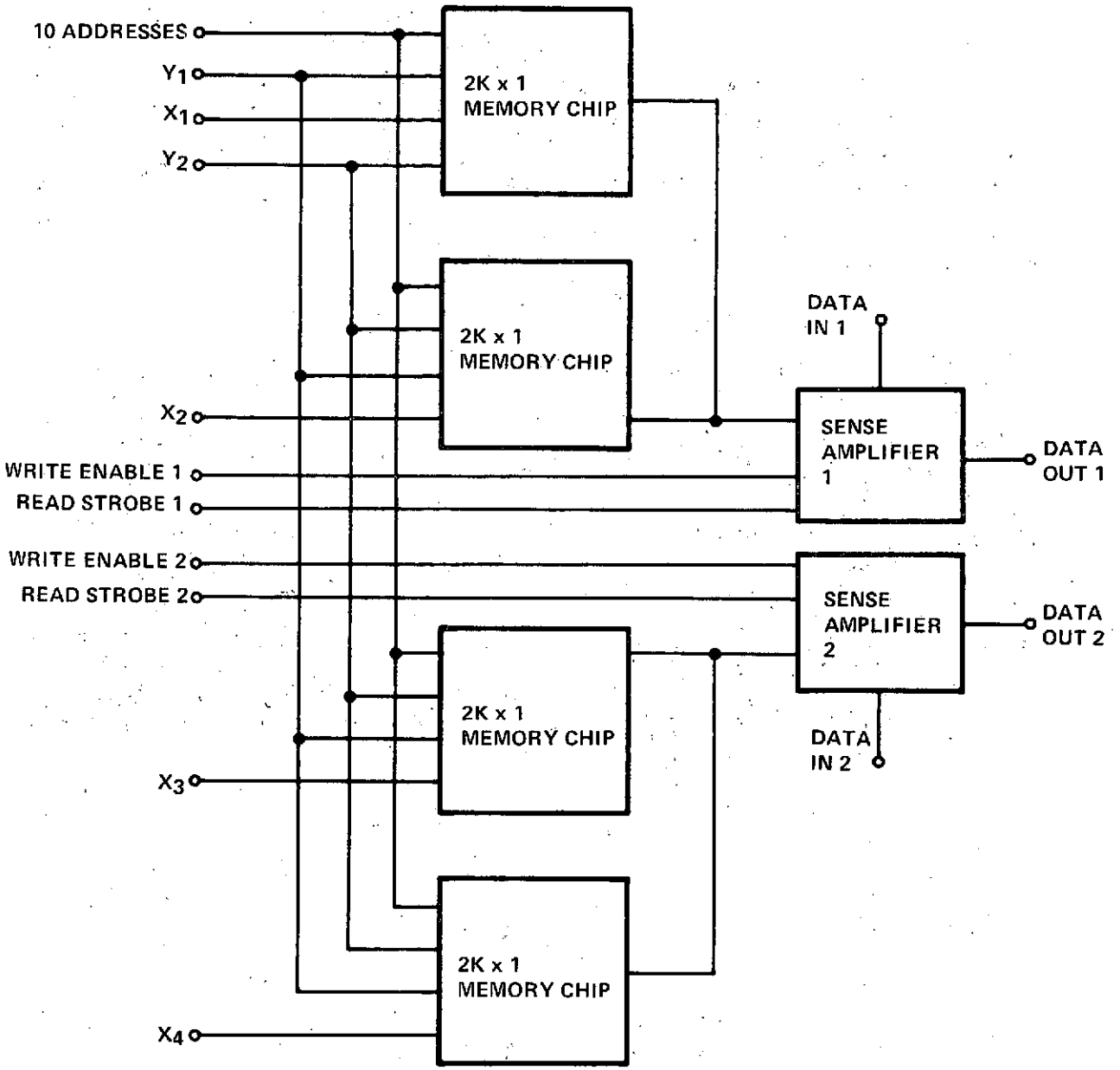
[1] McCarthy, C.E., "SUMC Memory Design Study," 15 March 1974, IBM, Huntsville, Alabama.



(Flecks showing on the substrate are epoxy residue after cover removal)

Figure 1-1. BMM Substrate and Chip Layout



4K x 2 CONNECT X_1 & X_3
CONNECT X_2 & X_4

8K x 1 CONNECT IN 1 & IN 2
CONNECT OUT 1 & OUT 2

X_{1-4} ARE CHIP SELECT LINES

$Y_{1,2}$ SELECT 1K ARRAYS WITHIN EACH 2K CHIP

Figure 1-2. Basic Memory Module Block Diagram

Table 1-1

SUMMARY OF IMPORTANT MEASURED BMM CHARACTERISTICS

Parameter	Test Conditions	Parameter Value	Section Giving Details
Read Access Time From Chip Select (T_{AX})	+35° C, not-strobed, nominal supply voltages	111.7* ns	3.2.1.2
	+125° C, not-strobed, worst-case voltages	166.6* ns	3.2.1.2
	-47° C, not-strobed, worst-case voltages	98.5* ns	3.2.1.2
	+125° C, strobed, worst-case voltages	108.6* ns	3.2.1.3
Read Access Time From Address (T_{AA})	As above	0 to 10 ns greater than T_{AX}	3.2.12, 3.2.1.4
Minimum Write Pulse Width	Worst-case temperature and voltage	≤25 ns	3.2.2
Operating Power	+35° C, 250 ns cycle, nominal voltage, 4K × 2	635* mW	3.5
	+35° C, 250 ns cycle, nominal voltage, 8K × 1	466* mW	3.5
	+125° C, 250 ns cycle, 4K × 2, worst-case voltage	617* mW	3.5
Standby Power	+35° C, 250 ns cycle, 4K × 2, nominal voltages	297* mW	3.5
Capacitance			
Chip Select Line	+35° C	<66 pF	3.4
Array Select Line		<30 pF	
All Others		< 22 pF	

*Average Value
**Extrapolated Value
All Temperatures are Case Temperatures.

Section 2

MODULE DESCRIPTION

The functional and electrical performance of the module is presented after the mechanical and semiconductor chip descriptions.

2.1 CONSTRUCTION AND MECHANICAL DESCRIPTION

The BMM module is a hermetically sealed alumina ceramic multiple chip carrier 0.948 inch square by 0.150 high. The ceramic base is fired with 36 holes to accept pins which are swaged in place after a circuit pattern has been applied to the top of the substrate. These pins protrude from the bottom surface of the substrate at 0.100 inch spacing, with two 9-pin rows located toward one edge of the ceramic base and two 9-pin rows toward the opposite edge. The area on the top of the substrate between the rows of pins is utilized for chip sites and an alumina ceramic sealing cap.

The chip carrier metallization is a single-layer, sputtered-and-etched metal film. Electrical connections to the chip and to the pins are formed by solder joints to exposed copper pads, which are part of the wiring pattern. Each semiconductor chip has solder pads on one surface that are matched by the solder pads on the chip carrier. Chips are placed on these sites and are held in place with flux until reflowed in an oven.

This flip chip approach, using proven controlled-collapse solder joint technology, permits several chips to be attached simultaneously. If necessary, faulty individual chips can be replaced. This attachment technology and earlier versions of it have been used in numerous high reliability aerospace systems. Its reliability has been demonstrated over billions of operating hours in IBM commercial equipment.

Module sealing is accomplished by epoxy sealing an alumina cap over the metallized lines running out to the pins. The hermetic seal is made in the area between the pins and the chip sites, avoiding the problem of leakage around the pins into the sealed cavity.

This type of sealing technique was chosen for four primary reasons: (1) tests to date indicate it can meet or exceed the seal leakage and environmental requirements of MIL-STD-883, "Test Methods and Procedures for Microelectronics"; (2) it is easily repairable in a manner which does not degrade the rest of the module; (3) both the initial and replacement seals are relatively inexpensive; (4) epoxy sealing eliminates the possibility of conductive particle entrapment within the packages, which could result from a solder type sealing process.

The lid can be removed by raising module temperature to a point where the epoxy softens enough to allow the lid to be lifted. This temperature is low enough not to degrade the solder joints, metallization, or chips within the module. The module is resealed by cleaning the surface area on the module and repeating the initial sealing procedure. Repair and reseal of the module offers higher yields with resulting reduced module production costs.

The ceramic substrates were manufactured by the IBM Systems Products Division, East Fishkill, New York. The memory and sense amplifier chips are standard commercial chips manufactured at the Burlington, Vermont, facility of that division. The substrate design, module assembly, and electrical testing were performed at the Federal Systems Division in Owego, New York. All memory chips were from a single lot, B050677. The lot make-up of the sense amplifier chips is not known. No module or chip burn-in was conducted.

2.2 CHIP ELECTRICAL DESCRIPTIONS

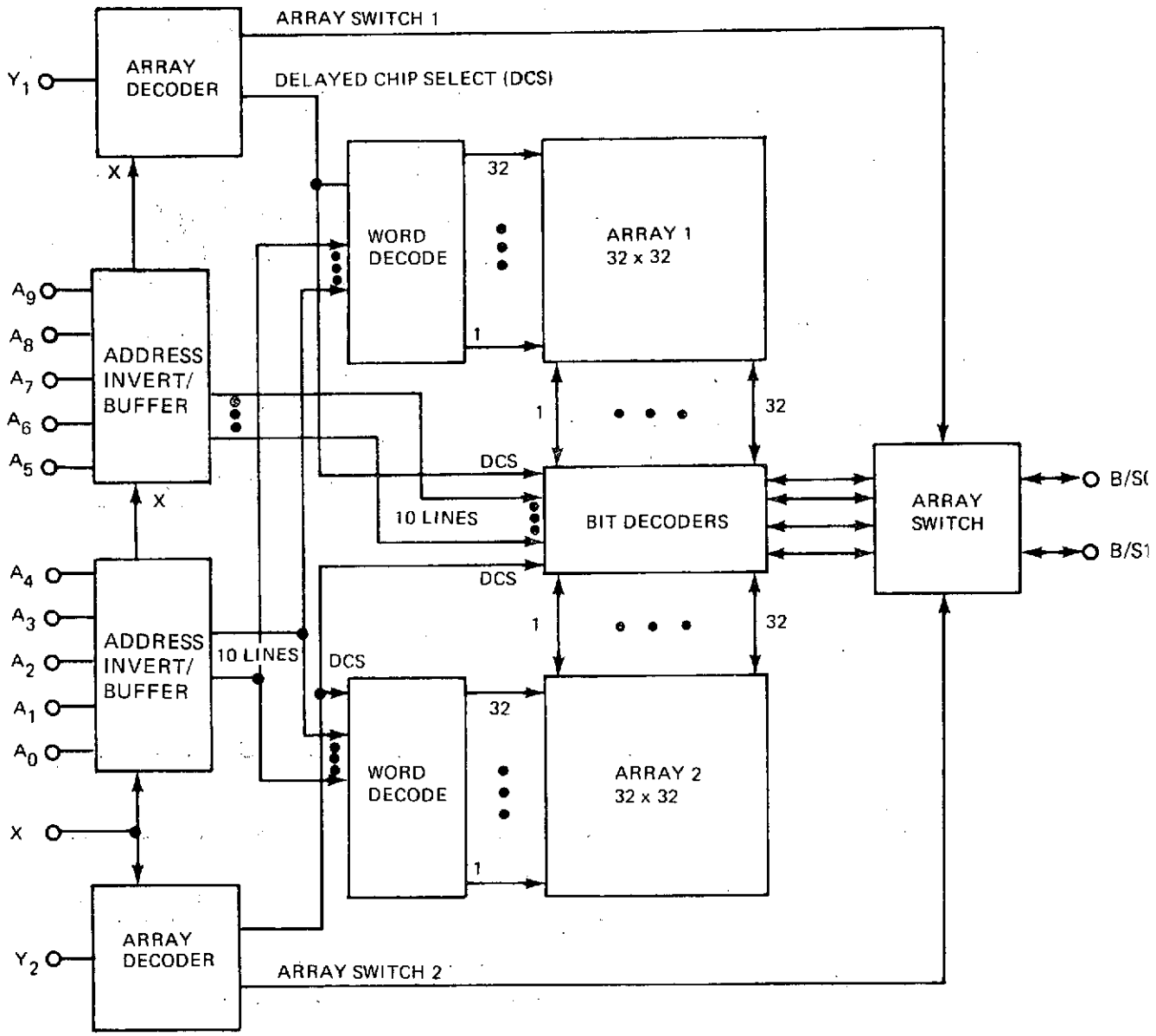
The BMM contains four identical memory chips and two identical sense amplifier chips. Their characteristics are presented here.

2.2.1 MEMORY CHIP

The memory chip utilizes a high performance, state-of-the-art N-channel FET process. Chips are passivated with ion trapping glass, resulting in hermetic seals at the chip level. A block diagram of this chip is shown in Figure 2-1. The 2048-bit chip is divided into two 32×32 arrays. Each array has its own word decoders, Delayed Chip Select (DCS) generator, and array decoder. The bit decoders and address inverter/buffers are common to both arrays.

To select a cell, ten addresses are applied. When the address is valid the X-pulse (chip select) can rise. This allows buffered and inverted address signals to be generated. The Delayed Chip Select pulse powers the outputs of the selected word and bit decoders, which select one cell in each array. The array decoders generate the AND function of X and Y_1 or X and Y_2. The resultant signal selects one of the two array bits which is connected to the data input/output lines B/S0 and B/S1. The fall of X initiates an on-chip restore operation which returns internal chip lines to appropriate standby levels.

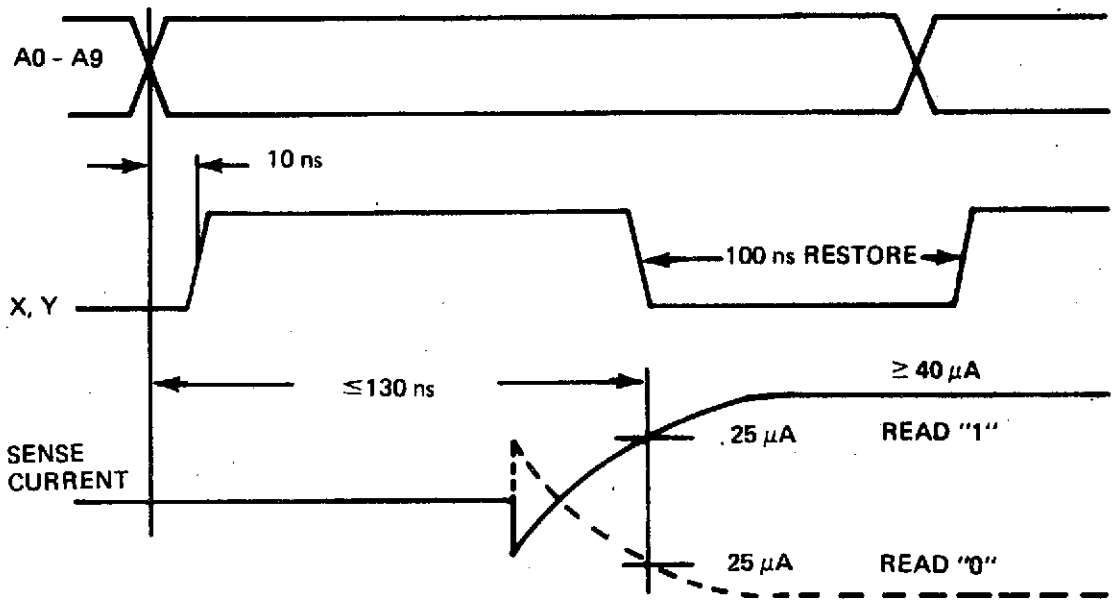
The timing diagrams for this chip are shown in Figure 2-2. Address (A_0 - A_9) and select input levels (X, Y_1 and Y_2) are 0 to 8.5 volts, nominally. The maximum down-level is 0.4 V and the minimum up-level is 7.5 V. Circuits which can be used to generate these signals from TTL levels are described in Section 2.4.3. In the BMM, the B/S0 and B/S1 input/output terminals are connected on the substrate directly to the differential sense amplifier. Since no module pin connections to this point are available, no direct characterizing measurements of memory chip outputs could be made.



B/S0 AND B/S1 ARE THE DIFFERENTIAL SIGNAL LINES FOR THE SINGLE BIT.

Figure 2-1. Block Diagram for a Single 2K × 1-Bit Memory Chip

READ CYCLE



WRITE CYCLE

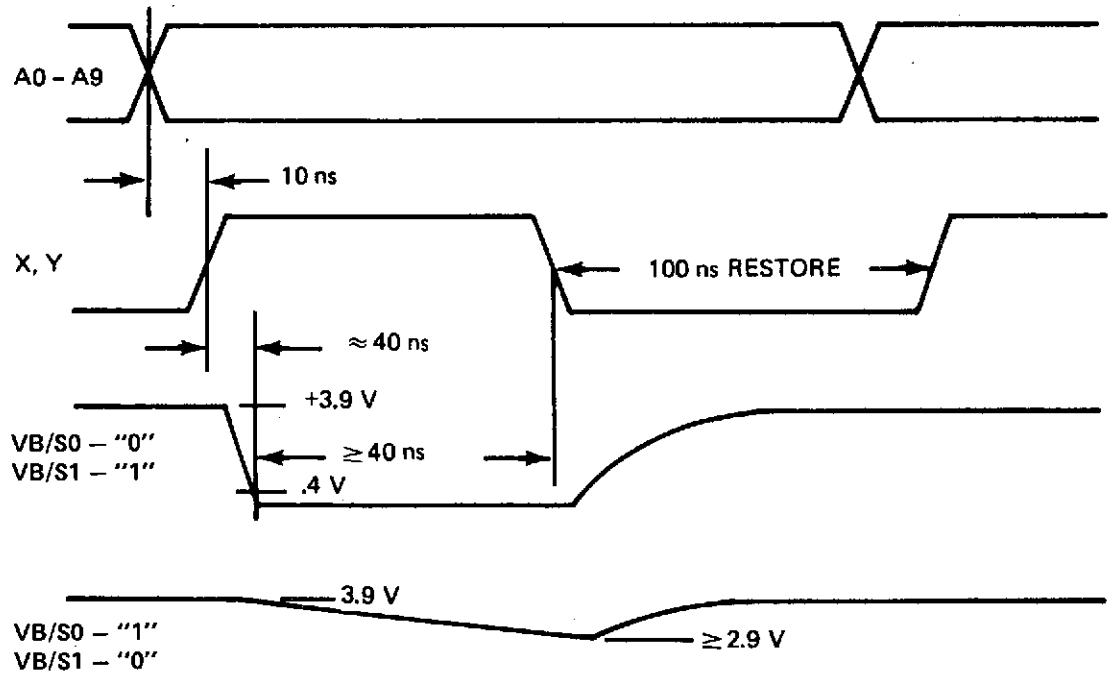


Figure 2-2. Memory Chip Timing

The nominal differential output sense current is at least 40 microamperes.

Three power supply voltages are required:

V_H = 8.5V ±5%

V_N = -3.0V ±5%

V_B = 3.3V ±5%

A fourth chip voltage, $V_L \approx 2$ V, optionally can be used to obtain lower speed and power. To achieve the desired speed and avoid the need for generating a fourth voltage, this option was not used. The commitment of the chip to the option is made through substrate metallization, thus it is unchangeable for the present BMM. While a V_L pin does exist on the module, it does not alter speed or power. This pin should be connected to V_B.

The nominal power for a memory chip is about 70 mW unselected and 150 mW selected.

2.2.2 SENSE AMPLIFIER/BIT DRIVER CHIP

The sense amplifier is a dual bipolar monolithic chip, although only one amplifier per chip is used in the BMM. As connected in Figure 1-2, it performs the two functions of sensing differential current from the memory chips during read operations, and driving the appropriate bit line to ground during write operations. A logic diagram of this circuit is shown in Figure 2-3.

During Read, the Write input is held down to a disable the bit driver. The sense amplifier maintains the bit sense lines (B/S0 and B/S1) at appropriate voltage levels (3-4 V), detects the differential current from the memory chips, and converts this signal to a TTL-compatible voltage level. The signal is gated by Data-Strobe (Read-Strobe) to the Data-Out pin of the module. This output consists of an open-collector TTL output stage to allow for external dotting. It can drive main memory unit internal bus, which requires sinking 15 mA at 0.4 V. The Data Input and Read-Strobe inputs are standard TTL inputs, each constituting two TTL loads. The Read-Strobe may be tied off to a fixed on-level, in which case data is available at the Data Out pin after the normal read access time.

During Write, one of the bit sense lines is pulsed to ground, while the other line is maintained at a high level by the sense amplifier. The Write signal must be at a logic "1" level. After Write operations, the bit sense line is returned to a high voltage level (approximately 3.8 V) by the sense amplifier. The Write Input appears as four TTL loads.

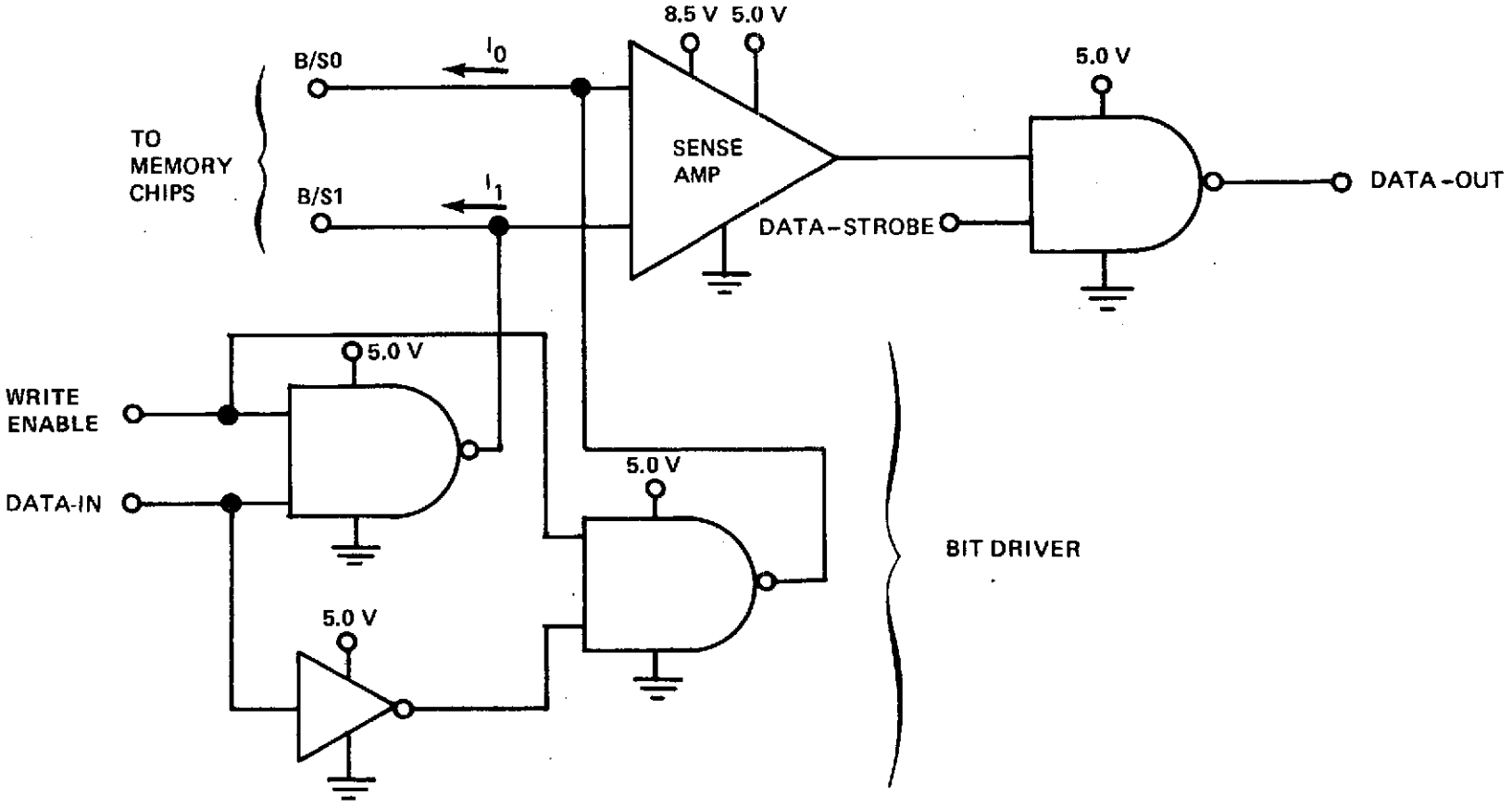


Figure 2-3. Single Sense Amplifier/Bit Driver

Typical AC performance for this part is shown in Figure 2-4. Inaccessibility of the differential input lines in the BMM precluded characterizing measurements of the sense amplifier alone.

This chip requires two supply voltages:

V_H = 8.5V ±5%

V_{CC} = 5.0V ±5%

At 50% duty cycle, the chip power dissipation for one sense amplifier is about 85 mW. The nominal differential sense current is 25 microamperes and the maximum is 300 microamperes.

2.3 MODULE ELECTRICAL DESCRIPTION

The four memory chips and two sense amplifiers are organized in a 4096 × 2-bit configuration, but may be externally connected for use in an 8192 × 1-bit application, as shown in Figure 1-2. Figure 2-5 illustrates the read and write cycle timing of the BMM to obtain an access time of 180 ns in either the 4K × 2 or 8K × 1 configuration. The maximum cycle rate in read operation is 4 MHz. The maximum cycle rate in write operation is 5 MHz.

The address and chip select inputs require logic level swings of 0 - 8.5 V, and are TTL compatible when driven by an open collector output driver pulled up to 8.5 V. High voltage TTL interface drivers described in Section 2.4.3 provide the described level shift for TTL interface with the BMM.

2.3.1 PIN NUMBERING AND FUNCTION

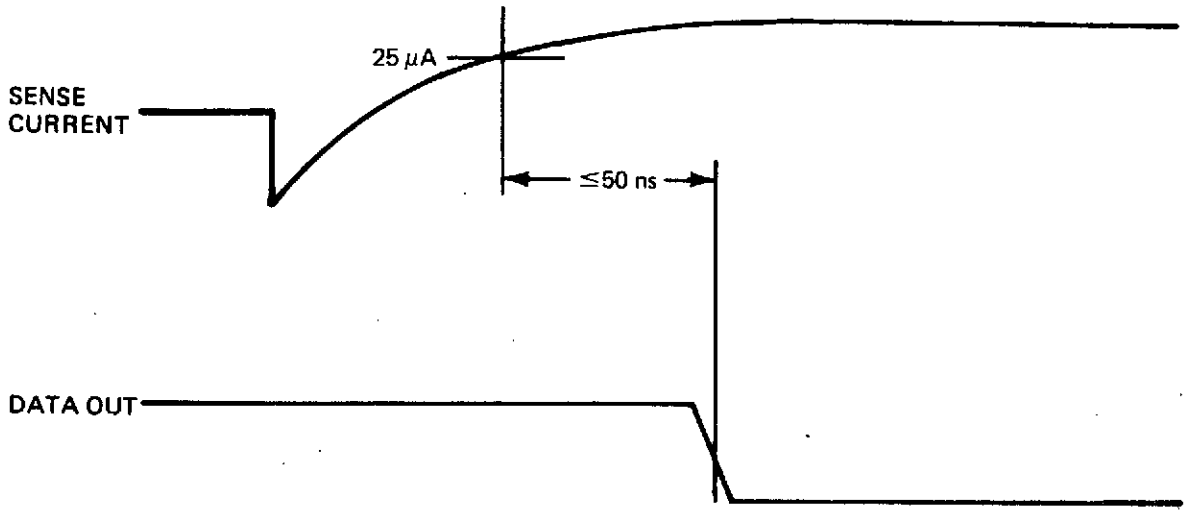
Figure 2-6 defines the module pin numbering (as viewed from the bottom (pin side) of the substrate) and gives the pin functions. Pin A-1 is permanently marked on the substrate. Four V_H pins were used to facilitate substrate wiring and to permit powering down part of the module if desired; they are connected together for normal operation. V_L is normally connected to V_B. In total then, four 5% tolerance power supplies are required; V_H, V_B and V_L, V_N, and V_{CC}.

2.4 INTERFACE REQUIREMENTS

2.4.1 8K × 1 APPLICATION

Figure 2-7 is a block diagram of the interconnections and logic required to implement the 8K × 1 BMM. The interface driver is a 2-input TTL-AND, with high-voltage output, described in Section 2.4.3. The X and Y controls form a matrix of eight 1K segments. The presence of one X and one Y control is required to address one of the 8K segments. The interface drivers and logic will drive all BMMs in a simplex system and are replicated as required in a fault-tolerant system.

READ



WRITE

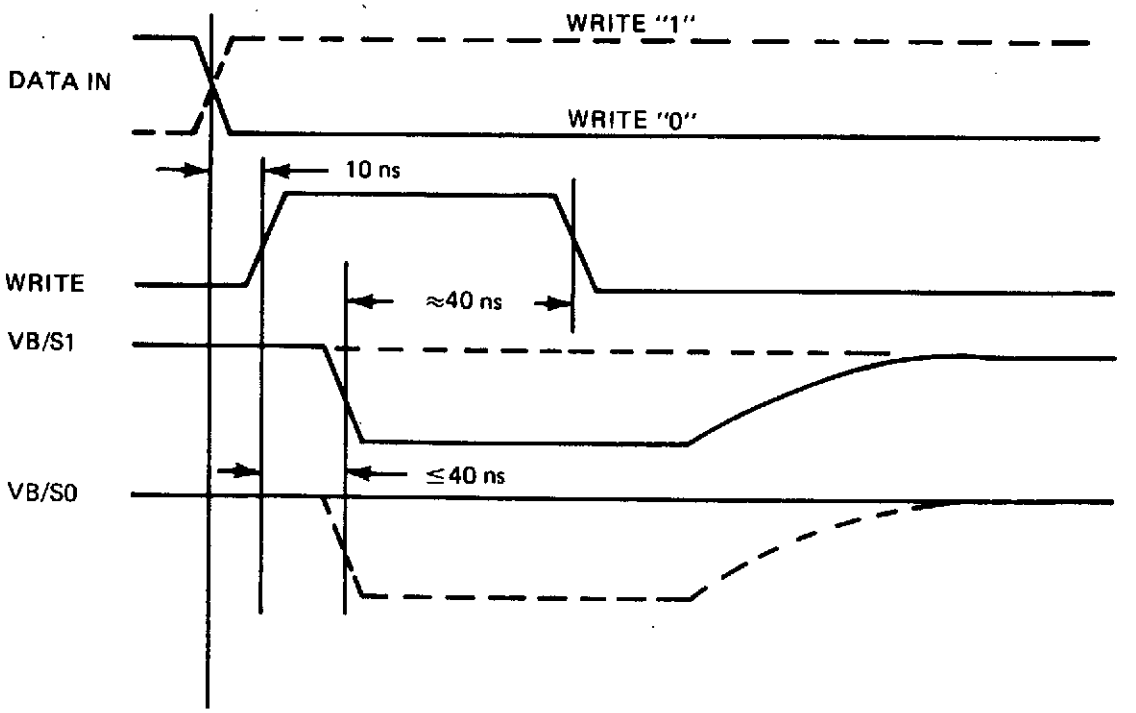
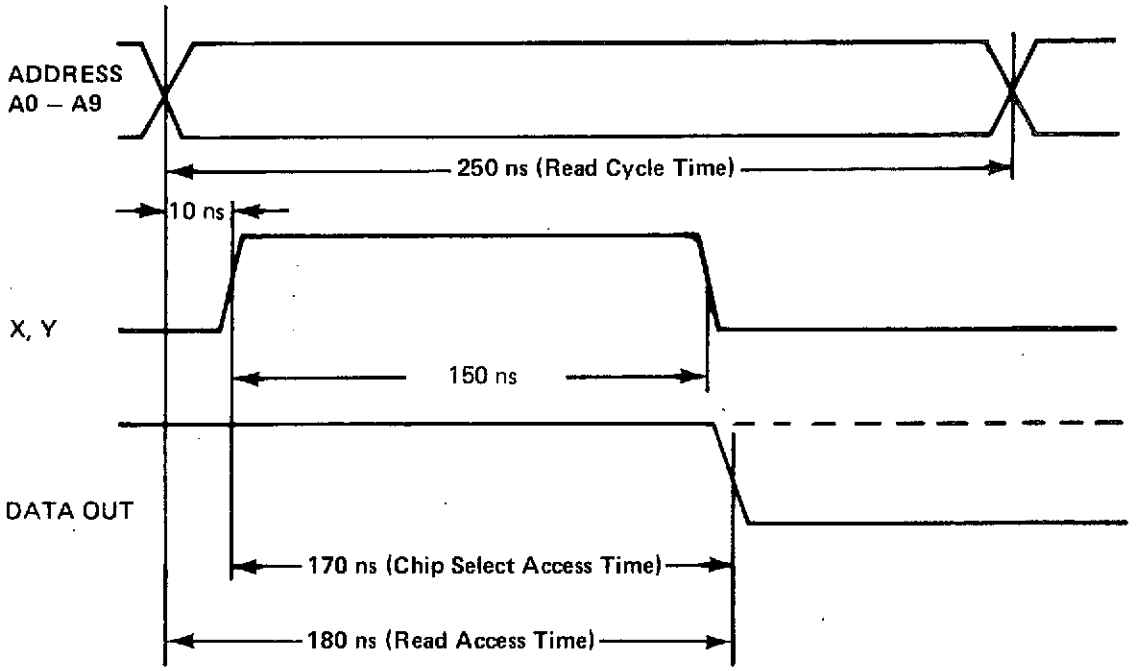


Figure 2-4. Sense Amplifier/Bit Driver Performance

READ TIMING



WRITE TIMING

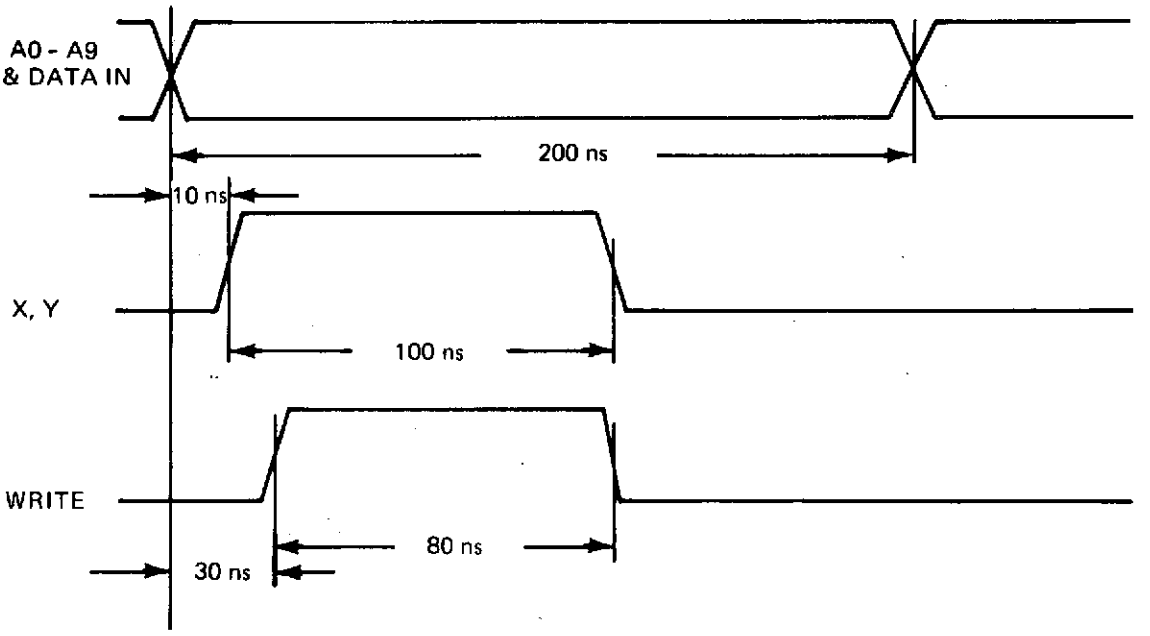
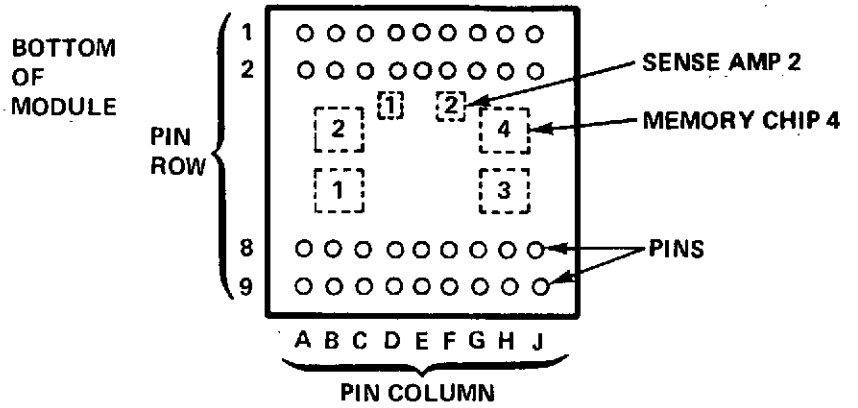


Figure 2-5. BMM Timing Requirements



Pin	Function	Pin	Function
A-1	RS1	A-8	V_H (Sense Amp 1)
B-1	BS2	B-8	V_H (Chips 1 & 2)
C-1	DI1	C-8	WS1
D-1	Ground	D-8	VB (3.3 V)
E-1	Y1	E-8	BS3
F-1	Y2	F-8	BS4
G-1	WS5	G-8	WS2
H-1	WS3	H-8	X3
J-1	RS2	J-8	V_H (Sense Amp 2)
A-2	Ground	A-9	DO1
B-2	WE1	B-9	X2
C-2	V_{CC} (5.0 V)	C-9	X1
D-2	BS1	D-9	BS5
E-2	V_N (-3.0 V)	E-9	Not Used
F-2	WS4	F-9	V_L (3.3 V)
G-2	DI2	G-9	V_H (Chips 3&4)
H-2	WE2	H-9	X4
J-2	Ground	J-9	DO2

Code

X – Chip Select (For Chips 1 to 4)

Y – Array Select (for Array 1 or Array 2 of a Memory Chip)

WS – Word Select
BS – Bit Select
} Address (A0 to A9)

RS – Read – or Data – Strobe
WE – Write Enable
DI – Data In
DO – Data Out
} (for Bit 1 or Bit 2)

V_B, V_{CC}, V_H, V_L, V_N – Supply Voltages

Figure 2-6. BMM Pin-out and Function List

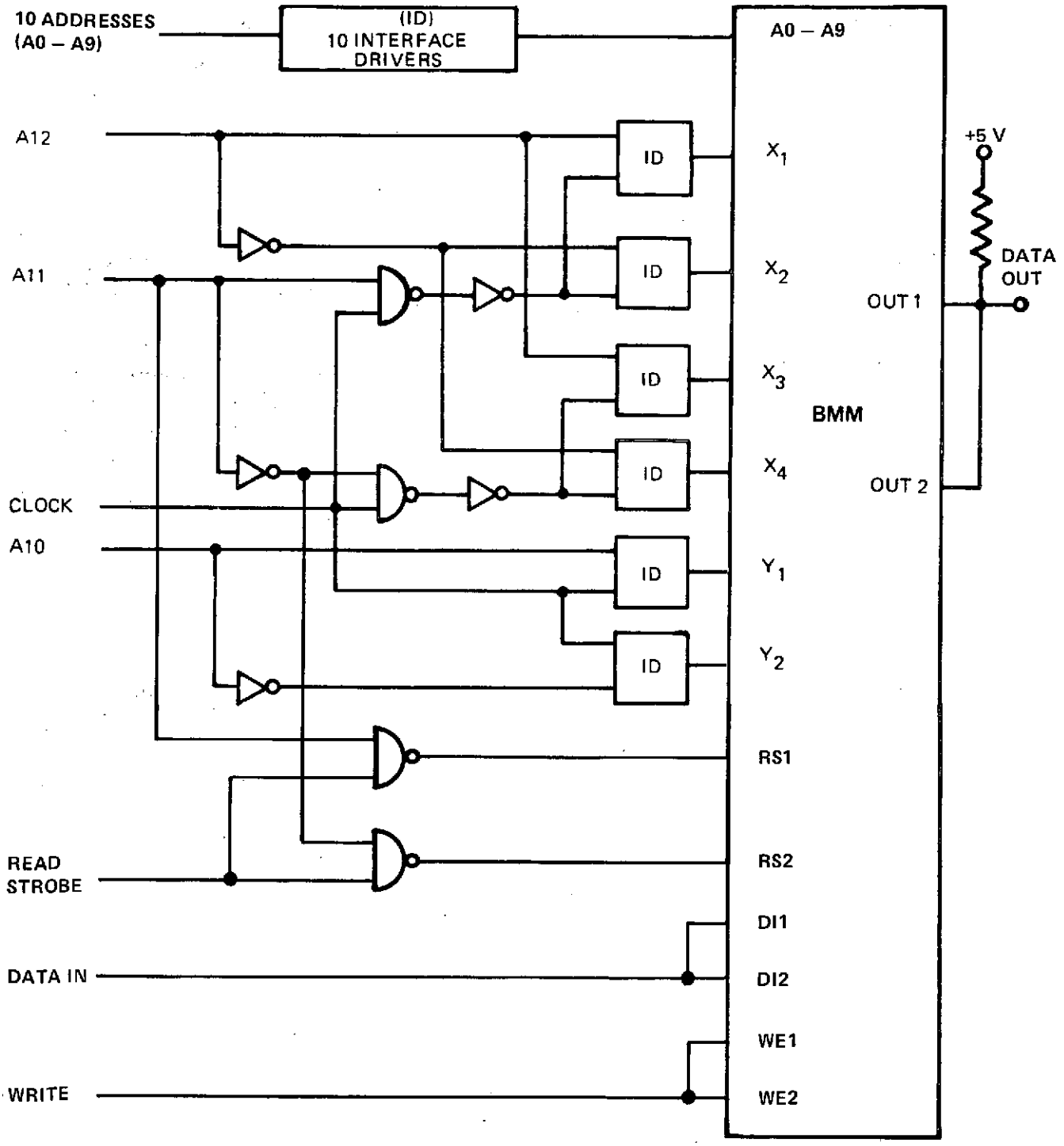


Figure 2-7. 8K × 1 Application

2.4.2 4K × 2 APPLICATION

Figure 2-8 is a block diagram of the interconnections and logic required to implement the 4K × 2 bit BMM. The X and Y controls form two matrices, each having four 1K segments. The presence of one X and one Y control selects two 1K segments. The interface drivers and logic will drive all BMMs in a simplex system, and are replicated as required in a fault-tolerant system.

2.4.3 INTERFACE DRIVER

Interface driver circuitry performs the function of converting TTL signal levels to the 0 - 8.5 V signal levels required to address the memory chip. Two high-performance circuits, which might be used to perform this function, are described in the following.

A bipolar interface driver chip currently being used by IBM for commercial temperature range applications has been tested in order to determine applicability. Tested units exhibited 50% - 50% delays of less than 30 ns at +125°C (worst case temperature), driving a capacitive load of 300 pF. This circuit performs an AND function on its two inputs, which represent one TTL load. Three circuits are available per chip. Chip I/Os are compatible with solder-reflow mounting techniques. The DC power dissipation for this circuit, assuming a 50% duty cycle, is 25 mW/circuit nominal (75 mW/chip). This circuit requires 5.0 V and 8.5 V supply voltages.

A second circuit with potential as the interface driver is under development by Texas Instruments. It is currently being reworked to address a low-temperature oscillation problem. Early prototype circuits have been tested over the MIL-Temp range and exhibited delays of less than 20 ns driving a 300-pF load. Typical DC power dissipation is 45 mW/circuit, with a 50% duty cycle. This circuit performs an invert function on its input, which represents 1.5 TTL loads. A second input can be used to bias the output in a high impedance state. This circuit requires 5.0 V and 12.0 V power supply voltages for operation. This circuit will be packaged in a 16-lead flatpack (four circuits/flatpack).

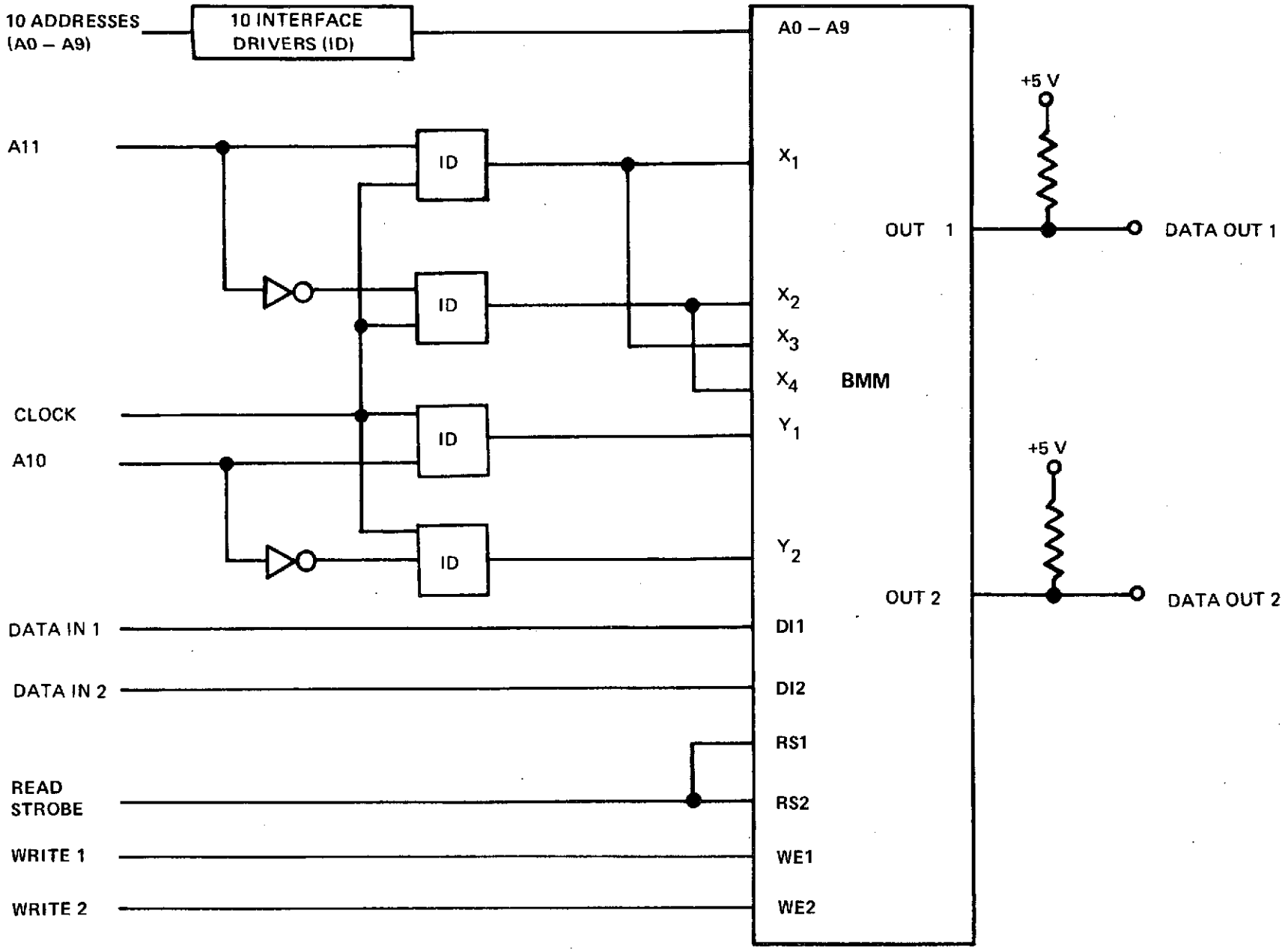


Figure 2-8. 4K × 2 Application

Section 3

MODULE PERFORMANCE MEASUREMENTS

3.1 GENERAL TESTING INFORMATION

A variety of AC and DC measurements were made over the case temperature range of -47° C to +125° C to establish the functionality and to characterize the performance of the BMMs.

The data taken are presented here in summary form for conciseness. The original data sheets have been retained on file and do permit determination of the behavior of any individual sample.

For some important parameters, data was taken on as many as 43 modules. To establish the broadest information base, all available data has been summarized here even though only 32 modules are required. In other cases of less critical or less variable parameters, representative data was taken on only a few samples.

Temperature measurements cited are case temperatures, T_C. The junction-to-case temperature differential at normal operating power was not measured but is estimated at about 6° C. At high temperature, where the failure likelihood was greatest, the estimated junction temperature, T_J, was 131° C, yet performance remained satisfactory. Test equipment limitations, however, permitted achieving an operating low temperature of only -47° C at the case, or (estimated) -41° C at the junction. Performance was generally improved at low temperature and there was no particular indication that a difficulty might be encountered at T_J = -55° C. Five samples in fact did successfully "cold start" at a junction temperature of -50° C or lower.

Functional and AC measurements were made using the COMPUTEST Model V-200 "VENTURE" Memory Tester. This high speed functional exerciser provides programmable power supplies, clock and timing pulses, and data pattern generators. It includes all necessary interface drivers, test sequencing, and error logging circuitry. An appropriate sequence of tests was defined and programmed (on magnetic tape) specifically for the BMM. In operation, the proper timing signals are established and, with the sample at a given temperature, the power supplies program to nominal voltages; then, the sample is exercised with a series of eight complex data patterns*. Each pattern exercises each bit with at least one read and write operation. Multiple patterns are more likely to reveal subtle bit faults. Any bit errors are automatically detected. Upon successful completion of this sequence, it is repeated for each of four additional worst-case power supply margins (the "box corners" of V_H ±5% and V_N ±5%).

*Load/Read, Addwrex, Walk Data, Ping Pong, Surround Disturb, Adjacent Disturb, Data Complement, and Half Data Complement.

3.2 AC MEASUREMENTS

3.2.1 READ ACCESS TIME

The read access time was measured by exercising the BMM in the manner described in Section 3.1 but with the Read Strobe enabled continually. The position of the VENTURE tester's error sensing strobe in the BMM timing cycle was varied until the time of accurate output data availability was established. Measurement of the error strobe time relative to the rise of the chip select (X) or address (A) pulses defined the Chip Select Access Time, T_{AX}, or the Address Access Time, T_{AA}. Measurements were normally reproducible to ±1 ns.

Since the VENTURE was time programmed in accordance with Figure 2-5, $T_{AA} = T_{AX} + 10$ ns. Inadvertantly, T_{AX} rather than T_{AA} was measured, and $T_{AX} = 180$ ns (rather than 170 ns) was used as reference condition for tests such as the power supply "SHMOOS." This is not a great problem since:

- The conventional T_{AA} can accurately be determined as $T_{AX} + 10$ ns
- As will be discussed in Section 3.2.1.4, the 10 ns interval may not be necessary; thus, T_{AA} would converge to the T_{AX} value used. That is, T_{AX} is the more fundamental and controlling access time.
- Major parameter variations are not expected for only a 10 ns variation in the reference condition.

Separate tests and circuit considerations have established V_H and V_N to be the most critical power supplies, thus the five margin conditions used were for these supplies. The conditions are listed in Table 3-1.

Table 3-1

POWER SUPPLY MARGINS

Margin	V_H (volts)	V_N (volts)	V_B, V_L (volts)	V_{CC} (volts)
1 (nominal)	8.5	-3.0	3.3	5.0
2	8.92	-2.85		
3	8.08	-2.85		
4	8.08	-3.15		
5	8.92	-3.15		

For all AC tests the sample was mounted in a zero-insertion force socket on a special test card. Temperature control was maintained within ±2° C by a Temptronix Thermal Spot Probe in direct contact with the top of the sample, with temperature monitoring done at the bottom of the sample.

To facilitate tester operation, a 300-ns cycle was used instead of 250 ns, where it would not compromise the parameter data involved.

The loading at the BMM Data Output was 100 pF to ground, with a 1-kΩ pull-up resistor to +5 V.

To ensure that reported data can always be correlated with the original measurements, all data will be presented in terms of T_{AX}, as measured.

3.2.1.1 Worse Case Margin for T_{AX}

Table 3-2 is based on a survey of five BMMs, and indicates that Margin 4 causes the worst-case (longest) T_{AX}, except at -46° C where conditions are worst for the nominal power supply voltage.

Table 3-2

WORST-CASE MARGIN IDENTIFICATION

Power Supply Margin	Average T_{AX} (ns)		
	T_C = -46° C	T_C = +37° C	T_C = +126° C
1 (nominal)	101.2*	111.2	161.8
2	85.4	110.8	159.2
3	92.4	113.6	164.0
4	97.6	114.8*	165.0*
5	85.4	110.8	159.8
*Worst case			

The effect of a variation in V_L, the memory array cell power supply, was also checked. Over the full temperature range, the access time was constant within ±1 ns for 1.9 V ≤ V_L ≤ 3.6 V, when V_B, V_H, and V_N were at nominal voltages.

3.2.1.2 Temperature Dependence of T_{AX}

Table 3-3 summarizes the measured temperature dependence of the chip select access time, T_{AX}. Figure 3-1 is a plot of this data.

Table 3-3

T_{AX} TEMPERATURE DEPENDENCE

Case Temperature (°C)	Power Supply Condition*	Access Time, T_{AX} (ns)			Number of Samples
		Average	Standard Deviation	Maximum Value Observed	
-47	Nom.	98.5	8.4	108	38
-47	WC	103.2	7.2	111	43
+35	Nom.	111.7	3.0	119	38
+35	WC	115.4	3.1	125	43
+85	Nom.	138.3	5.8	155	33
+85	WC	140.9	5.8	157	38
+125	Nom.	164.0	7.4	184	37
+125	WC	166.6	7.5	186	42

*Nom. = Nominal Voltages
WC = Worst Case (Margin 4)

Note: Data taken at both the nominal and worst-case margins identified in Section 3.2.1.1.

The BMMs were most sensitive to the Walk Data data pattern at -47° C, but at all other temperatures, Ping Pong was the worst case.

For each module, the access time was measured on each of the two 1K bit arrays of each of the four memory chips, and the largest single value was used as T_{AX} for that module. Figure 3-1 shows that, at +125° C, the overstress (case-to-junction temperature differential) of 6° C results in T_{AX} being about 5 ns longer.

Figure 3-2, which represents the cumulative distribution plots for the individual sample data, establishes that 90% of the samples will meet a specification calling for a T_{AX} of 170 ns without data strobing. This includes the extra 5 ns due to

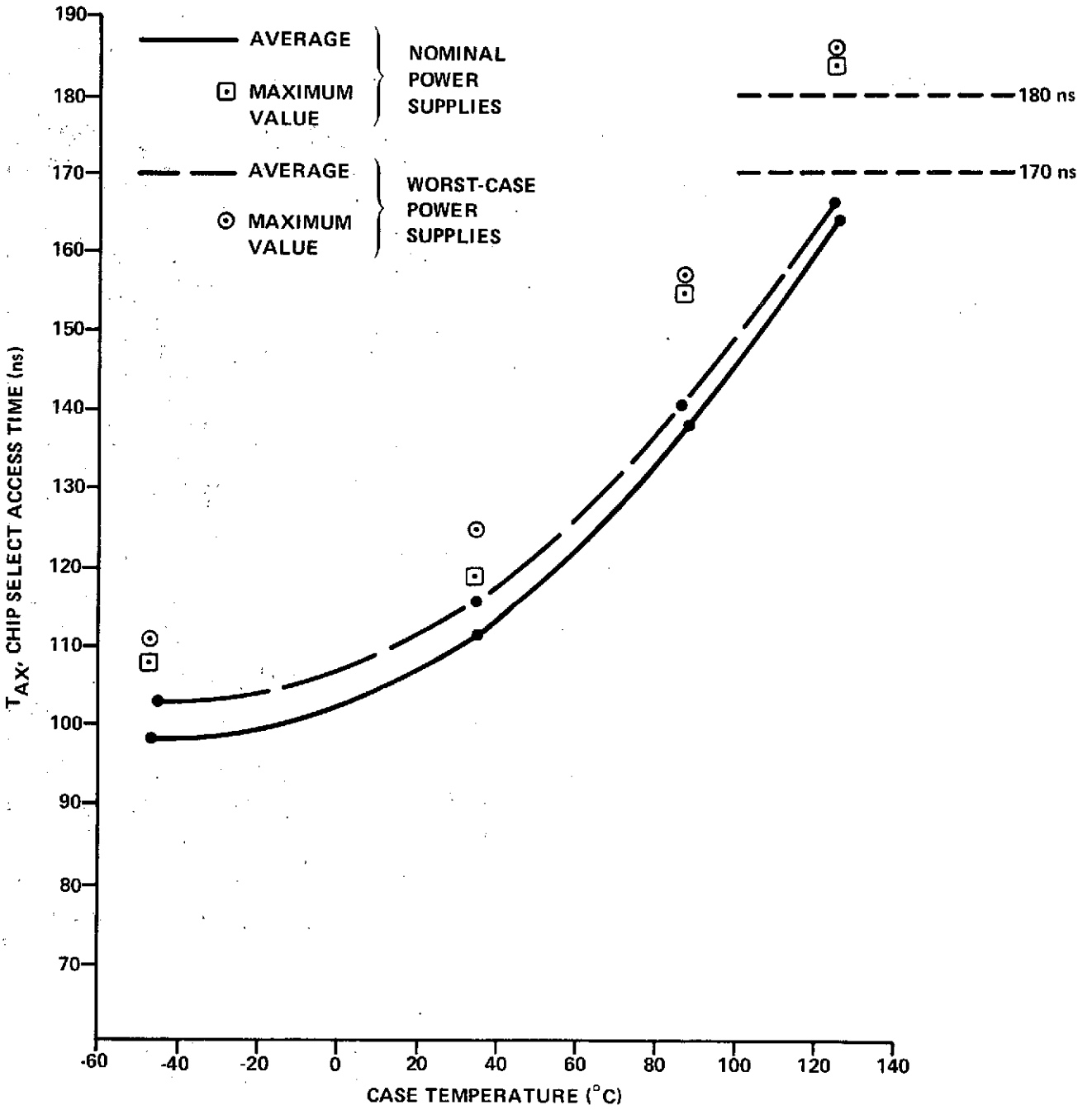


Figure 3-1. T_{AX} Temperature Dependence

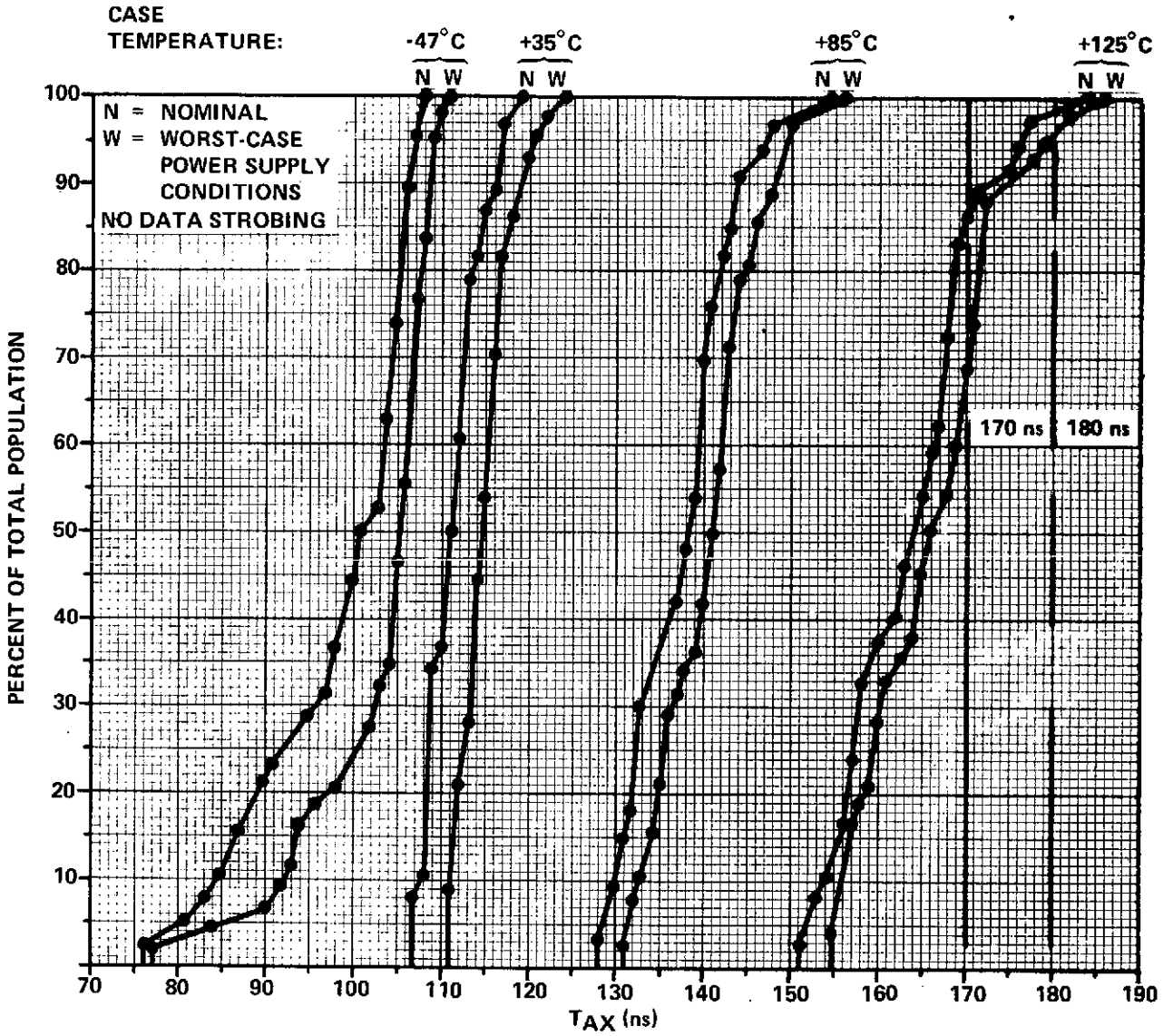


Figure 3-2. Cumulative Distribution of T_{AX}

temperature overstress and considers worst-case temperature and power supply conditions.

As mentioned earlier, T_{AX} may only need to be 180 ns. Only two samples out of 42 at the worst-case power supply margin, and one sample at the nominal margin, exceeded 180 ns. The distributions are fairly normal at +35° C, skewed toward shorter access times at +85° C and +125° C, and skewed toward longer access times at -47° C.

3.2.1.3 Data Strobing

The access time is reduced when the Read Strobe (RS) line is strobed at the time data is desired rather than being enabled continually. This improvement exists because, if the strobe line is always enabled, the Data Out gate output may be low and must be pulled up whenever an output "1" is required. With strobing, however, the Data Out gate output is always high and can be quickly pulled down if an output "0" is required. Thus, the average access time is less with strobing, implying more margin relative to 180 ns.

Table 3-4 compares T_{AX} for five samples, for strobed and unstrobed operation at the worst-case temperature and power supply margin. VENTURE measurement uncertainties increase to perhaps ±5 ns for strobed operations, but this is small compared to the average 58-ns improvement in T_{AX}. Further characterization is required to determine the optimum Read Strobe time position.

Table 3-4

T_{AX} FOR READ STROBED AND UNSTROBED OPERATION

Sample Number	RS Enabled Continually: T_{AX} to a 1 (ns)	RS Strobed: T_{AX} to a 0 (ns)	Difference (ns)
28-6'	172	95	77
28-10	157	107	50
28-12	171	106	65
28-20	157	112	45
28-24	168	115	53
T_C = +125° C, Voltage Margin 4			

3.2.1.4 Timing Delays

Measurements were made on five samples at T_C = -50°, 30°, and 125°C to determine the actual time delay required (refer to Figure 2-5) between the rise of the Address (and Data-In) pulses and

- The rise of the X and Y (chip and array select) pulses. The specified time is 10 ns.
- The rise of the Write Enable pulse. The specified time is 30 ns.

Also, a 20-ns interval is implicitly specified between the rises of Write Enable and the X and Y select pulses.

The BMM operated without error with any or all three delays reduced to zero. Potentially, this can simplify system timing and provide extra access time margin. However, it should not be exploited until after further investigation of the original need for these delays and verification that this behavior is not peculiar to the present chip lots.

3.2.1.5 Chip Select Rise Time Dependence

The chip select (X) line has approximately 62 pF capacitance; thus, depending on the driver used, select pulse rise times may be slower than other signal rise times. T_{AA} was measured on five samples for chip select rise times (1 V to 6 V) from 16 ns to 32 ns. As shown in Figure 3-3, T_{AX} increased more than the rise time changes. Only 30°C, nominal voltage data was taken.

All access time data cited in this report were taken with a chip select rise time of 16 ns. To incorporate the effect of other rise times into the access time, use the relations:

$$T_{AX'} = T_{AX} + \Delta T_{AX}$$

$$\Delta T_{AX} = 1.5\ (T_{RX} - 16) \qquad \text{for } 16 \leq T_{RX} \leq 32 \text{ ns}$$

Where

T_{AX} is the reported read address access time, in ns

$T_{AX'}$ is the desired compensated access time

T_{RX} is the chip select rise time

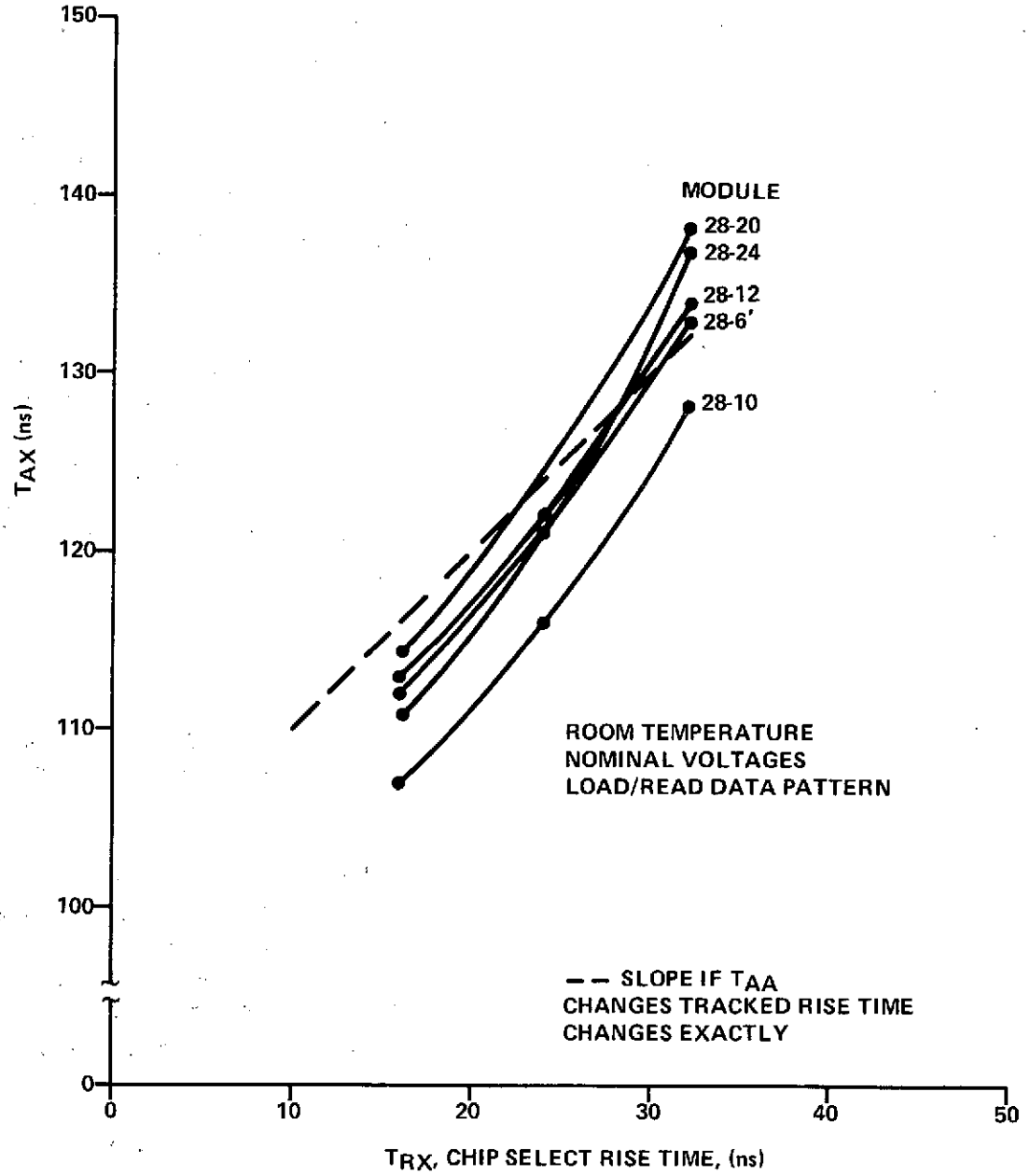


Figure 3-3. Access Time vs Chip Select Rise Time

Although no verifying data exists, this relation is probably reasonable for all voltage margins at room and low temperatures, but it may underestimate the high-temperature access time.

3.2.1.6 Cycle Time Variations

Five samples were functionally checked at worst-case voltages and reduced cycle times, to gain a better understanding of the BMM performance range.

At 250 ns cycle time and +125° C, no bit errors occurred with data strobing. Tester error sensing difficulties prevented proper measurement for the not-strobed case. At 200 ns cycle time, the samples worked in both the strobed and nonstrobed modes at +35° C and -46° C, but bit errors occurred in both modes at +85° C and +125° C.

3.2.1.7 Cold Start

A cold start test was conducted by thermally stabilizing unpowered modules at the lowest attainable temperature. Power was then switched on and a small (but unmeasured) fraction of a second later, normal tester data cycling was initiated. Inability to access the first bit in 180 ns would have constituted a failure. All five samples tested accessed within 180 ns for stabilized junction temperatures of -50° to -53° C. Furthermore, the cold start could be achieved with the zero timing delays discussed in Section 3.2.2.

3.2.1.8 SHMOO Plots

SHMOO plots define the power supply voltage combinations (envelope) for which the BMM achieves a 180-ns chip-select access time. For these tests V_B and V_L, and V_{CC}, were fixed at nominal values, while V_H and V_N were varied.

Initially, one chip from each of five BMMs was used for a SHMOO plot over the temperature range. Although Figure 3-4 has a very typical shape, it actually represents the sample exhibiting the smallest margin. (The numbers at the inner box corners are the 5% margin numbers defined in Section 3.1.) Invariably, high temperature provided the least margin and always at Margin 3. The Read-Strobe input was continually enabled for these tests, except at the indicated +125° C measurement when it was strobed normally.

Strobing always improved the margin, typically providing the equivalent of 0.25 V more margin in V_H or 0.6 V more margin in V_N.

Fourteen additional SHMOOs at +125° C were plotted, providing the basic information shown in Figure 3-5. Of the 19 devices tested, four samples (all included in Figure 3-5) had untypical U-shaped SHMOOs. Also, only four violated the 10% margin box. One sample had about a 6% margin, but in no case was a 5% margin box violated.

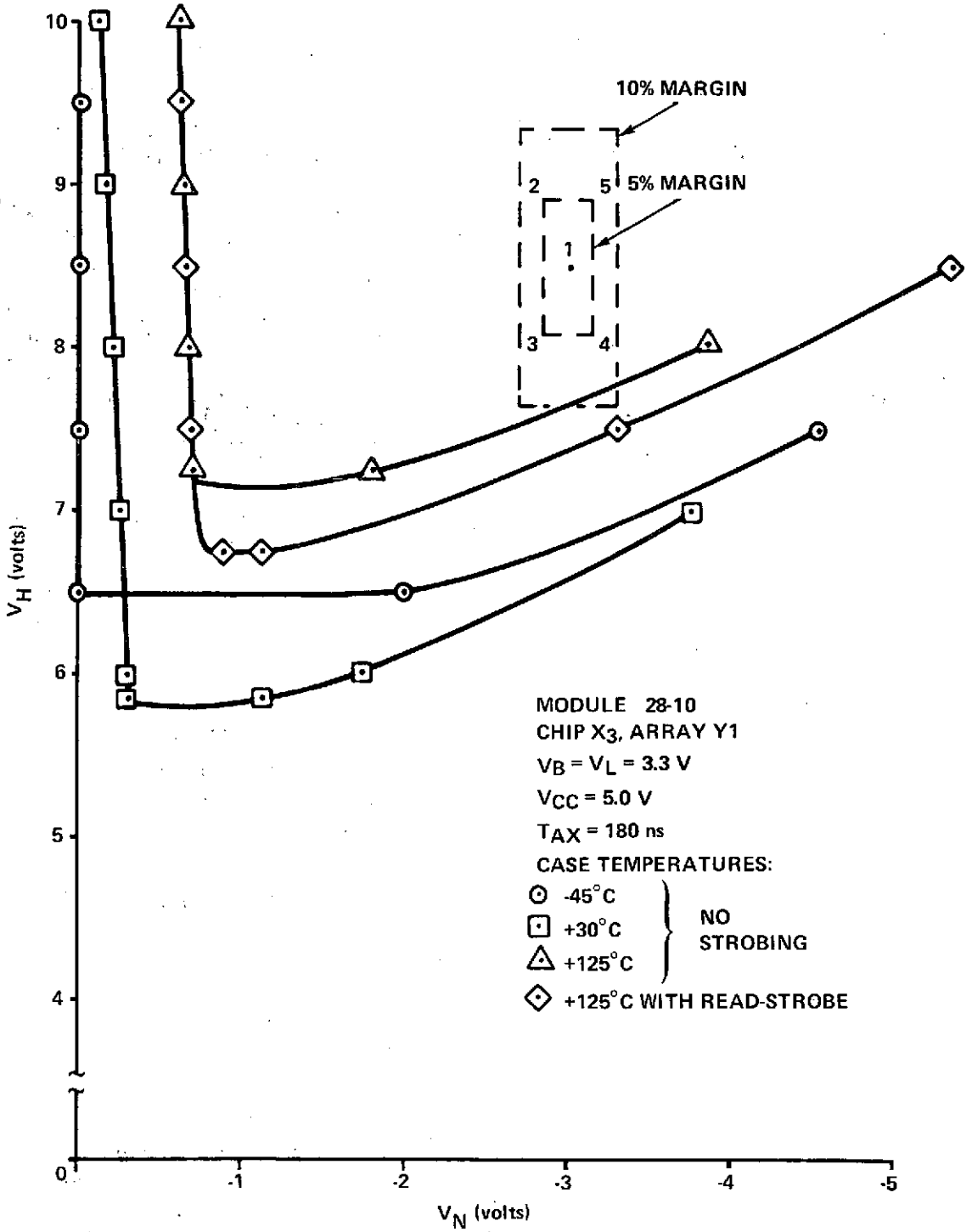


Figure 3-4. SHMOO Plots for Various Temperatures

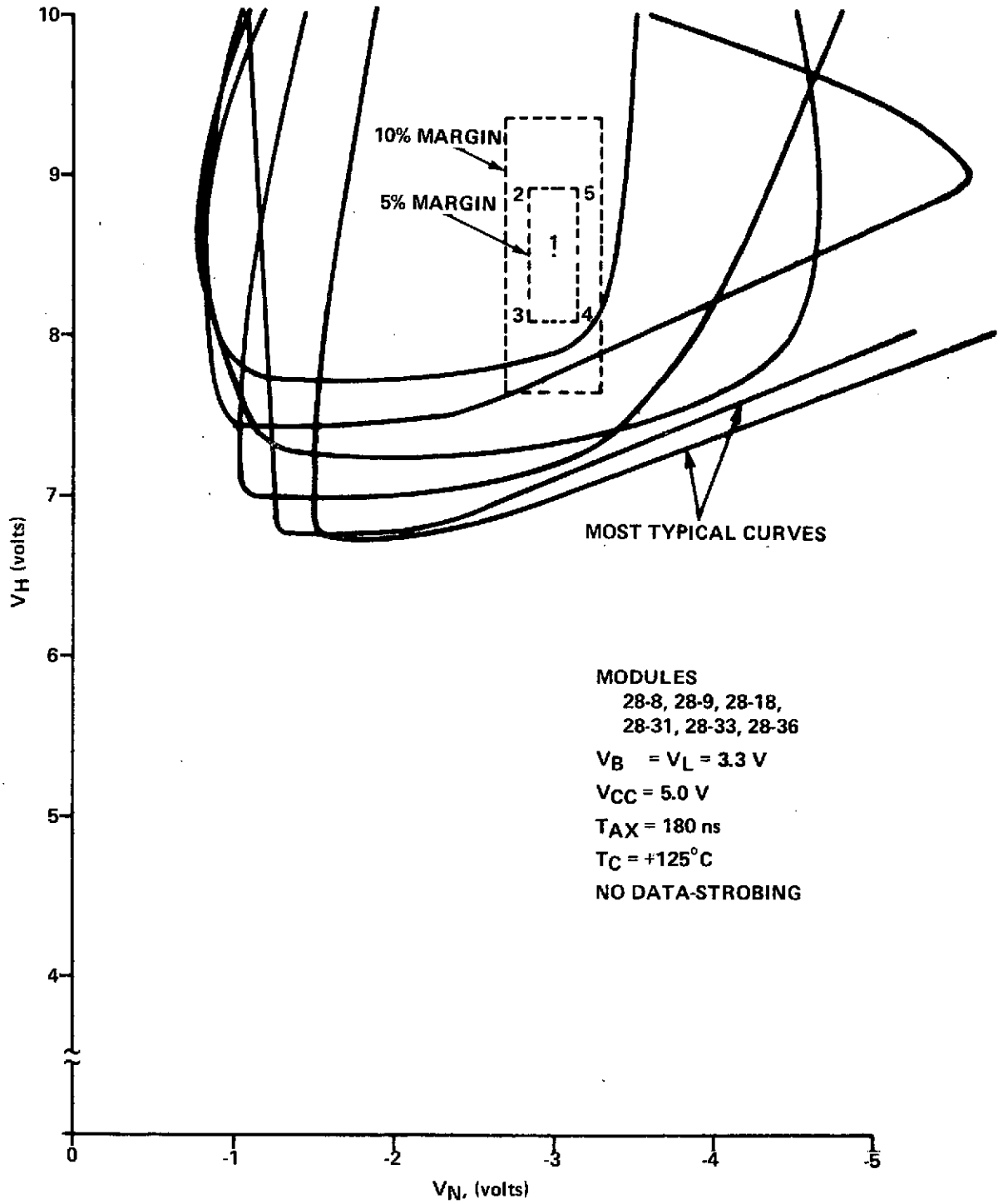


Figure 3-5. Representative +125° C SHMOO Data

The two samples with access times greater than 180 ns, as evidenced in Figure 3-2, were not included, since these are not to be part of the 32 modules delivered.

A change in the T_{AX} reference condition to 170 ns from 180 ns would certainly decrease the margins, but the shape would not likely change appreciably. However, the 6° temperature overstress significantly moderates this condition. A satisfactory yield of acceptable modules can be achieved even without data strobing.

Walk Data and Surround Disturb were the most sensitive data patterns.

3.2.2 MINIMUM WRITE-PULSE WIDTH

The write-pulse width was decreased until a writing error was detected. The specified nominal write-pulse width is 80 ns in Figure 2-5.

Based on five samples, the widest write pulse actually required was 25 ns at low temperature with any of the five power supply margins. At +35° C and +125° C, Margins 3 and 4 require a write pulse only 1 to 4 ns wider than Margins 1, 2, or 5. Margin 3 was identified as the worst case. As summarized in Table 3-5, 33 samples were measured over the temperature range.

Table 3-5

WRITE-PULSE WIDTH SUMMARY

Case Temperature (° C)	Write Pulse Width Required (ns)		
	Maximum	Average	Minimum
-47	25	21.8	21
+31	22	19.0	17
+85	23	17.9	16
+125	24	18.4	16

3.3 INPUT LEAKAGE CURRENTS AND ADDRESS DRIVE LEVEL

The DC leakage current of each of the ten address lines was measured using a DC plotter to trace the current response to a 10-V ramp signal applied sequentially to each input. Fifteen BMMs were checked at +30° C and the worst three of these at +120° C. Figure 3-6 summarizes the numerous traces obtained at room temperature. About 80% of the inputs had less than 160 microamperes leakage current at 8.5 V. The Word Select 4 (WS4) input typically had relatively large currents: 500, 385, and 305 microamperes at 8.5 V for modules 28-31, 28-9, and 28-20, respectively. Also the Word Select 1 inputs characteristically had large leakage currents with an untypical voltage dependence. Both the WS1 and WS4 leakage current behaviors evidently derive from the memory chip design and processing.

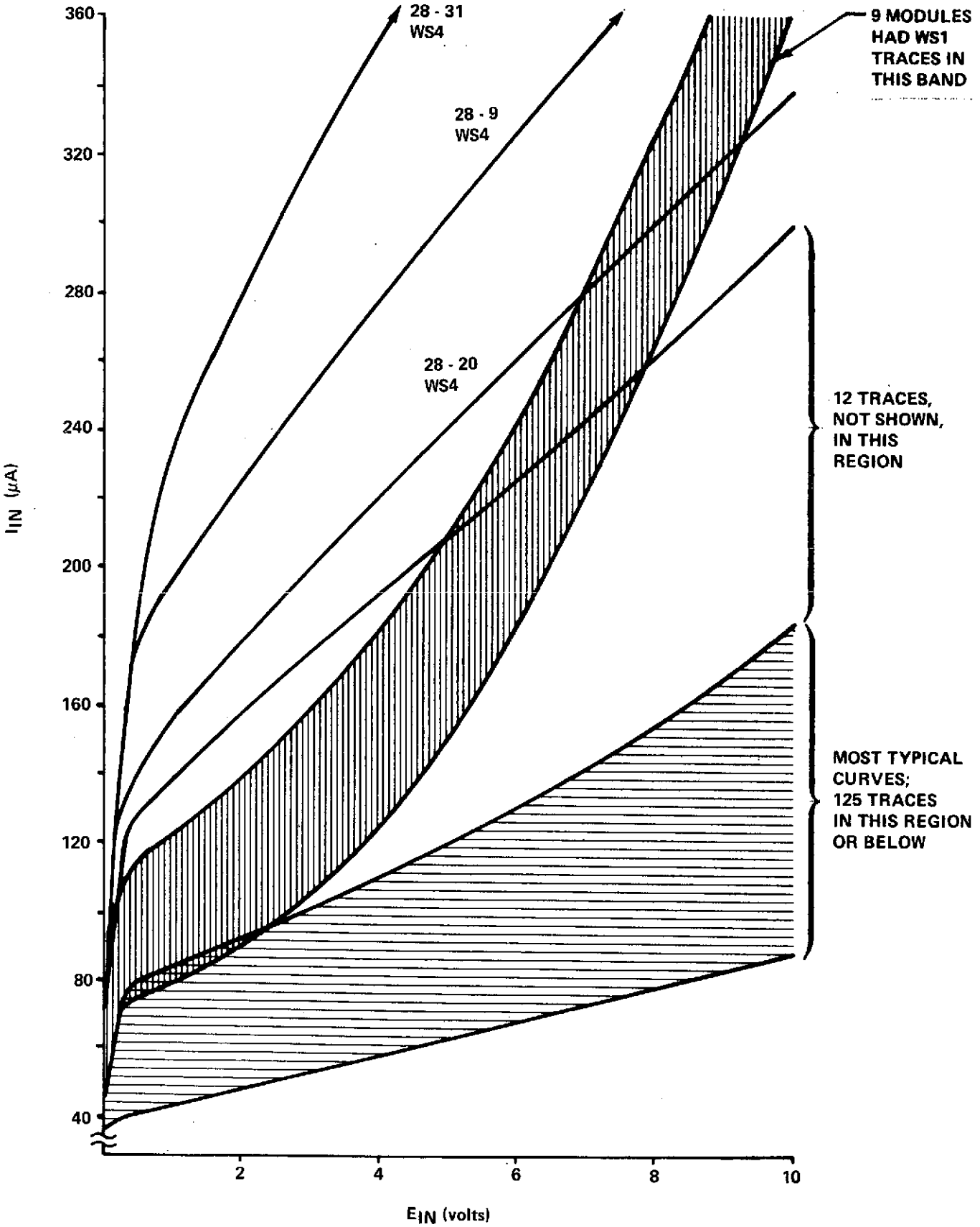


Figure 3-6. DC Input Current Leakage at 30° C

Data taken at +120° C unexpectedly showed leakage currents to be about 40 microamperes lower than room temperature values, although the cited features of Figure 3-6 were still preserved. A data reverification performed at the time evidenced no measurement error.

Excessive input currents could cause a droop in the address driver waveforms to perhaps as low as 6.5 V in a severe case. Therefore, the ability of the BMM to address properly with such pulses was tested by adjusting all address signals to 6.5 V pulse maximums. All five BMMs tested at +30° C and +125° C addressed properly. The samples used were those with the large WS4 and WS1 leakage currents.

3.4 CAPACITANCE

The 1 MHz capacitance to ground was measured for the various input and output lines. A Boonton Direct Capacitance Bridge, Model 75B-S8, was used. Since this capacitance generally does not pose a problem and only a small variation was expected, only 10 or 3 samples were measured at room temperature, as summarized in Table 3-6. Only the X and Y lines pose notable loading and require consideration for driving.

3.5 POWER

The BMM average power dissipation as a function of temperature is given in Figure 3-7 with specific values given in Table 3-7. The devices were in a 4K × 2 bit configuration. The operating or selected power was taken with 50% of the data bits in the "1" state.

The "average power" was computed using the average current drawn from each supply under "nominal" or "maximum" supply conditions. The "Max" power conditions are the average values achieved when the various power supplies were set at the 5% tolerance conditions found to yield maximum module dissipation. These values are V_H = 8.92 V, V_{CC} = 5.25 V, $V_L + V_B$ = 3.47 V, and V_N = -2.85 V. The power for each individual module was not computed, but a check of modules drawing the largest current from a particular supply showed that these used only about 5% more power than the average. The standard deviation of the important power supply currents was less than 5% of the mean. Ten to 32 samples were tested.

Data for the "Max" state of the 250 ns cycle time case was linearly extrapolated from the nominal case data; various checks establish its validity.

In the unselected or standby condition, when all X and Y lines are at a down level, only DC power is dissipated. If only a Y line is up (i.e., Y half-selected state) only DC power again is dissipated. If one or more X and no Y lines are up (i.e., X half-selected), both DC and AC power are dissipated in the selected chip(s).

Table 3-6

SUMMARY OF CAPACITANCE MEASUREMENTS

Control or Signal Line*	No. of Samples Measured	Capacitance (pF)			Measured to Ground Pin
		Max.	Min.	Avg.	
X_1	10	64.7	60.3	62.2	D1
X_2		65.5	61.0	63.9	D1
X_3		64.8	56.9	60.2	D1
X_4		63.4	58.1	61.7	D1
Y_1		28.9	27.4	28.1	D1
Y_2		28.2	26.5	27.2	D1
WE1		5.5	5.1	5.3	A2
RS1		4.9	5.9	5.4	A2
BS1		17.1	16.1	16.5	D1
WS1		21.5	19.8	20.6	D1
WS2	3	16.2	15.0	-	D1
WS3		17.3	16.3	-	D1
WS4		16.8	16.0	-	D1
WS5		16.5	15.2	-	D1
BS2		17.1	15.8	-	D1
BS3		15.7	14.9	-	D1
BS4		16.3	14.9	-	D1
BS5		16.3	15.1	-	D1
DI1		4.0	3.6	-	A2
DO1		10.3	9.9	-	A2
DI2		3.9	3.5	-	J2
DO2		10.3	9.6	-	J2
WE2		5.7	5.5	-	J2
RS2		5.9	5.4	-	J2

*Symbols defined in Figure 2-6

The 8K x 1-bit power was calculated by adding one-half of the 4K x 2-bit standby power to one-half of its operating power.

The sense amplifier and memory chip share the same V_H supply; no measurement was made of the power partitioning between these devices.

3.5.1 CYCLE TIME DEPENDENCE

Operating power decreases with increased cycle time. The principles involved in extrapolating power from one cycle time to another are explained here. They have been used on some data in this report (always so designated) to obtain 250 ns cycle time currents based on 300 ns cycle time data.

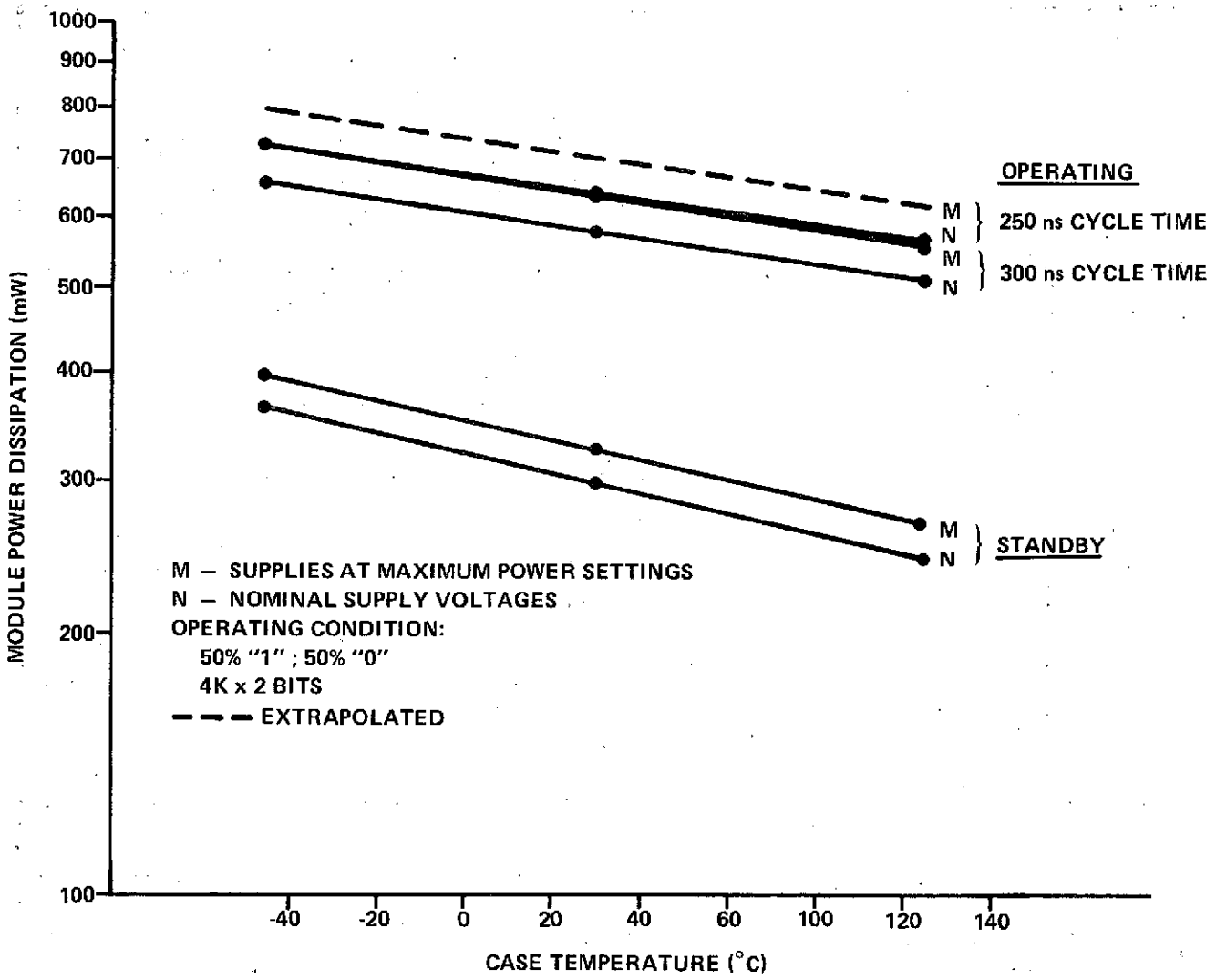


Figure 3-7. BMM Total Average Power vs Temperature

Table 3-7

AVERAGE POWER DISSIPATION SUMMARY

Mode	Cycle Time (ns)	Power Supply Settings*	Case Temp. (°C)	Supply Dissipation (mW)			Total 4K×2 Power (mW)	Calculated 8K×1 Power (mW)
				V_H	V_L+V_B	V_{CC}		
Operating	250	Nom.	-45	414	205	101	720	542
			30	402	132	101	635	466
			125	379	81	101	561	404
		Max.**	-45	455	226	111	792	595
			30	442	145	111	698	511
			125	417	89	111	617	411
Operating	300	Nom.	-47	343	210	101	654	509
			33	335	136	101	572	435
			125	321	85	101	506	376
		Max.	-47	384	222	111	717	558
			33	372	144	111	627	475
			125	357	90	111	558	412
Standby	None	Nom.	-47	67	205	92	364	364
			30	75	131	91	297	297
			125	73	80	93	246	246
		Max.	-47	81	216	101	398	398
			30	84	139	100	323	323
			125	84	85	103	265	265
The V_N supply dissipates less than 0.1 mW								

*See text
**Extrapolated data

Increased cycle time is normally added to the end of the address time when no transitions occur, so the analysis of the currents is simplified. For the BMM, current from the V_N supply is negligible (microamperes) and the currents from the V_{CC} and V_B supplies are independent of the cycle time. The current (I_L) from V_L constitutes the drain currents for the memory cells, and effectively is not dependent on the cycle time. The current (I_B) from the bit-line-restore voltage supply, V_B, varies inversely with the cycle time. However, V_L and V_B are connected together in the BMM. Since I_B is less than one-tenth of I_L, changes in I_B will not impact the current $I_L + I_B$ appreciably. (Measurements show only a +2% change in going from 300 ns to 250 ns cycle time over the full temperature range at nominal voltage.)

The current from V_H depends inversely and (roughly) linearly on the cycle time (for cycles longer than 250 ns), based on circuit equations. Measurements given in Table 3-8 substantiate this, showing a 19.5% average variation between 300 ns and 250 ns cycle times over the full temperature range at nominal voltage.

Table 3-8

SUPPLY CURRENT DEPENDENCE ON CYCLE TIME

Parameter	Cycle Time (ns)	Current (mA) at		
		-46° C	+30° C	+125° C
I_H	250	48.7	47.3	44.6
I_H	300	40.4	39.4	37.8
Ratio of Above	(250/300)	1.20	1.200	1.180
I_L and I_B	250	62.3	40.4	24.6
I_L and I_B	300	62.1	39.8	24.1
Ratio of Above	(250/300)	1.003	1.005	1.02

3.5.2 POWER SUPPLY CURRENTS

Figure 3-8 and Table 3-9 summarize the currents drawn from the various supplies, over the full temperature range, when the BMM is in the operate or standby mode in a 4K × 2-bit configuration. Currents for an 8K × 1 organization would be equal to or lower than for the 4K × 2.

In separate measurements, it was observed that I_H varies directly and linearly with V_H. The combined currents $I_L + I_B$ vary sublinearly with V_L and V_B, but they are a direct linear function of V_H. V_{CC} powers only the sense amplifier; I_{CC} varies directly and linearly with V_{CC}. V_N is the substrate bias; its value does not appreciably affect other supply currents.

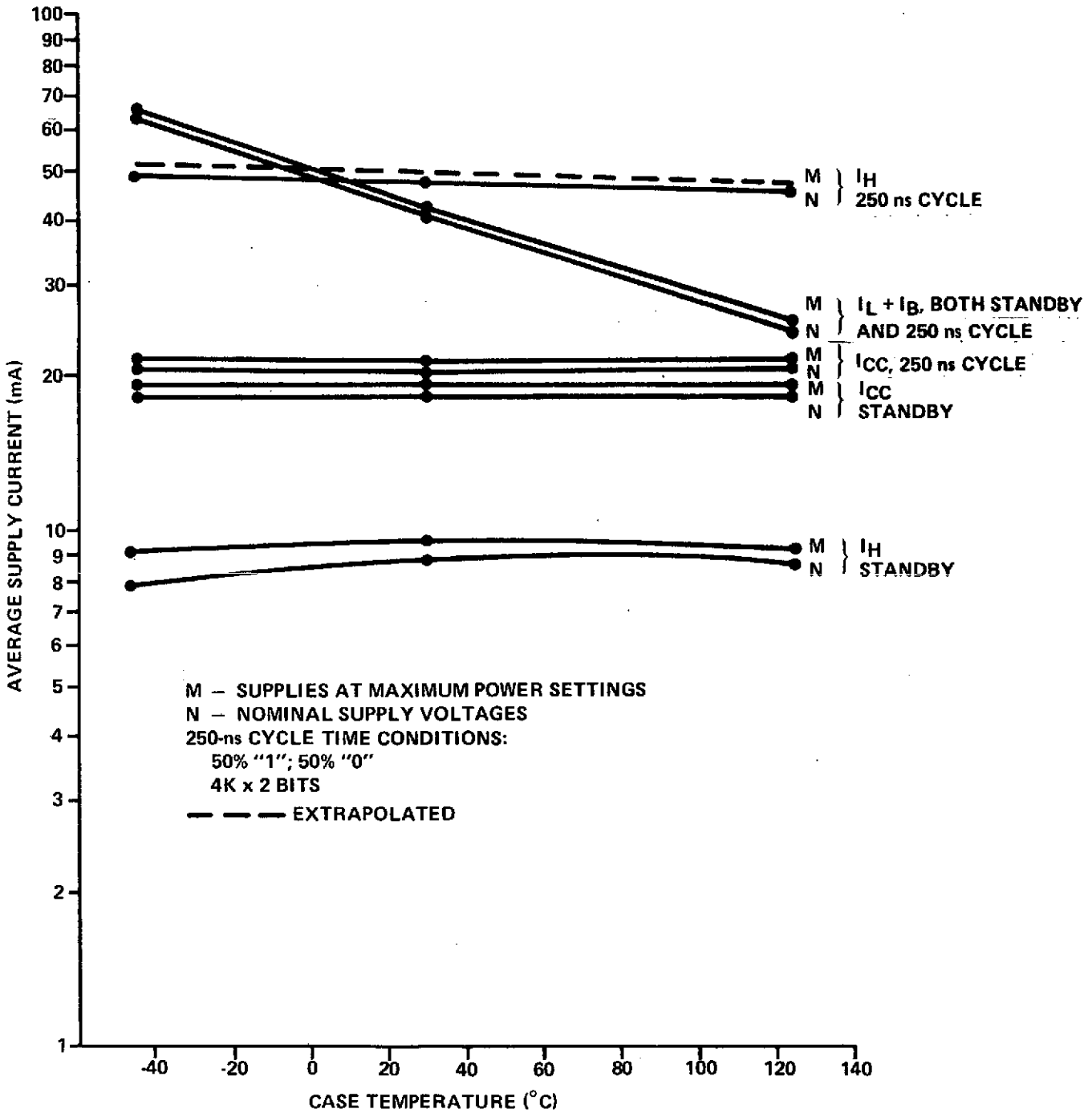


Figure 3-8. Average Power Supply Currents vs Temperature

Table 3-9

POWER SUPPLY CURRENTS

Mode	Cycle Time (ns)	Power Supply Settings*	Case Temp. (° C)	Average Value (mA)			Largest Value (mA)		
				I_H	$I_L + I_B$	I_{CC}	I_H	$I_L + I_B$	I_{CC}
Operating	250	Nom.	-45	48.7	62.3	20.3	59.2	65.9	
			30	47.3	40.4	20.0	52.7	41.9	
			125	44.6	24.6	20.6	47.2	25.9	
		Max.**	-45	51.1	65.4	21.4			
			30	49.7	42.4	21.1			
			125	46.8	25.9	21.7			
Operating	300	Nom.	-47	40.4	63.6	20.3			
			33	39.4	41.3	20.0			
			125	37.8	25.7	20.6			
		Max.	-47	45.4	70.7	21.4	48.2	77.9	22.6
			33	44.0	45.7	21.1	46.1	52.1	26.0
			125	42.2	27.1	21.7	45.0	31.0	22.8
Standby	None	Nom.	-47	7.84	62.1	18.3	8.2	63.0	
			30	8.84	39.8	18.1	8.3	40.9	
			125	8.64	24.1	18.6	9.2	25.2	
		Max.	-47	9.02	65.6	19.3	9.4	69.5	
			30	9.44	42.2	19.0	10.1	43.5	
			125	9.38	25.7	19.6	10.0	26.9	

V_N supply current is greatest at +125° C = 22 μA average, 52 μA largest value

*See text
**Extrapolated data

Section 4

CONCLUSIONS

The 32 required Basic Memory Modules were fabricated, functionally tested, and characterized with no notable problems. The data indicates that using the current fabrication techniques, including the one-time replacement of individual faulty memory or sense amplifier chips, will produce acceptable BMMs with a satisfactory yield.

The electrical parameter that will be most deterministic of the yield is the access time at +125° C at the worst-case power supply margins, with the Read-Strobe line enabled continually. Strobing this line, however, reduces the address access time to an average of 108.6 ns from an average of 176.6 ns. This provides considerable relief with respect to the 180-ns address access time goal. Also, the above values do not consider a beneficial 5-ns access time increment available from a minor thermal overstress. Furthermore, the module now uses a 10-ns timing delay that could probably be reduced or eliminated if extra access time margin proved desirable.

The ultimate need for access time margin depends on the rise time achieved for the selected input drivers, notably the chip select driver, since that line presents nearly a 70-pF load. If the worst-case driver rise time is longer than 20 ns, a shorter effective read-access time would be necessary to achieve a 200-ns read-access time for the Main Memory Unit.

The BMM will operate at a 250-ns cycle time, although a 300-ns cycle would be more easily achieved and would require 10% less operating power. The 250-ns cycle time, room temperature, nominal operating power of 635 mW compares very favorably with the originally projected 610 mW. The standby power is only 297 mW, compared with the 450 mW projected.

The BMM is inherently a volatile memory. Nonvolatility, a desirable feature for the Main Memory Unit, can be achieved by using a battery or energy-storage cell backup power supply. The details of this approach were not investigated in the present program.

Appendix A

TEST CARD DESCRIPTION

This appendix describes the layout and use of a special test card provided to facilitate laboratory testing of the BMM. By using only standard TTL logic levels* from appropriate timing and data generation test equipment, single BMMs may be functionally tested and exercised in either the 4K × 2-bit or 8K × 1-bit organization.

Figure A-1 shows the 3-11/16 × 5-1/2 inch test card with a BMM in the only socket connected. The test card provides:

- A zero-insertion-force test socket
- Sixteen TTL-to-MOS interface drivers and pull-up resistors suitably connected to those BMM signal lines that require 0-8.5 V signals, specifically the four Chip Select (X), two Array Select (Y), and ten Address lines
- A 1000-ohm pull-up resistor connected to V_{CC} for each of the two Data Output lines
- Decoupling capacitors.

The conductor patterns on the card permit either the direct soldering of signal lines or the plugging-in of the card into a 55-pin, in-line, 2-7/8 inch, edge-type card connector. A ground plane exists beneath the socket, and all ground lines are connected with it.

The 16 drivers are contained in three standard Texas Instrument SN7406N hex inverter buffer driver DIPs. Their open collector outputs are connected on the card to the 8.5-V V_H supply through 510-ohm pull-up resistors. The BMM 5-V supply provides the V_{CC} for the drivers.

Table A-1 lists the correspondence of the signal and power line names with the 55 test card pins and the 36 module pins. For convenience in signal tracing, the input and output pins of the driver DIPs are also listed along with the location of the driver output pull-up resistors. (Figure A-2 defines the DIP and resistor numbering system, when viewing the "reverse" side of the test card.) The signal and power line designations are explained in Section 2.3.1. Test card pin numbers are marked on the card.

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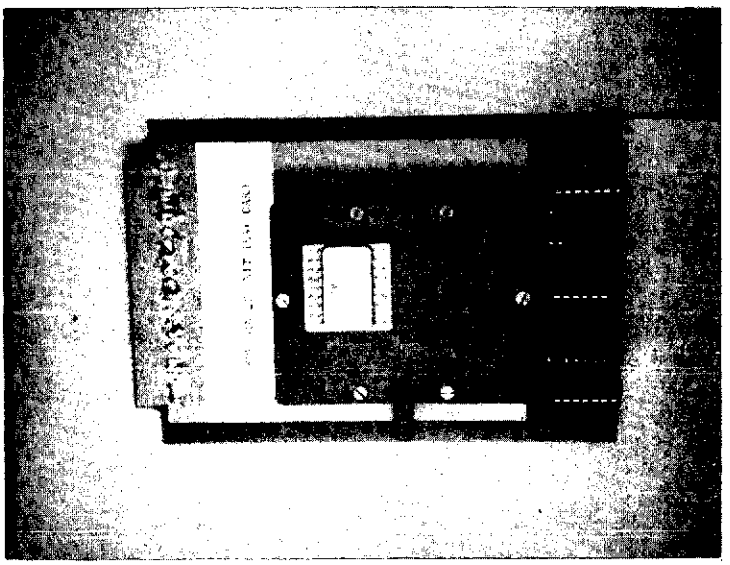
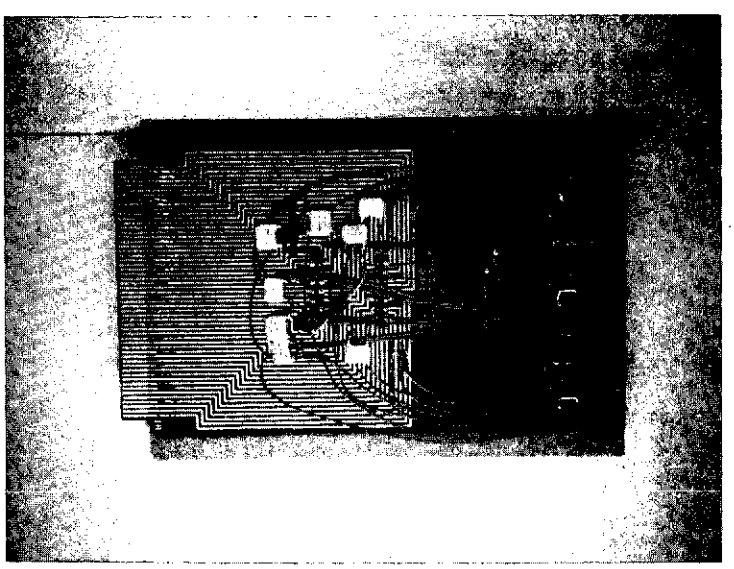
*Minimum up level is 2.4 V
Maximum down level is 0.4 V



a. Top side, with BMM unit in socket



b. Reverse side

Figure A-1. Test Card

Table A-1

TEST CARD PIN-FUNCTION LIST

Function	Card Pin Number	BMM Pin Number	Driver Input Pin	Driver Output Pin	Pull-Up Resistor
Y2	2	F1	U3-13	U3-12	14
WS5	3	G1	U3-11	U3-10	13
WS3	5	H1	U3-5	U3-6	11
RS2	6	J1			
Gnd.	8	J2			
WE2	9	H2			
DI2	11	G2			
WS4	13	F2	U3-9	U3-8	12
VN	14	E2			
BS4	16	F8	U1-9	U1-8	4
WS2	17	G8	U3-3	U3-4	10
X3	19	H8	U2-11	U2-10	8
VH	20	J8			
DO2	22	J9			
X4	23	H9	U2-13	U2-12	7
VH	25	G9			
VL	26	F9			
—	28	E9			
BS5	29	D9	U1-11	U1-10	5
X1	31	C9	U2-1	U2-2	15
X2	32	B9	U2-3	U2-4	16
DO1	34	A9			
VH	35	A8			
VH	37	B8			
WS1	38	C8	U3-1	U3-2	9
VB	40	D8			
BS3	41	E8	U1-5	U1-6	3
BS1	43	D2	U1-1	U1-2	1
VCC	44	C2			
WE1	46	B2			
Gnd.	47	A2			
RS1	49	A1			
BS2	50	B1	U1-3	U1-4	2
DI1	52	C1			
Gnd.	53	D1			
Y1	55	E1	U1-13	U1-12	6

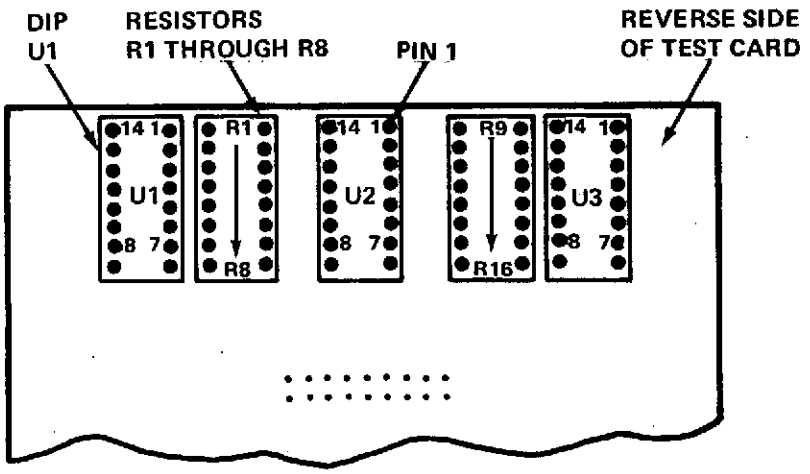


Figure A-2. Driver and Pull-Up Resistor Locations

To exercise a BMM in the test card:

1. Connect the four (5% tolerance) power supply voltages defined in Section 2.4.3. Connect V_L (card pin 26) to V_B (card pin 40)
2. Connect the desired loading on the Data Out lines.
3. Connect the test card for an 8K × 1-bit or 4K × 2-bit configuration, as desired, in accordance with Figures 2-7 or 2-8, respectively. The interface drivers used on the test card, however, do not possess the input AND function contained in the drivers shown in these figures. Thus, one two-input AND gate must be connected at each driver input to conform to these figures. None of the other timing logic shown is provided on the test card.
4. Provide timing signals in accordance with Figure 2-5. All signal lines are "high active." The Clock operates at the selected cycle time (e.g., 300-ns read cycle). Address A_0 signal is identical to the clock, and all other addresses are obtained by a binary countdown from A_0 (with correction for skew). A_0 through A_4 correspond to word select WS1 through WS5. A_5 through A_9 correspond to bit select BS1-BS5. A_{10} is the array select signal, Y. A_{11} (and A_{12}, if used) are the chip select signals (X).
5. The Read Strobe lines may be connected to a DC up level, in which case valid data is available at the Data Out lines any time after the read access time. Alternatively, the Read Strobe line may be pulsed with a pulse (typically 50 ns wide) after the access time, enabling data to be available at the output for the duration of this pulse.
6. For writing, the desired input data is made available synchronously with the address, and the write enable line is activated in accordance with Figure 2-5.