Final Report

DEVELOPMENT OF AN IMAGE CONVERTER OF RADICAL DESIGN

July 1972

Prepared for

MARSHALL SPACE FLIGHT CENTER
Huntsville, Alabama

Under

NASA 8-5112

By

WESTINGHOUSE ELECTRIC CORPORATION
Baltimore, Maryland

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FOREWORD

This final report was prepared by E. L. Irwin and D. L. Farnsworth of the Westinghouse Electric Corporation, Systems Development Division, Baltimore, Maryland. The reporting period covered is from July 1962 to July 1972. This effort was covered by contract NAS 8-5112. The NASA MSFC Program Monitor was C. T. Huggins.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

1. INTRODUCTION

Westinghouse, working under a variety of development programs, has been actively engaged in the field of photon response phenomena since the early 1960's. Through these efforts a number of fully implemented totally solid-state image converter systems have been assembled and the feasibiliy of a multiplicity of others has been demonstrated. Figure 1-1 presents a time-wise description of the progress made on solid-state array cameras between 1962 and the present under the current contract NAS 8-5112 to NASA's G. C. Marshall Space Flight Center; an effort which has capitalized on and closely paralleled advances in state-of-the-art semiconductor technology and has, as a result, contributed significantly to improvements in the field of solid-state imaging.

While the photosensitive nature of semiconductor materials was long recognized and even discussed in elementary physics courses, the full potential of the phenomenon remained in the hinterland until the advent of the aerospace age. Interest in this area, which has grown rapidly over the last decade, received its initial impetus from the stringent weight, power, and reliability requirements imposed on the special purpose sensors used in spacecraft, satellites, and interplanetary probes. To meet these requirements and produce acceptable all solid-state, electronically scanned (as opposed to electron-beam scanned) imaging systems, investigators have employed a wide variety of approaches to the fabrication of photo-responsive devices. Among the most promising of these have been thin-film sensors, monolithic photo-FET's, and epitaxially diffused phototransistors and photodiodes. The present program has led most recently to production of an advanced engineering model camera which employs a 200,000 element
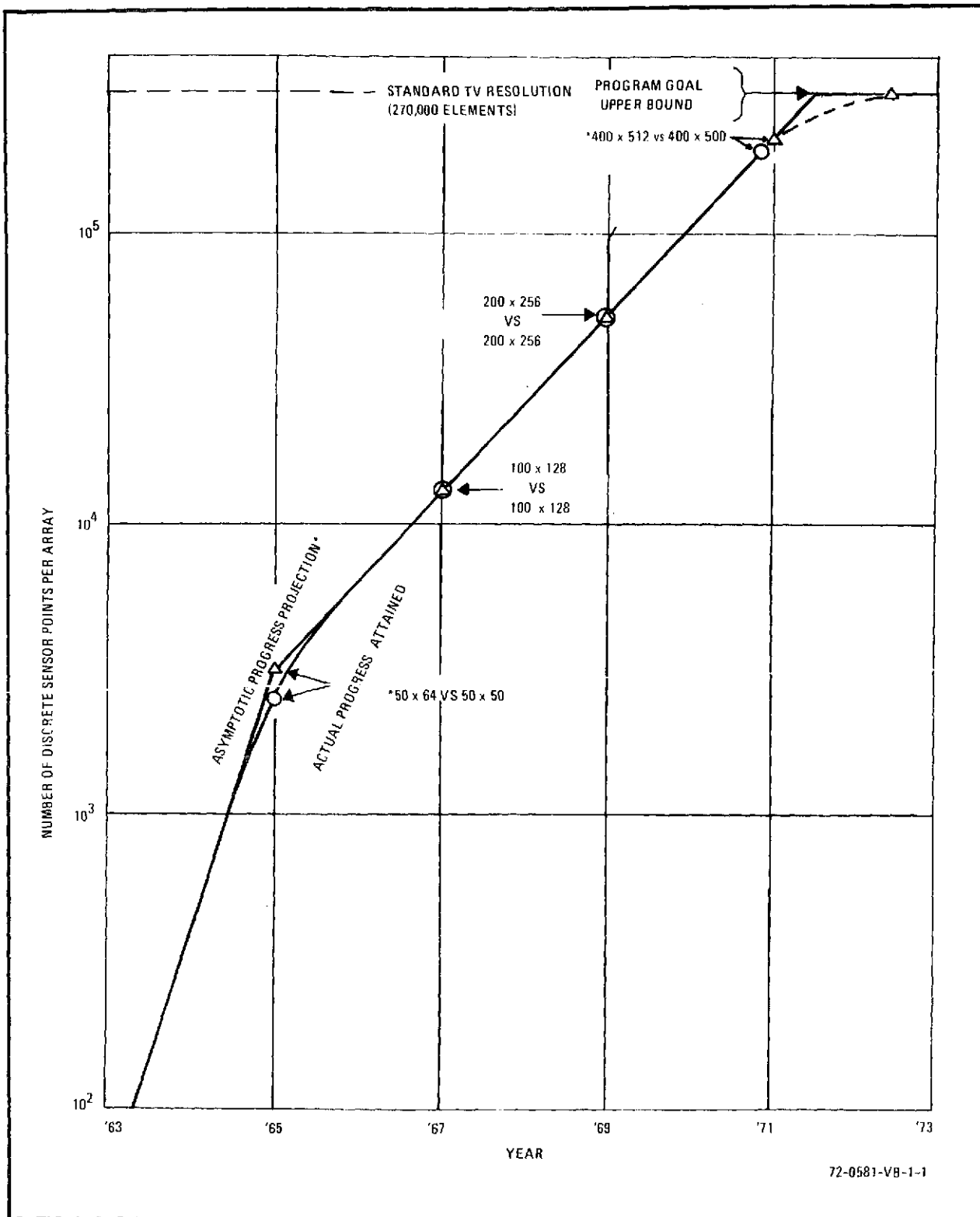
Figure 1-1. Delivered System Time-Progress Chart for
NAS 8-5112 Program

phototransistor array (organized in a matrix of 400 rows-by-500 columns)
to secure resolution comparable to commercial television.

As with former generations of lower density phototransistor matrices,
these 400-x-500 element mosaics have a well established X-Y physical
architecture. Collector rows are initially formed by an isolation diffusion
process such that each collector is separated from all other collectors by
back-to-back pn junctions. Into each collector region bases and emitters
are then diffused at selected intervals. Electrical connections are affected
at the ends of each collector row while successive emitter columns are
interconnected by aluminum conductors terminated in bonding pads. The
surface dimensions of a high density "45" array consist of 0.002-by-0.0025
inch center-to-center spacings of emitters and collectors, respectively, for
a total active detector area of 1 square inch. The 0.0025-inch center-to-
center collector row spacing includes the width required for the isolation
diffusion used to separate collector strips.

Response of solid-state photosensors to varying wavelengths of radiation
is fundamentally a function of the materials used in their construction.
While detectors fabricated from a wide variety of materials are under active
investigation, the greatest degree of success thus far has been achieved
with silicon devices due to the well established technologies involved. The
spectral response of these mosaics is essentially that of intrinsic silicon.
Some shift in peak response occurs as a result of the thicker overlaying oxide
layers and shallow diffusions that exist with integrated sensor arrays.
These factors, particularly the oxide thickness, can be controlled to a
limited degree if it is desired to shift the mosaic response.

In addition to the high resolution camera which makes use of a 400-x-500
element phototransistor mosaic, a number of lower resolution solid-state
array cameras have also been developed during the course of this program.
The first fully electronically scanned image converter system known, for
instance, was built in 1965. This camera incorporated a 50X-by-50Y photo-

transistor array and was initially designed to have its sensor elements operate in what is known as the static or dc mode—the only mode recognized up to that time.

Peculiarities noted in the system's scanned video soon led, however, to specification of the dynamic charge-storage or integration mode of operation for pn junction photodetectors. Detailed analyses revealed that the new operating mode constituted a major improvement in readout philosophy, so the 50-x-50 camera electronics was modified to capitalize on this advanced technique.

A portable demonstration camera was next delivered to NASA in 1967. This system has been shown and reported on extensively. It employs a phototransistor mosaic having 100Y-by-128X lines, and which therefore contains more than quadruple the number of individual sensor points that were available in 50-x-50 mosaics.

Improvements in the related technology of photolithography permitted a second quadrupling of the number of distinct photosensitive points per array in the third generation of matrices developed in 1968. These arrays were fabricated with 200 rows and 256 columns of sensor elements and have proven to have quite good performance when placed in a laboratory test vehicle readout system. One of the major provisions made in this particular adaptive electronics setup was the ability to preselect any given region or any single element out of any array under test for more detailed study. Comprehensive investigations carried out with the system subsequently facilitated specification of the systemological refinements that were necessary for successful acquisition and processing of the image video from succeeding generations of higher resolution phototransistor monoliths.

Confirmation of the techniques evolved through these studies was first realized in 1971 with a direct probing wafer evaluation test stand. This unit was designed specifically to pretest 400-x-500 element arrays while they were still in their original postprocessing, unscribed wafer form. Through

this expendiency their respective functional capabilities could be determined and compared without the necessity of completely bonding up each individual mosaic as it is fabricated. The electronics employed in this prober system is identical to that deployed in the fully implemented high resolution camera, except that the latter makes more extensive use of hybrid bare chip packaging.

2. SENSOR MONOLITHS

2.1 DEVICE DESIGN

In general, all current approaches to solid-state imaging utilize arrays of diodes, diode-diodes, diode-transistors, transistors, or hybrid thin film photoconductor-diode or transistor structures.

The advantages of the diode approach lie primarily in the ease of fabrication of diode arrays, the achievable packaging densities, and the relatively good uniformity achievable between elements. Line arrays of over 400 elements have been fabricated in silicon. Since only a single diffusion is necessary to achieve isolation in a line array, there is less processing damage involved with these structures and therefore better performance. Extension of diode sensing arrays to two dimensions requires additional processing to achieve isolation unless a separate lead is attached to each diode for read out, an approach which is impracticle for large size arrays. Provision for isolation reduces the achievable packaging density, introduces a cross talk and parasitic sensor element to the structure, and complicates the processing at the expense of minority carries life time.

If the overall array consists of adjacent line arrays utilizing XY interconnection techniques, two problems arise. First, unless all unaddressed rows and columns terminate in zero impedance, there are multiple photoconductive cross-talk paths through the various rows and columns which preclude use of the mosaic for any but single spot imaging applications. With zero impedance terminations, however, photovoltaic cross-talk problems arise.

The second disadvantage of a sequentially read diode mosaic, however, is the inability to operate such an array in a light integration mode. As a result, the output signal level is strictly a function of the light incident on the element during the readout time, with a resultant loss of overall light collection efficiency. For a mosaic as small as 100 x 100 elements, only 0.01 percent of the incident photons would contribute to the readout signal. As a result, simple diode arrays were not considered to be candidates for extensive imaging systems, such as those envisioned at the onset of this effort.

The next simplest structure is the diode-diode structure, which provides several advantages over the simple diode array. By way of explanation, this structure consists of one diode array which provides a commutating function and a second array matched on a one-to-one basis which provides the sensing function. Since each light sensor is isolated from the interconnection bus by a back biased diode except during its read period, cross talk is significantly reduced.

In the case in which a back-biased photodiode is used as the light sensor, charge storage light integration can be employed. The phenomenon described in detail elsewhere depends upon the charging of the light sensing diode to approximately the pulsing voltage level during each read cycle. This charge decays between read pulses as a function of the photon induced hole-electron pairs and junction leakage, and the output signal is obtained by monitoring the amount of charge replaced during each read pulse. While the diode-diode structure possesses the light integration phenomenon, the output signal available from the small diodes needed for large-order mosaics is such that direct readout of such a device is difficult. With XY interconnections, a voltage source is applied to the selected column in the other axis, and the charge transfer is monitored. Since all elements are interconnected, the pulse applied to the row is coupled to all of the elements along the row through the parasitic capacitances associated with the overall structure, as well as

through the leakage paths from the various unselected columns to ground. If the parasitic capacitances are large compared to the sensing diode capacitance, application of a readout pulse results in almost completely recharging the sensing element due to the current flow into the parasitic capacitance, effectively reading them out. For large-scale small total area mosaics, typical diode capacitances are on the order of a few picofarads, while the parasitic capacitances are generally orders of magnitude larger.

Conceptually, the diode-diode structure offers another advantage: the commutating diodes can be made using one technology (generally silicon because of the high quality junctions which can be achieved in this material) and the sensing diodes with a material whose characteristics match the particular spectral response desired.

In addition to the internal parasitic discharge problem, an external problem exists with the selection switches used to address the readout point. In most cases, the turn-on transient for the sampling switch will swamp the readout signal. If FET or MOS switches are used, this transient can act either to add charge to the readout bus or to remove charge from the bus, depending upon the polarity of the switching pulse applied to the gate. This problem is not unique to the diode-diode structure, although it is generally more severe with small quantities of charge available in such a mosaic.

The phototransistor mosaic is a form of diode-diode structure in which the structure is fabricated so as to have transistor action through the junctions. The structure would look essentially identical to a diode-diode structure, and the readout approach is generally similar. The strip collector mosaic is a specific configuration where the rows of transistor elements have a common, low impedance collector strip and the emitters of transistors in a column are connected by a metallized strip. As described, the phototransistor mosaic consists of an array of phototransistors with emitters and collectors, respectively, interconnected in row and column fashion. Figure 2-1 best illustrates the structure of the phototransistor mosaics selected.

INTERNAL COLLECTOR STRIPS Y
SURFACE EMITTER STRIPS X
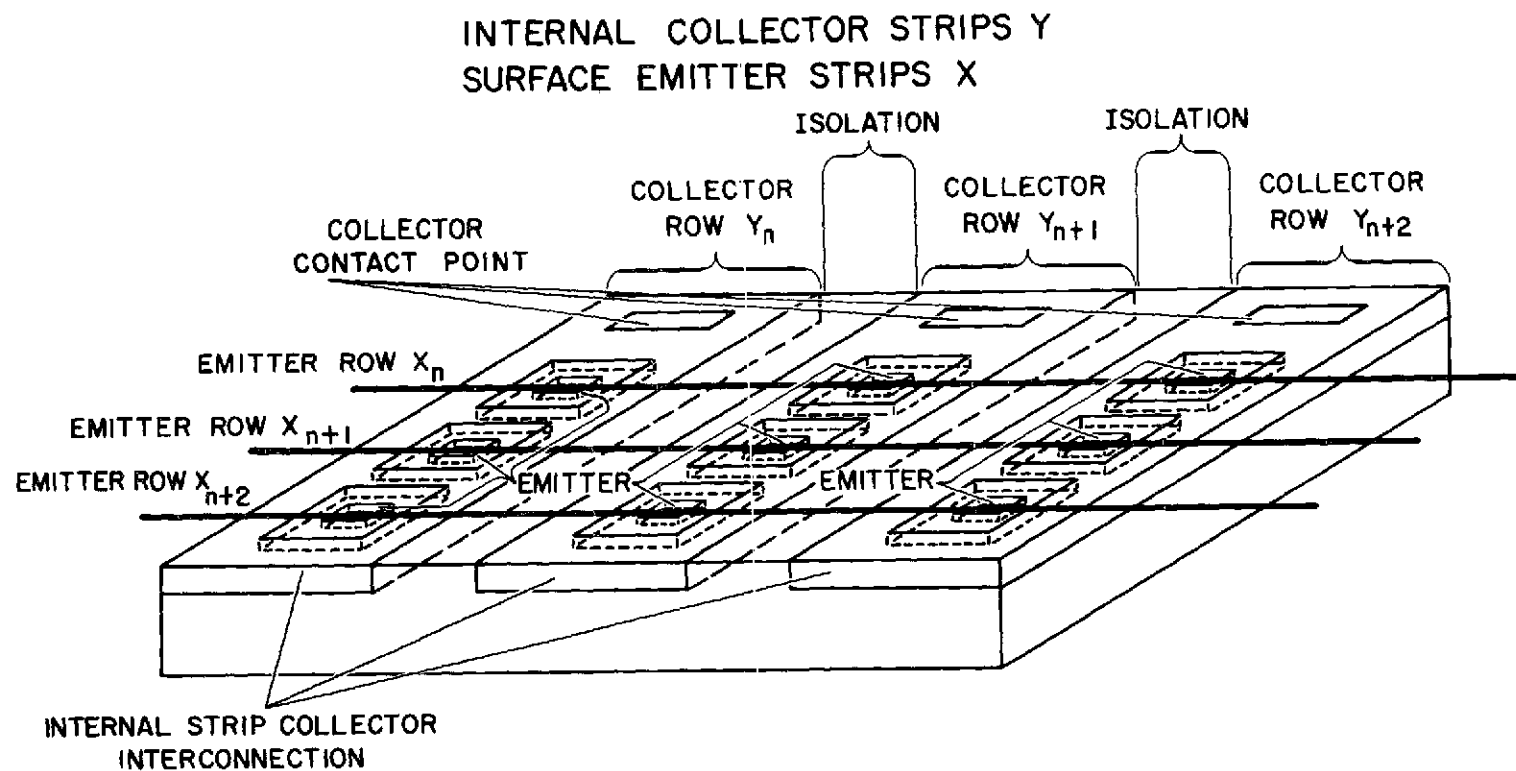
Figure 2-1. Structure of the Phototransistor Mosaic Selected

S5441A-VB-I-2

2.2 BIPOLAR STRUCTURE

The bipolar transistor structure is one of the best examples of the control and use of the pn junction which is produced by oxide-masked diffusion. The transistor structure to be described is illustrated in figure 2-2.

This is a double-diffused epitaxial transistor in the mosaic configuration. The diffused-epitaxial construction results in a four-layer npnp structure. A p+ isolation diffusion results in n type tubs or regions that are electrically separated by the back-to-back pn-junction diodes likewise formed during this diffusion step.

Current-voltage characteristics, gain, capacitance, etc, all depend upon the impurity profiles present in the four layer structure. Essentially, the impurity profile is described by the cross-sectional profile of the active device region. The typical starting substrate material is p-type silicon of about 10-ohm-cm resistivity. This corresponds to an acceptor impurity density of about 10^{15} atoms/cm^3. By a process of epitaxial deposition a layer of n type silicon is grown on the p type substrate to a thickness of 5 micrometers. When suitably isolated by a p+-type diffusion this layer becomes a series of long tubs electrically isolated from each other by back-to-back pn junction diodes. The isolation diffusion is accomplished by the planar process and is of sufficient depth to completely penetrate the n-type layer. Two additional planar diffusion steps are used to complete the npnp structure illustrated. A typical diffused impurity profile is illustrated in figure 2-3 where the impurity atom concentration is shown on a log scale as a function of linear penetration into the semiconductor surface. The epitaxial substrate junction is almost abrupt except for some concentration grading due to diffusion effects. This junction provides parasitic, voltage-dependent capacative coupling to the substrate which varies approximately as $V^{-1/2}$. The capacitive contribution due to sidewall regions formed by the isolation diffusion varies more nearly as $V^{-1/3}$ and is in parallel with the coupling capacitance. Typically the sidewall capacitance is about 0.1 pF/mil^2 for the abrupt junction component and 0.2 pF/mil^2 for the graded sidewall junction component.

2-5
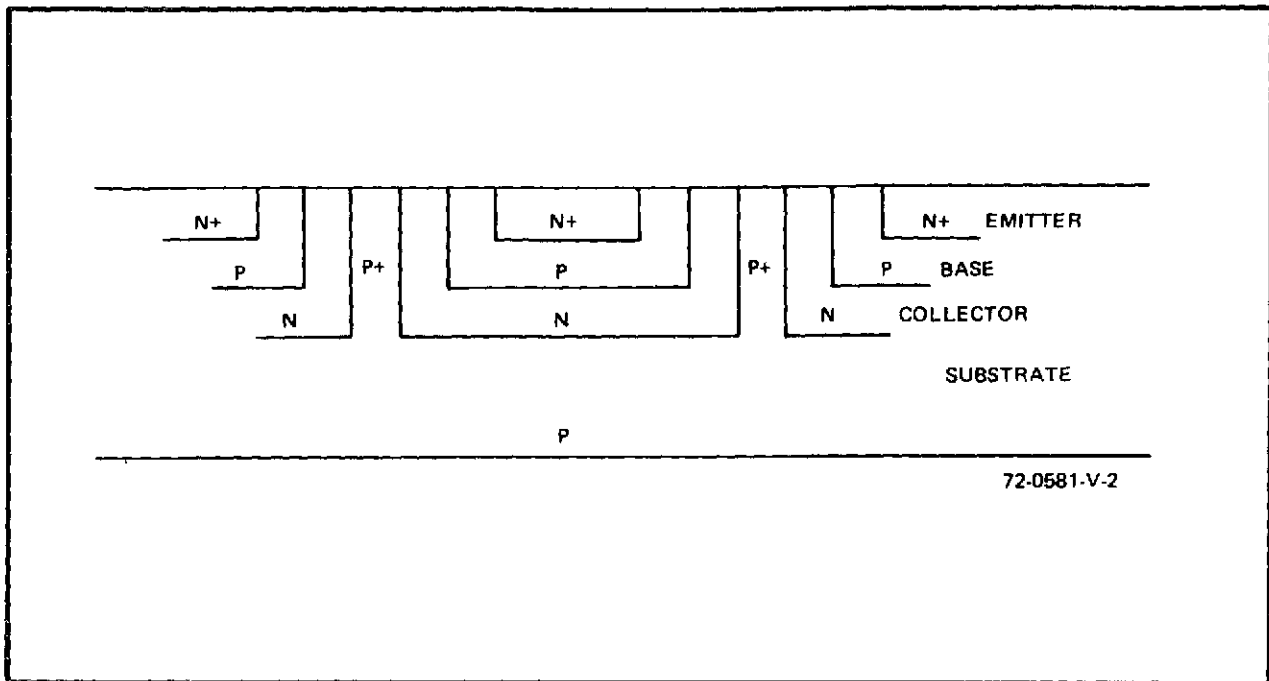
Figure 2-2. Transistor Structure
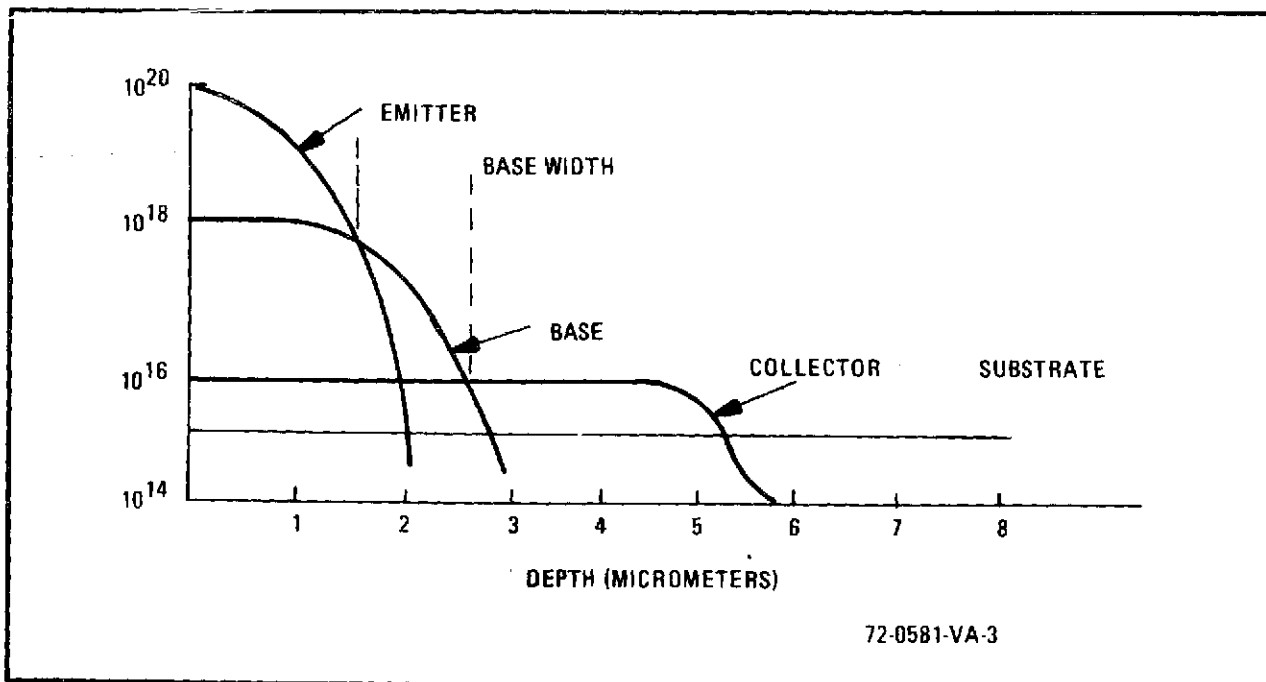
Figure 2-3. Impurity Profile

The isolated epitaxial n-region forms the collector regions of the mosaic. This region has uniform impurity doping, as shown in figure 2-3 with a typical donor concentration of 10^{16} atoms/cm^3. A p-type region is diffused into this n-type region to form the base of the transistors; the boundary between the p- and n-type regions is the collector junction. Since this is now a graded junction, the associated transistion capacity varies as $V^{-1/3}$ and is strongly dependent on the impurity concentration of the n-type region; a higher impurity concentration results in a lower capacity per unit area.

In designing the collector region the resistivity and thickness values that will eliminate collector current saturation must be selected. A particularly effective technique is to introduce a buried layer. This is a layer of high conductivity n-type silicon which is selectively placed between the n-collector and p-substrate. This buried layer functions as a shunting path for the collector current and lowers collector series resistance.

The resistivity and thickness of the collector region also determines collector breakdown. From a knowledge of the breakdown field in silicon and from depletion layer thickness calculations, a choice of resistivity and thickness may be made. The n-type emitter diffusion determines the base width value. The emitter is a high-conductivity n+ layer. Emitter injection efficiency depends strongly on the concentration ratio of impurity atoms in the emitter to impurity atoms in the base. In addition, for the diffused emitter the concentration gradient near the emitter junction has an important effect on injection efficiency, so that the emitter junction depth should be considered, particularly for operation at low levels.

2.3 MOSAIC DESIGN

The selection of a phototransistor mosaic as the sensor for the solid-state camera required that a technique be devised whereby the concept could be utilized. The concept and the technique devised is illustrated in figure 2-1. Each of the internal strip collectors is isolated from its neighbor by the junction formed between them. The collectors are n-type and the substrate

p-type. Individual bases are selectively diffused into these collector tubs and emitters in turn diffused into the bases. The emitters are then interconnected into separate rows by means of a surface aluminum strip. Connection to the collectors is made at the collector ends as shown. Not shown in this illustration is the low resistance n-type region provided as a subdiffusion beneath each collector row.

The isolation width to a great extent controls the size of the mosaic. That is, it functions to limit packing density. To provide the isolation, boron is diffused through an oxide window completely through the epitaxial layer. The minimum window opening is a compromise function between optical resolution available over an inch line and yield. A broken isolation line, broken because of a photographic plate fault, dirt particle, mask pin hole, etc, will result in paralleling two collectors, effectively doubling the apparent capacity of those elements and in general degrade the response of two rows. A widening of the isolation line, caused by many of the above sited defects, can cause a base to substrate short or a bad element.

The usable line width has decrease by almost an order of magnitude during the course of this endeavor, from a usable width of 0.003 inch to 0.0003 inch wide as used in the 400-x500 element design.

Other factors associated with the isolation diffusion limit mosaic size. This boron diffusion must penetrate the epitaxial layer completely; however, for each unit downward the diffusion also spreads laterally nearly two units (one on each side of center). Thus, if the epitaxial layer is 15 micrometers deep,then through a 75 micrometer window the diffusion width would be about 100 micrometers or greater than 0.004 inch wide. Early epitaxial layers had to be about this thick to provide good surfaces and uniformity. At present it is possible to grow epitaxial layers of 5 micrometers thickness of good uniformity of both thickness and resistivity. Thus the progress made in optical resolution has been augmented by epitaxial control and quality to lower the isolation space requirements to those shown in figure 2-4.
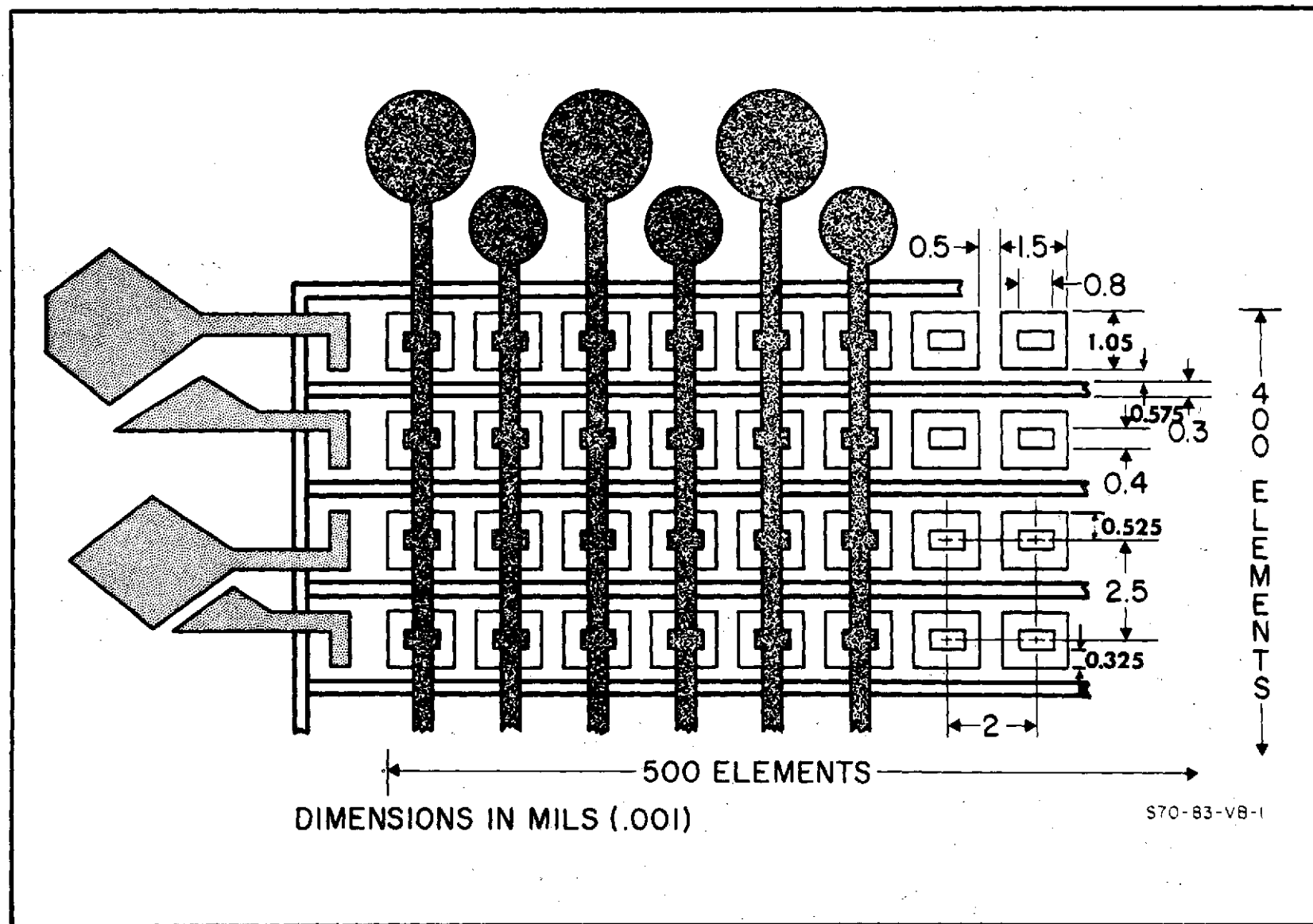
Figure 2-4. 400-x-500 Element Mosaic Dimensions

DIMENSIONS IN MILS (.001)

S70-83-V8-1

The photosensitive junction of principal interest in the phototransistor element is the base collector junction, both its periphery and bottom. Due to the thin diffusion utilized it is possible for this buried segment to absorb effectively the shorter wavelength photons. Under these conditions it is essential that the base be made as large as possible while the emitter is made as small as possible. The width of the base is restricted by the following: (1) the side wall of the isolation diffusion, (2) the extent of the depletion region, and (3) misalignment tolerances. As outlined above the base must not be allowed to short, either directly or via a depletion layer or channel, to the isolation diffusion. Furthermore, it is impossible to expect that the base window mask willbe aligned perfectly to the isolation pattern. Present state of the art allows a plus or minus 0.0001 inch maximum misalignment which may arise from physical misplacement of the mask to slight size descrepancies in the masks themselves. The dimensions selected and shown in figure 2-4 reflect these considerations and are compromises between absolute tolerances and yield and performance.

Figure 2-5 shows photomicrographs of a corner of each of the photomasks used to delineate the requisite areas of the mosaic. The following section will describe the processes and the specific application to the 400 x 500 element array.
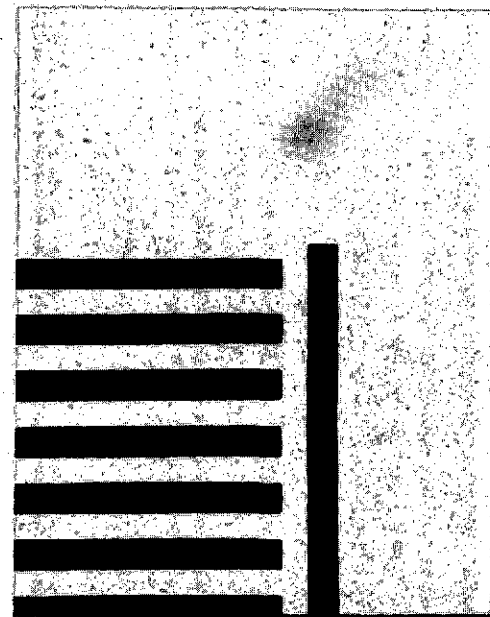
Subdiffusion
Mask 1
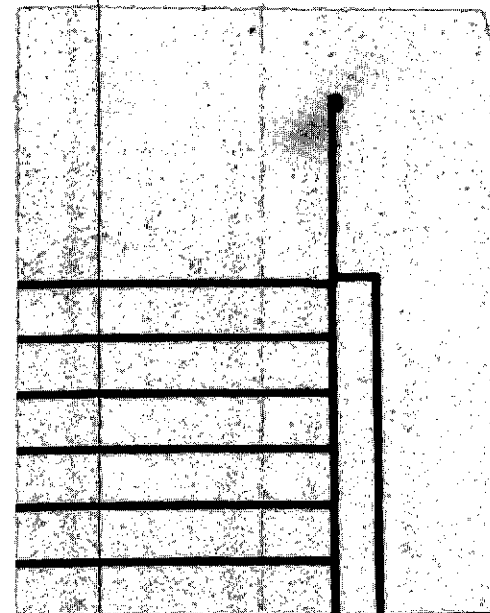
Isolation
Mask 2
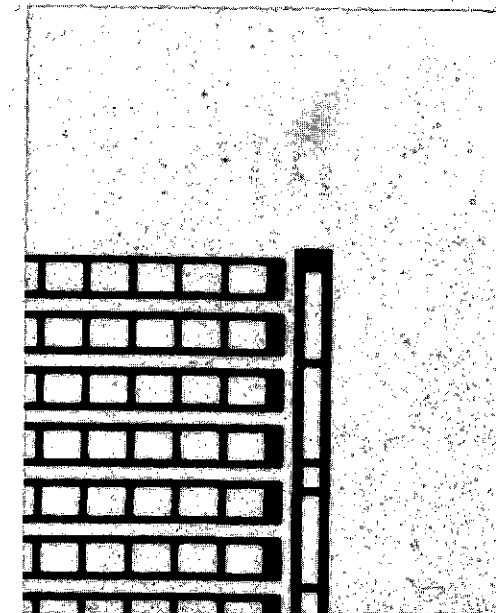
Base Definition
Mask 3
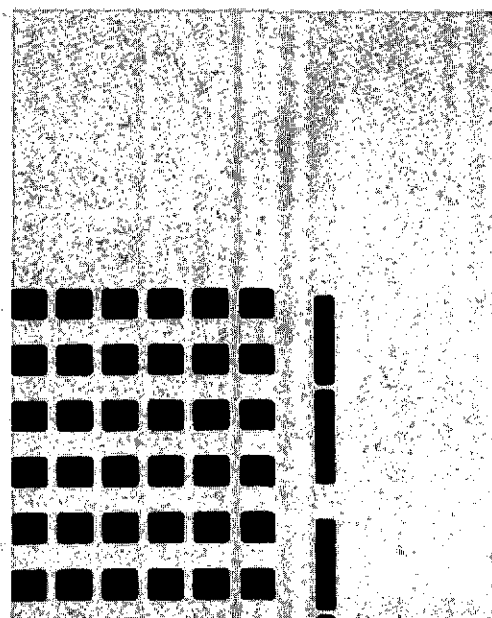
Base Diffusion
Mask 4
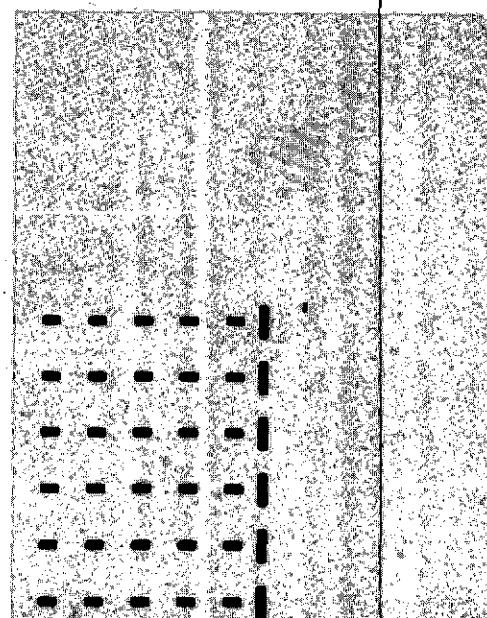
Emitter Diffusion
Mask 5
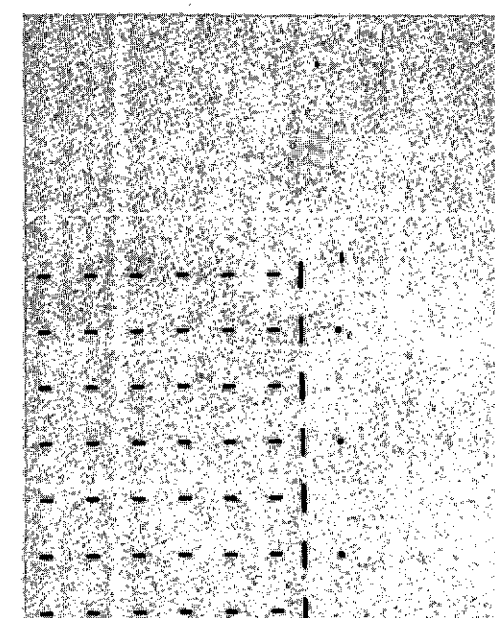
Contract Window
Mask 6
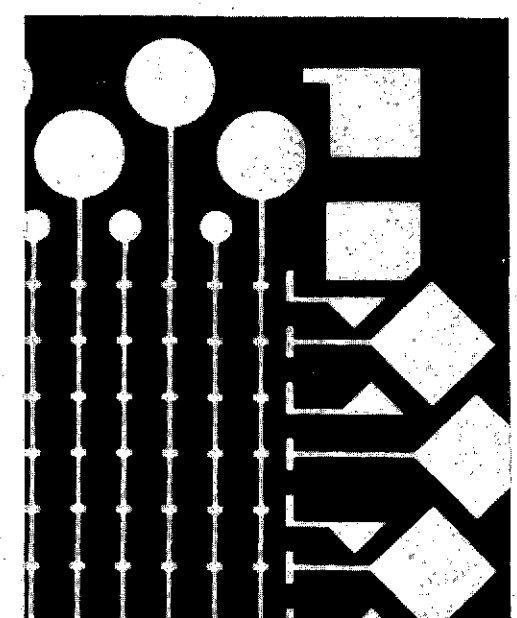
Metallization
Mask 7

72-0581-PB-4

Figure 2-5. Photomicrographs of Corner of Each Photomask

3. FABRICATION TECHNOLOGY

3.1 MATERIAL PREPARATION

The objective of material preparation is to produce a suitable surface on the silicon wafer for mosaic fabrication. The ideal surface for planar device fabrication generally is one that is flat, defect free, and uniform. These physical characteristics as well as the electrical parameters of the material must be compatible with all subsequent processing steps.

The physical specifications imposed by epitaxial growth require that the wafer surface be essentially free of defects and work damage. The surface is first prepared by mechanical lapping and polishing. Then the residual work damage is removed by chemical polishing and a short vapor etch (high temperature HCl etch).

The planar device fabrication process demands that the surface topology be flat so that junction depths move uniformly and predictably into the crystaline structure. To achieve proper electrical characteristics, an undisturbed crystal structure is necessary; therefore, such surface defects as scratches, microcracks, or insufficient removal of lapping damage must be prevented.

Defects such as pits, spikes or orange peel which often appear after subsequent processing, may have their cause or origin established during the material preparation steps. Therefore, great care must be taken to avoid contamination of the silicon, the equipment, or the materials used in the wafer preparation process.

Various methods have been used to provide damage free silicon wafers for mosaic fabrication. Among these are chemical polishing, mechanical-chemical polishing, and electro-chemical polishing. The chemical approach offers the greatest ease in obtaining defect free, uncontaminated wafers.

However, it is necessary to have a good mechanically polished surface to obtain a flat surface free of orange peal defects. Mechanical-chemical polishing provides a wafer that is usually sufficiently prepared for epitaxial growth. Electrochemical polishing combines an electrical potential, an etchant, and light to produce very useful surfaces; however, the cost is comparatively high.

The crystals used for mosaic processing are grown by the Czachralski method. These ingots, of suitable diameter, are sliced into wafer form utilizing diamond impregnated saws. The surface of the wafer at this point has considerable damage in the form of furrows and microcracks which extend some distance into the material. This damage is removed by planatary lapping, a process which also planarizes the major surfaces and reduces the wafer to a predetermined thickness. While the lapping removes the gross saw damage it in turn introduces damage due to the abrasive grit action to a depth of about 15 micrometers. After a very thorough cleaning to remove all traces of abrasive the finished wafers are given an optical polish. During this operation the 15 micrometer damage is removed but the 1 micrometer abrasive introduces its damage. The depth of penetration though is only a few micrometers. This damage is in turn removed by a slow chemical polish carried out in a rotary etcher. This etching introduces no further damage and does remove that introduced during the polishing operation.

The wafers must be inspected for surface flaws. Acceptable wafers have a specular surface which cannot be seen by direct microscopic examination. Dark-field illumination must be used to detect the minute long, thin scratches which may result from contaminated abrasive. The wafers, after inspection, are cleaned by vapour degreasing in trichlorethylene, boiling sulfuric acid, and deionized water. The dried wafers are then ready for further processing.

3.2 EPILAXIAL GROWTH

There are a number of conditions that should be satisfied for the successful growth of thin expitaxial films on a substrate. These are:

a. The deposited molecules must have a controlled degree of mobility on the substrate surface.

b. Isotropic forces must be present at the surface to promote a specific layer orientation.

c. The interface between substrate and film must not become delocalized by chemical reactions, alloying, impurity deposition, or impurity diffusion from the substrate.

d. The layer must wet the substrate surface.

e. The substrate must be free of mechanical defects which may serve as nucleation sites for a different crystal order then that obtained by the chemically active sites on the substrate surface.

For the condensation of a nonatomic gas, surface mobility can be controlled by the thermal energy of the substrate. Surface temperature fluctuations may promote surface reactions or even chemical reactions that can destroy the layer structure. These effects can be minimized by lower substrate temperatures, but a decrease in temperature requires a slower deposition rate to obtain a good epitaxial orientation. The lower temperature also enhances the spurious nucliation of diatomic or polymeric forms, either of which may tend to reduce or inhibit surface mobility. This leads to a nonoriented dispersion of growths on the substrate.

To obtain quality simiconductor epitaxial layers, silicon epitaxial systems must be controlled to close tolerances for certain parameters. A suitable silicon compound is introduced into a reaction chamber where the proper temperature, thermal gradient, carrier gas and impurity gas flows, and concentrations are capable of being closely controlled. With the proper control of these parameters, there is a thermal descomposition of the silicon bearing compound at the surface of the heated substrate which results in a

single crystaline form of epitaxial layer silicon being deposited on the heated substrate. By simultaneously controlling the type and concentration of impurities introduced in the gas train during the deposition, both the doping level and the conductivity type of the deposited layer may be closely regulated. The doping level of epitaxial layers grown in this manner is generally homogeneous, unlike the impurity concentration profile resulting from the diffusion process.

Epitaxial growth for some of the more common silicon bearing compounds occurs according to the following overall reaction:

$$SiH_4 + H_2 \rightarrow Si + 3H_2$$
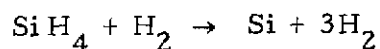
For reasons of apparatus and control simplicity gaseous impurities such as phosphine, arsine, and diborane are used. A typical silicon epitaxial run proceeds as follows:

Step	Reason
1. Wafer cleaning by organic solvent, hot acid, and hot water.	To remove residual polishing contamination and heavy metals.
2. Introduce wafers and carrier into reactor.	
3. Purge with N_2	To remove all oxygen from the reactor.
4. Purge with H_2	To replace all N_2 with H_2 and ready the system for high temperature operation.
5. Heat up and soak.	To allow system to approach thermal equalibrium.
6. High temperature HCl etch.	To produce a completely clean defect free surface.
7. High temperature purge	To clear spent reagents from reactor.
8. Actual disposition compound flow through reactor.	To deposit layer thickness with proper levels type of dopant.

8a. Introduction of controlled
    dopant flow.

9. High temperature purge   To clear spent reagents from
                                 reactor tube.

10. Cool in H_2

11. Purge H_2 with N_2 To remove H_2 before spinning
                                 as a safety precaution.

After inspection which consists of surface examination and test to deter-
mine layer thickness, type, and conductivity, the wafers are then sent to the
next operation, oxidation.

3.3 OXIDATION

The term "thermal oxides" refers to those oxides formed from a thermally
activated reaction of silicon with oxygen, water, or other oxygen bearing
species. The techniques currently in use involve reactions with oxygen
and steam.

Thermal oxidation involves the heating of silicon substrates to tempera-
tures in excess of 900°C in atmospheres of dry oxygen or steam. This is
accomplished in an open tube at atmospheric pressure as illustrated in figure
3-1.

The oxidation of silicon by dry oxygen, steam, or combinations of these
is themodynamically possible at room temperature; however, the reaction
rate is so slow that it makes this method impractical. For temperatures
less than 900°C at atmospheric pressure, the reaction rate is still quite
slow. Practical thermal oxidation techniques therefore use higher tempera-
tures, typically in the range of from 1000 to 1200°C, so that the time re-
quired to achieve oxide thicknesses suitable for masking purposes is on the
order of 20 to 90 minutes. These processes are primarily controlled by the
exposure of oxygen or water molcules to the silicon-oxide interface. The
reaction rate is described by the parabolic law

$$x^2 = kt$$

FURNACE

FLOW METERS

SILICON WAFERS

N_2

H_2

O_2

72-0581-V-5
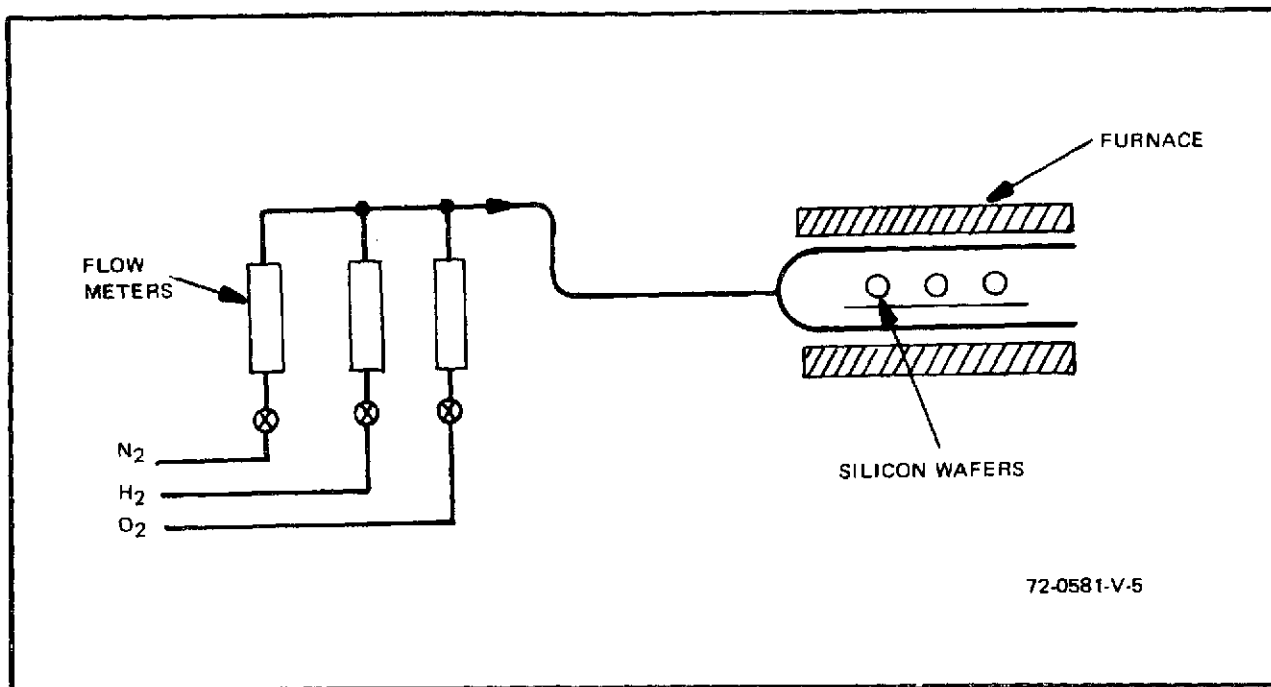
Figure 3-1. Open Tube Thermal Oxidation Apparatus

where x is the oxide weight or thickness, t is the time, and k is the rate constant. The rate constant varies as a function of the material resistivity or impurity doping and also as a function of crystal orientation.

The parabolic law holds true for temperatures above 1100 °C. Below 1100° C the relationship between x and t is found by experiment to depart from the above relationship and become more linear. Specifically, for temperatures below 1000°C an expression of the type

$$x^2 + k_1 x = k_2 t$$

concurs more closely with observations. The lower the temperature, the more linear the relationship becomes, which indicates that k_1 and k_2 are temperature dependant.

There are many methods that can be used to determine the thickness of oxide films. Optical interference techniques are the most commonly used and the most accurate. However, some optical methods are destructive to

3-6

an extent. Techniques developed by Tolansky for measuring Fizeau fringes have been used to measure the thickness of oxide film on silicon. In general, the oxide thickness can be determined by the color appearance of the wafer when viewed under controlled conditions. These colors are shown in table 3-1.

TABLE 3-1

SILICON OXIDE THICKNESS AND INTERFERENCE COLOR RELATIONSHIPS

Color	Thickness (Micrometers)			
	1	2	3	4
Grey	0.01			
Tan	0.03			
Brown	0.05			
Blue	0.08			
Violet	0.10	0.28	0.46	0.65
Blue	0.15	0.30	0.49	0.68
Green	0.18	0.33	0.52	0.72
Yellow	0.21	0.37	0.56	0.75
Orange	0.22	0.40	0.60	
Red	0.25	0.44	0.62	

These relationships are such that the color serves adequately for an in-process oxide thickness test.

The impurity masking ability of an oxide is dependent upon a number of factors. The most important factor is the value of the diffusion coefficient of the diffusing impurity in silicon. Two other factors are the type of oxide used for masking and the particular method of diffusion. All of the common donor impurities have small diffusion coefficients; hence they may be readily used; however, of the common p-type diffusants, only boron has the requisite low value. The minimum oxide thickness necessary to completely mask the diffusion of an impurity using this process has been determined experiment-

ally and found to be about 7000°A, a thickness readily obtained in a reasonable amount of time and at a reasonable temperature.

3.4 DIFFUSION

The diffusion process consists of two phases: (1) a deposition, and (2) a drive-in phase. During the deposition phase, the impurity is deposited upon the surface of the silicon wafer; a short diffusion into the surface takes place. The deposition resistivity or impurity atom concentration is generally controlled by holding the temperature constant and varying the time of deposition.

Following the inital deposition phase, the wafers are removed from the deposition furnance and placed in a drive-in furnance. The redistribution of impurities takes place in the drive-in furnance, resulting in changes in the sheet resistivity, impurity gradient, and junction depth. The heating of the wafer is performed in an impurity free atmosphere so that the only diffusion occurring is a redistribution of those impurities originally introduced during the deposition phase. The impurity redistribution may be modified by introducing controlled amounts of oxygen into the drive-in furnance, thus modifying the sheet resistivity. Also, during this drive-in procedure, the oxide required to protect the junction is grown.

The two-step process of diffusion, though more complex then a single, is preferred because:

a. Improved control and reproducibility of the diffusion is achieved. By separating the process into two steps the diffusion can be monitored more closely, and compensations can be made in the second step for errors in the first.

b. The oxides used for masking are more effective. Usually, the initial deposition step is done at a lower temperature than the redistribution step. The impurity doped glasses formed over the entire SiO_2 masked silicon are then removed by an HF etch, having only doped areas at those places in the silicon where diffusion is required. The lower temperature deposition

step therefore makes oxide masks more effective against the diffusion of impurities since oxide masks that would fail in a single step diffusion are satisfactory in a two-step process.

 c. The use of a two-step process results in a Gaussian distribution of the diffusing impurity. For some applications, the Gaussian distribution is more desirable than the complimentary error function distribution that results from a one-step process.

 d. A two-step diffusion process is more flexible and makes more effective use of the diffusion facilities available.

3.5 PHOTOENGRAVING

An oxide growth on a silicon wafer serves as an effective mask to prevent the diffusion of impurities. This mask material is grown uniformly on the wafer and thus does not afford a method of selectively diffusing an impurity into the silicon to form the various elements of the phototransistor matrix. Therefore, a photomask must be generated and the oxide selectively removed.

The photographic pattern is initiated with an engineering sketch drawn at about a 500 X scale. Each rectangular shape is reduced to its x and y origin and its Δx and Δy components. This format is required by the computer aided design system currently in use. These data cards along with instructions for matrixing the mosaic pattern are, with the appropriate program cards, introduced into the computer. The output is in the form of a line drawing of each level plus a composite of all levels.

If detailed examination of these plots reveals no errors, a magnetic tape is prepared by converting the data cards previously used to data points required for the pattern generator. This machine produces master reticles of the component parts of the mosaic at a scale of 10:1. These reticles are then composed in a step and repeat camera into the final photomask master plates. Submasters and working plates are made from these.

The high resolution obtained in exposing the plate can be lost if the developing procedure is improper. After exposure the plate is placed in reagent of

methyl alcohol for 30 to 45 seconds. This treatment not only preconditions the emulsion surface for the developers, but it also helps remove the pink stain (sensitizer stain) sometimes seen in the developed plate. The anti-halation backing is also removed by this treatment. Eastman Kodak D-8 is used full strength at 65°C. This alteration is the usual developing technique used to provide a denser image than can otherwise be obtained. The emulsion takes 2 minutes to properly develop, and continued agitation of all baths gives the best results. The developed plate is then placed in a 4 percent acetic acid solution for 15 seconds to neutralize the developer. Afterwards the plate is fixed and hardened in the conventional manner.

A modified form of Kodak Metal Etch Resist has been found to be the most suitable resist for this use. The resist is mixed, one part KMER to one part KMER thinner, and placed in capped tubes for centrifuging at 2000 g's for 16 hours. To increase the viscosity of the resist, the caps are removed and centrifugation is continued for 4 hours. The cleaned resist is then separated from the sludge by decanting, and the visocity adjusted.

The resist is now ready to be used in the photoengraving process. Ten cubic centimeter syringes make satisfactory dispensing units. A filtering unit containing a 0.8-micrometer filter is attached to the end of the syringe and a no. 17 hypodermic needle is attached to that.

When an oxidized silicon wafer is taken from the oxidation or diffusion furnances, it is inspected for defects. The wafer is then sprayed with trichloroethylene to remove any dirt or dust that may have settled on the wafer. It is important that no mechanical contact be made with the oxide surface since this could cause severe undercuting when the wafer is etched. The wafer is then stored in a clean furnace at 200°C for a minimum of 30 minutes. Storage of up to 2 days does not affect the wafer, but prolonged storage sometimes causes a change in etch factor.

The resist is dispensed from the hypodermic syringe through the filter and onto the wafer which has been placed on a spinner. The wafer is spun at 6000 rpm for 20 seconds. A slight downdraft of air around the spinner head will remove any strings of resist that form while the resist is being spun from the wafer.

Several factors affect the resist thickness: spin speed; the acceleration of the spinner head to full speed; resist viscosity; and, to a lesser extent, humidity. These parameters must be taken into account or increased resist thickness will result causing either poor resolution or an excessive number of pinholes.

The wafer is placed on a cold Teflon boat and put into an oven at 110 to 120 °C for 12 minutes. A teflon boat is preferred to prevent the wafer from sticking to the boat if the resist flows to the underside of the wafer. If a Teflon boat is not used, the oven temperature must be lowered to about 95 °C to adjust for the heat sink properties of the Teflon. After bakeout, the wafers should be stored in a clean area to prevent dust from settling which later could cause pinholes in the resist by blocking exposure light. To minimize undercutting the wafers should be processed through developing the same day they are coated.

The wafer is placed on a mechanism that alignes it with the photographic mask. Light fringes must be seen at two points or good mechanical contact is not made and poor resolution results. Before the resist is applied, the wafer flatness must be within 20 light fringes, as measured with an optical flat, or resolution will not be uniform across the wafer. It is necessary that a radium of 0.005 inch be present at the edge of the wafer since a buildup of resist at the periphery of the wafer would prevent intimate contact. To assure intimate contact a light mechanical pressure is applied to the wafer.

A Sun Gun is placed 1 foot from the wafer and turned on for 30 seconds to expose the resist. The pattern is developed by placing the wafer on a vacuum chuck in the vertical plane and spraying it with KMER developer for

30 seconds. Immediately after developing, the wafer is spray rinsed in a solution of 80 percent isopropyl alcohol and 20 percent KMER thinner for 15 seconds and blown dry. A stronger developing system will give sharper, cleaner lines; but some care must be exercised to keep from blowing narrow lines in the pattern from the wafer.

The image may now be inspected since the developing solvents have disolved the unexposed resist leaving the exposed resist pattern on the wafer. The inspection should include a check for proper alignment, cleanliness of the smallest openings, and completeness of the resist pattern.

The wafers are placed on a 1/2 inch thick Teflon block and placed in a postbake oven at 180°C for 20 minutes to drive off the developing solvents. Extended bakeout causes the resist to flow and close very narrow openings. A shorter bakeout may degrade adhesion.

The etching solution for oxide etching is:

$$\left.\begin{array}{l} 1000 \text{ cc } H_2O \\ 1 \text{ lb } NH_4F \end{array}\right\} \text{ Solution A}$$
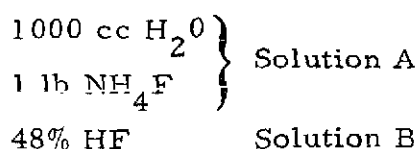
48% HF   Solution B

Ten parts of solution A are added to one part of solution B. The etch rate of this solution is 750 $\overset{\circ}{A}$ per minute for a neutral thermal oxide. Of course, this etch rate is related to temperature. Measurements for a cooled etchant show that there is no improvement in the etch factor over that found for it at room temperature.

The time required to completely remove the oxide from the open areas on the wafer is obtained by dividing the oxide thickness by the etch rate. One minute is added to the calculated value to allow for possible variations in the oxide thickness. If the wafer is removed from the etchant before the oxide has been completely removed, some difficulty in etching and under-cutting will result. This is apparently caused by leaching action of the resist.

A suitable etchant for aluminum is:

phosphoric acid	25 parts
nitric acid	1 part
acetic acid	5 parts

The bath is heated to 75-80°C. The wafer is supported and lowered into the bath. Etching is very rapid and the wafer must be withdrawn as soon as the aluminum disappears from the etched areas. The etch rate is about 15,000 $\overset{\circ}{A}$ per minute.

The removal of the resist from oxide coated wafers is accomplished by immsing the wafers in hot (150°C) sulfuric acid for 5 minutes and then rinsing in deionized water. This method is used for complete removal of resist between diffusions. However, in the case of aluminum coated wafers the acid would also remove the aluminum; therefore, a commercial resist stripper such as J-100 is used. This is heated to 85 to 90°C and the wafers immersed for 5 minutes. The wafer is then spray rinsed to remove the stripper and any residual resist.

3.6 MOSAIC PROCESSING

The conversion of these processing techniques to an operational mosaic is carried out by submitting wafers to a step-by-step process. Each group of wafers carries written instructions as to how each step is to be accomplished. Mechanical-chemically polished wafers are prepared in bulk and stored until needed. After assembling the required number of wafers, the processing proceeds as follows:

Step	Purpose
1. Chemical Polish	To removed the last traces of surface damage and clean.
2. Oxidation	Grow thermal oxide 5000Å deep.
3. Photoengraving	Open windows through which the subdiffusion can be made.

Step	Purpose
4. Arsenic Diffusion	Diffuse arsenic 20-30 fringes deep 80-100 ohms/sq. to reduce collector strip resistance and prevent collector pinch off.
5. Epitaxy	Grow a 5 micrometer 0.5 ohm-cm arsenic doped layer (all oxide remove prior to epi growth)
6. Oxidation	Grow a thermal oxide 7000Å deep.
7. Photoengraving	Open windows for the isolation diffusion.
8. Boron diffusion	Diffuse boron to a depth of 19-20 fringes 5 to 10 ohms/sq to isolate each collector row.
9. Photoengraving	Open windows for the base diffusion.
10. Boron diffusion	Diffuse boron to depth of 8 fringes 300 ohm/sq to form the base regions.
11. Photoengraving	Open windows for the emitter diffusion.
12. Phosphorus Diffusion	Diffuse phosphorus 6 fringes deep 5 to 10 ohms/sq to form the emitter.
13. Silox Passivation	Provide phophorus doped oxide as a passivation glass over the mosaic.
14. Photoengraving	Open windows where contact will be made to the silicon.
15. Phosphorus Diffusion	Diffuse phophorus very shallowly 5 to 11 ohm/sq to reduce contact resistance.
16. Silox Passivation	Provide phosphorus doped oxide as a passivation glass.
17. Photoengraving	Open windows where metal must contact the mosaic.

Step	Purpose
18. Aluminum Evaporation	Provide a $10,000\overset{\circ}{A}$ film of aluminum over the mosaic.
19. Photoengraving	Etch the aluminum into the required pattern.
20. Sinter	Heat treat the aluminum-silicon interface to provide ohmic contact.

After successfully completing each of these steps, the wafer is then ready for testing. Of course, in-process test are conducted at each step and those wafers failing are rejected. However, those wafers passing these static dc tests may fail due to defects that cannot be screened this way. The problem is that no contact can be made to the base regions of the mosaics in process, nor can extensive probe measurements be carried out. The physical size of the particular regions as well as the possibility of mosaic damage or contamination rule out these possibilities. Tests sites are provided at the mosaic periphy and these provide in-process test data. While not conclusive, this data does provide the only in-process electrical checks available. Figure 3-2 is a picture of a completed mosaic.

S9892A-BB-1
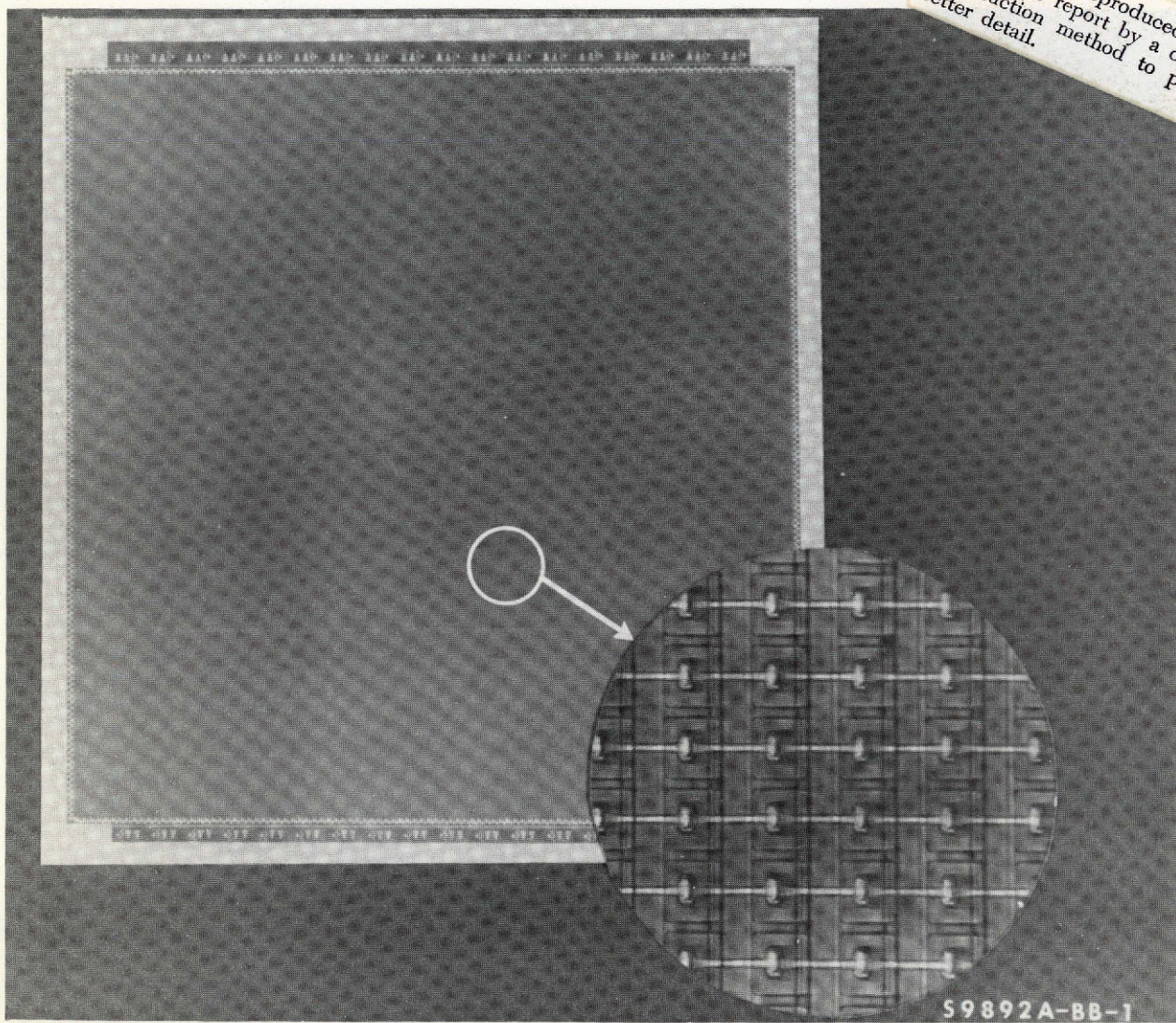
Figure 3-2. 400-x-500 Element Silicon Phototransistor Matrix Array

4. FUNCTIONAL THEORY

Two alternate readout modes of operation are obtainable with photo-transistor sensors: the dc or continuous mode and the integration (charge storage) mode. The dc mode of operation is the basic mode for continuous operation of the phototransistor, whereby photon generated carriers in or near the base region are beta multiplied, resulting in an output current proportional to the instantaneous photon flux on the sensor. When employed in large scale arrays, this mode of operation offers several drawbacks. First, output current is highly dependent on the beta of the phototransistor which, in a large array, might vary significantly from sensor to sensor, resulting in nonuniformity or loss of dynamic range. In addition, output signal level for normally encountered light levels is in the microvolt range for reasonably low values of load resistors. This low output level, coupled with an inherently high output impedance, normally requires that some amplification prior to commutation be provided.

The phototransistor integration mode, discovered in the course of development of the 50-x-50 element solid-state image converter for this program, is a dynamic mode of operation in which a transient output pulse is observed. This pulse is a measure of the total number of photons incident upon the light sensitive regions during the time between element samples.

Incident light continuously generates carriers which are stored on the junction capacitances of the phototransistor. Sampling consists of monitoring the discharge of the collector-base junction capacitance through a load resistance. The magnitude of the output transient depends on the total amount of light generated charge which was stored since the previous sampling.

The output obtained in this manner greatly exceeds that which would be obtained by reading out the static, light-generated photocurrent, which is a function of the light flux on the element only during the sample time.

4.1 INTEGRATION MODE OPERATION

In the analyses that follow, the effect of varying the readout/sampling period will be studied for a single discrete or noninteractive line array of phototransistor elements. The results will subsequently be extrapolated to arrays of phototransistors by adding in the extra parasitic elements that come into play with large mosaics and act to load their operation. Figure 4-1 shows the circuit configurations and the equivalent circuit diagrams that are used to describe respective portions of the total operating cycle of a phototransistor. The two capacitors shown as C_{BC} and C_{BE} are the base-collector and base-emitter junction depletion layer capacitances. The voltages specified pertain only to the case in which the readout period is long compared to any of the circuit time constants (Case I). Corresponding expressions for a very short (Case III) and an intermediate length (Case II) period are developed later in the text.

4.1.1 Single Phototransistors

Under the given stipulation that the readout period is very long, figure 4-1(a) shows the conditions that prevail at the end of this sampling interval. With the readout bias still applied at this point, it is assumed that sufficient time has expired to allow the collector-base capacitance (C_{BC}) to completely charge up to the V_{cc} supply voltage (Case I). At the beginning of this readout condition, the voltage across this capacitance had been reduced to a value lower than V_{cc} due to the charge generated by both light and leakage during the integration period.[*]

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[*] The charge generated consists of electron-hole pairs produced in both the p and n material at the collector-base and base-emitter junctions. These carriers tend to neutralize the charge at the junction and thereby reduce the voltage across the junction.
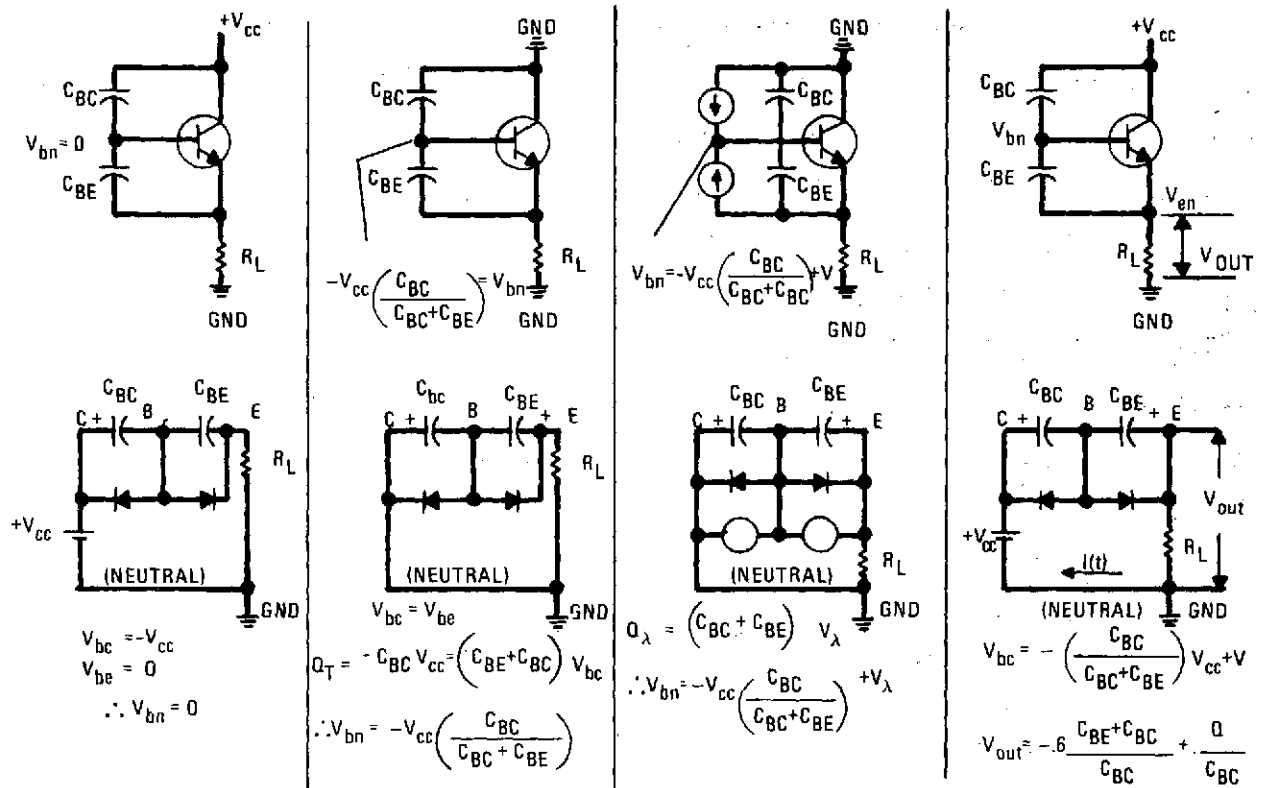
Figure 4-1. Phototransistor Integration Mode of Operation
(a) Readout; (b) Reverse Bias; (c) Integration; (d) Instantaneous Readout

Since the voltage across C_{BC} is lower than $+V_{cc}$ at the beginning of read-out, current starts flowing from the supply through C_{BC} and into the base of the transistor. Therefore, the base-emitter diode becomes forward biased as transistor action begins. For silicon, about $+0.6$ volt is dropped across this forward biased junction. As C_{BC} becomes charged to $+V_{cc}$, the current flowing into the base decreases, thereby decreasing the voltage drop across the base-emitter junction (this can be visualized by considering the current-voltage characteristic of the forward-biased base-emitter diode). Therefore, the assumption of a long read period (Case I) implies: (1) complete charging of C_{BC} to $+V_{cc}$; (2) no current flowing into the base junction; and (3) the voltage drop across the base-emitter diode to be zero. (Later in the

4-3

analysis it will be seen that this assumption leads to the presence of an extra term in the output expression which subtracts from the output of the device.) Therefore, the base-emitter capacitance is assumed completely discharged (it is assumed that no significant dc light generated current is flowing).

At the conclusion of this readout period, the device is reverse-biased (figure 4-1(b)) by returning the collector to ground. (We will consider the effects of emitter sampling switches later.) This voltage change charges the combination of C_{BC} and C_{BE} so as to back-bias both junctions. The charging of C_{BC} and C_{BE} in series through R_L causes a negative spike at R_L, but this spike has little energy. Its amplitude is normally limited by the rise time of the collector bias, since the exponent

$$R_L \left(\frac{C_{BE} \; C_{BC}}{C_{BE} + C_{BC}} \right)$$

is normally very short. When this charging has taken place $V_{bc} = V_{be}$. Since the emitter and collector are both at ground, by charge conservation

$$Q_t = -C_{BC} V_{cc} = (C_{BE} + C_{BC}) V_{bc} \tag{1}$$

where Q_t is the total charge stored on the base node during the readout period.

At the beginning of reverse-biasing when the collector is returned to ground, one notices that C_{BE} and C_{BC} are effectively put in parallel when looking from the base to ground. This means that any charge generated in the base will neutralize charge Q_t which is shared on C_{BC} and C_{BE}. Then the maximum charge which can be generated $(Q_{\lambda max})$ and still be theoretically read out is $-Q_t$ (i.e., the voltage change due to photon generated charge is in opposition to supply voltage). From (1) it follows that

$$V_{bc} = \left(\frac{-C_{BC}}{C_{BE} + C_{BC}} \right) V_{cc}$$

and, since $V_{bn} = V_{bc}$, this leads to

$$V_{bn} = \left(\frac{-C_{BC}}{C_{BE} + C_{BC}} \right) V_{cc}. \tag{2}$$

The reversed-biased condition described directly above initiates the integration period (figure 4-1(c)).

The current generators shown represent the photon and leakage current generation in both junctions. It is noted that the quasi-static equilibrium condition requires that $V_{bc} = V_{be}$ at each instant throughout integration. Therefore, if we assume a total light/leakage generated charge $= Q_\lambda$, then $Q_\lambda = (C_{BC} + C_{BE}) V_\lambda$, where V_λ is the voltage decrease (in magnitude) on each junction due to charge generation. Q_λ cannot exceed Q_t; so Q_t is a measure of device dynamic range. In addition, Q_λ is dependent on the light sensitivity of the device and the time allowed for the integration period.

$$V_{bn} = \left(\frac{-C_{BC}}{C_{BE} + C_{BC}} \right) V_{cc} + V_\lambda. \tag{3}$$

The readout cycle begins by returning the collector to $+V_{cc}$ (figure 4-1(d)). Assuming this voltage rise occurs instantaneously, both the base node-to-neutral return voltage (V_{bn}) and the emitter to neutral voltage (V_{en}) will instantaneously rise V_{cc} volts, so that

$$V_{bn} = V_{cc} - V_{cc} \left(\frac{C_{BC}}{C_{BC} + C_{BE}} \right) + V_\lambda = V_{cc} \left(\frac{C_{BE}}{C_{BC} + C_{BE}} \right) + V_\lambda \tag{4}$$

and $V_{en} = V_{cc}$.

A transient current will begin flowing immediately, and the emitter voltage V_{en} will tend toward ground. The time constant (τ) for the transient current is equal to

$$\tau = R_L \left(\frac{C_{BC} C_{BE}}{C_{BC} + C_{BE}} \right) \tag{5}$$

Transistor action is not present at this point because the base-emitter junction capacitance is charged such that the junction is reversed-biased.

Transient current flow with this time constant will continue until the voltage across the base-emitter junction is sufficient to forward-bias the base-emitter diode (nominally at +0.6 volt), thus turning on the transistor. This turn-on point is derived as follows (V_{on} is defined as the voltage at the emitter when the phototransistor turns on). As V_{en} falls to V_{on}, V_{bn} will fall from the level of (4) by an amount equal to

$$(V_{cc} - V_{on}) \left(\frac{C_{BE}}{C_{BE} + C_{BC}} \right) .$$

Thus, at the point of turn-on, $V_{en} = V_{on}$ and

$$V_{bn} = V_{cc} \left(\frac{C_{BE}}{C_{BC} + C_{BE}} \right) + V_\lambda - (V_{cc} - V_{on}) \left(\frac{C_{BE}}{C_{BE} + C_{BC}} \right) ; \tag{6}$$

which, upon combining teams, simplifies to

$$V_{bn} = V_\lambda + V_{on} \left(\frac{C_{BE}}{C_{BE} + C_{BC}} \right) . \tag{7}$$

By noting that $V_{en} = V_{on}$ and assuming $V_{bn} - V_{en} = V_{be} = +0.6$ volt at turn on, it is then found that

$$0.6 = V_\lambda + V_{on} \left(\frac{C_{BE}}{C_{BE} + C_{BC}} \right) - V_{on} = V_\lambda - V_{on} \left(\frac{C_{BC}}{C_{BC} + C_{BE}} \right)$$

or, solving in terms of V_{on}, that

$$V_{on} = (V_\lambda - 0.6) \left[1 + \left(\frac{C_{BE}}{C_{BC}} \right) \right] \tag{8}$$

But, since

$$V_\lambda = \frac{Q_\lambda}{C_{BE} + C_{BC}}$$

this in turn converts to

$$V_{on} = \left(\frac{Q_\lambda}{C_{BC}} \right) - 0.6 \left[1 + \left(\frac{C_{BE}}{C_{BC}} \right) \right] \tag{9}$$

It can be seen that the voltage termed V_{on} is directly proportional to the integrated charge. This is the output voltage (V_{out}) read in the integration mode (i.e., $V_{on} \equiv V_{out}$). The last term in this equation is the term referred to at the beginning of the analysis and appears because of the long read-out period (figure 4-1(a) and accompanying discussion). This term represents the voltage lost in turning on the base-emitter diode and subtracts from the lower end of the dynamic range, as can be seen when we consider that V_{out} cannot fall below zero volts. The light generated charge needed to bring V_{on} just to zero volts is, from (9),

$$\left(\frac{Q_\lambda}{C_{BC}} \right) = 0.6 \left[1 + \left(\frac{C_{BE}}{C_{BC}} \right) \right].$$

Thus, at least this much light generated charge is lost in turning on the transistor.

Realizing this, (9) must be modified when expressed in terms of V_{out} to read (for Case I, where a long readout time is assumed such that no voltage appears across the base-emitter diode at the end of readout)

$$V_{out} = \left(\frac{Q_\lambda}{C_{BC}} \right) - 0.6 \left[1 + \left(\frac{C_{BE}}{C_{BC}} \right) \right]; \text{ for } \left(\frac{Q_\lambda}{C_{BC}} \right) > 0.6 \left[1 + \left(\frac{C_{BE}}{C_{BC}} \right) \right]$$

$$V_{out} = 0; \qquad \text{ for } \left(\frac{Q_\lambda}{C_{BC}} \right) \le 0.6 \left[1 + \left(\frac{C_{BE}}{C_{BC}} \right) \right] \tag{10}$$

At this point, assuming the first condition in (10), the time constant increases to $\beta R_L C_{BC}$, since the transistor is on and C_{BE} is fully charged to 0.6 volt. The output waveform will look as shown in figure 4-2. The point of turn on (V_{out}) is the desired output, since it is proportional to Q_λ and is independent of β. The transient spike in figure 4-2 prior to V_{out} represents a noise voltage in the output. There are several ways of minimizing this spike, however. First of all, in sensor arrays there will normally be a device turning off for each device turning on, and the two noise spikes thus created are similar in amplitude and opposite in polarity so that they should cancel to some extent in the common output load resistor. Secondly, the rise time of the sampling pulse τ_s will normally be longer than the time constant (τ) of the noise transient (see equation (5)), since the values of C_{BE} and C_{BC} are quite small. For instance, in a representative silicon n-p-n mosaic, typical values are $R_L = 2K$ and $C_{BC} = C_{BE} = 0.2$ pF so that $\tau = 0.2$ ns. The τ_s factor should be small compared to $\beta R_L C_{BC}$, however, so that no active discharge begins prior to the application of full bias to the sensor. This means that it is desirable that:

$$+V_{cc}$$

$$\tau = \frac{C_{BC} C_{CE} R_L}{C_{BC} + C_{BE}}$$

$$V_{OUT}$$

$$\tau = \beta R_L C_{BC}$$

$$0V \qquad\qquad 0V$$

$$\tau = \frac{C_{BC} C_{BE} R_L}{C_{BC} + C_{BE}}$$

SAMPLE PERIOD

72-0581-VA-70-1
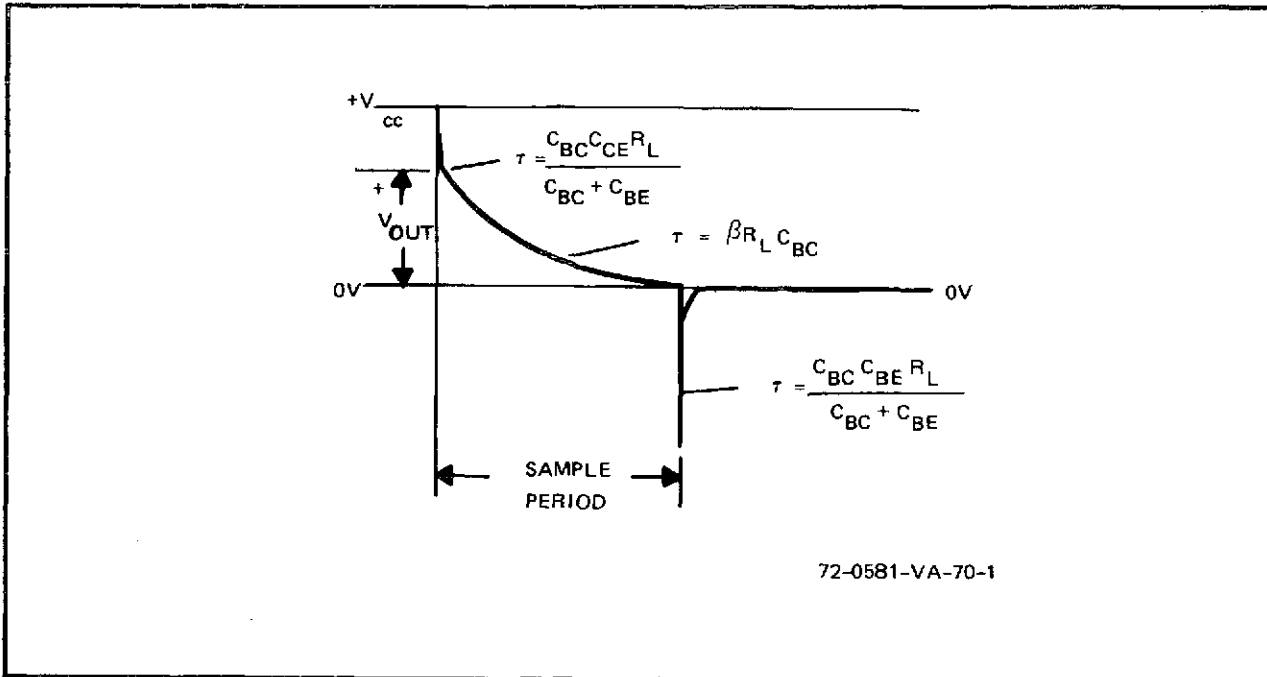
Figure 4-2. Output Waveform - Phototransistor Integration Mode

$$R_L \left(\frac{C_{BE} \, C_{BC}}{C_{BE} + C_{BC}} \right) < r_s < R_L \, C_{BC},$$

which can be achieved by minimizing C_{BE} with respect to C_{BC}.

Recalling again that Q_λ cannot exceed Q_t, it is found, upon plugging the expression (1) for $Q_\lambda = -Q_t = C_{BC} \, V_{cc}$ into (10), that

$$V_{out_{max}} = V_{cc} - 0.6 \left[1 + \left(\frac{C_{BE}}{C_{BC}} \right) \right]. \tag{11}$$

Hence, to increase the dynamic range at the lower end by extending the minimum detectable light level and at the high end by increasing the maximum output voltage, it is necessary to decrease C_{BE} with respect to C_{BC} so that the second term of (11) is minimized at 0.6 volt. As will be seen later, decreasing C_{BE} in mosaic devices has several other advantages.

The analysis presented above assumes a long readout time such that the readout current goes to zero (Case I). As the current in the base-emitter diode decreases, its resistance becomes very large, and in practice a very long time would be required to achieve zero volts across the base-emitter junction. It is also seen that letting this voltage go to zero results in a term which subtracts from the output. We now derive an equation for V_{out} where we consider the voltage at the base not equal to zero at the end of readout. In the analysis we will consider the base-emitter junction to have an ideal diode characteristic; i.e., $i_d = 0$ for $V_d \leq 0.6$, and $i_d > 0$ for $V_d > 0.6$, where i_d will be limited by the load resistance. The analysis breaks up into two subcases. The first of these (Case II) considers a readout condition prior to reverse-biasing where all the signal is readout, but where reverse-biasing occurs before the base-emitter voltage is allowed to drop to zero. This implies that $0 < V_1 \leq 0.6$ volt, where V_1 equals the voltage on the base at the end of readout, and that, considering an ideal diode, $i_d = 0$. For this case (instantaneously before reverse-biasing),

$$V_{bc} = (V_{cc} - V_1)$$
$$V_{be} = V_1$$
$$V_{bn} = V_1$$
$$V_{en} = 0 \qquad ; \qquad (i_d = 0).$$

The steps described in analyzing the long readout case, (1) through (9), can now be carried out, taking into account the additional voltage V_1 on the base. The output expression which is obtained is

$$V_{out}^{II} = (V_1 - 0.6) \left[1 + \left(\frac{C_{BE}}{C_{BC}} \right) \right] + \left(\frac{Q_\lambda}{C_{BC}} \right) \qquad (10a)$$

where, as before, $Q_\lambda = V_\lambda (C_{BC} + C_{BE})$. Since this case requires that $0 < V_1 \leq 0.6$ volt, it can be seen that the amount of light generated charge needed to forward-bias the base-emitter diode has been reduced to

$$\left(\frac{Q_\lambda}{C_{BC}} \right) = (V_1 - 0.6) \left[1 + \left(\frac{C_{BE}}{C_{BC}} \right) \right];$$

with the result that if we set $V_1 = 0.6$ (i. e. , a readout cycle which lasts just exactly long enough to read out the light generated signal), the output will simply be

$$V_{out} = \left(\frac{Q_\lambda}{C_{BC}} \right).$$

This condition is the ideal optimum, but for a practical application with considerable dynamic range (i. e. , from cycle to cycle a different amount of Q_λ is generated) and where the readout time is constant for each cycle; the readout time cannot be set so that exactly 0.6 volt is left on the forward-biased base-emitter diode at the end of every readout cycle. Practically, the readout time would be set according to the light levels expected.

In this case, the expression derived for $V_{out_{max}}$ proves to be

$$V_{out_{max}}^{II} = V_{cc} - 0.6 \left[1 + \left(\frac{C_{BE}}{C_{BC}} \right) \right] \qquad (11a)$$

which is the same peak output as given for Case I. Hence, it follows that by reading out in such a way that some value of V_1 volts is left on the base-emitter diode, the minimum detectable signal can be increased by an amount

$$V_1 \left[1 + \left(\frac{C_{BE}}{C_{BC}} \right) \right],$$

while still being able to read the same maximum output signal level. The dynamic range and the detectivity have thus been increased. So, for Case II where we read out only to the point where V_1 volts remains across the base-emitter diode (with $0 < V_1 \leq 0.6$), the general expression for the output is given by (10a). It will, however, be seen that, for $V_1 = 0$ (i.e., the long readout time first described), the (10a) equation for V_{out} reduces to that in (10); as it should.

In the second modification of Case I, we assume a sufficiently short read-out time that the signal from the previous cycle is not completely readout. This corresponds to leaving V_2 volts on the base upon reverse-biasing, where $0.6 < V_2 < V_{cc}$. For the first time, we now have a current flow in the load resistor at the end of readout. This situation will be denoted as Case III. It assumes the following conditions:

$$V_{bc} = (V - V_2)$$

$$V_{be} = 0.6 \text{ volt (an ideal forward-biased diode)}$$

$$V_{bn} = V_2$$

$$V_{en} = V_2 - 0.6 ; \quad (i_d \neq 0)$$

Again applying the previous analysis to this case, we obtain an output of

$$V_{out}^{III} = V_{NRO}^{(n-1)} + \left(\frac{Q_\lambda}{C_{BC}} \right) \tag{10b}$$

where

$$V_{NRO}^{(n-1)} = V_{en}^{(n-1)} = V_2^{(n-1)} - 0.6$$

denotes the amount of light generated voltage from the previous (n-1) cycle which was not read out. As before, $Q_\lambda = V_\lambda (C_{BC} + C_{BE})$. Here it will be seen that, under the stipulation that $0 < V_{NRO}^{(n)} < V_{cc} - 0.6$, the base-emitter diode will still be forward biased at the end of the n'th readout cycle. Subsequently, no charge will be needed to turn it on at the beginning of the next (n+1) cycle and the readout voltage obtained will be the sum of the light generated voltage during the (n+1)th integration period plus the light generated voltage which was left following the n'th cycle. As with both previous cases, the expression for $V_{out_{max}}$ is

$$V_{out_{max}}^{III} = V_{cc} - 0.6 \left[1 + \left(\frac{C_{BE}}{C_{BC}} \right) \right] \tag{11b}$$

Thus, for readout in Case III, we sense not only the light generated charge from the particular integration period, but also the light generated charge left over from the previous cycle which was not fully read out. While the maximum voltage which can be obtained is still the same, the maximum signal which can be generated solely within the specified integration cycle is reduced by V_{NRO} according to

$$V_{signal_{max}}^{III} = V_{out_{max}} - V_{NRO}^{(n-1)}$$

The foregoing development of the charge storage concept has been simplified in a number of respects. It was, for instance, assumed that the values of C_{BC} and C_{BE} were constant throughout the operating cycle. Actually, these capacitances are voltage sensitive, and the expression for the voltage discharge during the integration period should technically take these variations into account by being modified to allow for

$$V_c = \left[(V_o + V_a)^{(1-n)} - \left(\frac{I_\lambda t}{C_o} \right) \right]^{\left(\frac{1}{1-n} \right)} - V_a$$

where:

$V_{c'}$ = instantaneous voltage across the respective junction capacitance

V_o = initial voltage across capacitance $\left[\text{normally zero as per prior analysis}\right]$

V_a = built-in junction potential

C_o = initial value of capacitance $\left[\text{under initial } V_o \text{ biasing conditions}\right]$

I_λ = leakage plus light generated junction current

n = junction characteristic factor $\left[\frac{1}{2} \text{ for step junction or } \frac{1}{3} \text{ for graded junction}\right]$

It will usually be found, however, that the computational complications thus introduced contribute little to an understanding of the basic processes at work. They were, therefore, avoided completely in the present discussion.

4.1.2 Junction Capacitance Ratios

On reviewing the equation for V_{out} in the foregoing analysis section, it can be seen that one of the prime objectives in designing a phototransistor structure to be operated in the integration mode is to maximize the ratio of C_{BC} to C_{BE}. This, in effect, maximizes the dynamic range of the device for a given absolute value of C_{BC}. In addition, C_{BE} should be minimized to reduce the charge required to forward bias the base-emitter diode, since this charging must take place through R_L and, as mentioned previously, becomes a source of transient noise in the output. Fortunately, the time constant for this charging is not multiplied by beta and is therefore of short duration compared to the true output.

The absolute value of C_{BC} should also be optimized, since V_{out} is inversely and Q_t directly proportional to C_{BE}. Where high light levels are to be encountered such that saturation cannot be prevented by providing a shortened integration time, a high value of C_{BC} is desirable to increase Q_t. Decreasing C_{BC} to increase output voltage in lower level applications can

easily be carried to extremes. Even if C_{BE} can be kept small in comparison, when Q_t is extremely small the resulting lack of base drive for the phototransistor increases the beta dependence of the device.

4. 1. 3 Array Phototransistors

We will now extend our discussion to arrays of phototransistors operating in the integration mode. Figure 4-3 shows a section of the type silicon mosaics used in the solid-state imaging systems developed on this program. Collector strips delineate each row of elements. Thus, all phototransistors in a given row have a common collector. Discrete base and emitter regions are diffused into the collector strip to form individual transistors. Vapor deposited aluminum leads tie the emitters of each column of phototransistors together across the strip collector structures. Each common emitter line is (for analysis purposes here) attached to an FET switch, which is then connected to the output load. Access to each element is obtained by applying a bias voltage to its collector strip and by closing the FET switch connected to its emitter line. To prevent gross crosstalk between elements, the collector strips must have a low resistance. Isolation between emitters in a row is inherently provided by the dual-junction (diode-diode) nature of each phototransistor. Figure 4-4 depicts the approximate electrical equivalent circuit for a mosaic and the cited switches.

The fabrication of multiple phototransistors in the strip collector array configuration described above complicates the description of the integration mode of operation. Because the emitters of a column are tied together, each transistor along the line will see tied to its emitter a capacitance (C_{PT}) equal to

$$(M - 1) \left(\frac{C_{BE} C_{BC}}{C_{BC} + C_{BE}} \right) = C_{PT}$$

INTERNAL COLLECTOR STRIPS Y
SURFACE EMITTER STRIPS X

ISOLATION   ISOLATION

COLLECTOR   COLLECTOR   COLLECTOR
ROW Y$_n$ ROW Y$_{n+1}$ ROW Y$_{n+2}$

COLLECTOR
CONTACT POINT

EMITTER ROW X$_n$

EMITTER ROW X$_{n+1}$

EMITTER ROW X$_{n+2}$

EMITTER   EMITTER

INTERNAL STRIP COLLECTOR
INTERCONNECTION
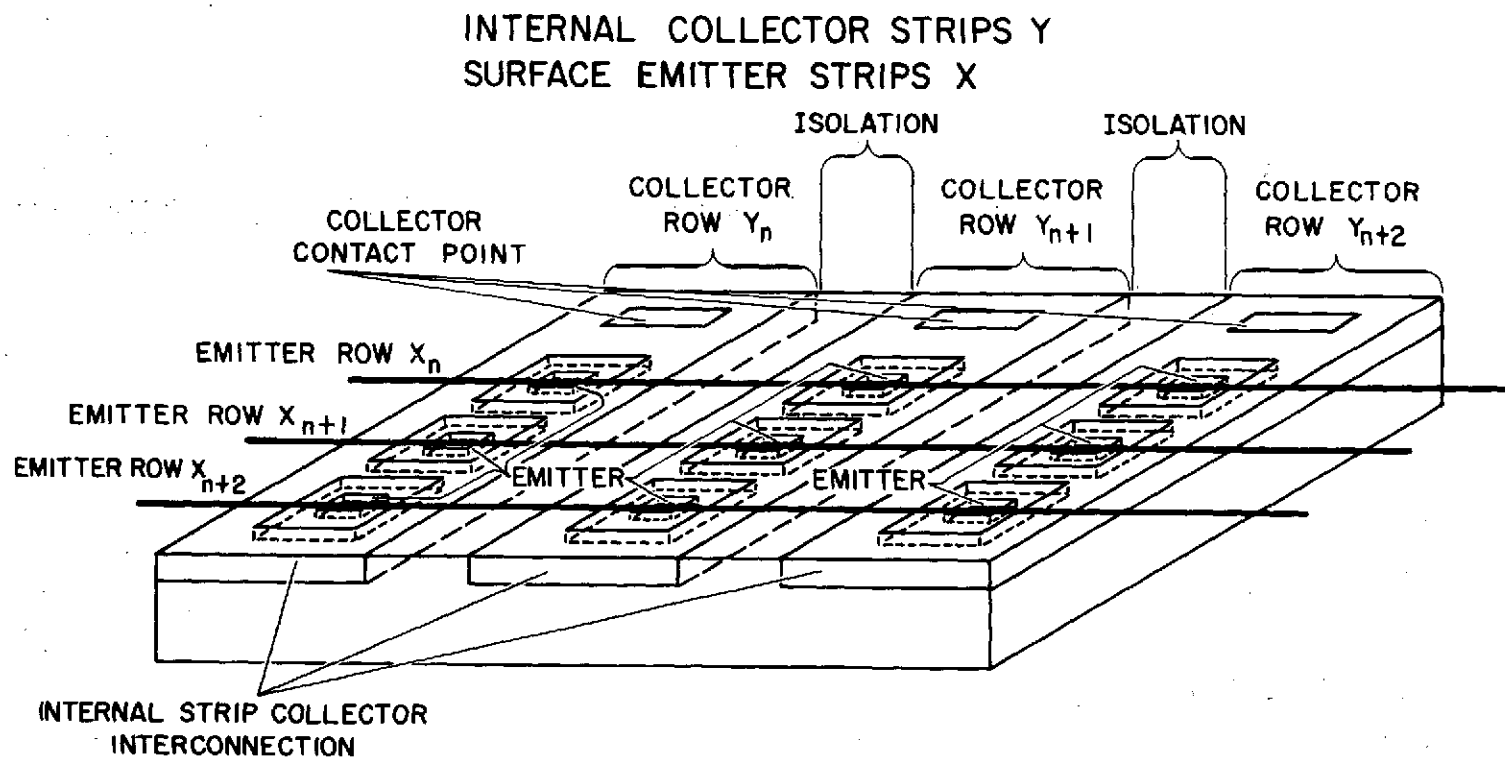
S5441A-VB-I-2

Figure 4-3. Section of Collector Strip - Mosaic Configuration
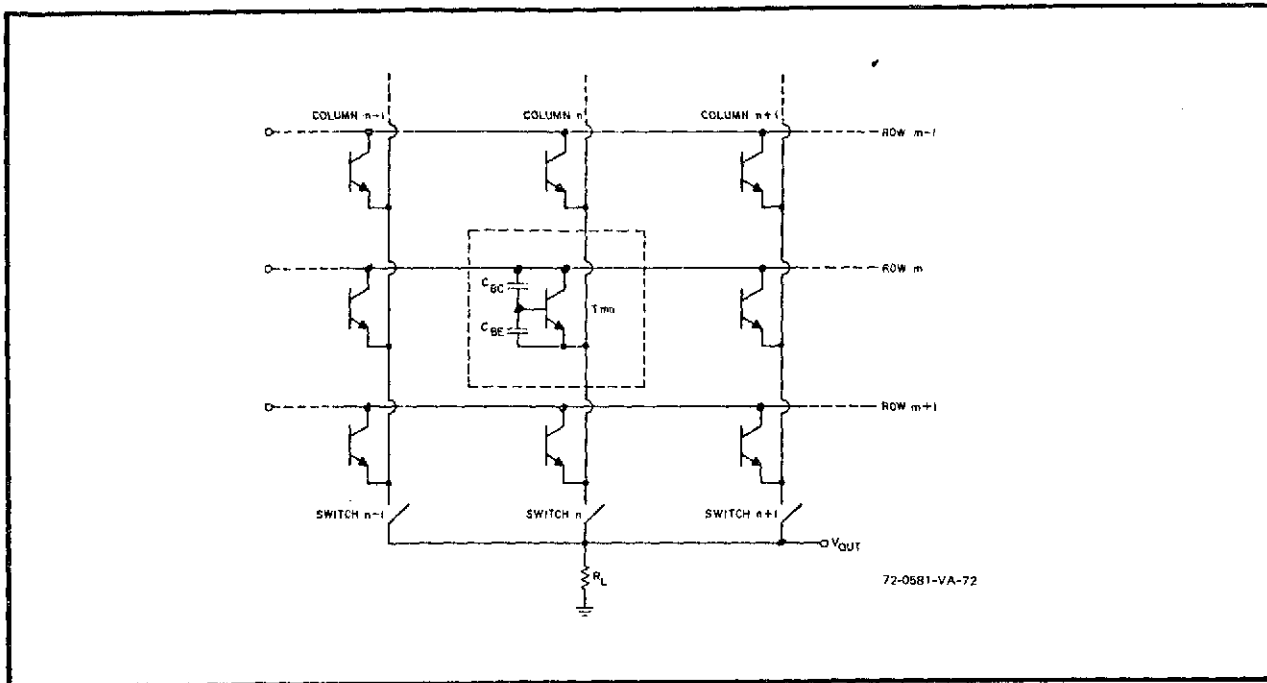
Figure 4-4. Equivalent Circuit of Mosaic-Strip Collector
Configuration

where M is the number of phototransistors in the column. This is just the parallel combination of the equivalent (series) capacitance of all other photo-transistors, connected to the column (figure 4-5). Since the emitter lines of the array are left floating when none of its transistors are being read out, this capacitance couples the emitter line to ground through the low impedance collector strips. In the analysis that follows we will see that this capacitance lowers the output voltage in the readout phase by sharing the output voltage with C_{BC} and increasing the readout time constant. In addition, it allows the voltage at the emitter to vary from ground: an effect that will be discussed in detail later.

Analysis of the operation of a phototransistor in a mosaic closely follows the analysis presented for a discrete phototransistor when certain obser-vations and assumptions are made. First, since typically M is fairly large

4-16

$(>100$ in mosaics of reasonable resolution), it will be seen that $C_{PT} >> C_{BE}$ independent of the values of C_{BE} and C_{BC} (unless, of course, C_{BE} is on the order of $(M - 1)\ C_{BC}$; a case which was previously shown to be intolerable for the single phototransistor case as well). Secondly, it is assumed that the collector strip resistance can be approximated as zero. Thirdly, that the effects of switch resistance and capacitance are made negligible through the use of an ideal switch (effects of switches will be discussed later). And finally, provided the value of C_{BE} is smaller than C_{BC}, so that variations in emitter voltage across C_{PT} (discussed above)— which appear across the series combination of C_{BC} and C_{BE}--are felt primarily across C_{BE}. Later we will see that a high positive voltage coupld appear at the base of the phototransistor if this assumption is not valid. Such a voltage would forward bias the base-collector diode, causing transistor action in the reverse direction and destroying phototransistor operation.

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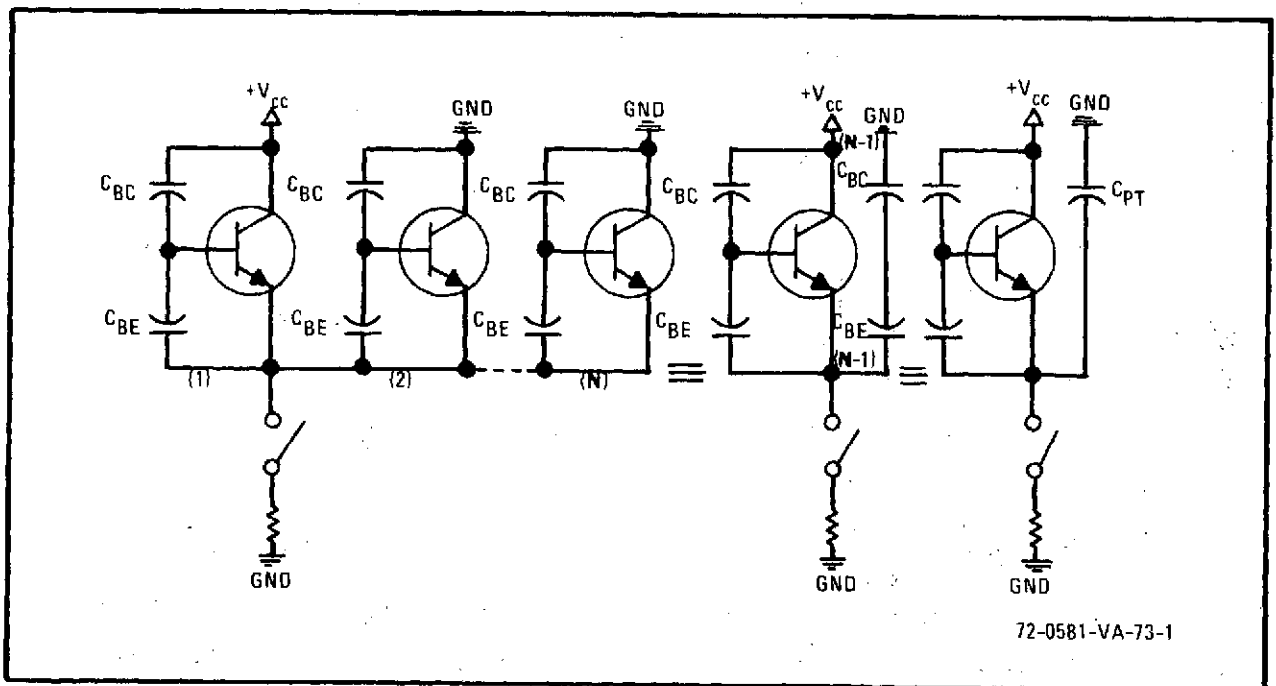
Figure 4-5. Common Emitter Line Capacitance

4-17

We will analyze the operation of a transistor in the mosaic designated as element T_{mn}, where the subscript "m" refers to the row in which it is located and the subscript "n" refers to its column location. The mosaic has a total number of rows = M and a total number of columns = N. Operation of the mosaic entails reading out all the phototransistors in the following sequence: T_{11}, T_{12} ..., T_{1N}, T_{21} ... T_{2N}, ..., T_{m1} ... T_{MN}. The integration period for each element is the period of time between samplings of that element.

We will begin the analysis by observing T_{mn} at the end of its readout phase. This starting point is taken because any prior charge distribution on C_{BE}, C_{BC}, and C_{PT} for transistor T_{mn} is erased. A long readout condition similar to the single transistor Case I is assumed.

a. End of Readout of T_{mn} (figure 4-6(a) . The same first step conditions which were given in Case I for a single phototransistor apply since C_{PT} is shorted out by the load; i.e.,

$$V_{bc} = +V_{cc}$$

$$V_{bn} = 0$$

$$V_{en} = 0.$$

b. Readout of Transistors $T_{m, n+1}$, $T_{m, n+2}$ .... $T_{m, N}$ (viz., the rest of the elements in collector strip "m" in figure 4-6(b)). During this time the load resistor no longer appears across C_{PT}, but no current flows in T_{mn} since there is no change in potentials. Thus, the same condition as in (a) continues to prevail.

c. Readout of Transistors $T_{m+1, 1}$, $T_{m+1, 2}$ ..., $T_{m+1, n-1}$ (which are all the transistors, in the next collector strip, up to the one whose emitter is tied to T_{mn}). Two different conditions prevail in this phase which are linearly superimposed as follows. First, T_{mn} becomes reversed biased

as its collector row is grounded. By this action the charge stored initially on C_{BC} alone becomes shared with C_{BE} and C_{PT}. By charge conservation

$$Q_t = -V_{cc} C_{BC} = V_{bn} \left[C_{BC} + \frac{C_{BE}}{\left(\frac{C_{BE}}{C_{PT}}\right) + 1} \right] \quad ;$$

but, since $C_{PT} \gg C_{BE}$, is is seen that

$$\frac{C_{BE}}{\left(\frac{C_{BE}}{C_{PT}}\right) + 1} \; \tilde{\rightarrow} \; C_{BE}$$

which means that the base node potential will be expressed as

$$V_{bn} = \left(\frac{-C_{BC}}{C_{BC} + C_{BE}}\right) V_{cc},$$

and this will be recognized as the same condition which prevailed upon reverse biasing a single phototransistor. Hence, the effect of C_{PT} is to put a slightly negative voltage on V_{en} when the transistor is reverse biased. But, since $C_{PT} \gg C_{BE}$ and C_{BE} is of the same order of magnitude as C_{BC} (usually smaller is desired), the level of this voltage is very low and essentially $V_{en} \cong 0$.

In addition, notice that transistor $T_{m+1, n}$ becomes forward biased since its emitter is grounded through C_{PT}. A positive voltage, which will here be called V_x, correspondingly appears across C_{PT}. This voltage is dependent upon the signal voltages on $T_{m+1, n}$ and the ratio of $\beta C_{BC} + C_{PT}$ due to transistor $T_{m+1, n}$ being active. This voltage is of the order of magnitude

4-19

$$V_{bn} = \left(\frac{-C_{BC}}{C_{BC}+C_{BE}}\right)V_{cc} + \left(\frac{C_{BE}}{C_{BE}+C_{BE}}\right)V_{en}$$

(c) $V_{en} = V_x$

$$V_{bn} = \left(\frac{-C_{BC}}{C_{BC}+C_{BE}}\right)V_{cc}$$

(d) $V_{en} = 0$

$$V_{bn} = \left(\frac{-C_{BC}}{C_{BC}+C_{BE}}\right)V_{cc}$$

$V_{en} = 0$ (e)

$V_{en} \cong 0$

$$V_{bn} = \left(\frac{-C_{BC}}{C_{BC}+C_{BE}}\right)V_{cc} + V_\lambda$$

(f)

$$V_{bn}{}^0 = \left(\frac{-C_{BC}}{C_{BC}+C_{BE}}\right)V_{cc} + V_x \Bigg\}\ \text{INITIAL CONDITIONS}$$

$V_{en}{}^0 \approx 0$

(g)
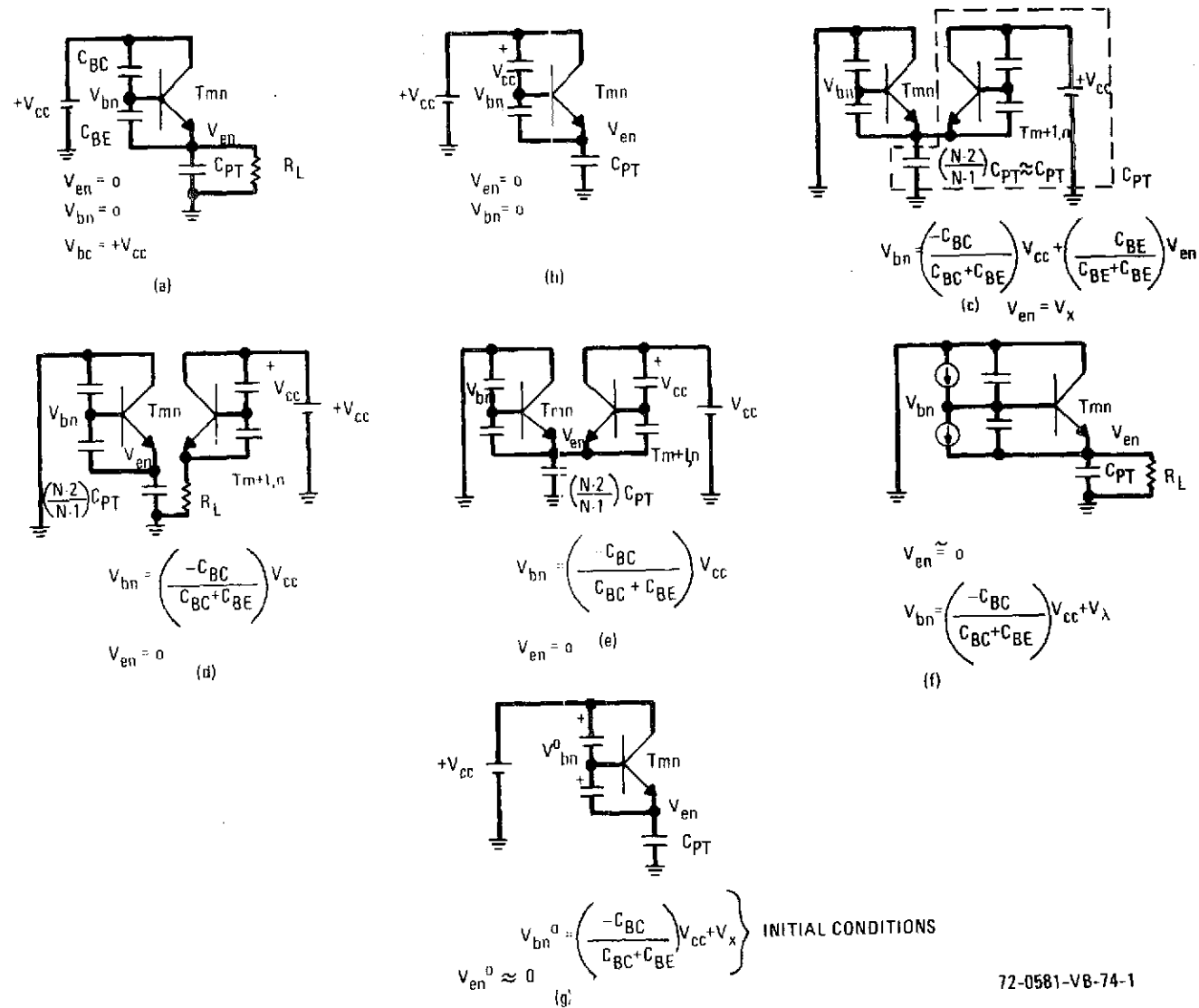
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Figure 4-6.   Operation of Phototransistor in Mosaic

of $\beta\left[C_{BC}/(\beta C_{BC} + C_{PT})\right] V_{cc}$ and can be appreciable for a large β and C_{BC} on the order of C_{BE}, because βC_{bc} is then on the order of C_{PT}. Voltage V_x is shared across the C_{BE} and C_{BC} capacities of transistor T_{mn} and, if $C_{BE} \approx C_{BC}$, approximately $V_x/2$ appears at the base of T_{mn}. This excess voltage is linearly superposed upon V_{bn}, which was originally $-V_{cc}\left[C_{BC}/(C_{BC} + C_{BE})\right]$ due to reverse biasing and which rises toward ground with incident light. There is a possibility that the rise due to V_x will turn T_{mn} on in the reverse direction and thereby destroy the desired operation. Observe, however, that as C_{BE} becomes larger for a fixed C_{BC} (increasing the positive voltage across the base-collector), C_{PT} also becomes larger, tending to reduce the voltage V_x at the emitter. This reduces its contribution at the base. For $C_{BE} \ll C_{BC}$, most of the voltage V_x will be dropped across C_{BE}, and the base will stay negative. Under the reasonable assumption that the ratio of C_{BE} to C_{BC} is such that T_{mn} does not go into reverse transistor operation when V_x appears at its emitter, the final base voltage at this time (figure 4-6(C)) will be

$$
V_{bn} \cong \left(\frac{-C_{BC}}{C_{BC} + C_{BE}}\right) V_{cc} + \left(\frac{C_{BE}}{C_{BE} + C_{BC}}\right) V_{en}
$$

where $V_{en} = V_x$ is some positive voltage.

    d. <u>Read Transistor $T_{m+1, n}$</u> (the transistor sharing the emitter line with T_{mn} in figure 4-6(d)). The load is now switched onto emitter line "n" discharging C_{PT} from V_x to ground. The base voltage now returns to

$$
V_{bn} = \left(\frac{-C_{BC}}{C_{BC} + C_{BE}}\right) V_{cc}
$$

and
$$
V_{en} = 0.
$$

e. Read Transistors $T_{m+1, n+1}, \ldots T_{m+1, N}$ (figure 4-6(e)). There is no change across T_{mn} during this time since there is no current flow in transistor $T_{m+1, n}$ or T_{mn}.

f. Readout of all the Remaining Transistors in the Mosaic up to $T_{m-1, N} \ldots$ (reading out the transistors remaining up to the first one in the row of T_{mn}, i.e., $T_{m+2, 1} \ldots T_{m+2, n}; \ldots T_{M, 1} \ldots T_{M, N}; \ldots T_{11}, \ldots T_{1N}; \ldots T_{m+1, N}$). The remaining phototransistors are now read out, and the analysis for each row follows exactly the analysis for row m+1. For each row read out, the voltage at the emitter of T_{mn} goes up to some positive voltage (V_x) and then returns to ground. The base voltage of the end of each of these readout periods is still

$$V_{bn} = \left(\frac{-C_{BC}}{C_{BC} + C_{BE}} \right) V_{cc}$$

and the emitter voltage is zero.

g. Integration. Light plus leakage generated charges dimenish the voltage on the base of T_{mn} between the times it was read out. During this interim period the equivalent circuit in figure 4-6(f) is effective. The charge disturbing base voltage is expressed as

$$Q_\lambda = V_\lambda \left(C_{BC} + \left[\frac{C_{BE}}{\left(\frac{C_{BE}}{C_{PT}} \right) + 1} \right] \right) \simeq V_\lambda (C_{BC} + C_{BE})$$

where V_λ is the voltage change on the base due to integration, and the latter approximation is valid due to $C_{PT} \gg C_{BE}$.

The base node voltage is accordingly altered as

$$V_{bn} = \left(\frac{-C_{BC}}{C_{BC} + C_{BE}} \right) V_{cc} + V_\lambda$$

while the emitter potential remains essentially zero due to the load resistor effectively shunting C_{PT}.

h. Readout of Transistors $T_{m,1} \cdots T_{m,n-1}$ (the transistors preceding element T_{mn} along row "m" in figure 4-6(g)). The readout collector voltage V_{cc} is applied to T_{mn}. The load resistor is not switched across C_{PT}, however, since T_{mn} is not yet being read out. Current will flow through C_{BC}, C_{BE}, and C_{PT} until $V_{BE} = +0.6$, at which point the transistor will turn on. The amount of charge that mut flow to make this voltage appear across C_{BE} is derived from figure 4-7(a) to be

$$\Delta Q = \Delta V_{be} C_{BE}$$

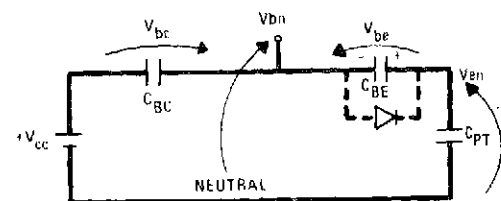$$= \left[+0.6 - V_{bn}^{\,0} \right] C_{BE}$$

where

$$V_{bn}^{\,0} = \left(\frac{-C_{BC}}{C_{BC} + C_{BE}} \right) V_{cc} + V_\lambda$$

with superscript "0" denoting "value-after-integration."

Once this amount of charge has flowed through C_{BC} and C_{PT} in series, the change in the base voltage will be

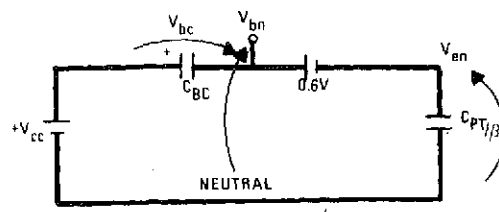$$\Delta V_{bn} = \left[0.6 - V_{bn}^{\,0} \right] \left(\frac{C_{BE}}{C_{BC}} \right)$$

4-23

Figure 4-7.   Equivalent Circuits of Phototransistor T_{mn}

while that in the emitter voltage is

$$\Delta V_{en} = \left[0.6 - V_{bn}^{\ 0} \right] \left(\frac{C_{BE}}{C_{PT}} \right) \approx 0.$$

The transistor will now turn on, shorting out C_{BE} (figure 4-7(b)). Since the transistor is on, the reflected capacitance of C_{PT} into the base is C_{PT}/β. The voltage appearing on C_{BC} at turn on is

$$V_{bc}^{\ 0} = V_{bn}^{\ 0} + \Delta V_{bc} = \left(\frac{-C_{BC}}{C_{BC} + C_{BE}} \right) V_{cc} + V_\lambda \left[0.6 - V_{bn}^{\ 0} \right] \left(\frac{C_{BE}}{C_{BC}} \right).$$

The difference between the supply voltage, less 0.6 volt dropped across the base-emitter diode, and the initial voltage on C_{BC} will be shared across C_{BC} and C_{PT}/β. Hence, the voltage at the emitter of T_{mn} just prior to closure of the emitter line sampling (or commutation) switch is

$$V_{en} = \left\{ V_\lambda + V_{bn}^{\ 0} \left(\frac{C_{BE}}{C_{BC}} \right) - 0.6 \left[1 + \left(\frac{C_{BE}}{C_{BC}} \right) \right] + V_{cc} \left(\frac{C_{BE}}{C_{BE} + C_{BC}} \right) \right\}$$
$$\left(\frac{\beta C_{BC}}{\beta C_{BC} + C_{PT}} \right)$$

4-24

but,

$$V_{bn}{}^0 = V_\lambda - V_{cc} \left(\frac{C_{BC}}{C_{EC} + C_{BE}} \right)$$

so,

$$V_{en} = \left\{ (V_\lambda - 0.6) \left[1 + \left(\frac{C_{BE}}{C_{BC}} \right) \right] \right\} \left[\frac{1}{1 + (C_{PT}/\beta C_{BC})} \right].$$

Then, since $V_\lambda = \left[Q_\lambda / (C_{BE} + C_{BC}) \right]$, it follows that

$$V_{en} = \left\{ \left(\frac{Q_\lambda}{C_{BC}} \right) - 0.6 \left[1 + \left(\frac{C_{BE}}{C_{BC}} \right) \right] \right\} \bigg/ \left[1 + \left(\frac{C_{PT}}{\beta C_{BC}} \right) \right]. \tag{12}$$

Observe that this relationship is the same as the peak output expression obtained for the single transistor case, except that the signal voltage has been reduced by the factor $\left[1 + (C_{PT}/\beta C_{BC}) \right]$. Since decreasing the ratio of C_{BE} to C_{BC} will decrease C_{PT} relative to C_{BC}, it is seen that decreasing C_{BE} relative to C_{BC} also reduces the effective signal division at the output.

When the load resistor is switched across C_{PT} at the emitter of T_{mn}, the instantaneous voltage read out is $V_{en} = V_{out}$. We see, consequently, that the read out voltage follows the same form as V_{out} for a single photo-transistor, although voltage divider action has taken place between βC_{BC} and C_{PT}. T_{mn} will subsequently discharge with a time constant $\tau = (\beta C_{BC} + C_{PT})R_L$ until C_{BC} charges to $+ V_{cc}$ at the end of readout. This is, as before, a first-order approximation, since the nonlinear resistance and capacitance of the base-emitter diode has not been included in the discharge time constant.

4.1.4 Switching Considerations

One obvious omission in the description above has been in not considering the presence of commutation switching in the emitter line, since in a system application typically only one load resistor is provided. The advent of junction field effect transistors (FET's) and insulated gate field effect devices (IGFET's or MOSFET's) has provided a semiconductor switch free of the offset voltage problems formerly associated with bipolar type analog switches. Because of this inherent advantage, discussion of commutation switches will be limited to FET types.

There are two conflicting requirements which must be met in the selection of a suitable FET switch for commutation application - low ON resistance and low device capacitance. ON resistance should be kept low in relation to the load resistor selected so that 1) the signal is not lost in voltage division between switch resistance and the load, and 2) variations in switch resistance do not become a sizable fraction of the load resistance and cause additional "pattern noise" in the output. Decreasing ON resistance requires increasing the physical dimensions of the channel, thus increasing gate capacitance and drain-to-source capacitance. Since a transient discharge is being sampled, switching noise coupled through the gate capacitance can be a serious limitation on the minimum detectable signal. The amount of charge coupled through C_{gate} must be less than the charge from βC_{BC} to prevent switching transients from masking the signal. In addition, variation of C_{gate} can cause pattern noise on the peak signal level when C_{gate} is not insignificant in comparison to βC_{BC}.

An additional source of difficulty encountered from the high capacitances associated with these switches is illustrated in figure 4-8. Since all the emitter switches are tied together at the load, the series combination of C_{DS} and C_{PT} for the (m-1) additional switches will appear in parallel across
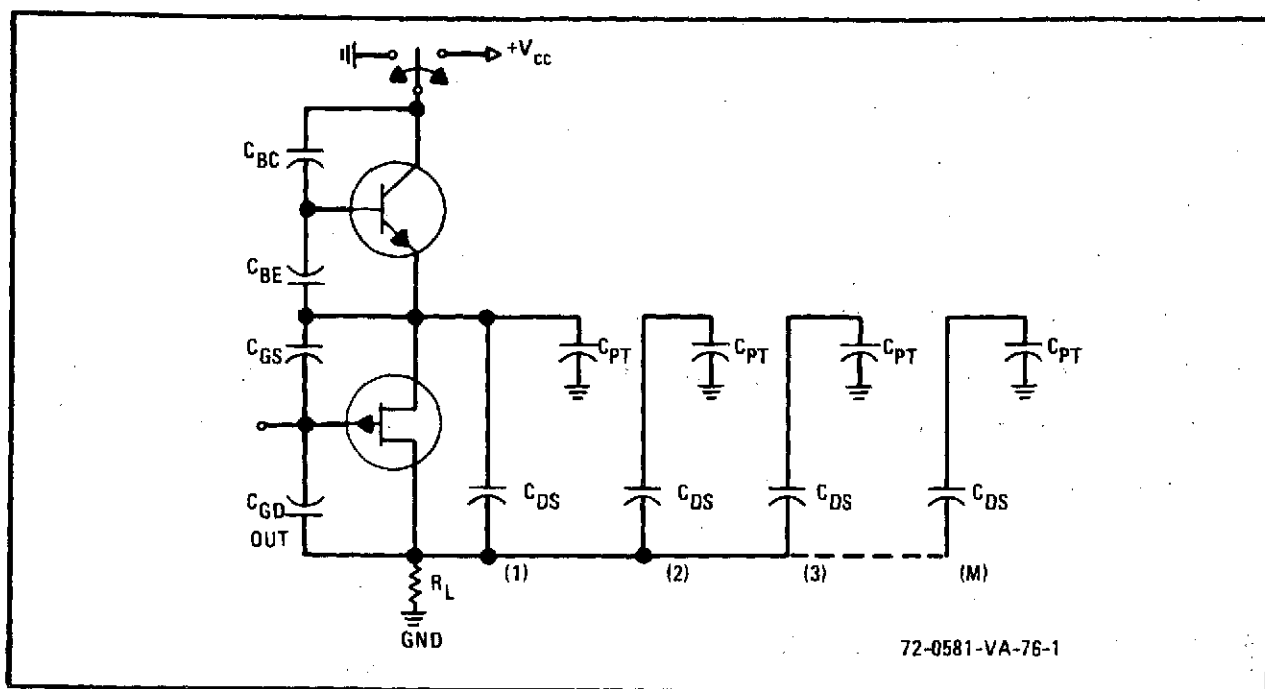
Figure 4-8. Emitter Line Switch Capacitance

the load.* Since C_{DS} normally is much smaller than C_{PT}, C_{DS} predominates and the total load capacitance is $C_L = (m-1)\, C_{DS}$; where "m" is the number of emitters per collector strip, and C_{DS} is the switching device's drain-to-source capacitance. C_L becomes a voltage divider against βC_{BC} (in a similar manner to C_{PT}) for not only the output signal but also for the output noise. An excessive C_{DS} can therefore significantly reduce signal output and increase the time constant required to completely read out the signal — an action which necessarily leads to crosstalk from one collector

---

*By providing an additional set of collector switches, the load resistor can be placed in the collector, thus removing the stipulated source of load capacitance and reducing the effect of switching transients in the output by switching the emitter to ground rather than to the load. The effect of the collector capacitance across the load is similar to the capacitance described here, however, and is of similar value.

strip to the next due to the signal charge that remains in the C_{DS} capacitance of a given switch to be read out on the next closure of that switch. In addition, if C_L becomes large compared to βC_{BC}, then β variations can have a pronounced affect on the output level.

The varity of our original statement that a compromise must be made between ON resistance and device capacitance of the commutator switches is thus aptly demonstrated. Any final selection of an FET switch must accordingly take into account the parameters of the mosaic with which it is to be used. Sensor output impedance, capacitance, and signal levels are the most important factors to be accounted for.

4.2 PERFORMANCE CHARACTERISTICS

An understanding of pulsed-bias integration mode sensing requires at least preliminary consideration of steady-state (fixed bias) photocurrent. Figure 4-9 illustrates the dc output current from a typical phototransistor as a function of incident light flux density from an incandescent source of
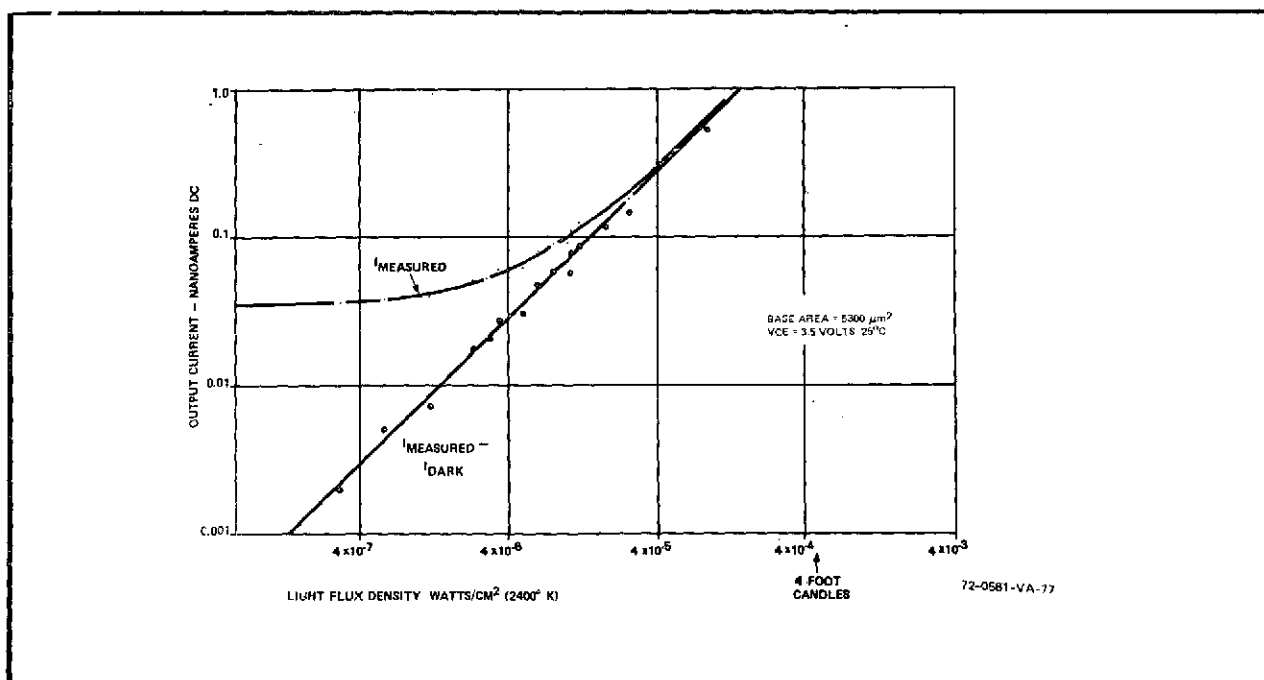

Figure 4-9. Steady State Phototransistor Response

source of 2400°K color temperature. The light levels shown match the usable sensitivity region for integration mode operation. The curve is characterized by two asymptotes: a dark current corresponding to thermally generated carriers, and a light-dependent term or photocurrent. The dark current is established at about 30 pA for this particular device and follows typical silicon junction behavior in doubling for every 8°C rise in temperature and varying roughly as the square root of the reverse collector-base voltage applied.

The photocurrent term, extrapolated from the curve by subtracting off dark response as shown, corresponds to a response characteristic of 7.5 x 10^{-6} A/W/cm^2. The extrapolated asymptote has unity slope, so photocurrent is a linear measure of incident light (instantaneous photon flux). Since the effective area for this transistor - slightly larger than the area outlined by the device's base diffusion oxide window - was 5,300 μm^2, this response term can alternately be expressed as 0.14 μA/μW.

The output plotted in figure 4-9 is I_{CEO} since no connection to the phototransistor base is made and it is allowed to float open circuited. Therefore, I_{CEO} represents the sum of the optically and thermally induced collector junction currents I_{CBO} (emitter open) times the transistor current gain beta. This steady-state photocurrent I_{CEO} is accordingly seen to be directly dependent on beta and exhibits all the variations of that parameter across a large array of sensors.

Figure 4-10 presents the same type of static performance data, but in a little different form, for a smaller geometry device out of a 200-x-256 element phototransistor array. Since the effective base area for this sensor is on the order of 1,800 μm^2, or roughly a factor of 3 less than that of the previous structure, it is seen that, while the absolute magnitudes of the leakages are different (again by approximately a factor of 3), the relative leakage current densitities—obtained by dividing $I_{leakage}$ by A_{base} — at identical supply levels of +3.5 volts are quite similar. Specifically,

large device: $I_1/A_b = \dfrac{30 \text{ pA}}{5300 \ \mu m^2} = 5.66 \ fA/\mu m^2 = 5.66 \ mA/m^2$

small device: $I_1/A_b = \dfrac{10 \text{ pA}}{1800 \ \mu m^2} = 5.56 \ fA/\mu m^2 = 5.65 \ mA/m^2$

Conversion Note: $fA = femto\text{-}Amp = 10^{-15} \ Amp = 10^{-12} \ mA$

and, $m^2 = 10^{12} \ \mu m^2$

Upon taking into account the uncertainty limits of experimental data, then allowing for the many processing parameter variations which can occur during fabrication of these devices, and finally discovering that the respective data was taken by different people at two points in time separated by nearly 3 years, such close agreement is little short of phenominal. By this very fact though, the data serves to emphasize the preciseness of the measurement techniques employed and confirms the scalability of the functional parameters of a known device to predict those of an unknown unit with only a knowledge of the relative difference in their sizes.

A further significant factor evident in the curves of figure 4-10 is a soft-kneed collector-emitter breakdown condition at just under +4 volts normal mode bias and just under -3 volts inverted mode bias. Existence of this general type of condition has been observed in nearly all operable matrix arrays from 10-x-10's to 400-x500's, and in many line array structures, It is responsible for limiting the upper end dynamic range of integrated array sensors. Origin of the effect is believed rooted in the high impurity concentration gradients ordinarily generated in forming the various junctions in these monoliths. Some success in increasing the knee point voltage has been achieved recently by adopting a slow-cool cycle following specific diffusion operations. This allows any lattice strain that has been induced during the diffusions to anneal out and permits the formation of less abrupt, more gradual junction transition regions having lower electric field intensities built in across the boundary.
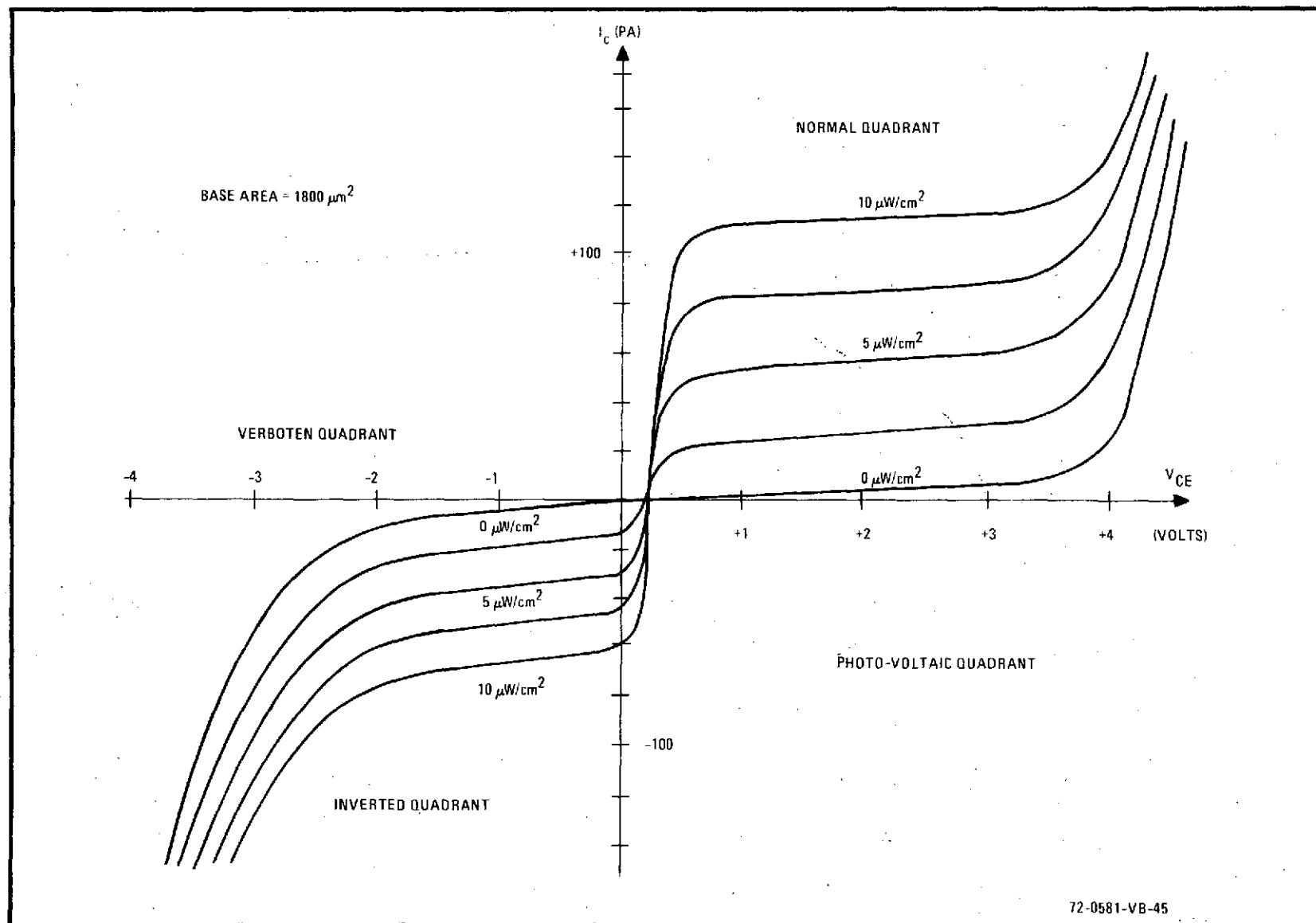
Figure 4-10. Irradiated-Base Output Family Characteristics
of Phototransistor

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To gain an insight into the interaction or degree of isolation between adjacent elements in rows of monolithic phototransistor, it is instructive to check into how the response of these sensing structures varies over their surface area. Measurements of this type involve the use of well focused, small diameter light spots swept in precise X-Y coordinates across a detector while observing its output. When the resulting data is plotted on a surface layout diagram of the element as a family of lines denoting relative response levels, a sensitivity contour map - analogous to land map contouring - will be obtained. Such a mapping is depicted in figure 4-11 for a representative small geometry phototransistor matrix array element. If a slice is taken vertically through the center of the sensor so as to look at a diffusion cross-section, the above data will yield a sensitivity profile map like that in figure 4-12. Here, the peaking effect occurring at those points where the base-collection junction comes to the surface are more vividly evident. The contour map, on the other hand, displays a more complete description of the distribution of such points.

Final points to note from these sensor sensitivity mappings are the existence of cross-talk regions and an extreme dip in the response in the vicinity of the emitter. This latter loss of output around the emitter is not intrinsic to the sensor structure but rather is caused by obscuration or shadowing of the emitter area by the aluminization metal strip used to commonalize successive devices along an array accessing emitter line. The extent of interaction between adjacent base areas lying along a common collector row is denoted by the cross-hatched regions in the inter-base space. For any specific array, the area commonly under adjacent sensitivity curves will be indicative of the relative optical cross-talk between elements in that array.

Now, considering the dynamic pulsed mode characteristics of phototransistors, the first factor to check out is the effect storage time has on junction leakage. Figure 4-13, which appears quite similar to the static
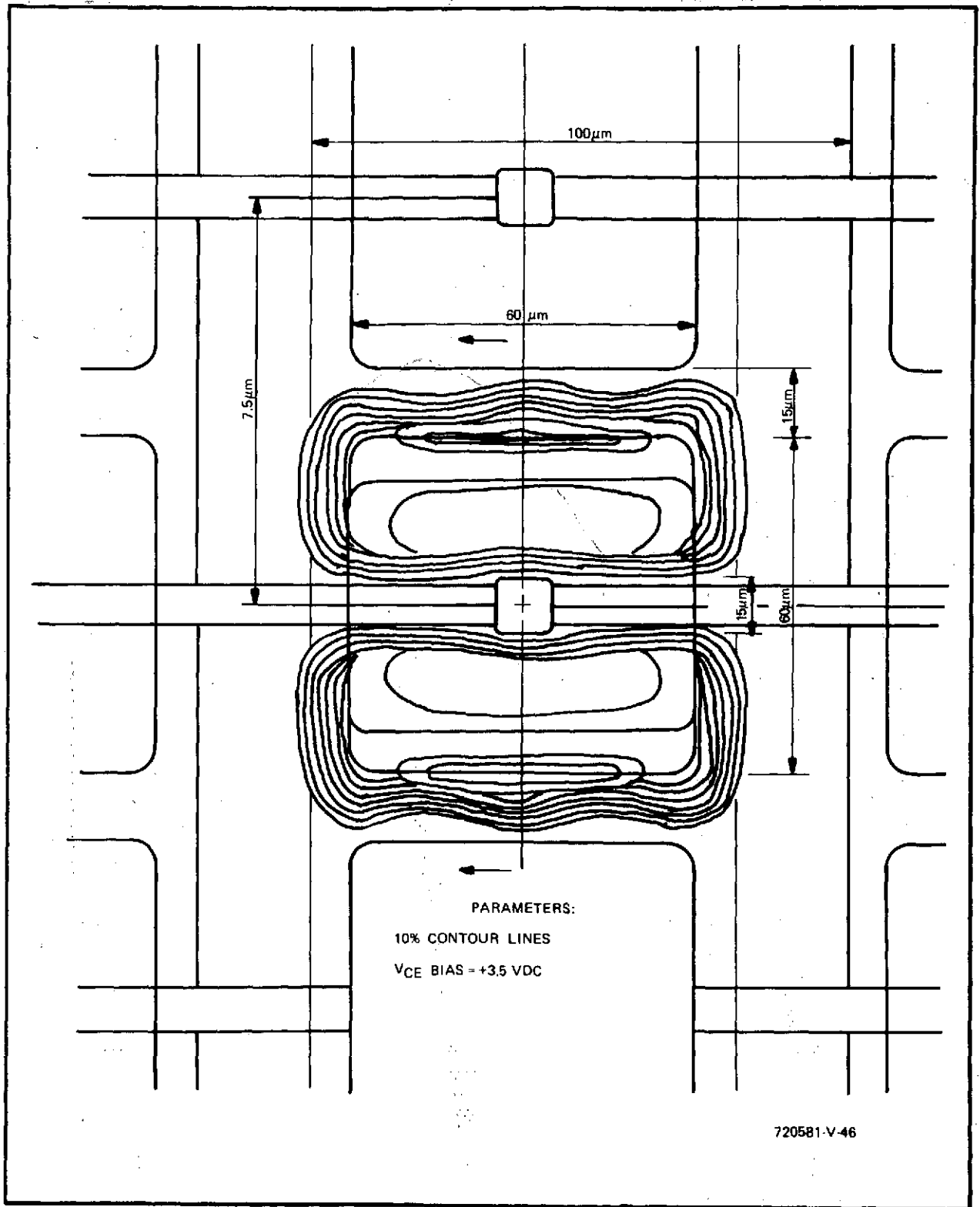
Figure 4-11. Sensitivity Contour Map for Small Geometry Sensor Mosaic

4-33
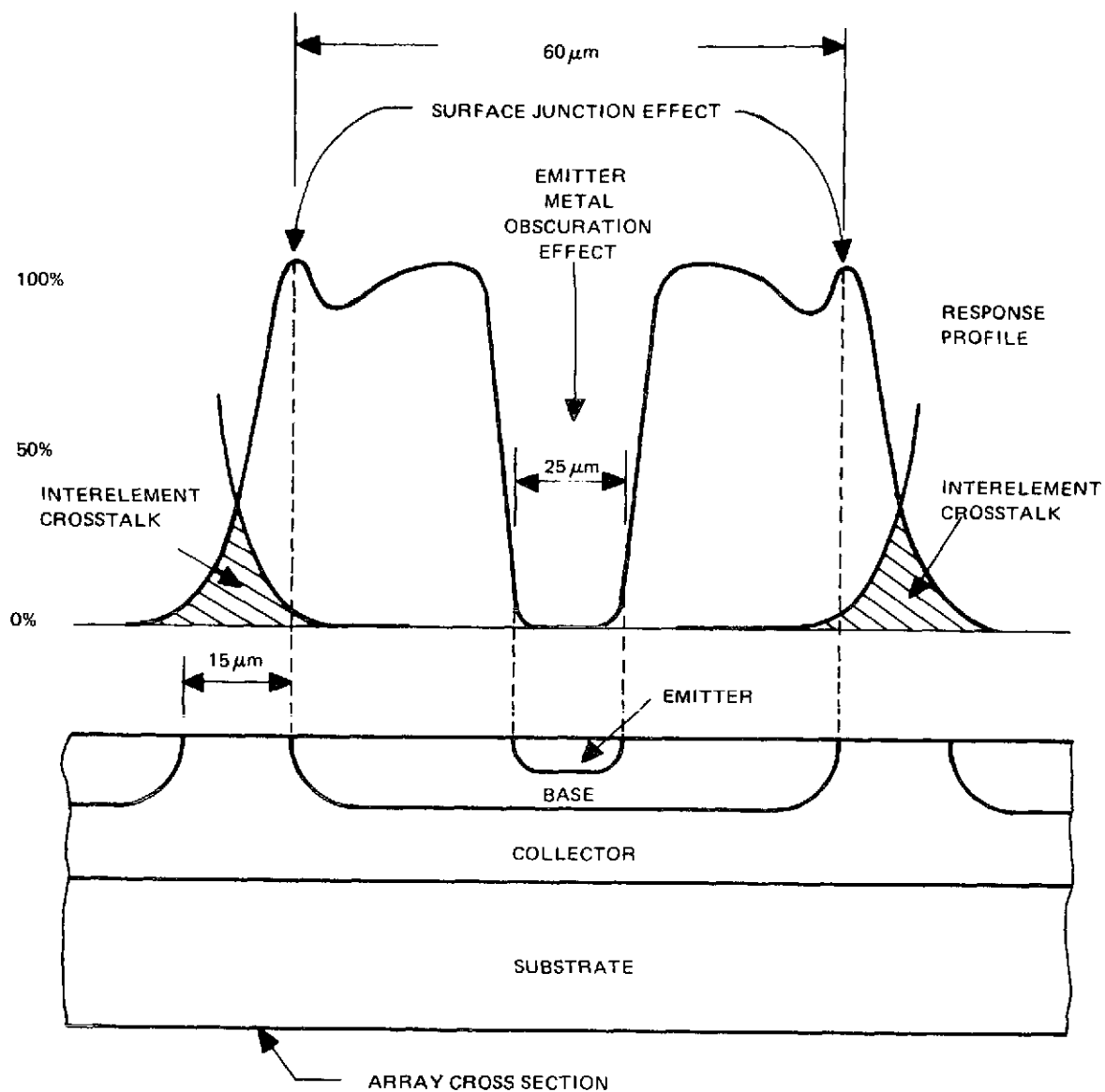
Figure 4-12. Sensitivity Profile Map for Small Geometry
Sensor Mosaic
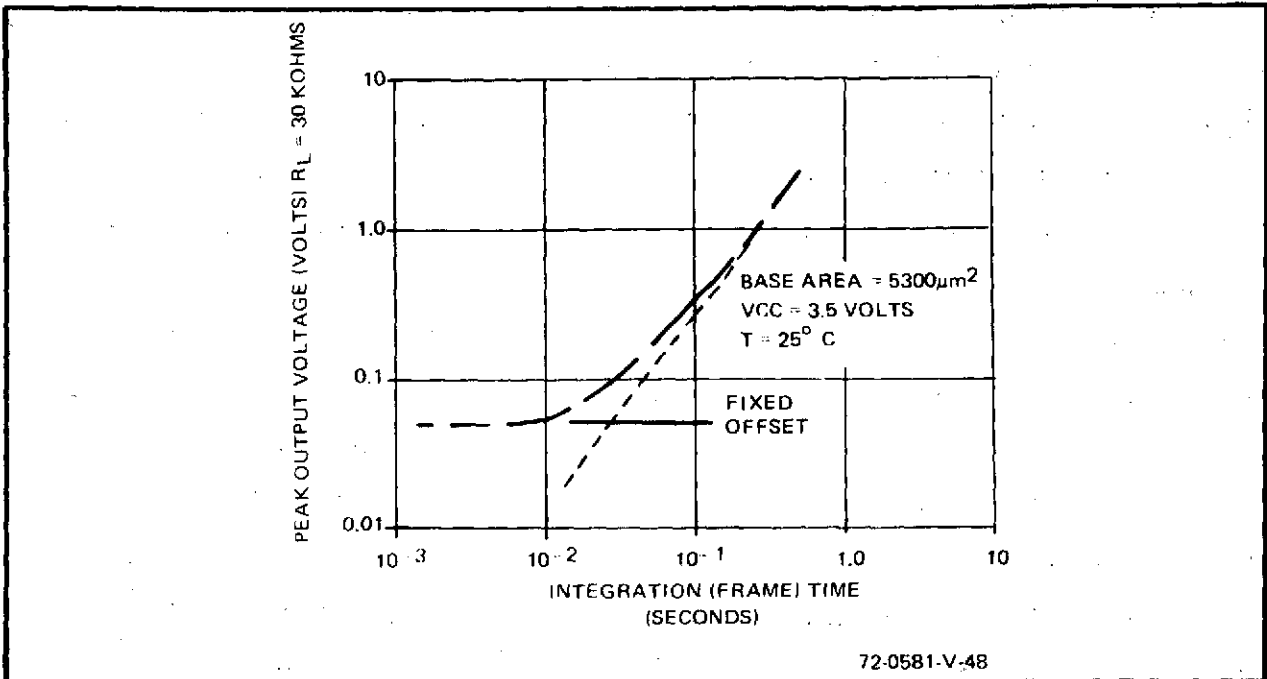
Figure 4-13. Pulsed Mode Phototransistor Dark Response

characteristic of figure 4-9, reveals that the thermally-induced dark current

component of I_{CBO} also integrates during the frame time, producing an un-

wanted output and reducing the useful dynamic range. This curve plots the

integration mode's peak output voltage against frame time for the unillumi-

nated sensor of figure 4-9. Neglecting difficulties in extrapolating

the true slope, the dependence is seen to approach that of a linear integrator.

The limitation on dynamic range here is manifest as a fixed error output

signal which is independent of integration time. This term is due both to

external charge flow required to reverse-bias the emitter-base depletion

capacitance C_{BE}, as demanded by the external conditions on entering the

integration configuration, and to return of this charge when sampling bias

is applied. Therefore, its magnitude is determined by the ratio C_{CB}/C_{BE} -

the smaller the ratio, the larger the error term.

Extending our discussion to more macroscopic operational facets of phototransistors, we can discover a number of distinctive characteristics from figure 4-14. The plots here show the peak output from the previous phototransistor structure versus incident irradiation for two different frame rates at two different supply levels. These curves further dramatize the inherent upper and lower bounds that constrain the usable dynamic range of a photosensor; viz., the saturation and dark response asymptotes, respectively. The curves for a 60-Hz frame rate show an appreciable region where linear dependence on incident light is established. The 10 Hz results, contrarily, are dominated by excessive buildup of dark leakage. Outputs at 4×10^{-6} W/cm^2 do differ by a factor of 6, though, which is the ratio of the integration times.

Also in evidence in this figure is the shift in dynamic range expected of integrating detectors when the frame time is altered. This characteristic has potential for automatic electronic light control in imaging; that is, by
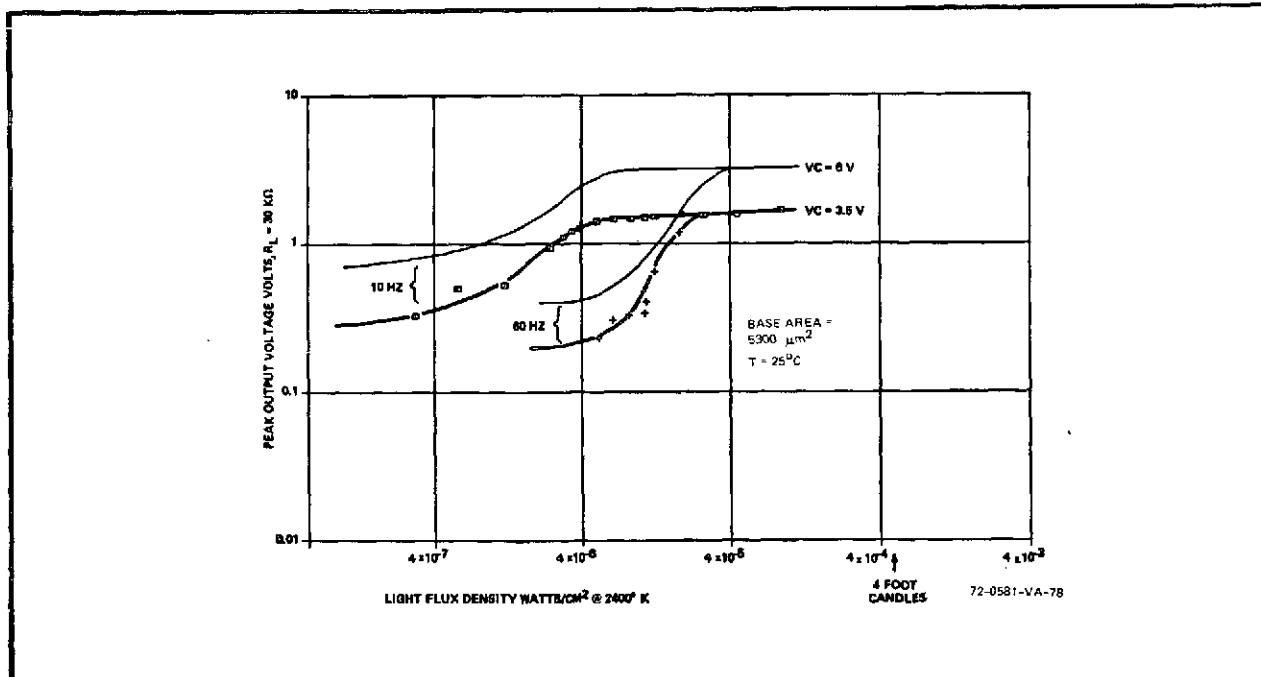

Figure 4-14. Pulsed Mode Transfer Characteristics at Two
Frame Rates for Two Collector Voltages

varying the frame rate, the useful region for gray-scale detection can be centered at different absolute light levels, with much the same result as stopping down the optical interface lens. Note finally here that, in general, the slopes of the respective curves do not change appreciably between the two supply voltages, but that both the saturation levels and the dark response offsets do show a direct dependence on V_{CC}.

Figure 4-15 further elaborates on the effect of dark I_{CBO} on a pulsed sensor's dynamic range. This figure is a plot of peak output versus integration time, at different temperatures, for a fixed light level within the device's effective dynamic range. Increased leakage with temperature is seen to change the proportionality constant between output and integration time, since the quantity being integrated over time is I_{λ} (fixed) + $I_{leakage}$ (temperature variable). For example, at 10^{-2} seconds the increase in output from -50 to +25 degrees Centigrade is about one-third to one-half the -50°C total output. Based on temperature characteristics of the leakage component, its value at -50°C should be, at most, $0.01 \times 0.6 \times I_{\lambda}$ and, therefore, negligible with respect to the photocurrent at the lowest temperature.

On this particular set of data, the limiting asymptotes are too close together to allow the true slope of the integration characteristic to be calculated; however, the linear behavior has been observed elsewhere. These slopes do not change appreciably with temperature. Calculation of an integration rate from the curve, using the light flux density given and the -50°C output value at 10^{-2} seconds, gives 300 volts per footcandle second. Theoretical prediction of this characteristic, using the I_{CEO} per footcandle value from figure 4-15, beta of 50, and C_{CB} of 0.1 pF, gives 190 volts per footcandle second.

An appreciation of the relative transfer characteristic differences affected by changing the sensor geometry can be obtained from figure 4-16. Here, the results for two alternate sized devices are compared to the above reference element. One is approximately half its size, while the other is
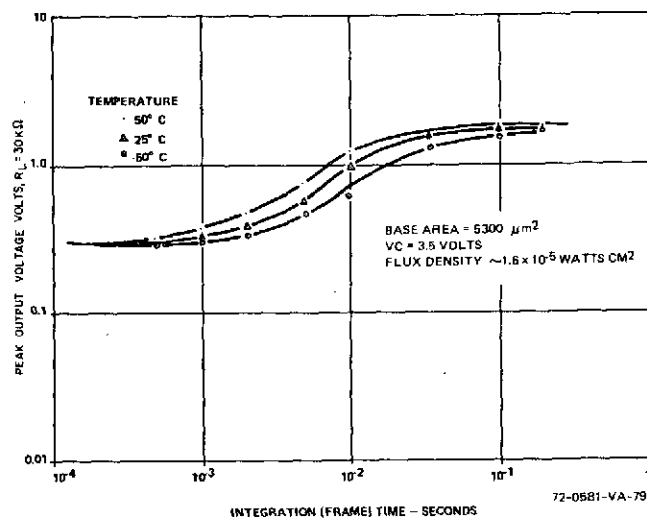
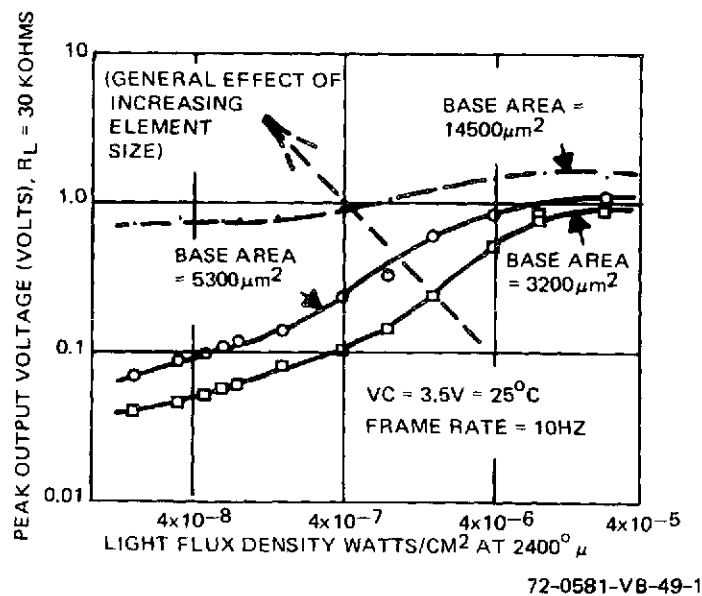Figure 4-15.   Temperature Dependence of Pulsed Integration

Figure 4-16.   Pulsed Mode Transfer Characteristics for
Different Element Designs

4-38

nearly three times as large. Direct comparison of these characteristics shows that the general effect of increasing the size of an element is to move the entire transfer curve upward to the left along a negative unity slope line (shown dotted). Since the high end saturation level is set primarily by the supply voltage whereas the low end leakage offset is directly a function of the sensor area, it is seen that a constriction of the dynamic range for the large sensor occurs under the stipulated long integration time and supply potential. While some of this range could be picked back up by increasing the frame rate (i. e. , shortening the integration time), the fixed offset level discussed from figure 4-13 will quickly come onto play to stop any further extension.

The final characteristic of a phototransistor affecting its performance in an imaging situation is its response to varying electromagnetic radiation wavelengths. A comparison of the relative spectral response of a typical monolithic silicon phototransistor with that of the human eye (which defines what is referred to as the photometric region of the electromagnetic spectrum) and a large area commercial silicon photodiode is made in figure 4-17. Quite obviously here, the response range of integrated array imagers using silicon phototransistors is seen to extend over a considerably wider spectrum than that of the human eye, but not out to the theoretical limits closely approximated by the photodiode. With a peak response in the near infra-red, silicon phototransistors are very receptive to use with or coupling to GaAs type of lasing photoemitters. Incandescent bulbs having high IR content also will function very well with these sensors. Conversely, some types of fluorescent bulbs with the preponderance of their output in the blue region will interface much less efficiently. Consideration of the illuminating source characteristics must therefore always be made to accurately predict the performance of phototransistors and the systems in which they are used.
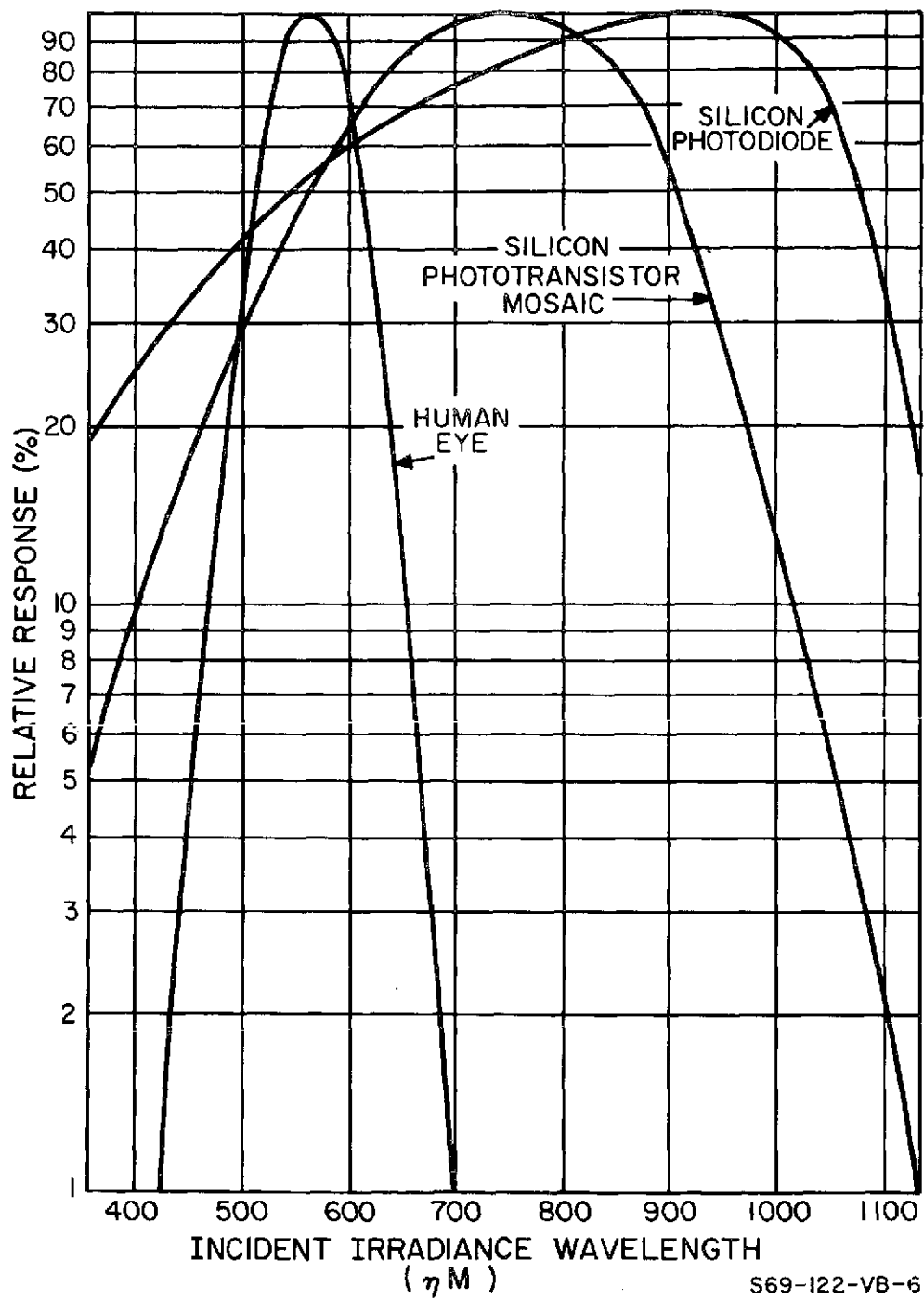
Figure 4-17. Spectral Response Comparison

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4-40

5. SYSTEM METHODOLOGY

To facilitate production of high grade state-of-the-art solid-state tele-vision cameras having stable and versatile performance characteristics, Westinghouse has developed and refined construction principles which are based on the use of row-column organized phototransistor monoliths, as discussed previously, and high level hybrid mixes of specially built peripheral circuitry boards and substrates. By separating sensor and scanning functions in this manner, it is possible to optimize the individual unit and yield performance factors and to thus avoid the expensive production costs that have been painfully demonstrated throughout the electronics industry to follow attempts to exceed the technological limits that exist on the extent of LSI (large scale integration) permissible in a given system.

This is not to say that an entire camera cannot conceivably be fabricated in a single "self-scanned" chip form. Work in this area is in fact being actively pursued. But, a rational and unbiased review of the problems associated with single-chip design objectives shows that, in light of current state-of-the-art technological capabilities, the costs are extremely high (almost to the point of being prohibitive) on both a developmental and a production scale for large sensing structures in which the number of elements (and hence the system resolution) begins to approach the industry standard of approximately 300,000 picture elements per television frame. Mechanization of solid-state mosaic readout systems in which X-Y interconnection leads are brought out on a one-to-one basis from the array, on the other hand, has posed no unresolvable difficulties for mosaics of approximately this size so long as overly stringent restrictions are not imposed on the

aggregate unit's size or power consumption. Even these stumbling blocks are surmountable today, though, by capitalizing on the rapid progress that has been made with MOS devices and the major proliferation of LSI logic functions that have become available.

In the following discussions the basis for these observations will be elucidated further, along with detailed considerations of the manner in which prior molecular image converters and their associated system accessories have been mechanized, and future cameras can be, to circumvent various technological limitation problems. The specific items which will be reviewed to establish the basis for a general system design philosophy are

- Array scanning logic types and organizations
- Sensor interfacing and signal acquisition techniques
- Video amplifier and signal processing electronics
- Information display and data utilization equipment
- Supplemental data smoothing and signal conditioning schemes.

Within these broad areas there must of course be included at least perfunctory cogitation on the characteristics of the scene to be imaged and its relationship to the intrinsic sensor parameters, the image scanning and data presentation format to be employed, the features and interactive affects of any special control functions needed, and the nature of and permissible drain from the primary power source available. Factors that will not be covered in depth are size and weight restrictions and operational requirements since they vary too widely with individual application situations to be covered effectively within the scope of this report.

5.1 ARRAY SCANNING

The foremost systemological consideration in the design of any fully solid-state image detection system is the organizational philosophy of the scanning telectronics. It sets the tone of all subsequent developments for

the system, including both electrical complexity and mechanical structuring. Consequently, all factors which influence it or are influenced by it should be evaluated fully before making any final choice of the approach to be taken in a particular situation.

A thorough understanding of the basic principals of the detecting mechanism employed is, of course, a must. While there are a number of sensor types which are potential candidates for incorporation in a molecular image converter (MIC), the presentation here will be confined to planar epitaxial double diffused phototransistor mosaics fabricated and operated in the manner discussed earlier and organized in the row-column accessed fashion illustrated in figure 5-1. Note that this is a generalized schematic containing no specific information about the access line switches or the signal developing load. These are details which vary with the type of circuitry ultimately used, and hence can change drastically as new techniques and logic families are evolved.

The underlying fundamentals of element accessing remain constant however, and are equally applicable to emitter readout (wherein the signal developing load is placed in the emitter switch to ground line) or collector readout (for which the load is located in the collector switch to V_{cc} lead). In particular, observe that activation of a specific combination of one collector and one emitter switch will enable proper biasing conditions to reach and thereby open up a charge flow path through one and only one distinct sensor element located at the cross-coincident junction point of the two array access lines that are addressed. Being digitally locateable in this manner by X-Y coordinates, unique and repeatable readout of any given element is readily provided by simply establishing a reference system and counting off the proper number of row and column access lines.
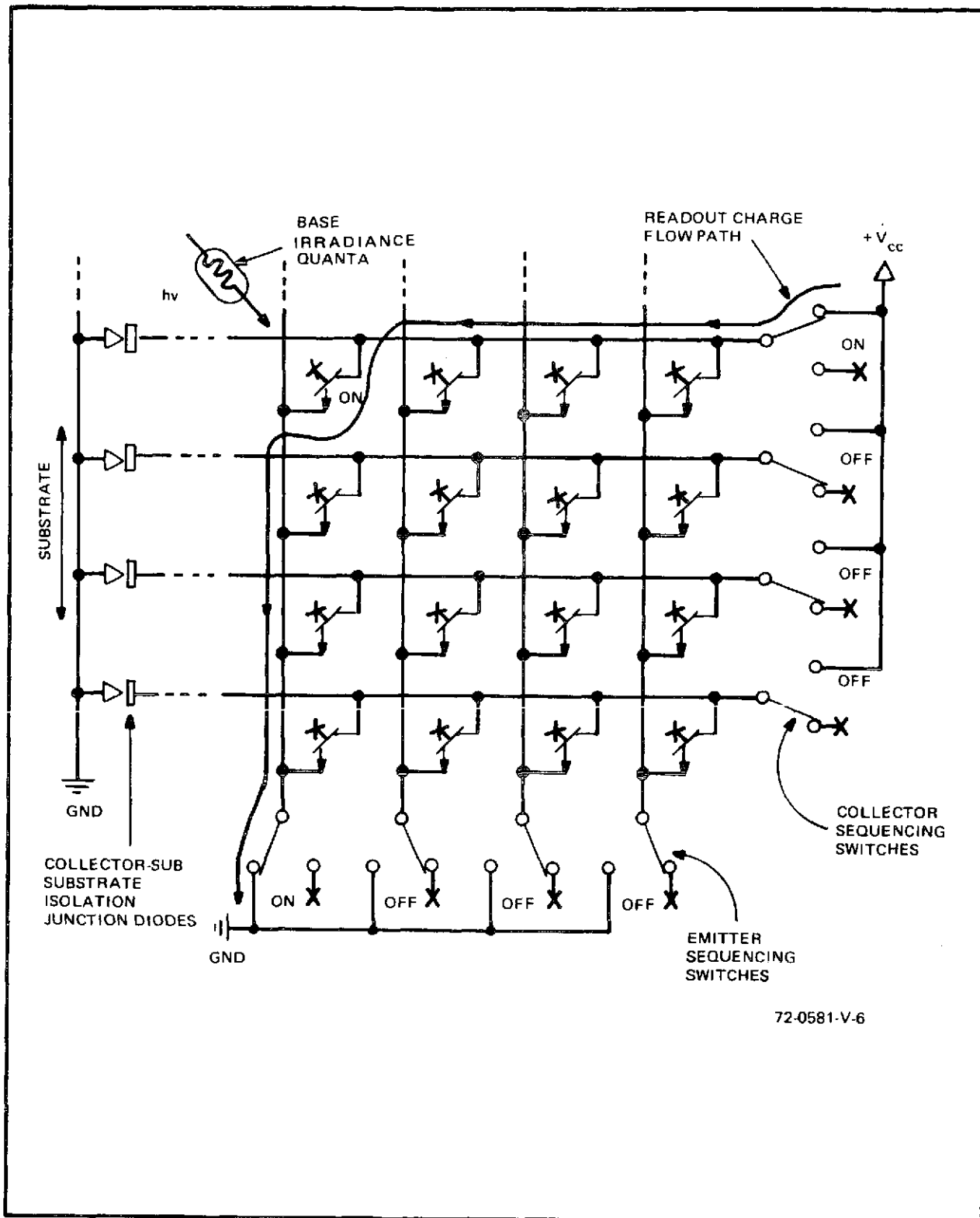
Figure 5-1. Schematic for 4-x-4 Element Section of a
Phototransistor Matrix

Sequential scanning of the entire array in the basic fashion of a TV raster will similarly be facilitated by applying high and low speed, respectively, binary counting circuitry along the X- and Y-axes. The actual counting operations can be carried out with either long chains of serial-in/parallel-out shift registers or with properly timed counter-decoder combinations having appropriate numbers of bits. One precaution frequently overlooked by the unwary, though, is that, as indicated in figure 5-2, a sequential progression of the matrix aggregation of sensor points must be referenced to a starting point at the lower left-hand corner on the front surface of the array—not the lower right-hand corner! The reason for this can readily be understood from a check of figure 5-3. This figure illustrates the right-for-left and top-for-bottom flipping (or total inversion) of an image which occurs when a simple lens is employed as the optical interface between the object and image planes.

If scanning of the object plane data is to take place from top-to-bottom and left-to-right across its front surface beginning in the upper left-hand reference corner (as per standard TV practices), then scanning at the image plane must progress from the diametrically opposed corner; specifically, the lower right-hand corner if viewed from the rear—as is the case for conventional high vacuum image tubes, such as vidicons, which are electron beam scanned—or the lower left-hand corner if viewed from the front— which is the case with molecular image monoliths, such as phototransistor mosaics, which are scanned electronically. Confusion on this point, despite its amost ridiculous simplicity once recognized, has led to a certain degree of consternation when printed text material appeared virtually unintelligibly on a system display monitor due to a mirror effect.

Returning now to figure 5-2 with the basis for the indicated scanning directions established, the next point to consider is the timing relationship between the horizontal scanning (or column interrogation) pulses and the
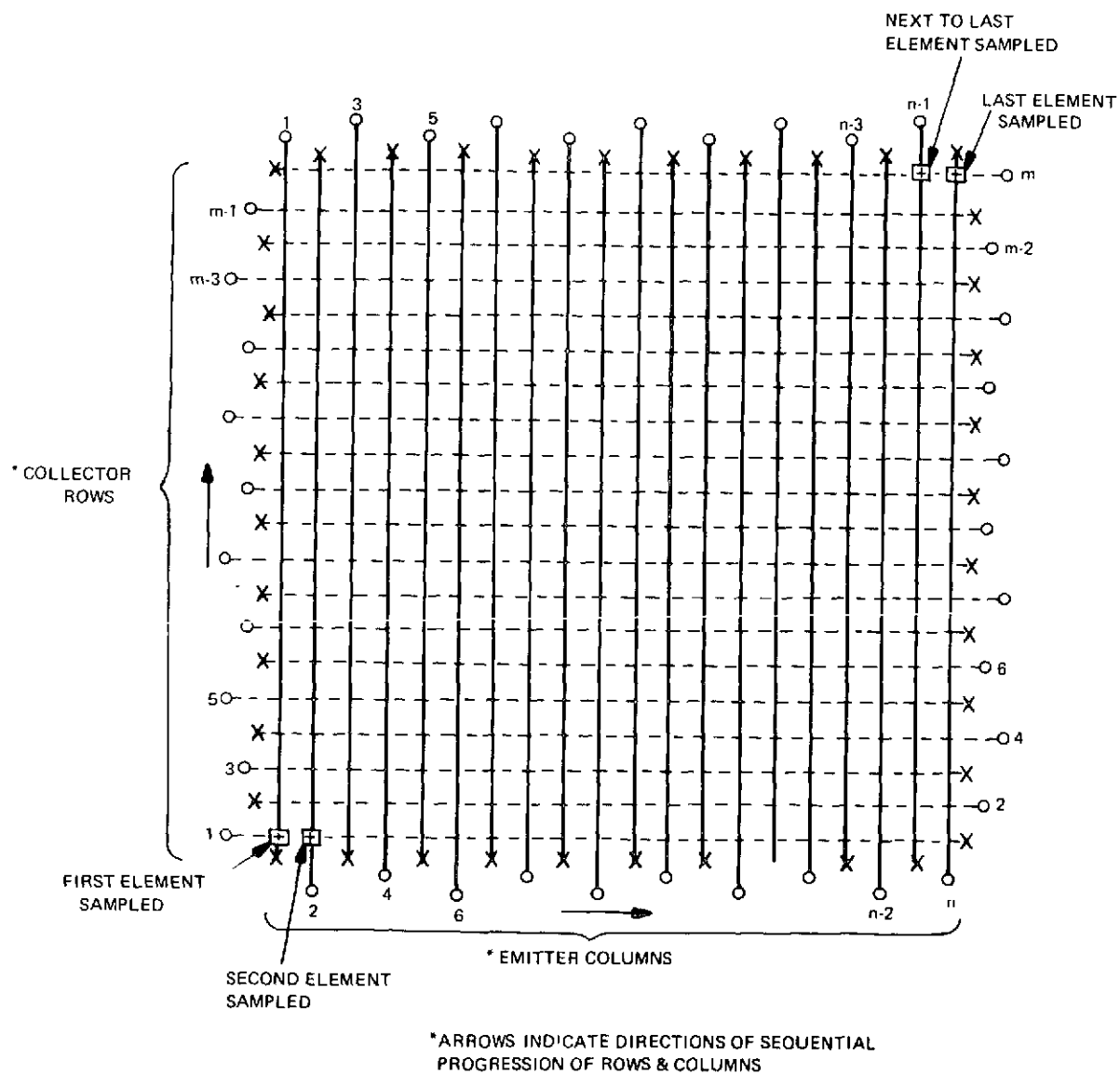
Figure 5-2. Basic Elemental Interrogation Format for X-Y
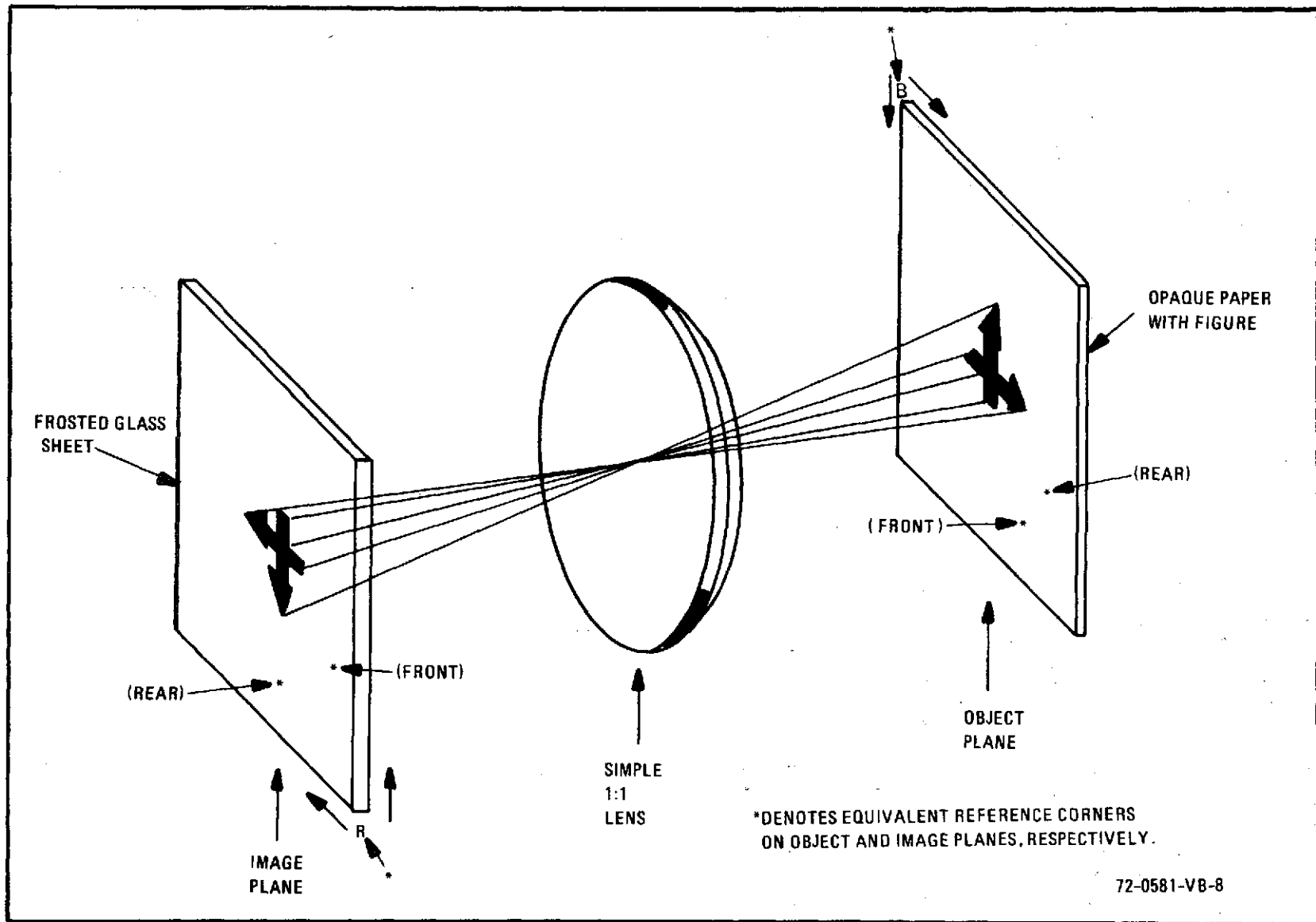Accessed Sensor Mosaics

5-6

Figure 5-3. Optical Interface Image Inversion Through Simple Lens

vertical scanning (or row address) pulses. Since it is necessary to completely scan out all points along any given horizontal row before advancing vertically to the next row, it is apparent that the column sequencing rate (for an M-by-N element array) must be slightly greater than N-times the row advance rate—to allow for an interline blank or retrace interval. The verity of this statement is illustrated more graphically in figure 5-4. Also indicated here is the normal situation engendered for row sequencing. Specifically, the count ordering of successive rows is arranged such that only every other row is addressed during each standard television style field. With two fields interlaced 2:1 per TV frame, it follows that odd numbered lines (i.e., rows 1, 3, 5, ... etc) will receive drive pulses during the first field while even numbered lines (i.e., rows 2, 4, 6... etc) will be driven during the second field. On the array layout diagram of figure 5-2 this amounts to progressing up the pads along one side of the array during one field, then up the other side during the alternate field.

ROW (m-k) SELECT PULSE

ROW (m-(k-2)) SELECT PULSE

COLUMN (1) SELECT PULSE

COLUMN (n) SELECT PULSE

INTERLINE BLANK PERIODS
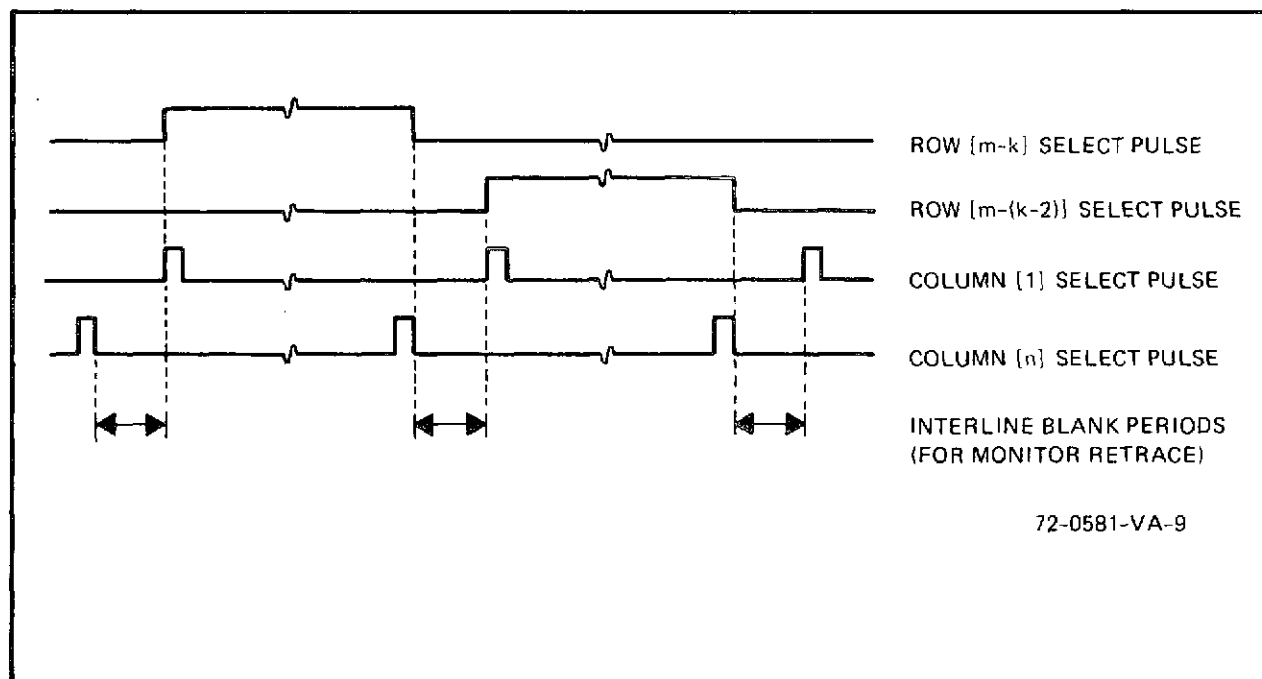(FOR MONITOR RETRACE)

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Figure 5-4. Basic Electronic Scanning Digital Timing
Relationships for an M-by-N Element Array with Row Interlacing

From the previous fabrication section it will be recalled that considerations of array symmetry and pad size normally dictates that successive row and column contact pads be brought out opposing sides of large monoliths in a staggered arrangement much like that depicted. As enumerated above, this fact can be used to advantage in row counter sections by enabling the sequencing logic that drives a particular side only during its consociate field time. For column counting an identical state of affairs does not exist though since bit-by-bit sampling along each scan line is conducted in an un-interrupted, sequentially contiguous fashion rather than being interlaced. The interrogation pulse generation circuitry must allow for this by supplying successive addresses to first one side and then the other, then back again and repeat. If a simple shift register chain like that in figure 5-5a is used to originate this time contiguous stream of pulses, cross-over lines around or behind the array will always result regardless of the side of the array on which the register is placed. Since the symmetry line for a single register arrangement is right down the center of the sensor wafer, the only way of avoiding cross-overs and providing equal length leads to both sides would be to position the register behind and in the exact middle of the array.

Usually, though, placement of any of the counting electronics centrally behind the detector mosaic poses somewhat of a problem due to conflicts with other circuitry requirements. To get around these difficulties, a redundant arrangement of two identical registers - one on each side of the array - can be employed. This scheme, shown in figure 5-5b, facilitates excellent symmetry, but requires twice as many register stages per side as there are lines per side. Inclusion of extra delay stages in each register chain is necessary to avoid having two address pulses occur simultaneously, or even be partially overlapped as would be the case if phased rather than common clocking was employed.

5-9

In those situations where the outputs from successive sensor elements are handled in serial form along a single channel, time contiguous nonoverlapping line interrogation pulses like those shown in figure 5-6a can be used. If, however, outputs are to be taken in parallel along two or more channels, it is permissible, and in fact may prove advantageous, to institute overlapped time-sharing interrogation pulses similar to those illustrated in figure 5-6b. To generate this type of timing waveform a dual register design, analogous in many respects to that already covered but refined as shown in figure 5-5c, may be employed. Time-sharing in this manner allows the register lengths to be reduced and their clocking rates to be lowered by a factor equal to the number of parallel channels. In the example presented, a factor of two has been used. Alternate phases of the divided down (halved) clock frequency are shown fed to the two opposing registers so that their respective bits will be advanced 90 degrees out of phase.

While registers of the general type covered here have the advantage of extreme simplicity - at least in basic concept - their extreme susceptibility to latch-up and loss of shift synchronization becomes increasingly critical as the number of stages is expanded. Consequently, practical implementations of shift register timing circuitry will nearly always be found to include specially added features intended to circumvent or negate the effects of anomalies occurring in long register chains. Such provisions normally appear as some form of recycling control redundancy whereby the sequencing address register chain is broken up into subgroups whose operation is independently administered by a self-governing, multitiered functional breakout arrangement of master feedback loop controlled register sections similar to that in figure 5-7. Through this expediency the burden of count synchronization and continuity maintenance is transferred away from the working address register stages which frequently encounter extreme load variations as well
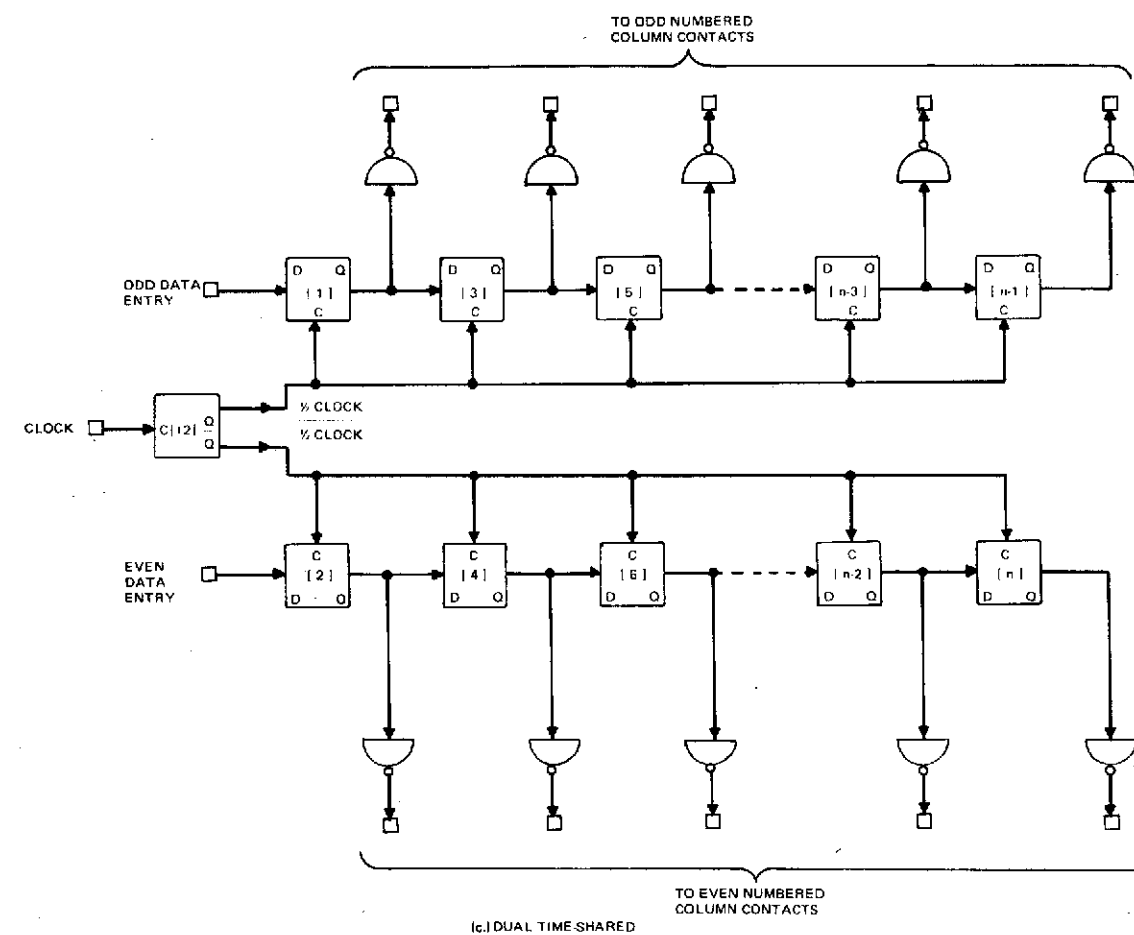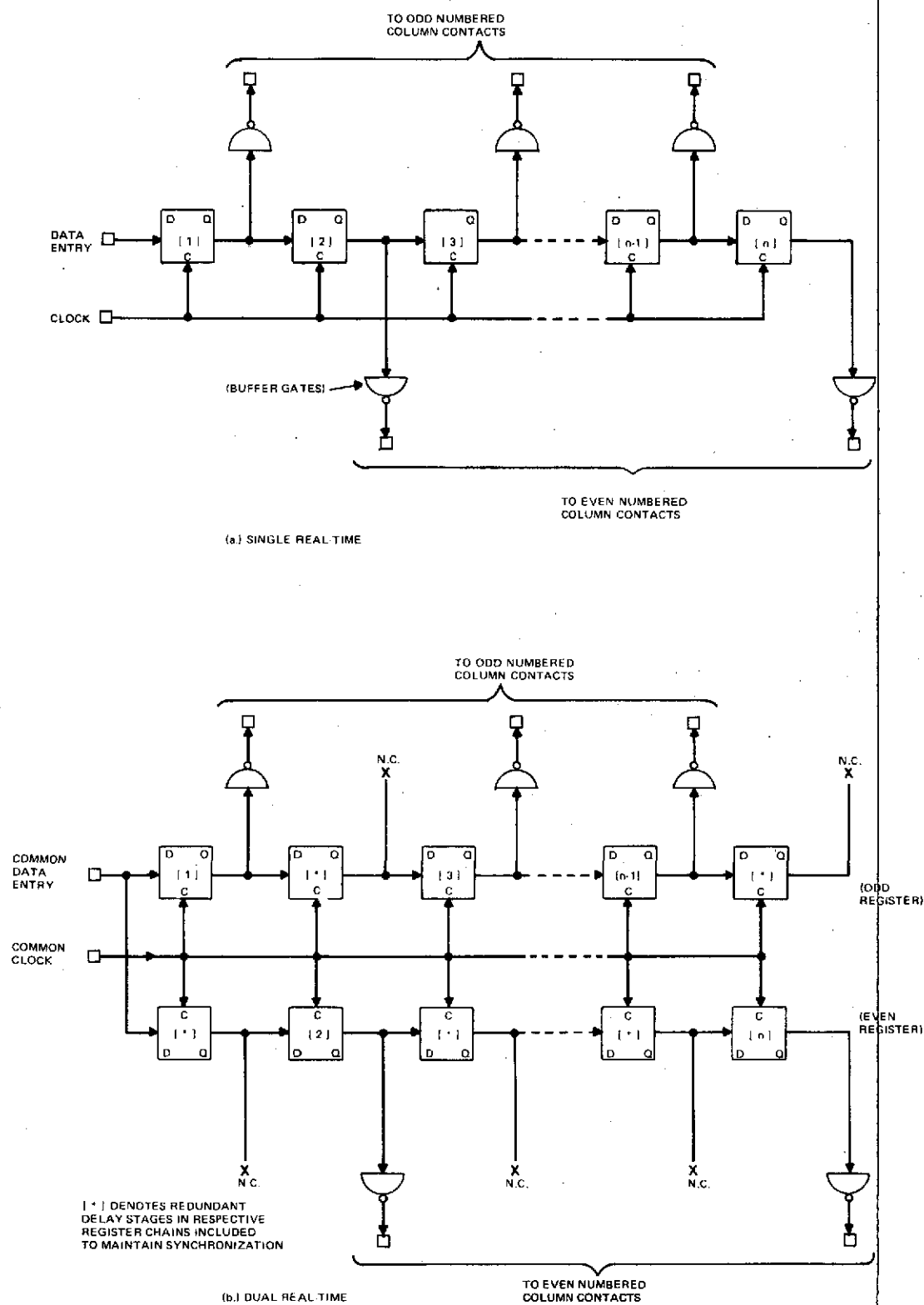
Figure 5-5. Shift Register Column Sequencer Chains

5-11

(A) REAL-TIME

(B) TIME-SHARED
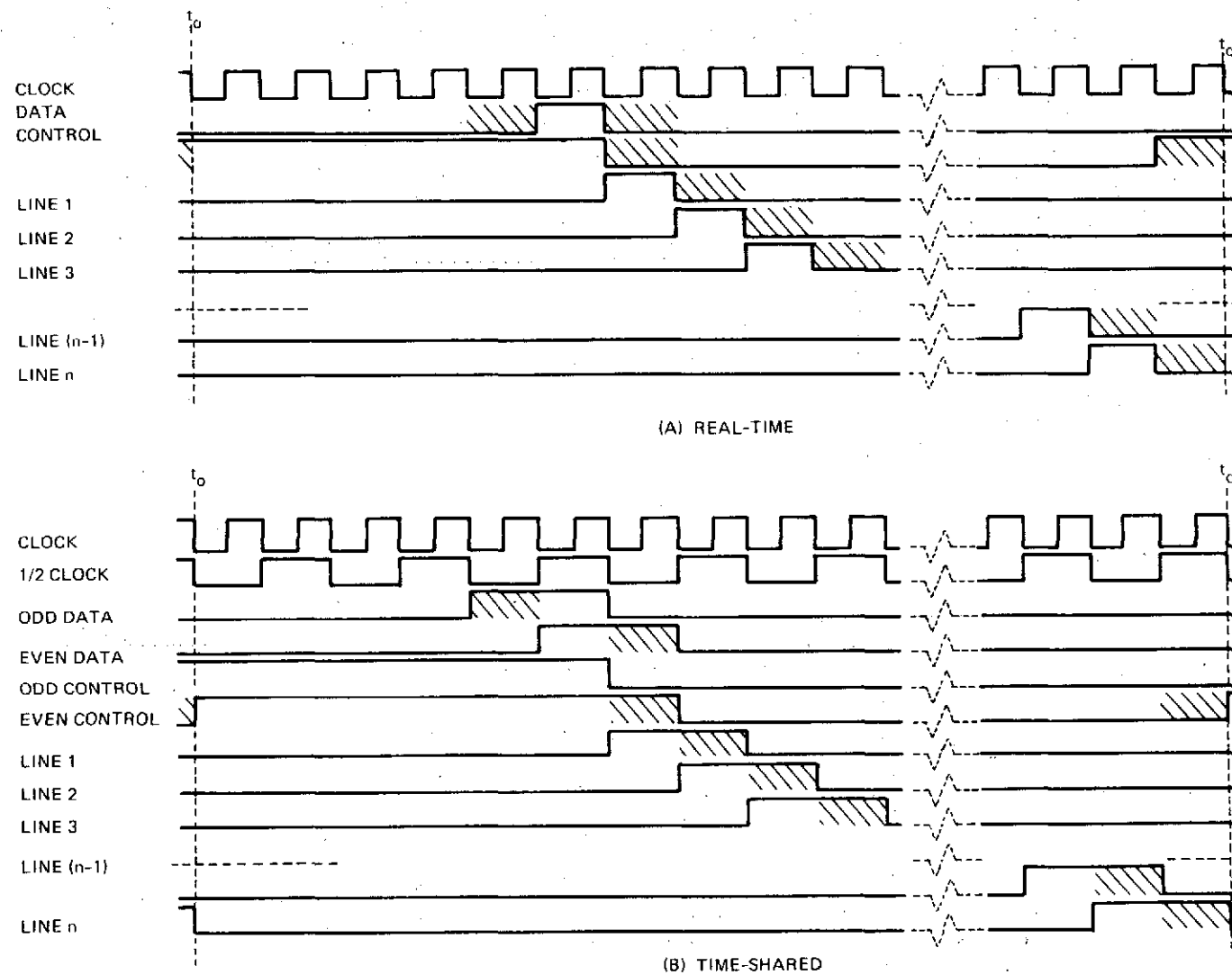
72-0581-VA-11
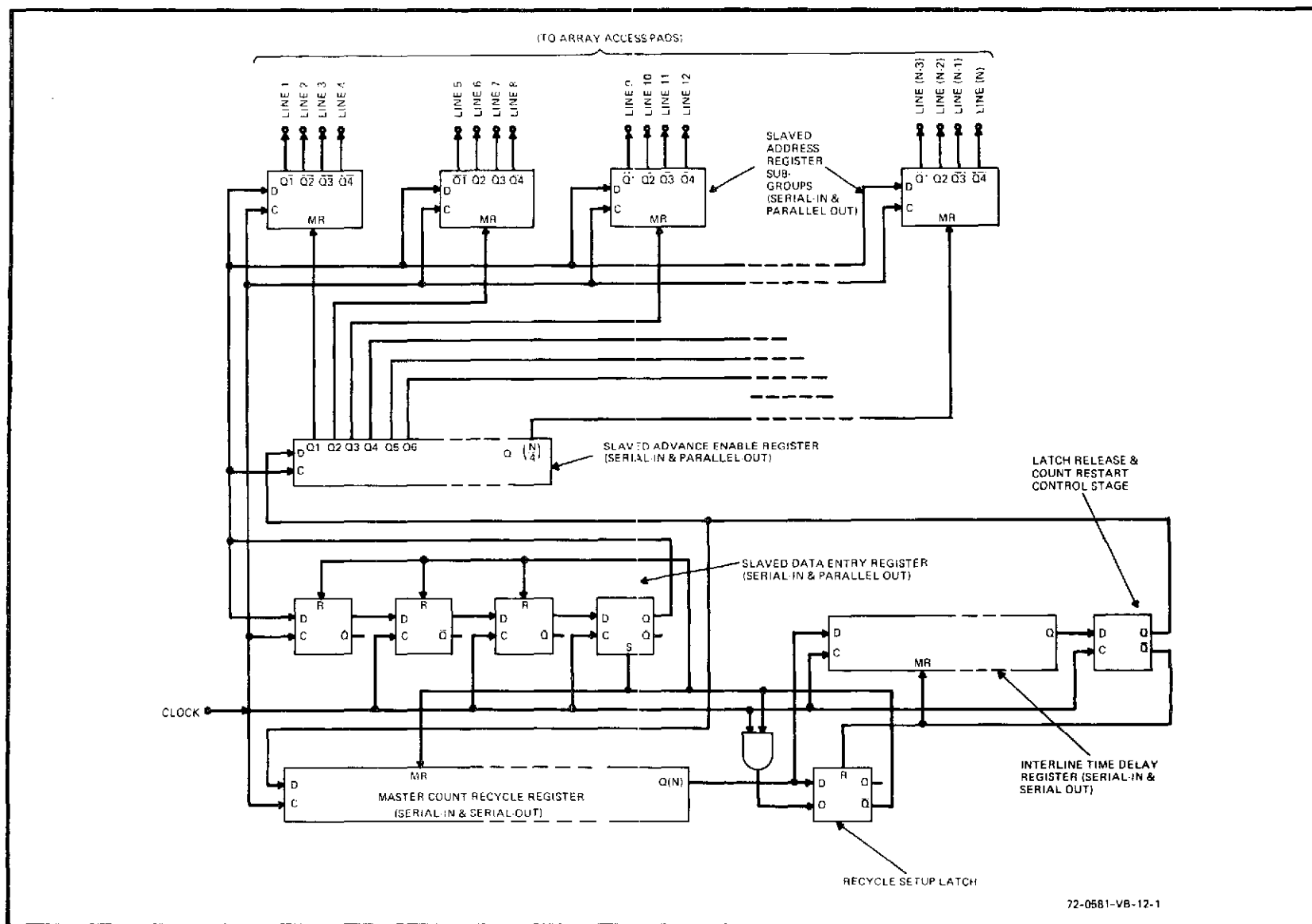
Figure 5-6. Column Sequencer Timing Diagram

Figure 5-7. Serial Shift Register Sequencer with Built-in Control Redundancy

as other disruptive transitory conditions. Quite apparently, however, much of the originally espoused advantage in design simplicity is lost by this maneuver. There are, nonetheless, several successful systems in existence which incorporate equivalent designs. The one illustrated in figure 5-8 is typical of the techniques employed when the system deploys a two-dimensional area coverage matrix. More frequently, register chains are restricted to use with one-dimensional line arrays.

The logical alternative to shift register sequencers is, of course, appropriately configured counter/decoder combinations. While the initial design work involved in establishing adequate and correctly timed interrogation pulse sequencers based on the counter/decoder concept may appear (and indeed usually proves to be) more intricate and involved than that required for a comparable arrangement of shift registers, the end result, as seen from the generalized counter/decoder system design in figure 5-9, under equivalent conditions will be little if any more complex. Comparison of the block diagrams in figures 5-8 and 5-9 reveals a comparable splitting of functions in each in the immediate vicinity of the array, and points out the originizational differences that exist in the timing control sections. The designs are not completely equivalent in that the C/D (counter/decoder) scanning format exactly follows the EIA standard for commercial U.S. television, and is therefore compatible with any average home receiver type monitor; whereas the SR (shift register) scanning format has merely been made to resemble the EIA convention by allowing for nominal interline and interframe retrace or blanking intervals. Output pulses delineating these periods are shown labeled as horizontal and vertical syncs, respectively, and must be used with more adaptive (and more expensive) general purpose display monitors.

Just as with a shift register style sequencer, there are a great many different ways of implementing the electronics for a counter/decoder based timer. The variety is in fact wider for the latter since the count order
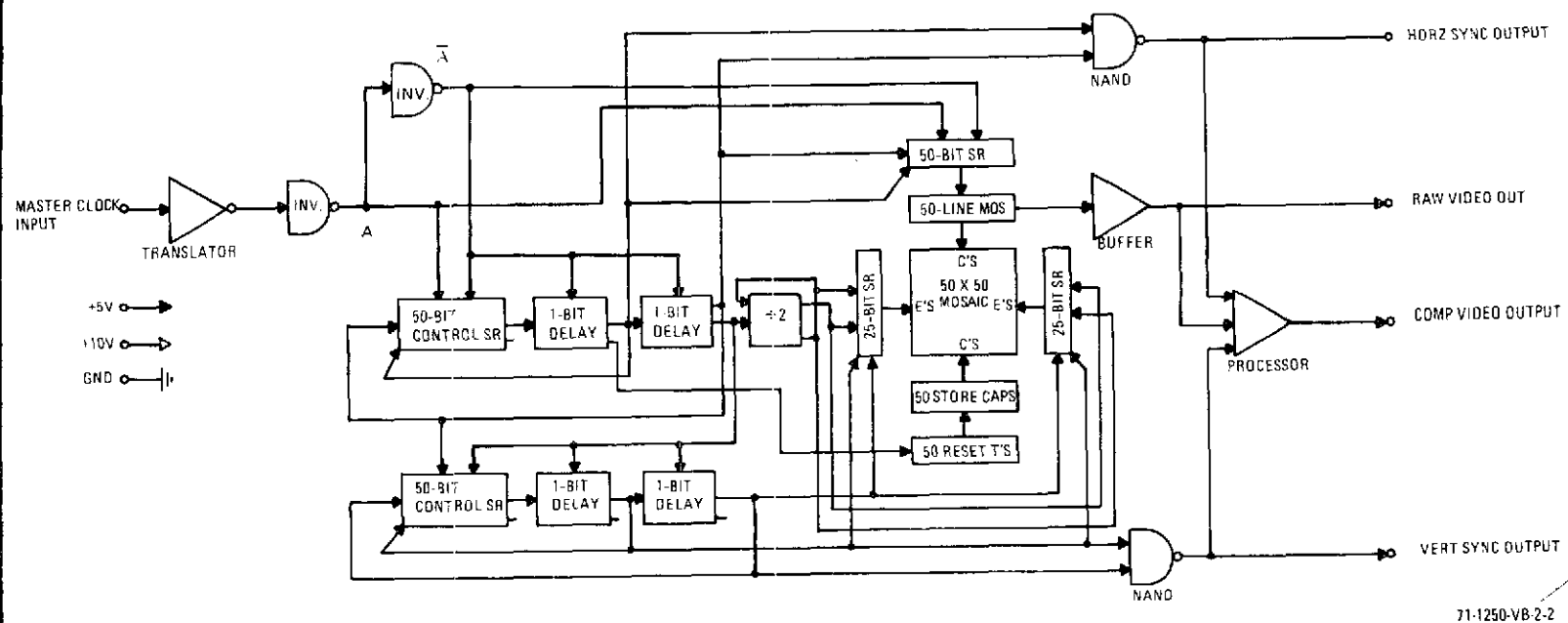
5-15

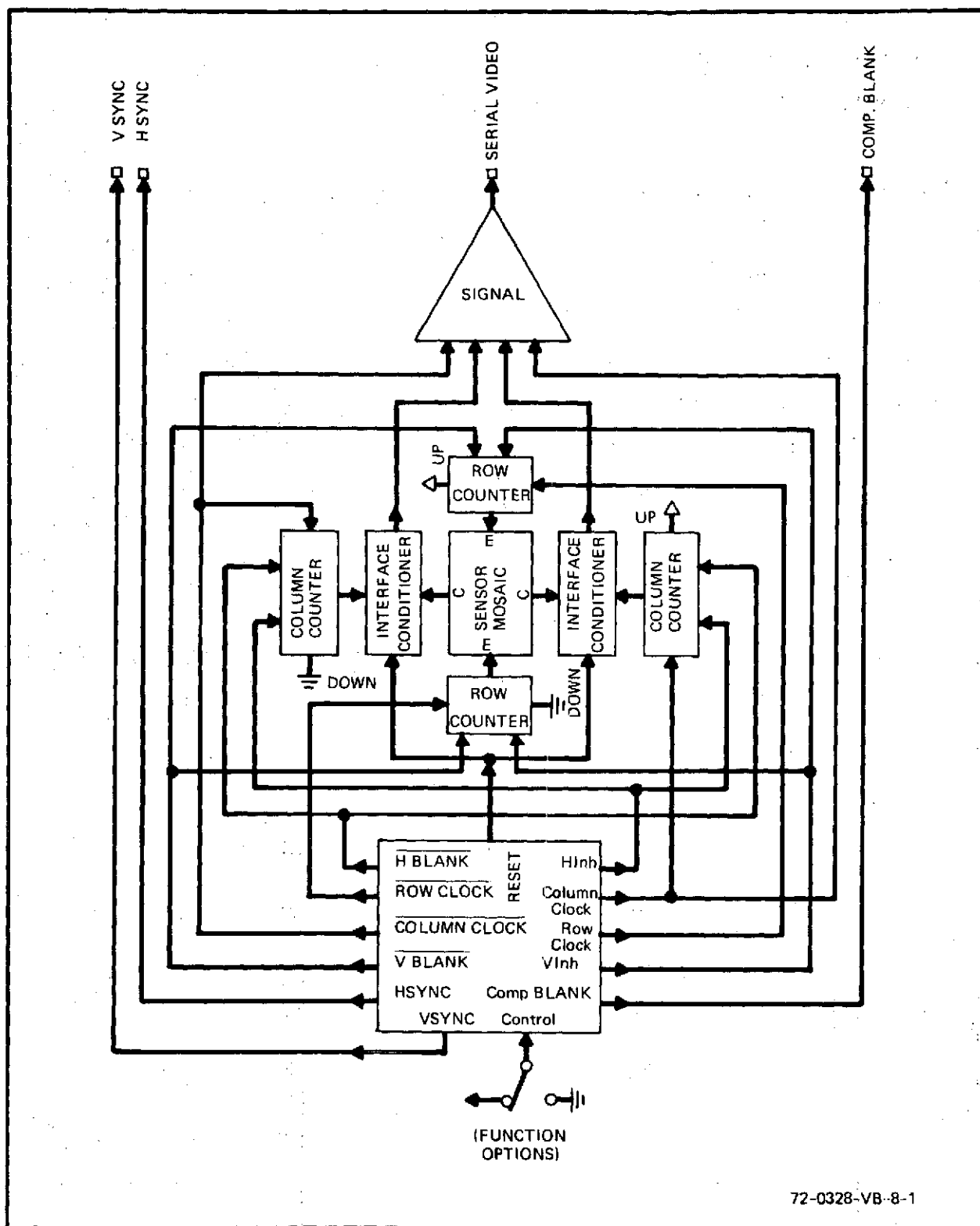Figure 5-8. Shift Register Scanned 50-x-50 Element MIC System Design with Control Redundancy

Figure 5-9. Generalized Split-Function Counter/Decoder Timed MIC System Design

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5-17

has a binomially expanded spectrum of ways it can be arranged, and the counter binaries (flip-flops) can be set up for synchronous as well as asynchronous clocking. Consider for example the design of a modulo 20 counter (i.e., a counter that cycles through 20 binary states). If it is decided to employ asynchronous clocking, whereby each successive flip-flop in the counter chain is clocked by the output of the preceding one so that the sequence of state changes appears to ripple down the chain (hence the frequently encountred name of "ripple counter"), then all that is necessary to establish a satisfactory design is to determine the number of binary stages required and at what state (combination of outputs) the aggregate counter will be forcibly recycled. In the present case it will be assumed that the count is to progress through binary number states "0" to "19" normally and be reinitialized by detecting the occurrence of state "20."

To ascertain the number of binary stages a counter must have, it is necessary to be cognizant of the fact that each stage added to the chain will double the maximum number of counts permissible; and, further, that this maximum number must be no less than the number desired. Accordingly, from the relationship

$$2^N \geq 20$$

where N is an integer denoting the number of stages, it is found that a 20 state counter must contain five flip-flops. Upon connecting these five stages in chain-like fashion with the output of the first feeding the clock input of the second, the second output feeding the third clock, and so on, a basic ripple counter capable of 20 or more different binary combinations of its outputs will be instituted. Since this raw counter can pass through 32 rather than 20 different stages, though, a further refinement to the design is needed. In particular, some form of gating logic must be added to tell the counter when to end its count and begin again. If the string of flip-flops comprising the counter are designated as A, B, C, D, and E

proceeding from first to last, a check of the states of the various outputs at the time of count "20" will show that this particular number can be uniquely segregated from the desired counts of "0" through "19" by detecting the simultaneous presence of the C and E outputs. A coincidence recognition pulse generated from the detected condition can then be folded back and used to restart the count.

Upon bringing all of the foregoing facets together, the extremely simple final circuit design presented in figure 5-10 is obtained. As with basic shift-register schemes discussed earlier, it has the attractiveness of utter simplicity in both concept and fact. But its very lack of finesse frequently proves to be its downfall. This comes about by way of the unavoidable delays introduced by ripple - through clocking and asynchronous recycling; which result in false decodes in any follow-up decoding logic, plus serving to restrict the maximum counting rates that can be managed. Despite such shortcomings, ripple counter based systems have at times been deployed with reasonable success. As a case in point, figure 5-11 displays the block diagram specifications of a uniquely structured image converter design which relies heavily on asynchronous operation of its counter stages, particularly with regard to their ability to tolerate forced entry into a pre-determined state. This system has been embellished with banks of special, function control switches to facilitate selection of total array scanning or any fractional part or sector thereof down to a single line or even a single element at the discretion of the human operator. The inclusion of such pro-visions is not standard practice in the design of solid-state array cameras but, as demonstrated here, it can be accomplished in a straight forward manner with C/D sequencers anytime the need arises. With S/R sequencers, on the other hand, the task would be truely monumental.

For systems larger than that in figure 5-11, continued use of the ripple counter design philosophy is not advised since the sequencing speeds in-crease rapidly with the size of the array and delay or timing skew (offset)
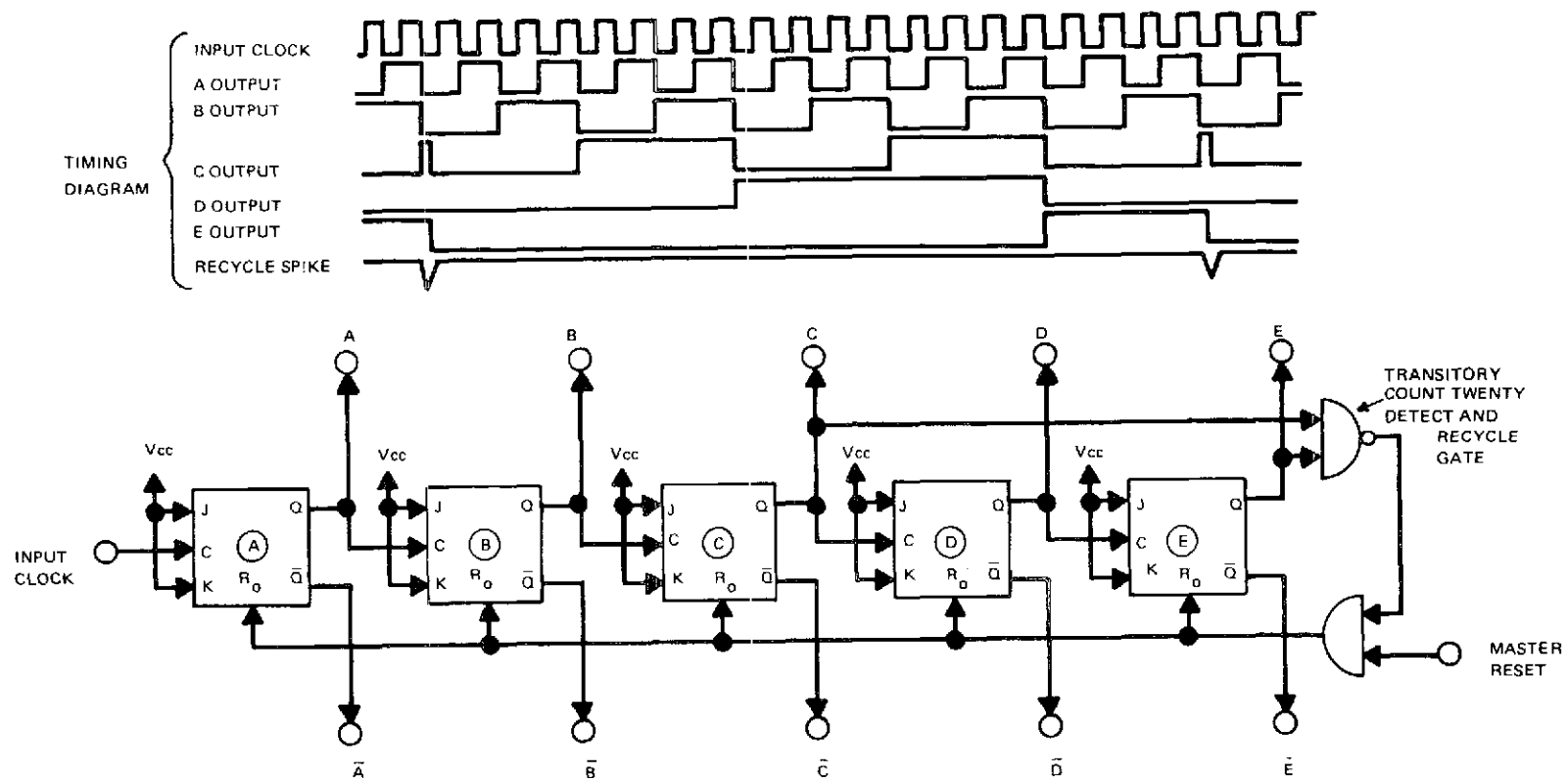
Figure 5-10. Asynchronous Modulo 20 Ripple Counter Design
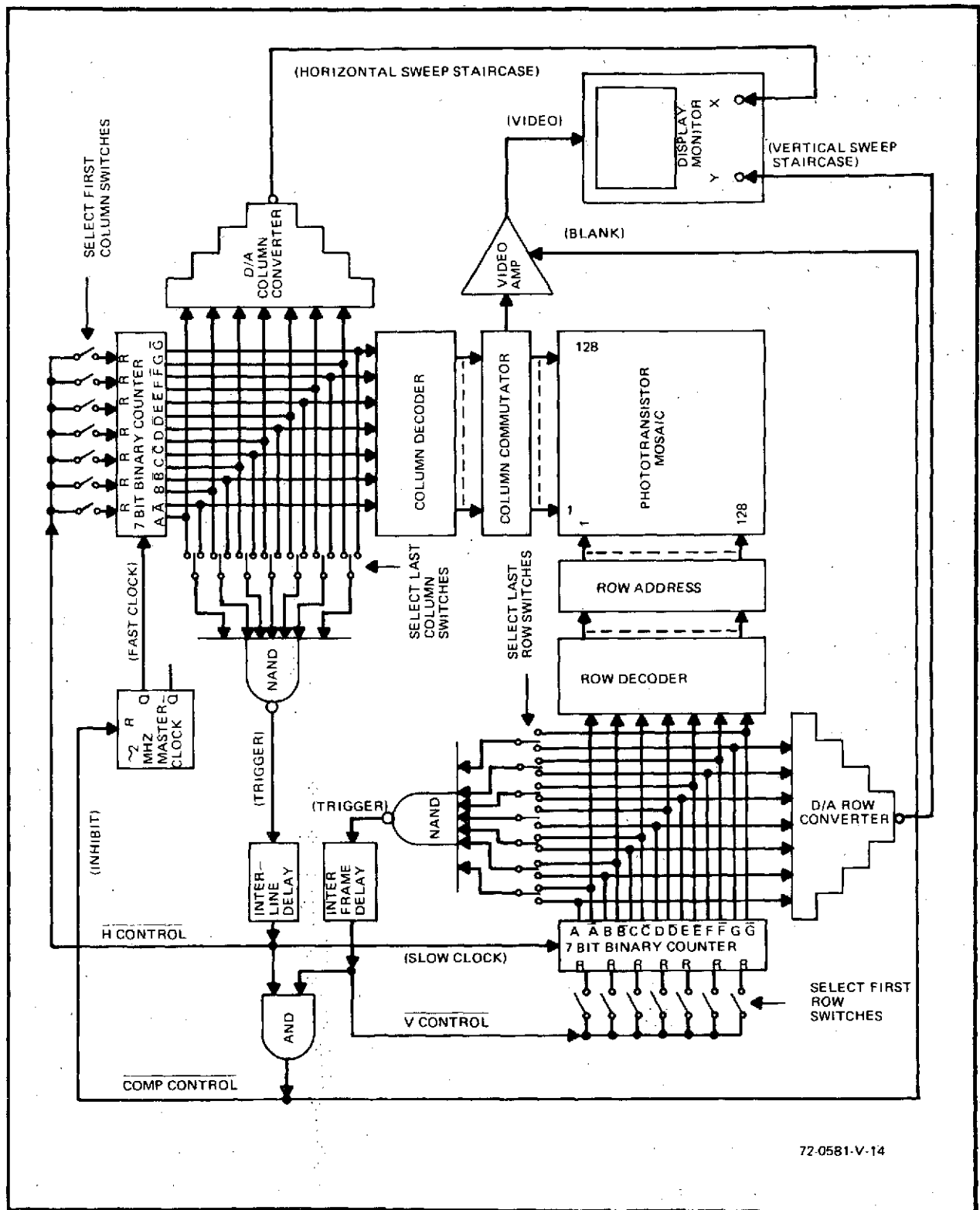
Figure 5-11. Counter/Decoder Timed 128-x-128 Element MIC System
Design Featuring Sector Scan Selection

5-21

between successive interrogation pulse edges becomes highly critical.
To circumvent these deficiencies in asynchronous counter capabilities it is obligatory that a changeover be made to fully synchronous concepts. Here though, considerably more care and sophistication must be exercised in deriving a proper network design. It will, therefore, prove highly advantageous to employ more advanced design techniques including Karnaugh maps, map entry tables, and state diagrams. In the following paragraphs these design tools will be used without expounding on their theoretical validity. They are true and they do work. Anyone not already familiar with the various procedures can find full developments of the fundamental concepts in any one of a number of excellent texts on logic design.

Considering once again the protracted situation where the design for a modulo 20 counter is desired, the added constraint will be imposed that the MR (maximum recovery) factor - which denotes the total number of delay elements, either gates or flip-flops, through which a state change command must pass before reaching any given output - must be minimized so far as possible at all points in the counter network to speed up its operation and eliminate skewing among its outputs. This automatically demands that a synchronous counter arrangement be employed, and that no tiered gating be employed in establishing proper flip-flop inputting conditions.

The first step in working out the design for a synchronous counter is to specify what its count sequence should be. In real-life situations this will frequently be controlled by other system parameters; but if not, it will have to be selected on some basis, quite possibly arbitrarily. Experience has shown that if this latter situation does exist and there is indeed complete freedom of choice with regard to ordering of the count progression, a little time spent in trial-and-error experimentation can lead to significant simplifications in circuit complexity, and hence in package count of devices needed to implement the resultant design. For the present case it will be assumed that the count is to progress in order from "0" through "19" in the same

manner as previously. With the count sequence thus chosen, the state change schedule for the counter can be prepared in the manner indicated in table 5-1. In this schedule the map entires needed for Karnaugh mapping of the respective flip-flop input conditions are obtained by comparing the time $(n + 1)$ state of any given stage to its time (n) state under each of the binary number setup conditions and noting whether or not the stage toggles. If the output of the binary has remained unaltered, then either a "1" or a "0", depending on which applies, is placed in the appropriate block. Conversely, if the output is different, then the corresponding change of state will be denoted by either a "$\mathbb{1}$" (meaning "change-to-a-one," or simply "change-one") or a "ϕ" (meaning "change-to-a-zero," abbreviated "change-zero").

Once the complete listing of map entry data is generated, the entries can be transferred verbatum over to their corresponding Karnaugh maps with "don't care" states designated by "X." The result of this operation appears in figure 5-12. From these maps the necessary, although possibly not sufficient as will be shown, input equations for the respective flip-flops can be derived from a knowledge of the map entry table characteristics of the type binary being deployed. Since the predominant type encountered in practice is the J-K variety, it has been adopted here.

Upon picking out maximally inclusive groupings of states within the Karnaugh maps which encompass all change-one or change-zero points according to the requirements of the reference J-K flip-flop map entry table included in figure 5-12, the collection of boolean logic expressions which is obtained appears as follows:
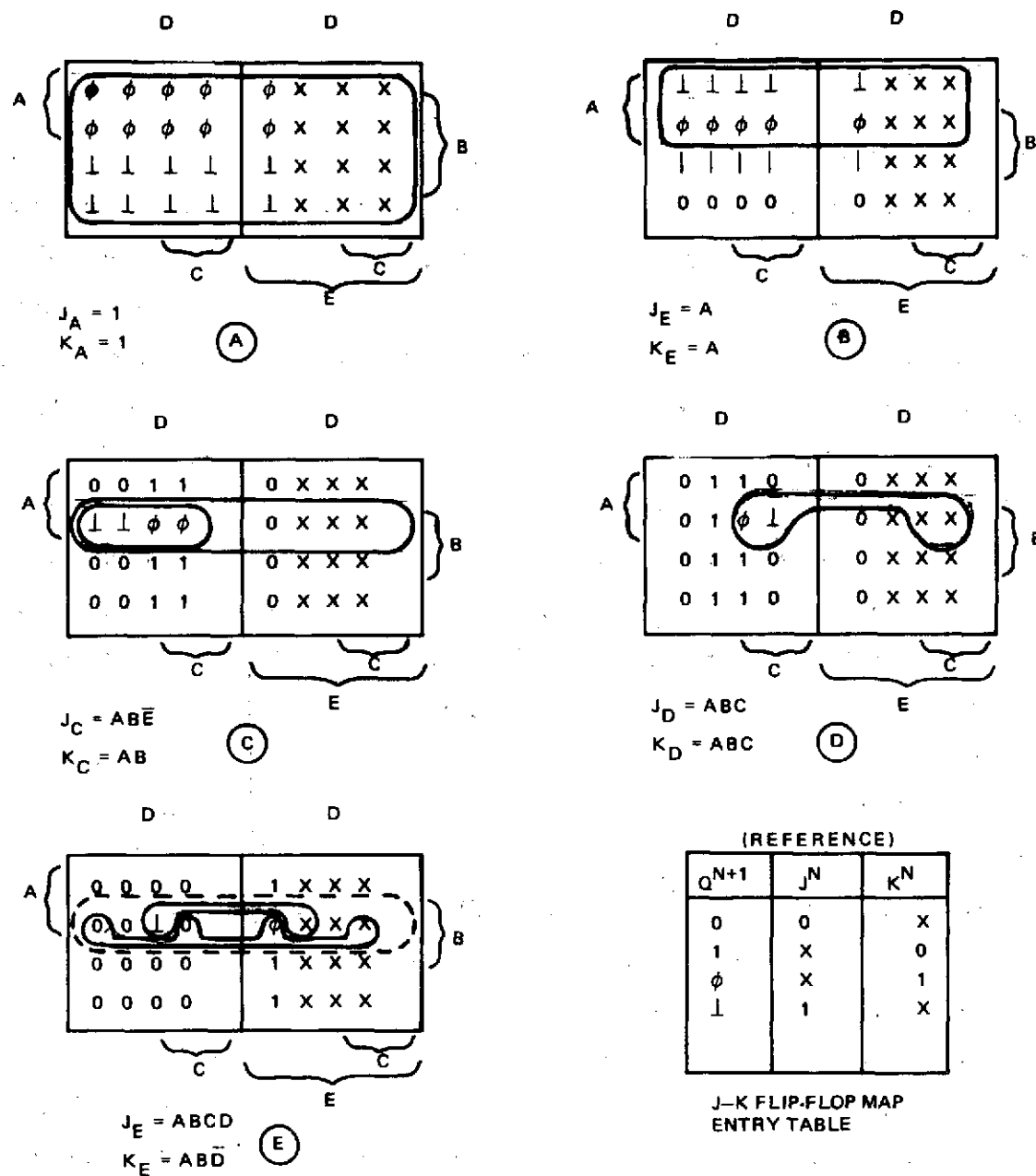
"A" Flip-Flop   - $J_A \equiv K_4 = $ "1" (i. e., inputs are held fixed at a "one" state)

"B" Flip-Flop   - $J_B \equiv K_B = A$

"C" Flip-Flop   - $J_C = AB\overline{E}$

$K_C = AB$

5-23

TABLE 5-1

MODULO 20 COUNTER STATE CHANGE SCHEDULE

Binary No.	Time (n) E D C B A	Time (n+1) E D C B A	Map Entries E D C B A
0	0 0 0 0 0	0 0 0 0 1	0 0 0 0 ⊥
1	0 0 0 0 1	0 0 0 1 0	0 0 0 ⊥ φ
2	0 0 0 1 0	0 0 0 1 1	0 0 0 1 ⊥
3	0 0 0 1 1	0 0 1 0 0	0 0 ⊥ φ φ
4	0 0 1 0 0	0 0 1 0 1	0 0 1 0 ⊥
5	0 0 1 0 1	0 0 1 1 0	0 0 1 ⊥ φ
6	0 0 1 1 0	0 0 1 1 1	0 0 1 1 ⊥
7	0 0 1 1 1	0 1 0 0 0	0 ⊥ φ φ φ
8	0 1 0 0 0	0 1 0 0 1	0 1 0 0 ⊥
9	0 1 0 0 1	0 1 0 1 0	0 1 0 ⊥ φ
10	0 1 0 1 0	0 1 0 1 1	0 1 0 1 ⊥
11	0 1 0 1 1	0 1 1 0 0	0 1 ⊥ φ φ
12	0 1 1 0 0	0 1 1 0 1	0 1 1 0 ⊥
13	0 1 1 0 1	0 1 1 1 0	0 1 1 ⊥ φ
14	0 1 1 1 0	0 1 1 1 1	0 1 1 1 ⊥
15	0 1 1 1 1	1 0 0 0 0	⊥ φ φ φ φ
16	1 0 0 0 0	1 0 0 0 1	1 0 0 0 ⊥
17	1 0 0 0 1	1 0 0 1 0	1 0 0 ⊥ φ
18	1 0 0 1 0	1 0 0 1 1	1 0 0 1 ⊥
19	1 0 0 1 1	0 0 0 0 0	φ 0 0 φ φ
0	0 0 0 0 0	0 0 0 0 1	0 0 0 0 ⊥

Figure 5-12. Karnaugh Mappings of Flip-Flop Input Conditions for
Sample Design Modulo 20 Counter

5-25

"D" Flip-Flop   - $J_D \equiv K_D = ABC$

"E" Flip-Flop   - $J_E = ABCD$
$K_E = AB\overline{D}$

When these equations are converted into a hardware design, the counter configuration appearing in figure 5-13 is the end result. This arrangement of flip-flops and gates satisfies both the foregoing input equations and the original stipulation of minimized MR factors throughout. The MR factor for all stage outputs is one (1), corresponding to the delay through a single binary, while the largest stage input MR factor is two (2), equivalent to the delay through one binary and one logic gate in series.

While the counter will, exactly as shown, sequence through the specified states in the state change schedule of table 5-1 in proper order once started correctly, there remains one additional point to consider before committing any hardware to the design. In particular, it must be determined whether the counter is able to correct itself if it should be started in or otherwise be forced into one of the disallowed binary number count conditions, "20" through "32." About the most expeditious procedure for making this determination is to prepare a complete state diagram for the counter as it stands and examing this diagram for lock-up conditions occurring outside the master or trunk loop. As seen in figure 5-14a, such a subloop from which the counter cannot extricate itself does exist. At this point one of two tracts can be taken. One is to simply leave the design alone and rely on use of the forced initializing reset at some externally predetermined number of count cycle periods to ensure that the counter never remains out of its trunk loop for an extended time. In many applications such an arrangement is completely satisfactory, particularly if the given counter is used as a subunit whose operation is slaved to and controlled by a larger master counter somewhere in the system.
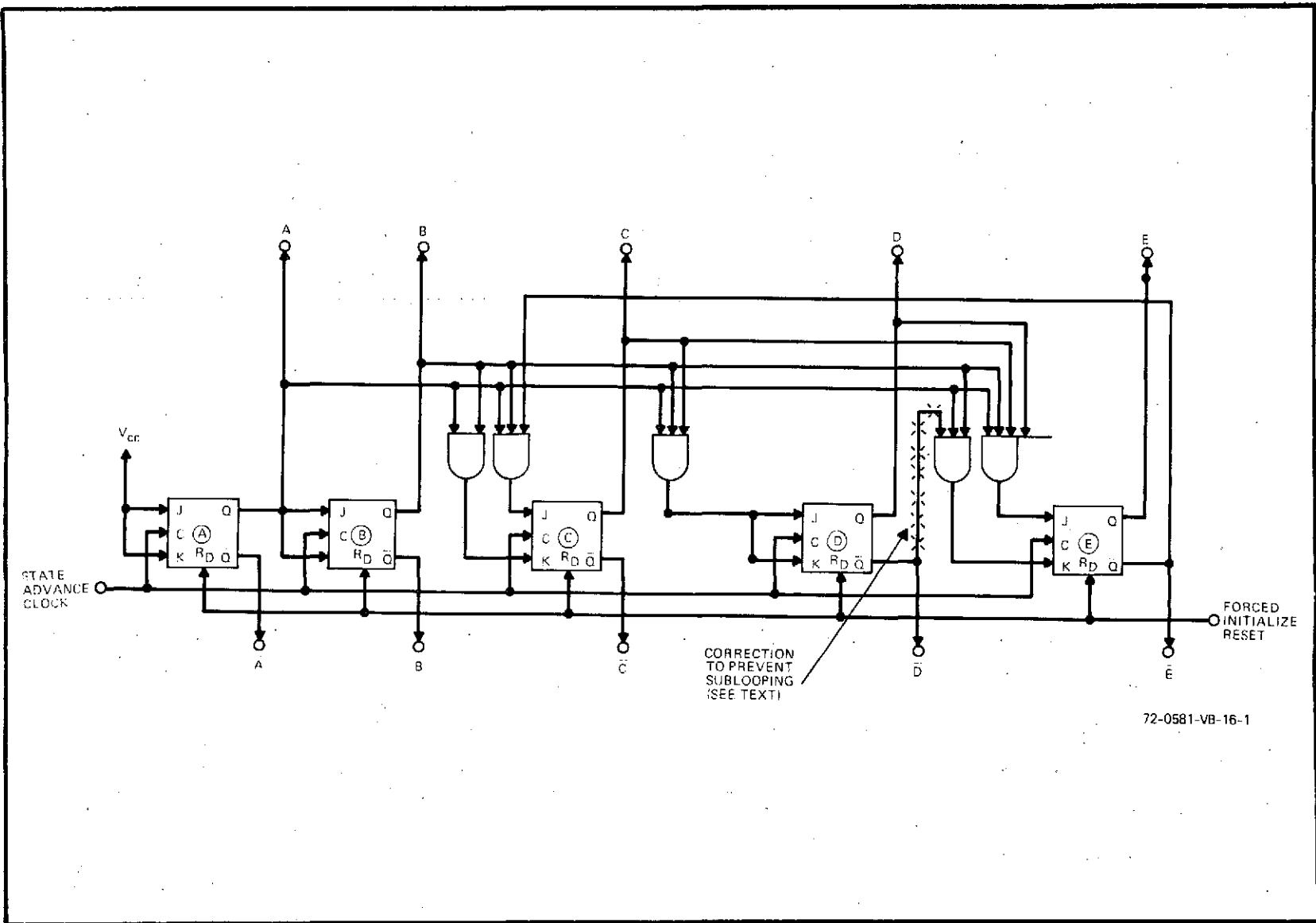
Figure 5-13. Circuit Diagram Implementation of Modulo 20 Counter Flip-Flop Input
Equations Derived from Karnaugh Maps

Instead of just letting things ride, though, it is much better practice to check further into the counter sublooping situations so as to discover a means of preventing it. In the course of these investigations it will soon be recognized that it is necessary to adjust the input conditions to one of the last three stages (i.e., flip-flops C, D, or E) in a fashion so contrived that the affected stage will be tripped out of its locked condition at some point in the subloop. While there are numerous possibilities here, the simplest corrective measures is to delete the $\overline{D}$ connection to the AND gate driving the K input of the E flip-flop so that the resultant input equation becomes

$$K_E = AB$$

This modification, which picks up additional states in the E flip-flop Karnaugh mapping in figure 5-12 to make the grouping maximally inclusive (as it should have been originally), causes the occurrence of simultaneous high states at the A and B outputs to be immediately intolerable to the E stage when it is in its high state and result in its undergoing a transition of states at the next clock time. Any situation that causes the counter to enter one of the states formerly in the lock-up subloop is therefore aborted and the counter is routed back over an open return path to its proper trunk loop. Confirmation of this fact is ultimately supplied by preparing a new state diagram for the adjusted counter design, such has been done in and no new closed loops have been introduced. With this final measure of assurance, the finished counter design can be confidently relied on to perform as expected.

From the foregoing development of a representative synchronous counter design, it has undoubtedly become ponderously evident that the complete procedure for deriving and confirming the design of fully synchronous counter-decoder style timing logic "from scratch" requires much greater care than either asynchronous C/D timers or S/R sequencers. The rewards in performance when dealing with high data rate systems having critical timing

5-28
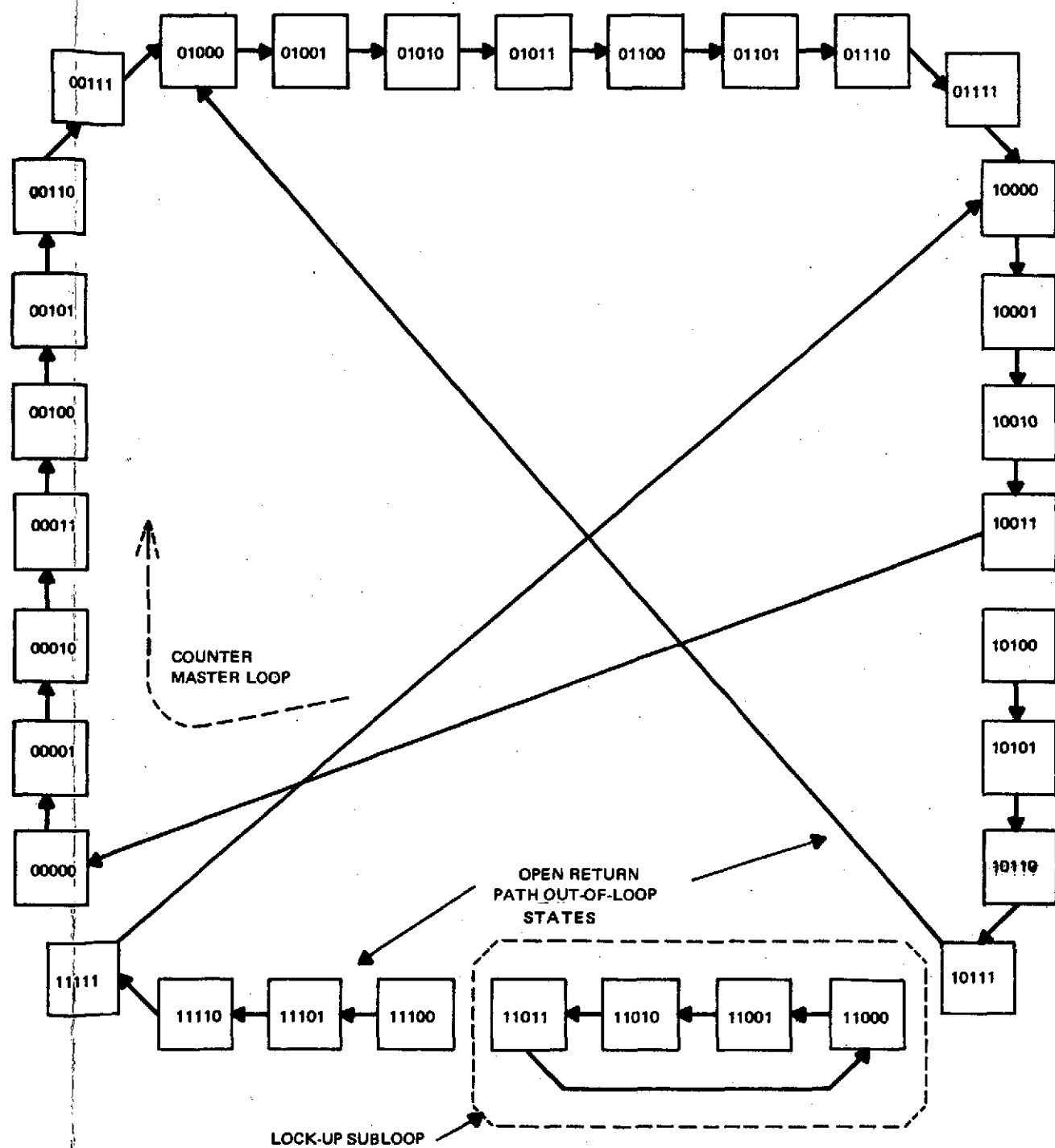
(a) ORIGINAL CONTAINING UNCOMPENSATED LOCK-UP SUBLOOP
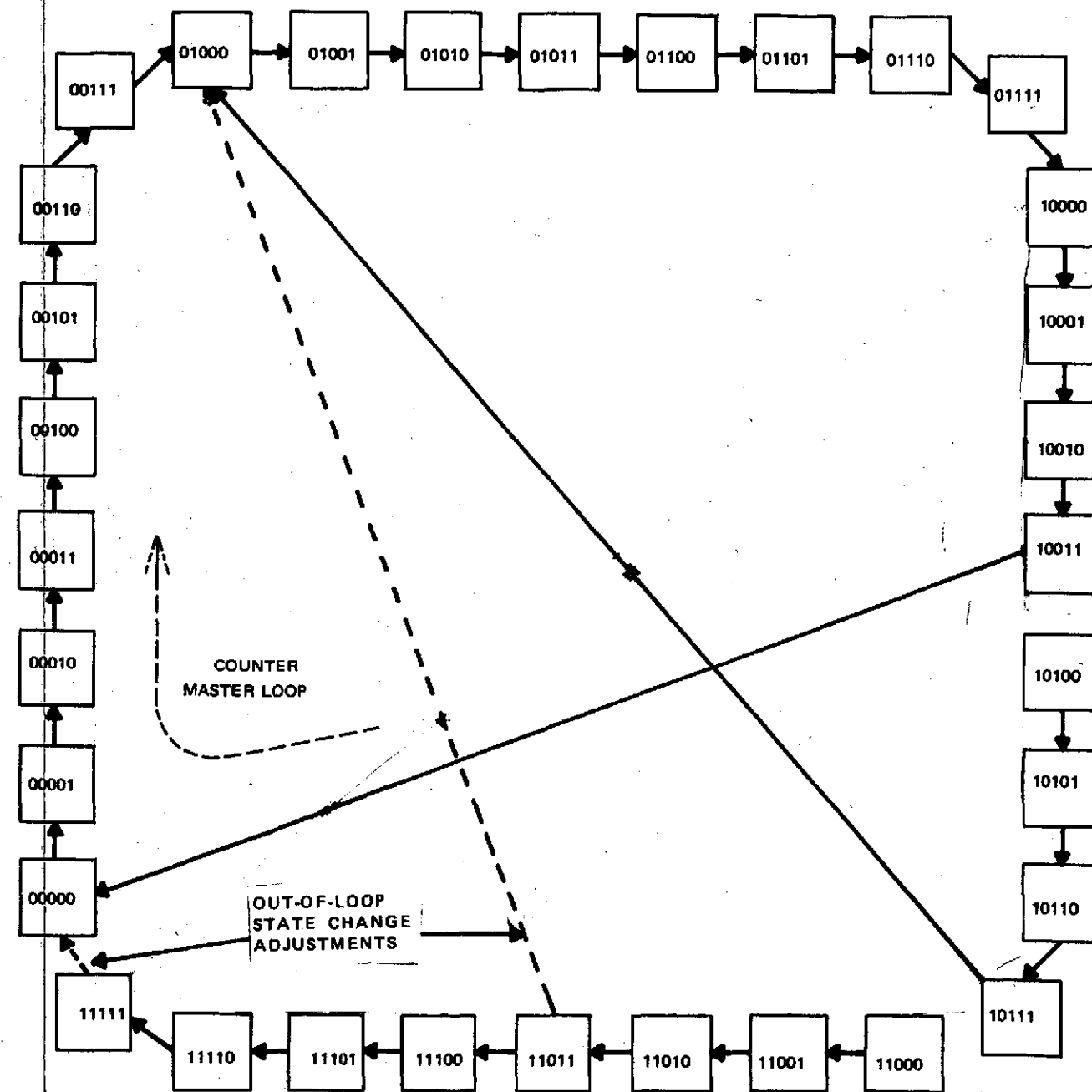
(b). MODIFIED WITH LOCK-UP SUBLOOPING CONDITION ABORTED

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Figure 5-14. State Diagrams for Modulo 20 Counter Design

requirements far outweigh such preliminary discomforts. Another fortunate fact enhancing further the attractiveness of synchronous C/D circuitry, even in less demanding applications where asynchronous C/D or S/R electronics would serve the purpose, is that much of the fundamental design work on numerous counters and a variety of decoder configurations has already been carried out by manufacturers of commercial logic families who have made them available as a wide and rapidly expanding menagerie of standard product line MSI devices.

By capitalizing on the ready availability of these well designed and specified counters and decoders, high quality synchronous timers can be assembled with comparative ease without going through the extensive design derivations elucidated above. The circuit configuration depicted in figure 5-15, for instance, appears quite simple but actually exhibits a fairly high degree of sophistication. It is a synchronous counter/decoder which employs split-phase clocking to achieve overlap time-shared interrogation of 32 sensor array columns. It generates the type of output waveforms shown previously in figure 5-6b, but its complete design was established solely from a timing diagram and a cursory knowledge of digital switching circuits. No input/output boolean equations, state diagrams, Karnaugh maps, or any other specialized design aids were needed since the fundamental counter designs had already been checked out by the manufacturer. The system designers task has thus been greatly eased by the ability to generate complex counter arrangements for use as subunit parts in a larger composite system without going through the time consuming job of dickering with the state change relationships of every binary in a counter chain.

As was indicated, earliest design concepts for solid-state array cameras assumed simple shift register scanning. The technology available at the time, though, was not able to deliver registers of sufficient length or reliability. Consequently, since the design sophistication to handle
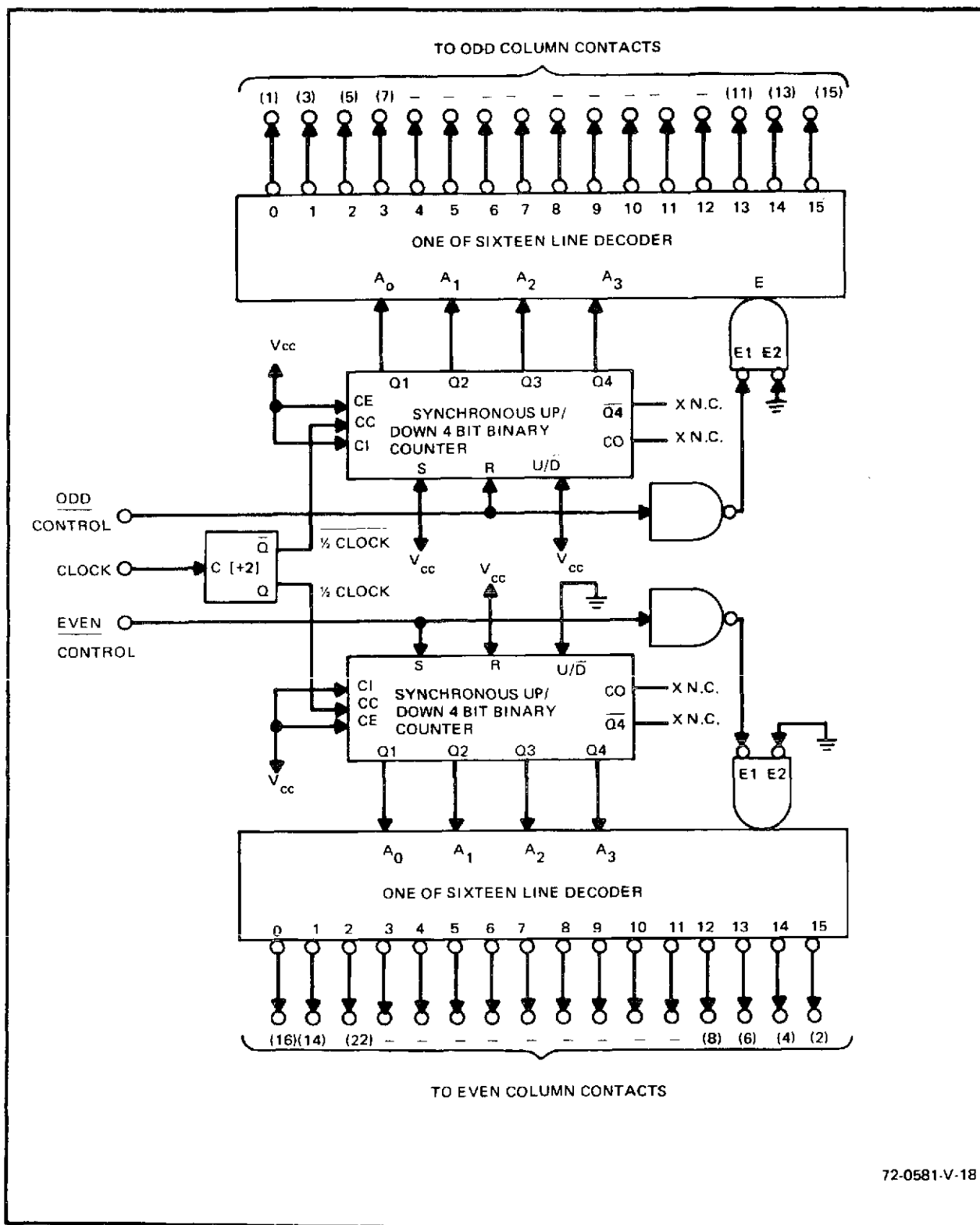
5-31

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Figure 5-15. Time-Shared Synchronous Counter/Decoder Column
Sequencer Design Using Commercial Logic Blocks

5-32

synchronous counters had not yet been adequately evolved, the natural next step was to asynchronous logic. With time the dominant logic arrangement ultimately swung around to fully synchronous clocking schemes, due largely to their inherently higher speed capabilities.

A similar evolution in the types of devices used has also taken place. Experimentation at its very earliest stages used discrete switching transistors. Next came DCL (direct coupled logic) - merely an extension of discrete transistor switches; then RTL (resistor-transistor logic) - a slight modification of DCL; and, finally, DTL (diode-transistor logic) - the first truely noteworthy general purpose logic family. This family was subsequently used with sensor arrays ranging in size from 1-x-5 element lines to 200 x 256 element matrices. The next refinement was to TTL (transistor-transistor logic) - a highly adaptive family for which a major proliferation of complex functions has been developed. It is presently the dominant choice of logic types for applications calling for clocking rates under 50 MHz. Above that ECL (emitter coupled logic) - a nonsaturating family - becomes preeminent. At the other end, below 2 MHz, CML (complimentary MOS logic) is currently coming on very strong due to its greatly reduced power consumption.

It has only been with the development of this latter family, CML, that register chains of any appreciable length have begun to become economically practical to build. Due to the low volume call for them though, and the fact that they would almost automatically have to be sold in chip form due to packaging problems, no serial-in/parallel-out registers of greater than 20 bits have been made available commercially. The present best choice of logic types and organizations is therefore in a highly volatile state, with a mix of families and/or circuit configurations frequently proving optimum in particular cases. The trend in solid-state array cameras is toward more extensive use of CMOS circuitry, however, and it is believed that the CML family will rapidly take over most jobs below 10 MHz in the next few years and ultimately be totally dominant in imaging systems.

5.2 SIGNAL ACQUISITION

Despite its simple X-Y accessed design, there are a great many different ways of interfacing with and scan converting the image data from a phototransistor mosaic. The basic arrangements which were used in all the earliest developmental model image converters built by Westinghouse called for driving either the collector strips or the emitter lines with active pull-up and/or pull-down saturated bipolar logic devices while commutating the elemental signal information bits at the opposing electrode (emitter or collector, respectively) access terminals through SPST (single-pole-single-throw) analog FET switches which were summed directly into an operational amplifier. The basic features of this signal handling scheme implemented for emitter readout are presented in figure 5-16. Active logic gates shown here drive the array collector strips, in sequential fashion, alternately between the low ground state and a high V_{CC} level. During the time that any given collector row is high, the emitter line FET's are
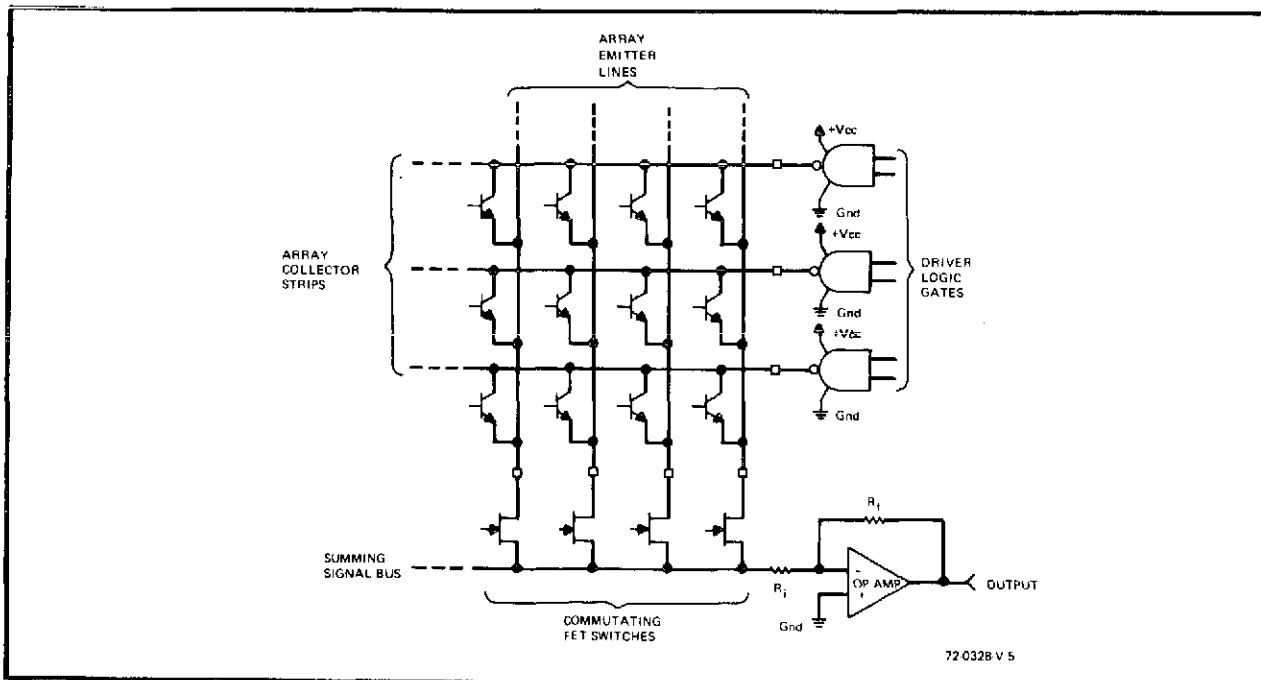

Figure 5-16. Standard Emitter Readout for Phototransistor Arrays Using J-FET Line Commutation and Operational Amplifier Signal Scanning

progressively sequenced to commutate successive emitter accessed signals directly onto a common summing bias that is connected to the summing node of a conventional operational amplifier.

Systems using arrays of up to 200-x-256 elements were eventually implemented with reasonable success with fundamentally unrefined forms of this peripheral circuitry, but the performance of each fell somewhat short of what had been projected. One of the fundamental problems that existed with the circuitry, and which served to restrict its lower end dynamic range, was that a small portion of the signal charge coupled out of the sensor elements was lost through the gate electrode of the junction field-effect type of commutating devices employed. Moreover, the dynamic "ON" impedance of these devices was found to vary inversely with the emitter line signal voltage amplitude as a result of source impedance induced negative feedback causing their gate-to-source control voltages to fluctuate. Both of these effects, gate junction charge extraction and ON impedance variation with signal level, acted to degrade the inherent dynamic range capabilities of the sensor array. As a result, six gray shade renditions was about the best that was ever secured from any system implemented with such circuitry.

A further factor restricting extension of this basic approach to larger sensor arrays - such as the 400-x-500 mosaic - is that very high speed MOS or J-FET switches with at least moderate drive capabilities and exceptionally low R_{ON} resistances would be required. In particular, for a 400-x-500 element system it will be found, for typical parameters of

$C_{CB} \simeq 0.1$ pF (collector-to-base capacity)

$C_{ES} \simeq 60$ pF (emitter line-to-ground capacity)

$\beta \simeq 30$ (beta of phototransistor)

$\tau_{EL} \simeq 106$ nsec (period of master clock)

that the combined load and device resistance should satisfy

$$(C_{ES} + \beta C_{CB}) (R_{ON} + R_{LOAD}) < 1/4 \ \tau \ Element$$

$$(R_{ON} + R_{LOAD}) < [106/4 \ (60 + 3)] \times 10^{-9} \times 10^{12}$$

$$(R_{ON} + R_{LOAD}) < (106/252) \times 10^{4}$$

$$(R_{ON} + R_{LOAD}) < 500 \ ohms$$

However, the switching device's R_{ON} resistance alone will be of this magitude (for any device of acceptable size) - and will typically vary by up to 20 percent from unit-to-unit. From this observation it is apparent that the recharge time constant is so short as to preclude using such a scheme with large, high density array readout systems.

Additional anomalous effects attributable to the commutation devices in early systems, which detracted from the cosmetic quality of their displayed images by introducing vertically oriented line pattern noise, were the result of intradevice nonsymmetry and interdevice inequality in the feedthrough switching transients coupled through their respective gate-drain capacitors. Recognition of these device and circuitry organization shortcomings in the early stages of design review for the electronics to be used with 400- x-500 element mosaic (shown previously in figure 3-1) led to specification of the array interface and signal acqusition circuitry design modifications revealed in figure 5-17. The principal innovations appearing in this figure are (1) specially built monolithic n-channel MOS-FET commutating devices, (2) unique low-impedance current summing networks, and (3) higher order multiplexed signal processing.

By overlapping the recharge intervals for successive elements, this improvement of the basic emitter readout circuitry facilitates handling extremely high data rates. In particular, the speed and R_{ON} requirements of the per-line FET switching devices can be relaxed to nearly any level desired by increasing the degree of multiplexing employed. There are practical limits
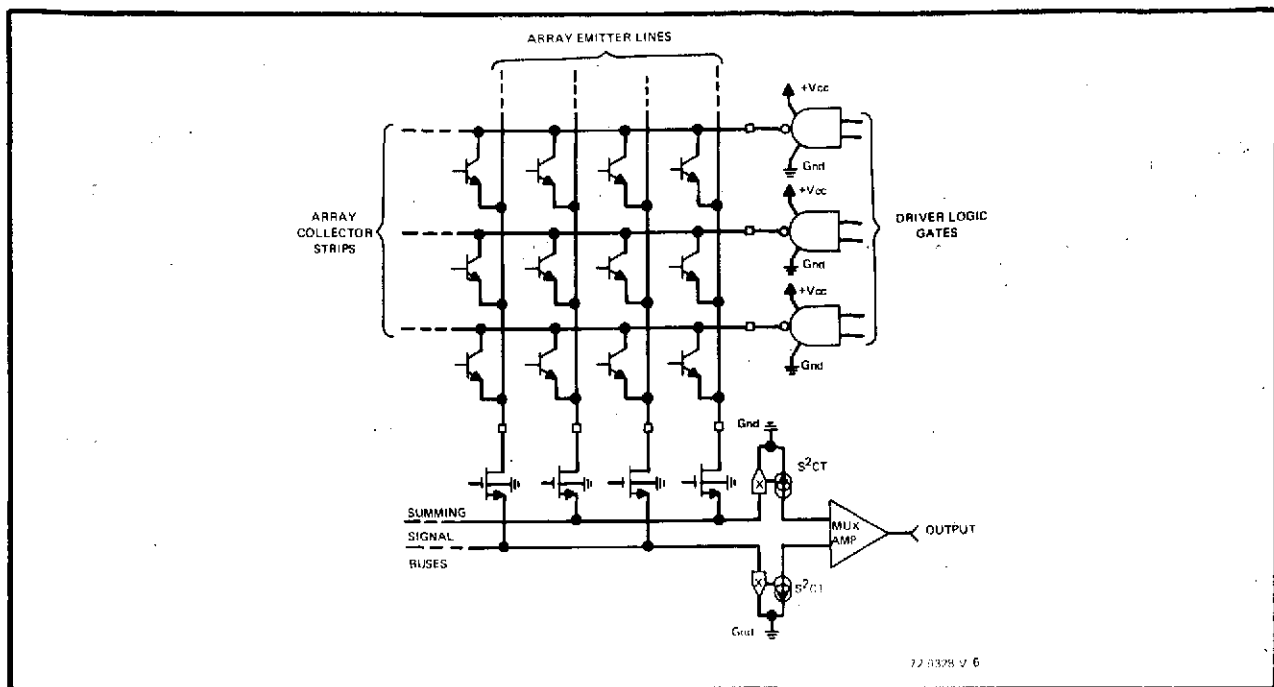
Figure 5-17. Time-Shared Emitter Readout for Phototransistor
Arrays Using Multiplexed MOS-FET Line Commutation and Solid-
State Current Transformer Signal Summing

to this process though, since higher order multiplexing greatly increase
the complexity of the logic encoding and selection circuitry. Consequently,
the least degree of multiplexing consistent with sufficiently relaxed switch-
ing requirements will provide the best tradeoff between performance and the
high cost of additional system complexity.

For a 400-x-500 element readout system using a 9.45 MHz master clock, it
is apparent that the normal serial per element recharge interval will be
only about 106 nsec. By using eighth order multiplexing this period can be
increased by exactly a factor of eight; i.e., if m = multiplex order, then the
per element multiplexed recharge period will be given by

$$\tau_{recharge} = m \, \tau_{clock} \approx m \left[3 \, (C_{ES} + \beta \, C_{CB}) (R_{ON} + R_L) \right]$$

which, for the conditions cited where m = 8, yields

$$\tau_{recharge} = 8\ \tau_{clock} \approx 8 \times 106 = 848\ nsec$$

Since it was the resistance factors in the expression for τ_{clock} that controlled the upper data rate limit, it is obvious that the restriction on total resistance can now be lowered by one-eighth; i.e., with m = 8, R_{total} can be

$$R_{total} < 8 \times 500 = 4.0\ Kohms$$

If this value is split evenly between R_{ON} and R_L, then the per line selection devices "ON" resistance need only be

$$R_{ON} < 2\ Kohms$$

and this can be achieved relatively easily and with good consistency using state-of-the-art silicon planar processing technology.

Development of these monolithic commutation device strips has accordingly been accomplished and has overcome the device-to-device characteristic variations of discrete units noted earlier quite well. The fact that they are MOS in structure also assures good symmetry in their feedthrough transients (a fact which can be used to advantage in nulling out spikes). Discovery and application of the uniquely characterized solid-state current transformer network for performing the signal summing function at the commonalized source leads then provides a means of preventing negative feedback from causing the "ON" impedance of the commutation devices to vary with signal amplitude. Multiple parallel-sequenced selection of signal lines possesses the additional attribute of lowering the total parasitic capacity tied to the input of each of these summing amplifiers to 1/m (i.e., 1.8 for m = 8) of the single bus total, while simultaneously facilitating rejection of commutation induced noise by the principal of coincident sampling windows. Through these facilities, the system electronics built for the 400-x-500 element camera is able to output video with low coherent pattern noise and realize images having eight shades of gray.

Continuing efforts in the realm of system refinement have led most recently to the evolution of an advanced signal acquisition philosophy whereby the form of the video produced is no longer a series of amplitude variable pulses of marginal duty cycle but is rather a 100-percent duty cycle boxcar video chain. The process involved is analogous to a sample-and-hold operation, but it is executed directly at the array accessing terminals as part of the scan conversion process rather than being tacked-on as an after thought introduction of some form of serial S-and-H circuitry. In addition to producing boxcar video, this array readout scheme provides significantly improved sensor terminal parameters and buffers the array so that high speed commutation transients cannot effect the distribution of charge infor- mation within the matrix.

As indicated in figure 5-18, application of this system refinement - which has been named dump-and-store (abbreviated DUST) signal acquisition - to a phototransistor monolith involves first rotating the array by 90 degrees
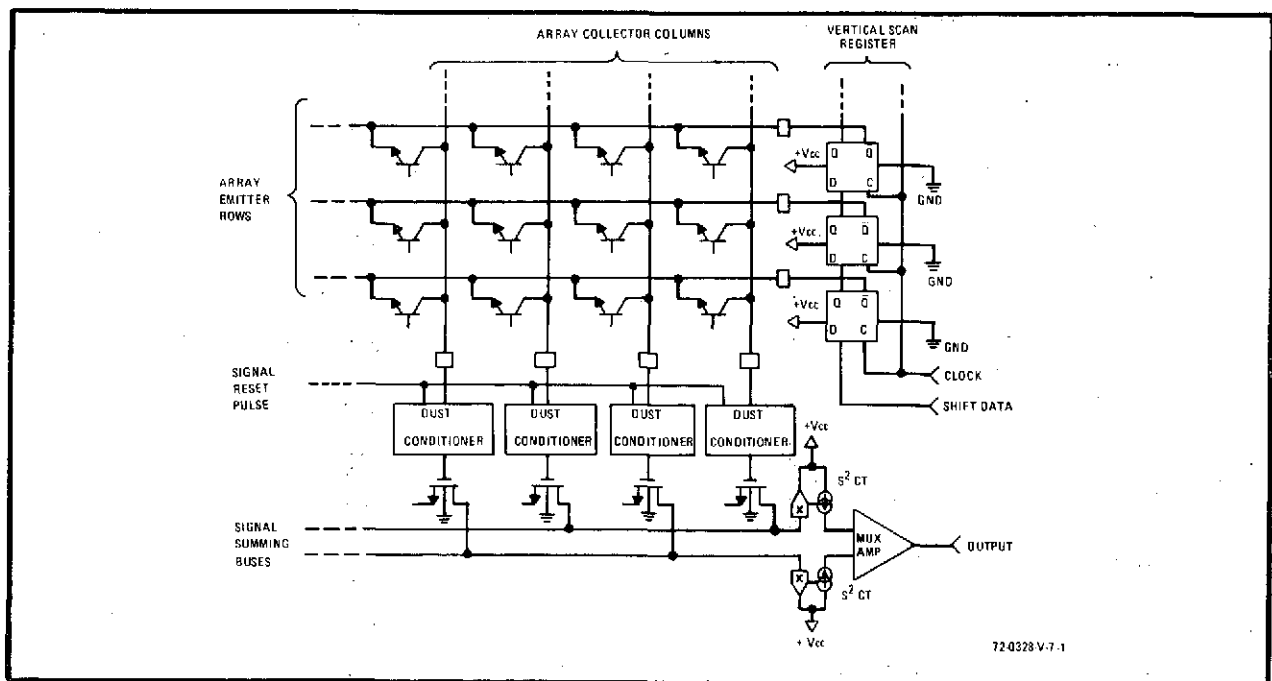

Figure 5-18. Time-Shared DUST Interface for Phototransistor Arrays Using Multiplexed MOS-FET Column Commutation and Solid-State Current Transformer Signal Summing

5-39

from its former orientation with direct accessing line commutation procedures. Signal information pumped out through the collector columns in parallel each time an emitter row is activated to its low state by the slow scan vertical shift register is subsequently conditioned and held as an analog level by the DUST circuitry. High speed time-shared gating of successive signal bit current conversion MOS-FET's followed by serial multiplexing to reject gating transients then completes the scan conversion process and yields a 100 percent duty cycle, boxcar form of analog output signal.

Functionally the DUST principal is surprisingly simple. It is developed from (1) observing that an integration mode photosensor, when configured in a monolithic array, will be at least partially "dumped" (i.e., readout or reset) immediately following activation of the first array access line to which it is connected due to the large parasitic capacitance which exists on the opposing access line; and then (2) posing the question, "Why not enhance this effect by forcibly dumping the element through an externally controllable mechanism and thus bypass the effects of terminal parasitics?" Figure 5-19(a) shows this idea put into practice using the S^2CT network as the external forcing function mechanism which linearly passes intelligence bearing signal charge through to a holding capacitor, C_H, and, by virtue of its unidirectional nature and extremely low input impedance characteristic, provides full buffering of the array plus shorted-out shunting of array parasitics. The circuitry within the dashed outline corresponds to that found in each of the "dust conditioner" blocks of figure 5-18.

Following changeover of a row (i.e., emitter line) switch to its ground state, the signal information from an entire line of sensor elements will, with this arrangement, be transferred out of the array through the respective S^2CT networks and be held (temporarily stored) in parallel on the C_H capacitors as a series of analog signal potential bits. The individual output
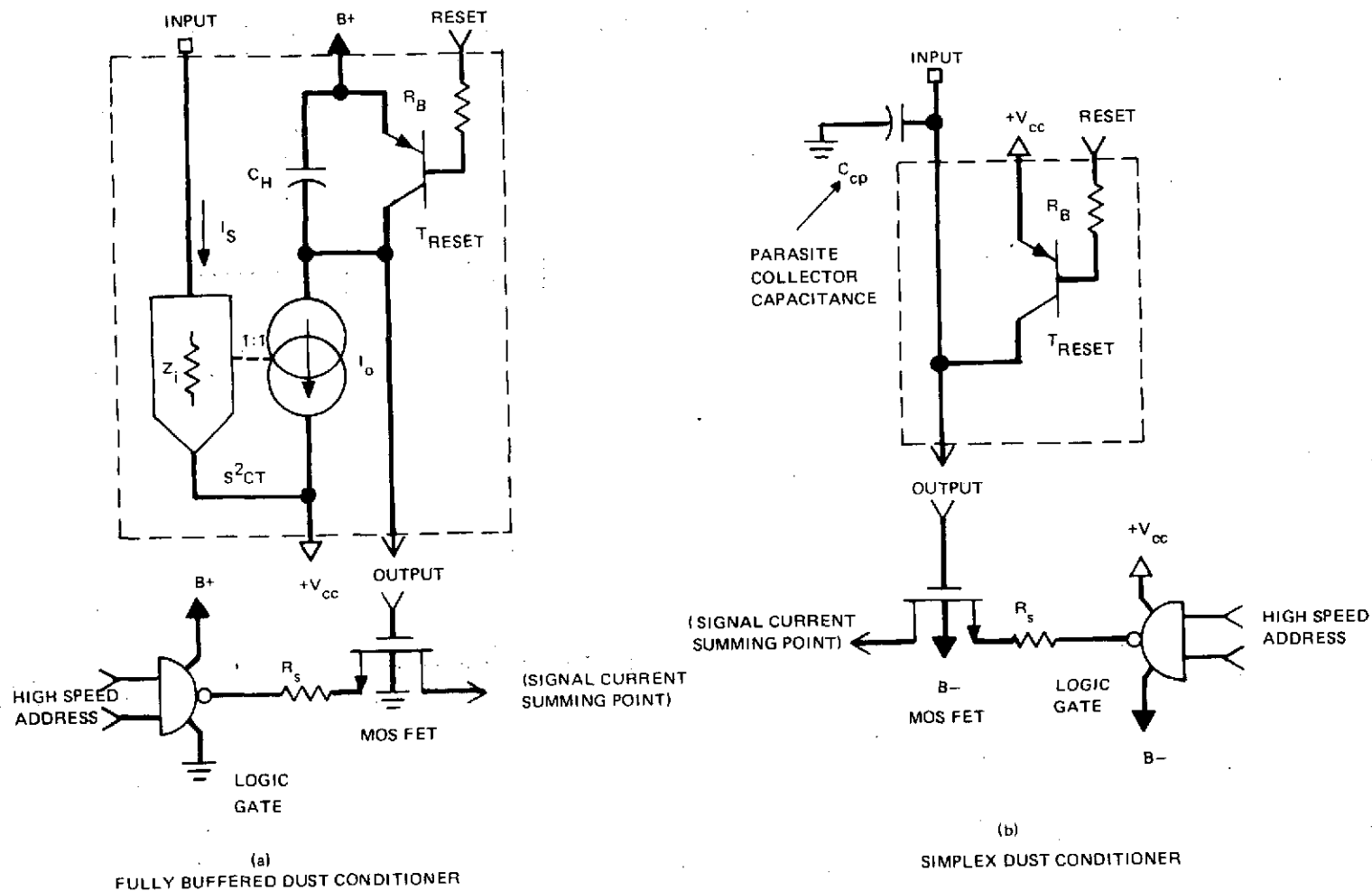
Figure 5-19. Alternate DUST Conditioner Circuitry for
Integrated Array Imagers

signals subsequently available for commutation by the current conversion follower MOS-FET's will accordingly follow the relationship

$$v_o = V_o = (1+\beta) \left[\frac{Q_{io} + Q_\lambda \left(\frac{\tau_\ell}{\tau_i}\right)}{C_H} \right] (1-\epsilon^{-\tau_i/\tau_\ell}) \qquad \text{DUST}$$

where Q_λ is the quantity of minority carrier charge generated by photon irradiation, Q_{io} is the initial value of charge stored in the sensing junction capacitance, τ_ℓ is the leakage or recombination time constant of the junction, τ_i is the integration period, C_H is the external signal charge holding capacitance, and β is the beta gain of the phototransistor when in its active region. Opposed to this, the output obtained from each element under equivalent standard collector readout conditions would be

$$v_o = (1+\beta) \left[\frac{Q_{io} + Q_\lambda \left(\frac{\tau_\ell}{\tau_i}\right)}{C_{CP} + C_{BC}(1+\beta)} \right] (1-\epsilon^{-\tau_i/\tau_\ell}) \; \epsilon^{-t/R_L \left[C_{CP}+C_{BC}(1+\beta)\right]}$$

$$\text{STAN}$$

where the extra factors in evidence are R_L, the signal developing load resistance, C_{CP}, the parasitic collector line capacitance, and C_{BC}, the detection diode's depletion layer capacitance.

In confirmation of earlier declarations, comparison of the above DUST and STAN equations points up the fact that the output with dump-and-store signal acquisition is a 100 percent duty cycle, invariant voltage level over each element sample period; whereas for standard signal readout it is a transient spike whose decay time constant, $R_L \left[C_{CP}+C_{BC}(1+\beta)\right]$, depends on the various terminal loading factors. It should further be observed that the quantity of charge pumped out of the sensor upon activation of its first address line, namely

$$Q_s = (1+\beta)Q_b = (1+\beta)\left[Q_{io} + Q_\lambda\left(\frac{\tau_i}{\tau_\ell}\right)\right](1-\epsilon^{-\tau_i/\tau_\ell}),$$

is controlled by the intrinsic quanta conversion parameters of the detector and is totally independent of the final output loading time constants. Consequently, by detecting a direct function of this charge (specifically, the charge accumulation voltage across a capacitor) rather than a time differential function of that charge (such as the charge flow voltage developed across a resistor) virtually complete utilization is made of the inherent capabilities of the device.

Besides the many obvious advantages of the dust principal over more conventional practices, it turns out that one of the fundamental elements required in its formation (namely, a storage capacitance) can be instituted in surrogate form by making use of a previously undesired parasite within the sensor monolith structure; i.e., the collector bus capacitance, C_{CP} (see figure 5-19(b)). While a "simplex" form of dust conditioner formed in this manner produces "boxcar" video like the fully buffered dust circuitry, it looses all aspects of the latter's array isolation capabilities due to elimination of the S^2CT coupling network. In noncritical applications it will perform nearly as well as the true DUST technique, however. And, in practically all instances, can be implemented more simply and with less associated peripheral circuitry than any other type of sensor readout. The DUST philosophy on signal acquisition (in one or the other of its alternate forms) has, therefore, become the preemptive choice for all future solid-state array camera systems.

5.3 SIGNAL PROCESSING

Processing of signals in an integrated array camera, as in any image capture/transfer/utilization system, involves all those signal handling operations necessary to place the scan converted image intelligence from the photodetector in a form usable by the information outputting mechanism. It begins at the interface to the sensor and terminates at the output of the camera. From there on handling of the image data is the responsibility of the intermediary channel transfer structure and the receiving signal consumption device.

Even in the simplist image converter, processing involves some type of summing to combine successive bits of image data and at least a nominal degree of amplification to boost the amplitude of sensed signals, but usually also includes format altering through the introduction of synchronization data to form a composite video and power buffering to drive coaxial cables. Other common operations for higher resolution converters are signal multiplexing to combine time-shared video channels and automatic gain control to maintain consistent signal levels under varying conditions. Another operation encountered occasionally is analog-to-digital (A/D) conversion to facilitate information transmission in noisy environments.

At times there may also be highly specialized signal handling techniques (for conditioning a video stream to enhance its intelligibility) applied within the camera, but these are not considered to be part of normal signal processing. They are accordingly covered separately in paragraph 5.4 of this report. The scope of our discussion here is limited to those modes of signal processing which act to change the form rather than the content of the image information carrying video. Emphasis will be on the more refined techniques that have been evolved for high resolution solid-state matrix array half-tone imagers like the engineering model "45" PICTURE camera.

The first processing operation in an integrated array camera occurs as a summing function performed on the successive elemental slices of video that are sequentially commutated out of the array. Details of the mechanics involved in implementing this and other processing functions in the system depend heavily on the mode of readout employed (i.e., whether signal acquisition occurs at the emitter or collector terminals of a phototransistor mosaic), the organizational format of scanning adopted, and the rate of sequencing involved; as well as on considerations of the type and parameters of available IC electronics, the constraints imposed on physical size, and the factors effecting permissible power dissipation. In early developmental MIC (molecular image converter) systems, such as the 100-x-128 element converter in figure 5-20, initial commutation interface summing was provided by an ordinary operational amplifier because it was about the easiest known way of securing a nominally low impedance summing node. This arrangement, illustrated in figure 5-21, was made marginally acceptable by the fact that a moderately large (typically $\geq$ 2 K ohm) input line
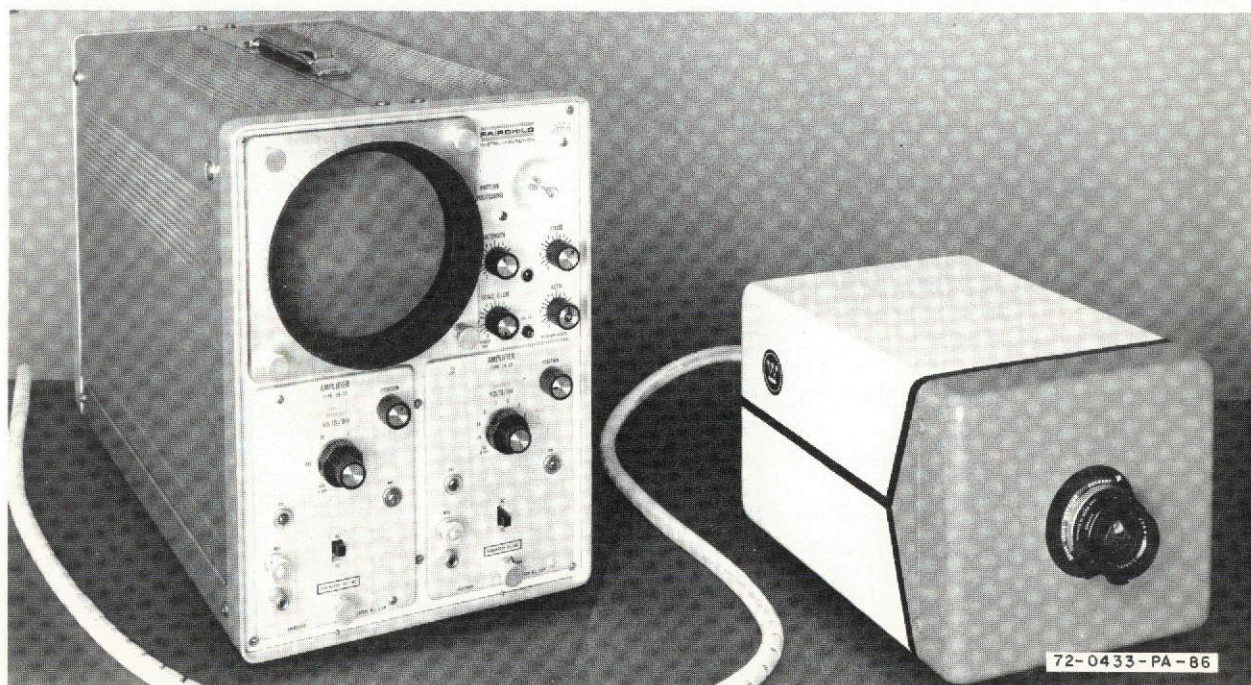

Figure 5-20. 100-x-128 Element Integrated
Array Camera and Monitor

FET SIGNAL SAMPLING SWITCHES

E_1 E_2 E_3 ETC. ← EMITTER COLUMN LINES

R_f

R_i

VIDEO OUT

$-A$

LOGIC SEQUENCING PULSE INPUTS
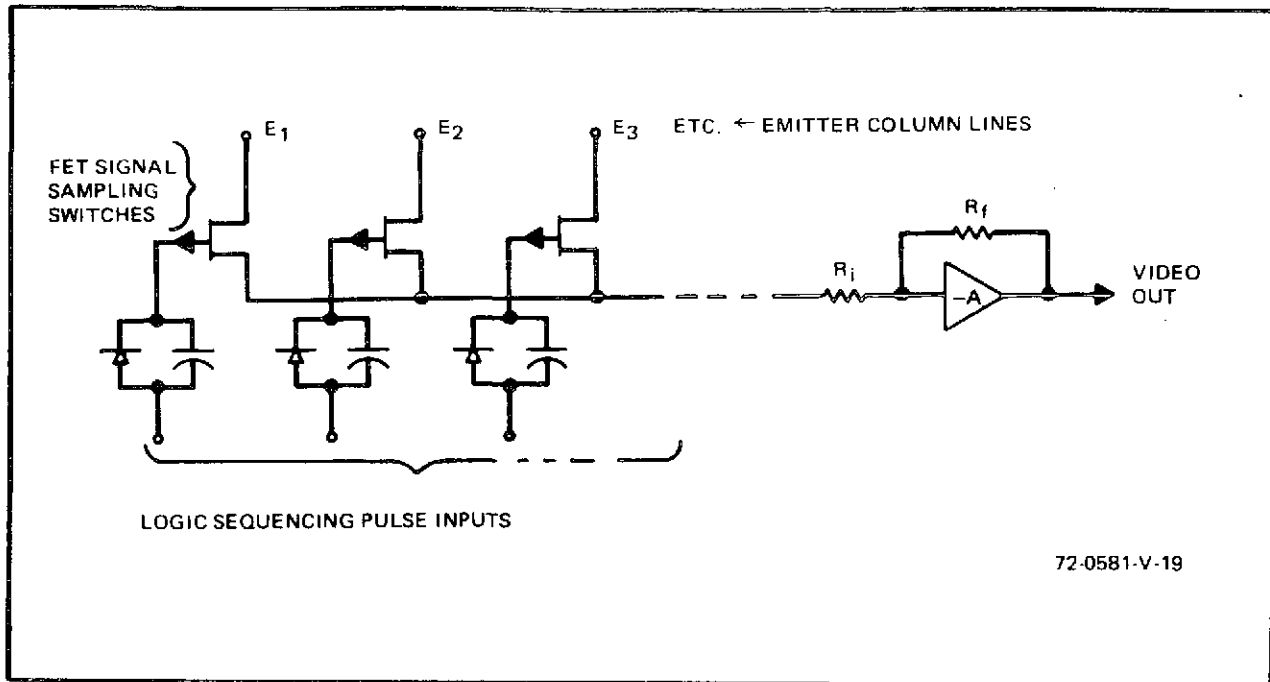
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Figure 5-21. Op Amp Commutation Summing

resistance R_i had to be employed to prevent the occurrence of transient overload saturation or possible lock-up of the differential input stages of the op amp. Due to this resistance, the successive emitter sampling FET switches did not operate into a low impedance and therefore suffered degenerate feedback with an attendant loss in dynamic range.

Another factor noted in the operation of the largest system to use op amp summing, namely the 200-x-256 element laboratory test vehicle, was that an increase in the number of lines commutated caused a further degradation of performance from capacitive loading. Some improvement of this condition was subsequently realized by breaking up the total number of lines into four groups, with each group being fed to a separate op amp. Having thus separated the totality of lines into four quadrants, though, it was necessary to recombine the individual signals into a common output by passing them through a second level of commutation (see figure 5-22). This scheme does

5-46

QUADRANT 1 EMITTER FET's
QUADRANT 2 EMITTER FET's
QUADRANT 3 EMITTER FET's
QUADRANT 4 EMITTER FET's

QUADRANT SEQUENCING LOGIC PULSE INPUTS

VIDEO OUT

2nd LEVEL SUMMER

PARALLEL 1st LEVEL SUMMERS
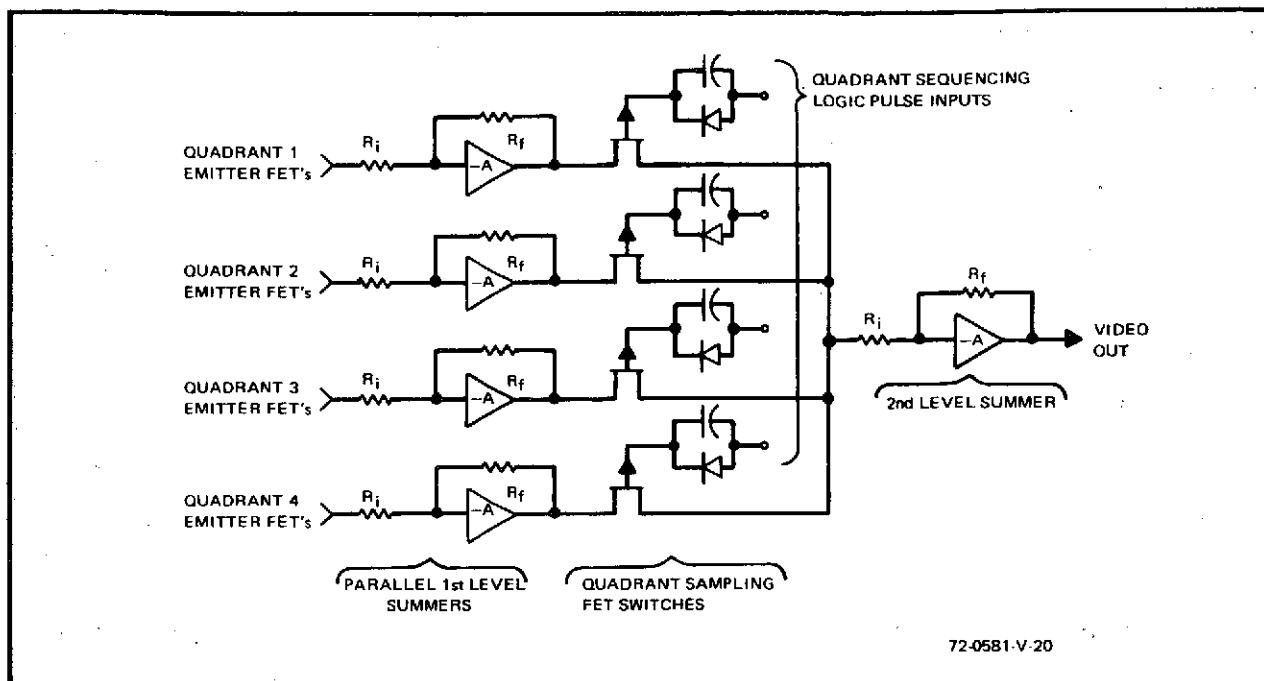
QUADRANT SAMPLING FET SWITCHES

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Figure 5-22. Dual Level Op Amp Commutation Summing

not constitute true time-sharing, since the signals moving along any two of the parallel summer channels do not occur simultaneously or time-overlap in any way; but it can be considered a first crude attempt at higher order signal multiplexing.

To institute true time-shared signal processing and thereby realize a reduction in the bandwidth requirements of the initial signal handling circuitry, the organizational format for scanning of the array must be changed. Instead of using serially contiguous edge-coincident pulses to interrogate the array, trains of parallel time-overlapping phased pulses must be generated (see paragraph 5.1) and used to gate only every second, or third, or fourth, or eighth, etc—depending on the number of parallel channels employed— element's signal commonly onto a specific channel.   In the 400-x-500 element MIC, eight channels are employed in the immediate vicinity of the array. These are segregated into two groups of four channels which, following

5-47

intermediate boost amplification, pass through a first level of multiplexing to serialize the eight original low bandwidth channels down to two channels having medium bandwidths. A final level of multiplexing is then applied to serialize these into a single high bandwidth video output channel.

An idealized timing diagram for this sequence of operations is presented in figure 5-23. To correlate the waveforms here with the points in the system where they apply, the simplified function diagram in figure 5-24 will prove helpful. The only apparent point of inconsistency between these two figures is that the timing diagram alludes to signals from system electronics called 4BFR's (meaning, simply, four bit folded registers) whereas the function diagram indicates no such circuits. Use of the 4BFR designation in the timing diagram is made because it is these registers which originate the time-overlapping sequence of pulses that are used in the initial array interrogation gating. The dashed transitory signals accompanying each of the 4BFR heavy gating pulse lines represent the analog image video commutated through the respective hybrid analog summer channels in figure 5-24.

Recognizing the shortcomings of prior commutation signal summers that made use of op amps, the "45" PICTURE camera has been supplied with the uniquely characterized three-transistor network type of summer seen in figure 5-25. This network, consisting of transistors Q1, 2, and 3 and descriptions referred to as a solid-state current transformer (S^2CT), forms an exceptionally good summer due to its inherent characteristic input impedance Z_i being on the order of only 0.1 ohm – which is less than the ESR (equivalent series resistance) of an ordinary filter capacitor. As a result, the series inputting resistance R_x appearing in figure 5-25 can be as low as 10 ohms and still satisfy the inequality $R_x \geq 100 Z_i$ needed to ensure that a linear transfer will be realized from a voltage based signal source.
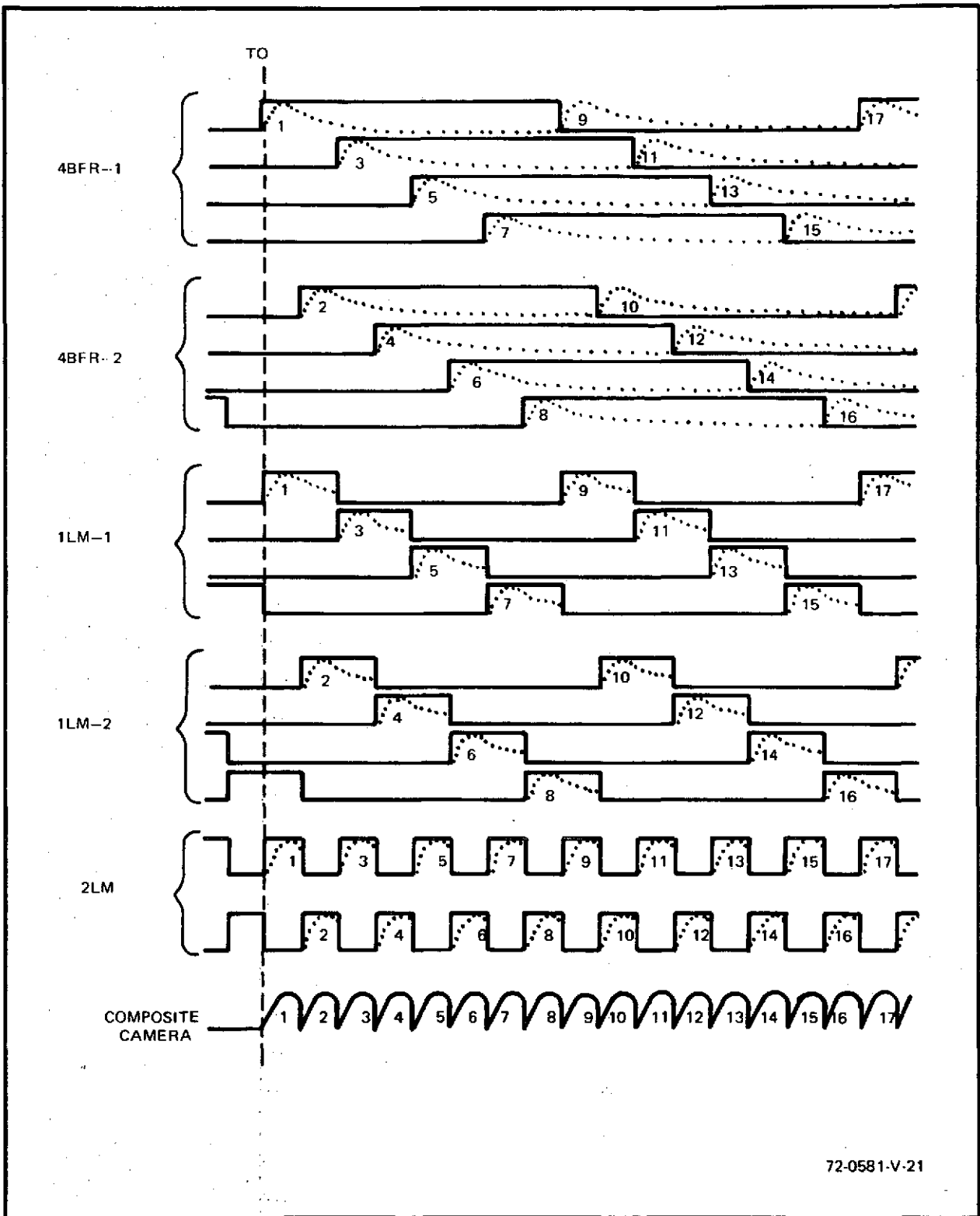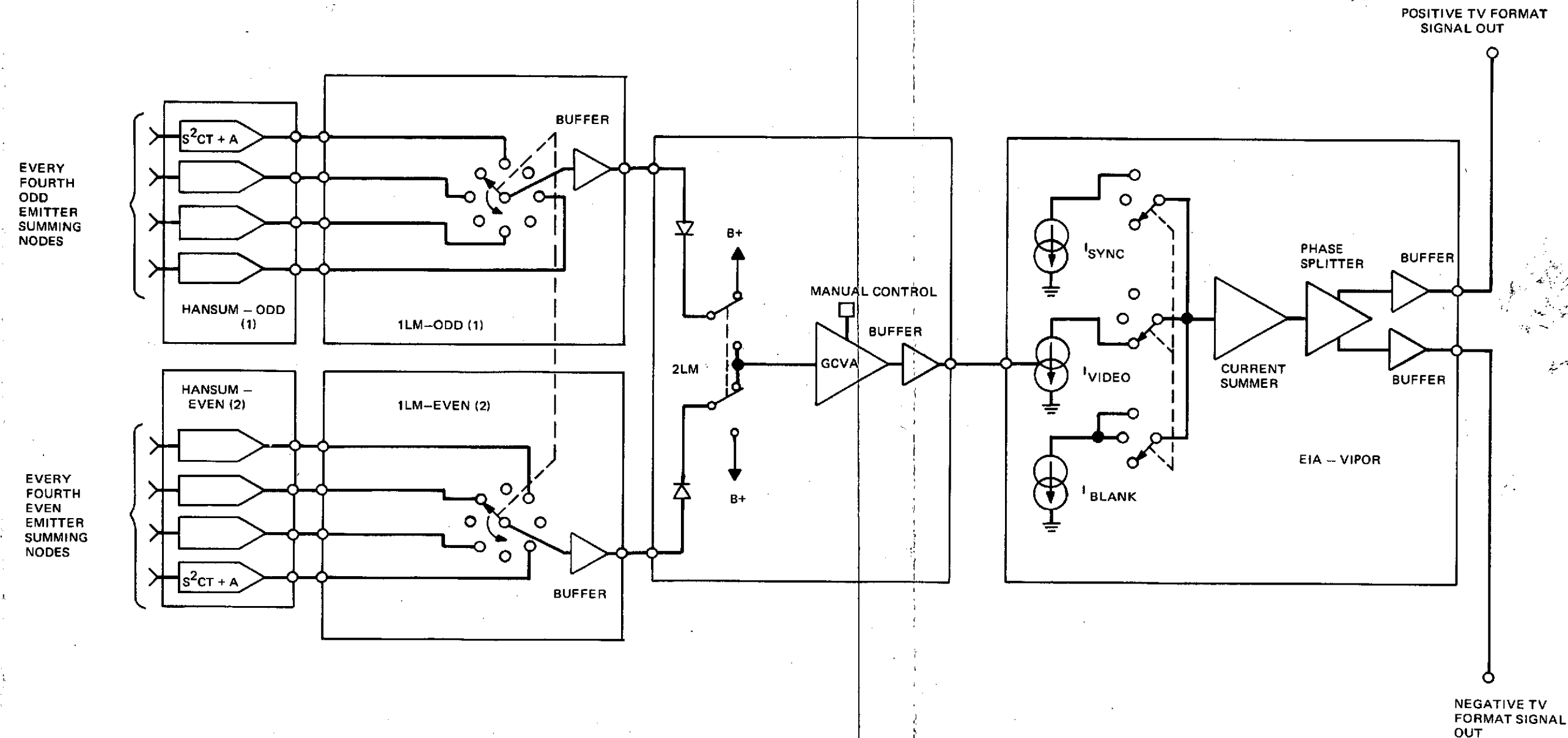
Figure 5-23. Idealized Timing Interrelationships for Video Signals
Processed Through "45" PICTURE System Electronics

72-0581-V-21

5-49

Figure 5-24. Basic Function Diagram of Analog Signal Chain
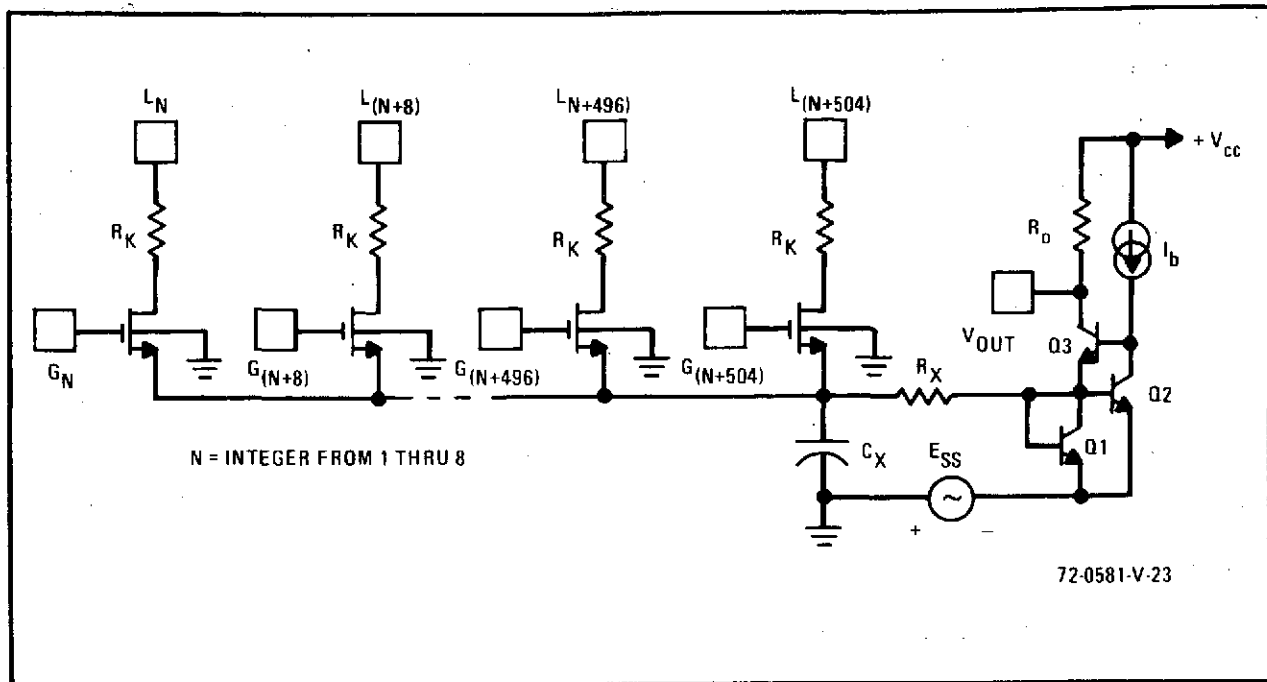in 400-x-500 Element Integrated Array Camera

72-0581-V-22

Figure 5-25.   One-of-Eight Solid-State Current Transformer Summed
Signal Commutation Channels in PICTURE "45" Camera

A negative polarity offset voltage E_{ss} equal in magnitude to one diode
drop, is applied to the low lead return point of Q1 and Q2 in the circuit so
that the input point potential at their bases will be maintained at zero rather
than $+V_{be}$ volts relative to ground.   This assures that even the lowest of
millivolt signal levels found at the array access lines will be coupled linearly
through the commutating MOS-FET's to the input and thence to the output of
the S^2CT stage without suffering undue losses or excessive charge pumping
from the FET source-substrate junctions.   Control of the static dc level at
the output of the summer is then facilitated through a slow response (low
bandwidth) feedback loop from the output of a follow-up boost amplifier to
the devices comprising the bias current source I_b.

Serial multiplexing operations carried out in both subsequent levels of
signal processing to combine the parallel time-shared video channels back
into a single channel are executed much in the fashion of a shunt ac coupled

clamping chopper, as illustrated in figure 5-26. One of the primary require-
ments for this chopping scheme to function properly is that the shunting
impedance Z_c supplied by the parallel connected capacitor, C_p, at the lowest
signal frequency of interest must be much less than the output segment, R_o,
of the series coupling resistance when the channel is not being sampled; or,
simply, that the inequality

$$Z_c = \frac{1}{\omega_{min} C_p} = \frac{0.1592}{f_{min} C_p} \ll R_o$$

must be satisfied. With f_{min} taken as the horizontal TV line rate of 15.75
kHz and R_o assumed to be 500 ohms, the value of the capacitor used should
accordingly be

$$C_p \gg \frac{0.1592}{f_{min} R_o} = \left(\frac{0.1592}{15.75 \times 0.5} \right) \times 10^{-6} = 0.02 \, \mu f$$

to avoid excessive baseline drift during nonsampled periods. Taking the
symbol "$\gg$" (normally read as much, much greater than) to mean "$\gtrsim 100$
times as large as" leads to a minimum C_p value of 2 μF. Confirmation of
this rough computation can be obtained experimentally by checking the differ-
ence in baseline drift for capacitors ranging in size from 0.47 to 47.0 μF.
The final value subsequently settled on in this manner as the best compromise
of all competing factors will usually be on the order of 22 μF, about 10 times
the approximate minimum size worked out above.

Once the image data bits from the sensor matrix have been fully processed
into a raw serial form signal, it remains only to alter the signal format
through the introduction of synchronization data before passing the composite
video on through the interface transmission channel to the final intelligence
consumption point. If an image reproduction display monitor intended for
human viewing is employed, the most common video format will be the
EIA standard for commercial television. It is that type of composite
output that is generated by the video processor included in the functional
diagram of figure 5-24. In this particular case, the design principle is
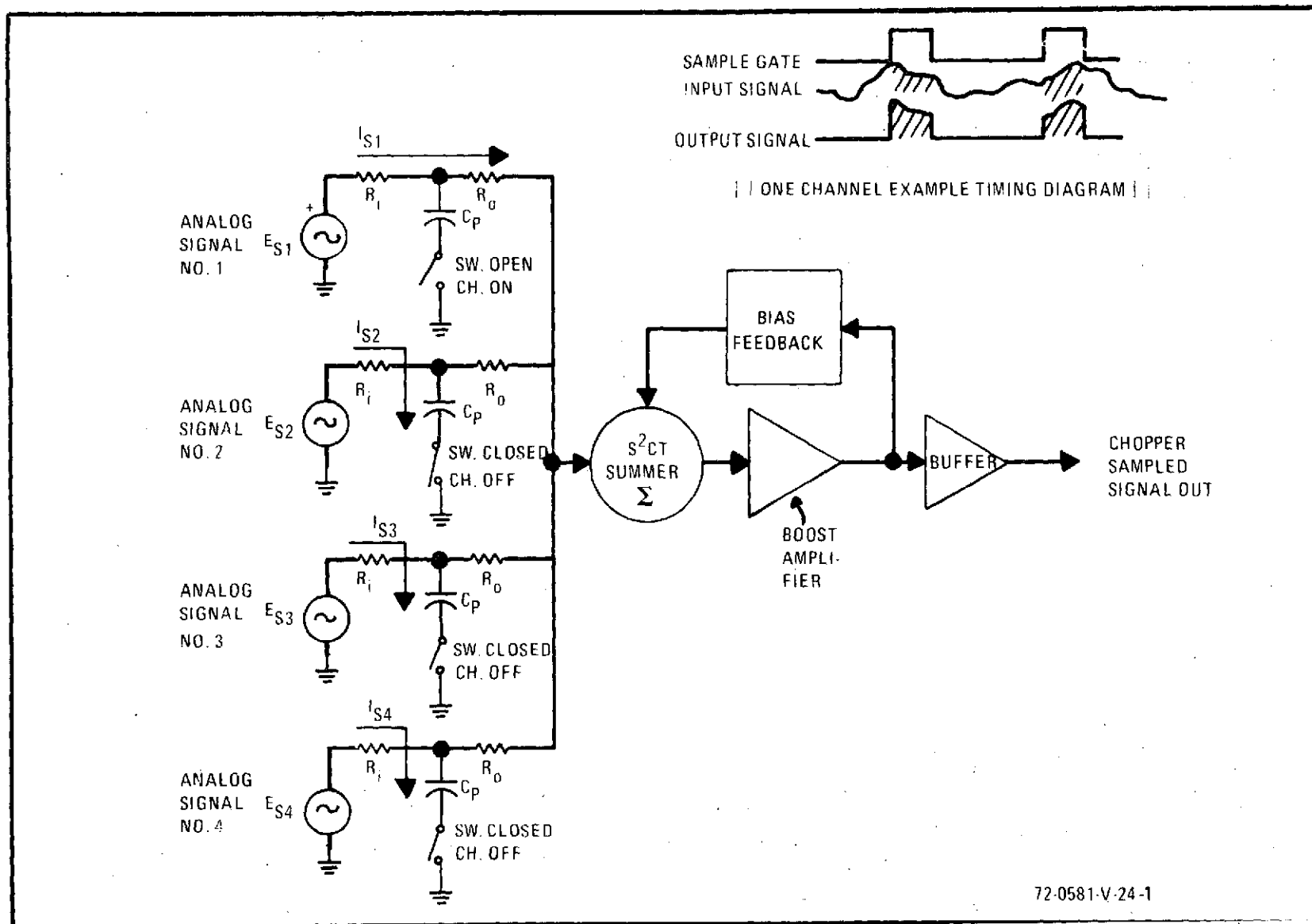based on the use of gated current sources.

SAMPLE GATE

INPUT SIGNAL

OUTPUT SIGNAL

| ONE CHANNEL EXAMPLE TIMING DIAGRAM |

I_{S1}

R_i R_0

C_P

ANALOG
SIGNAL E_{S1}
NO. 1

SW. OPEN
CH. ON

BIAS
FEEDBACK

I_{S2}

R_i R_0

C_P

ANALOG
SIGNAL E_{S2}
NO. 2

SW. CLOSED
CH. OFF

S^2CT
SUMMER
Σ

BUFFER

CHOPPER
SAMPLED
SIGNAL OUT

BOOST
AMPLI-
FIER

I_{S3}

R_i R_0

C_P

ANALOG
SIGNAL E_{S3}
NO. 3

SW. CLOSED
CH. OFF

I_{S4}

R_i R_0

C_P

ANALOG
SIGNAL E_{S4}
NO. 4

SW. CLOSED
CH. OFF

72-0581-V-24-1

5-55

Figure 5-26.   Four-Channel Analog Sampling Processor Using
Parallel Capacitively Clamped Chopping

During the element sequencing line time when scan converted image data is output from the array, the video current source (I_{video}) — controlled by the raw serial form analog signal input — is fed directly to the system output. During the interline and interfield times, this source is disabled and a fixed amplitude blanking current source (I_{blank}) — controlled by a binary mixed blanking pulse input — is substituted in its place. On top of the blank level is then superimposed the various horizontal sync and vertical serration and equalization pulses needed to control the display monitor sweep generators. This operation is accomplished by composite synchronization pulse input gating of the sync current source (I_{sync}). Obviously there are many diverse ways of implementing a circuit capable of combining the analog and digital portions of a composite video signal. What is believed to be one of the most simple and novel designs available anywhere, based on the gated current source concept, is revealed in figure 5-27.

The uniqueness of this circuit lies in the fact that it calls for only one type of active device and only two values of resistance, will handle input video signals having a dc offset of as much as 5 volts, can have its blank and sync gating pulses supplied from any type of positive polarity logic with swings of up to 30 volts, will operate from supplies of from +4 to +30 volts, and consumes only 2 milliwatts at 4 volts with its current drain increasing by 85 μA/volt for higher supply levels. It contains its own built-in regulator section, consisting of transistors Q15 through Q19, to facilitate such wide range operation and stability. An S^2CT network, formed by Q12, 13, and 14, is employed as the primary summer portion of the circuit to assure excellent transfer linearity. Allowance for dc coupling of analog input video not referenced to ground to its input is made by clamping the input (via Q1) during the blank periods and injecting a trimmable counteractive current level by way of Q7. Transistors Q3 through Q6 form a current steered AND gate driver for Q7. Sync signals are introduced via transistors Q8 through Q11, which constitute a DTL style gated current source.
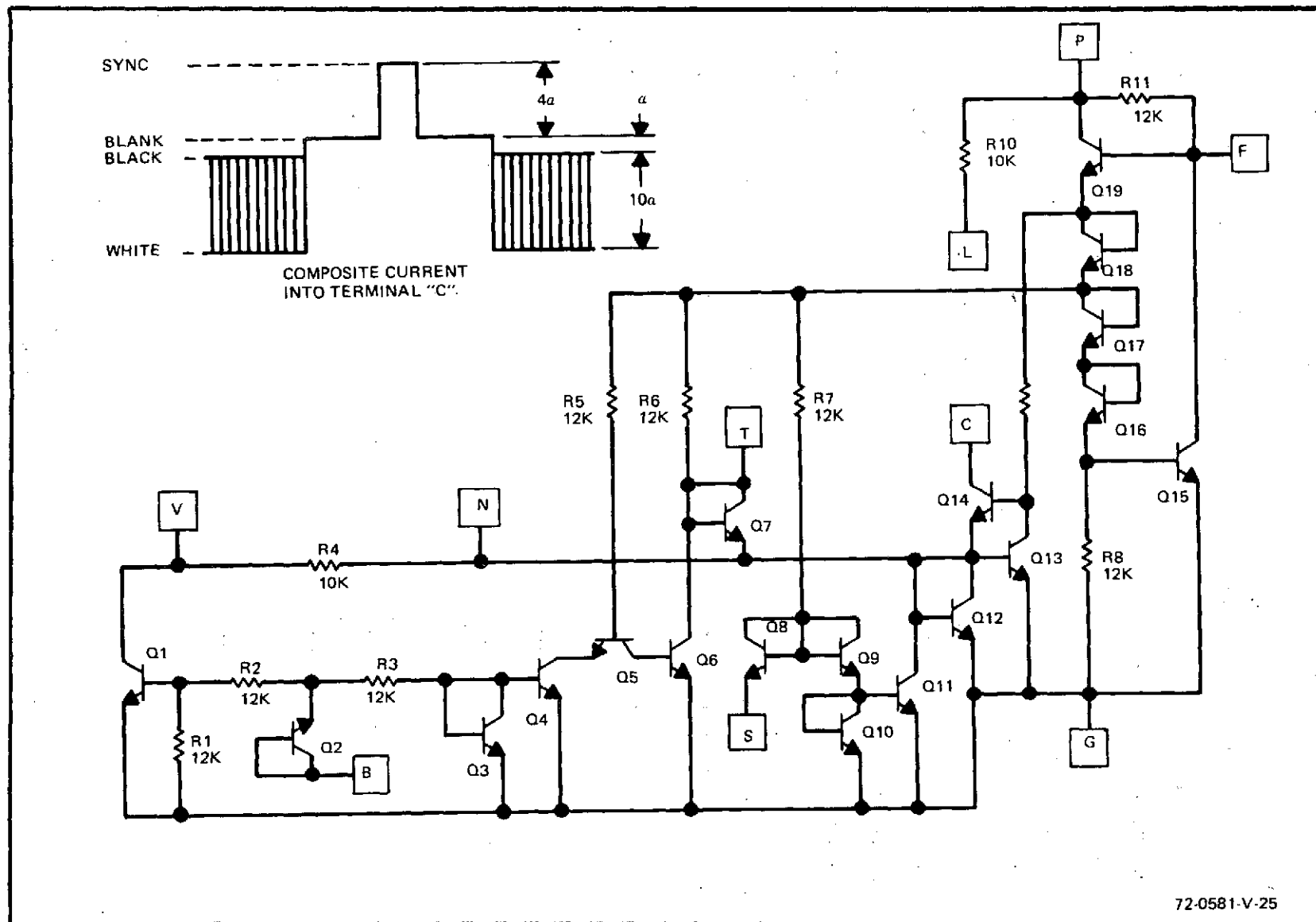
Figure 5-27. Low Power LSI Configured EIA TV Format Video Generator

72-0581-V-25

The primary design constraint imposed to arrive at this type of circuit configuration was that the final unit had to be ameanable to easy monolithic integration. Its performance capabilities have been demonstrated in both a discrete breadboard implementation and an intermediary quasi-monolithic breadboard using two general purpose compatible family chips packaged in a 0.5-inch-square 10-pin flat pack. Final Generation of masks for producing the circuit in fully monolithic form is being held in abeyance until the breadth of the demand for such a structure is more firmly established.

To supply adequate drive to power the coaxial cables used at the output of the camera and which exist internally between the first and second multiplexers, complementary push-pull stages like that shown in figure 5-28 have been incorporated. The basics of this driver are well known and there can be found a number of slightly modified versions of it in common use throughout industry. As configured here, a duo set of similarly characterized npn and pnp matched pair transistors is used to form the push-pull power
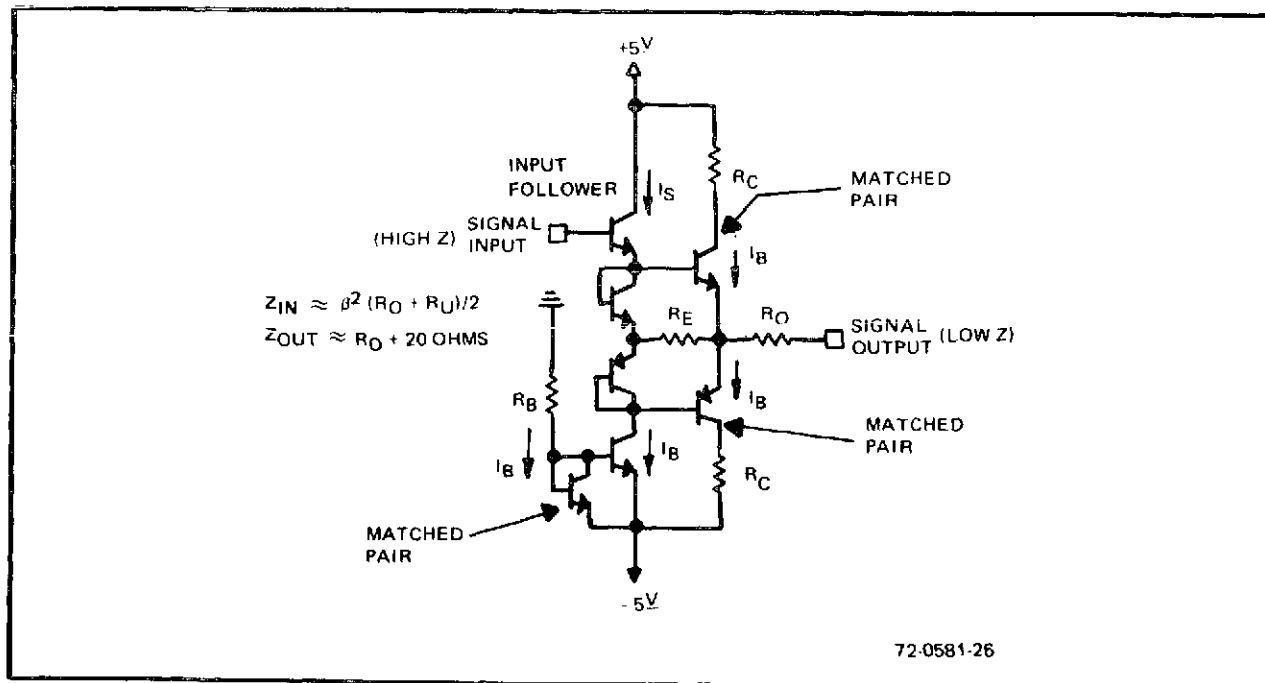

Figure 5-28. High Performance Complementary
Push-Pull Power Line Driver

5-58

output section. Use of matched pairs instead of diode-transistor combinations assures minimally powered linear operation with no cross-over distortions. Input drive is supplied through a simple emitter-follower while the static bias current level is set by a current source pair fed from a fixed resistor. Collector resistors are included in the output stage supply lines to prevent accidental shorting of the output from causing excessive current drain and subsequent device burn-out. Since the inherent output impedance of the stage is only about 20 ohms, it is possible to include a resistor in series with the output line to match the surge impedance of any coax being driven.

Although none of the MIC systems developed on the present program have incorporated any form of AGC, inclusion of this feature in recent experimental R&D imagers has demonstrated an ability to shift the system response dynamic range midpoint by approximately 3 dB to handle different average scene illumination conditions. Refinements of the technique to tailor the shape of the gain-reduction transfer relationship are expected to facilitate attaining an enhanced control range of at least 6 dB, and possibly 10 dB with some of the more advanced signal processing innovations (such as DUST signal acquisition) which have reduced noise levels.

The type of setup that could be applied to a high resolution system employing higher order time-shared signal processing is depicted in figure 5-29. In a functionally tiered design like this, it is best to regard each succeeding level of processing as a separate, self-contained subsystem and incorporate an AGC feedback loop around each channel amp within that level. While this will necessitate matching of the AGC characteristics for paralleled channels, trimming of the per-channel gain parameters was already a prerequisite, so very little additional work is entailed in producing the aggregate circuitry. Furthermore, the extreme difficulty of matching, tailoring, and fractionally apportioning the response to a single master feedback loop is avoided. The master override shown in figure 5-29 is included to indicate the possibility of manually disabling the automatic functions and establishing fixed gains for the various stages.
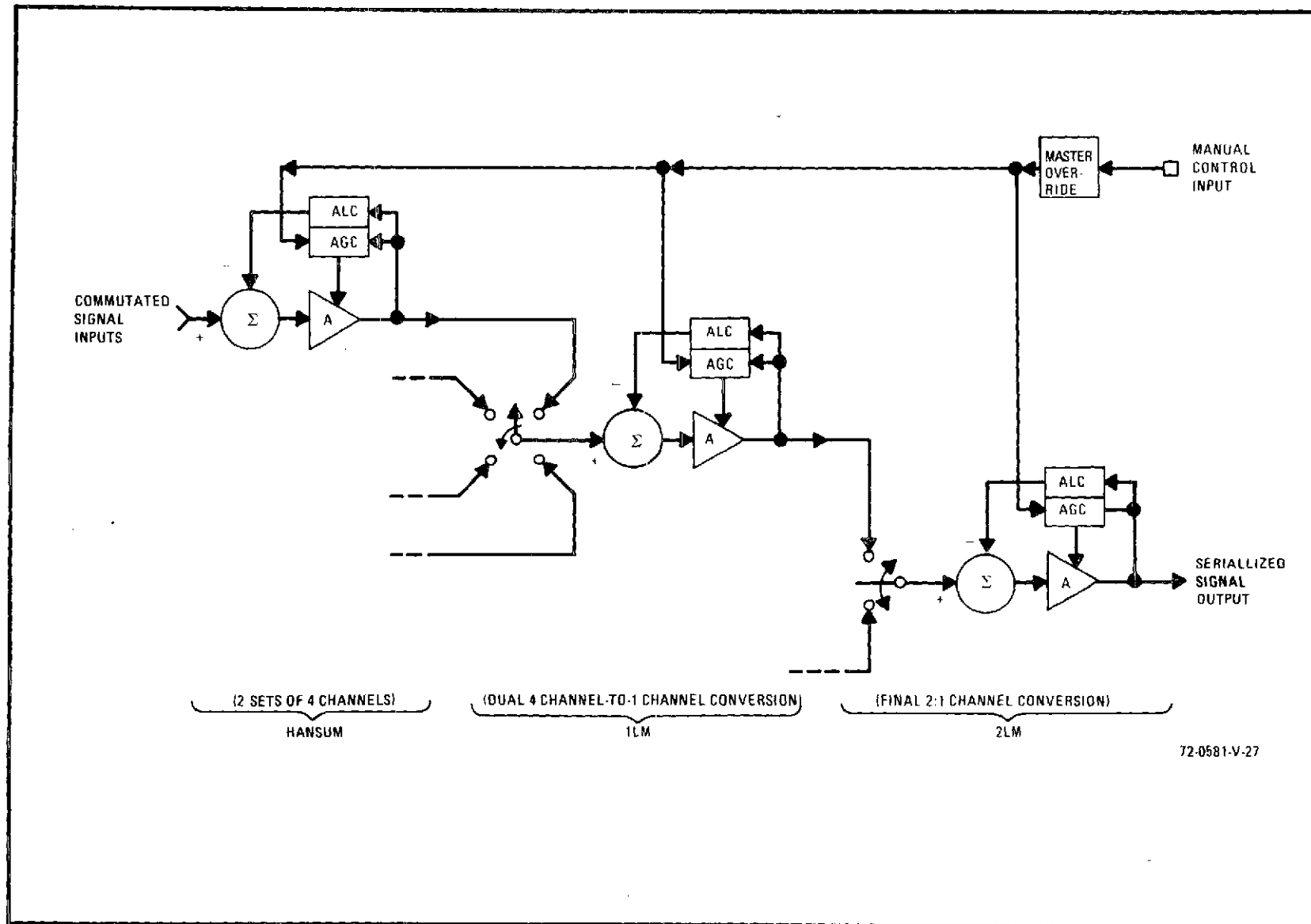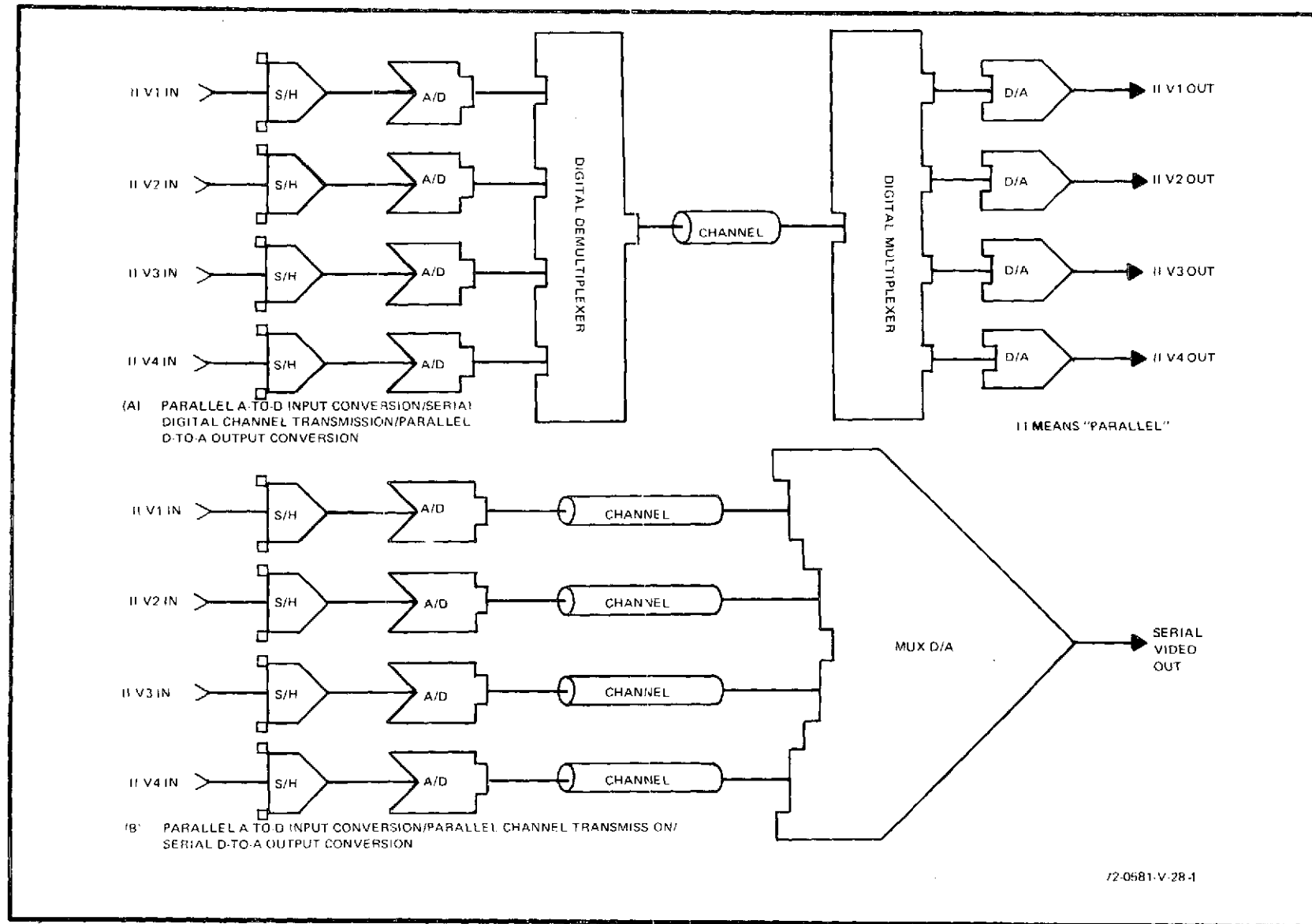
Figure 5-29.   Time-Shared Analog Signal Processor Chain With
Self-Looping Per-Stage Automatic Gain Control

As suggested earlier, it is possible to employ digital-to-analog conversion techniques in conjunction with any of the foregoing processing to improve the effective signal-to-noise ratio whenever the information must pass through a noisy channel environment. Details of the input and output conversions used in any arrangement of this type can vary so widely with the various system parameters affected and the form of conversion electronics employed that an in-depth review of the alternative becomes well beyond the scope of this report. A cursory examination of the fundamental philosophy can be made from the two sample conversion schemes depicted in figure 5-30. The first, part a, assumes parallel channels of analog data (such as have been discussed for the 400-x-500 imager) are supplied at the input. Further, it is assumed that the output signals utilized at the intelligence consumption point— following A/D conversion, channel transmission, and D/A conversion— are also in parallel analog form. Use of a single channel carrier is facilitated by incorporating digital multiplexing and demultiplexing operations at the transmission and reception ends, respectively.

In part b of this figure is shown an alternate arrangement calling for parallel input signal conversion and data transmission followed by parallel-to-serial multiplexed A/D conversion into a single output analog signal line. Quite obviously there are a number of further modifications that can be made to either of these subsystem organizations. In some cases there may be an advantage to adopting the parallel digital channel approach, while in others there may be an overriding requirement why a single channel should be employed. The A/D conversions needed can be accomplished by any one of a number of techniques, included among which are ramp comparison, successive approximation, totally parallel, etc. As with other portions of the signal processing circuitry in an integrated array image converter, ultimate selection of specific electronics rests with the systems designer who must be cognizant of all aspects of the particular application.

(A) PARALLEL A-TO-D INPUT CONVERSION/SERIAL DIGITAL CHANNEL TRANSMISSION/PARALLEL D-TO-A OUTPUT CONVERSION

II MEANS "PARALLEL"

(B) PARALLEL A-TO-D INPUT CONVERSION/PARALLEL CHANNEL TRANSMISSION/ SERIAL D-TO-A OUTPUT CONVERSION

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Figure 5-30. Block Diagram Examples of Digital Conversion of Analog Data

5.4 INFORMATION DISPLAY

There are several types of image monitors which can be deployed with an integrated camera to facilitate remote viewing of the pickup end scene. All monitors currently in common usage for outputting half-tone gray scale images employ electron-beam flying spot scanned cathode-ray tubes having Z-axis modulation and either electrostatic or electromagnetic beam deflection. Recent experimental developments, which are presently still in the laboratory phenomenon classification, have demonstrated the feasibility of flat-screen, nonhigh vacuum displays using X-Y coordinate current or electrostatic field excitation of special film materials. For now, though, we will be concerned only with CRT types which have seen frequent use with imaging systems.

As indicated, intensity modulated CRT's used for image reproduction can be broken down into two basic classifications according to the type of beam deflection they employ; i.e., either electrostatic or electromagnetic. Under electrostatic we have

      a. Z-axis modulated laboratory oscilloscopes

      b. Z-axis modulated trace-storage displays

      c. General purpose X-Y-Z data monitors

with the latter also occurring in electromagnetic deflection form. This latter type includes

      a. General purpose X-Y-Z data monitors

      b. Commercial TV studio displays

      c. Home television receivers.

The majority of early system applications with low resolution exploratory model integrated array cameras used electrostatic style monitors due to their greater ease of diversified and variable parameter operation.

On the current program, Z-axis modulated electrostatic deflection laboratory oscilloscopes having a P2 phosphor were deployed with

      a. Original first generation 50-x-50 camera

b. Second generation 100-x-128 laboratory test vehicle

c. Fully packaged portable demonstration 100 x 128 camera

d. Third generation 200-x-256 expanded test vehicle.

For the fourth generation of 400-x-500 element converters, though, image reproduction has been facilitated through the use of (1) an electrostatic general purpose monitor for the wafer test stand, and (2) electromagnetic home TV receivers for the LSHI packaged camera; with the latter deployment made practical by the adoption of the EIA standard television format for scanning. All prior systems employed a more generalized scanning format and contained D/A staircase sweep generators to drive the deflection plates of their electrostatic CRT displays.

Reproduction capabilities of the monitors applied to the respective imagers evolved on this program have been adequate to allow the displaying of images having the resolution and dynamic range inherent to the camera system. Typical display monitor photos for these systems are shown in figure 5-31, with parts (a) through (d) being obtained, respectively, from the 50-x-50, 100-x-128, 200-x-256, and 400-x-500 element MIC's. Progressing through this series, the steady increase in resolution that has been achieved over the course of the program will be readily apparent. Also seen in taking the first three generations in order, however, is a marked increase in the vertically oriented line pattern noise that detracts from the cosmetic quality of the output images captured by solid-state array cameras. In the most recent 200,000 element converter, whose typical unenhanced image is presented in figure 5-31(d), nearly all the fixed pattern that was attributable to the scanning electronics in former system designs has been made negligible by advanced scanning and signal processing techniques.
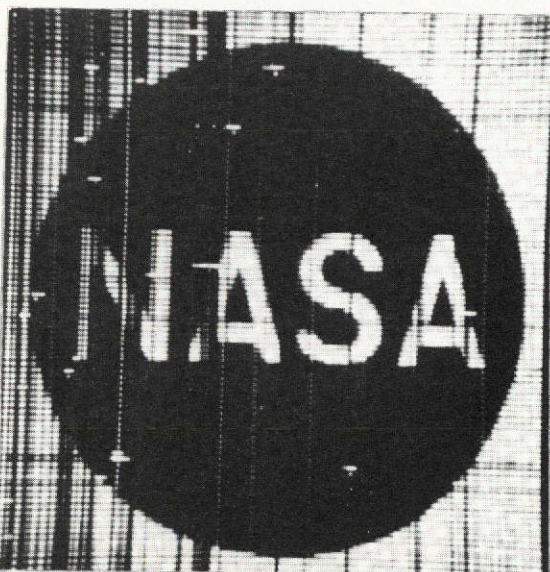
Defects which remain in the images produced by the PICTURE "45" camera, including the scattered line pattern groups that are in evidence, are almost solely attributable to problems within the sensor array. Vertically oriented low or nonresponsive lines or parts of lines are caused by open
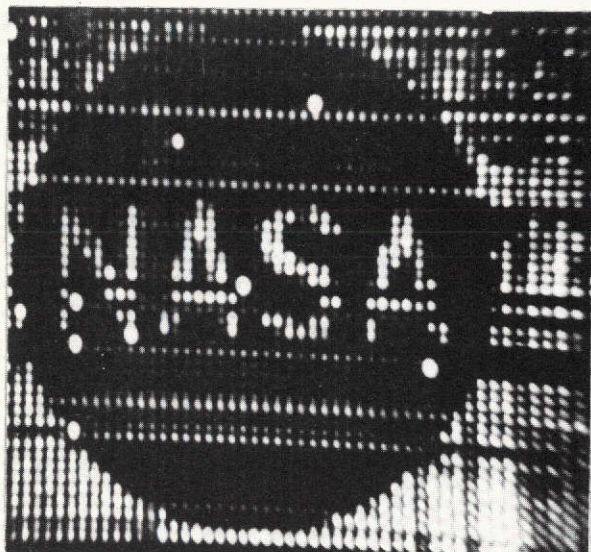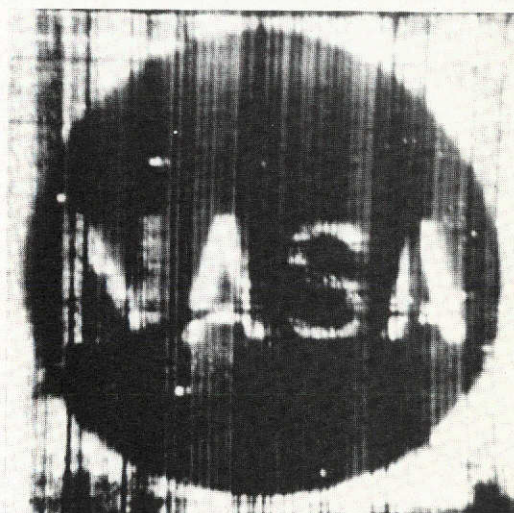
(A)
50 X 50 CAMERA IMAGE
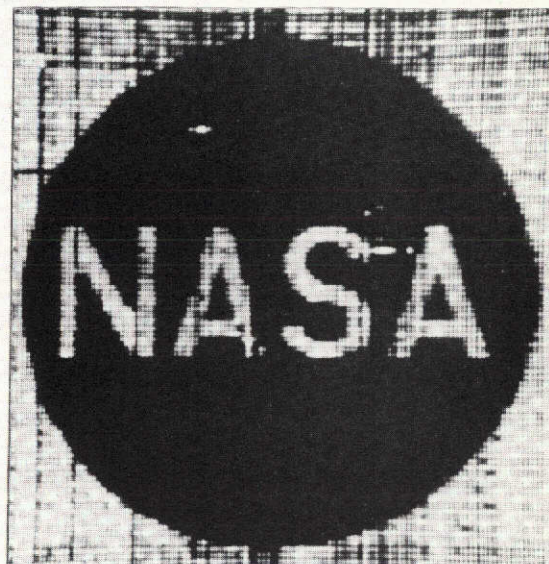
(B)
100 X 128 CAMERA IMAGE

(C)
200 X 256 CAMERA IMAGE

(D)
400 X 500 CAMERA IMAGE

72-0581-8H-29

Figure 5-31. Representative Display Monitor Photos of
Output Images from Successive Generations of the
Image Converter of Radical Design

or else excessively loaded (by virtue of shorts) column access lines to the array. The terraced sequence of dead areas appearing in the lower right-hand center portion of the display over the letter "s" are the result of step-and-repeat mask alignment errors introduced during fabrication processing of the array. Finally, the grainy (salt and pepper) appearance of nearly the complete left half of the image, which results in a loss of effective resolution, is a manifestation of extensive but randomly distributed poor (open) emitter contacts. A complete listing of these and other types of failures that can occur in phototransistor monoliths is presented in figure 5-32, which includes schematic representations of such faults in the array. Supplemental procedures for overcoming, cancelling, or circumventing certain types of display anomalies are covered more fully in paragraph 5.5.

Emphasis of all work on the current program has been on half-tone gray scale imaging, and accordingly has called for the use of information utilization units capable of outputting for human consumption a visual photoconverted image from the camera video. In different applicational situations there would not necessarily be a CRT display monitor used. If, for example, the camera is viewing a scene containing only high contrast black-white regions (such as a map or printed text), then a two-level binary form of go/no-go display structure could be employed, or the information could be sent to a computer for interfacing with other types of data. Applications calling for these types of display formats include OCR (optical character recognition) and TMR (tactical map reader) systems. A further example of a novel information usage unit that has received much attention recently is the tactile (sense of touch) stimulator belt being experimented with to give persons totally blind some simile of sight. This is an exciting field which may soon see greatly expanded application of integrated array imagers.

CROSS SECTION VIEW
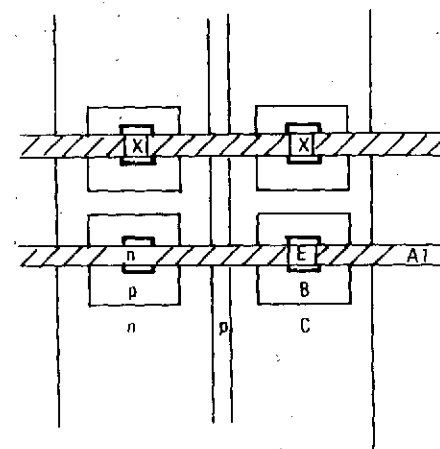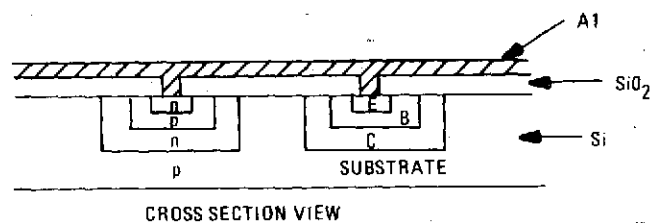
PLAN LAYOUT VIEW
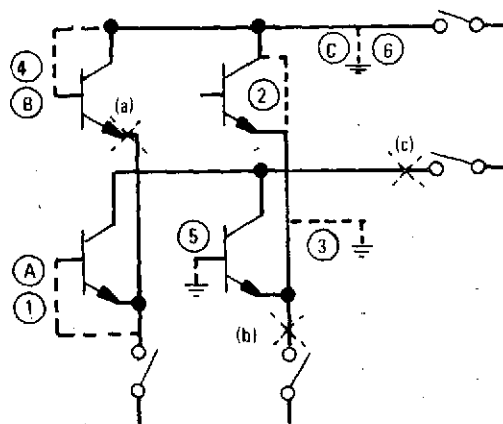
CATASTROPHIC DEFECTS POSSIBLE

1	EMITTER-BASE	
2	EMITTER-COLLECTOR	
3	EMITTER-SUBSTRATE	SHORTS
4	BASE-COLLECTOR	
5	BASE-SUBSTRATE	
6	COLLECTOR-SUBSTRATE	
A	EMITTER-BASE	LEAKY
B	BASE-COLLECTOR	JUNCTIONS
C	COLLECTOR-SUBSTRATE	
(a)	EMITTER CONTACT	
(b)	EMITTER BUS LINE	OPENS
(c)	COLLECTOR BUS LINE	

72-0581-VB-30-1

Figure 5-32. Possible Failures in Phototransistor Monoliths

5.5 SIGNAL CONDITIONING

As the result of a fairly extensive study program into the mechanics of display aberrations which appear in the output images from solid-state camera system there have been certain major improvements realized while the feasibility of a number of other techniques has been demonstrated. In this paragraph we will examine some of the more significant developments in the area of image enhancement.

To begin this discussion, the types of display faults being attacked should be reviewed first and the point of their origin ascertained. Figure 5-32, shown in the previous paragraph, gives an extensive breakdown of the type failures that can occur within or at the terminals of a phototransistor monolith. These are summarized in table 5-2 along with other problems that can occur at various other points in an overall image capture/transfer/utilization system configured in the general manner depicted in figure 5-33. As indicated, each point in the system has certain potential problems which can degrade aggregate performance. A correlation can be made between these problems and the visual effect they will have on the output image from a review of table 5-3.

Most concerted effort and, correspondingly, most success in improvement has been for pattern noise abberations which appear as bright or dark spots and lines. In the area of regional shading it has been concluded that maintenance of processing uniformity to secure arrays with minimal parameter variations across their surface dimensions is the only truly effective means of instituting worthwhile improvements. Little that is more than marginally effective can be done after-the-fact in the surrounding system electronics to smooth out regional shadings. Reductions in the losses to effective system dynamic range have also proven practical. However, while improvements have been achieved with regard to each of the visual appearance areas, many of the contributing sources remain and further studies have been initiated on company internal programs.

5-68

TABLE 5-2

GENERAL DESCRIPTION OF IMAGE DEGRADING FACTORS
IN EACH SECTION OF IMAGING SYSTEM

Point In System	Type Of Potential Problems
Sensor Array	Catastrophic sensor defects Elemental gain variations Leakage current differences
Acquisition Circuitry	Commutation offset levels Line sequencing transients Signal throughput nonlinearity
Processing Circuitry	Signal line multiplexing transients Signal line amplification imbalances
Display Monitor	CRT conversion nonlinearities CRT dynamic range limitations
System Timing	Counter/decoder delay irregularities
Address Circuitry	Row address driver inconsistencies
Raster Generation	Horz and/or vert sweep nonlinearities
Transmission Channel	Shorted or open coaxial cable

TABLE 5-3

DESCRIPTION OF ABERRATIONS IN OUTPUT OF TYPICAL
SOLID-STATE IMAGING SYSTEM

| Visual Appearance	Contributing Sources
Bright or dark spots	Catastrophic sensor defects Junction breakdown leakage differences
Bright or dark lines	Catastrophic sensor defects Elemental gain variations Commutation offset levels Switching transients Timing delay irregularities Signal line gain differences Raster scan nonlinearities
Regional shading	Elemental gain variations Signal line gain differences
Gray shade loss	Sensor-to-monitor gamma mismatching Monitor CRT dynamic range limitations Acquisition circuitry nonlinearities
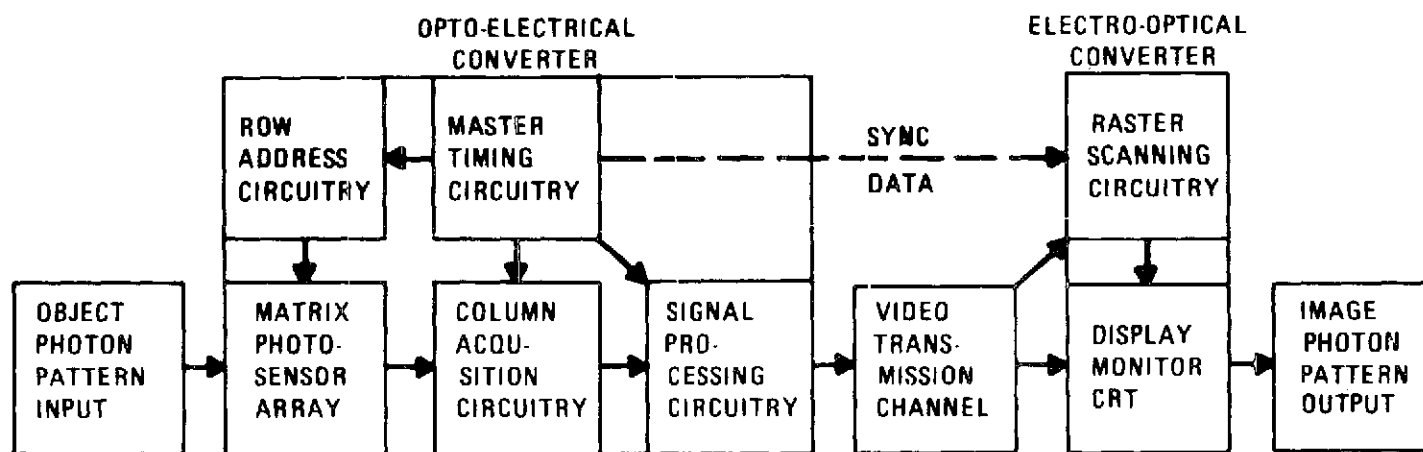
Figure 5-33. General Block Diagram of Imaging System

The approaches that have been taken to the problem of image enhancement cover a wide spectrum of techniques and philosophies: some highly effective, others practically useless. Table 5-4 enumerates the principal techniques that have been applied in the cited problem areas. All except the last, as stated previously, have resulted in notable improvements in image display quality. Considering this latter problem first in our discussion here, figure 5-34 points out the basic features of the principle attempted and the point in the system where it was applied. The idea is quite simple and is a direct extension of arrangements that have been used quite successfully with line array converters. It merely entails the introduction of passive divider networks in series with each column access line where the array data is extracted. This is intended to provide a means of trimming the parameters of the column and effect an adjustment in the amplitude of succeeding signal outputs.

TABLE 5-4

APPROACHES TAKEN TO IMAGE ENHANCEMENT

| Problem Area	Improvement Technique Employed
Gray shade loss from gamma mismatching and monitor limitations	Introduction of nonlinear amplifier into monitor with characteristics tailored to produce gamma matching
All forms of fixed background noise arising from array defects and readout sequencing anomalies	Application of a video disc recorder to memorize dark signal background pattern and then subtract it from later video during normal imaging Use of special overamplitude video pulse feedforward blanker electronics to cancel bright spots
Portion of vertical line pattern arising from commutation device offsets	Introduction of specialized subsystem into converter to memorize and null out row-repetitive offset levels
Portion of vertical line pattern arising from switching transients	Development of active and passive networks capable of cancelling spikes by complementary action
Regional shading across the array as result of elemental gain variations	Insertion of amplitude controlling trimmable parameters in each column access line of the sensor array
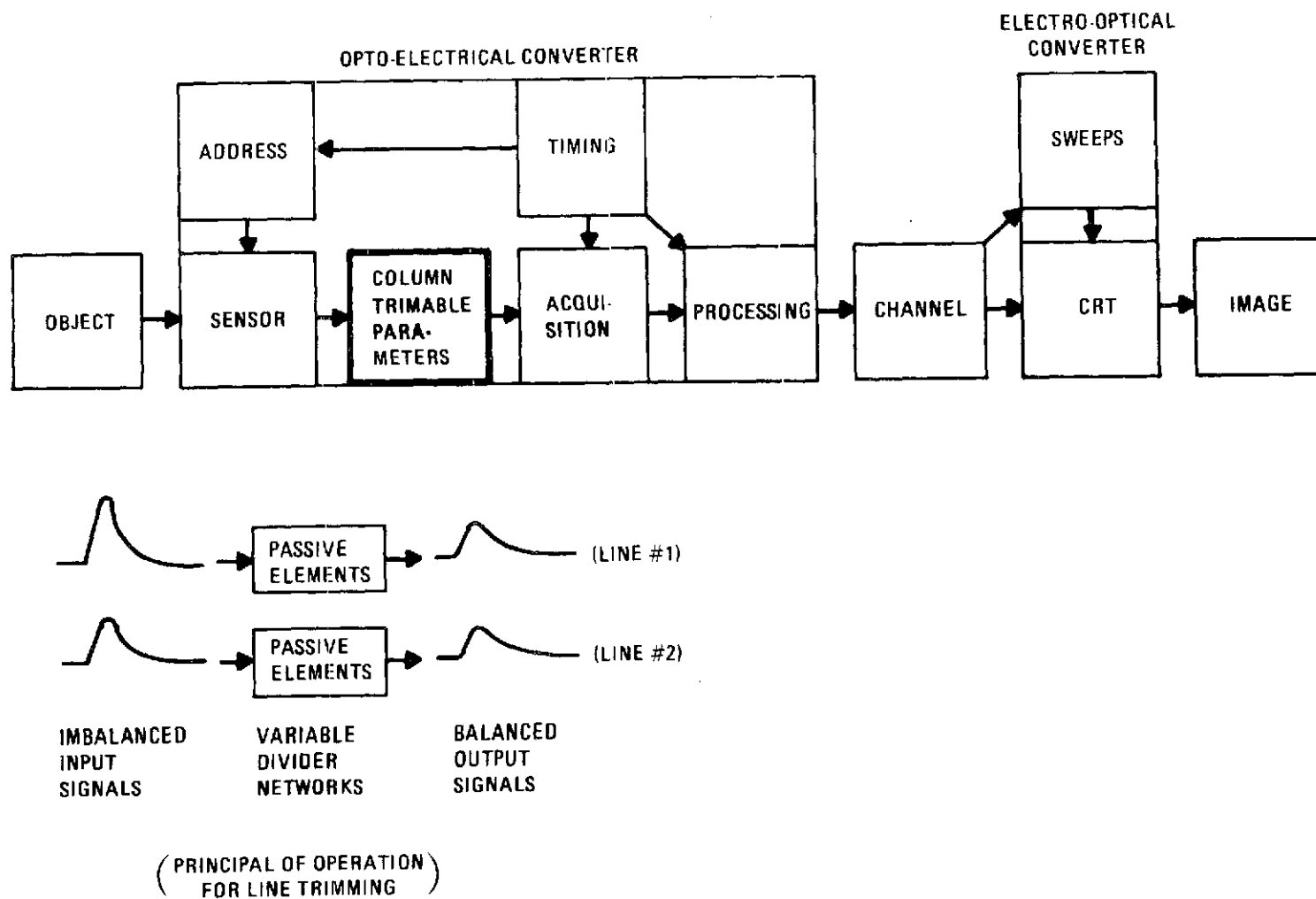
Figure 5-34. Imager Block Diagram With
Column Trimmable Parameters Inserted

72-0581-V-32

While the principle works well with simple one-dimensional linear sensor arrays, its effectiveness with two-dimensional matrices proves marginal due to the major difference in array parasitics loading the access lines and the fact that the shading ratios relative to their orthogonally oriented neighbors for all elements up a particular column line are not necessarily identical. This latter point is what completely negates the principle's usefullness with area coverage arrays. It was accordingly abandoned in favor of pressing for tighter processing controls during fabrication of the sensors.

Turning our attention next to switching transient noise which contributes to vertically oriented line patterns as a result of its columnarly organized commonality (having been originated by the FET commutation devices), it is found that the technique adopted in this case proved highly effective. In particular, by generating an opposing pattern of complementary transient spikes and summing them in at appropriate points in the system and at the correct amplitudes, around 20 dB of spike suppression has been realized. The fundamentals of this scheme and its point of application in an integrated imager are depicted in figure 5-35. Active as well as passive differentiating and amplitude control circuitry for generating and introducing the required complementary spikes has proven effective. Which type is applied in a particular situation depends on the relative amplitude needed and the impedance levels involved at both the driving and summing points.

Another highly effective development applied to solid-state array cameras to improve the appearance of their output displays is a feedforward over-amplitude video signal blanker designed to remove bright spots. A diagram of the resultant circuitry as it was implemented in the 100-x-128 packaged camera and the 200-x-256 expanded test vehicle imager is presented in figure 5-36. Here it will be seen that the output from the first video amp is a processor chain is applied to the inputs of both the second ampl and a level sensitive Schmitt trigger (or comparator). The outputs from this trigger are made to respond only to input pulses having an amplitude greater than some
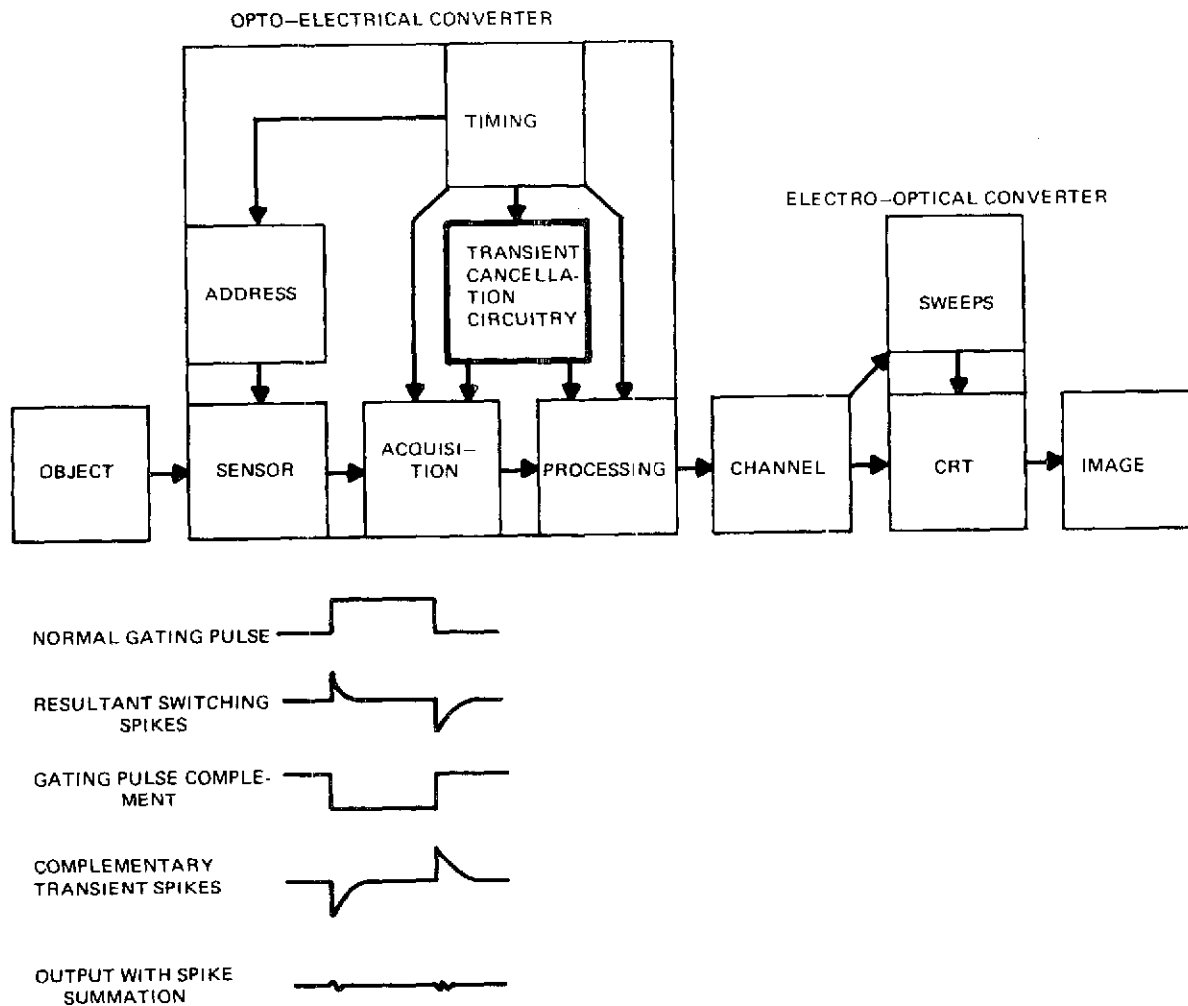
Figure 5-35. Imager Block Diagram with Transient
Cancellation Circuitry Added
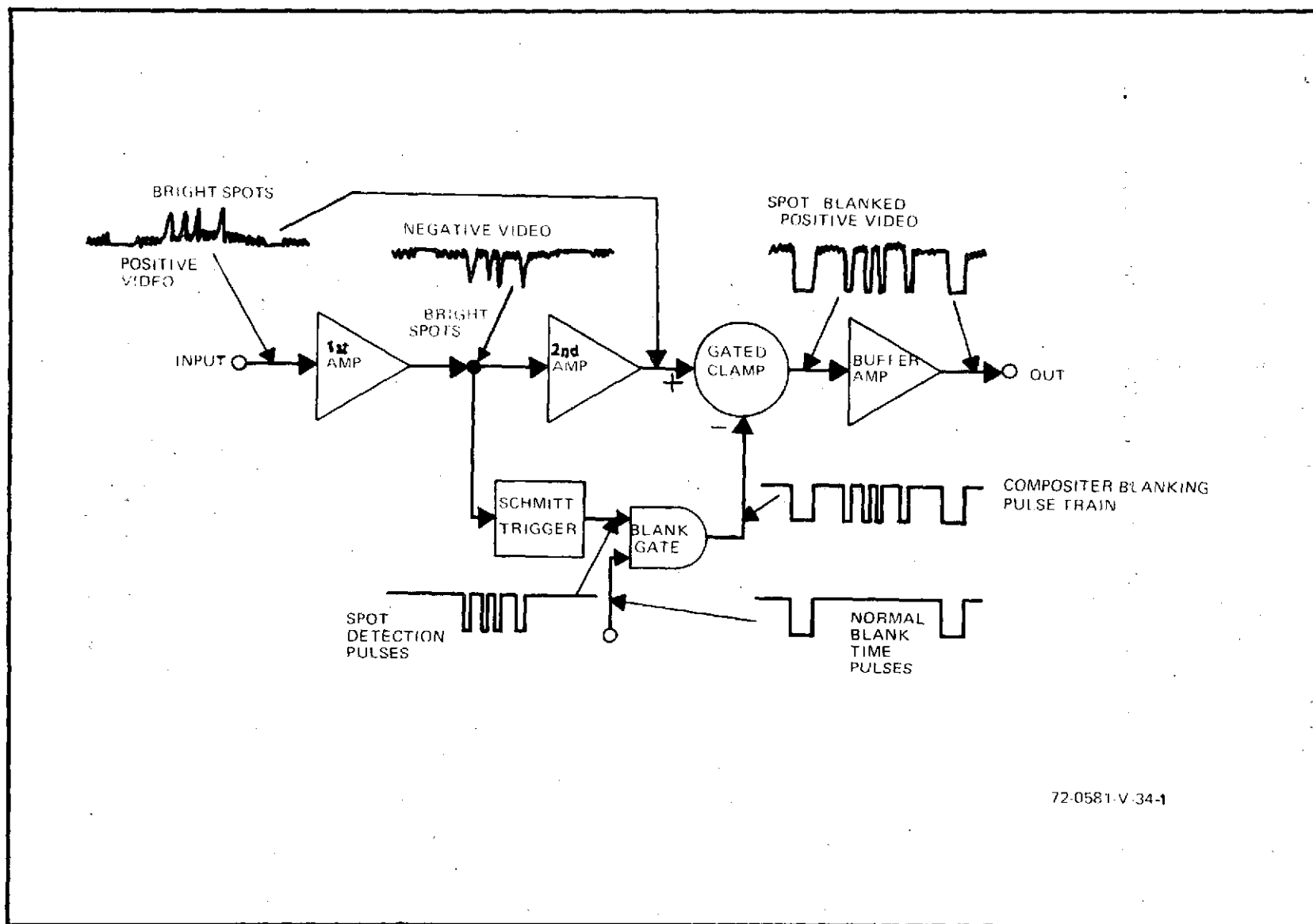
Figure 5-36.   Block Diagram of Overamplitude Bright Spot Blanker

preselected level. Time-positioned spot detection pulses thus obtained are then "fed forward" and combined with the normal interline blank pulses to effect clamped blanking of the second video amp output at those times when over-amplitude video pulses are present at the output of the first amp. In effect the circuit shoots holes in the raster wherever a bright spot normally exists and substitutes an aesthetically less objectionable black spot. The improvement in display appearance is readily seen in the monitor photos of figure 5-37 taken from the 200-x-256 element system.

Further dramatic enhancement of the cosmetic quality of image reproduction from integrated images can be obtained by introducing a specialized postconverter processor — in the form of a video disc recorder built by the Westinghouse Research and Development Labs — between the camera and monitor in the manner illustrated in figure 5-38. With this equipment in place, it is possible to memorize virtually all aspects of the detrimental fixed background noise and subsequently subtract it from the desired image video. The basic functions performed within the recorder in executing this task are also depicted in the above figure. A comparison of the before and after results of such a cancellation procedure carried out with the 200-x-256 system is made in the displayed image photos of figure 5-39. Part(a) of this figure shows the raw background pattern raster which is placed into memory on the disc. In part(b) is then shown the appearance of the cleaned-up raster obtained by subtracting out the background noise. The sequence of dark vertical lines which appear in the cancelled raster are caused by imperfect operation of the D/A converter which generates the horizontal sweep deflection staircase voltage. Regrettably, it was not known that the condition existed prior to running the series of tests with the disc recorder which produced these photos. Quite obviously, from any of the "before" images, the condition is all but totally masked by the heavy and dominant light and dark patterns that exist without subtraction.
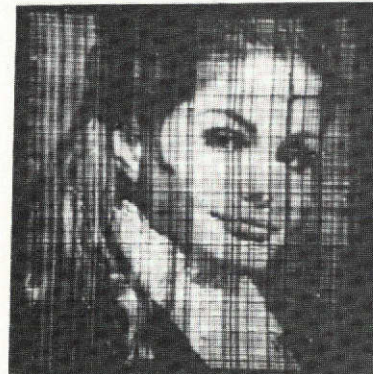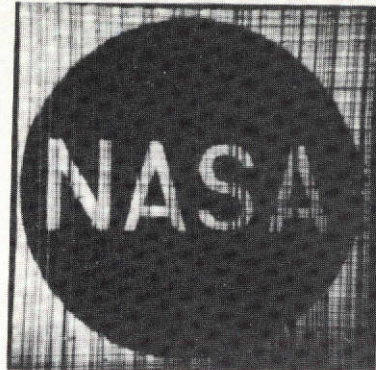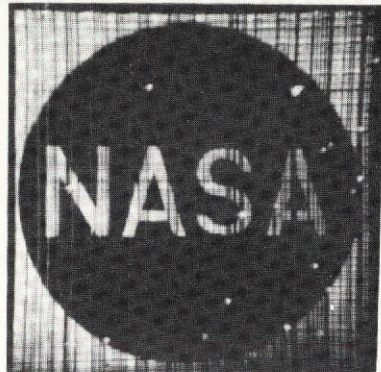
BEFORE IMAGES
WITH SHORTED ELEMENT
BRIGHT SPOTS PRESENT

AFTER IMAGES
WITH SHORTED ELEMENT
BRIGHT SPOTS BLANKED

72-0581-P-35

Figure 5-37. Effect of Bright Spot Blanking
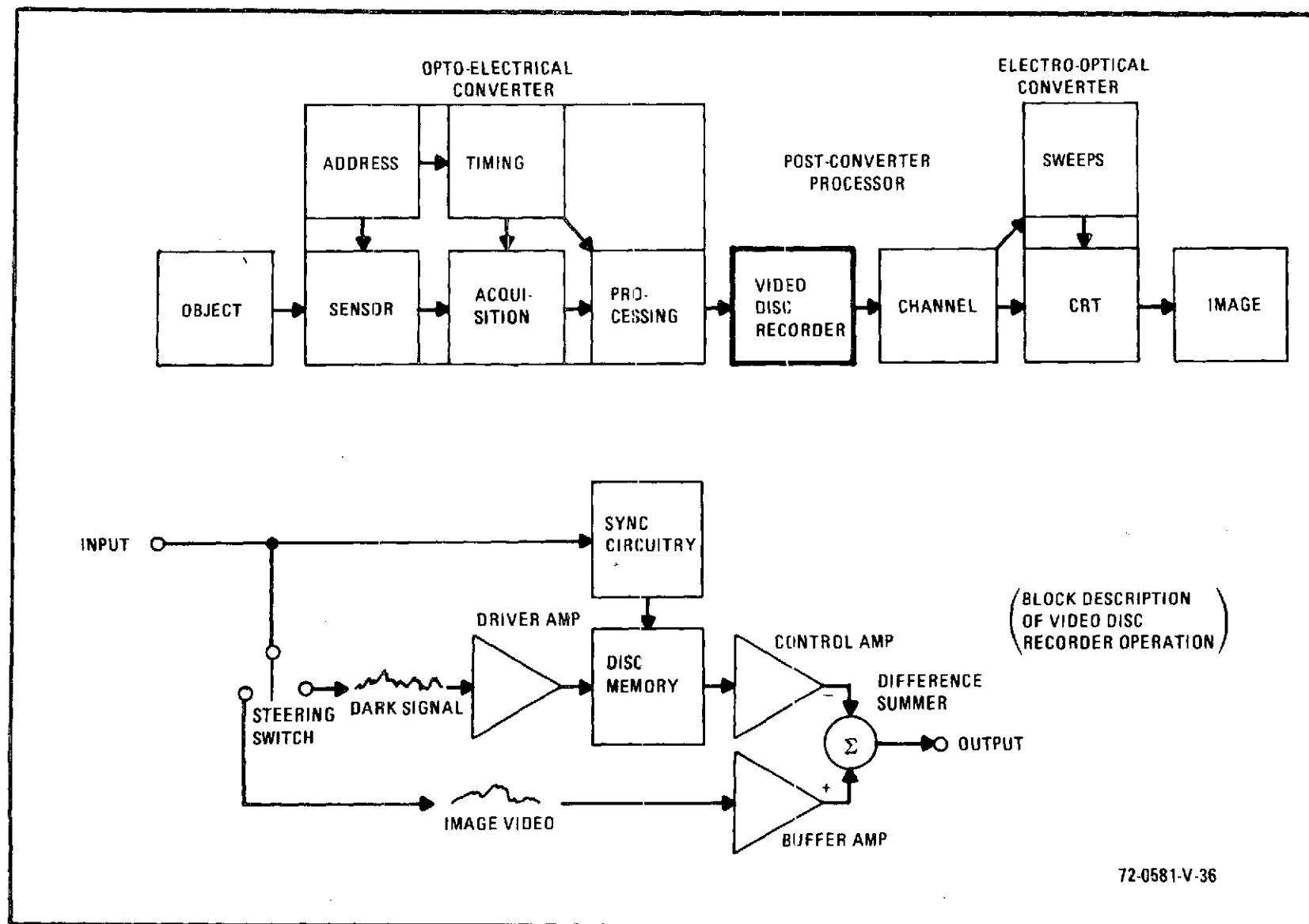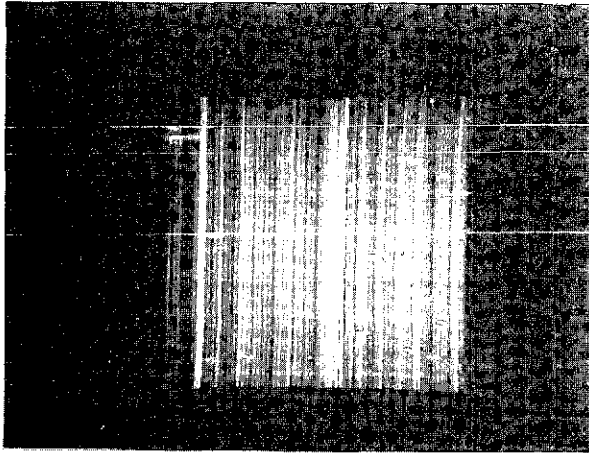on Image Appearance

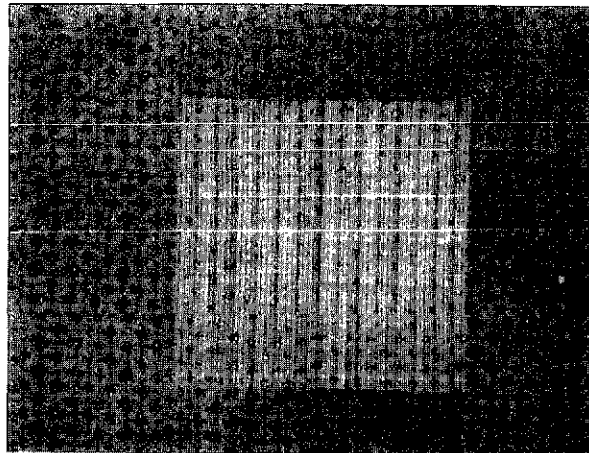Figure 5-38. Imager Block Diagram with Postconverter
Processing Supplied

The set of images in figure 5-39(c) and (d) illustrate the improvement in image quality realized for situations where two-tone black/white objects are viewed. While the enhanced performance can be seen here, it is even more dramatically illustrated in the multiple half-tone images of figure 5-39(e) and (f). Take particular note of the upper left side of the image around the girl's ponytail and the lower middle area where her neckline extends beneath her chin. Through the attainment of this level of image purity, the practicality and attractiveness of integrated array imaging systems in a wide range of applications should be assured. The drawback, of course, is the somewhat cumbersome disc recorder equipment.

By introducing one further subsystem technique into the camera electronics (in addition to bright spot blanking and switching transient cancelling), it should be possible to achieve essentially the same total improvements in display quality as is supplied by postconverter processing of the unconditioned raw camera video through a disc recorder. Specifically, by incorporating an offset level nulling subsystem (which contains a simple serial-in/serial-out type of shift register memory as indicated in figure 5-40), those portions of the background pattern not removed by eliminating commutation transient based noise and shorted element bright spots can be internally nulled out. A full circuit design for this subsystem has not been experimentally evaluated, but the IC's required to implement the type of electronics involved are readily available and could be pulled together rapidly following any call for them in a particular system application program.
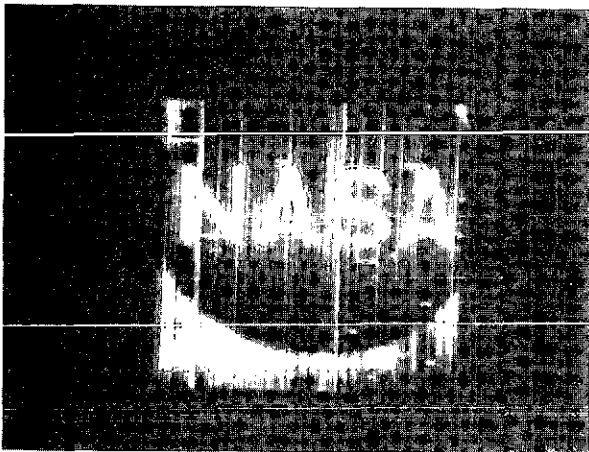
The final signal conditioning technique investigated on this program was nonlinear amplification intended to more ideally match the conversion gamma characteristics of the input solid-state camera to the output CRT monitor. In a closed-circuit form of system connected directly by coax cables, the easiest (not necessarily the best) point of introduction for a gamma matching amplifier is within the display unit as suggested by the diagram of figure 5-41.
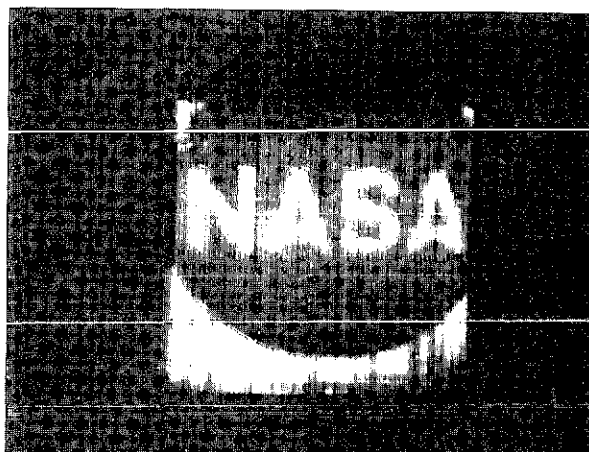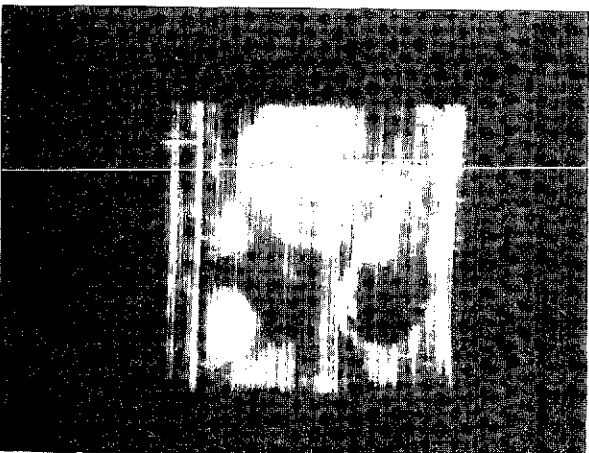
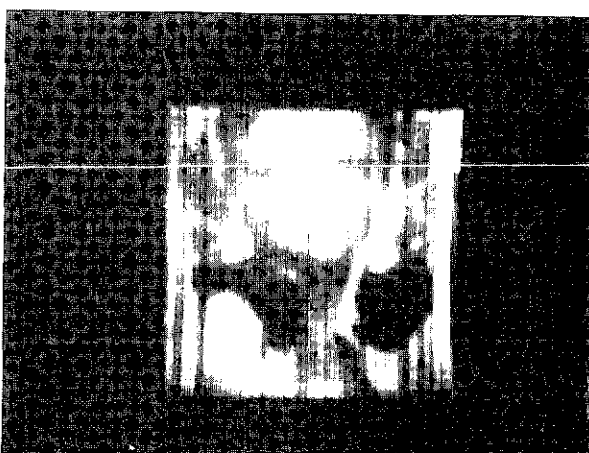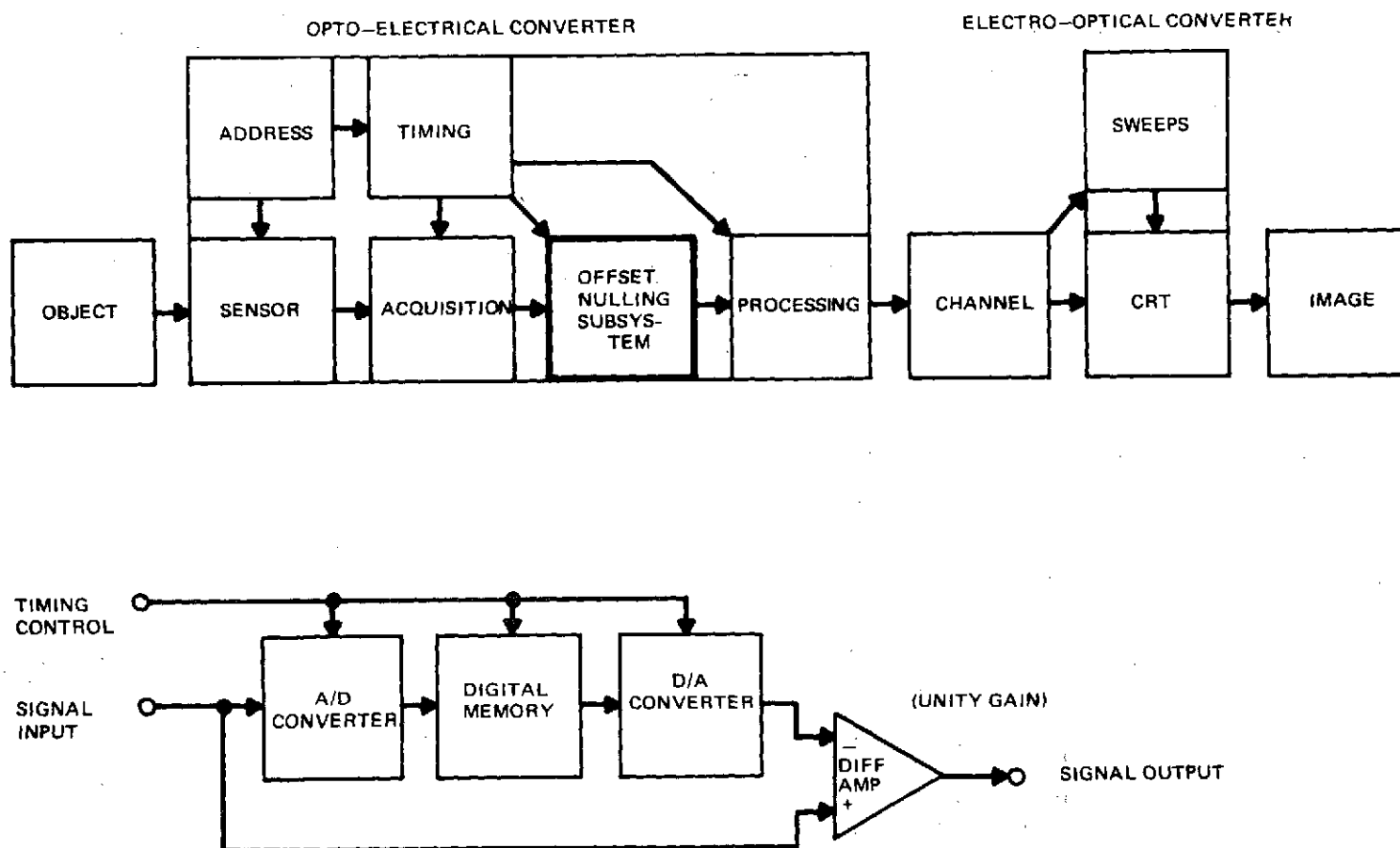Figure 5-39. Effect of Postconverter Processing
on Image Appearance

5-80

OPTO–ELECTRICAL CONVERTER

ELECTRO–OPTICAL CONVERTER

ADDRESS

TIMING

SWEEPS

OBJECT

SENSOR

ACQUISITION

OFFSET NULLING SUBSYS- TEM

PROCESSING

CHANNEL

CRT

IMAGE

TIMING CONTROL

SIGNAL INPUT

A/D CONVERTER

DIGITAL MEMORY

D/A CONVERTER

(UNITY GAIN)

DIFF AMP

SIGNAL OUTPUT

72-0581-V-38

Figure 5-40. Imager Block Diagram with Commutation
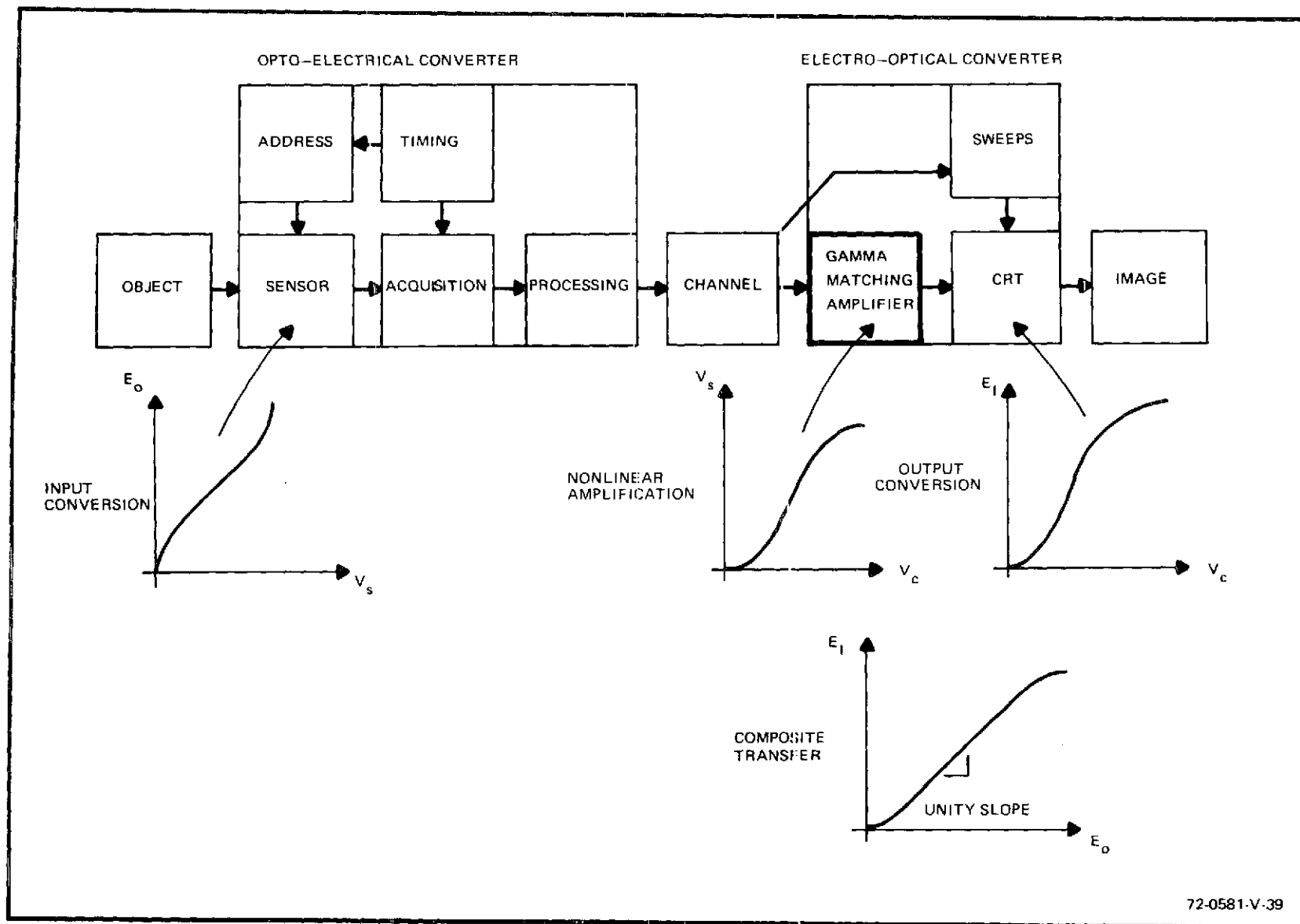Offset Nulling Subsystem Installed

Figure 5-41. Imager Block Diagram with Input/Output
Gamma Matching Provided

The need for such circuitry arises principally from the fact that, over its usable dynamic range, the conversion gamma for a solid-state sensor exhibits almost a perfect unity slope whereas, over the same range, the transfer characteristic for a CRT display device is typically on the order of two (i. e. , exhibits a power function slope of approximately 2 on a log-log plot). One of the best ways discovered to provide the needed adjustable linearity in the matching amplifier is illustrated in figure 5-42.

In this scheme a square-rooter module forms the basic nonlinear element which, when used in conjunction with an adder, subtractor, and variable gain linear amp, can be used to synthesize a controllable nonlinear power function that can be set anywhere between unity (1) and about one-third (1/3). Details of the principal square rooting and subtracting functions provided in this reciprocal gamma synthesizer are presented in figure 5-43. Part(a) illustrates how the original input (Z), its root ($Z^{1/2}$), and the difference ($Z^{1/2}$ - Z) transfer curves are interrelated. Parts(b) and(c) of figure 5-43, respectively, reveal particulars of the circuitry designs that are used in the composite
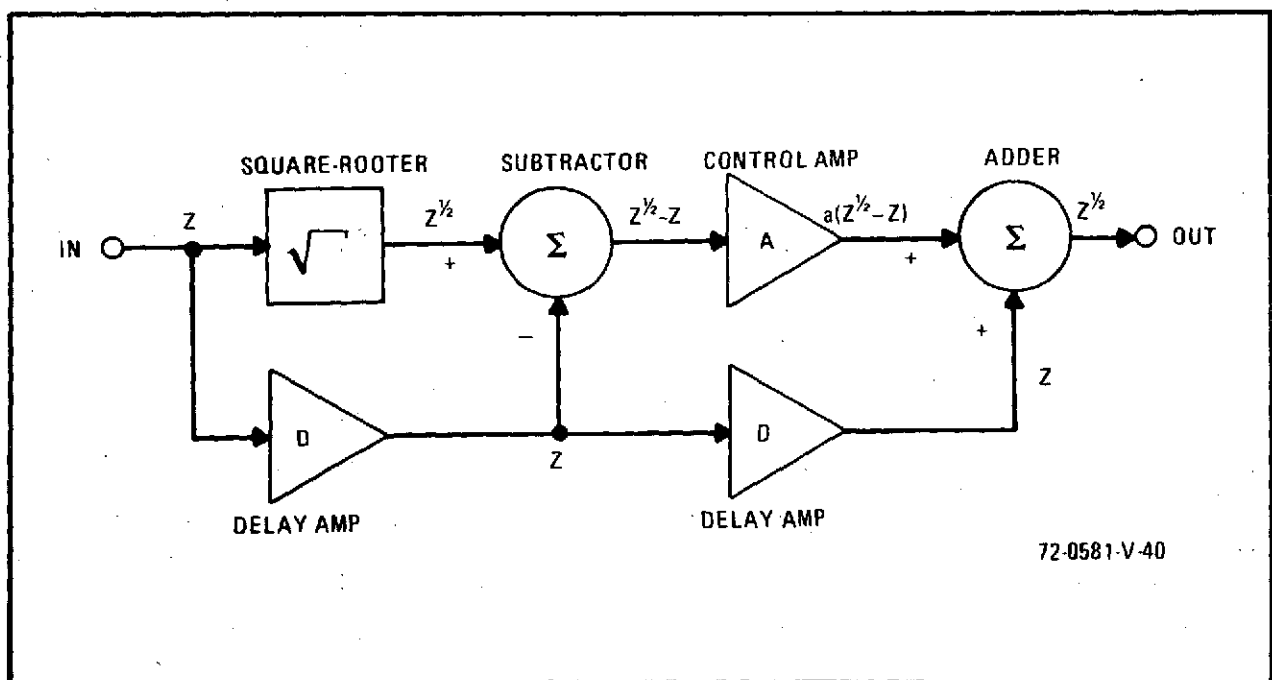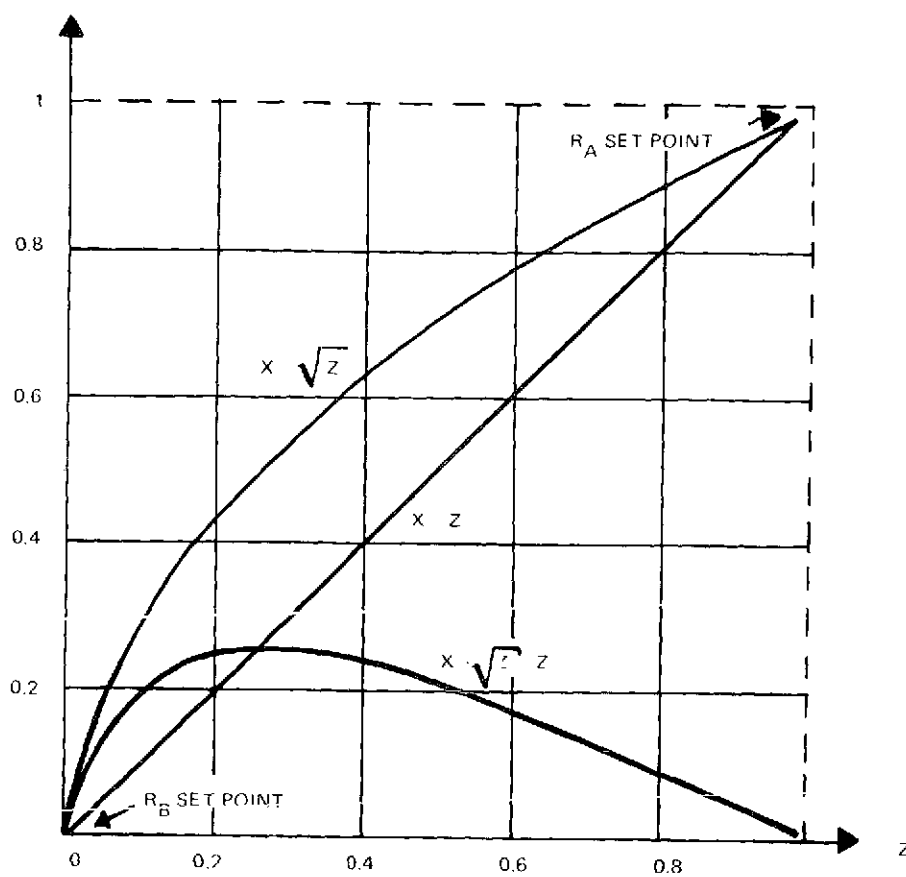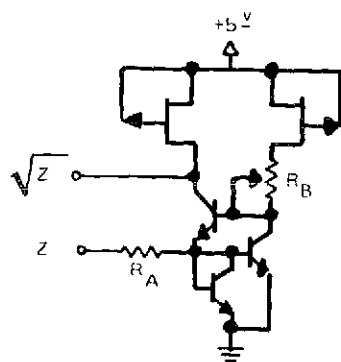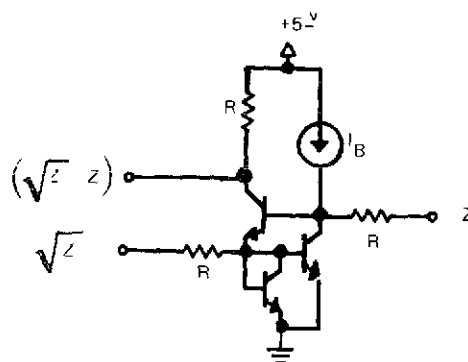

Figure 5-42. Functional Block Diagram of
Reciprocal Gamma Synthesizer

(a) TRANSFER CURVES

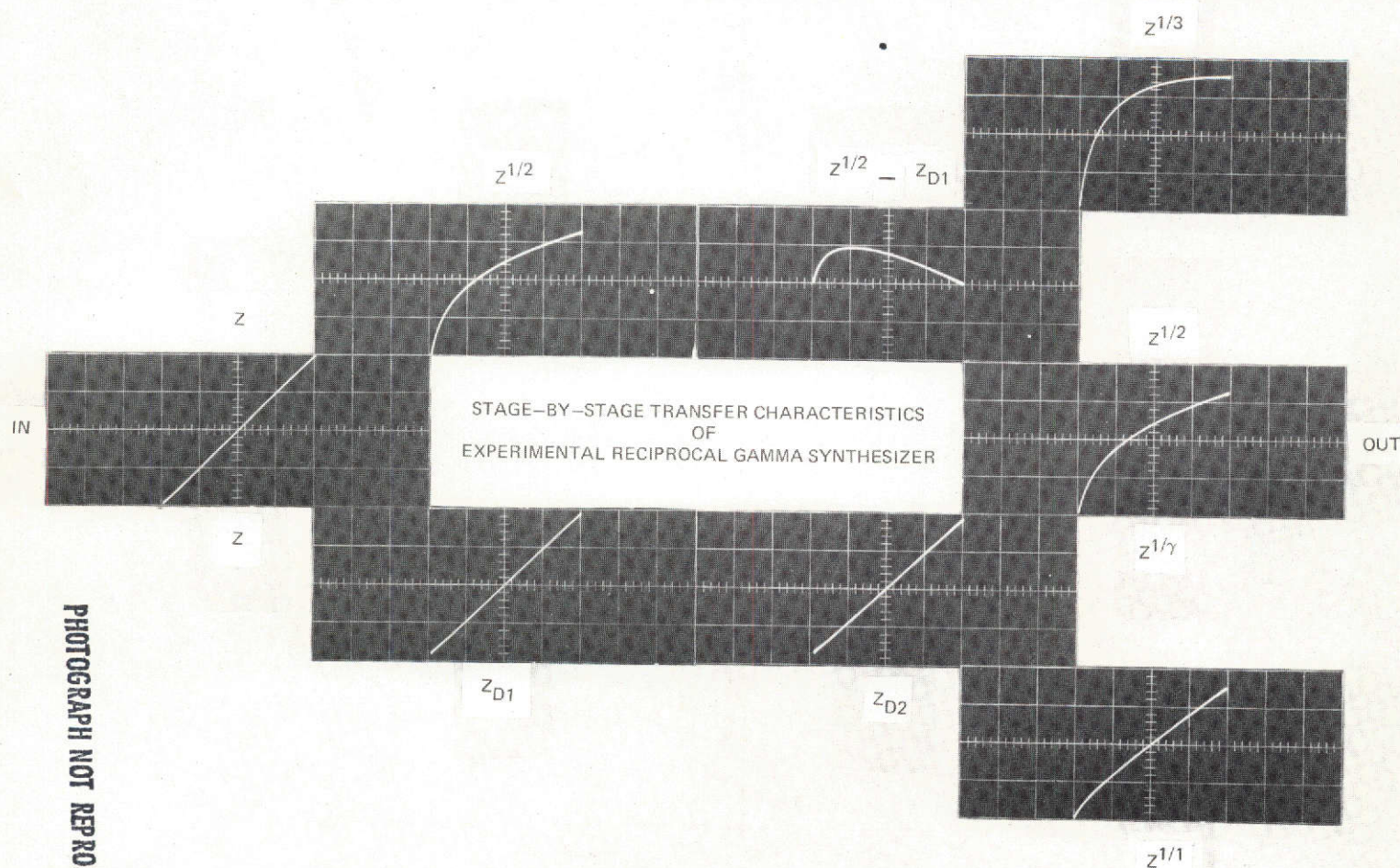(b) SQUARE ROOTER

(c) DIFFERENCE SUMMER

72-0581-V-41-1

Figure 5-43. Reciprocal Gamma Synthesizer
Primary Function Specifications

circuit design of figure 5-44 to implement the square-root and subtraction functions. In each it will be seen that an S^2CT bipolar triplet has been employed as the primary signal throughput and mixing network to assure stability and predictable response. Figure 5-45 then shows the stage-by-stage transfer characteristics realized from an experimental breadboarding of the design.

By introducing this circuit into the amplifier chain of an imaging system which mates a solid-state camera to a high vacuum monitor, the reciprocal degree of gain nonlinearity necessary to match the almost ideally linear quantum conversion process gamma of a phototransistor matrix operated in the integration mode to the highly nonlinear luminosity excitation characteristics of the display CRT phosphor can be provided. Once the condition is established, the output display monitor image will faithfully represent the gray tone variations existing over the object viewed by the camera.

Figure 5-44. Composite Reciprocal Gamma Synthesizer Circuit

72-0581 V-42-1

STAGE—BY—STAGE TRANSFER CHARACTERISTICS
OF
EXPERIMENTAL RECIPROCAL GAMMA SYNTHESIZER

72-0581-P-43

Figure 5-45.   Stage-by-Stage Transfer Characteristics of
Experimental Reciprocal Gamma Synthesizer

6. DEPLOYMENT PROFILE

Through the advent of advancements in semiconductor technology realized over the last decade, integrated imaging systems are today a practical reality. These system can be supplied in either hybrid scan form using one-dimensional linear arrays in conjunction with alternate axis mechanical motion or in fully electronic scan form using two-dimensional area arrays. Their performance characteristics can be tailored to specific application requirements and resolution comparable to commercial television can be achieved.

In those situations where maximum dynamic range and highest quality image reproduction are primary considerations — and the possibility of increased mechanical complexity can be tolerated — hybrid-scan line array converters are the obvious choice. Conversely, in those instances where long term, no-maintenance reliability while viewing still as well as moving targets with no motion of it own are primary system requirements — and a slight degradation in the cosmetic quality of displayed images will not be overly objectionable — electronic-scan matrix array cameras will predominate. With either type system, though, there can be complete architectural freedom exercised in mechanical structuring by the systems designer since he is no longer saddled with the long tubular shaped framework that is prescribed by necessity when using electron beam scanned imaging tubes. Examples of systems which illustrate this freedom will be found in the following paragraphs.

6.1 LINE-ARRAY SYSTEMS

While the primary goal of the continuing effort in solid-state imaging at Westinghouse has been the design and fabrication of solid-state bidimensional imaging converters having TV resolution, considerable work has also been

accomplished in the area of one-dimensional solid-state sensor array imaging systems. Efforts in this area have been focused on their application in character recognition and page scanner systems, as well as on their use in the study of photosensor parameters (spectral response, irradiance response, sensitivity profile, etc) and the interrelationships of these parameters to the requirements of imaging system electronics. The principal results of these studies were covered earlier in paragraph 4.4.

In figure 6-1 a montage of phototransistor line arrays is presented. This particular selection includes a variety of transistor structures having (variously) 3.5 mil, 7.0 mil, and 12.5 mil center-to-center spacings. To effectively deploy such sensors in an imaging situation requires that the object being viewed move past the array, or else that one axis of mechanical scanning be provided by linear motion of either a mirror placed in front of the detector or by the detector itself. Conditions distinctive to the application will determine which arrangement will be most effective.
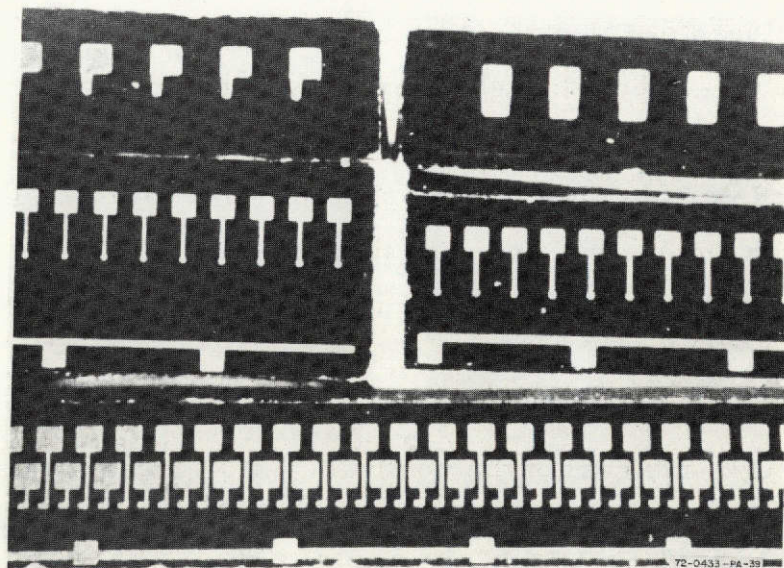
PHOTOGRAPH NOT REPRODUCIBLE

Figure 6-1. Montage of Phototransistor Line Arrays

Space probe missions calling for a planet fly-by, for instance, would probably rely on motion of the vehicle and hence of the array across the target. In page readers, on the other hand, passage of the document past the sensor is the standard practice. To view scenes lying in a parallel plane which have no relative movement along an axis orthogonal to that of the pickup device though, some form of oscillitory motion by or within the line array imaging system will be necessary.

One example of an early linear array image converter built some time ago with hybrid bare chip sequencing logic will be found in figure 6-2. Here the array consists of an 80 element row of matched photosensors. Successive elements in the row are interconnected to their respective logic interrogation blocks through nine overlapping layers of flexible gold coated Kapton wiring, which has been quite descriptively referred to as "seaweed". The dynamic range realized with this mechanization was better than 10:1 and uniformity was maintained within ±2 percent.
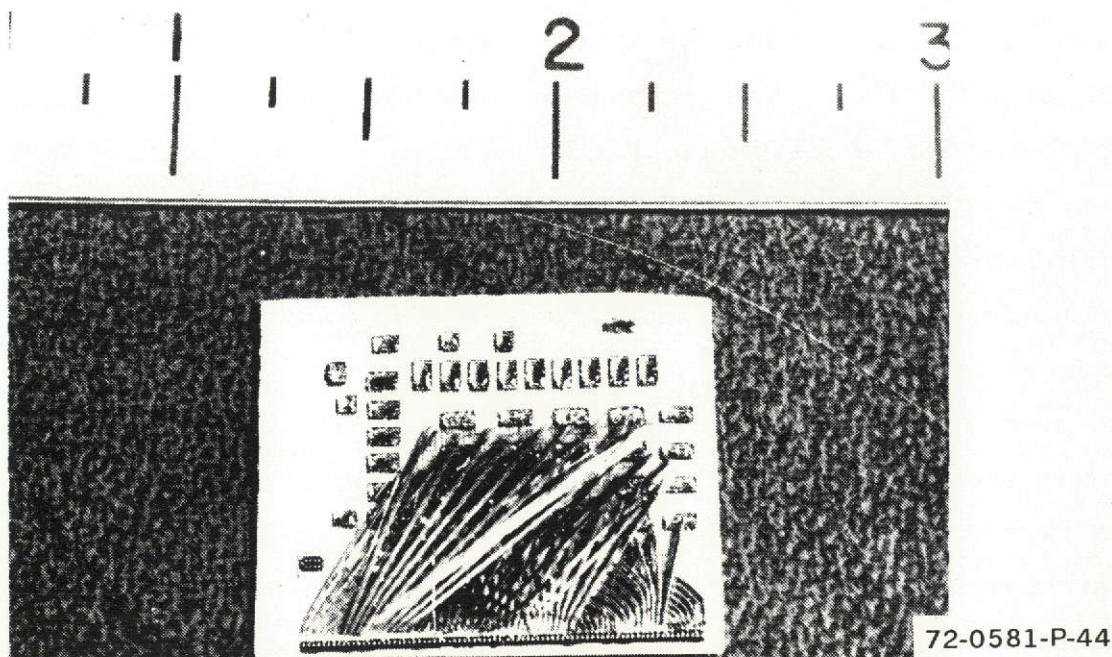

72-0581-P-44

Figure 6-2. Early Model of Linear 80 Element Phototransistor
Array with Hybrid Bare Chip Logic

Even though unidimensional linear sensor organizations like this typically exhibit greater dynamic range than bidimensional matrix configurations as a result of their greater simplicity, tight element characteristics matching over any great length presents no mean task. To circumvent the problem, an extended length sensor array is commonly built up from a series of shorter lines that have been probed, tested, and hand-picked for matched parameters. Figure 6-3 displays a 400 element line array intended for OCR document scanning that was fabricated using this technique.

The subunit strips making up the array here were initially processed in 50 element sections with their individual phototransistors spaced on 7.5 mil centers. After selective testing, eight strips were laser scribed out of the original wafer and mounted on a previously prepared ceramic substrate to form the 3 inch long composite sensor line shown. Along either side of the line was then added the two series of specially built 16 bit shift register dice that are in evidence. In tandem, these registers carry out the required sequential interrogation of contiguous phototransistors along the array.

Imaging capabilities of the linear array system cited above and a shorter 1-by-40 line array converter are revealed in the display monitor photos of figure 6-4. These photographs were facilitated by mechanical scan rotation of the sensor/lens system. The 1-x-40 array image in figure 6-4a was picked up from a synchronous sweep real-time display while the 1-x-400 array image in figure 6-4b was secured from a delayed single sweep display on a storage monitor. The frame rate in both instances was approximately 240 lines per second.

One of the fundamental limitations on low-light-level imaging with any integrated optoelectronic photodetection system, whether it be of the line array variety discussed here or the matrix array type considered next, is the dark level leakage offset variations which are the result of uncertainties in reseting a storage junction to a specific, fixed potential following each readout. Advanced design concepts making use of a combination of

6-4
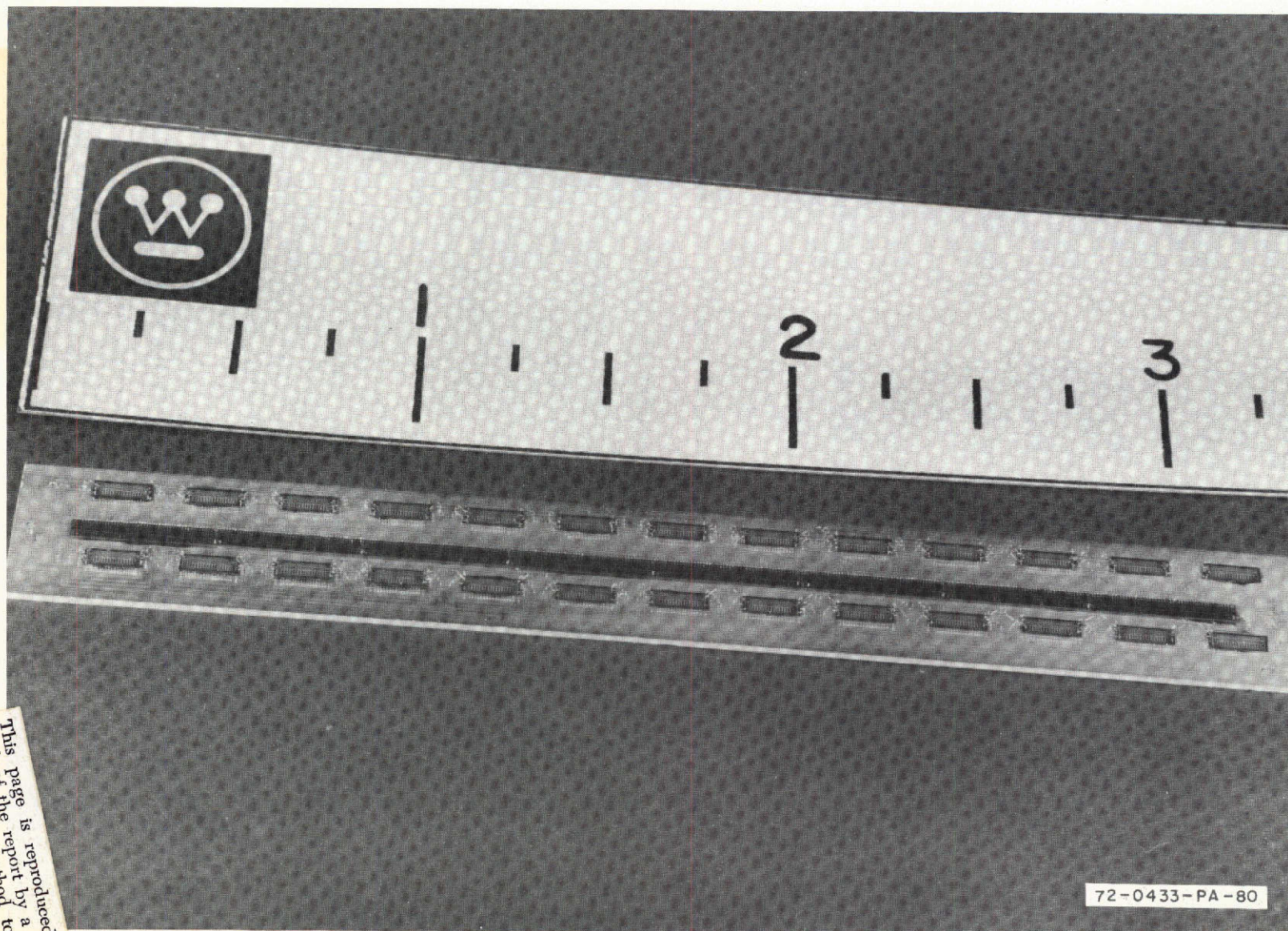
72-0433-PA-80

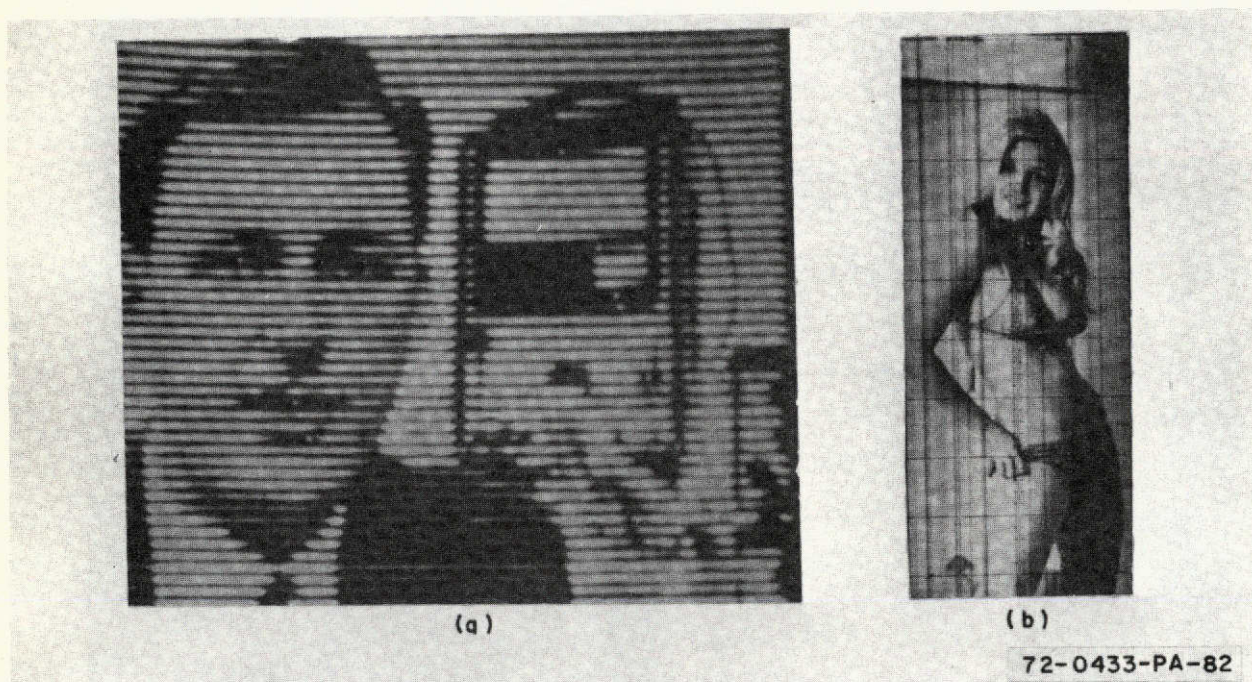Figure 6-3.   400 Element Line Array Fabricated in 50 Element Sections

Figure 6-4. Hybrid Scanned Imaging

time-sharing, sample-and-hold, and read/reset subtractor techniques have
been advocated for minimizing these leakage factors, and preliminary test
results in the area have generally been promising. A reasonable measure
of success here could conceivably extend the functional range of integrated
imaging systems down to the starlight regions now reached only by SEC
and equivalent types of imaging tubes.

The foregoing is a cursory description of the work Westinghouse has
accomplished in the phototransistor linear array area. This area of con-
cern was initiated in 1962 and has continued to the present time with support
of both government contracts and in-house funding.

6.2 MATRIX ARRAY SYSTEMS

Development of the first known fully solid-state image converter was, as
indicated earlier, made on this program by Westinghouse in 1965 following
extensive research into the characteristics of junction photodetectors, the
processes of fabricating integrated arrays, and the evaluation of scanning

6-6

techniques using line arrays and line array systems like those discussed in the preceding section. While the performance of this camera was far from earth shaking compared to home television standares, the fact that a thin flat slab of silicon had been made to capture an image without the assistance of mechanical motion was a truely remarkable achievement at the time.

Studies of the operation of this camera led to numerous refinements in integrated imaging systems techniques, including the discovery of the now dominant integration mode of operation. Subsequent systems following this trail blazer contained, respectively, phototransistor arrays of 12,800 elements, 51,200 elements, and 200,000 elements — roughly a quadrupling of the number of sensor points-per-array with each generation. Vertical streaking was evident in their images as a result of a combination of dead (or non-responsive) lines and digital scan conversion switching noise. This remains the major aesthetic distraction which has deterred any great proliferation of solid-state array cameras. Ongoing efforts like those described in paragraph 5.5 are directed toward alleviating the condition.

Development work paralleling that for the above cameras has resulted in production of a variety of novelly configured image converters. The unit in figure 6-5, for instance, contains a 50-x-50 element array along with all necessary scanning and signal processing electronics and is housed in a volume of approximately 1 cubic inch. Designed in 1967, this image converter was provided with the then prevelent DTL logic family to accomplish the various counting and decoding functions needed and internally fabricated C-MOS transmission switches to commutate the array output signals. Interconnects between the sensor mosaic and the sequencing circuitry were made along conductors etched from gold coated flexible substrates of 3-mil-thick Kapton (a polymide film produced by E. I. duPont deNemours & Co., Inc.) to facilitate folding the peripheral bare chip electronics around to planes parallel to the sides of the housing and perpendicular to that of the array and thereby conserve volume. Power consumption for the system was relatively
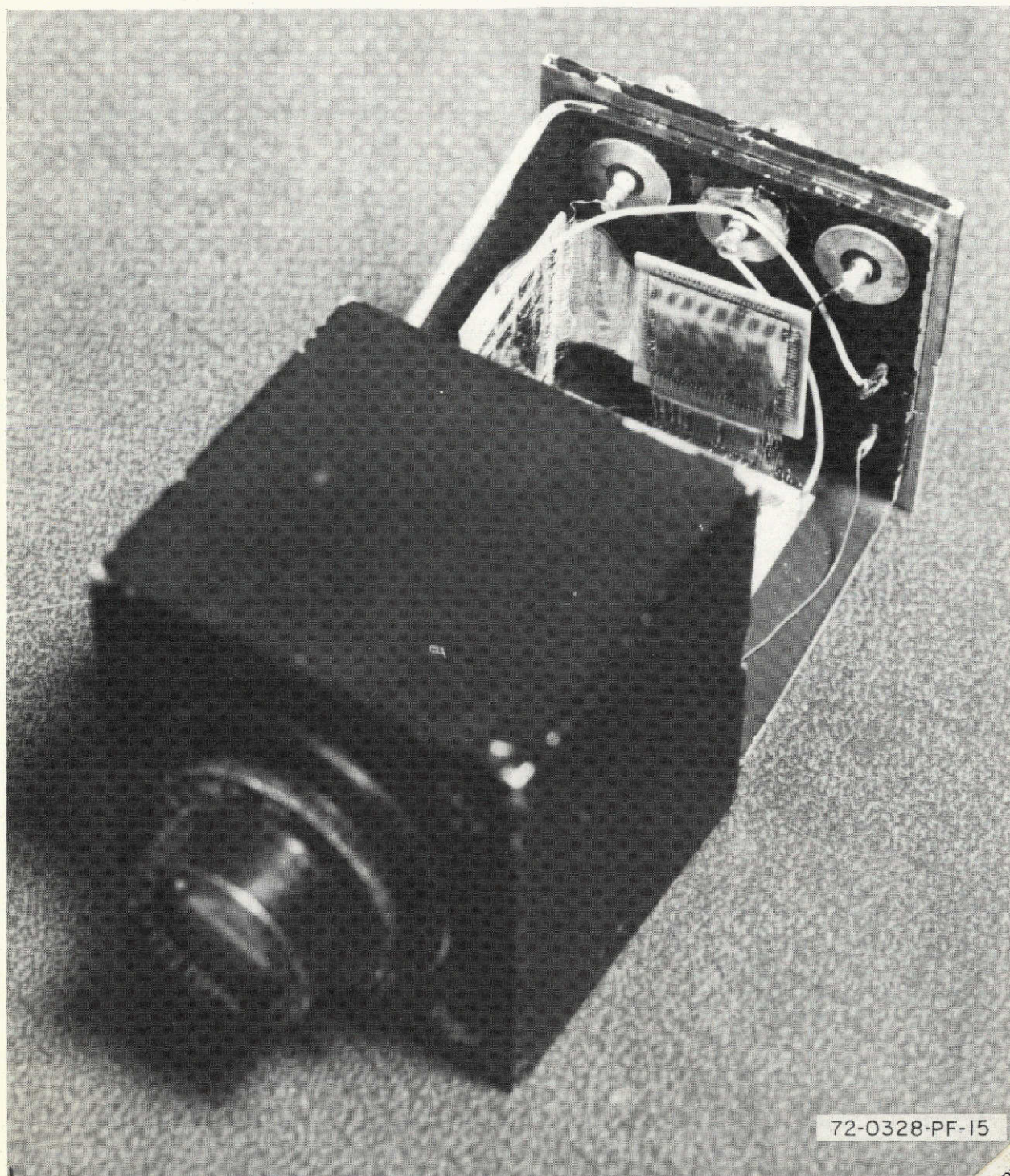
72-0328-PF-I5

Figure 6-5. "Cubic Inch" 50-by-50 Element Camera

6-8

high (on the order of 1 watt) due to the type of logic employed. Similar units can now be fabricated in even less volume and with at least 2 orders of magnitude less power by changing over to the micropowered CML device family.

A second example of a uniquely packaged solid-state array camera system is provided in figure 6-6. As seen here, an entire integrated imaging system —plus a self-contained battery supply capable of powering the system for better than 2 hours — has been installed in the film cartridge space of a commercial super 8 movie camera. The heart of the system is a 50-by-80 element sensor array built on the same elemental spacing as its big brother, the 200-by-256 element sensor array. The 50-by-80 element camera system makes use of available integrated circuit analog and digital chips by employing what has been called "hybrid" large-scale integration or multichip packaging. Specifically, a total of 117 MOS and bipolar integrated circuit chips, together with a number of MOS capacitors and diffused resistor chips,
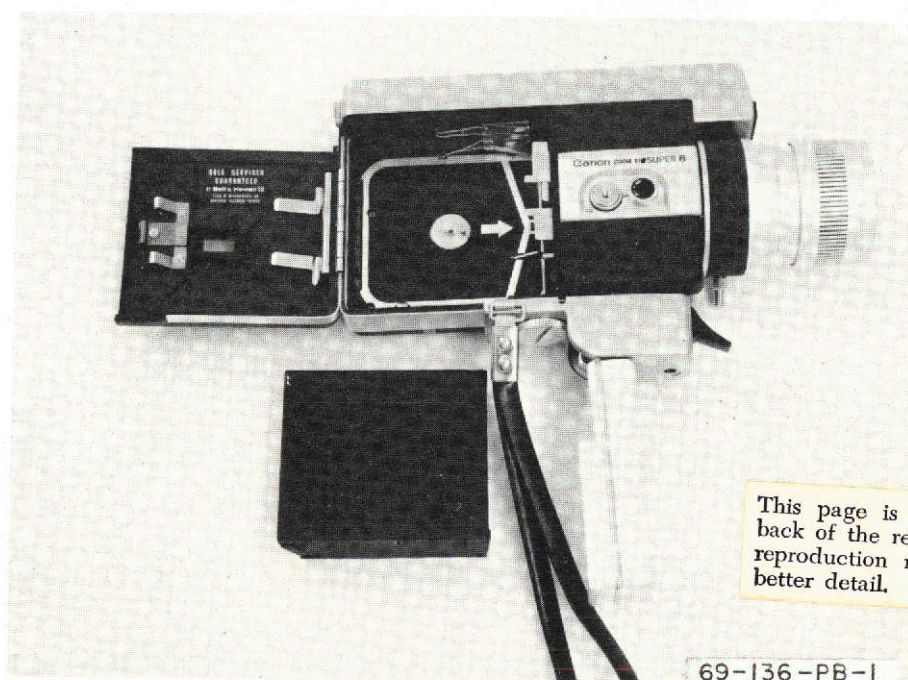
69-136-PB-1

Figure 6-6.   Super 8 Movie Camera Packaged Integrated Image Converter

are mounted on a single 2. 6 – by–3. 0 inch gold evaporated ceramic substrate (figure 6-7). This technique permits moderately dense packaging without the accompanying long lead time and high development costs of full-blown LSI packaging. For simplicity of optics, the primary circuitry carrying sub-strate is placed in a package similar to the standard movie film cassette appearing in figure 6-6. This does not necessarily represent the smallest or simplest packaging scheme, but it does provide a convenient test bed for system evaluation and gives an indication of the variety of packaging configurations achievable.

Other examples of area array integrated imaging systems that have been proposed include OCR document scanners, low-cost "throw-away" remote surveillance cameras, and tactical map readers interactively interfaced through a computer. Still further potential applications exist in such diverse areas as mine safety monitoring, missile or bomb guidance, EROS satellites, star tracking, spacecraft docking maneuvers, and blind ambulatory aids. It is anticipated that these plus many other fields will soon see widespread usage of molecular, TV-like cameras.
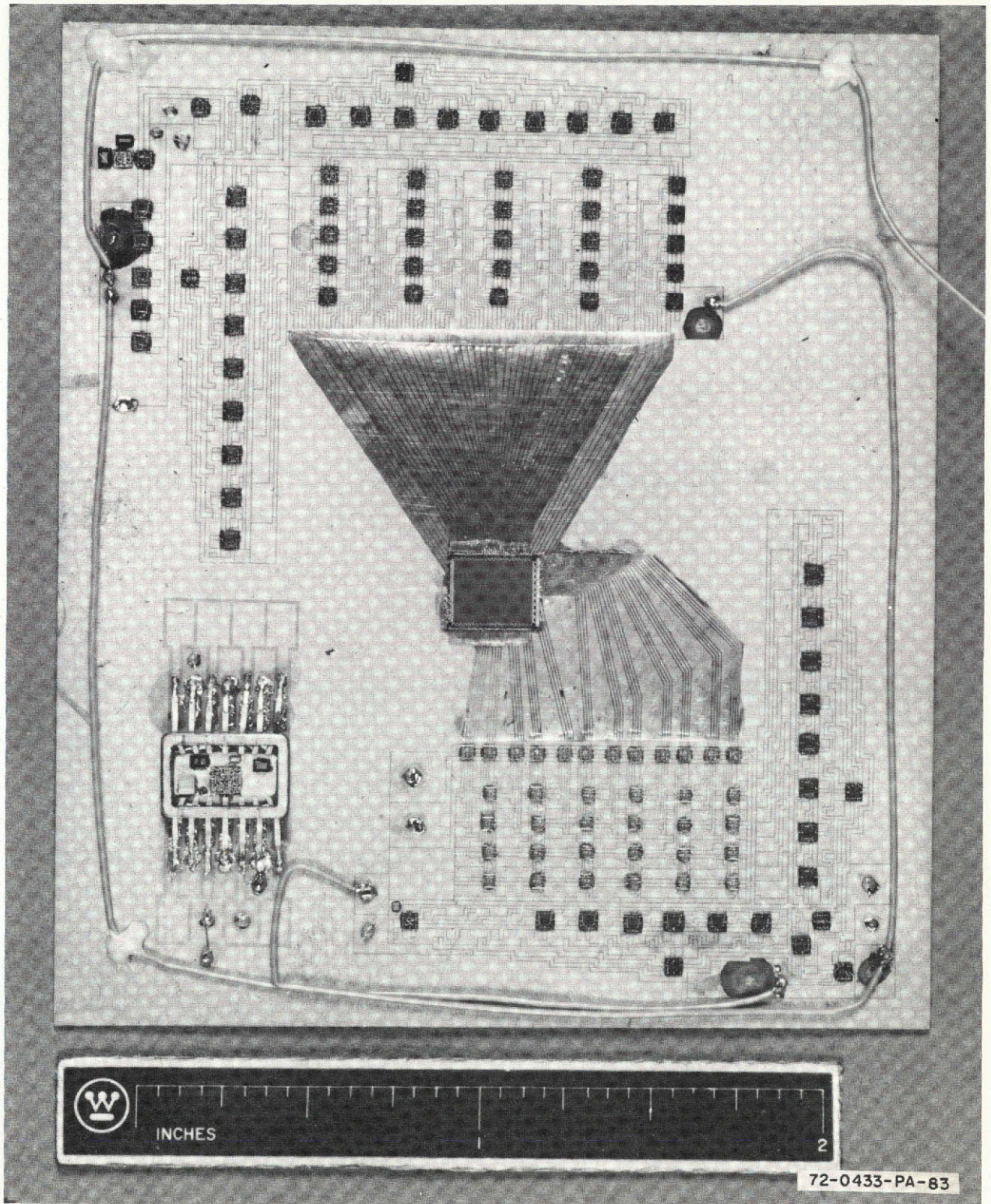
Figure 6-7. 2.6- by-3 Inch Electronics Substrate in Super 8 Image Converter

7. 400-BY-500 CAMERA

Earlier work on the Image Converter of Radical Design program led to development of 50-x-50, 100-x-128, and 200-x-256 element solid-state imaging systems. Each of these successive generations was directed toward the evolution of an integrated array imager having resolution capabilities comparable to those of commercial television. This effort has now culminated in production of the unique, planar architectured 400-x-500 element molecular image converter (MIC) shown in figure 7-1. As configured here, the camera is completely self-contained needing only a source of 110 volt ac power, is totally molecular in design using state-of-the-art silicon technology devices throughout, and is output interface compatible with any conventional TV studio type display monitor.

Functionally and physically this system is divided into two distinct sections: the image converter mainframe, which is 10-x-10-x-2 inches and contains the 400-x-500 element photosensor array and all scanning and control electronics; and the detachable supply/processor subunit, which is 10-x-3-x-2 inches and contains the multiple power converters and EIA format video processor. Electrical outputs from the camera mainframe are in the form of raw, scan-converted image video and separate blank and sync pulses. These signals may be used directly if desired, or they may be passed on to the remotely programmable subunit where the processor combines them into a 1 volt peak amplitude EIA format TV video composite signal which is then output in both positive and negative polarity push-pull form. Scan synchronization for the system is provided by an Apollo moon camera type digital sync generator while master clocking is selectable from either an internal crystal controlled source, which produces the US standard 525 line 60 interlaced fields-per-

72-0581-P-50

Figure 7-1.   Engineering Model 400-x-500 Element Integrated
Array Camera

second TV scanning format, or an externally variable source, which permits tailoring the system frame rate to meet individual application requirements.

The nonenchanced conversion transfer range typically realized for irradiance in the range of 400-to-1000 nanometers (10 percent response points) is eight shades of gray, with the minimum irradiance level of approximately 0.2 $\mu W/cm^2$ at 30 Hz frame rates being limited primarily by scan conversion uniformities. Signal information bandwidth, with internally controlled scanning, is 4.5 MHz — identical to that for commercial television and resulting in the same qualitative resolution in line-pairs. Power input to the system electronics, on the order of 12 watts, and packaged camera weight, nearly 5 pounds, are moderately high due to the conservative design approach that was taken with this developmental converter. Both values can be substantially reduced in specific application MIC's by capitalizing on recent MOS technology improvements and tailoring the structural frame accordingly. Realizeable specifications in these areas should be 1 watt and 1 pound.

7.1 MECHANICAL LAYOUT

All aspects of the mechanical design for the engineering model PICTURE "45" camera have been selected to assure the structural integrity and thermal management necessary for reliable system operation in a laboratory/office type of envinronment not exceeding 30°C. The main camera chassis is formed as essentially a one dimensional plane from a 10-inch-square area block of aluminum. Over this fits a dust cover which is tailored in depth to make the aggregate chassis-plus-cover thickness 2 inches to match the required dimension of the detachable subunit. A 50 mm Leitz lens having variable iris settings of f/1.4-to-f/16 and continuous focus adjustment attaches to a circular lens mount secured in the chassis cover by 4 bolts and adds a centrally located 2-1/2 inch projection. The back surface, which is milled out to form a large finned heat sink (see figure 7-2), is kept machine flat and free of all projections to facilitate mounting the camera on a vehicle bulk-heat or domicile wall in the fashion of an ordinary picture frame.
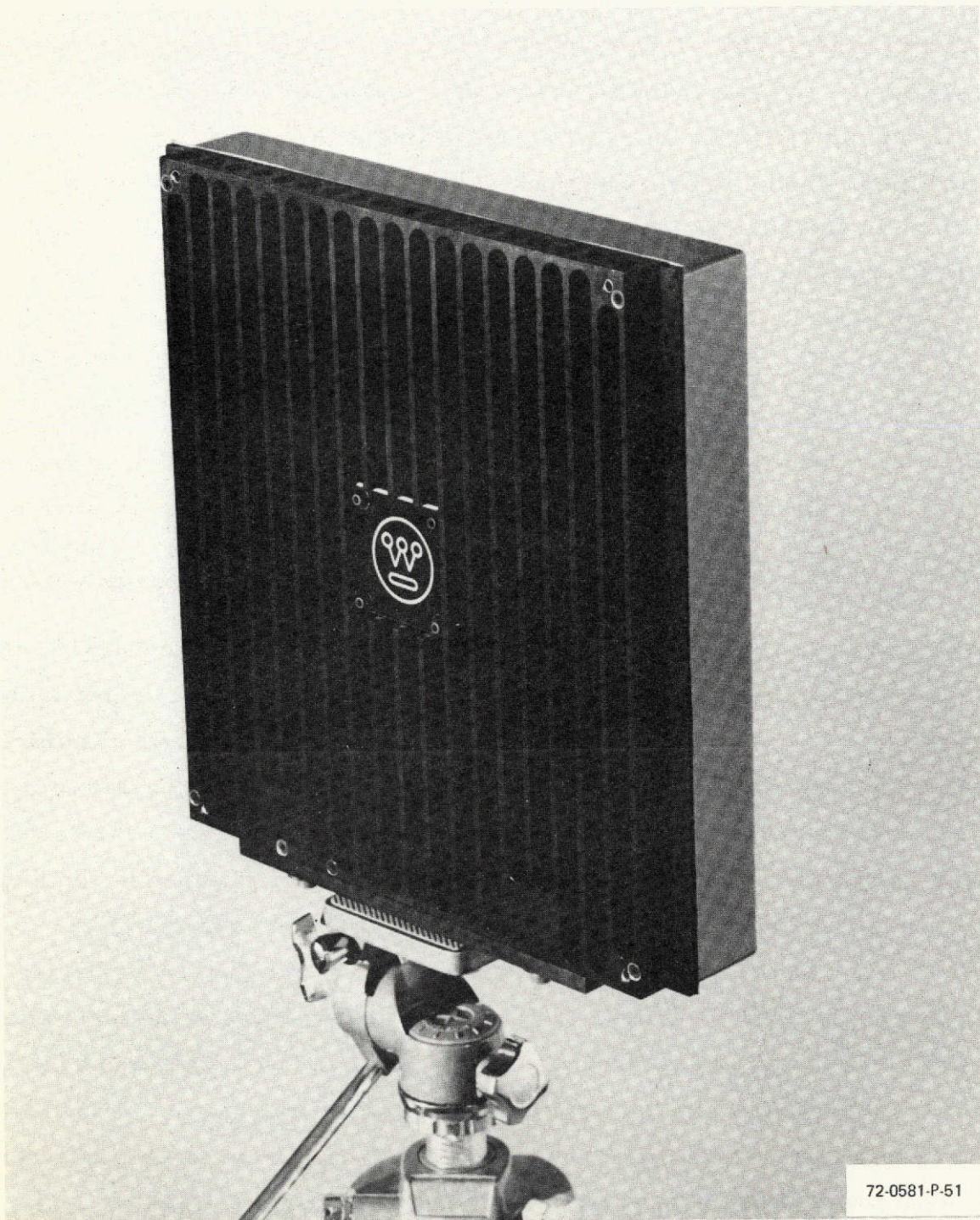
72-0581-P-51

Figure 7-2.   Backplane View of 400-x-500 Element Camera Mainframe

Separation of the aggregate converter into two distinct units was instituted so that the scanner head could be operated remote from its power supply. Furthermore, with this arrangement it is possible to operate the imager from primary sources other than single phase, 60 Hz, 110 Vac by substituting and alternate supply/processor subunit for the original. This allows, for instance, for powering the converter from a battery, or the 28 Vdc commonly found in aircraft and spacecraft. In addition, should it be desired to change the format of the system output video to something other than the EIA standard for commercial television, such a change can be accomplished without the need for entering the camera mainframe to introduce the required circuit modifications.

In prior generations of solid-state array cameras the sensor element and readout circuitry densities were sufficiently low that conventional printed circuit packaging of integrated circuits and mechanical connector interfacing with the mosaic was practical. For the 400-x-500 system, though, the quadrupled sensor element density requires that considerably more sophistication be exercised in both circuit and equipment design. Long leads and mechanical connectors between the readout circuitry and the matrix array have been avoided to minimize the interline capacitance and accompanying crosstalk noise that has beset former systems. State-of-the-art larger scale hybrid integration (LSHI) techniques for the packaging of bare chip microcircuit components on polished alumina substrates are employed throughout to achieve the density of perpheral circuitry required in the system. Special attention has been given to details of the network designs implemented with these packaging techniques so as to optimize circuit speed while minimizing power usage related temperature gradients and maintaining compatibility with available integrated circuit chip parameters.

Organization of the system electronics within the camera mainframe, as seen from the internal view presented in figure 7-3, follows a well-ordered planar layout of functional subsections that fit together much like a large
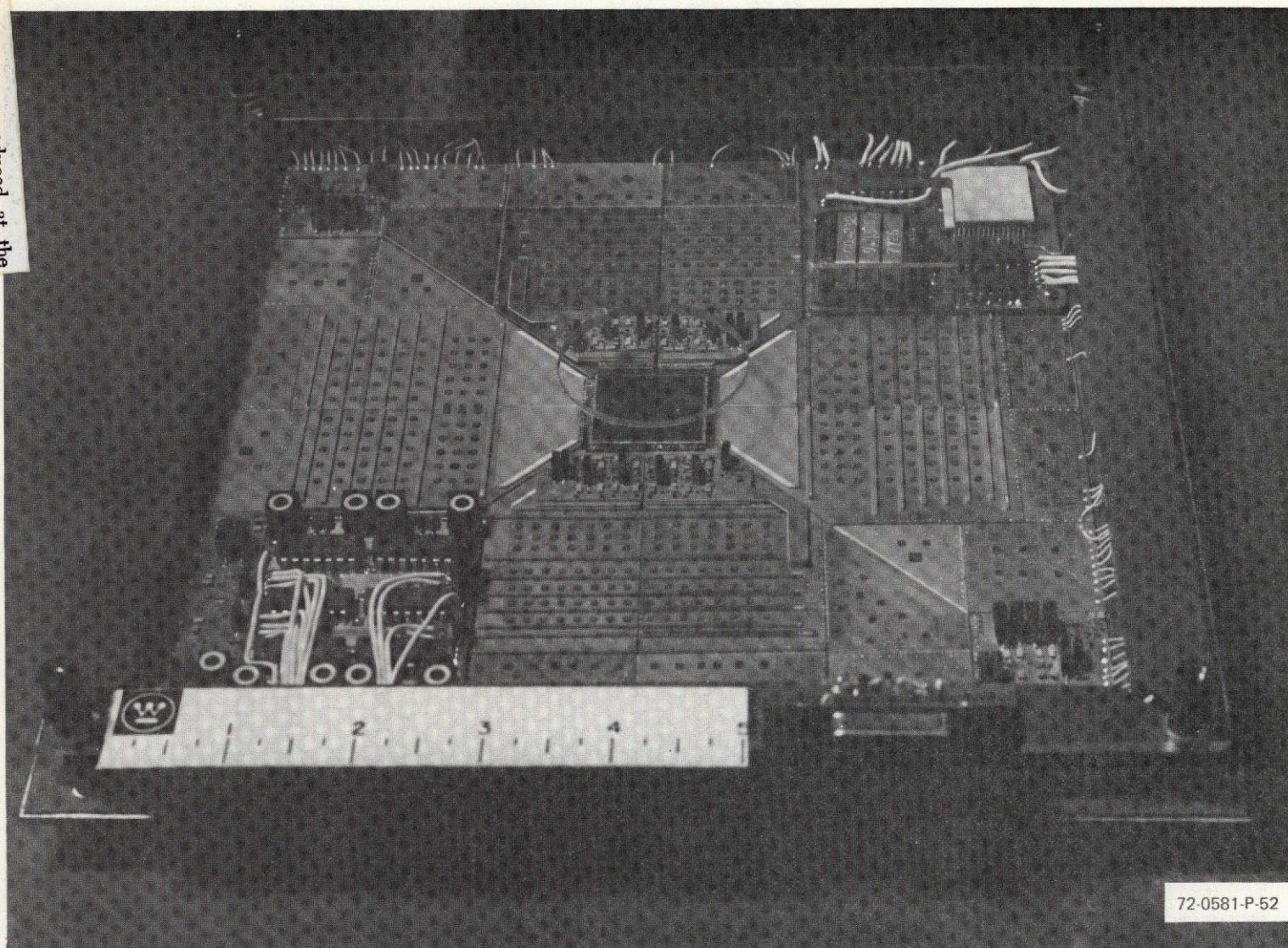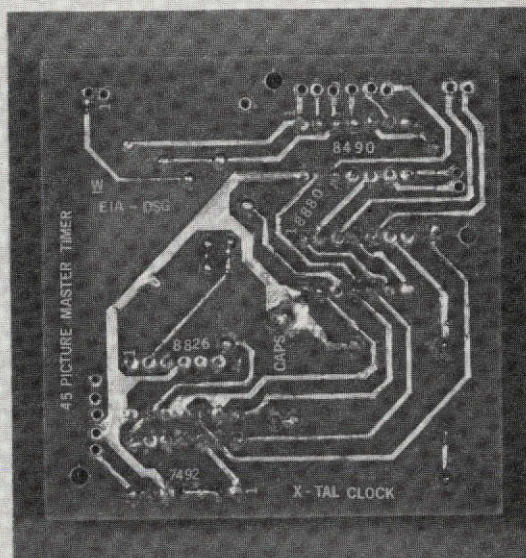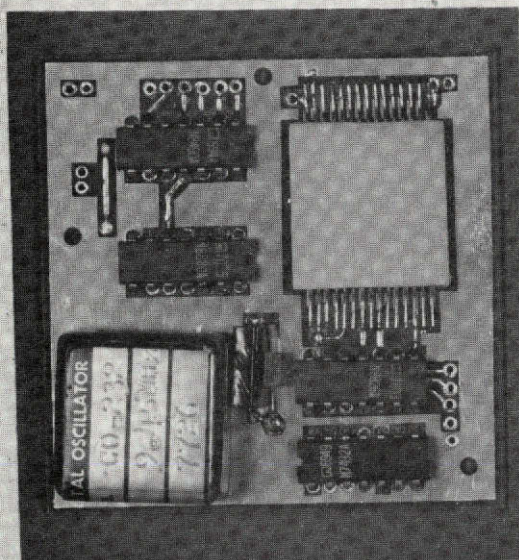
72-0581-P-52

Figure 7-3.   Internal View of 400-x-500 Camera Mainframe Showing LSHI Packaging Layout

jig-saw puzzle. Taken in-total, this aggregate collection of ceramic substrates and printed circuit boards has been said to resemble a planned model city development — high rise apartments, storage tanks, cross streets and avenues, central plaza, encircling beltway, etc. The breakdown of electronics on the individual circuit boards is established on the basis of a tradeoff balance between functional unit modularity and cost effective component count. Two of the sections thus established are implemented in discrete-package printed circuit board form rather than hybrid bare chip ceramic substrate form due to the nature of the components they contain.

These two boards, shown in greater detail in figure 7-4, house the entire master control electronics for the scan conversion and multiplexed signal processing operations carried out in the camera. In figure 7-4a appears the master timer circuit board containing the 9.45 MHz crystal clock, which initiates all system functions, the Apollo moon camera type digital sync generator, which formats the basic scanning operations, and the miscellaneous counters and gates that are interrelated with the clock and sync generator in total management of system functions. The multiple gate board in figure 7-4b contains two banks of trim pots which, through the unique characteristics of the logic gates to which they are connected, are used to precisely delay and edge-coincidence-match opposing phases of the sampling windows used in the analog section multiplexers. It is readily obvious that these two boards constitute about the tightest printed circuit layout packaging possible, and thus do not materially influence the overall camera size.

Except for these two master control oriented sections, all other portions of the mainframe electronics are fabricated in hybrid bare chip form. In addition to greatly reducing total packaged system volume, this approach facilitates the elimination of numerous mechanical connectors and the placement of array interfacing circuitry directly adjacent to the sides of the mosaic wafer. Furthermore, it permits the use of pretested components, in-process tests, and corrective rework of sufficient level to achieve a much

A. MASTER TIMING BOARD
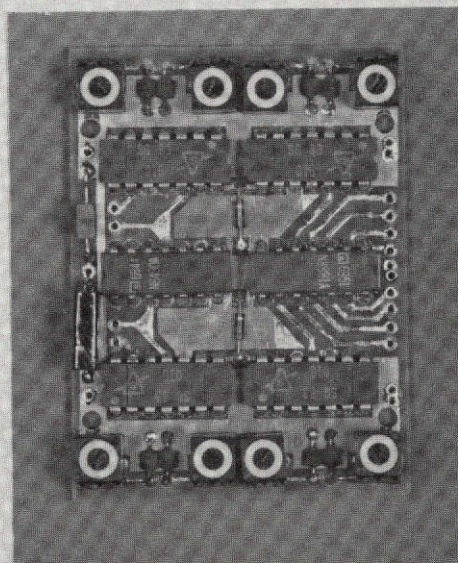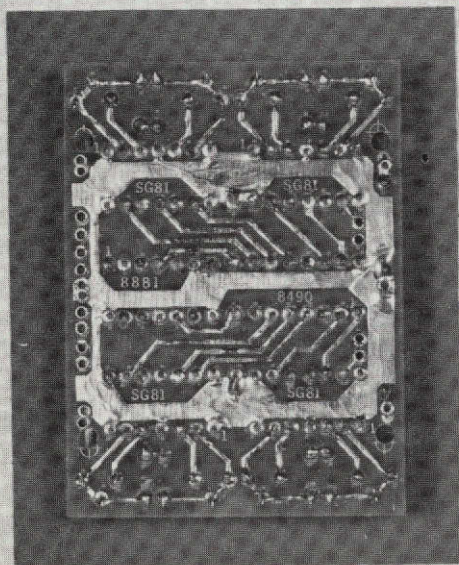
B. DELAY GATING BOARD

72-0581-P-53

Figure 7-4. Master Control Electronics PC Board in 400-x-500 Camera

higher process yield at a lower unit cost than could be realized by totally monolithic large scale integration (LSI) techniques. This is particularly true where, as in the present case, only one developmental or a few prototype systems or circuits are being built; and where, therefore, component microcircuit dice must be obtained from associated suppliers.

Process fabrication of the individual substrates is accomplished using the reverse etch technique for engraving isolation grooves between conductive lands. The substrate material employed is electronic grade alumina having an 8 microinch finish. Metallization is provided as a two step evaporated chromium-gold deposition in which 300 $\overset{\circ}{A}$ to 500 $\overset{\circ}{A}$ of chrome is used for adhesion and is supplemented by 15,000 $\overset{\circ}{A}$ to 20,000 $\overset{\circ}{A}$ of pure gold for low resistance conductors. Cutting to size is accomplished with a water bath diamond saw. Figure 7-5 shows one of the more distinctively shaped substrates. The various silicon integrated circuits, thin film resistors, and hybrid capacitor chips are mounted on the finished base substrates in an insulating Doryl varnish compound having a thermal coefficient of expansion closely matching that of silicon. Thermo-compression ball-and-stitch bonding is used to interconnect integrated circuits to individual substrate conductor lines and to interface between adjacent substrates. Supply, ground, and control and signal line connections to the peripheral wiring channel harness are made through number 30 copper wires silver epoxied to oversize pads on the outermost substrates (see for example the 1LM analog processor substrate in figure 7-6) and low temperature soldered to tie points on a PC board strip placed along the bottom of the wiring channel.

In some areas it has been expeditious to incorporate a second level of super-strate material overlaying the base substrate. This was done to provide crossover buses for carrying common signal lines and supply voltages to widely separated components, or to reduce the density of lines in the fan-in address area around the photosensing matrix and thus relax the fabrication tolerance for etching the requisite conductor runs. On the large
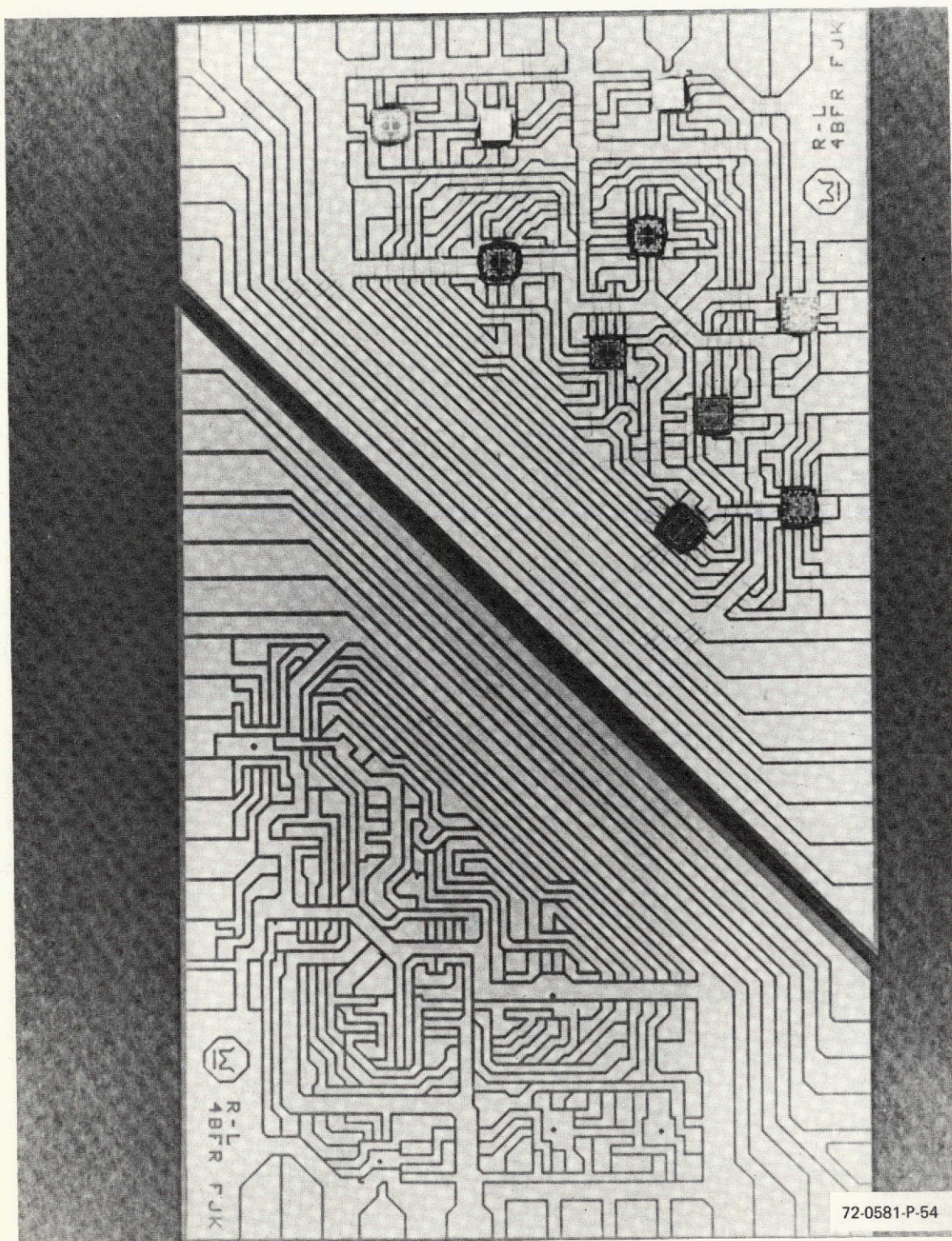
Figure 7-5. Unique Trapezoidal Shape Substrate Used in 400-x-500
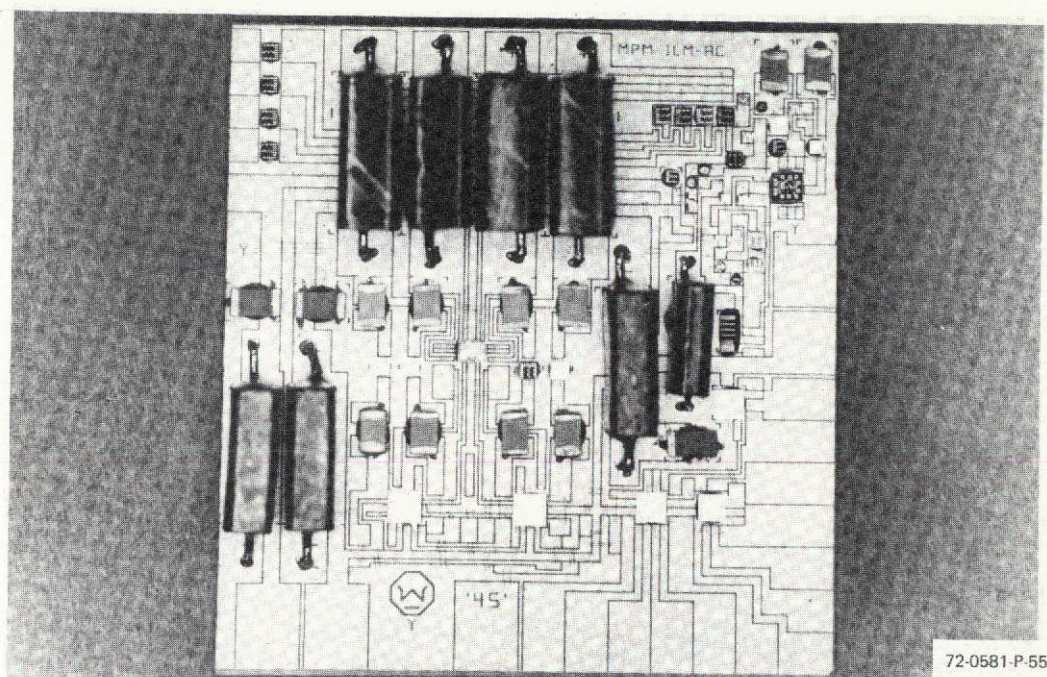Camera

Figure 7-6. Wiring Channel Interfaced First Level Multiplexer
(1LM) Substrate

array interface substrates, the resultant fan-in superstrates are of sufficient
size to permit their use as areas where extra circuitry can be mounted. As
seen in figure 7-7, this idea was in fact executed on the column (emitter)
interrogation substrates to facilitate placement of the multichanneled signal
acquisition and first level amplification electronics immediately adjacent to
the array. Consequently, long leads at this critical point are eliminated,
transfer noise pickup is minimized, and highest quality performance is
assured.

Finally, in the exact middle of the camera scanner head is located the
200, 000 element phototransistor mosaic. The array is initially mounted on a
specially formed aluminum alloy pedestal and then inserted through an
aperture provided in the back plate of the camera. This pedestal is precisely
machined for flatness and proper height to place the sensor at the focal point
of the system lens. Due to leakage currents in the silicon photomosaic

7-11

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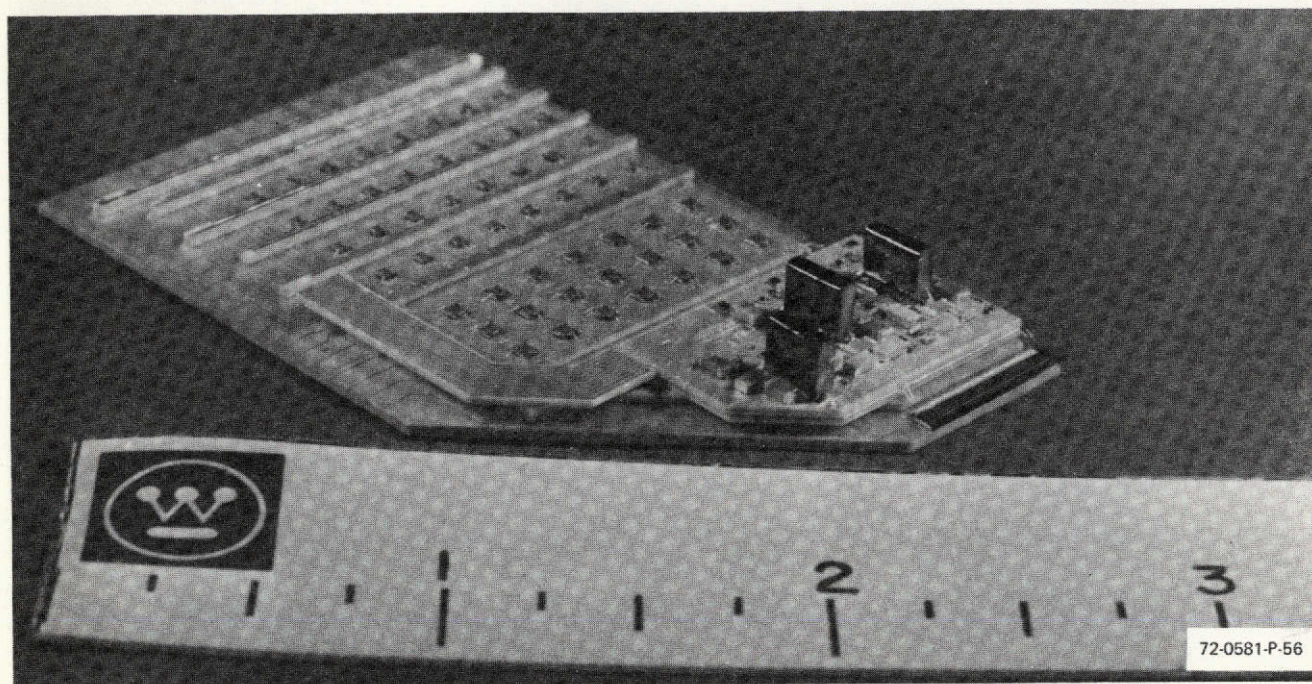reproduction method to provide
better detail.

Figure 7-7. Compound Level Column Interrogation Substrate in
400-x-500 Camera

having the characteristic of doubling for every 8°C rise in temperature,
consideration was given to the possibility of including a multistage bismuth
telluride thermoelectric cooling element in the mounting pedestal. Thermo-
dynamic analysis revealed, however, that such devices are so ineffecient
that little if any gain would truely be realized in reducing the detector
temperature. Instead, the mounting fixture into which the mosaic pedestal
fits has been provided with thermally nonconductive insulating bushings.
This greatly inhibits the direct conductive transfer of heat from surrounding
circuitry; and therby, due to a greater temperature gradient, aids in
expelling convectively transferred heat. Preliminary operational tests with
the system indicate that this is a sufficient measure to assure that an
acceptable image capture ratio is maintained for operation in the stipulated
laboratory/office environment.

Interface connections between the detector chip and its surrounding address electronics substrates is made by way of 0.5-mil diameter gold wires that are thermo-compression ball bonded to the mosaic pads and ultrasonic stitch bonded to the corresponding peripheral substrate conductor lines. This slightly odd mixed bonding procedure was necessitated by the unavailability of a ball bonder having sufficient throat clearance to allow execution of the necessary operations on the fully composed 10-inch-square area of the camera mainframe. Contacts on the mosaic, totalling 904 (including redundant substrate connections at its four corners), are split evenly between opposing pairs of parallel sides. Each emitter (column) section, one above and one below the mosaic, contains 250 connections. The two collector (row) sections, to the left and right of the array, have 200 connections each.

As seen through the foregoing discussion, the functional design for the 400-x-500 element engineering model integrated array camera, while not strictly adhering to all facets of a general approach, does follow good design practices regarding thermal dissipation, component density, in-process yields, and fabrication testing requirements. Due to the peripheral electronics being implemented as functional subassemblies designed to fit together on a common ground plane, the final system is both reliable (as a result of the minimal amount of rework punishment incurred during fabrication) and rework modifiable (because any of the substrate assemblies or the mosaic sensor can, if necessary, be removed and replaced without harm to the remaining circuitry).

Versatility of the system is further enhanced by the fact that it has been split into a primary scanner head section and a remotely locateable adjunct power converter section which can be altered or modified at will without endangering the master array scanning electronics of the camera. Further, to facilitate demonstration displaying of the camera and viewing of the internal structure of its LSHI circuitry, the mainframe has been fitted with a clear
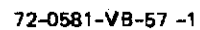
plexiglass protective cover plate to prevent inadvertent handling damage. Finally, a special, sectionally cut-away substitute camera housing cover panel is provided to satisfy the anticipated need to display the electronics layout while the system is in operation.

7.2 ELECTRICAL SPECIFICATIONS

During the initial stages of development on the engineering model 400-x-500 element Image Converter Of Radical Design it was realized that a clocking rate of 9.45 MHz necessary to make the system's output compatible with EIA standard US television monitors would not provide sufficient per-element sampling dwell time to fully read out and reset the elements in the array if interrogation was executed in the same manner as previous systems. It was subsequently concluded, after reviewing all the readout modes available, that proper readout conditions could be provided by a higher level scanning technique wherein successive elements are read out in time-shared over-lapping intervals. The fundamentals of this procedure are developed in Section 5.

A further constraint was then imposed that a minimum of cross-over lines between opposing sides of the array should be maintained. To do this requires that the scanning circuitry located along any given side of the array must be complete within itself except for master control lines. As a direct consequence of this, a moderate degree of redundancy is inherent throughout the resultant design. Reference to Appendix A, figure A-1 will point out the essential block diagram details of the system electronics which forms the 400-x-500 element camera. The physical layout format for the various subsections indicated within the camera mainframe is presented in figure 7-8. Table 7-1 contains a complete listing of the abbreviated names assigned to the program.

Master control of the system timing is provided by the MAT board (shown previously in figure 7-4). This board, whose detailed schematic is found in Appendix A, figure A-2, contains both the 9.450 MHz crystal clock and an

MAINFRAME

PERIPHERAL WIRING CHANNEL

| 1LM | 2φ5BBC | ½ – 64LD – 2 | ½ – 64LD – 1 | MT (PC) |

4BFR

BINMOS R | BINMOS L

M200C

10LD

½ 20LD 1 | HAN SUM | ½ 20LD 2

LEVCODE L | MOSAIC | LEVCODE R

LEVCODE R | LEVCODE L

½ 20LD 2 | HAN SUM | ½ 20LD 1

10LD

BINMOS L | BINMOS R | M200C

4BFR

2LM | DG (PC) | 1LM

½ – 64LD – 1 | ½ – 64LD – 2 | 2φ5BBC

INPUT/OUTPUT INTERFACE

72-0581-VB-57 –1

Figure 7-8. "45" PICTURE Camera Mainframe Substrate Layout

7-15

TABLE 7-1

SCHEDULE OF PROGRAM ABBREVIATIONS

MAT	-	MAster Timer
GATE	-	delay GATE (s)
2∅5BBC	-	2∅ (phase) 5 Bit Binary Counter
M200C	-	Modulo 200 Counter
4BFR	-	4 Bit Folded Register
64LD	-	64 Line Decoder
20LD	-	20 Line Decoder
10LD	-	10 Line Decoder
LEVCODE	-	LEVel COnverter DEcoder
BINMOS	-	BIpolar decoded N-channel MOS
HANSUM	-	Hybrid ANalog SUMmer
1LM	-	1(st) Level Multiplexer
2LM	-	2(nd) Level Multiplexer
VIPOR	-	VIdeo ProcessOR
"45"	-	"400-by-500" element sensor
PICTURE	-	Photon Image Converter with Television Universalized REsolution

Apollo lunar camera type Westinghouse digital synchronization generator (pictured in figure 7-9); plus a divide-by-twelve counter, two divide-by-two J-K binary flip-flops, and the necessary gating to allow injection of an external clock. Quite naturally, only one unit of this kind is deployed in the camera. The gate board (included in both figures 7-4 and A-2) is also a one-of-a-kind layout. Functionally this board performs the task of delaying the clocking triggers to the 4-bit "D" registers on the 1LM substrates (see figure A-8) so as to open up contiguous 212 nanosecond signal sampling windows during the sensor output signal peak intervals. These two
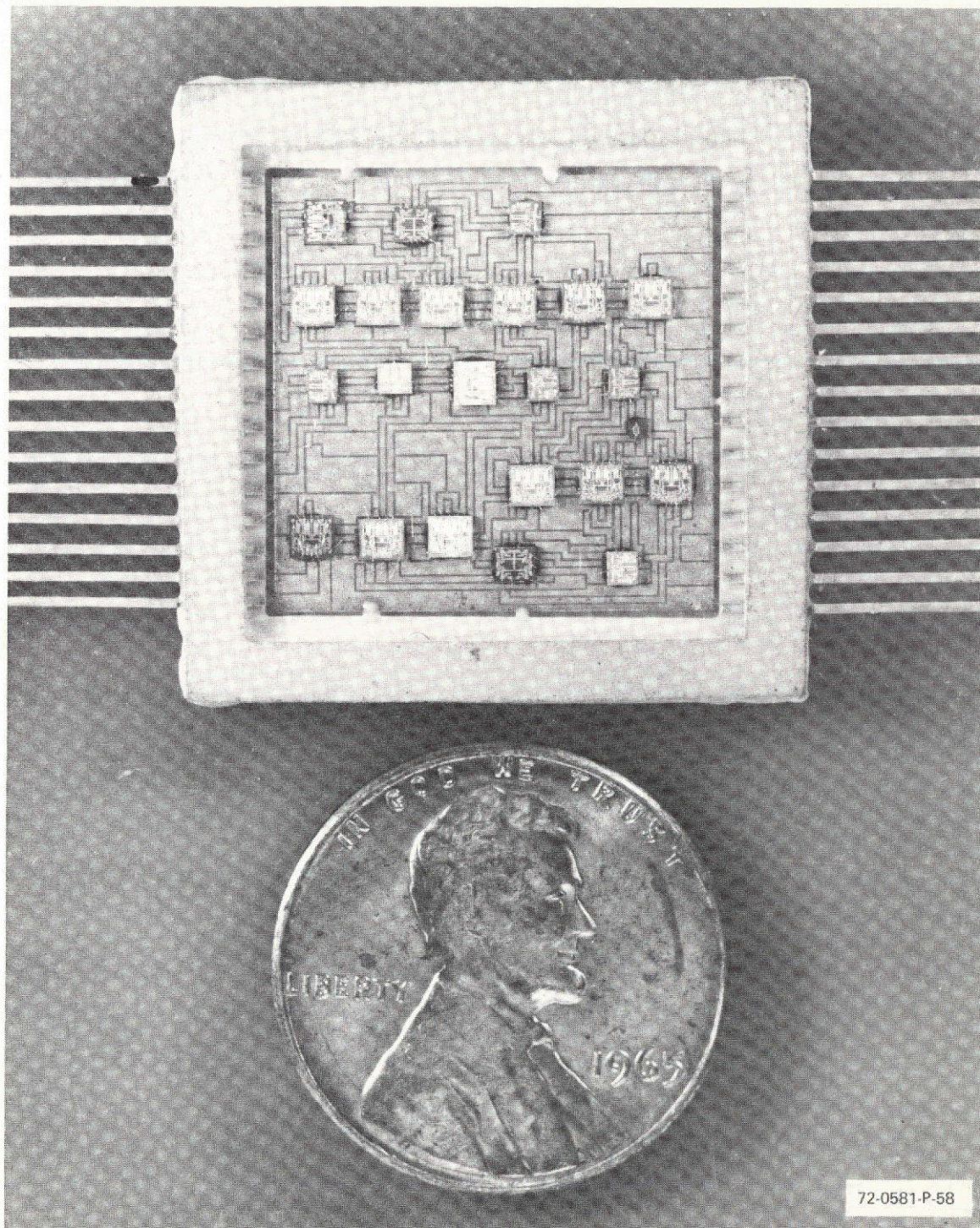
72-0581-P-58

Figure 7-9. Westinghouse EIA TV Format Digital Sync Generator

multiplexers reduce the eight parallel data streams (four each) from their associated HANSUM substrates (also shown on figure A-8) to two overlapping time period video streams before sending them along to the 2LM substrate of figure A-9.

In this final level of multiplexing the sequential application of a 106 nanosecond sampling window alternately between the two remaining parallel data streams combines them into a single serial output data stream which is passed out of the camera mainframe to the subunit processor through the I/O connector (figure A-10). Time positioning of the sampling window is facilitated by two additional controllable delay and gate blocks on the GATE board which are fed by the previously delayed 1LM register clocking pulses used in generating the first level multiplexing double-length windows. The complete delaying operation on the GATE board consists of two distinct stages with two delay gates per stage so that both a delaying and a squaring-up operation can be performed on the respective clocking pulses.

Comparison of the circuitry in the 1LM and 2LM sections will show that basically the same circuitry techniques are employed in each. Sampling is carried out in the manner of a shunt ac clamped chopper followed by sufficient amplification to overcome divider losses suffered in sampling. Maintenance of correct static or average operating levels with these dc coupled circuits is facilitated by a gated feedback loop which is activated during the normal interface retrace and synchronization periods.

It will be noted, however, that slightly different amplifier arrangements are provided on the 1LM and 2LM substrates. In particular, a fixed gain is instituted following the first multiplexing operation whereas the second level of multiplexing is followed by an amplifier whose gain can be varied. This provision was made to allow setting of the final input signal to the EIA video formatting board to a level just sufficient to produce 100 percent "white" modulation for sensor signal levels just slightly below the average sensor element saturation point. The dynamic range of the entire analog processing

chain is then set such that overamplitude shorted element video will be clipped and be considerably less objectionable than was the case in former camera system image outputs.

Note, however, that this arrangement does not replace the usual defective white spot with a black spot (or, more accurately, a hole in the raster). As was done by the innovative bright-spot-blanker circuits that were retrofitted into the 100-x-128 and 200-x-256 element image converters. The reason for this modified scheme is simply a matter of response speed. With the two former systems one sensor element readout period was, at the very least, around 1 microsecond. That meant that 100 nanoseconds of inherent delay in the attack and/or recovery of the trigger circuit used in the BSB electronics was of little consequence. On the other hand, in the 200 K element system sequenced at 30 frames per second, the final, fully seriallized per-element data interval is only 106 nanoseconds (i.e., the period of the master 9.45 MHz clocking signal). Here it is quite apparent that even a 30 or 40 nano-second slip in the response of the overamplitude signal control device could prove significant.

From a check of the VIPOR schematic (figure A-9) it will be observed that this final processor combines the separate analog imager video and digital mixed blank and composite sync signals into a composite EIA standard TV style video signal having a ratio of 5:2 between the peak video and peak sync signal amplitudes. Outputs from the unit are provided in both positive and negative polarity (180 degree phased complimentary) form to facilitate interfacing with any monitor, regardless of which polarity signal it may require at its input. The amplitude of the signals available from the processor, when terminated into a 75 ohm coaxial cable, will be fixed at about 1 volt peak video and 0.4 volt peak sync tips. Limited adjustment of these levels can be made by appropriate pots in the processor electronics.

Reference back to the system block diagram at this point will reveal that the foregoing discussion has delt solely with the analog signal handling

electronics employed in the PICTURE "45" camera to acquire and process the scan converted photon image intelligence from the 400-x-500 element mosaic. It now remains to discuss the manner in which the various counting and decoding circuits function, and how they are interrelated in initiating and managing proper scan sequencing within the system.

To produce the distinctive overlapped sequential pulses entailed in multiplexed commutation of the 400-x-500 element array, a slight departure from normal logic design practices was necessary. In particular, the column sequencer counting operations are instituted by phased clocking of two pairs of 4BFR and 2Ø5BBC substrates, the circuitry for which is shown in figure A-3. Initiation of the basic eight phases of time-shared overlapping selection pulses is facilitated by feeding complimentary 4.725 MHz clock phases to two four-bit folded registers (sometimes referred to as twisted-tail ring counters), one on either side of the mosaic (see figure 7-8). The odd and even output pulse trains from these registers appear as waveforms a, b, c, and d (appropriately subscripted) in the timing diagram of figure 7-10. Also indicated here is the basic form of the outputs from the dual-phase synchronous counters which have a built-in cycle control feature.

Controlled cycling in this instance refers to the provision that is made for allowing an automatic internal stoppage of their counting function once they have completed a full count sequence cycle. After this lock-out has occurred, an external initiate or "enable" gate (referred to as an inhibit/reset pulse on the timing diagram) must be input to the counter before another counted through cycle can take place. To facilitate complete, nonextraneous decoding of 256 time periods from each of the 4BFR's (odd and even), both consociate 2Ø5BBC substrates consist of two 90 degree shifted-phase binary counters. Their outputs are so related that one counter is used to decode the true output intervals from a register while the other is used to decode the negation (or compliment) intervals — hence the subscripts T and N on waveshape A through E in figure 7-10.
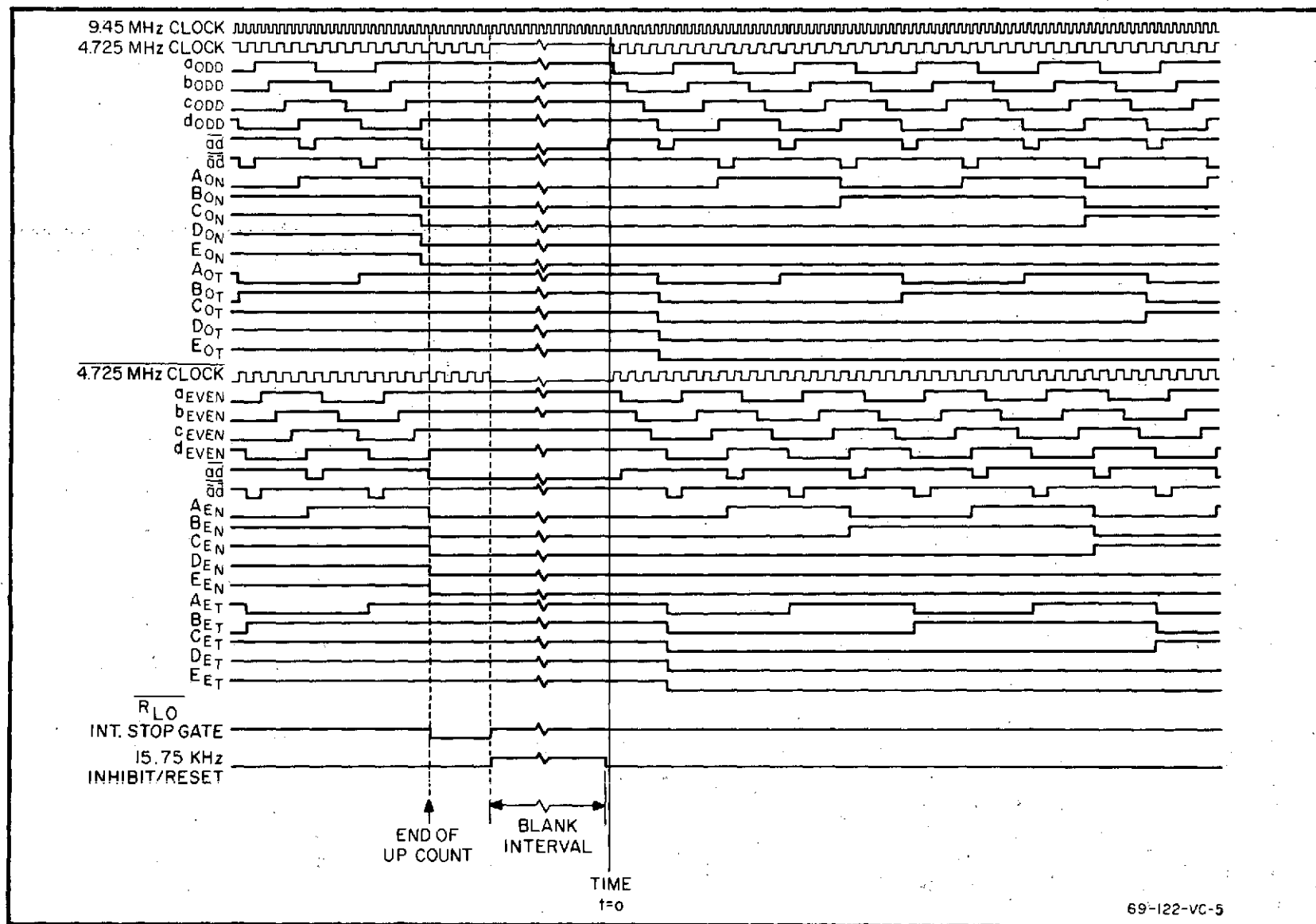
Figure 7-10. Column Counter Timing Diagram

The actual decoding functions are carried out in a fairly straightforward manner in two levels by commercially available TTL logic elements. First level decoding of the two 2∅5BBC outputs is performed on two 64LD substrates (for which the circuitry is presented in figure A-4), each of which contains a bank of four one-of-sixteen decoders. Outputs from these decoder blocks are sent through a follow-up band of hex inverter chips so that they will be of the proper polarity when passed to the final level of decoding on the BINMOS substrates (figure A-7). The process of overlap time-shared sequencing of successive sensor array columns and commutation of every eighth column (every fourth out either side of the matrix) is then completed on the BINMOS substrate through a bank of 2-input NAND gates, which are again followed by "reinversion" hex's to correct their polarity for proper gating of the n-channel MOS-FET line switching devices. A point to note here is that had NOR gates (in the low power TTL line) been available at the time the system design was finallized, it would have been possible to eliminate both bands of hex inverters used for polarity correction in the above decoding operations. These gates are now available and can be used in future systems if desired to realize significant savings in both power consumption and physcial size of the system electronics layout.

A similar, although less complex, sequence of operations is carried out in the row address sections of the camera. Drive voltage sequencing to the collector rows progresses in a normal, contiguous, edge-to-edge manner with no overlap as provided by conventionally designed counter/decoder electronics. Since there are a total of 400 collector rows split evenly with access to alternate odd and even ordered groups of 200 coming out either side of the matrix, and, further, since they are to be sequenced in an interlaced manner with all odd and then all even numbered rows sequentially selected, two M200C substrates (figure A-3) having cycle control provisions are all that is needed to generate the required scanning signals. Controlled cycling in this case, while internally similar to that described for the 2∅5BBC

7-22

substrates, serves to select which bank (odd or even) of the mosaic collector rows is being sequenced during alternate interlaced TV type fields.

First level decoding of the outputs from either of the M200C units is accomplished by an associated pair of 1OLD and 2OLD substrates like those shown in figure A-5. As in the column sequencing decoders, follow-up "reinversions" are included to correct the polarity of the initial decoder outputs. Final level decoding and collector row address driving is then provided by the LEVCODE substrates (see figure A-6) which contain the same basic types of gates as were found on the emitter interface substrates. In the decoding operations in both sections, an extra enable (inhibit) input from the MAT board is employed to prevent a line from being selected during the interline or interframe retrace intervals and thereby destroying the information available from it.

7.3 SYSTEM OPERATION

The operating procedures to be followed with the engineering model 400-x-500 element integrated array camera are quite simple and few precautions are necessary. Below are listed the main items to be aware of.

7.3.1 General Operating Instructions

To initiate operation, follow this sequence of steps:

a. Affix the supply/processor subunit directly to the camera mainframe, or interconnect it through the appropriate length cable for remote operation.

b. Position the camera on the tripod for stable maneuvering and swiveling around a given scene area, or attach carrying handle for mobile operation.

c. Ensure that power switch is in OFF (center position of three way toggle) and plug in power cord from supply/processor module to source of 110 Vac, 60 Hz, 1 phase primary power.

d. Connect a BNC terminated 75 ohm coaxial cable from the correct polarity output jack to the input of a standard TV studio type monitor.

e. Energize the monitor and allow it to warm up.

f. Throw power switch on the system's supply/processor unit to its ON-INT position.

g. Adjust lens aperture and focus settings for best appearing image on monitor.

The primary precautions to exercise under normal operating conditions are to avoid extending viewing of the sun or extended operation in environments exceeding an ambient of 30°C, and to avoid subjecting the system to undue G-force shocks. While reasonably sturdy mountings have been provided, no exact spec's have been placed on the shock resistance of this developmental system.

7.3.2 Removal and/or Change of Cover Plate

If it is desired to remove the mainframe chassis cover plate for viewing of the internal electronics layout or to convert over to the cut-away cover for operational display, the following procedure should be used:

a. Deenergize system and remove all power and monitor cabling.

b. Remove system from tripod and lay flat on a workbench or table top.

c. Remove the lens and lay aside for protection.

d. Remove the four retainer screws in the four corners of the cover plate and lift it straight up and away from the chassis.

e. Direct observation can now be made of the internal system electronics.

> CAUTION: The unit should not be left in this condition
> without placing a cover plate over the hole in the
> protective plexiglass panel, since damage to the sensor
> array can result.

f. Replace the coverplate by reversing the above steps, or preceed to step g if the cover plate is being changed.

g. Remove the four circular lens mount bracket retaining screw/nut combinations and drop bracket out from under cover.

h. Place lens mount bracket under alternate cover plate and, with decorative faceplate piece in position, attach by inserting the four screw/nut retainers.

i. Install new cover plate by reversing steps a through d above. The only additional precaution here is that no attempt should be made to probe into the internal electronics while the cover plate is off, and the plexiglass protective panel should not be removed as inadvertent damage can too easily follow.

If improper operation is encountered it is suggested that the manufacturer be contacted regarding corrective measures.

8. SUMMARY AND CONCLUSIONS

A period of approximately 10 years has been spent in the development of a solid-state imaging system capable of TV quality resolution. This effort has brought about the perfection and adaptation of many advances in solid-state technology. The mosaic itself is an outstanding example of large scale integration. This is, of course, obvious when one considers the fact that there are 200,000 active elements packed into a 1 square inch area. Line and spot defects still create the largest problem, but are amenable to correction. Steadily improving photomask making procedures continue to reduce the number of defects per plate. Handling and processing techniques continue to improve to eliminate defects caused by dust, dirt, or mechanical abuse. Furthermore, the silicon material used is continually being made more and more defect free. These factors plus the extensive experience accumulated indicate that it is now possible to produce mosaics of significantly greater quality. This, plus improvements in signal processing, make it possible to design and fabricate usable solid-state camera systems with TV quality resolution.

There are a number of applications which require medium levels of resolution. Systems of this type can be readily fabricated with a high degree of form factor freedom. Circuit design and implementation have reached a degree of sophistication which enables the systems user a large degree of freedom in the area of electronics format and form.

It only remains for a significant number of systems to be fabricated to demonstrate that the cost of an all solid-state imaging system can be

brought to a level below that of any other type of imaging system. In addition, these more economical systems will have those solid-state virtues so important to cost effective operation:

- Light weight
- Low power requirements
- Low voltage requirements
- High reliability
- Long lifetime
- Ruggedness
- Very long shelf life.

For those applications needing these attributes, the solid-state camera is an excellent answer.

APPENDIX A

PICTURE 45 CAMERA
SCHEMATIC DIAGRAMS
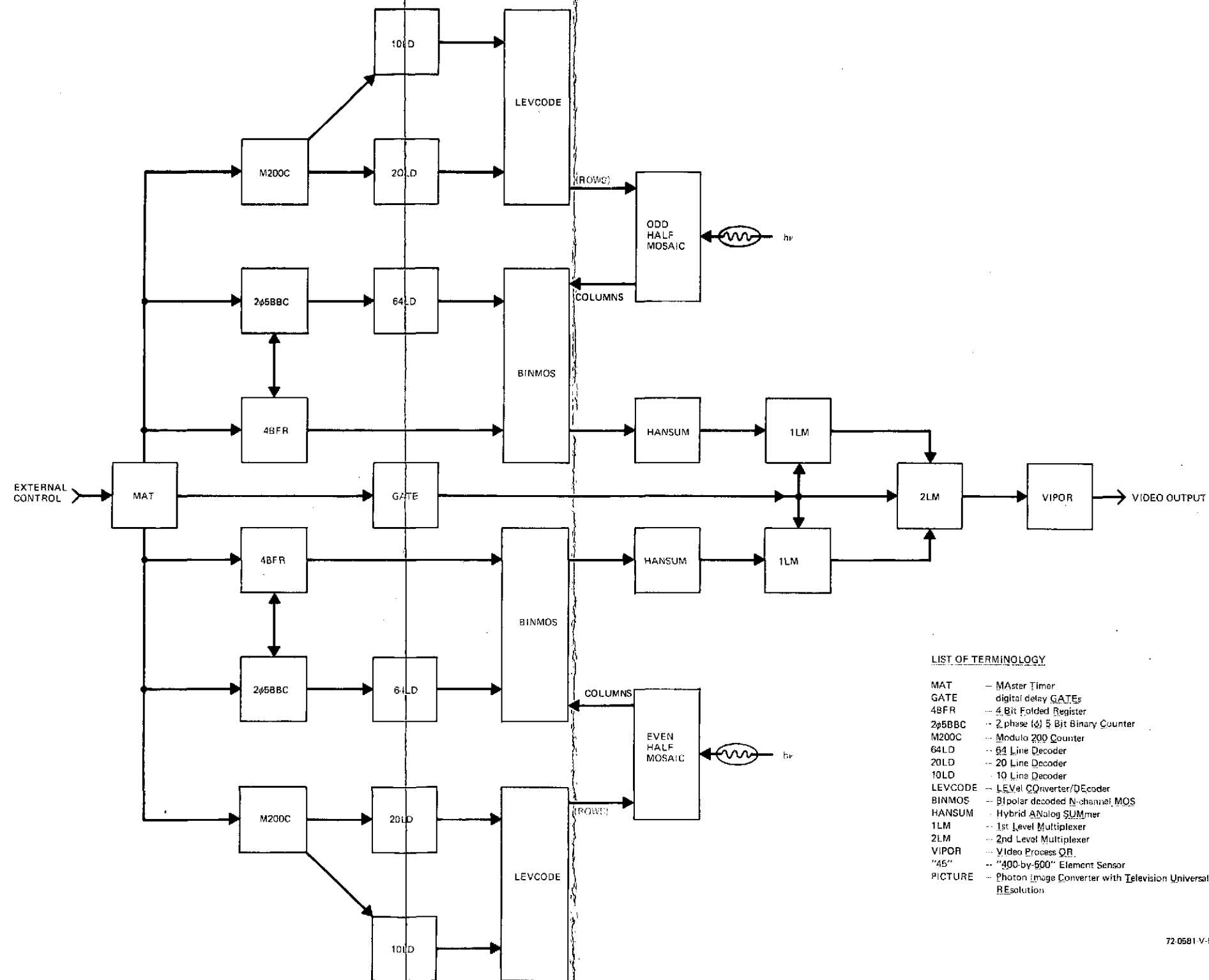
LIST OF TERMINOLOGY

MAT	— MAster Timer
GATE	— digital delay GATEs
4BFR	— 4 Bit Folded Register
2φ5BBC	— 2 phase (φ) 5 Bit Binary Counter
M200C	— Modulo 200 Counter
64LD	— 64 Line Decoder
20LD	— 20 Line Decoder
10LD	— 10 Line Decoder
LEVCODE	— LEVel COnverter/DEcoder
BINMOS	— BInary decoded N-channel MOS
HANSUM	— Hybrid ANalog SUMmer
1LM	— 1st Level Multiplexer
2LM	— 2nd Level Multiplexer
VIPOR	— VIdeo Process OR
"45"	— "400-by-500" Element Sensor
PICTURE	— Photon Image Converter with Television Universal REsolution

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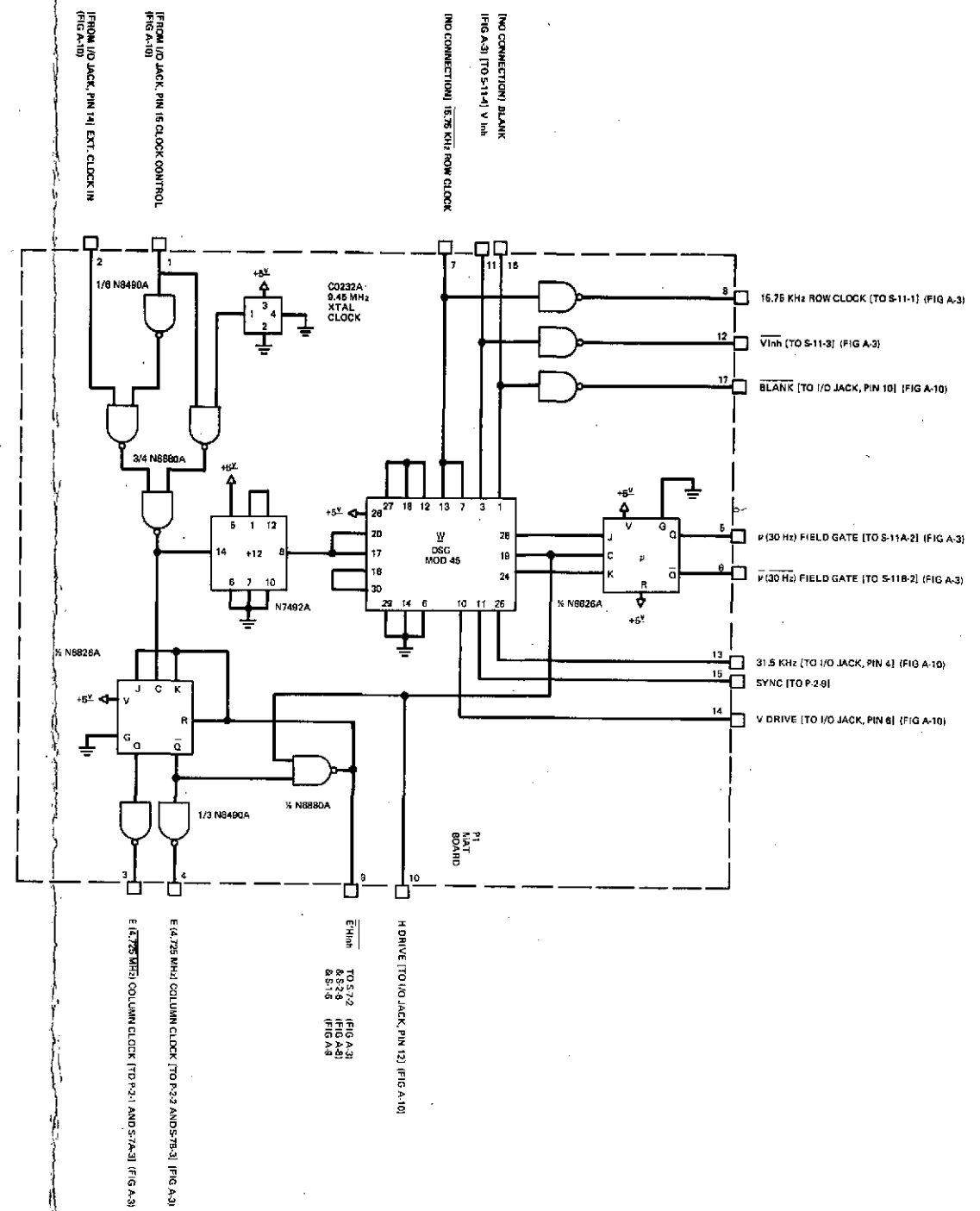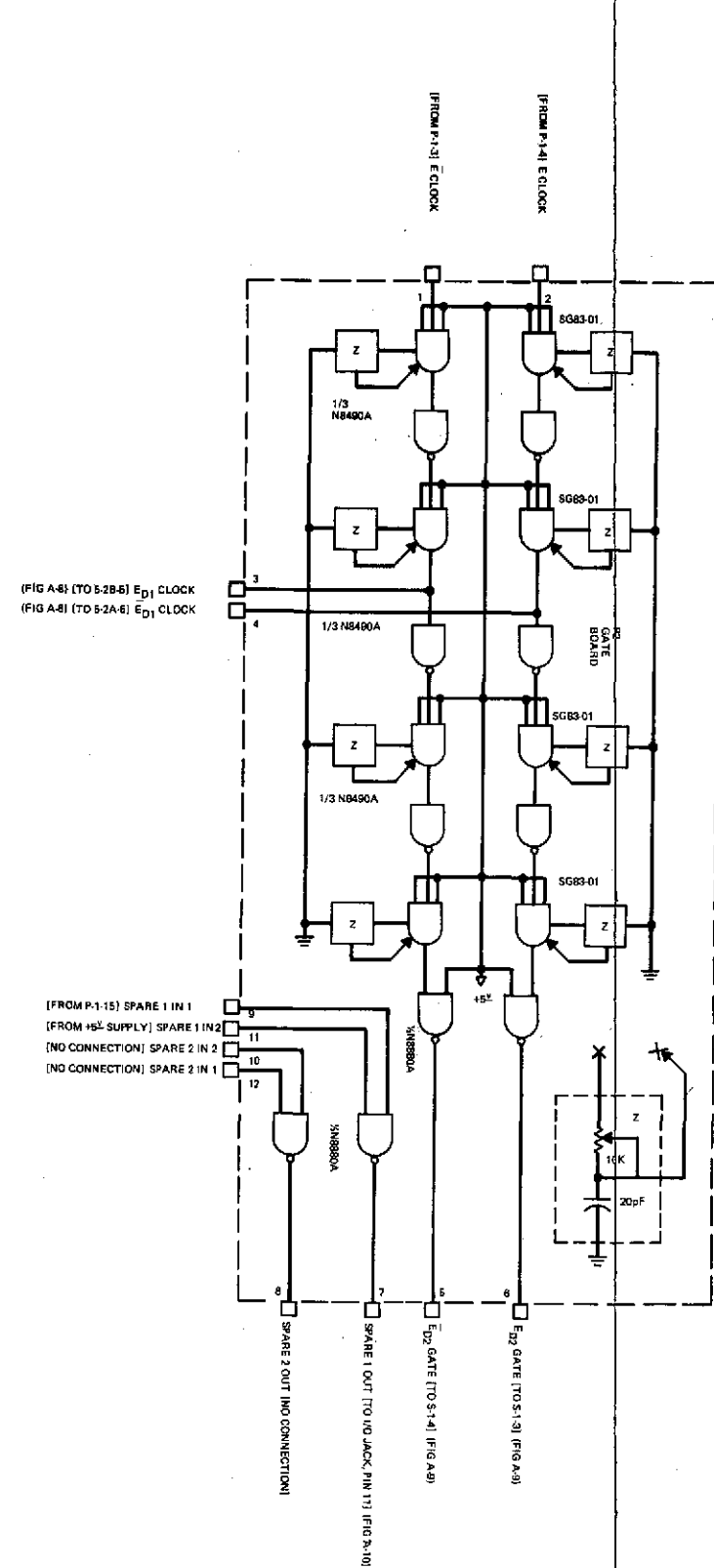Figure A-1.   Signal Flow System Block Diagram

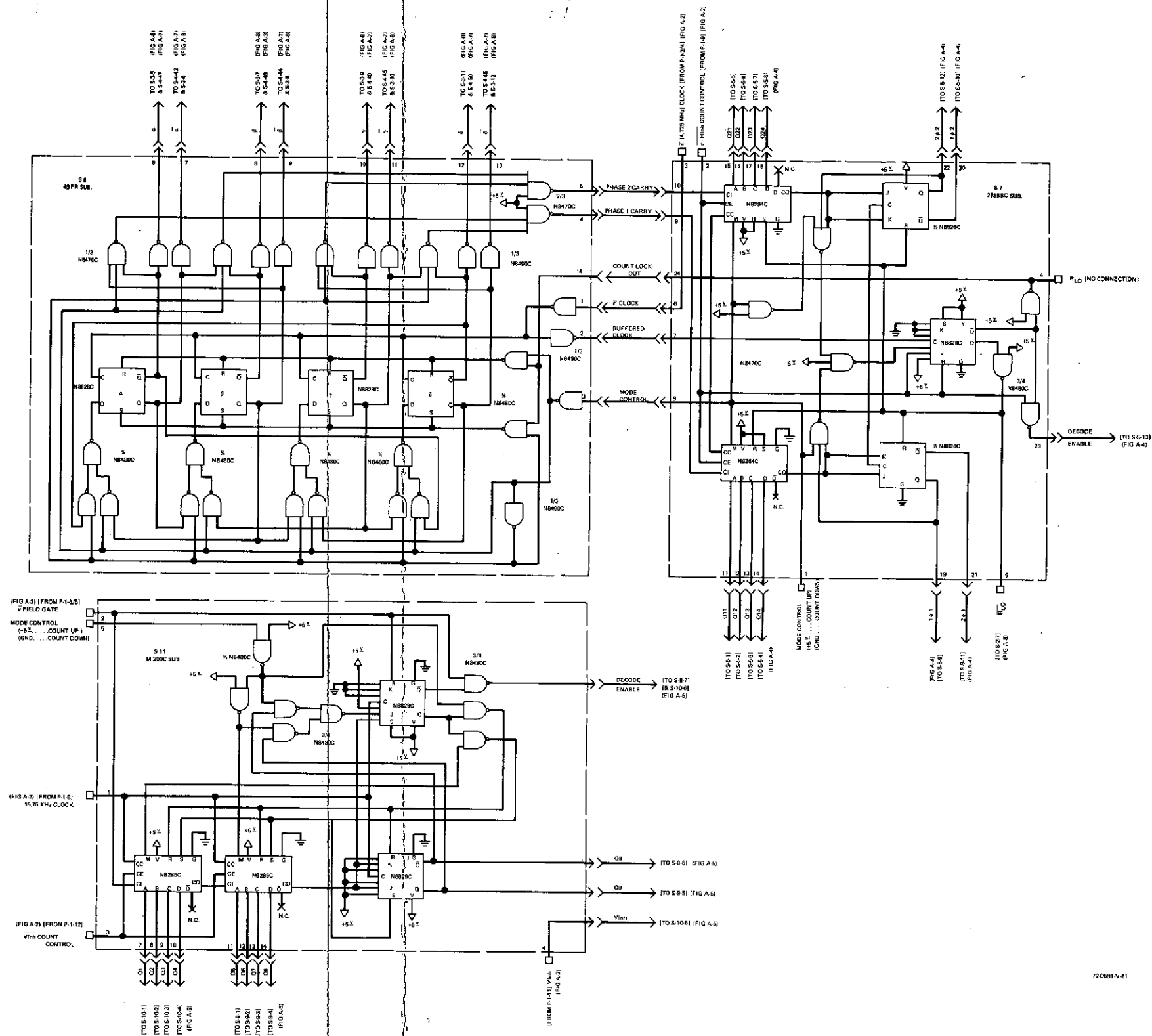Figure A-2. Master Timing and Gating Electronics

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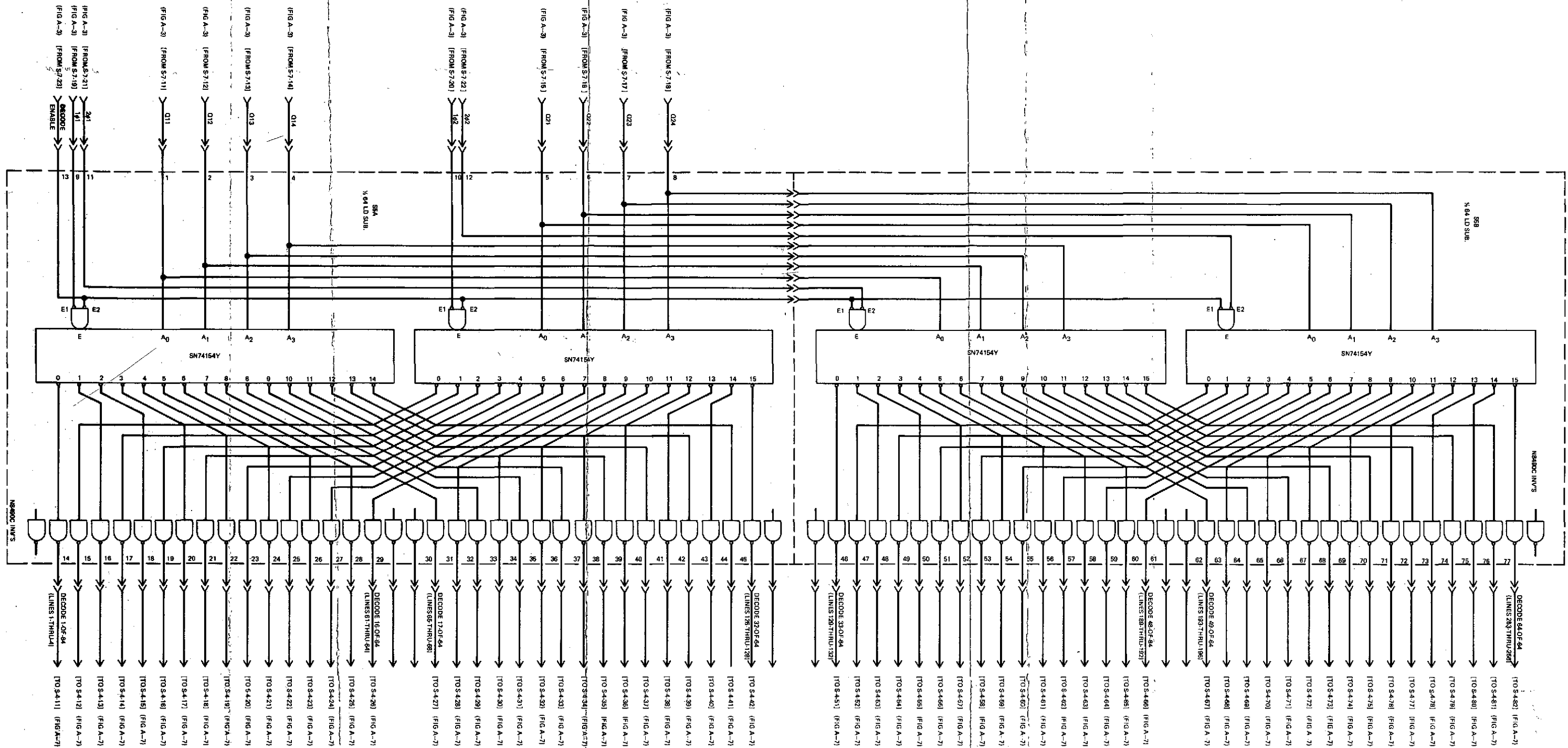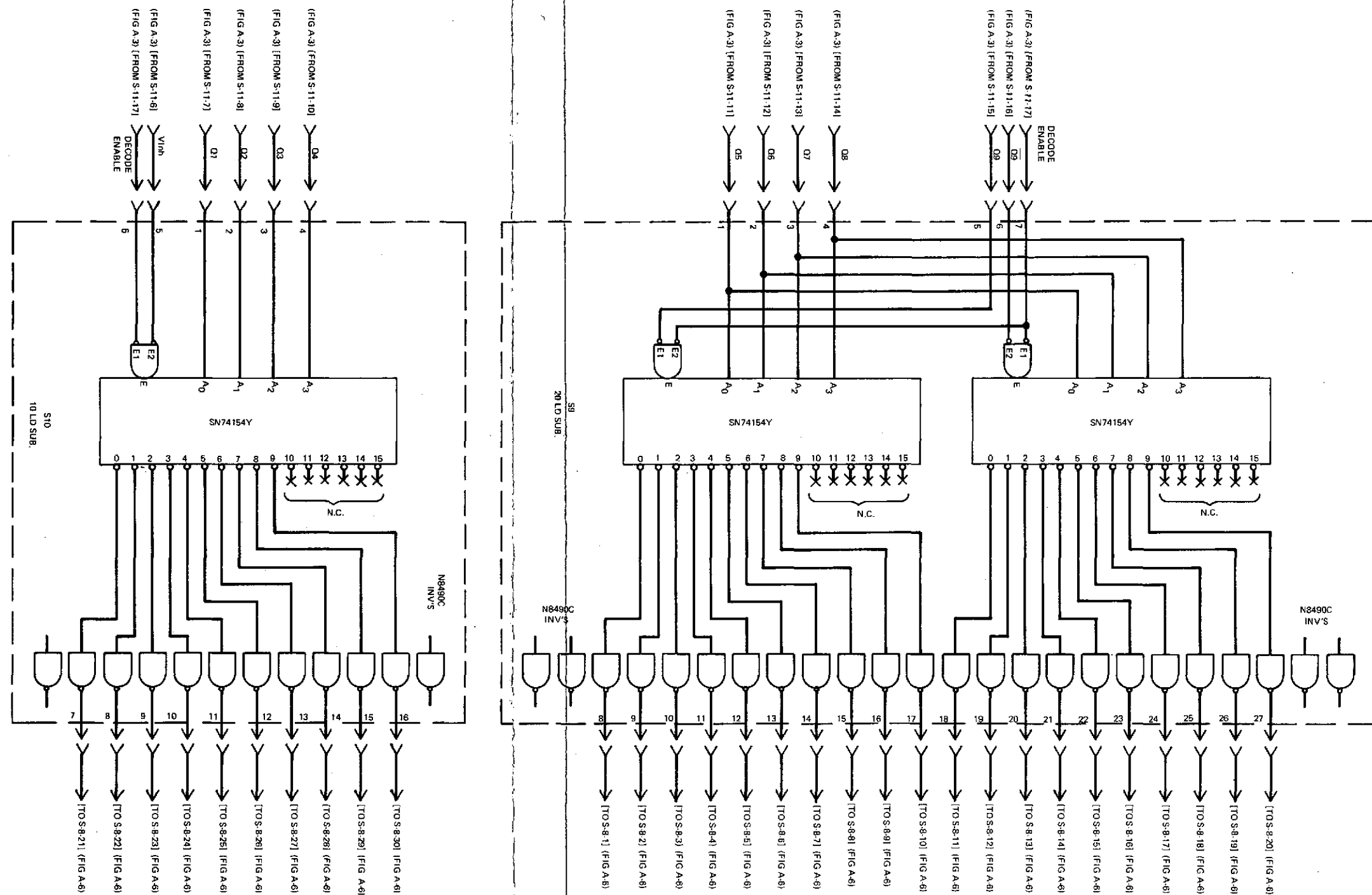Figure A-3.   Time-Shared Column Counter and Interlaced Field
Row Counter Electronics
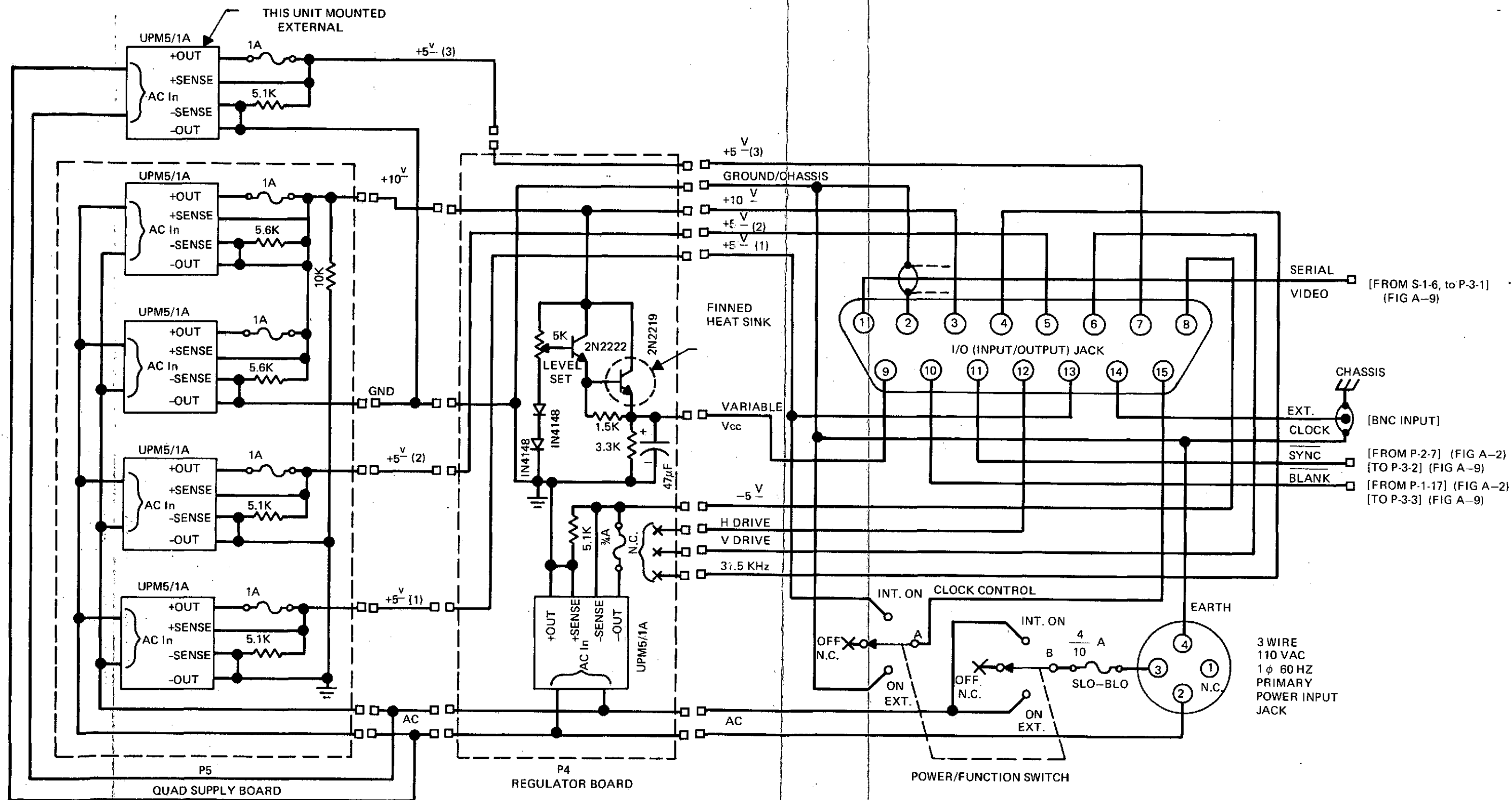
Figure A-4. First Level Column Decoder Electronics

Figure A-5. First Level Row Decoder Electronics

A-11

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Figure A-6. Final Level Row Decoder/Array Driver Electronics

A-13

Figure A-7. Final Level Column Decoder/Signal
Commutator Electronics

Figure A-8. Signal Acquisition and First Level Video
Multiplexing Electronics

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Figure A-10. System Power Supply Subunit Circuitry

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