DESIGN, PROCESSING, AND TESTING OF LSI ARRAYS FOR SPACE STATION

BY

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16. Abstract

The objective of this research program continues to be the development of a low-power, high-performance metal-oxide-semiconductor (MOS), 256-bit random access memory (RAM) with beam leads. Support has previously been made available to develop an aluminum-gate current-sense version and a silicon-gate voltage-sense version of this memory. Both types of devices performed very well, which resulted in the present effort to make a silicon-gate unit with beam leads. The beam lead process on bulk silicon wafers is fairly well standardized but not easily transferred to silicon-on-sapphire (SOS). Beam-lead process development on SOS is discussed, and initial electrical results on beam-lead SOS TA5388 devices are presented. A comparison of the beam-leaded 256-bit RAM (TA6567) layout is made with the non-beam-leaded version (TA6473).

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DESIGN, PROCESSING, AND TESTING OF LSI ARRAYS FOR SPACE STATION

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SUMMARY

The objective of this research program continues to be the development of a low-power, high-performance metal-oxide-semiconductor (MOS), 256-bit random access memory (RAM) with beam leads. Support has previously been made available to develop an aluminum-gate current-sense version and a silicon-gate voltage-sense version of this memory. Both types of devices performed very well, which resulted in the present effort to make a silicon-gate unit with beam leads. The beam lead process on bulk silicon wafers is fairly well standardized, but not easily transferred to silicon-on-sapphire (SOS). Beam-lead process development on SOS is discussed, and initial electrical results on beam-lead SOS TA5388 devices are presented. A comparison of the beam-leaded 256-bit RAM (TA6567) layout is made with the non-beam-leaded version (TA6473).

I. INTRODUCTION

RCA's silicon-on-sapphire research and development program includes materials and basic device research, computer-aided circuit design, mask-making techniques, and advanced CMOS array design using Large Scale Integration (LSI).

Previous circuit design efforts using silicon-on-sapphire (SOS) process techniques have resulted in a 256-bit aluminum-gate current-sense random access memory (RAM). Further developments involved the inclusion of silicon-gate technology and addition of a tri-state voltage-sense amplifier. The latter version of the memory has performed almost exactly as intended in the design.

The present phase of this project is to develop a low-power, high-performance metal-oxide-semiconductor (MOS), 256-bit random access memory (RAM) with beam leads. The development of beam-leaded SOS technology has combined the standard SOS process with a modified microbridge beam-lead process. The mechanical feasibility of this technology has been demonstrated using as the test vehicle the dual complementary plus inverter circuit (TA5388). This circuit was fabricated on SOS and metallized using the beam-lead base metal and gold beam technology; it was then laser-scribed, separated, and bonded to a standard 14-lead ceramic DIP.

Subsequent efforts have been to improve the beam-lead processing and to establish the electrical base line data for the beam-lead CMOS/SOS devices using the TA5388 circuit.

Along with this effort, the 256-bit RAM (TA6567) circuit was redesigned for beam leads and is currently being processed.

II. BEAM-LEAD PROCESS DEVELOPMENT

The beam-lead SOS process conveniently lends itself to electrical evaluation, both before and after the formation of the gold beams. The approach has been to merge the standard self-aligned silicon-gate SOS/CMOS process with the bulk beam-lead process using a modified microbridge technology to form the beams as was described in Quarterly Technical Report No. 11.

The beam-lead process evaluation is to be made in these phases. First, the base-metal evaluation can be done by comparing the electrical results of wafers with base-metal replacing the standard aluminum metal, both having a Si_3N_4 passivation layer covering the entire device. The second evaluation can be made on the same wafers with the base-metallization used in phase one after the gold beams are formed. Finally, the same circuits can be evaluated after scribing, separating, and bonding the chip to the ceramic substrate.

The adaption of the base-metal process to SOS is complete; the initial electrical results on the TA5388 circuit for this phase with Si_3N_4 passivation are discussed in another section. Problems of reproducibility and stabilization of the electrical properties of the devices with base-metal, as reported in Quarterly Report No. 12, were resolved by correcting a mask error. The error caused the MOS device to have a dual-gate structure, i.e., both a polysilicon gate and metal gate, with the potential of the polysilicon gate floating. A 2000-Å-thick Si_3N_4 passivation layer deposited by CVD and chemically etched is used for protection against contamination during the beam-lead processing. The parameters of this layer (Si_3N_4 thickness, method of deposition, and method of etching) for stabilization of the electrical device characteristics have not been completed because of the mask error.

The major process development is being focused on the gold beam and pillar formation. The problem is the adhesion of the thick photoresist to the copper layer to obtain good etching of the pillar opening and sharp definition of beam and pillar during the subsequent gold-plating step.

Wafers with the TA5388 circuit and wafers with the TA6567 circuit have been processed through beam formation. The initial electrical results on the beam-leaded TA5388 devices are discussed in Section III, and the TA6567 circuit is described in Section IV.

III. INITIAL ELECTRICAL RESULTS ON BEAM-LEADED TA5388 DEVICES

Both NMOS deep-depletion mode and PMOS enhancement mode transistors on the TA5388 circuit were successfully fabricated using the standard silicon-gate process with the aluminum metal replaced by the Ti/Pd/Au beam-lead base metal. The electrical characteristics of the transistors with the beam-lead base metal were similar to those with aluminum metal. The electrical instability previously reported was caused by a mask error and has been corrected.

The data presented here cover the initial electrical wafer-probe measurements on the devices in the TA5388 circuit before and after gold beam formation. The values for the device parameters are to be considered only as an indication of the current beam-lead SOS processing state of the art and not as typical values. At this time, the beam-lead processing steps are fairly well defined, and the electrical test results will be used to optimize the processing. The values for typical base line electrical parameters will then be stated.

Figure 1(a) shows the I-V characteristics for both the PMOST and the NMOST (origin in lower left corner of the figure) after the beam-lead base metal step. For comparison, Figs. 1(b) and (c) show the same curves after the gold beam step for the PMOST and the NMOST, respectively. These curves are typical of the devices on this wafer before and after beam formation.

Histograms comparing the threshold voltages before and after beam formation for the PMOST and NMOST are shown in Figs. 2 through 5. The ordinate is normalized to the number of readings in the histogram cell with the largest population. The abscissa is divided into 100 cells and the units are in volts. Table I lists the 'mean' values for V_{TH} shown in the histograms.

Table I

Threshold Voltage

	PMOST (V)	NMOST (V)
After Beam-Lead Base Metallization	-0.71	1.16
After Gold Beams	-1.02	0.73

The values in Table I indicate a negative shift in V_{TH} for the PMOST and NMOST of 0.31 V and 0.43 V, respectively. The cause of this

(a)

(b)

(c)

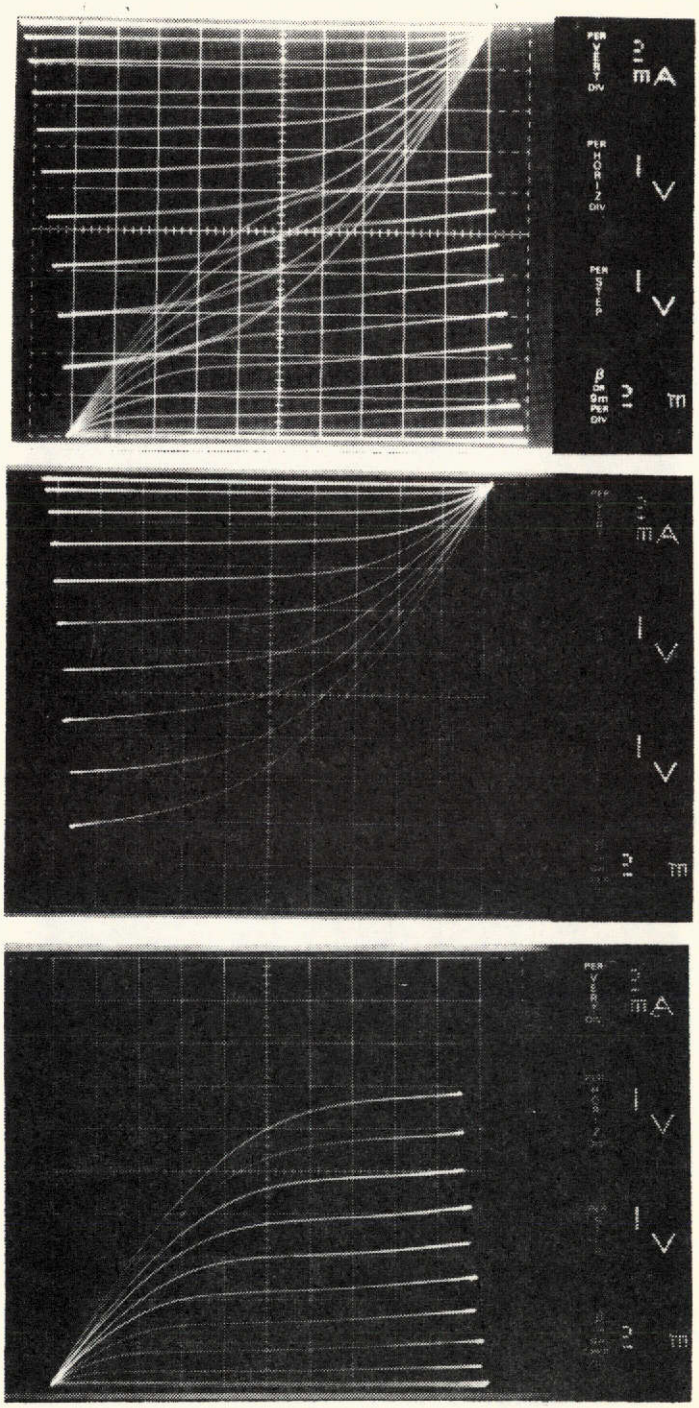

Figure 1. I-V characteristics of beam-leaded TA5388 devices before and after gold beam formation. (a) PMOST and NMOST after beam-lead base metallization, (b) PMOST after gold beams, and (c) NMOST after gold beams.

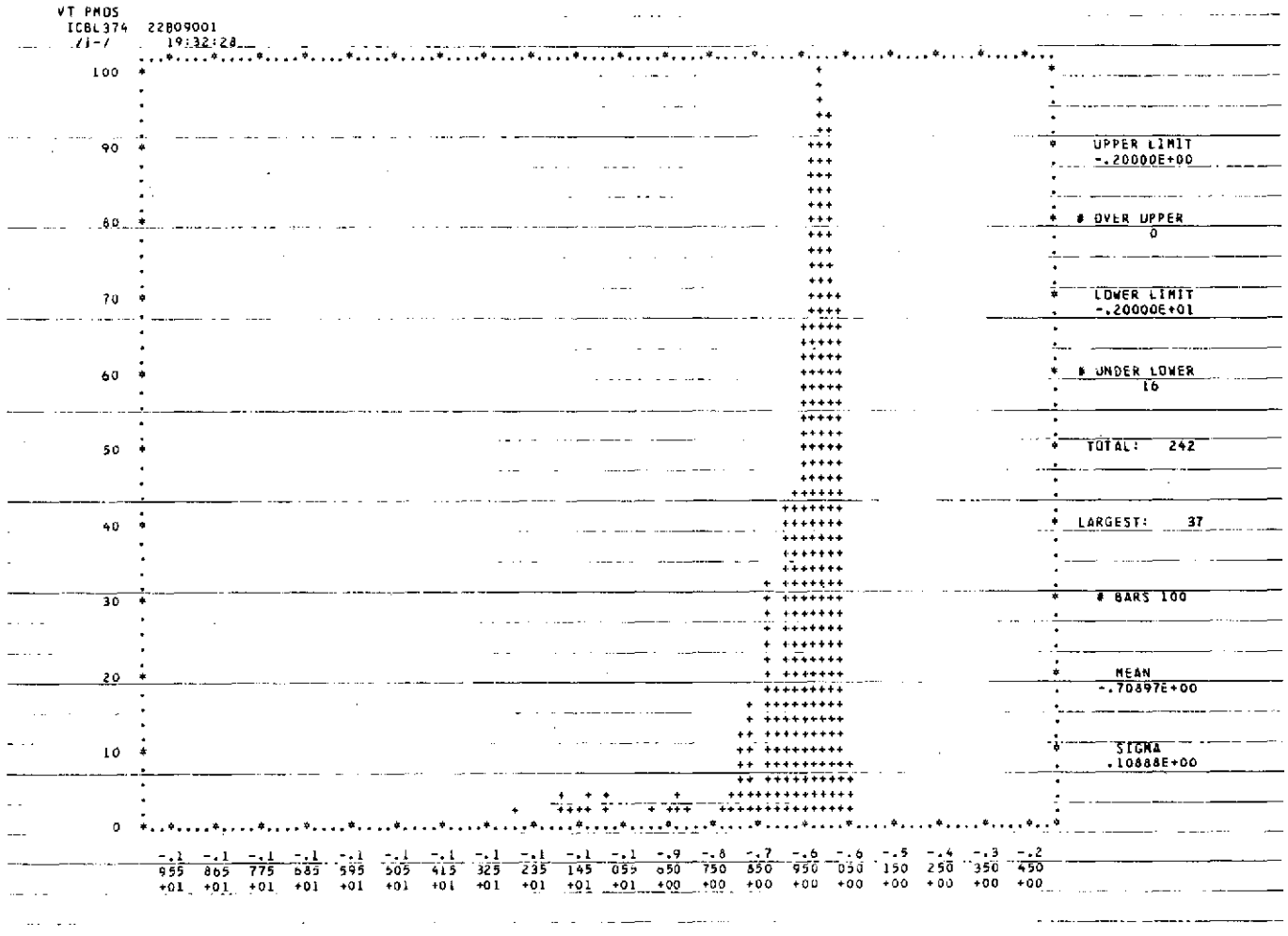

Figure 2. Histogram of TA5388 PMOST V_{TH} after beam-lead base metallization.

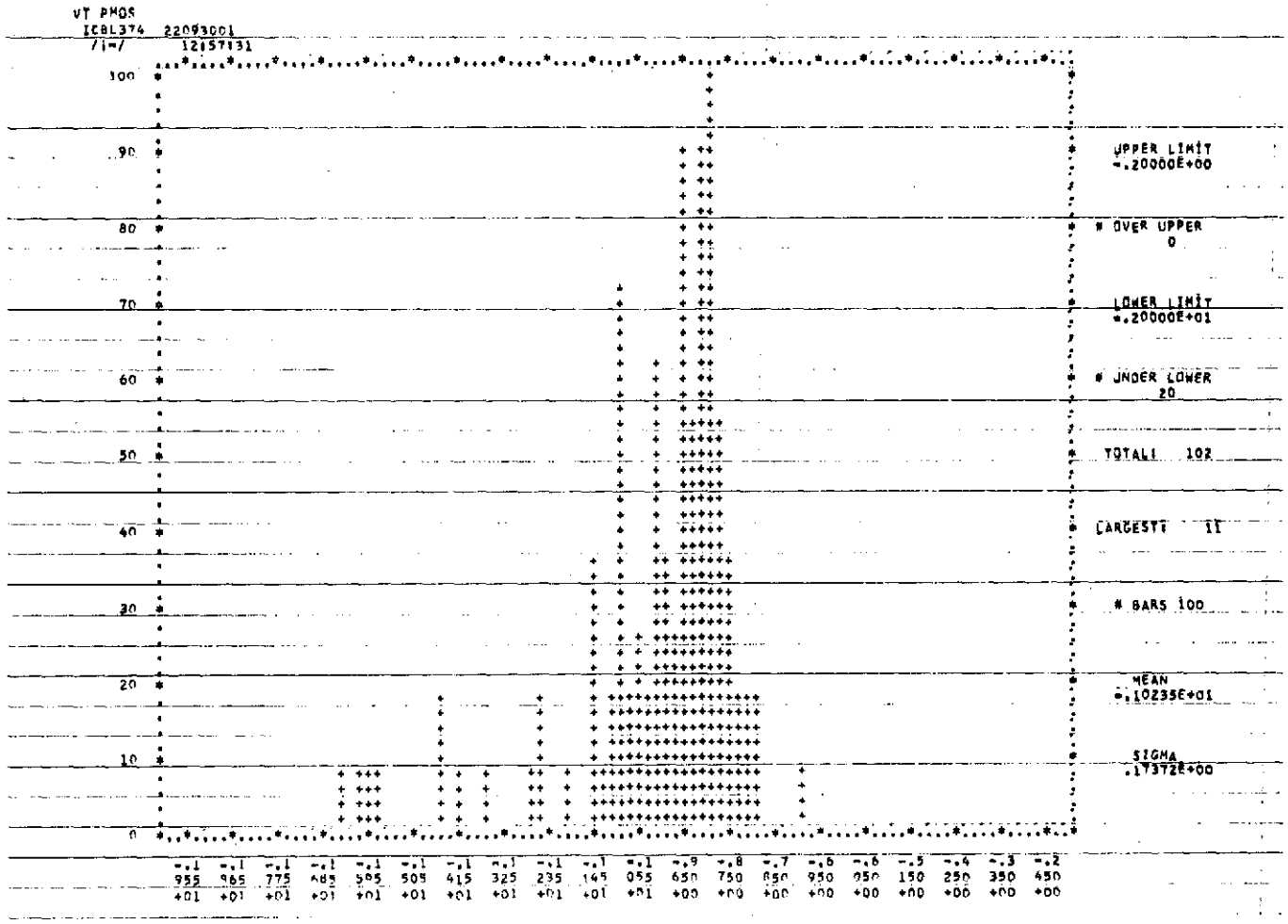

Figure 3. Histogram of TA5388 PMOST V_{TH} after gold beams.

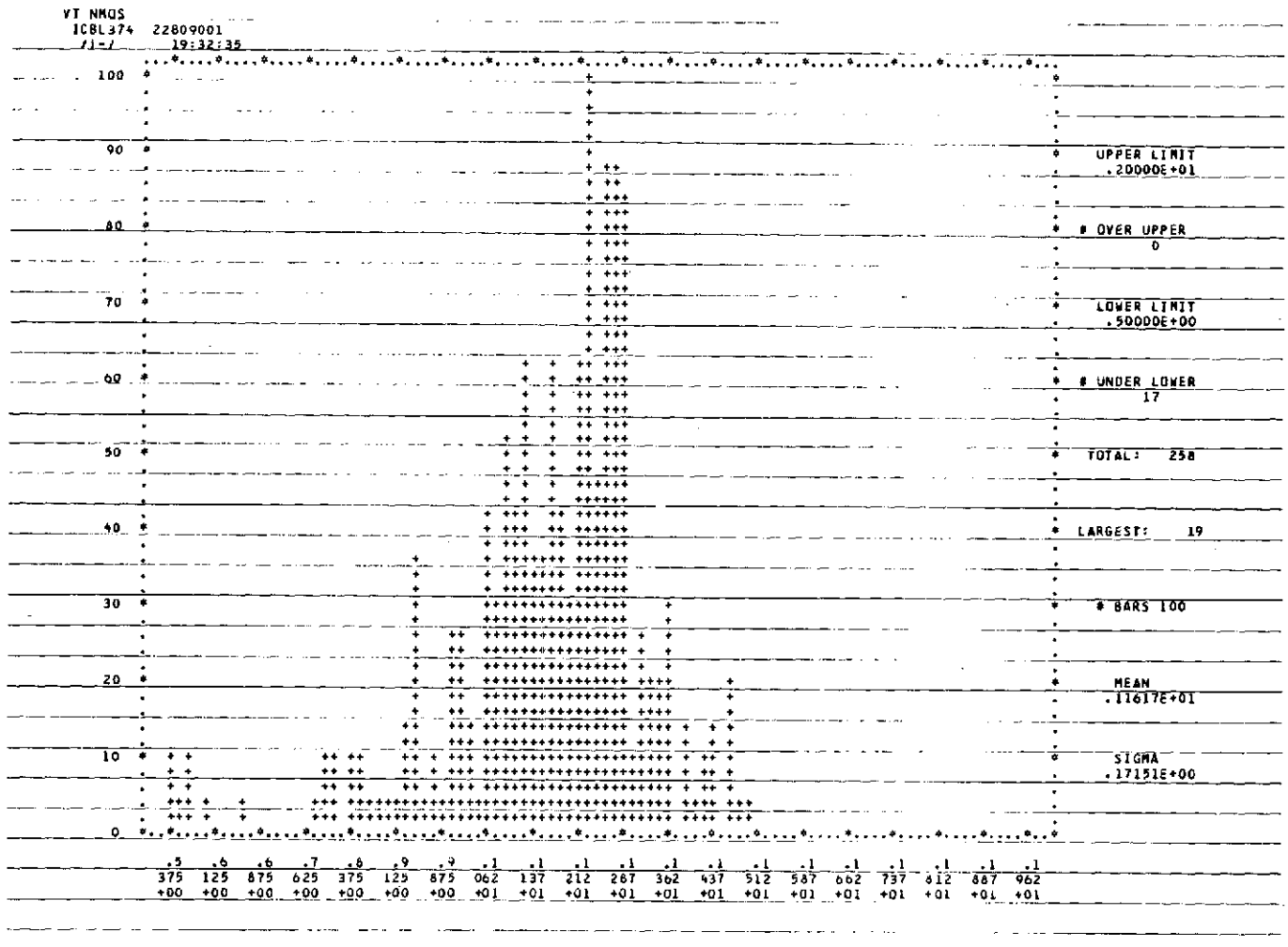

Figure 4. Histogram of TA5388 V_{TH} after beam-lead base metallization.

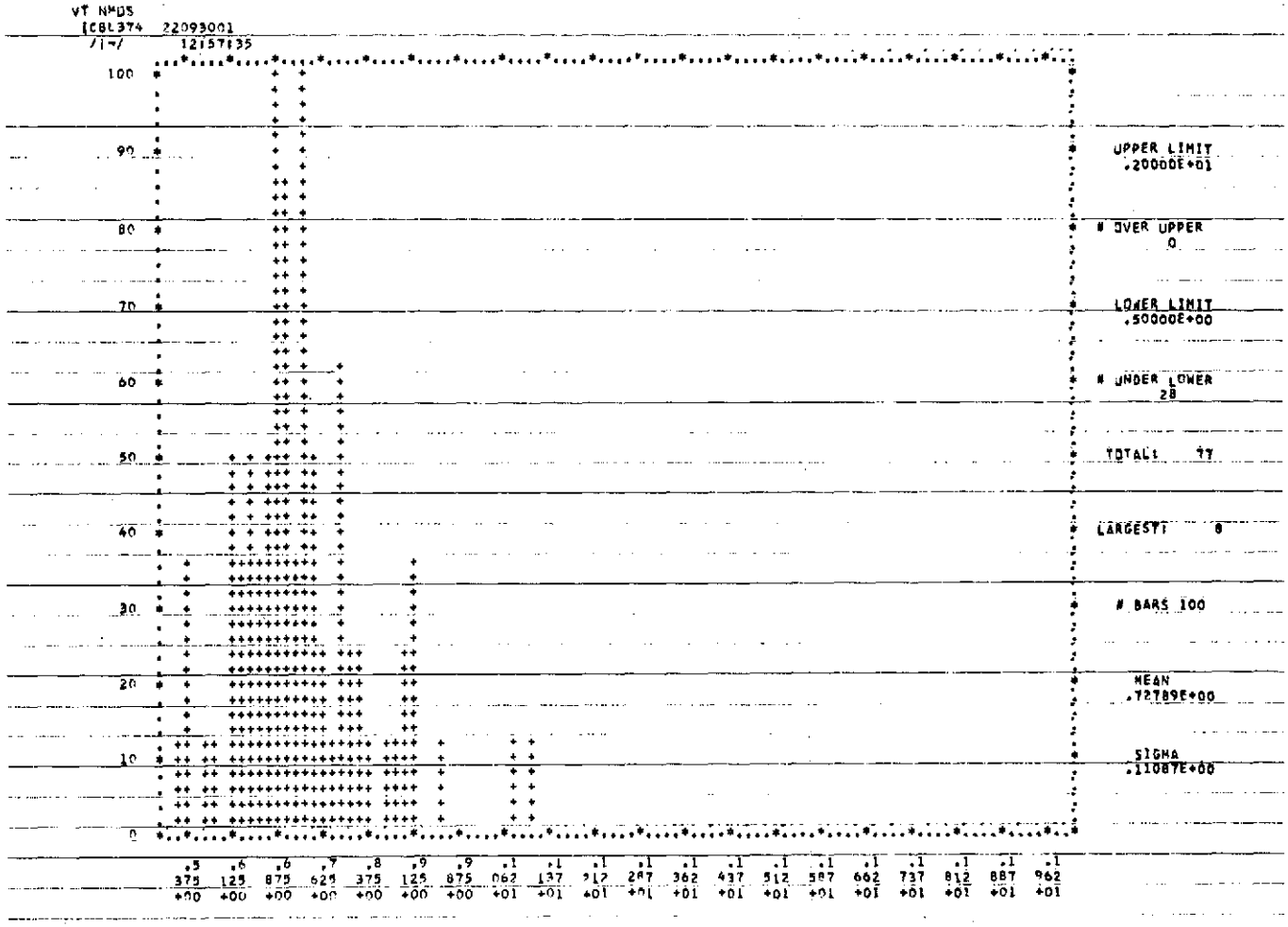

Figure 5. Histogram of TA5388 NMOST V_{TH} after gold beams.

shift is being investigated. More wafers are being processed to determine the electrical base line for this process and to determine if the shift is typical of the process.

IV. BEAM-LEADED 256-BIT RAM

In Quarterly Report No. 12 we described the design of the TA6567 circuit as the beam-lead version of the silicon-gate 256-word by 1-bit static SOS CMOS RAM, designated as TA6473. Figure 6 is a photomicrograph of the TA6567 beam-leaded 256-bit RAM chip on the wafer after formation of the gold beams. Several features can be seen that differ from the initial TA6473 design.

The most notable change is in the number of pads at the periphery of the circuit. Due to the desire to place the maximum number of beams at 20-mil centers around the chip, the total number of pads was dictated by the chip size. The chip size, defined as the step and repeat distance between chips including 2-mil scribe streets, was fixed at 135 mils by 145 mils. This decision was made to conform to EAI standards regarding beam-leaded integrated-circuit dimensions. The chip size was selected as a result of matching the EAI standards to accommodate the 256-word by 1-bit RAM that had been previously developed with the TA6473 circuit. With the guidelines established for the overall chip dimensions, the 20-mil center-to-center spacing between beams was reflected in seven pads for beams on each side of the chip.

Of the total 28 beams only 15 beams actually are needed for the circuit operation and 8 beams go to the test devices included in the TA6567 for improved process control. The remainder of the beams are dummy beams to improve the mechanical strength of the chip to ceramic substrate bonding. Beams were also placed as symmetrically as possible at the corners of the chip to minimize the difficulties of the "wobble" bonding step.

The beams from adjacent chips are readily noticeable as they interdigitate with the beams on the chip in the center of the photomicrograph. The beams extend over the 2-mil streets and actually over the neighboring chip, allowing a nominal beam overhand of about 4 to 5 mils after the chips are separated. The shadow effect on the pillar area of the beam in Fig. 6 is caused by nodules forming during the gold beam plating. This should not present a problem and can be eliminated by improving the gold-plating process.

The pads on the TA6567 are 4 mils by 8 mils, which is twice the normal pad area. This was done to allow the gold pillar and beam to be formed on a 4 mil x 4 mil region of the base metal that was not damaged by a probe, if the wafer was electrically tested after base metal and before beam formation. The electrical test probe is restricted to the remaining 4 mil x 4 mil area.

Another noticeable feature in Fig. 6 is the input protection scheme on the TA6567, which differs from that of the TA6473. The Zener diode protection reported on page 7 of Quarterly Technical Report No. 12 was implemented on the TA6567 circuit and appears as a series of four parallel bars associated with 11 of the input pads.

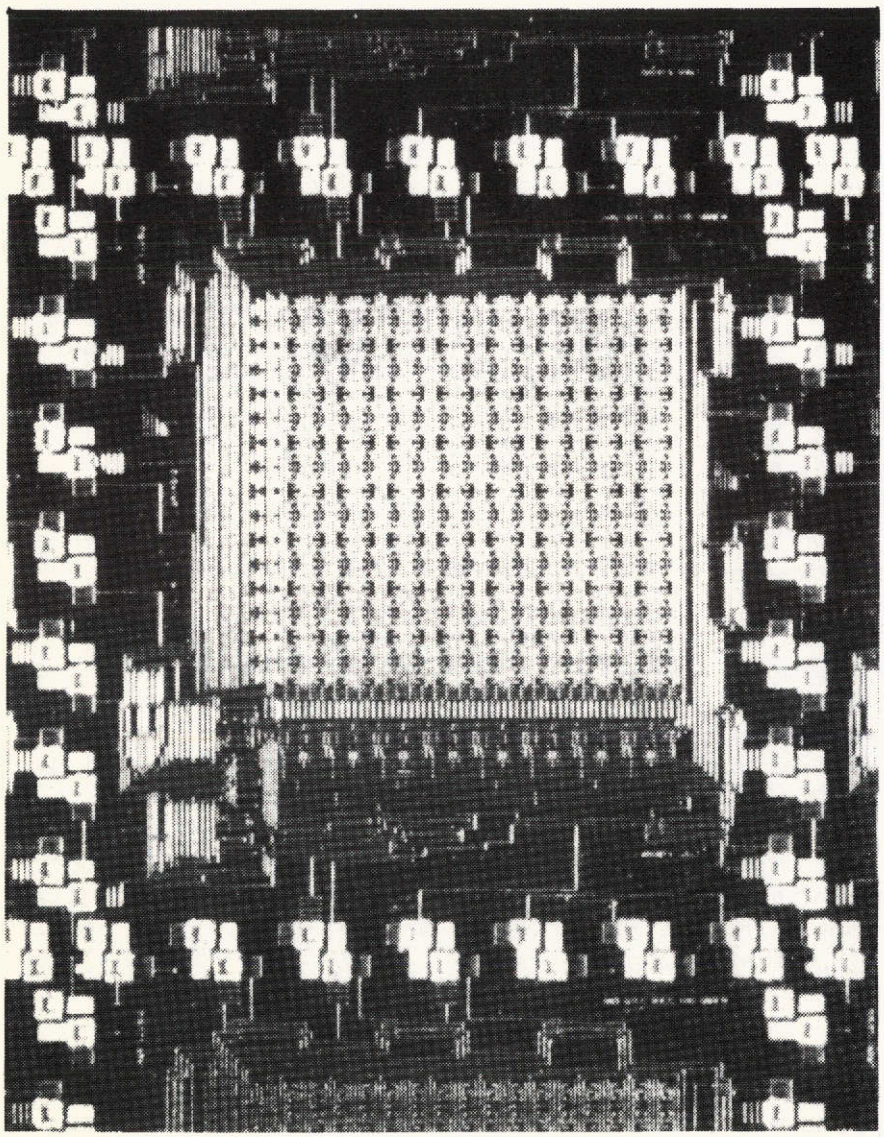

Figure 6. Photomicrograph of the TA6567 beam-leaded 256-bit RAM chip on wafer after gold beam formation.

V. CORRECTION

In Quarterly Technical Report No. 12, dated February 1974 and issued under NASA Contract No. NAS12-2207, change item 5 on page 8 to read:

5. Ten square, polysilicon bar: This resistor consists of a band of polysilicon that is divided (5 squares for each) by the doped oxide mask step. Thus, the subsequent drive-in of the diffusion source yields half of the polysilicon bar doped p+ while the other half is doped n+. Since the polysilicon is deposited as p-type, the n+ drive-in will not counter-dope the polysilicon. The result should yield a resistor of approximately 70 ohms per square. If there is an error in the doping of the polysilicon which could manifest itself as a p+/n+ diode in the test bar, this could then be detected.

VI. PERSONNEL AND EXPENDITURES

During the quarter reported herein the following personnel contributed to the contract:

W. C. Schneider	Project Scientist
R. J. Hollingsworth	

Total expenditures through March 31, 1974 have been $192,765 including profit. Problem areas that may create an overrun: none at this time.

VII. NEW TECHNOLOGY APPENDIX

It was concluded from the review of the work that there were no reportable items of New Technology under the contract during the period covered by this report.