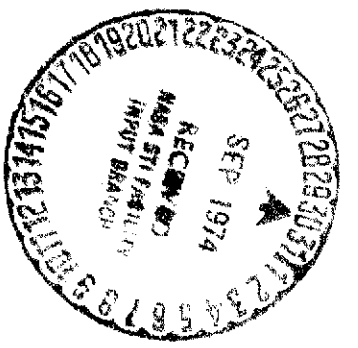
DESIGN, PROCESSING, AND TESTING OF LSI ARRAYS FOR SPACE STATION

BY

W. C. SCHNEIDER

QUARTERLY TECHNICAL REPORT NO. 14

AUGUST 1974



PREPARED UNDER CONTRACT NO. NAS12-2207 BY
RCA LABORATORIES
PRINCETON, NEW JERSEY 08540

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1. Report No.	2. Government Accession No.	3. Recipient's Catalog No.

4. Title and Subtitle	5. Report Date
DESIGN, PROCESSING, AND TESTING OF LSI ARRAYS FOR SPACE STATION	July 1974
	6. Performing Organization Code
7. Author(s) W. C. Schneider	8. Performing Organization Report No. PRRL-74-CR-53
9. Performing Organization Name and Address RCA Laboratories Princeton, NJ 08540	10. Work Unit No.
	11. Contract or Grant No. NAS12-2207
	13. Type of Report and Period Covered Qtly. Technical Report No. 14(4/1/74-6/30/74)
12. Sponsoring Agency Name and Address George C. Marshall Space Flight Center National Aeronautics & Space Administration Huntsville, Alabama 35812	14. Sponsoring Agency Code

15. Supplementary Notes

16. Abstract

The goal of this research program is the development of a beam-leaded low-power, high-performance metal-oxide-semiconductor (MOS), 256-bit random access memory (RAM). Previous success with the aluminum-gate current-sense version and a silicon-gate voltage-sense version led to the present effort to make a beam-leaded silicon-gate RAM. Some problems unique to the silicon-on-sapphire beam-lead process development are presented. Beam-leaded SOS TA5388 devices using a Si_3N_4 passivation layer were shown to have good electrical parameters. Ten mechanical samples of the beam-leaded 256-bit RAM (TA6567) bonded on ceramic substrates were delivered to NASA, Huntsville, Alabama.

17. Key Words (Selected by Author(s))	18. Distribution Statement
Random access memory (RAM) Beam-lead process	

19. Security Classif. (of this report)	20. Security Classif. (of this page)	21. No. of Pages	22. Price*
Unclassified	Unclassified	16	

*For sale by National Technical Information Service, Springfield, Virginia 22151.

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SUMMARY

The goal of this research program is the development of a beam-leaded low-power, high-performance metal-oxide-semiconductor (MOS), 256-bit random access memory (RAM). Previous success with the aluminum-gate current-sense version and a silicon-gate voltage sense version led to the present effort to make a beam-leaded silicon-gate RAM. Some problems unique to the silicon-on-sapphire beam-lead process development are presented. Beam-leaded SOS TA5388 devices using a Si_3N_4 passivation layer were shown to have good electrical parameters. Ten mechanical samples of the beam-leaded 256-bit RAM (TA6567) bonded on ceramic substrates were delivered to NASA, Huntsville, Alabama.

I. INTRODUCTION

RCA has been a pioneer in the research and development of silicon-on-sapphire (SOS) technology. The many facets of this program include materials and basic device research, computer-aided circuit design, mask-making techniques, and advanced CMOS array design using large-scale integration (LSI).

Support has previously been made available to develop an aluminum-gate current-sense version and a silicon-gate voltage-sense version of the low-power, high-performance CMOS/SOS 256-bit random access memory (RAM). Success with both types of the RAM resulted in the present phase of this project to develop a low-power, high-performance metal-oxide-semiconductor (MOS), 256-bit RAM with beam leads. The development of the beam-leaded SOS technology has combined the standard SOS process with a modified microbridge beam-lead process. The mechanical feasibility of this technology has been demonstrated using as the test vehicle a dual complementary pair plus inverter (TA5388). This circuit was fabricated on SOS and metallized using the beam-lead base metal and gold beam technology; it was then laser-scribed, separated, and bonded to a standard 14-lead ceramic DIP. Stable TA5388 devices have been made using a Si_3N_4 passivation layer. Subsequent efforts have been to improve the beam-lead processing and to establish the electrical base line data for the beam-lead CMOS/SOS devices using the TA5388 circuit.

The 256-bit beam-leaded RAM circuit (TA6567) was processed, and ten mechanical samples assembled on ceramic substrates were delivered to NASA, Huntsville, Alabama.

II. BEAM-LEAD SOS PROCESS DEVELOPMENT

The beam-lead SOS process development is mainly concentrated on the Si_3N_4 passivation layer, gold pillar and beam formation, and subsequent chip separation and bonding to a ceramic substrate. The Ti/Pd/Au base metal process is satisfactory from both an electrical viewpoint and a mechanical viewpoint.* The development areas are discussed below.

A. Si_3N_4 Passivation Layer

The present procedure requires the Si_3N_4 layer to be deposited by CVD in the AMT800 reactor just prior to the opening of contacts and the base metal step. The contacts are first opened in the Si_3N_4 layer and then through the SiO_2 layer by chemical etching. The first goal is to determine the optimum thickness for electrical passivation that is consistent with the standard processing techniques.

An experiment on BL/SOS** TA5388 circuits with three different Si_3N_4 passivation layer thicknesses (500 Å, 1200 Å, and 2000 Å) was completed; mechanically good beams were obtained. The initial hand-probed electrical test data indicate good passivation for all thicknesses of Si_3N_4. No threshold voltage shift was observed after gold beam formation, as was previously reported (ref. 1). Additional evaluation and electrical testing are being done on the wafers.

B. Gold Pillar and Beam Formation

One of the more critical parts of the BL/SOS process is the formation of the second level of gold metallization, i.e., the pillar and beam formation. The processing sequence was described in detail in Quarterly Technical Report No. 12 (ref. 2).

Figure 1 is a scanning electron micrograph (SEM) photograph of three beams and the base metal on the corner of a BL/SOS chip. The

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*The base metal process gives good ohmic contacts between the silicon and the base metal. Also, it passes the "scotch tape" adhesion test; i.e., scotch tape is smoothed out over the base metal on a wafer and then pulled off rapidly without removing the base metal. This qualitative test is an indicator of good base-metal-to-substrate adhesion.
**BL/SOS - beam-lead silicon on sapphire.

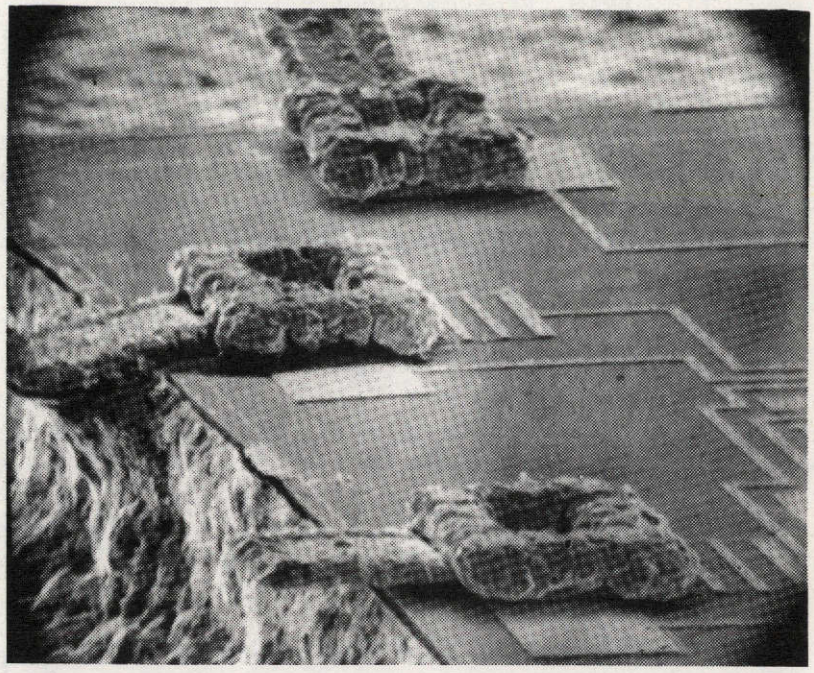

Figure 1. SEM of gold beams and base metal on corner of BL/SOS chip.

SOS wafer was laser-scribed and broken by mechanical roller breaking. The photomicrograph is shown for orientation purposes in this discussion. Notice the large grain size of the electroplated gold, especially around the pillar or anchor pad. This condition can be minimized by controlling the PH and the percentage of gold in the electroplating bath. Figure 2 shows a scanning electron microscope (SEM) photograph of a beam and pillar formed in a well-controlled gold-plating bath. Here the grain size of the gold at the top of the beam is smaller than that of the beams in the previous case. In both cases, the gold at the bottom of the beam was well defined by the photoresist and then rounded off as the beam thickness approached and then exceeded the thickness of the photoresist. This variation in beam cross section has not presented any problem in subsequent processing.

The subsequent series of SEM photographs (Figs. 3 through 5) show the build-up of the gold pillar and beam. Figure 3 shows the via opening defined in the photoresist after etching the copper to expose the base metal and after plating the gold pillar. Figure 4 is the same

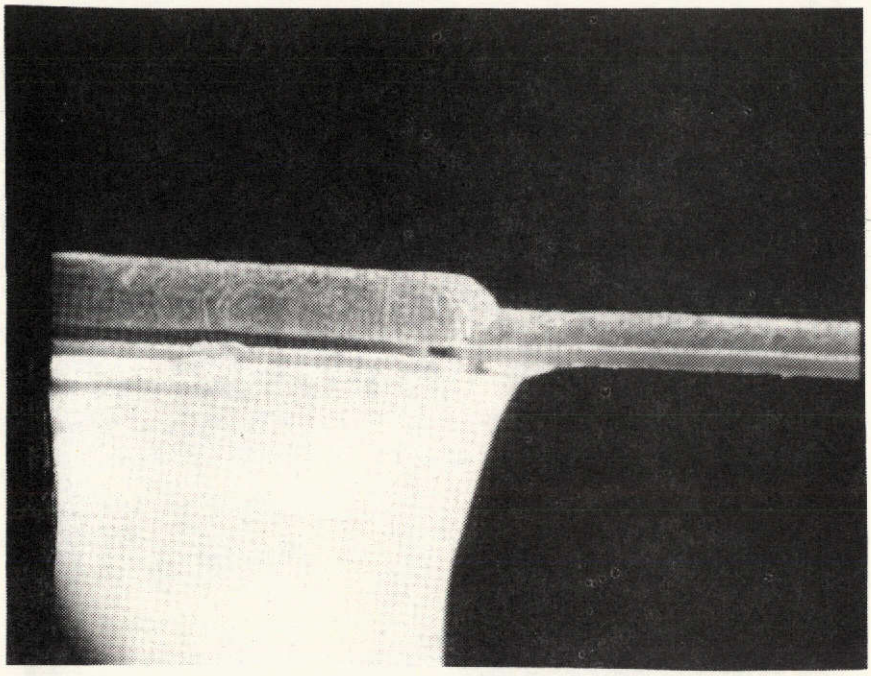

Figure 2. SEM profile of gold beam on BL/SOS chip.

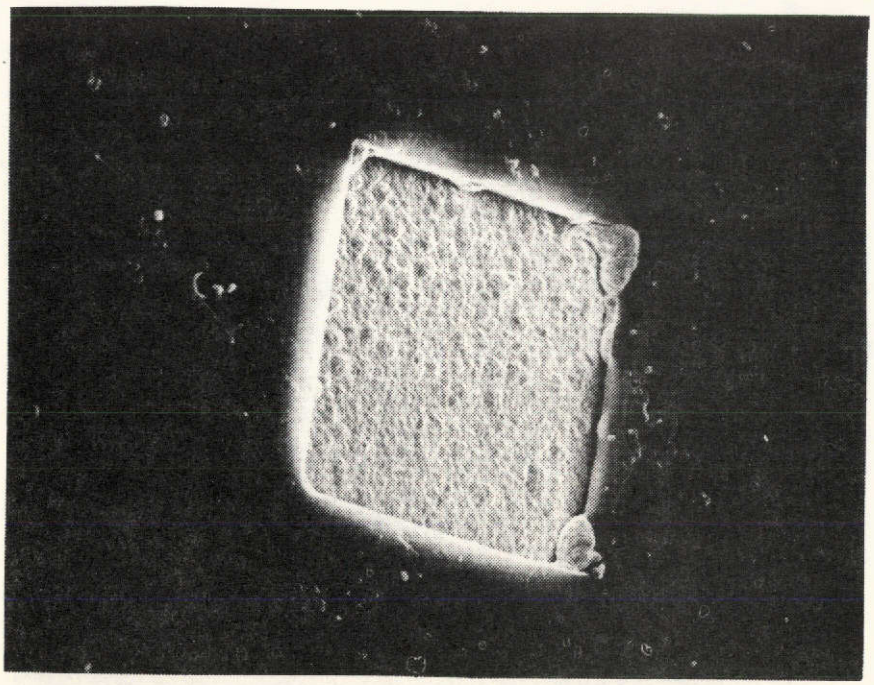

Figure 3. SEM via opening in photoresist after etching the copper and plating the gold pillar.

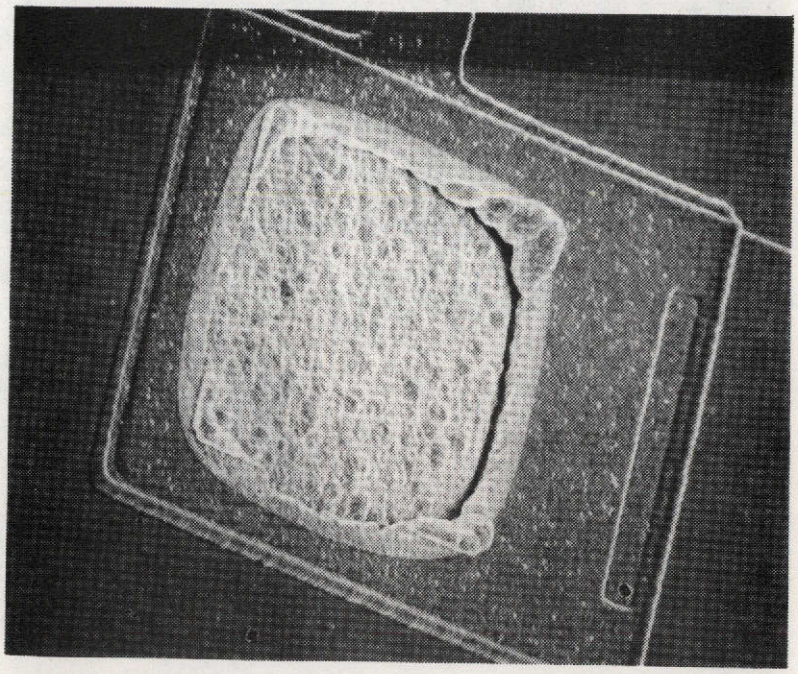

Figure 4. SEM of same area as in Fig. 3 with photoresist removed.

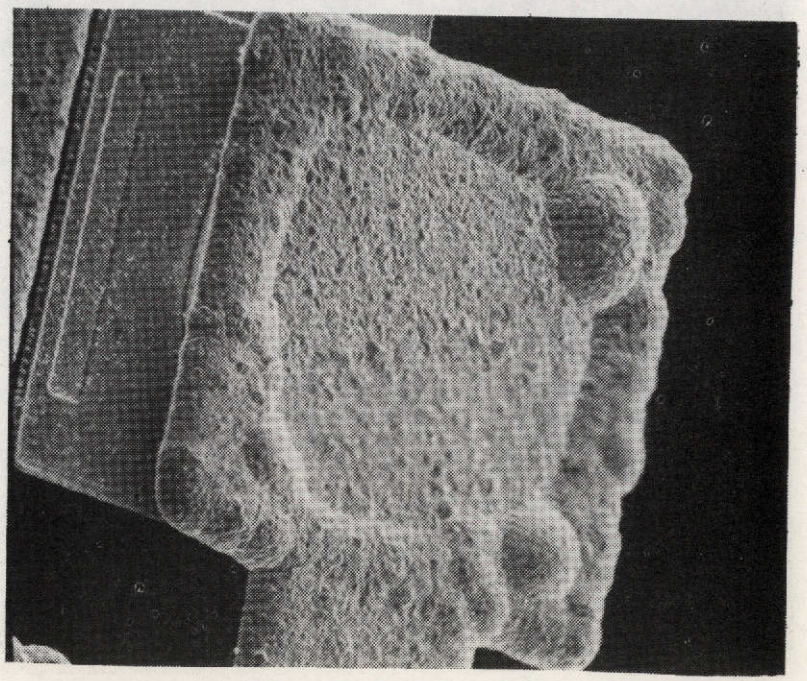

Figure 5. SEM of same area as in Fig. 3 with completed gold beam lead.

area with the photoresist removed to expose the copper layer that replicates the area surrounding the via. The contact pad and base metal, and a rectangular contact opening to the protective diode array are clearly outlined. Note the nonuniform plating of gold around the edge of the via opening that causes the beam gold to plate thicker around the edge of the pillar opening. This effect is observed on most of the beam leads made by this process on SOS and does not cause a problem in subsequent processing.

C. Chip Separation and Bonding

The laser scribing and breaking of beam-leaded SOS wafers as described in a previous report (ref. 3) is a fairly standard technique. Additional improvements will be to increase the throughput and the scribing alignment accuracy.

The feasibility of separating the chips using a wafer expander was demonstrated but not optimized. Figure 6 is a photomicrograph of the BL/SOS TA5388 circuit on the wafer before scribing. Note the interdigitated beams and the length of the beam overhanging the adjacent chip. Figure 7 is the same circuit (the magnification differs from that in Fig. 6 but only the relative spacing is important for this discussion) after scribing, breaking, and expanding.

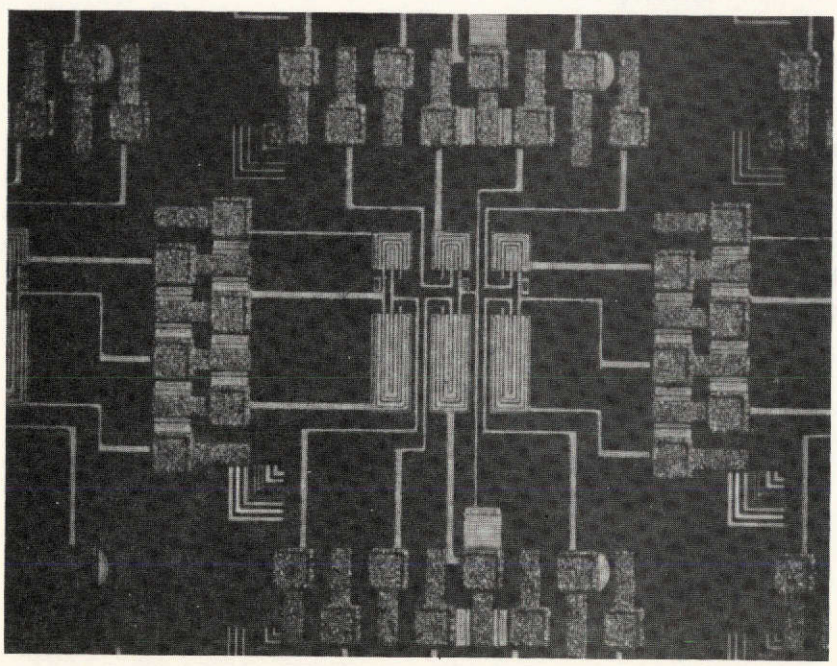

Figure 6. Photomicrograph of BL/SOS TA5388 circuit on the wafer before scribing.

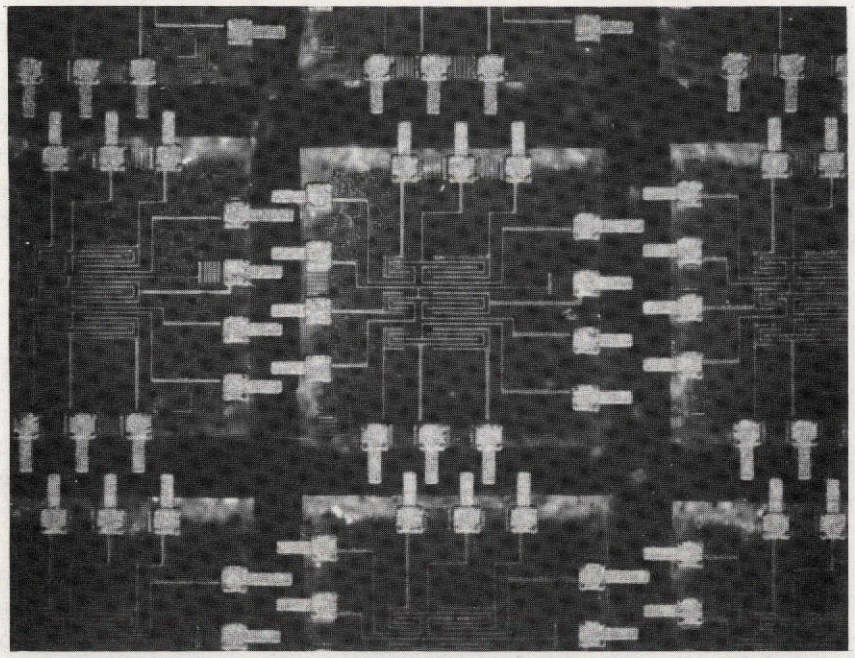

Figure 7. Photomicrograph of BL/SOS TA5388 circuit after scribing, breaking, and expanding.

With the proper expansion, the beams are no longer interdigitated and a chip can be easily removed without bending the beams.

The assembly of beam-leaded SOS chips on the ceramic substrate is done by "wobble-bonding." Both the BL/SOS TA5388 dual complementary pair plus inverter circuit (53 mils x 53 mils, 14 beams) and the BL/SOS TA6567 256-bit RAM circuit (135 mils x 145 mils, 28 beams) have been wobble-bonded on ceramic substrates. Further discussion of the TA6567 is given in Section III.

III. BEAM-LEADED 256-BIT RAM TA6567

The description of the beam-leaded silicon-gate 256-word by 1-bit static SOS CMOS RAM designated as TA6567 was given in previous quarterly reports (refs. 1 and 2). In this quarter, the TA6567 beam-leaded chip has been successfully fabricated and assembled as a mechanical sample on a ceramic substrate. Figure 8 is a photomicrograph of the TA6567 chip beam-leaded to a 24-pin DIP ceramic substrate. The actual circuit outline is visible through the transparent sapphire substrate. Ten mechanical samples of this type were delivered to the Contract Monitor this quarter to satisfy one part of the deliverable items listed under Contract No. NAS12-2207.

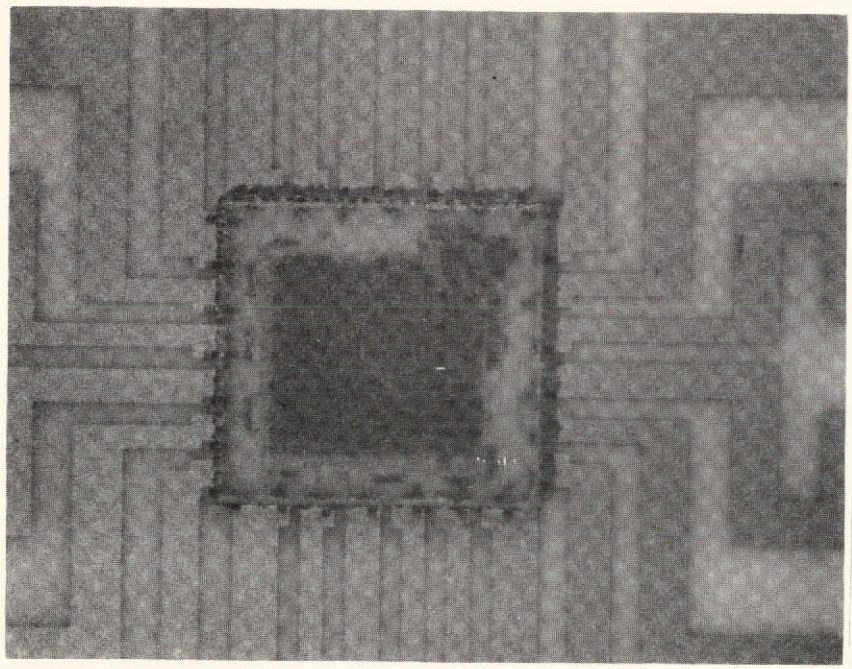

Figure 8. Photomicrograph of BL/SOS TA6567 256-bit RAM chip bonded onto a ceramic substrate.

IV. PERSONNEL AND EXPENDITURES

During the quarter reported herein the following personnel contributed to the contract:

W. C. Schneider	Project Scientist
R. J. Hollingsworth	

Total expenditures through June 30, 1974 have been $202,280 including profit. Problem areas that may create an overrun: none at this time.

V. NEW TECHNOLOGY APPENDIX

It was concluded from the review of the work that there were no reportable items of New Technology under the contract during the period covered by this report.

REFERENCES

1. W. C. Schneider and R. J. Hollingsworth, Design, Processing, and Testing of LSI Arrays for Space Station, Quarterly Technical Report No. 13, Contract NAS12-2207, May 1974.

2. W. R. Lile and R. J. Hollingsworth, Design, Processing, and Testing of LSI Arrays for Space Station, Quarterly Technical Report No. 12, Contract NAS12-2207, February 1974.

3. W. R. Lile and W. J. Greig, Design, Processing, and Testing of LSI Arrays for Space Station, Quarterly Technical Report No. 11, Contract NAS12-2207, October 1973.