RESEARCH ON SPACECRAFT ELECTRICAL POWER CONVERSION

For

National Aeronautics and Space Administration

Twenty-Sixth Status Report

For Six-Month Period Ending February 28, 1974

Research Grant Number

NGL-34-001-001

Supplement No. 13

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Durham, North Carolina

(NASA-CR-140038) RESEARCH ON SPACECRAFT ELECTRICAL POWER CONVERSION Status Report, 1 Sep. 1973 - 28 Feb. 1974 (Duke Univ.) 10 p HC $4.00 CSCL 10A

N74-33482

Unclas
G3/03 48791

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March 1, 1974

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Background

Research on this project has been conducted in the Department of Electrical Engineering at Duke University since May 1961. It was originally supported under Grant Number NsG 152-61. The number was changed to Grant NGL 34-001-001 on June 19, 1968 when the project was put on the three-year step-funding program of NASA. Supplement 13 of this grant covers the period from March 1, 1973 to February 29, 1976. The present semiannual status report covers the period from September 1, 1973 through February 28, 1974. It summarizes the various research activities conducted during this six-month interval.

Personnel

During the period covered by this report, personnel associated with the project were:

Professor Thomas G. Wilson, Principal Investigator, and Professor Harry A. Owen, Jr., Associate Investigator, both part time; Mr. Fred C. Y. Lee, Mr. Anil K. Ohri, and Mr. De-Yu Chen, doctoral candidates, full time; Mr. William W. Burns, III, graduate student, part time; and Mr. Jimmy Hartley, technical assistant, half time.

Documentation

Work during the six-month interval covered by this report included preparation of the following six documents:

[1]. A paper abstract entitled "Nonlinear Analysis and Duality Relations Applied to a Family of LC Tuned Inverters" was accepted to be presented at the IEEE Power Electronics Specialists Conference, Bell Laboratories, Murray Hill, New Jersey, June 10-12, 1974.

[2]. A paper abstract entitled "Voltage-Spike Analysis and Suppression for a Free-Running Parallel Inverter" was accepted to be presented at the INTERMAG Conference, Toronto, Canada, May 14-17, 1974.

[3]. A paper abstract entitled "Digital Computer Simulation of Inductor-Energy-Storage DC-to-DC Converters with Closed-Loop Regulators" was accepted to be presented at the Spacecraft Power Conditioning Electronic Seminar, ESRIN, Frascati, Italy.

[4]. The full text of a paper entitled "Design of Two-Winding Voltage Step-Up/Current Step-Up Constant-Frequency DC-to-DC Converters" was published in the IEEE Transactions on Magnetics, Vol. MAG-9, No. 3, pp. 252-256, September 1973.

[5]. The full text of a paper entitled "Analysis and Modeling of a family of Two-Transistor Parallel Inverters" was published in the IEEE Transactions on Magnetics, Vol. MAG-9, No. 3, pp. 414-418, September 1973.

[6]. The full text of a paper entitled "Analysis of Starting Circuits for a Class of Hard Oscillators: Two-Transistor Saturable-Core Parallel Inverters" was published in the IEEE Transactions on Aerospace and Electronic Systems, Vol. AES-10, No. 1, pp. 100-112, January 1974.

Research Summary

Considerable success, as described in past status reports, has been attained in applying state-plane methods of nonlinear analysis to investigate the steady-state characteristics and starting behavior of some of the most widely used self-oscillating magnetically-coupled square-wave inverters. See Ref. (1) at the end of this report and Items [5] and [6] on page 2. The last status report mentioned an effort which has just been initiated to investigate the possibility of extending this basic method of analysis to a group of power-conditioning circuits called LC-tuned square-wave inverters. This type of circuit employs an inductor-capacitor tuned network instead of a saturating magnetic core to control the switching of the power transistors, and thereby control the frequency of the square-wave output. During the present reporting period, the analysis method mentioned above has been successfully applied to this new family of LC-tuned inverter circuits. It has been shown that these inverters can be reduced to a common second-order equivalent circuit, consisting of only three *series* elements: 1) a five-segment piecewise-linear current-controlled resistor, 2) a linear inductor, and 3) a linear capacitor. Additionally, certain duality relationships have been established between the family of saturable-core parallel inverters and the family of LC-tuned parallel inverters. It is through these duality relationships that many useful results developed for inverters in the former family as described in Item [5] on page 2 can be applied to inverters in the latter family.

The analysis shows that the stable limit cycle of this new family of inverters is basically a relaxation oscillation. With proper design, inverters in this family produce an approximately square-wave output voltage. Parameter influences on inverter performance have been investigated and approximate bounds for parameter variations can be established beyond which the inverter may cease to oscillate.

Finally, requirements for the starting of oscillations have been examined and two illustrative starting circuits have been analyzed. It can be shown that the concepts developed in the previous analysis of starting-circuits for saturable-core inverters are applicable to LC-tuned inverters. An abstract of this phase of our research activities has been prepared, Item [1] on page 2, and work has been started on the preparation of a technical paper.

Effort has also been directed to obtaining a better understanding of the high-amplitude voltage spikes which occur in dc-to-square-wave parallel inverters of the Royer type. The existence of these unwanted high-voltage spikes has been one of the important practical considerations influencing the design of this type of inverter. These spikes, occurring at the beginning of each half cycle of output voltage, are one of the major causes of power-transistor failure in such inverters. In the past, these spikes usually have been attributed to leakage inductance in the power transformer, inductance associated with the load, and/or the after-saturation inductance of the saturable-core transformer. Such explanations have been primarily descriptive providing little quantitative information.

During the past six months, the state-plane method has been employed to investigate this problem and has been able to show in detail the mechanism whereby voltage spikes can be produced in such inverters with negligible inductances and purely resistive loads. See Item 2 on page 2. This work, building upon some of the results in Ref. (1) at the end of this report, analyzes the same basic configuration as the one studied there, but this time, without the commutating diodes which served to simplify the previous analysis by eliminating the possibility of either transistor entering its inverse region.

In the present analysis, the common-emitter model used for the PNP transistors is redefined to include in the collector characteristic, the avalanche-

breakdown region and the inverse-conduction region, and to include in the base characteristic a family of curves with negative as well as positive emitter-to-collector voltage. The analysis shows that the inverter can be represented by a second-order equivalent circuit consisting of three parallel elements: a nine-region piecewise-linear resistor, a four-segment piecewise-linear reactor, and a linear capacitor. The dynamics of the system are studied using state-plane methods which clearly and concisely portray transient and steady-state motions of the system as curves on a plane. Results of the analysis permit prediction of the magnitude of both current and voltage spikes, and permit conclusions to be drawn concerning the relative importance of various circuit parameters including some of the small but vitally influential ones such as saturation inductance of the square-loop core, parasitic capacitances of the transistor junctions and transformer windings, reverse-current gain β_R of the transistors, and the magnitude of the avalanche breakdown voltage. This information provides insight for inverter design and guidance in choosing means for the suppression of spikes.

Also mentioned in the last status report was an effort to develop a way to evaluate the performance of closed-loop regulated converters. In particular, a computer program originally developed by IBM under the name Continuous System Modeling Program (CSMP) has received much attention. This program models the system at the "block diagram" level rather than the component level as in many of the various circuit analysis programs nowadays available. The structure of this program is such that information about the system under investigation is fed into the computer in terms of differential equations in a form of input/output "blocks" which define the dynamic behavior. Other "blocks" are available to simulate the control functions of the system and the switching of the system from one mode of operation to another.

In the past six-month period, considerable effort has been expended on modifying and adapting this program for use in the Department of Electrical Engineering's PDP-11/45 digital computer and interfacing it with graphic-display units. This work is now complete and several simulation runs have been made on inductor-energy-storage dc-to-dc converters with closed-loop regulators. The results have been very encouraging and this approach appears to be an effective way to predict the transient response of this class of converter which by other means is an extremely difficult task. An abstract has recently been prepared describing this approach. See Item [3] on page 2.

Another simulation run, done at the request of NASA personnel, was for a preregulating current step-up converter to be used for the X-ray experiment on the High-Energy Observatory (HEAO-A2) satellite. The result of this simulation also was satisfactory, and it is believed that many more important electronic power processing systems may be investigated for transient response due to input-voltage and output-load disturbance with sufficient accuracy by using this simulation program.

A continuing attempt has been made to simulate a Direct Energy Transfer (DET) System by means of the IBM program product ECAP II. Unfortunately, the difficulties and delays encountered during the initial stages of this endeavor have continued throughout this reporting period. As a result of these difficulties and IBM's subsequent response to them, it is now felt that this particular circuit analysis program does not have the capability it was originally thought to have had. Consequently, procedures were initiated in February of this year to cancel the rental of ECAP II. It is still believed, however, that this approach to the study of large scale power conditioning systems is a promising one, and additional circuit analysis programs, such as IBM's Advanced Statistical

Analysis Program (ASTAP) and U.S. Air Force's SCEPTRE, are being investigated.

In the meantime, a second approach to the DET System has been pursued. This approach involves the simulation of this system by using IBM's Continuous System Modeling Program (CSMP). This program, as described earlier in this report has been modified and adapted for use in the Deaprtment of Electrical Engineering's PDP-11/45 digital computer. Presently, a preliminary model of some of the subsystems of the DET System proposed for use on the IUE spacecraft has been stored in the computer. An extension of this model to include the remaining subsystems is planned for the upcoming period.

Work has continued on the computer aided design of two-winding energy-storage dc-to-dc converters. A computer aided design procedure for the case of a two-winding converter with a constant-frequency controller was completed, and a technical paper prepared as mentioned in the last status report. See Item [4] on page 2. Additional new work along this line was carried out during this reporting period for the two remaining cases: the two-winding constant-on-time, and the two-winding constant-off-time converters. From analysis of this converter with these two controllers, design procedures were developed for these two new cases and FORTRAN IV programs were written to implement the designs. The structure of these programs is similar to that for the constant-frequency converter. Converter circuits of these two types will be constructed and tested in the laboratory during the next period to verify the results obtained from these computer programs.

Work has also continued on the conversion of the nine single-winding-converter design programs in Ref. (2) from FOCAL language to FORTRAN. Completed and reported in the last status report was the conversion of one of the nine programs, the voltage step-up constant-frequency converter. The conversion of

the remaining eight programs was completed during this reporting period. With these programs available in FORTRAN, the design algorithm developed for the nine single-winding converters may be readily adapted to many more digital computer installations thereby making this design tool available to many more potential users.

References

1. Fred C. Y. Lee, T. G. Wilson, and Sam Y. M. Feng, "Analysis of Limit Cycles in a Two-Transistor Saturable-Core Parallel Inverter," IEEE Transactions on Aerospace and Electronic Systems, Vol. AES-9, No. 4, pp. 571-584, July 1973.

2. D. Y. Chen, H. A. Owen, and T. G. Wilson, "Computer-Aided Design and Graphics Applied to the Study of Inductor-Energy-Storage dc-to-dc Electronics Power Converters," IEEE Transactions on Aerospace and Electronic Systems, Vol. AES-9, No. 4, pp. 585-597, July 1973.