MEMORY SYSTEMS FOR SIGNAL GENERATING PHOTOELECTRIC IMAGE DETECTORS

Edwin W. Dennison

Hale Observatories
Pasadena, California USA

INTRODUCTION

The recent developments in signal generating electronic image detectors have necessitated a corresponding development of digital memory systems which have the capacity to handle the large amount of information contained in a typical image. Current memory technology enables the practical use of memories containing 4×10^9 bits and larger which can be used as image integrators and storage devices. A memory of this type was built at the Hale Observatories as part of a joint project with the University of Princeton Observatory. It has been successfully used with a high gain pulse-counting television camera tube, and also with a silicon target image detector with an analog-to-digital converter between the detector and the memory. In both cases the memory clearly demonstrated the power of this form of image integration. Some valuable experience was gained with this memory and a recommended list of design criteria for future memories has been made. Alternative systems are possible for photoelectronic detectors, using a slow scan readout.

THE PRINCETON-HALE DIGITAL MEMORY

The memory elements of this system are dynamic MOS shift registers. The maximum number of words is 65,536, the minimum number is 2,048. The memory size can be changed in binary increments between these limits. The memory words are serially accessed with a two coordinate raster type addressing system. The total number of pixels (picture elements) per scan line, and the total number of scan lines per frame can be set at between 8 and 2,048 in binary increments. The memory has, in fact, always been used in a 256 × 256 raster pattern. The additional flexibility was intended to allow the use of this memory with rectangular spectroscopic images.

To increase the time available to input new data the memory was divided into 8 banks which are sequentially shifted. The input data, which can be in the form of 1 to 16 bits, is clocked into a multiplexer which distributes the data to the memory banks. This arrangement gives the circuitry eight times the pixel period for accessing, adding, storing, and shifting the data. In the usual mode of operation the pixel period is 208 n-sec (4.8 MHz), but the operating circuitry has approximately 1.7 μ sec to process each memory word. The currently addressed memory word is also multiplexed out to an 8-bit digital-analog converter, which the operator may set to any 8 contiguous bits.

The pixel or word frequency can be set over the range from 9.6 KHz to 4.8 MHz. The fact that the memory elements are dynamic in operation means that there is necessarily a lower limit to the pixel rate and also that the controlling circuitry must allow for computer access, horizontal and vertical blanking periods, and flexibility in data acquisition, without stopping the memory shift clocking long enough to degrade the data. The master timing circuitry which controls the format of the data clocking also generates sync pulses, blanking pulses, and standard clock pulses. All of these timing pulses are available for synchronizing the circuits which are external to the memory. The clock pulses are transmitted to the camera unit and back, to automatically allow for propagation delays in the 700 feet of coaxial cables connecting the camera unit and the memory (for the 200" operation). For most of the actual display operations, the composite video and sync signals were sent directly to a standard video monitor. This monitor allows the operators to see the image in the memory as it changes during the integration period.

The total integration time can be set from 1 to 9,999 seconds. Other operator controls can be used to start, or stop, the integration, suspend the integration, record the data, etc. All of these controls have been arranged to provide the operator with the maximum possible flexibility and convenience.

The image data, telescope coordinates, time, object name, and other relevant information are all recorded on 9-track industry-compatible magnetic tape under the control of a Raytheon computer. The image memory interface circuits have provision for integration control and data transfer to the computer, but do not allow data to be transferred into the memory from the computer.

Some of the circuitry performs dynamic tests on the memory to ensure that the memory data stays in synchronizm with the clock pulses. Although the system as a whole has not been entirely trouble-free, no clocking or word address problems were ever encountered.

APPLICATIONS

The two camera systems which have been used with this memory are being described elsewhere at this symposium.[1,2] In the first case (Lowrance et al) the system was used in the pulse-counting mode, i.e., the words in the memory were incremented by 1 if the detector sensed the presence of a signal during the time interval corresponding to each pixel. In the second case (Alsberg et al) the video signal was processed in a 8-bit digitizer during each pixel time, and the resulting value was added into the corresponding memory word. In both cases the memory was run at the 4.8 MHz pixel rate and a standard TV monitor was used to evaluate the image during the integration. All other system conditions were

essentially the same except that in the first case the data were read out by the computer, and in the second case a "line-snatch" technique was used to read out the data, one line at a time. The final recording was on magnetic tape in both cases. In the second case, a thorough analysis of the noise spectrum established that the system was operating as a perfect integrator.

OPERATIONAL EXPERIENCES

To summarize our operational experiences I will list the specifications which I would use if I were building an image memory at this time.

1. Static data storage — The memory should be capable of storing information in a static form. The important problem to avoid is the requirement that the data be shifted periodically to insure its retention.

2. Random access — Serial memory devices are difficult to reconfigure for different image formats and are generally constructed from finite length modules.

3. 65,536 words expandable to 262,144 words — This allows the initial format to be 256 × 256 pixels with possible expansion to 512 × 512 pixels.

4. At least 16 bits per word — Larger words may be desirable but there appears to be no justification for a word size larger than 24 bits.

5. Data transfer in and out of memory — This two way data transfer capability is most valuable for memory diagnostic tests, reviewing previously recorded images, and possibly for some data reduction operations at the observatory site.

6. 10 MHz maximum word rate -

7. Input of 12 bit data word - Preferably provision should be made for an input of the full memory word size.

8. Real time video or amplitude display - During the image integration period or during image analysis it is extremely valuable to have a visual presentation of the image.

9. Changeable operating parameters - The entire range of possible operating parameters cannot be built into the original unit, but provision must be made for easy modification of the central control circuits. This could be by the use of micro-computers or an interchangeable control module.

10. Manual and computer interface for controls - The actual memory system operation should be controllable by either a computer or a simple operator panel. The status of all counters and registers must be computer readable.

11. Camera system I/O registers - These registers should provide for either computer or manual camera controls and status sensing.

12. Easily operable at laboratory and observing locations - In most cases this implies that the system must be self-contained, although in some cases standard computer installations may be available. It is also possible that a system could be developed with a standard CAMAC interface.

GENERAL COMMENTS

It would appear that no single photoelectron image detector system has been developed to the point where it can be used for all applications and image detector development will continue for a number of years. Our experience does indicate that it is possible to construct a memory system which can be effectively used on a variety of image detectors. The advantages of digital memory systems are that they provide

a) Ideal integrators;

b) Real time display of images during data integration;

c) Re-display of images after the data-recording;

d) The possibility of performing rapid image processing at the observing location.

It is interesting to note that the above specifications can be met for a slow scan readout system (approximately 20 KHz) by the use of a mini-computer with a disk, magnetic tape output, and some form of video display. The performance of a system of this type will be inferior to that of a separate memory system, but in many cases, this reduced performance may be an acceptable consequence of budget or time limitations.

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REFERENCES

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2) Paper Number 25 High resolution electron microscope imaging with silicon diode array target vidicons. H. Alsberg and R. E. Hartman, Jet Propulsion Laboratory, California Institute of Technology Pasadena, California.