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WIDEBAND INFRARED RECEIVER BACKEND

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16. Abstract

This report describes the design, operation, and configuration of the receiver backend for a wideband infrared tracking receiver. The receiver design incorporates a squaring loop to enable it to track the Doppler shifted carrier which is Phase Shift Keyed modulated. The receiver has a 400 MHz instantaneous bandwidth and tracks signals whose carrier frequency at the backend input is between 200 and 900 MHz with frequency variation rates greater than 20 MHz/second. The output data is compatible with MECL III logic.

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ABBREVIATIONS AND SYMBOLS

A	Doppler frequency acceleration (Hz/second^2)
A_F	Loop amplifier dc gain (volts/volt)
AGC	Automatic Gain Control
AM-DSB-SC	Amplitude modulation, double sideband, suppressed carrier
B_N	Receiver noise bandwidth (MHz)
B_o	Loop natural frequency = $2\pi f_o$ (radians/second)
$B_{3\ dB}$	Receiver bandwidth at which response is down 3 dB (Hz)
C_{CI}	Ratio of carrier power to total power at input to frequency doubler
C_{co}	Ratio of carrier power to total power at frequency doubler output
C_{so}	Ratio of sideband power to total power at frequency doubler output
D	Doppler frequency rate (Hz/second)
E(P)	Loop tracking error = $\theta_s - \theta_v$ (radians)
f_N	Loop one-sided noise bandwidth (MHz)
f_{PEAK}	Frequency at which loop response is maximum
f_s	Receiver input carrier frequency
f_{sig}	Modulated IF signal
$f_{3\ dB}$	Frequency at which loop response is down 3 dB from zero frequency response (Hz)
G_o	Open loop gain = $G_p A_f G_v$
G_p	Loop phase detector sensitivity (volts per radian at IF)
G_v	VCO tuning sensitivity (radians/seconds per volt)
IF	Intermediate frequency
LO	Local oscillator
MB/s	Megabits per second
N	Receiver noise power in bandwidth B_n (watts)
N_{loop}	Noise power in loop noise bandwidth
P	La Placian operator
S	Total signal power
SNR	Signal-to-noise ratio
S(t)	Baseband signal
T_s	Loop tracking response = θ_v/θ_s
VCO	Voltage controlled oscillator
α	Phase shift keyed carrier suppression factor

θ_s	P plane baseband representation of input signal phase
θ_v	P plane baseband representation of VCO phase
δ	Loop damping function
ω_{peak}	$2\pi f_{peak}$ (radians per second)
$\omega_{3\ dB}$	$2\pi f_{3\ dB}$ (radians per second)
$\triangleq$	Equals by definition

PREFACE

This is the final report on Contract NAS 5-23183 entitled "Wideband Infrared Receiver Backend." The program objectives were the study, development, and the fabrication, of a 10.6 Micrometer Doppler Tracking Receiver Backend. This receiver is to be used to track in frequency and to coherently demodulate the AM-DSB-SC 200 to 900 MHz RF signal output from an infrared heterodyne front end developed at AIL under Contract NAS-5-23119. The two subsystems constitute a preprototype of a spaceborne 300 megabit receiver which will become part of a system designed to demonstrate the feasibility of wideband satellite-to-satellite communications.

The study and design were directed toward providing a reliable high performance receiver suitable for unattended space operation. The receiver configuration chosen during the design phase employs a signal squaring tracking loop to provide the coherent reference required for optimum signal demodulation. This technique was chosen because it is the simplest and most reliable approach to satisfying the receiver's requirements.

The fabricated receiver performed in all respects in accordance with its design specifications, and represents a significant step in demonstrating the feasibility of a high data rate satellite-to-satellite 10.6 micron data link.

1.0 INTRODUCTION

This is the final report describing the design, operation, and configuration of a wideband infrared Doppler tracking receiver backend developed by AIL under Contract NAS-5-23183.

2.0 DESIGN OBJECTIVES

Carrier frequency range	200 to 900 MHz
Rate of carrier frequency change	Greater than 20 MHz/sec
Acquisition time	Less than 60 ms for initial set within ±85 MHz
Instantaneous bandwidth	400 MHz (3 dB)
Modulation	AM-DSB-SC
Noise figure	Less than 5 dB (excluding photomixer)
Data rate	300 MB/s (see Figure 5-12)
Bit error rate	
Automatic gain control (AGC)	15 dB minimum noncoherent
Video output	MECL levels into 50 ohms
Nominal power requirements	≈25 watts

2.1 APPLICATION

This receiver backend was designed to be compatible with a 10.6 micron infrared heterodyne mixer being developed under NASA Contract NAS-5-23119. The combined front and backends will serve as the preprototype of a space-qualified model of a wide-band satellite-to-satellite heterodyne infrared receiving system.

2.2 SIGNAL CHARACTERISTICS

The signal entering the receiver backend from the IR mixer will have a carrier frequency ranging between 200 and 900 MHz (20 MHz/sec maximum rate of change) depending upon the Doppler frequency shift encountered. It will be binary double-sideband amplitude modulated with the carrier being suppressed on the order of 20 dB below the total signal power (which is nearly equivalent to binary phase shift keying). The binary modulation will be NRZ-L with a data bit-rate consistent with the back-end's 400 MHz (3 dB) instantaneous bandwidth.

The anticipated noise power available from the photomixer is on the order of -75 dBm in the receiver's 400 MHz noise bandwidth. Thus, a -65 dBm signal power from the photomixer will provide about a 10-dB SNR when the receiver is quantum noise limited. The back-end's 5-1500 MHz preamplifier (physically located on the photomixer mount) provides a gain of 50 dB to raise these power levels to a range appropriate for further processing. A 10 to 20 dB signal dynamic range is anticipated.

3.0 CANDIDATE TECHNIQUES

3.1 RECEIVER BACKEND REQUIREMENTS

An efficient receiver for the demodulation of the double sideband suppressed carrier (DSB-SC) signals subject to the varying Doppler shifts must perform the following functions (reference 1):

- Obtain a coherent replica of the carrier
- Extract the modulation with minimum error

The manner of performing these functions must be compatible with the receiver design goals of high data rate, wide range of Doppler frequencies, Doppler rate, minimum signal frequency acquisition time, and digital modulation (for which DSB-SC approaches Phase Shift Keying).

3.2 POSSIBLE APPROACHES TO DATA DEMODULATION

The general problem of DSB-SC demodulation has received attention for many years. Reference 2 describes four generalized techniques particularly applicable to digital demodulation. These techniques are:

A. Conventional phase lock loops for carrier extraction that do not make use of sideband energy (Figure 3-1)

B. Squaring loops that extract the carrier replica via a squaring operation on the RF signal (Figure 3-2)

C. Generalized costas loops that perform demodulation while extracting the carrier replica (Figure 3-3)

D. Data aided modulation wipeoff loops that employ decision directed feedback to enhance the signal-to-noise ratio of a standard phase lock loop (Figure 3-4)

Technique (A) is least efficient, while (B) and (C) have nearly identical performance since both make full use of sideband energy via mathematically equivalent operations (references 1, 2, and 3). The last technique (D) is relatively new, but is well described in references 2 and 4.

3.3 SELECTED TECHNIQUE

Figure 3-5 is a generalized block diagram consistent with the four techniques shown on Figures 3-1 through 3-4. Two coherent references are obtained from the Coherent Replica Extractor Block. One reference, the coherent LO, tracks the incoming signal

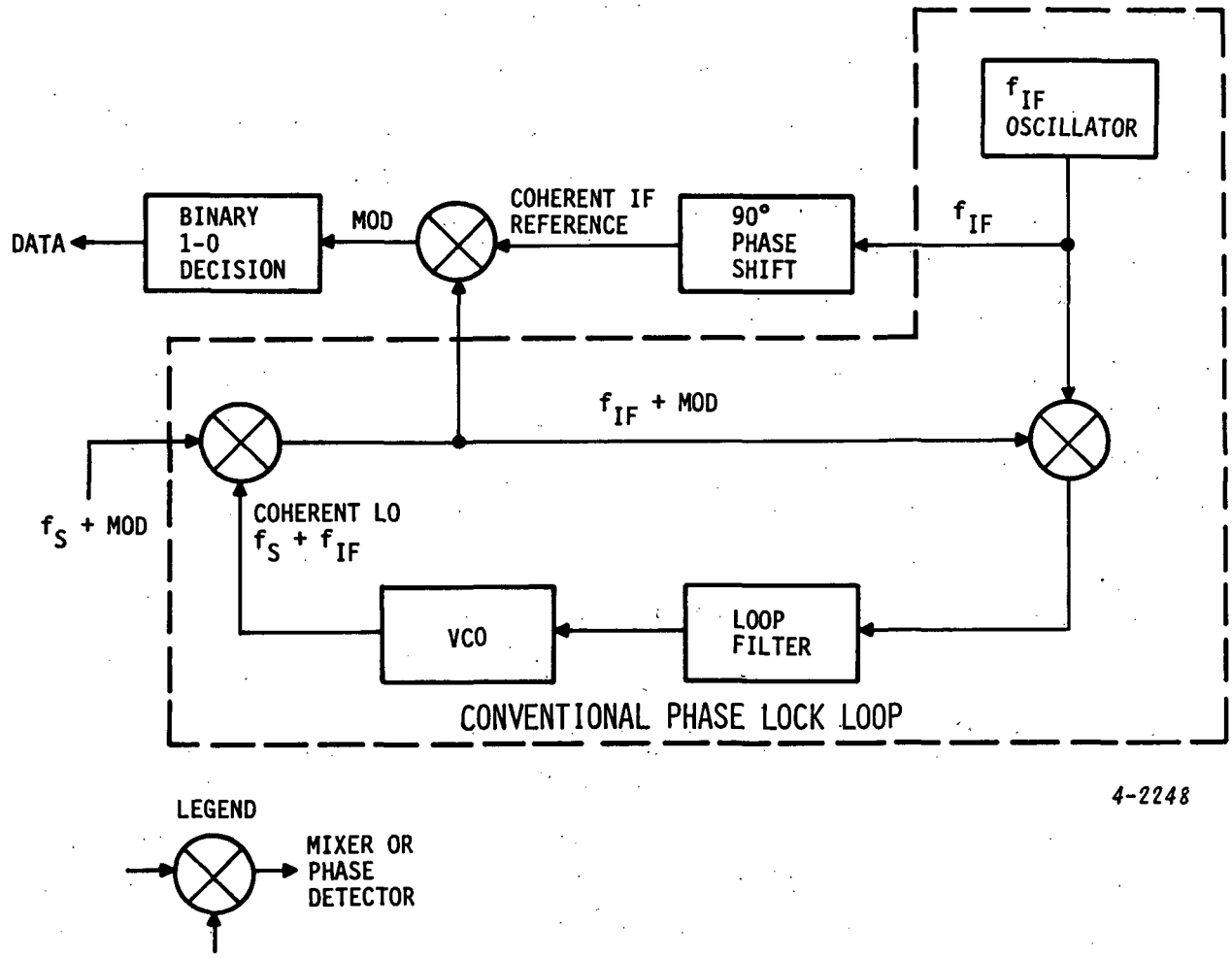


Figure 3-1. Conventional Phase Lock Loop

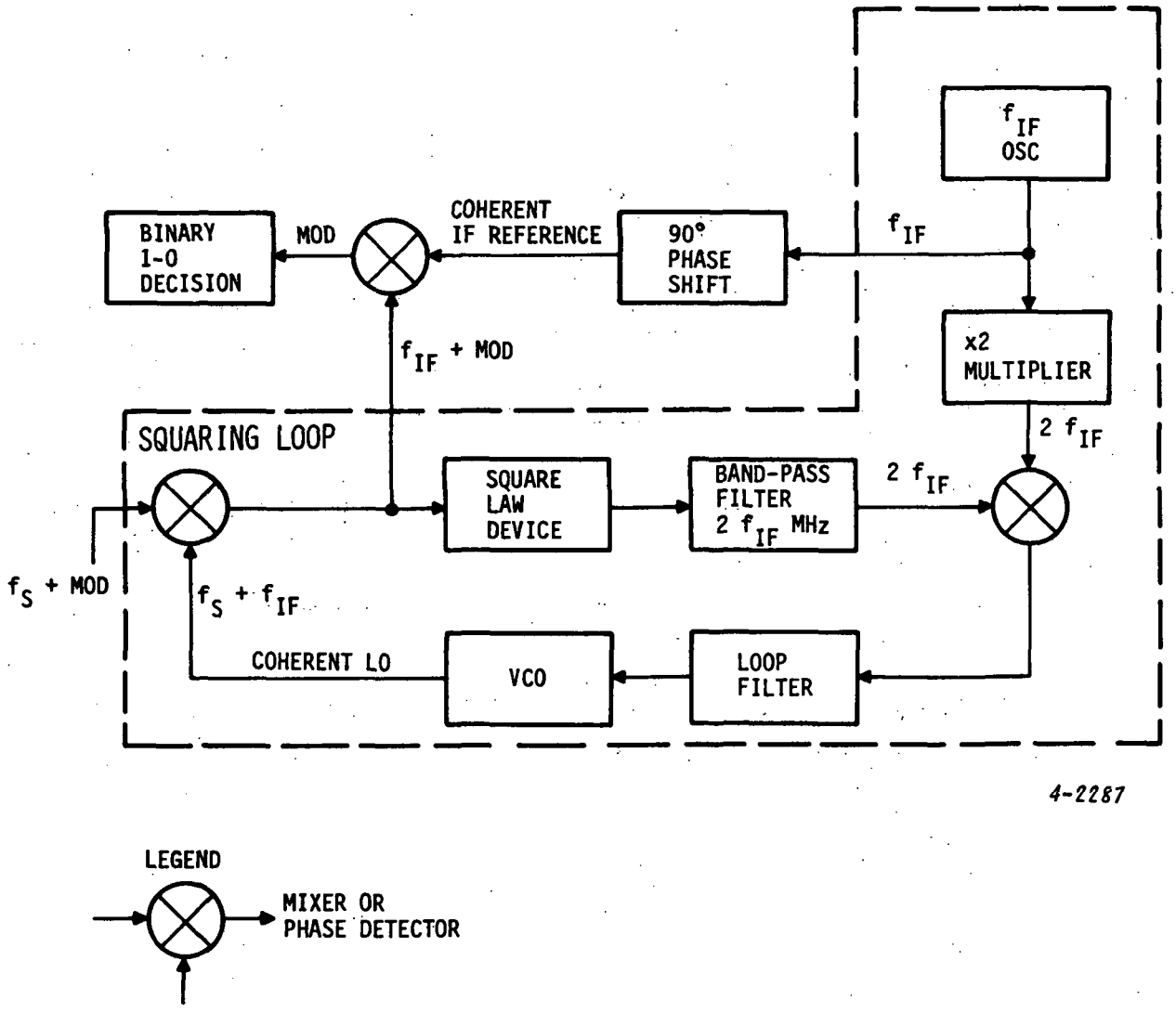


Figure 3-2. Squaring Loop

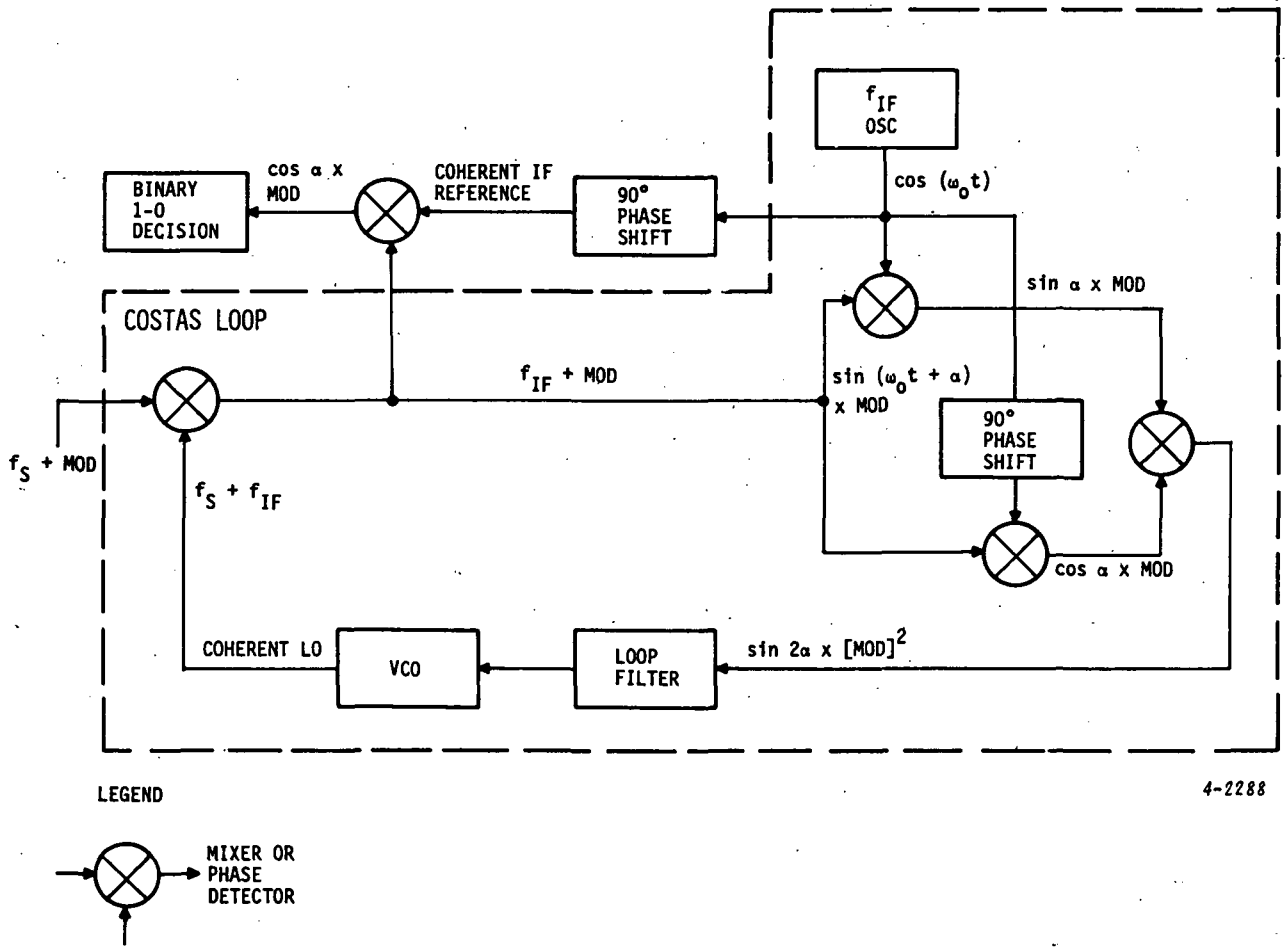


Figure 3-3. Costas Loop

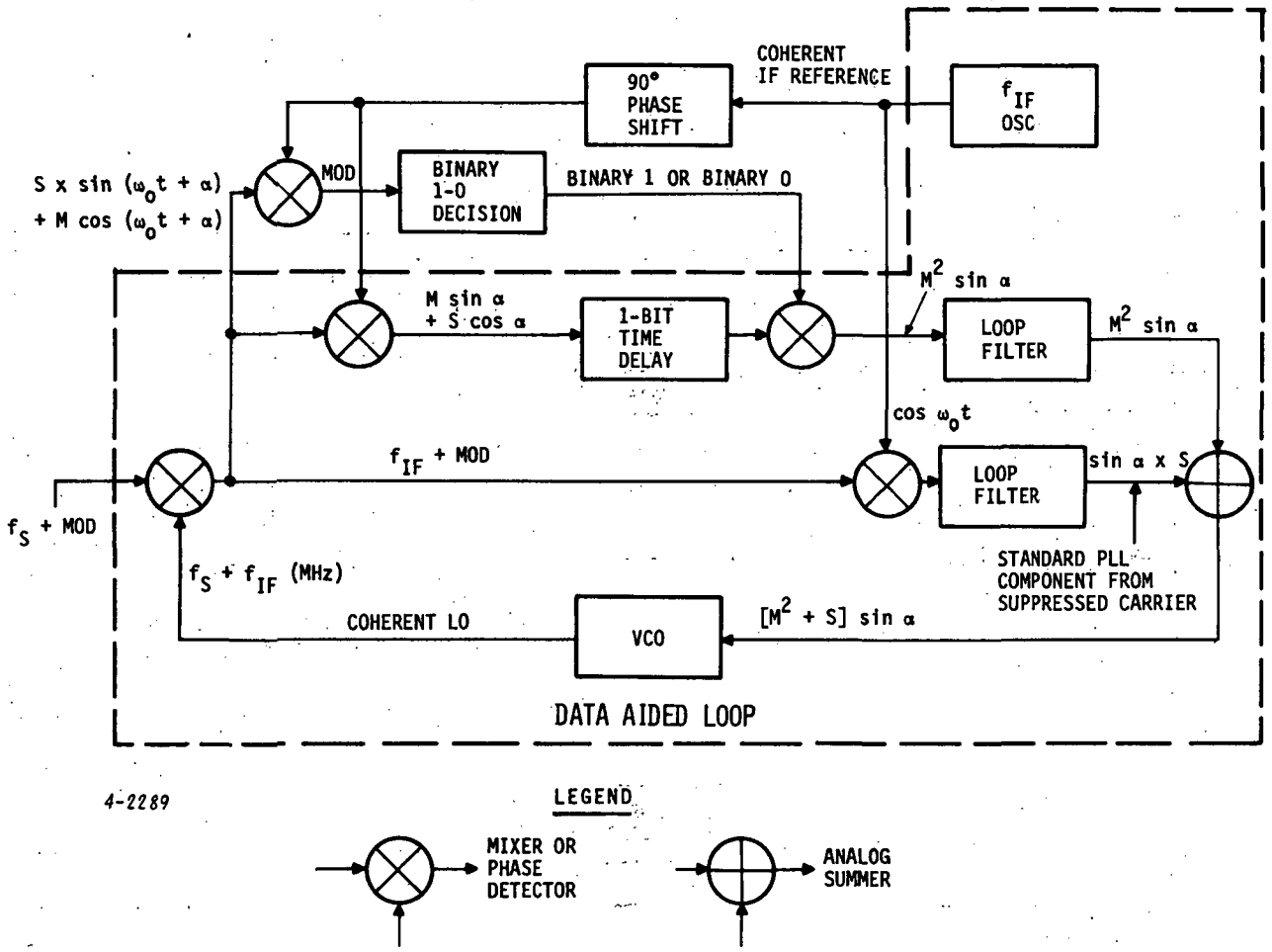


Figure 3-4. Data Aided Loop

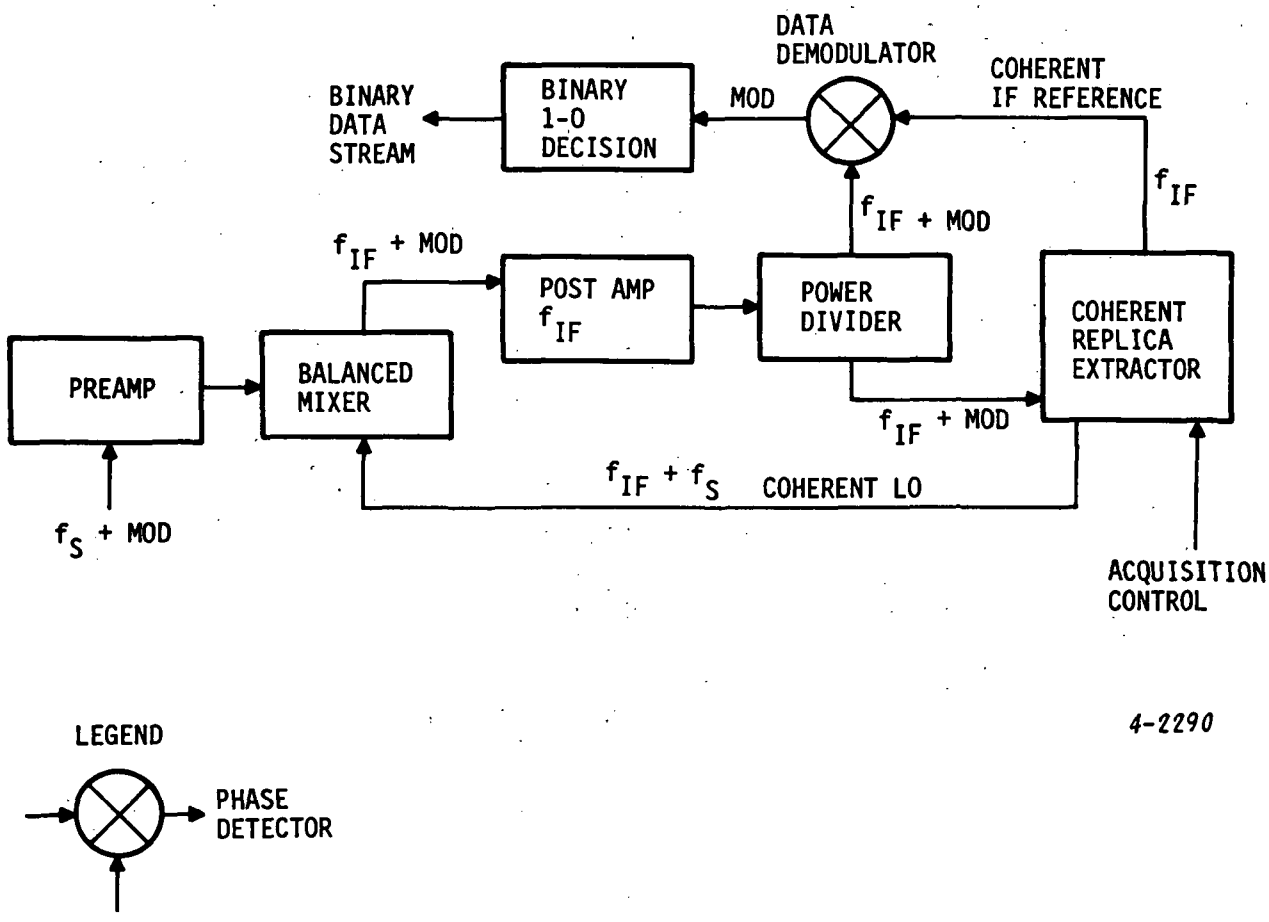


Figure 3-5. Generalized Loop

carrier with a constant frequency offset equal to the receiver's intermediate frequency (IF). This reference is used to coherently translate the incoming signal to its IF. The other reference, the coherent IF reference, is used to coherently demodulate the IF signal. Thus the major design decision that had to be made was selection of the optimum technique for obtaining these two references.

It was realized early in this program that the large ratio of modulation bandwidth (400 MHz), to required tracking loop bandwidth (kHz range), could allow high signal-to-noise ratios in the tracking loop even when the received signal power was low. Thus, sophisticated carrier recovery techniques such as the data aided loop (Figure 3-4) were discarded.

The standard phase lock loop of Figure 3-1 was also discarded since it ignores the energy in the signal sidebands and would present operational difficulties in avoiding false sideband locks.

The choice was then between the mathematically equivalent squaring and Costas loops. The squaring loop was finally chosen as the optimum technique due to its potential for providing the fewest problems during its development when considering the high receiver data rate.

3.4 SIMPLIFIED RECEIVER DESCRIPTION

A simplified block diagram of the developed receiver backend is shown on Figure 3-6. The modulated signal at a carrier frequency of f_s is amplified in a wideband preamplifier (5 to 1500 MHz) to a level of about -10 dBm. It is then upconverted in the first mixer to the IF center frequency of 1500 MHz. (The 1500 MHz center frequency was chosen due to the availability of efficient high performance components at this frequency.) The LO for the mixer is maintained at a frequency of $(1500 + f_s)$ MHz by the tracking loop.

The upconverted signal is then passed through a linear phase band-pass filter (400 MHz = 3 dB bandwidth) after which it is split into two paths. The upper path goes to the data demodulator, while the lower path provides the signal for the tracking loop. The tracking loop signal is further amplified to a level of about +15 dBm and enters the frequency doubler where the bi-phase PSK sideband energy is converted to carrier power at 3.0 GHz (as described in paragraph 4.3). A portion of this 3.0 GHz carrier is then made available to the tracking loop phase detector, where its phase is compared to that of a 3.0 GHz reference derived in a similar manner from a 1500 MHz crystal controlled

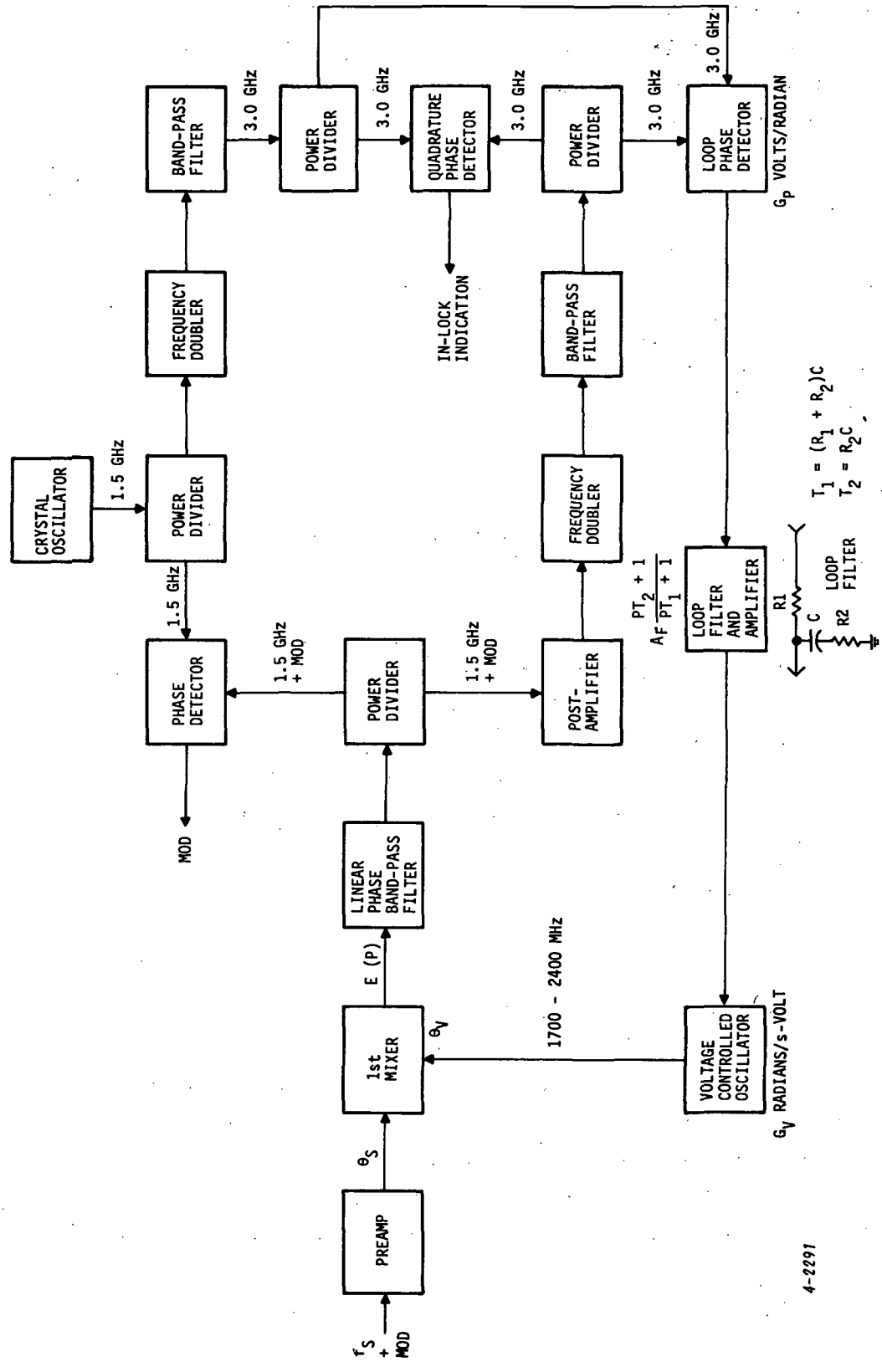


Figure 3-6. Simplified Receiver Block Diagram

reference source. The quadrature phase detector performs the same phase comparison but is in quadrature with the loop phase detector in order to provide an indication of the tracking loop being in lock.

The error voltage from the loop phase detector is appropriately conditioned in the loop filter and amplifier so that the VCO will properly track the changing frequency of the modulated signal.

The 1500 MHz reference is also applied to the data demodulator so that when the VCO is tracking, both inputs to the data demodulator will have the proper phase to demodulate the signal.

4.0 RECEIVER ANALYSIS

4.1 TRACKING LOOP P-PLANE ANALYSIS

The parameters determining the tracking loop characteristics are:

- Loop phase detector sensitivity, G_p volts/radian
- Loop filter transfer function, $1 + T_2P/1 + T_1P$ (Figure 3-6)
- Loop amplifier dc gain, A_F
- VCO tuning sensitivity, G_v radians per second/volt

With no other frequency selective elements of consequence within the loop (for instance, the VCO modulation and the loop amplifier bandwidths being far in excess of the tracking loop bandwidth), the phase transfer function between the first mixer signal input θ_s and its VCO input, θ_v is:

$$\frac{\theta_v}{\theta_s} = \frac{(1 + PT_2)\, K_p\, K_v\, A_F}{P(1 + PT_1) + A_F\, K_p\, K_v\, T_2P + K_p\, K_v\, A_F} \tag{1}$$

and under the easily satisfied condition that $G_oT_2 >> 1$ with $G_o \triangleq K_pK_vA_F$

$$\frac{\theta_v}{\theta_s} = \frac{(1 + PT_2)\, G_o}{T_1\left[P^2 + P\, G_o\, \frac{T_2}{T_1} + \frac{G_o}{T_1}\right]} \tag{2}$$

If we now define the parameters σ and B_o:

$$\sigma \triangleq \frac{1}{2}\sqrt{\frac{G_o\, T_2^2}{T_1}} \tag{3}$$

$$B_o^2 \triangleq \frac{G_o}{T_1} \tag{4}$$

$$\frac{\theta_v}{\theta_s} = \frac{1 + 2\sigma \frac{P}{B_o}}{1 + 2\sigma \frac{P}{B_o} + \frac{P^2}{B_o^2}} \tag{5}$$

which is then the loop tracking response, T(S).

The loop tracking error is E(P)

$$E(P) \triangleq \left(\theta_s - \theta_v\right)$$

$$E(P) = \frac{\theta_s \times P^2/B_o^2}{1 + 2\sigma \frac{P}{B_o} + \frac{P^2}{B_o^2}} \tag{6}$$

Figure 4-1 is a normalized plot of some characteristics of θ_v/θ_s versus the parameter σ. The 3-dB radian frequency $\omega_{3\ dB}$, the frequency ω_{peak}, at which the loop response peak occurs, and the magnitude of the peak are all included. The general literature (reference 11) and our experience indicate that choosing $\sigma = 1/\sqrt{2}$ as a nominal value will provide good noise and tracking performance, which is plotted on Figure 4-2. Then

$$\theta_v/\theta_s = \frac{1 + \sqrt{2}\ \frac{P}{B_o}}{1 + \sqrt{2}\ \frac{P}{B_o} + \frac{P^2}{B_o^2}} \tag{7}$$

$$E(P) = \frac{\theta_s \frac{P^2}{B_o^2}}{1 + \sqrt{2}\ \frac{P}{B_o} + \frac{P^2}{B_o^2}} \tag{8}$$

The one-sided noise bandwidth of the tracking loop, f_N, will then be about $f_N = 2\pi f_o$ Hz, which is about π times the 3-dB loop frequency, $f_{3\ dB}$. ($f_{3\ dB}$ in Hz is about $2 \times f_o$ as shown on Figure 4-2.)

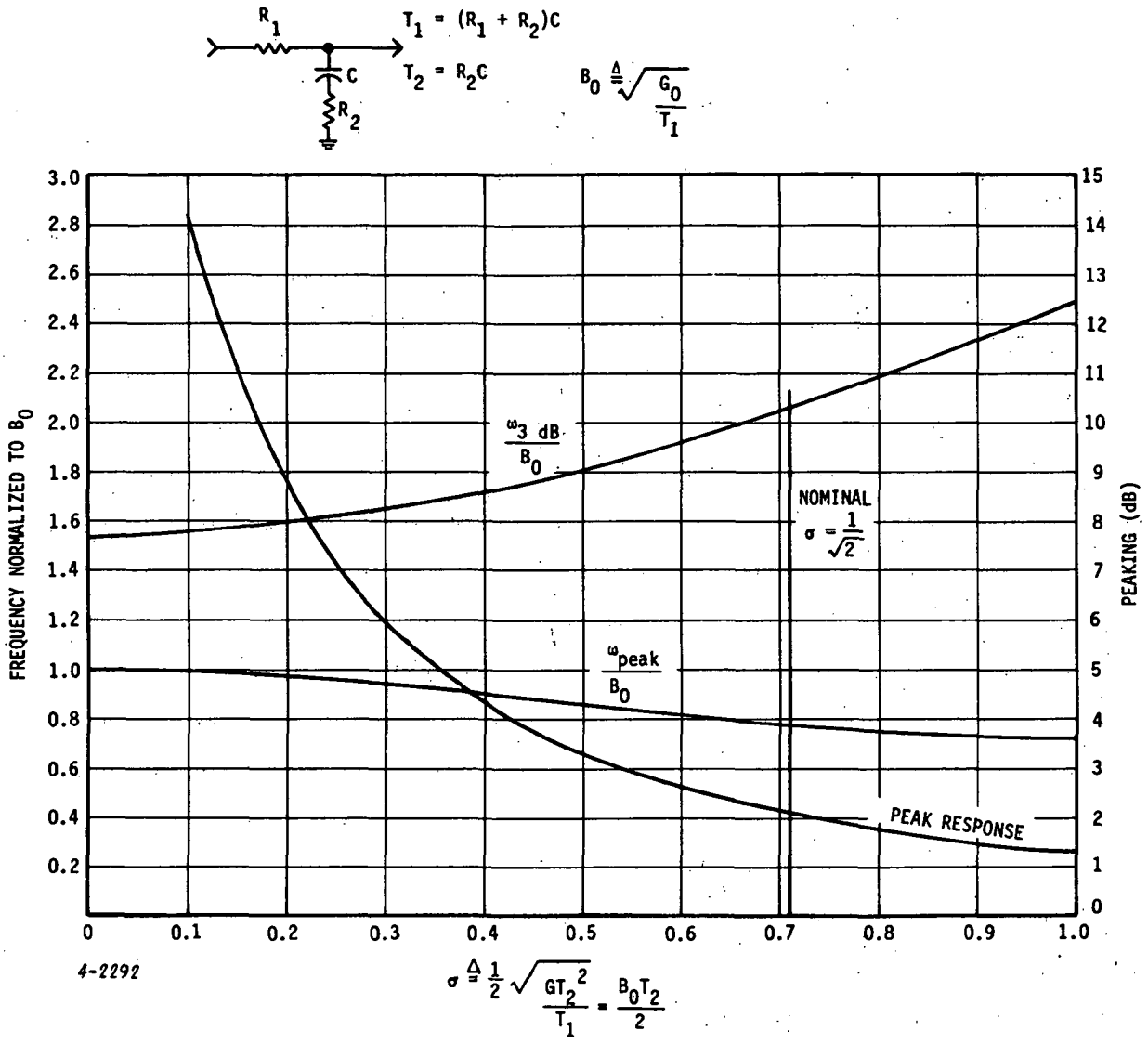
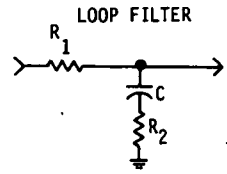


Figure 4-1. Loop Response Versus Damping

$$\sigma = \frac{1}{2}\sqrt{\frac{Gt_2^2}{t_1}} = \frac{1}{\sqrt{2}}$$

$$B_0^2 = \frac{G_0}{t_1}$$

$$B_0 = \frac{\sqrt{2}}{t_2}$$



$$t_1 = (R_1 + R_2)C$$

$$t_2 = R_2C$$

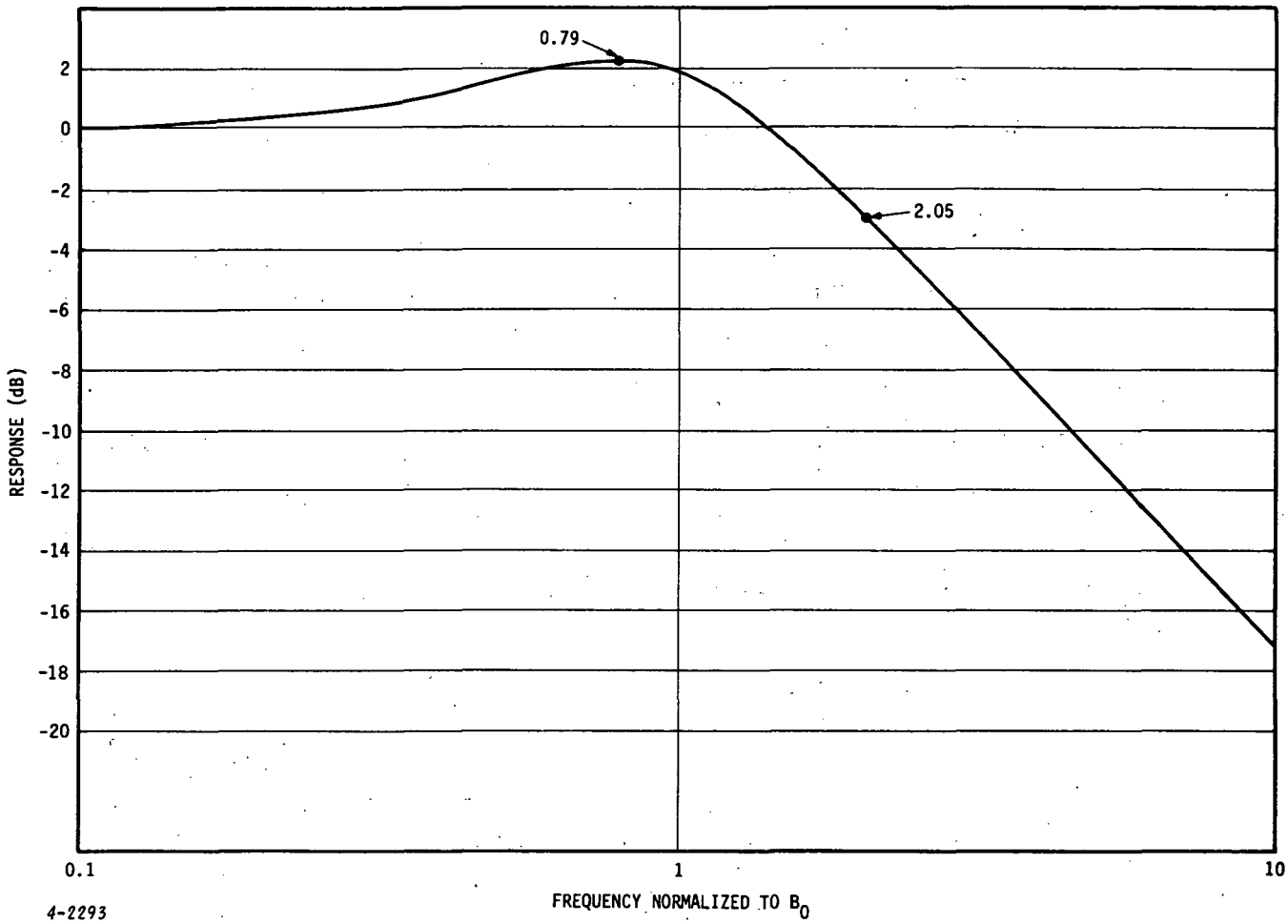


Figure 4-2. Normalized Phase Lock Loop Response

4.2 TRACKING LOOP PARAMETERS

The following lists the nominal magnitudes of the receiver tracking loop parameters:

- VCO sensitivity (G_v) = $2\pi \times 5 \times 10^7$ radians/sec-volt
- Phase detector sensitivity (G_p) = 2×0.1 volts/radian
  (The factor of 2 is due to the frequency doubler)
- Loop dc amplifier voltage gain (A_F) = 600
- T_1 = 0.15 second
- $T_2 = 2.7 \times 10^{-6}$ seconds

With $B_o = \sqrt{\frac{G_v G_p A_F}{T_1}} = 5.01 \times 10^5$ radians/sec, f_o = 79.8 kHz; from equation 4, and

$$\sigma = \frac{1}{2}\sqrt{\frac{G_v G_p A_F T_2^2}{T_1}} = 0.68 \text{ from equation 3.}$$

The loop one-sided noise bandwidth, $f_N = 2\pi f_o$ Hz, is $\approx 2\pi \times 79.8$ kHz = 501 kHz.

The phase detector sensitivity of 0.2 volt/radian and the loop amplifier voltage gain of 600 provide a 120 volt/radian error sensitivity for the VCO. Thus, with the VCO sensitivity of about 50 MHz/volt, 700/50 = 14 volts of VCO correction voltage is required to tune the VCO over a 700 MHz range. This is obtained by 14/120 = 0.12 radians change at the demodulator phase detector.

The measured tracking loop frequency response is shown on Figure 4-3 and shows good agreement with theory and Figure 4-2.

4.3 FREQUENCY DOUBLER ANALYSIS

The form of the noiseless modulated IF signal with suppressed carrier is:

$$f_{sig} = \sqrt{2}\, S(t) \cos \omega_{IF} t + \sqrt{2}\, \alpha \cos (\omega_{IF} t + \theta) \qquad (9)$$

where S(t) is either plus or minus unity, ω_{IF} is the IF center radian frequency, α is a constant defining the degree of carrier suppression, and θ is some arbitrary phase reference. The constraint of finite bandwidth will slow down the state transitions, and group delay distortion will further change the signal from this form. However, this analysis will not consider such signal disturbances.

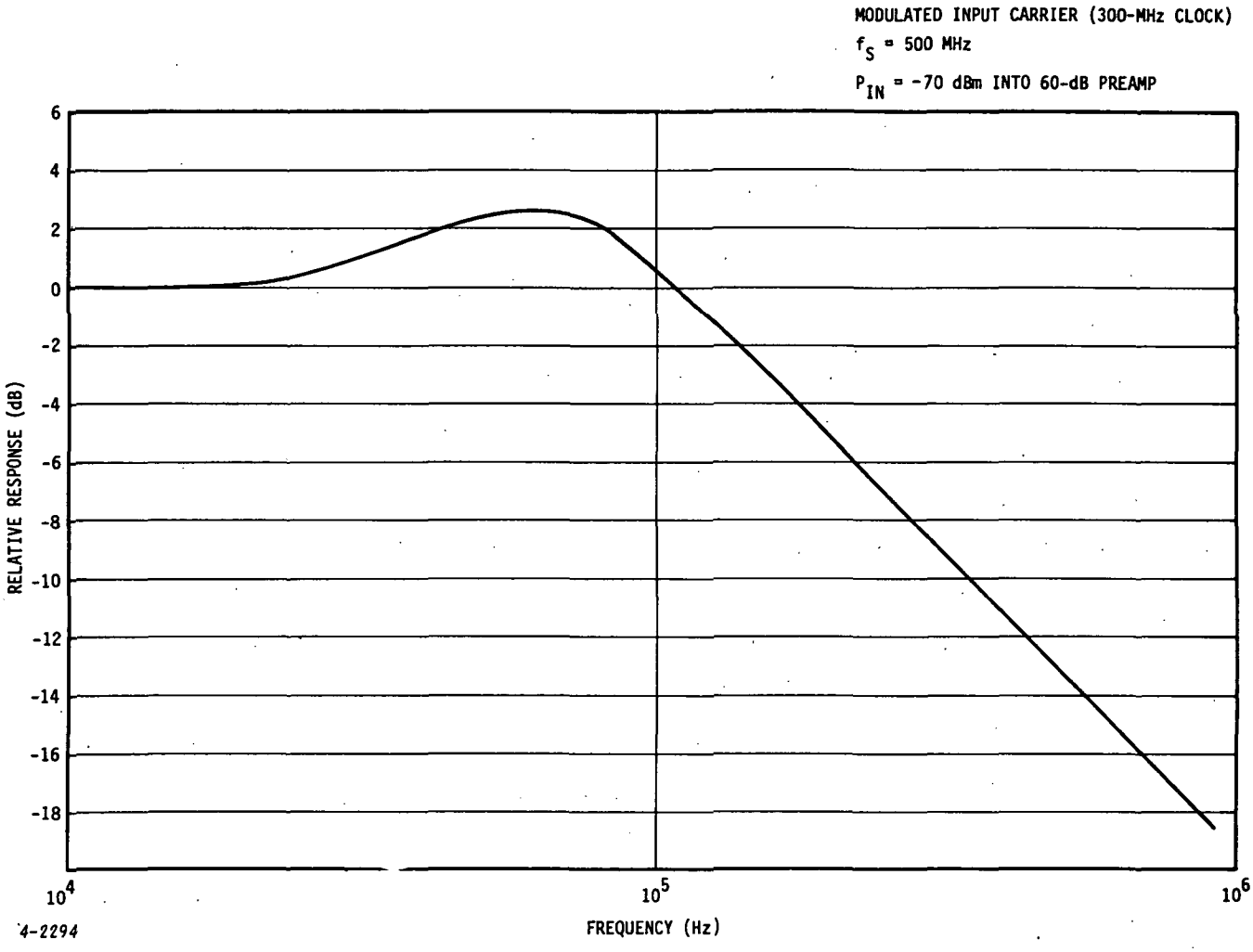


Figure 4-3. Measured Tracking Loop Frequency Response

The total signal power is $(1 + \alpha^2)$ when the long term average of S(t) is zero; $\alpha^2/1 + \alpha^2$ being defined as the carrier suppression ratio.

$$C_{CI} \triangleq \frac{\alpha^2}{1 + \alpha^2} \tag{10}$$

After a squaring process the signal becomes f_{sig}^2 at frequency $2\omega_{IF}$ which may be expressed as the sum of two orthogonal components with K being the doubling constant.

$$\begin{aligned} f_{sig}^2 = K \left[2\, S(t)\, \alpha \cos \theta + S(t)^2 + \alpha^2 \cos 2\theta \right] \cos 2\omega_{IF} t \\ - K \left[2\, S(t)\, \alpha \sin \theta + \alpha^2 \sin 2\theta \right] \sin 2\omega_{IF} t \end{aligned} \tag{11}$$

The modulation sideband components in f_{sig}^2 are described by:

$$2\, KS(t)\, \alpha(\cos \theta \cos 2\omega_{IF} t - \sin \theta \sin 2\omega_{IF} t)$$

while the restored carrier is:

$$K \left[S(t)^2 + \alpha^2 \cos \theta \right] \cos 2\omega_{IF} t - K \alpha^2 \sin 2\theta \sin 2\omega_{IF} t$$

The sideband power, with $S(t) = \pm 1$ and the long term average of S(t) being zero, is then $2K^2 \alpha^2$ and the carrier power is

$$\frac{1}{2} K^2 \left[(1 + \alpha^2)^2 - 4\alpha^2 \sin^2 \theta \right]$$

Thus the doubler output has a ratio of sideband power to total output power of C_{so}.

$$C_{so} \triangleq \frac{1}{1 + \dfrac{1}{4\, C_{CI} (1 - C_{CI})} - \sin^2 \theta} \tag{12}$$

A plot of the doubler output sideband suppression C_{so} versus the input carrier suppression C_{CI} is shown on Figure 4-4 for the limiting cases of θ equaling zero and $\pi/2$.

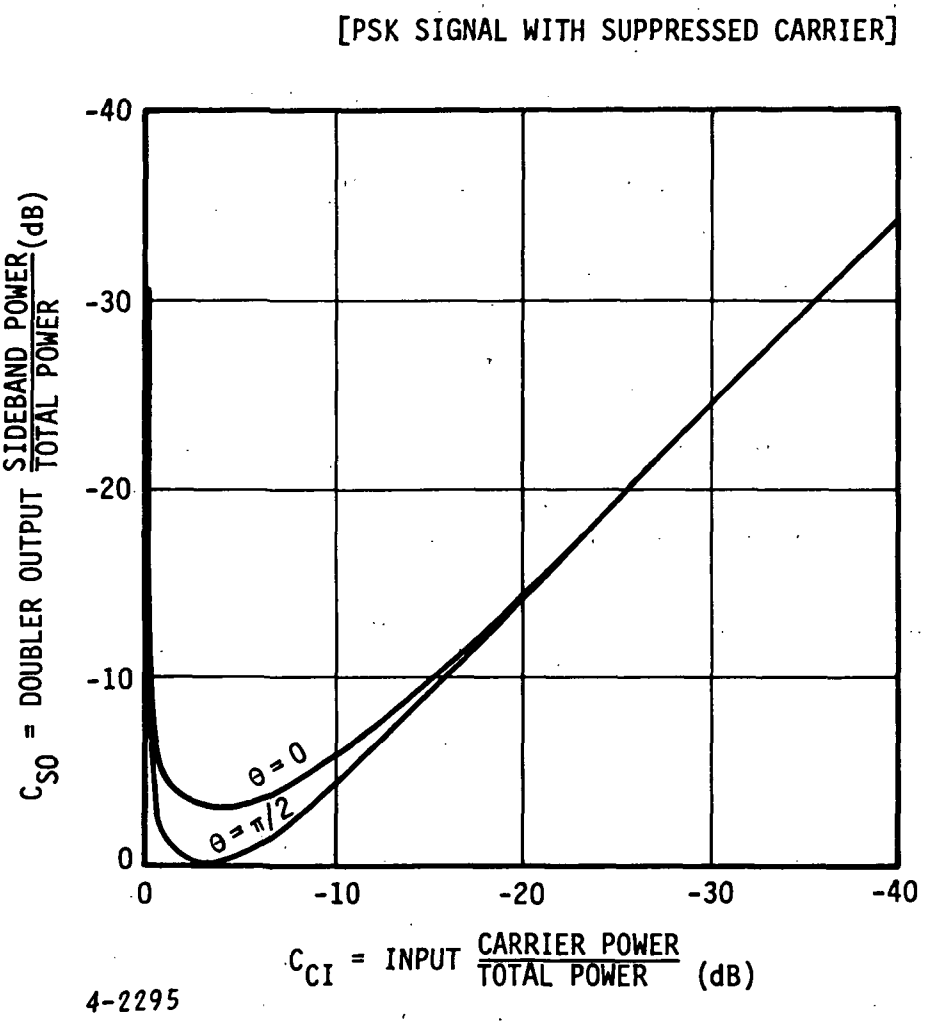


Figure 4-4. Theoretical Frequency Doubler PSK Sideband Suppression

The efficiency of the frequency doubler in extracting the carrier reference is C_{co}, the ratio of the doubler output carrier power to its total output power.

$$C_{co} \triangleq \frac{1 - 4\,C_{CI}\,(1 - C_{CI})\,\sin^2\theta}{1 + 4\,C_{CI}\,(1 - C_{CI})\,(1 - \sin^2\theta)} \tag{13}$$

This efficiency is plotted versus C_{CI} on Figure 4-5 for the limiting cases of θ equaling zero and $\pi/2$. It is evident from this figure that the doubler efficiency may degrade rapidly as the input carrier suppression decreases below 10 dB.

4.4 SIGNAL-TO-NOISE RATIO

The receiver signal-to-noise ratio (SNR) is determined by the receiver's noise figure, its noise bandwidth, and the signal power within this bandwidth.

The noise power, referred to the optical mixer output, is $(-114 + 10 \log B_N + NF)$ in dBm where B_N is the receiver noise bandwidth in MHz and NF is the ratio (expressed in dB) of the effective noise temperature (in kelvins) at the optical mixer output to 290 K. The noise bandwidth of this receiver is determined by the IF band-pass filters and is about 400 MHz, the receiver's 3-dB bandwidth, and the receiver noise figure is about 15 dB (4 dB for backend alone). Thus the preamplifier equivalent input noise power is about $(-114 + 26 + 15) = -73$ dBm (-84 dBm for backend alone). The minimum operating SNR anticipated within the 400 MHz noise bandwidth is about 10 dB. However, this SNR is increased within the tracking loop due to the loop's narrower bandwidth, as shown by the following.

Given a White-Gaussian noise power N in the IF bandwidth B_N, and ideal frequency doubling of the signal (that is, all sideband energy converted to carrier power) whose power at the frequency doubler input is S, the SNR within the tracking loop can be determined.

The doubler output signal power will be $S^2/2$ and the effective noise power in the one-sided loop noise bandwidth f_N is:

$$N_{loop} = N \frac{f_N}{B_N} (2S + N) \text{ when } f_N << B_N \tag{14}$$

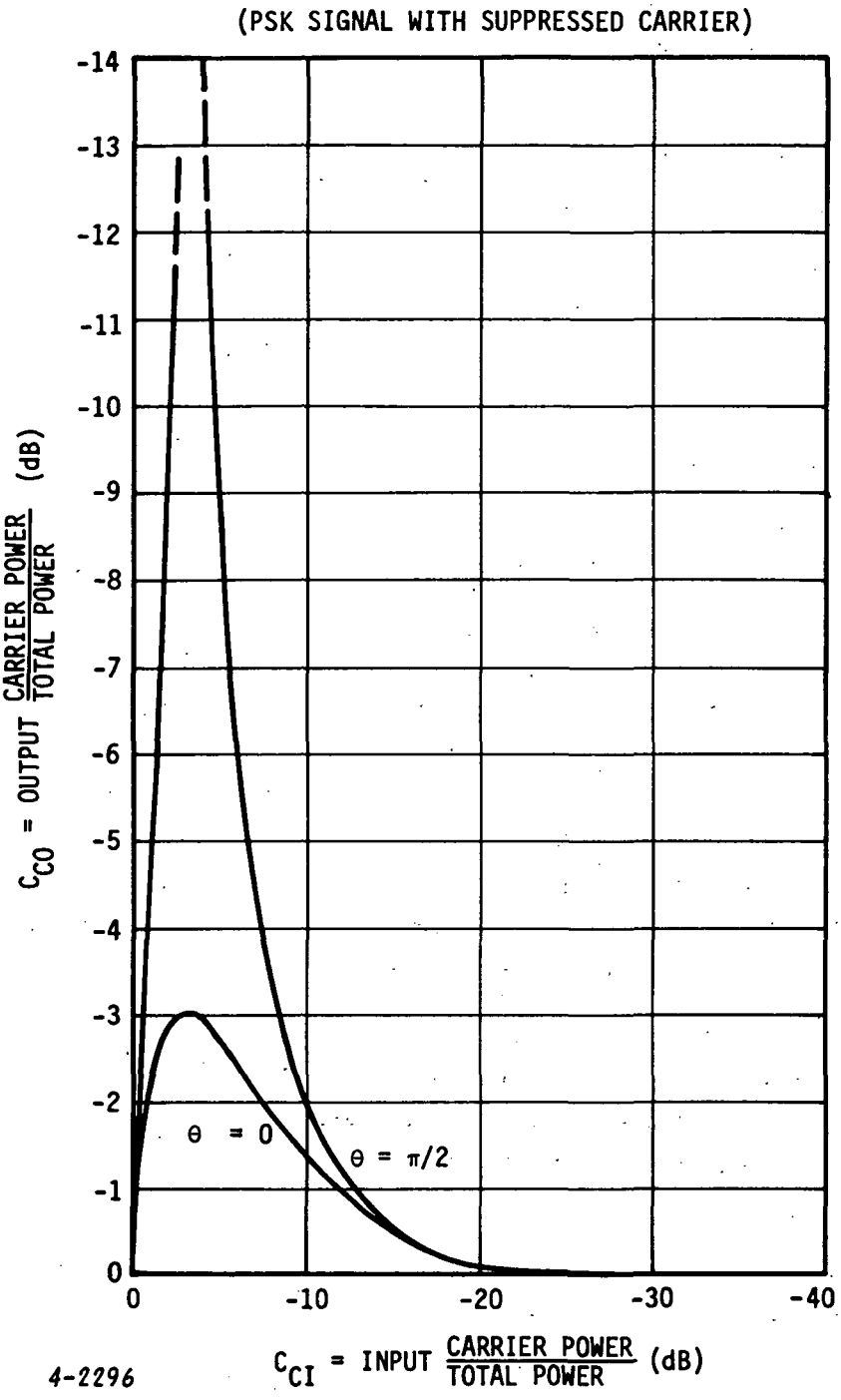


Figure 4-5. Theoretical Frequency Doubler Efficiency

Using linear analysis the loop SNR will be:

$$SNR_{loop} = \left(\frac{S}{N}\right)_{IF} \times \left[4\,\frac{f_N}{B_N}\,\left(1 + \frac{N}{2S}\right)\right]^{-1} \qquad (15)$$

Paragraph 4.2 indicates that the loop noise bandwidth is about 0.5 MHz. Thus, SNR_{loop}

$$SNR_{loop} = \left(\frac{S}{N}\right)_{IF} \times \frac{1}{\frac{4 \times 0.5}{400}\left(1 + \frac{N}{2S}\right)}$$

$$SNR_{loop} = \left(\frac{S}{N}\right)_{IF} \times \frac{1}{5.0 \times 10^{-3}\left(1 + \frac{N}{2S}\right)} \qquad (16)$$

which provides about a 23 dB improvement in SNR_{loop} for $\left(\frac{S}{N}\right)_{IF}$ greater than 10 dB.

4.5 RESPONSE TO FREQUENCY TRANSIENTS

The transient phase error E(P) is of interest when tracking Doppler shifted signals.

$$E(P) = \frac{\theta_s \left(\frac{P}{B_o}\right)^2}{1 + \sqrt{2}\,\frac{P}{B_o} + \left(\frac{P}{B_o}\right)^2} \qquad (17) \text{ from equation 8}$$

A Doppler shifted signal will generally have both a linear and a quadratic component. The signal $f_s = Dt + At^2$ with $t \geq 0$ may be considered a worst case Doppler representation for a satellite communications link since its P plane representation indicates a discontinuity at t = 0. Since

$$f \triangleq \frac{d\theta}{dt}, \quad \theta_D = 2\pi \int f_s\, dt$$

$$\theta_D = \left(+\frac{1}{2}\,Dt^2 + \frac{1}{3}\,At^3\right) 2\pi \qquad (18)$$

The first term represents the Doppler rate (D Hz/sec); the second term the Doppler acceleration (A Hz/sec^2). In P plane notation with $t \geq 0$, the linear model tracking loop baseband input is $\theta_s = \left[+D/P^3 + 2\,A/P^4 \right] 2\pi$. Thus,

$$E(P) = + \frac{\frac{D}{B_o^2} \times 2\pi}{P\left[1 + \sqrt{2}\,\frac{P}{B_o} + \left(\frac{P}{B_o}\right)^2\right]} + \frac{2A/B_o^2 \times 2\pi}{P^2\left[1 + \sqrt{2}\,\frac{P}{B_o} + \left(\frac{P}{B_o}\right)^2\right]} \tag{20}$$

The equivalent time response is:

$$E(t) = \frac{2\pi D}{B_o^2}\left[1 - \sqrt{2}\, e^{\frac{-B_o}{\sqrt{2}}t} \sin\left(\frac{B_o t}{\sqrt{2}} + \pi/4\right)\right] \text{ radians}$$

$$+ \frac{2\pi 2A}{B_o^2}\left[t - \frac{\sqrt{2}}{B_o}\left(1 - e^{\frac{-B_o}{\sqrt{2}}t} \cos\frac{B_o}{\sqrt{2}}t\right)\right] \text{ radians} \tag{21}$$

The asymptotic value for the phase error E(t) is $2\pi D/B_o^2$ radians due to Doppler rate and $4\pi A/B_o^2\, t$ radians due to the Doppler acceleration at large values of t.

Thus a Doppler rate, D, of 20 MHz/second will cause a maximum phase error of about 5×10^{-4} radians (0.03 degree) for a tracking loop such as that of the developed receiver whose B_o is 5×10^5 radians/second (80 kHz). A similar phase error will occur when the ratio of the Doppler acceleration, A Hz/sec^2, to its duration in seconds is about 10^7.

Figure 4-6 shows the receiver's tracking loop response to a simulated Doppler frequency shift contour whose maximum rate is about 90 MHz/second. The loop phase variation with time, shown on the figure, is indistinguishable from that of steady state variations to slow frequency changes, indicating that the receiver's performance will not be affected by the anticipated Doppler dynamics.

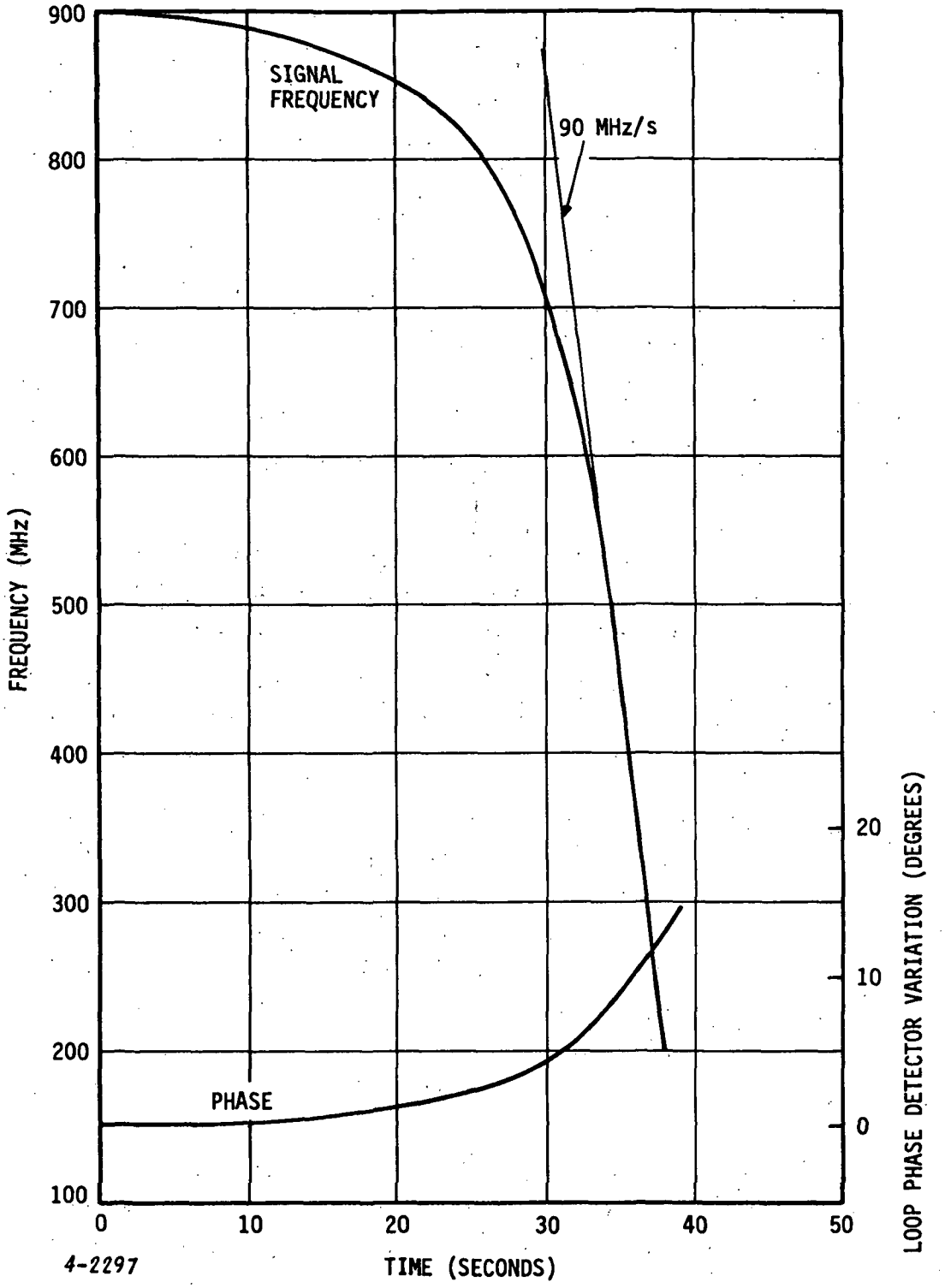


Figure 4-6. Measured Response to Simulated Doppler Signal

4.6 FREQUENCY ACQUISITION

Frequency acquisition (the locking of the tracking loop to the incoming signal f_s) is accomplished through both manual and automatic operations. Manual tuning of the VCO places its frequency in the vicinity of the correct value, so that a triangular type automatic frequency sweep may complete the acquisition. The sweep searches about 170 MHz each 120 milliseconds, until the VCO places the IF signal within the acquisition range of the tracking loop, at which time the sweep is stopped. Thus an initial preset of the VCO frequency to within 85 MHz of its proper value will ensure lock within 120 milliseconds.

4.7 RECEIVER GAIN CONTROL

Two automatic gain control (AGC) loops, each with 1 second time constant filters, are provided within the receiver. The first loop provides about 15 dB of control prior to the first mixer. This functions to maintain the signal level into the data demodulator at a near constant level.

The second AGC loop has more than 35 dB of control and is located in the IF path of the tracking loop. Its purpose is to maintain the frequency doubler input power constant, so that the tracking loop gain will not be a function of signal level.

The receiver AGC permits operation with optical mixer output signal levels between approximately -75 and -40 dBm, covering SNR values between approximately 0 and 30 dB.

4.8 DIGITAL DATA PROCESSING

It is apparent from all of the references previously cited, that matched filter or synchronously controlled integration (integrate and dump) of the demodulated signal, during each bit period followed by a 1-0 decision based on the integrated signal value at the end of the bit period, is the optimum method of binary signal detection. However, the difficulties anticipated in implementing this matched filter technique at the high bit rates expected do not seem justified, considering the small advantage it would provide over much simpler approaches as shown in Figure 6-9, p 289, of reference 14. It is shown there that less than 1 dB of signal degradation is to be expected due to the use of linear filters.

The digital data processing approach chosen for this receiver shapes the signal spectrum at IF with the Bessel band-pass filter, and then restores the binary logic levels, after demodulation, with logic elements having 1-0 thresholds symmetrical about the signal zero input voltage.

Note that it is inherent within a squaring loop system that the data output, for either input data state, has two possible equi-probable phases differing by 180 degrees. Thus, binary transition coding is the desirable data coding.

5.0 RECEIVER BACKEND DESCRIPTION

5.1 BLOCK DIAGRAM

The block diagram of the receiver backend is shown in Figure 5-1. This figure includes the control functions and signal monitors available at the backend control panel. This block diagram is a detailed version of the simplified receiver described in paragraph 3.4.

5.2 PRINCIPAL RF COMPONENTS

The following is a listing of the receiver backend's principal components and their significant characteristics.

- AGC - Amp 1--This amplifier has a gain controllable nominally between -5 and +10 dB over a frequency range of 5 to 1500 MHz (A-1).
- Amp 2--This amplifier has a nominal gain of 17 dB between 1 and 2 GHz (A-2).
- Amp 3--This amplifier has a nominal gain of 30 dB between 1 and 2 GHz and a 1 dB gain compression at +30 dBm output power (A-3).
- Amp 4--This amplifier, used to amplify the demodulated signal, has a nominal gain of 40 dB from 0.01 to 400 MHz (A-4).
- MECL 1-0 Decision--This block consists of a differential MECL line receiver whose output is at MECL logic levels (A-5).
- VCO--This device may be tuned between 1.5 and 3.0 GHz with a nominal output power of +23 dBm. Its tuning characteristic is shown in Figure 5-2 (O-1).
- 1.5 GHz Oscillator--This oscillator is phase locked to an internal crystal controlled source and has an output power level of about +24 dBm (O-2).
- Mixer 1--This mixer is a doubly balanced device with a measured conversion loss of less than 5 dB (M-1).
- Mixers 2 and 3--These devices are doubly balanced with IF port responses extending down to dc and conversion losses and dc offsets optimized for 3.0 GHz LO and RF inputs (M-2 and M-3).
- Mixer 4--This mixer is doubly balanced with the frequency response of its RF and LO ports being between 1 and 2 GHz and its IF port between dc and 600 MHz (M-4).
- Bandpass Filter, Bessel--This is a 5-pole linear phase filter (F-1). Its frequency response is shown in Figure 5-3.

- Bandpass Filter, 1.35 to 1.65 GHz--This filter is centered at 1.5 GHz with a 3 dB bandwidth of 314 MHz. It has greater than 40 dB rejection to frequencies greater than 1700 MHz and lower than 1300 MHz (F-2).
- Bandpass Filters, 2.85 to 3.15 GHz--These filters are nominally 300 MHz wide with rejections of 68 dB at 1.5 GHz and 59 dB at 4.5 GHz (F-3 and F-4).
- AGC-2 Gain Control--This unit is a controllable absorptive modulator with greater than 35 dB of available isolation in the frequency range of 1-2 GHz (G-1).

5.3 CIRCUIT DIAGRAMS

The circuits described in paragraphs 5.3.1 and 5.3.2 are all contained within the backend control chassis.

5.3.1 Backend Frequency Control

A schematic of the backend frequency control circuits is shown in Figure 5-4. This schematic depicts:

- The tuning voltage amplifier U6 which amplifies with unity gain the tuning voltage from the backend control.
- The loop amplifiers U7, Q2, and Q3 which amplify the loop phase detector output with a gain of about 56 dB at dc.
- The loop filter elements R28, R29, and C6 which serve as the feedback components of U7.
- The acquisition sensing components U1, CR1, CR2, and U2 (with low-pass filter components R3 and C1) which amplify and filter the quadrature phase detector output. The gain of dc amplifier U1 is controlled by R2.
- The sweep oscillator U3, U4, and U5 which produces a triangular waveform with a period of 0.125 seconds and a peak-to-peak amplitude of about 2 volts at the output of U4.
- The sweep-stop transistor Q1 which stops the sweep when the output of U2 rises to about +10 volts, or when the stop sweep control terminal is brought to about +5 volts.
- The summing amplifier U8 which sums the outputs of the tuning voltage amplifier U6 and the sweep output from U4 for further amplification by Q2 and Q3.

5.3.2 Backend AGC Amplifiers

A schematic of these amplifiers is shown in Figure 5-5. U9 amplifies the AGC-1 detector output with gain controlled by R-74. AGC-1 control becomes active when the output voltage of U9 exceeds the voltage threshold established by R59 and R60 at which time the negative output voltage of U10 controls the gain of Amp-1.

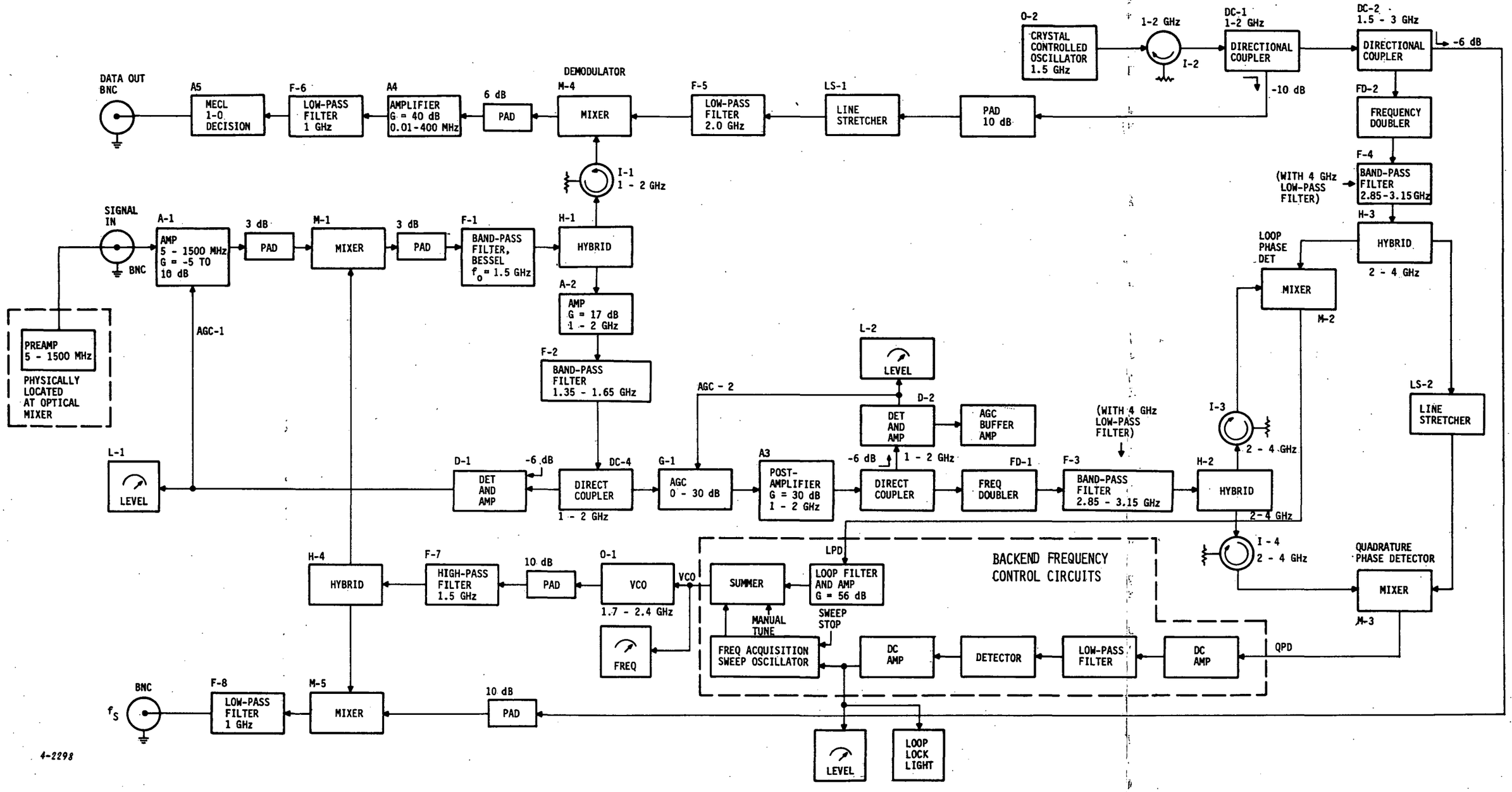


Figure 5-1. Receiver Backend Block Diagram

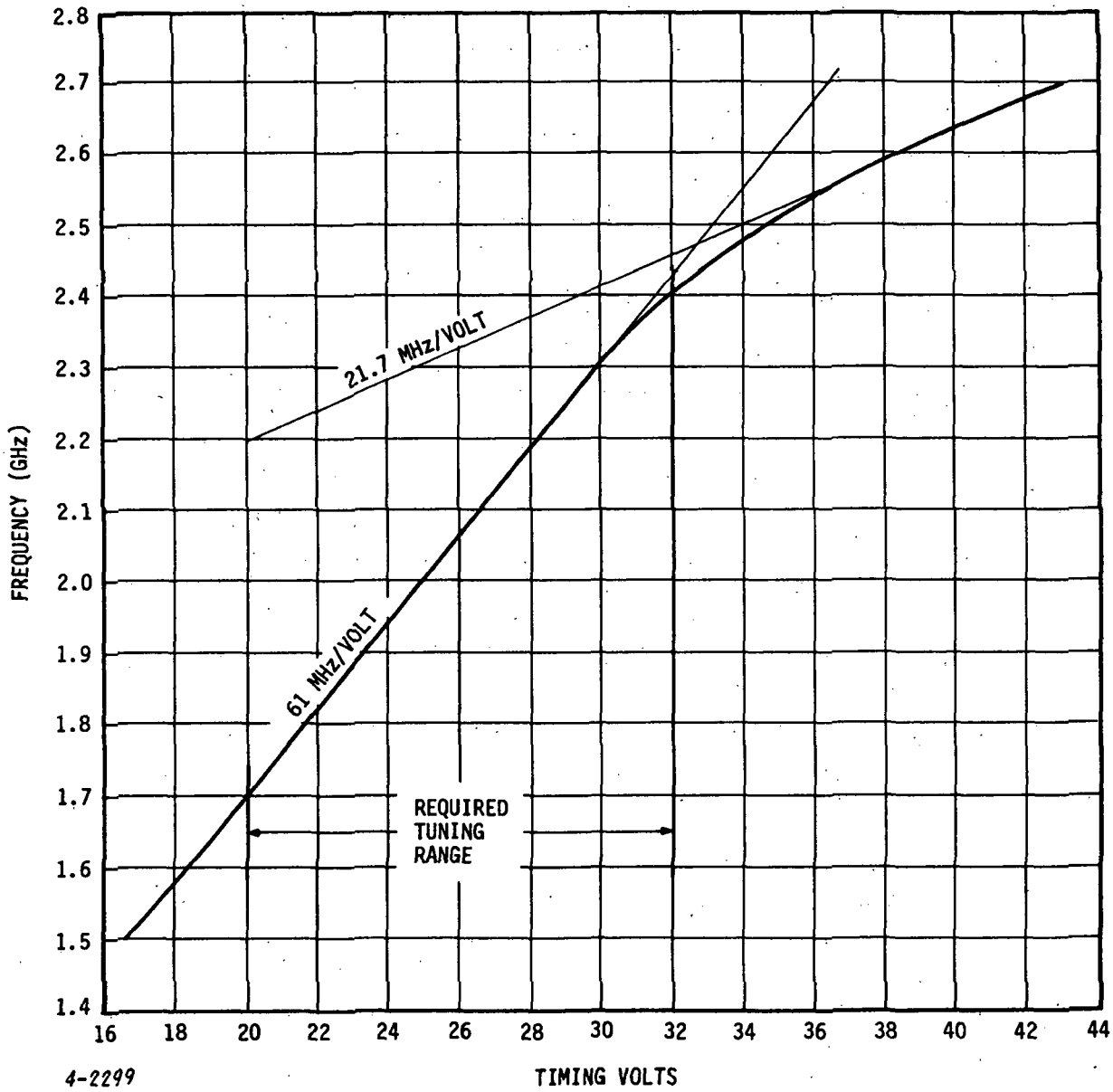


Figure 5-2. VCO Tuning Characteristics

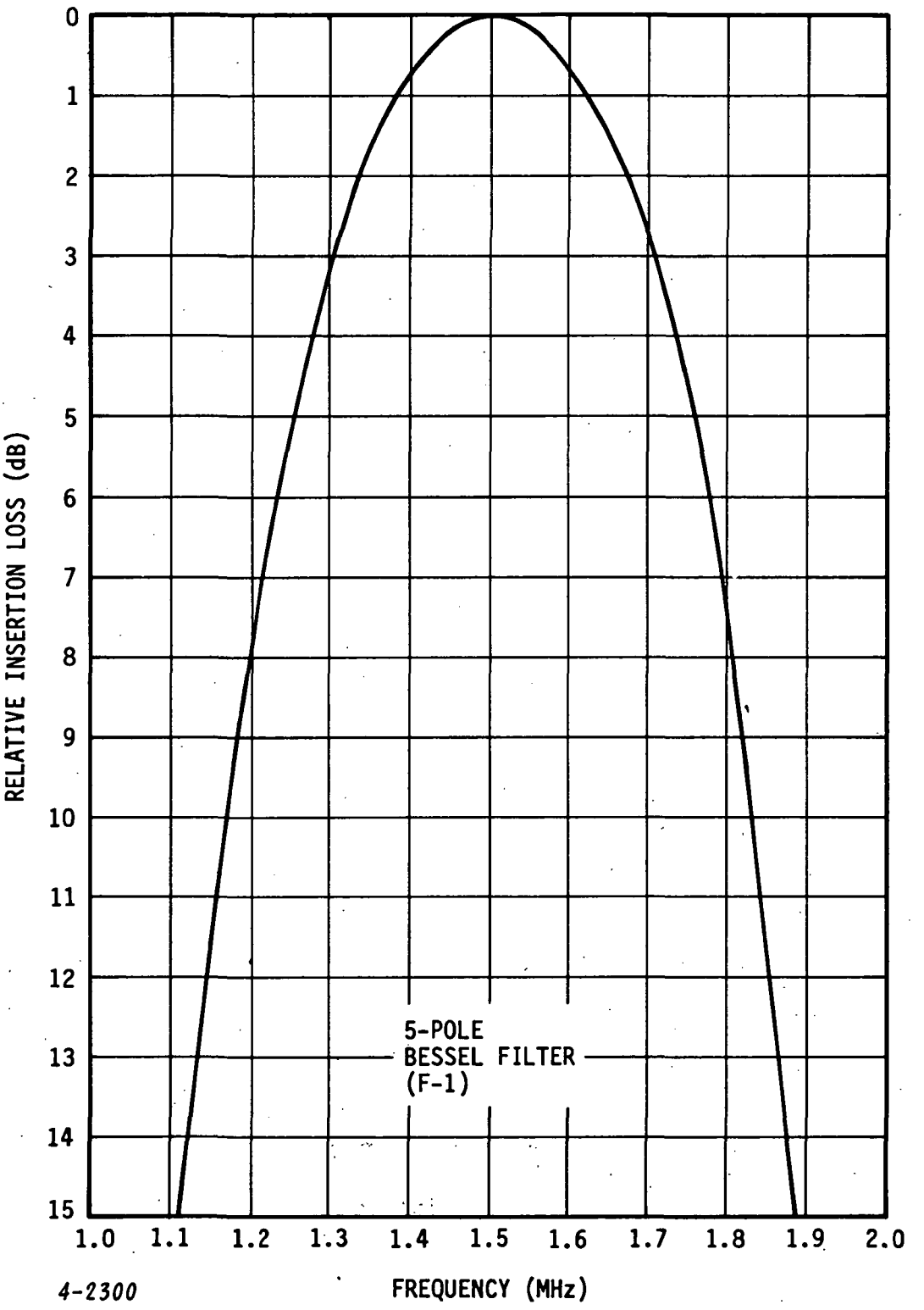
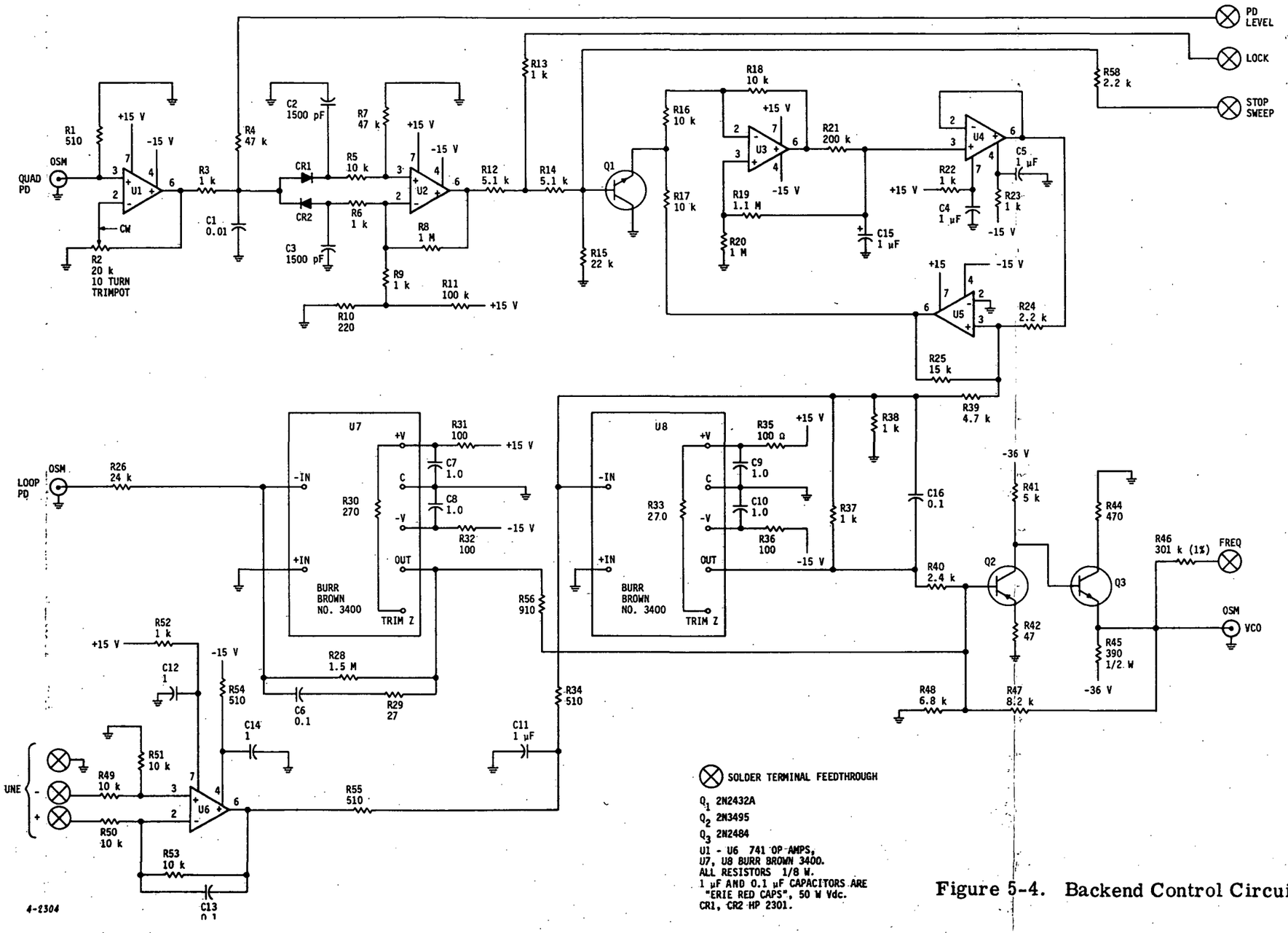


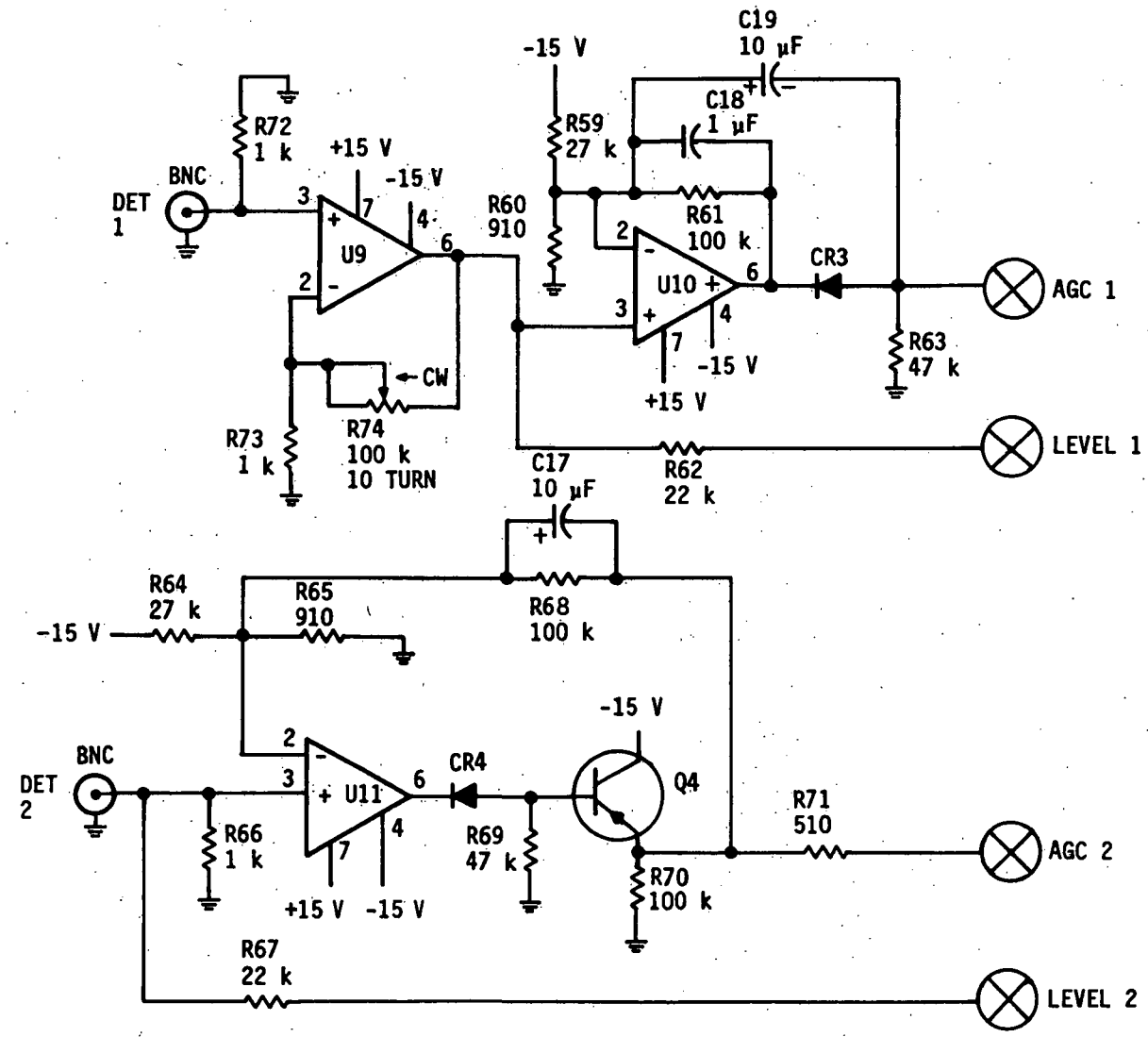
Figure 5-3. Filter Frequency Response



SOLDER TERMINAL FEEDTHROUGH

Q_1 2N2432A
Q_2 2N3495
Q_3 2N2484
U1 - U6 741 OP AMPS,
U7, U8 BURR BROWN 3400.
ALL RESISTORS 1/8 W.
1 µF AND 0.1 µF CAPACITORS ARE "ERIE RED CAPS", 50 W Vdc.
CR1, CR2 HP 2301.

Figure 5-4. Backend Control Circuit Diagram



U9 - U11 741 OP-AMP
Q4 2N3495
CR3, CR4 1N914

4-2301

Figure 5-5. Backend AGC Amplifier Circuit Diagram

U11 amplifies the AGC-2 detector output voltage when it is more negative than the threshold established by R64 and R65, at which time the absorptive modulator AGC-2 gain control element is controlled by the current amplifier Q4.

5.3.3 Backend MECL 1-0 Decision

These components are within the chassis marked MECL. The schematic is shown in Figure 5-6. The MECL device used is the MC 1692 line receiver that contains four differential input logic elements and a voltage reference which is at the logic transition voltage. The input pins used, 4 and 5, are connected to this reference so that the logic element will have a symmetrical response to the ac-coupled demodulated signal at pin 4. A 1 K resistor between the ac-coupled output from pin 2 and +15 volts raises the output voltage swing to about 0.7 ±0.4 volts for the two logic levels when the unit is dc-coupled to a 50 ohm load to ground.

5.3.4 AGC Buffer Amplifier

This chassis (schematic in Figure 5-7) has been added to provide replicas of the AGC signals to external subsystems where they may be used to provide optical pointing information. U-3 and Q-1 performance is identical to U-11 and Q-4 of the backend AGC amplifiers (paragraph 5.3.2). U-1 and U2 amplify the AGC-2 detector voltage and provide nominal voltage levels of ±2 volts balanced to ground.

5.3.5 Backend Control Panel

The backend circuits receive their power and control from the backend control panel assembly via a 20-foot cable. The control circuits are contained within the control chassis (schematic in Figure 5-8) with the required switches and controls on the panel.

A ten turn 10 K tuning potentiometer on the panel and R1 and R2 control the output voltage of U1 when the panel TUNE switch is in the MANUAL position. When the TUNE switch is in its EXT position, a front panel connector provides the input to U1 so that the VCO control voltage at its output may be externally programmed.

The in-lock indication signal from the backend is amplified by U2 and Q1 to provide current to light a front panel LED indicating tracking loop lock.

The sweep switch on the panel, when in its off position, provides a +5 volt level via R14 and R15 to the backend stop sweep line forcing the sweep to stop.

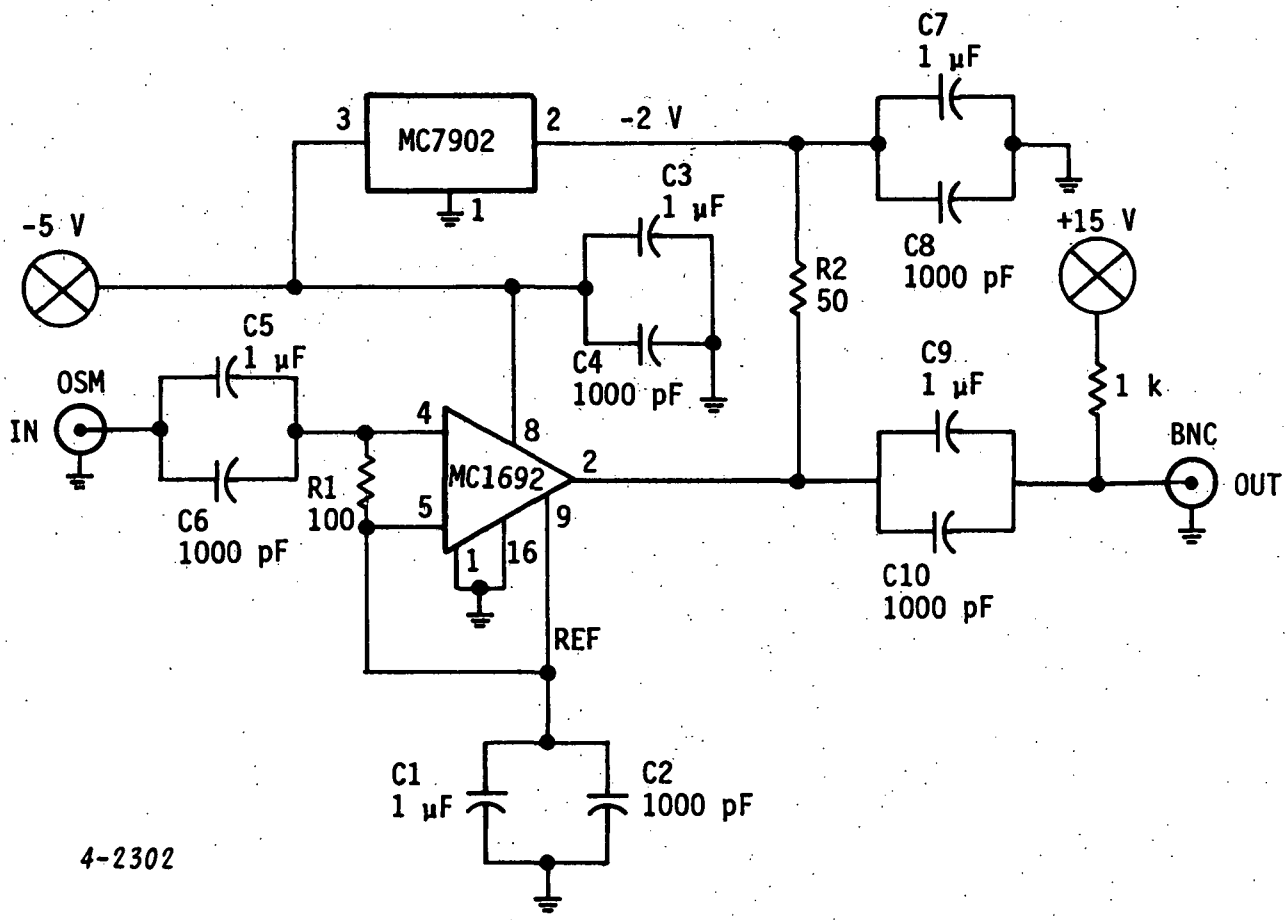


Figure 5-6. MECL 1-0 Decision Circuit Diagram

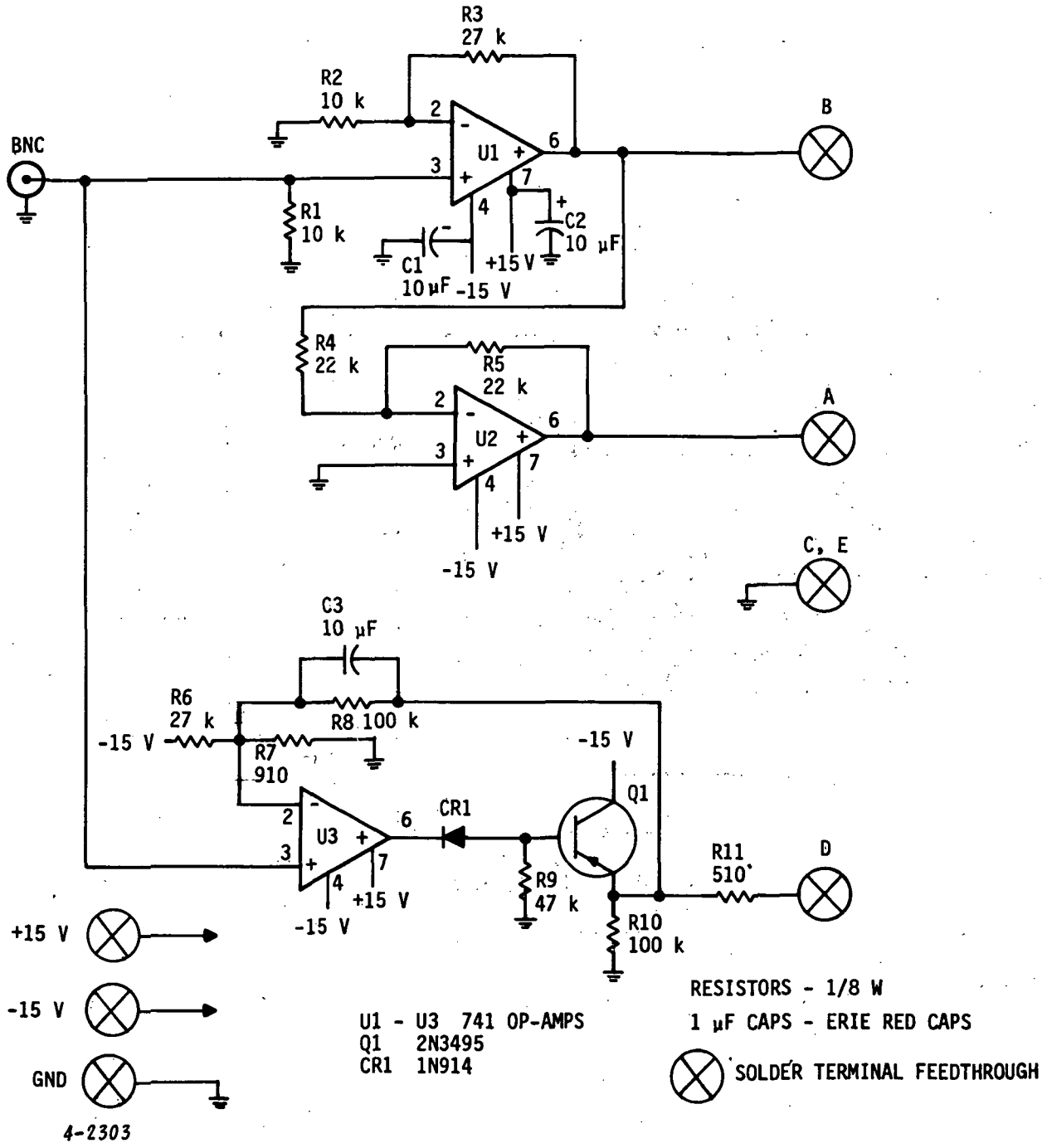


Figure 5-7. AGC Buffer Amplifiers Schematic

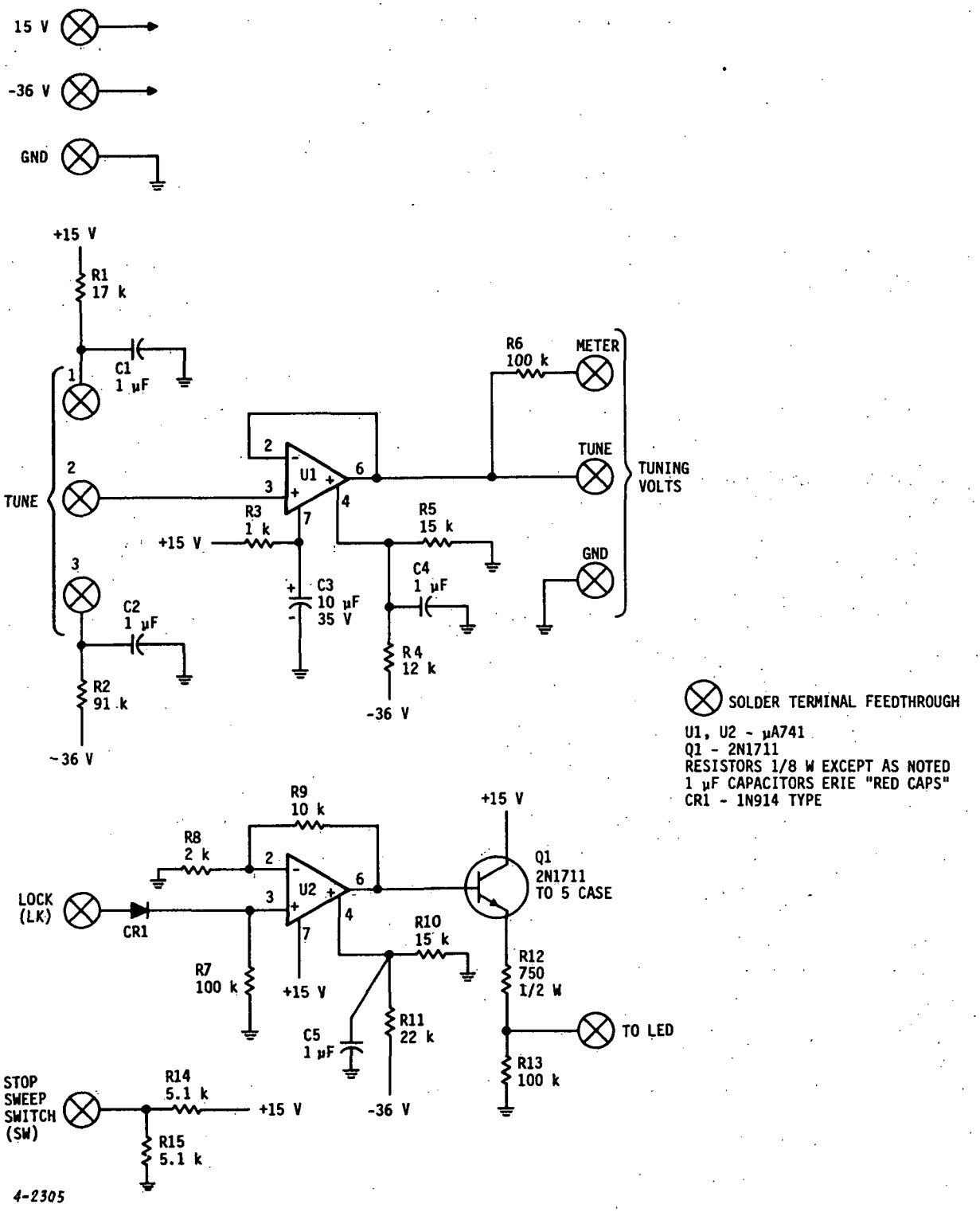


Figure 5-8. Backend Control Panel Circuit Diagram

5.4 MEASURED PERFORMANCE

Receiver backend performance data was obtained using a modulated signal source designed by AIL under NASA Contract NAS-5-23211. This signal source provides a PSK signal (greater than 20 dB carrier suppression) modulated at a 300 megabit rate whose carrier frequency can be varied between 200 and 900 MHz.

Bit error rate data was taken with Tau-Tron Inc. S-1000-A Digital Communications Test Transmitter and S1100A Digital Communications Test Receiver; both were provided as government furnished equipment.

5.4.1 AGC Transient Response

Figure 5-9 indicates the AGC-2 detector voltage response to a signal step 15 dB above noise. Figure 5-10 shows the same data in a manner indicating that the AGC-2 response time constant is very nearly 30 milliseconds. The data was taken with 50 dB of preamplifier gain external to the backend (Figure 5-1).

5.4.2 Tracking Loop

The measured frequency response of the tracking loop has been plotted on Figure 4-3. The loop's measured sensitivity to slow frequency variations is shown in Figure 5-11 (the response to rapid frequency changes was discussed in paragraph 4.5). Note that the phase variations shown in Figure 5-11 are at the loop phase detector and, due to the loop frequency doublers, are twice that occuring at the data demodulator.

5.4.3 Data Bit Error Rates

The bit errors measured at a data rate of 300 megabits/second are shown in Figure 5-12. Their deviations from theoretical PSK limits are detailed in Figure 5-13. The increasing error rates at the lower signal frequencies are attributable to higher levels of signal image and VCO leakage powers appearing at the output of the Bessel 1.5 GHz filter due to the filter's broad bandwidth (inherent in linear phase filters).

5.4.4 Data Waveforms

Photographs of receiver output data waveforms as displayed on a Tektronix Type 661 sampling oscilloscope are shown in Figures 5-14 and 5-15; all photos are taken of 300 megabit data. Figure 5-14 shows photos taken at an SNR of 8 dB. Those marked Linear were taken at the input to the MECL 1-0 decision elements, while the photos labeled MECL were taken

at the output of the 1-0 decision elements. The photographs in Figure 5-15 are similar except that their SNR was 20 dB.

The 200 and 500 MHz linear photos at 8 dB SNR in Figure 5-14 show similar levels of noise consistent with their similar error rate performance as extrapolated in Figure 5-13. The corresponding photos at 20 dB SNR in Figure 5-15 illustrate the presence of signal image and VCO leakage power at the lower signal frequencies as discussed in paragraph 5.4.3.

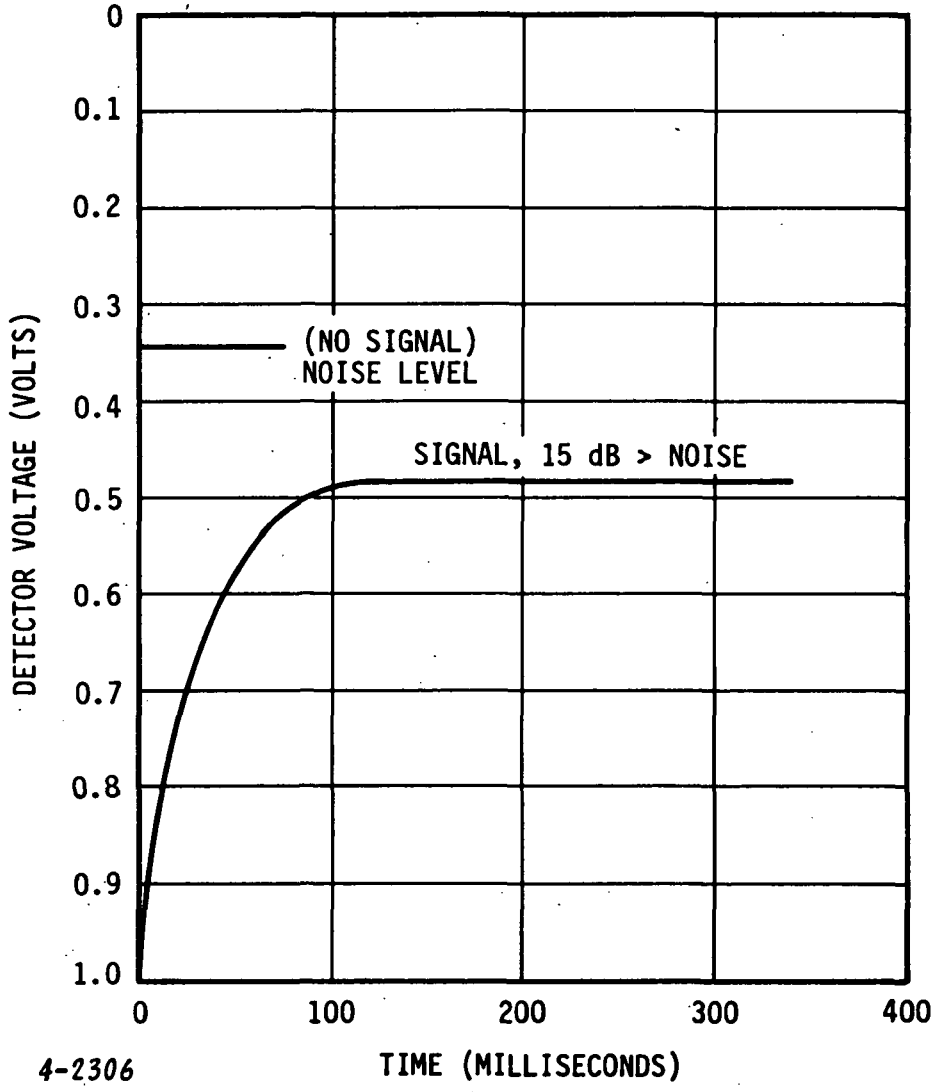


Figure 5-9. AGC-2 Detector Voltage

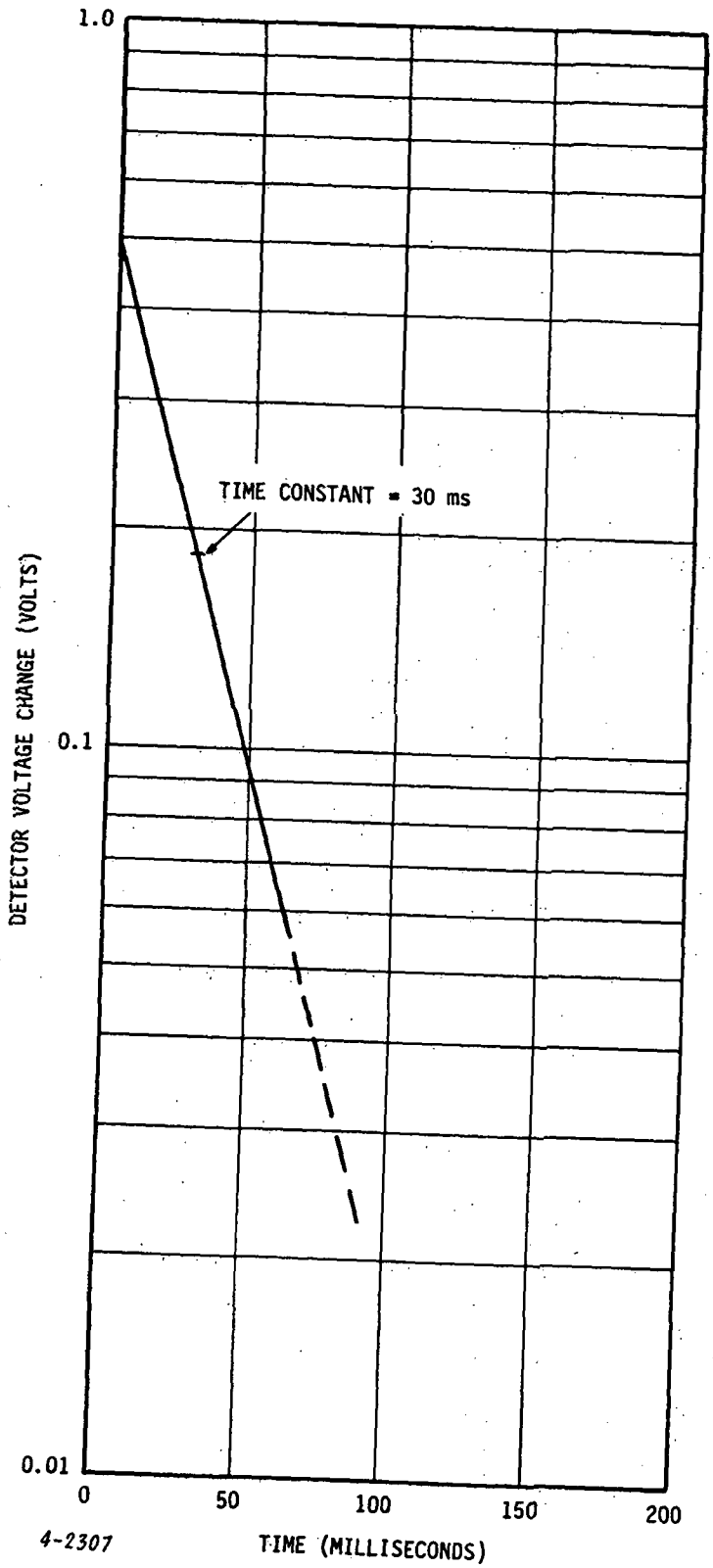


Figure 5-10. AGC-2 Detector Transient Response

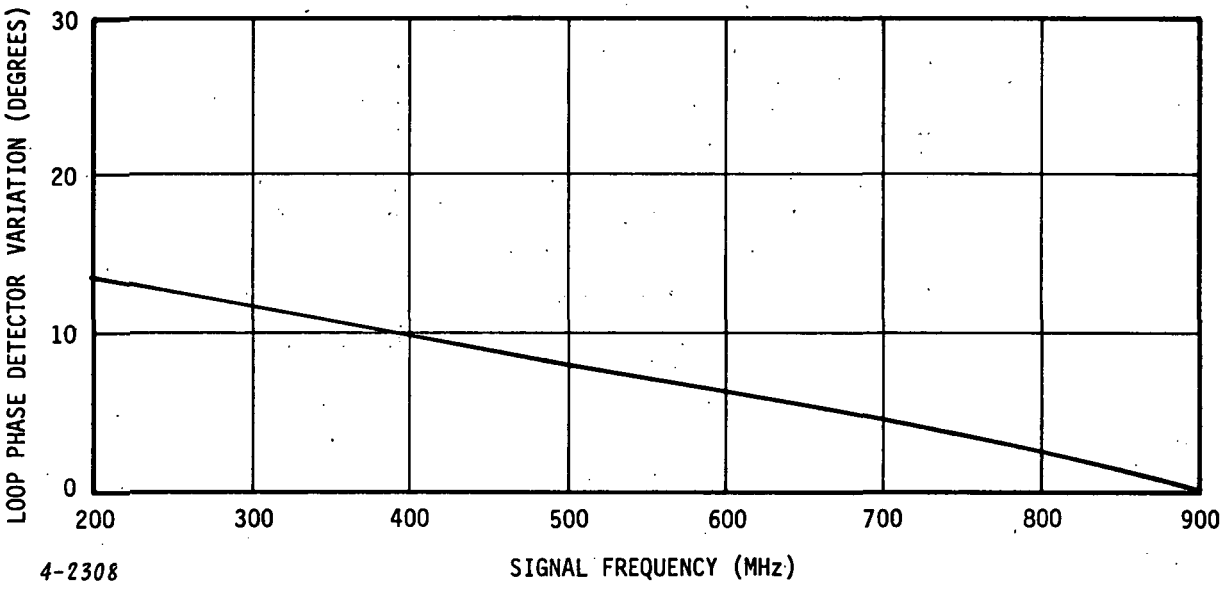


Figure 5-11. Measured Tracking Loop Sensitivity

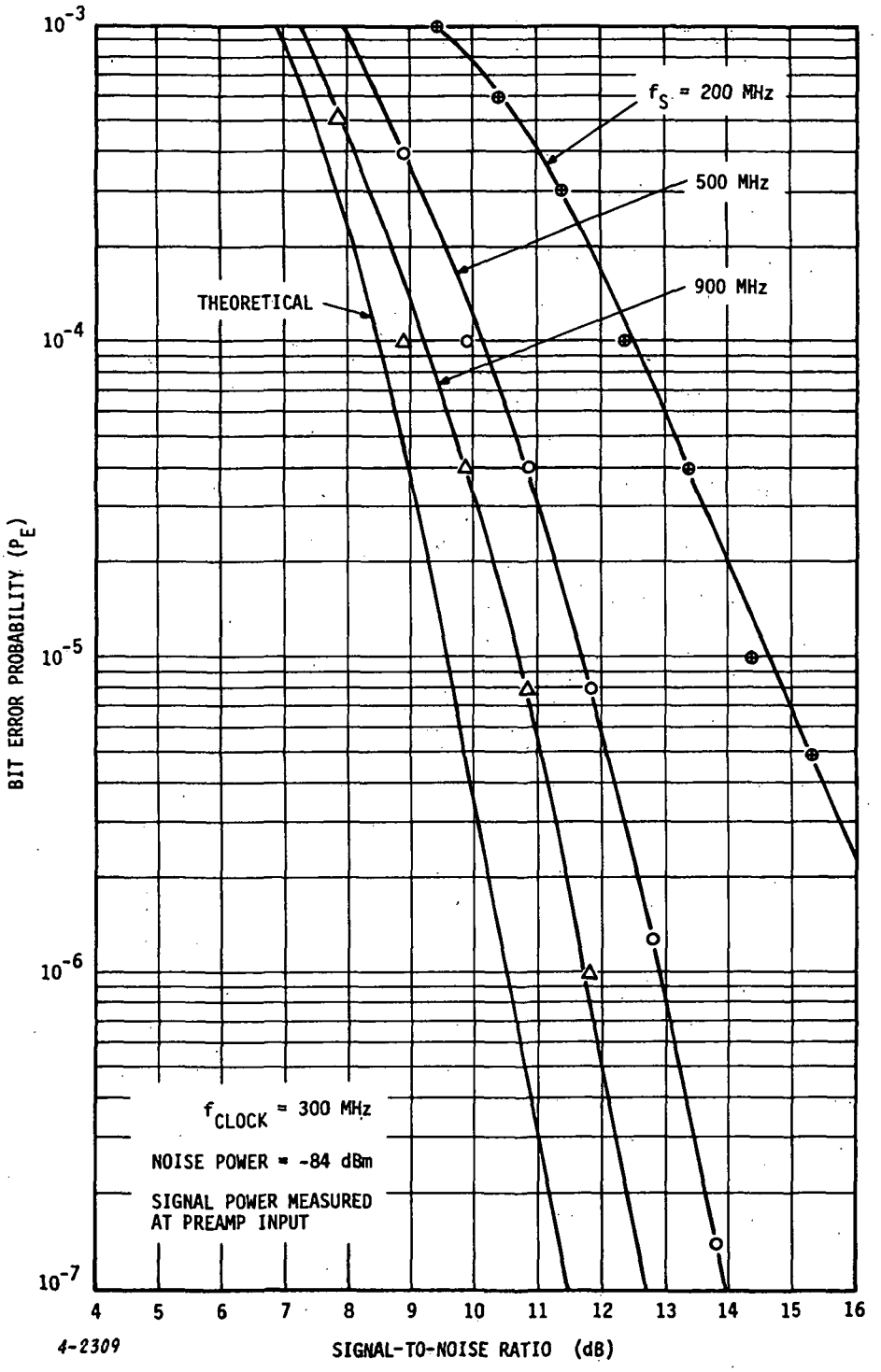


Figure 5-12. Measured Bit Error Probabilities

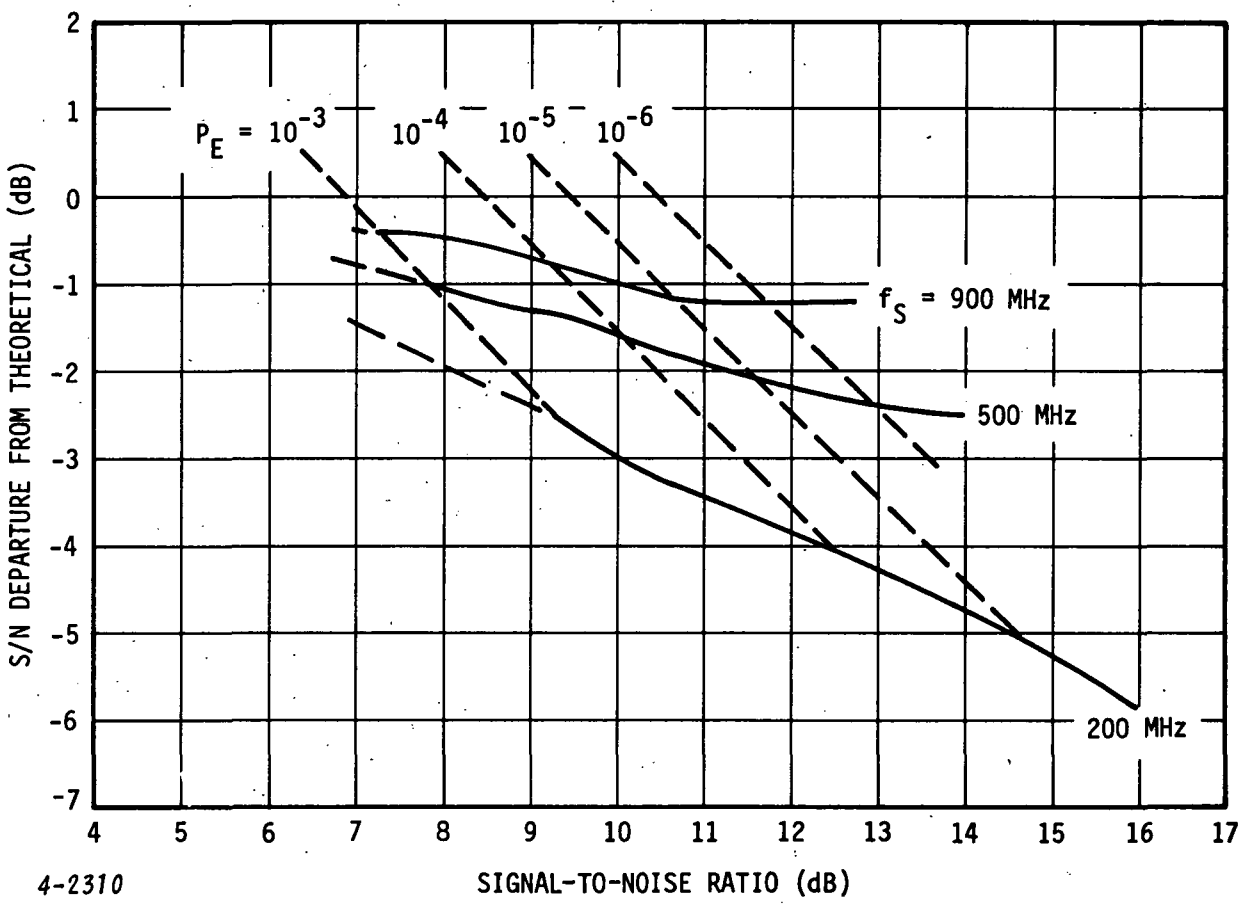
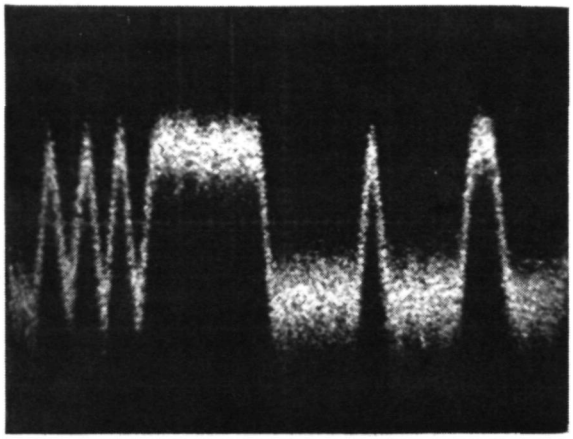


Figure 5-13. Bit Error Rate Departure From Theoretical

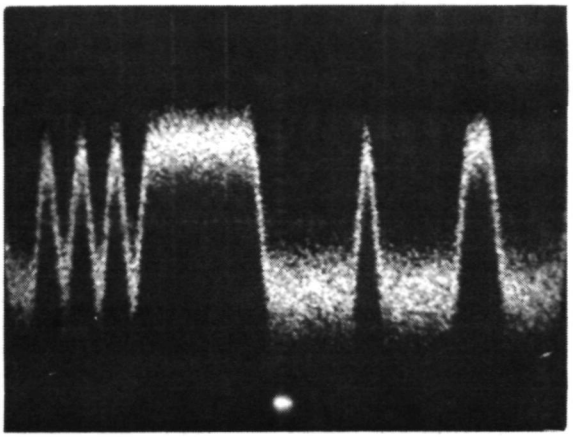
300 MBS DATA

SIGNAL FREQUENCY = 200 MHz

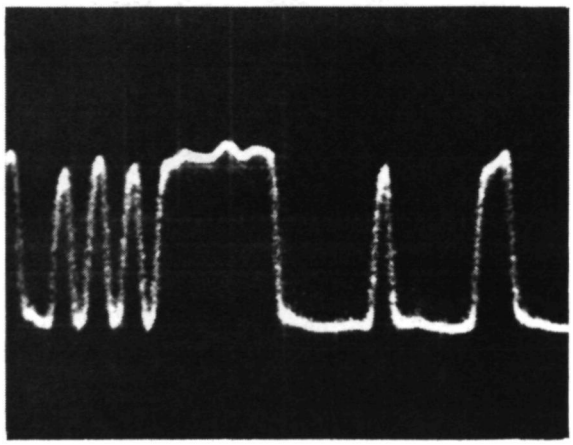


LINEAR

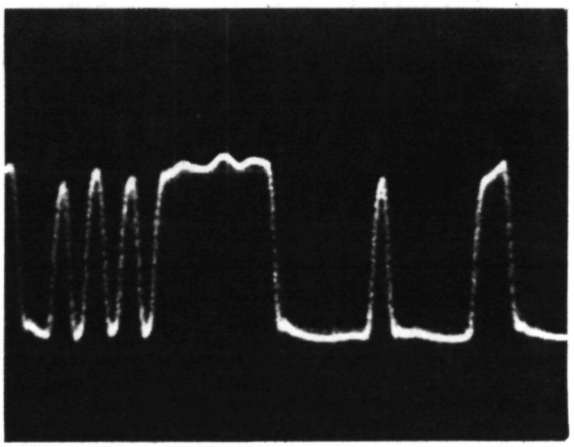
SIGNAL FREQUENCY = 500 MHz



LINEAR



MECL



MECL

4-2311

OSCILLOSCOPE SETTING:

VERTICAL = 200 mV/cm
HORIZONTAL = 10 ns/cm

Figure 5-14. Data Waveforms, SNR = 8 dB

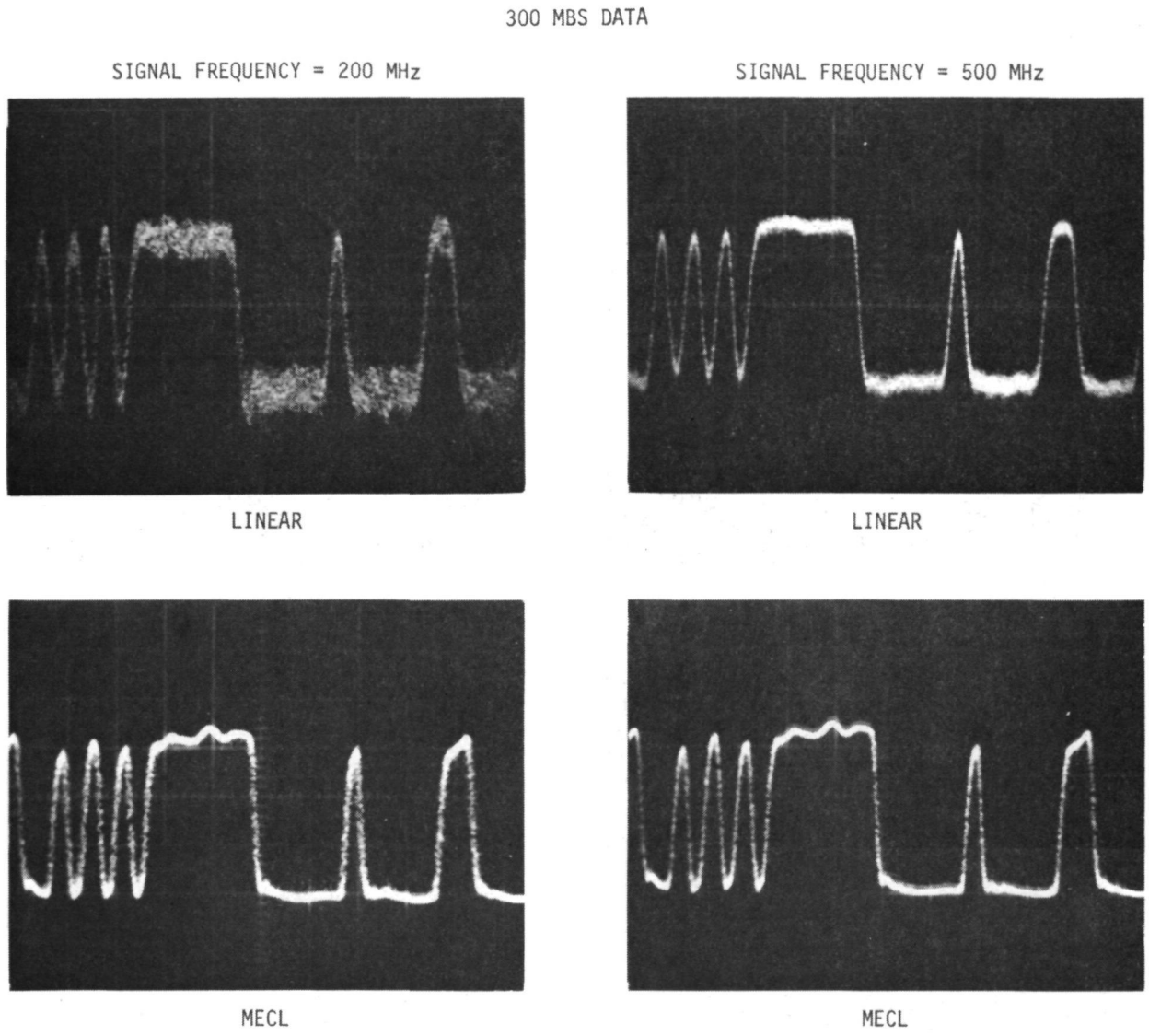


Figure 5-15. Data Waveforms, SNR = 20 dB

6.0 OPERATING INSTRUCTIONS

6.1 SIGNAL INPUTS AND OUTPUTS

6.1.1 Control Panel Assembly

The control panel assembly requires ac power to its line cord at 105 to 125 volts and 50 to 60 Hz. It provides regulated dc voltages and low frequency signal and monitor lines to the backend via a 26 pin connector mounted on its rear surface. The front panel BNC connector may be used to connect an external voltage to be used as the tuning control voltage for the backend VCO.

6.1.2 Backend Assembly

All input and output connectors are mounted on one surface of the backend enclosure.

The input connectors are a 26 pin PT065E-16-26S(SR) connector for power and control functions and a BNC female connector for the input RF signal (input).

There are two output BNC female connectors. One provides the demodulated data (Data) while the other provides a -8.5 dBm CW signal (Monitor) at the same frequency as the input carrier (200 to 900 MHz). A 10 pin connector is provided for the AGC buffer output voltages.

6.2 INTERCONNECTION

The 20 foot cable provided is the only interconnection between the control panel and the backend assemblies.

6.3 OPERATION AND CONTROLS

Operation of the receiver backend requires powering the control panel assembly, connecting the 20 foot cable, and providing a signal to the backend signal input BNC connector.

The backend tuning control (either manual or external) should then tune the VCO to a frequency in the vicinity of 1500 MHz above the signal's carrier frequency. Signal acquisition should then occur if the sweep switch is ON or, if it is OFF, when the tuning control tunes the VCO to within the tracking loop's acquisition range. Acquisition is indicated by illumination of the Lock light on the control panel. After acquisition, the signal carrier frequency is available for measurement at the backend Monitor BNC connector.

A digital panel meter on the control panel may monitor, as selected by a six position switch, any one of 5 signals; or it may be connected to test terminals for use as a digital voltmeter for testing purposes.

The five monitored signals are:

- Tune--The tuning voltage provided to the backend
- Frequency--The voltage at the VCO tuning port
- L-1--The AGC-1 detector voltage
- L-2--The AGC-2 detector voltage
- PD-L--The quadrature phase detector output voltage

6.4 BACKEND ADJUSTMENTS

The only backend adjustments anticipated are those of two coaxial line stretchers and one trimpot.

The two line stretcher adjustments are independent of each other. The unit to the input of the quadrature phase detector is to be adjusted to maximize the magnitude of the dc quadrature phase detector output (when the tracking loop is locked) which may be monitored at the PD-L meter switch position. Trimpot R2 in the backend chassis establishes the stop sweep acquisition threshold so that the sweep will stop when the proper loop-lock is present, but will not stop on any lower level and lock to some spurious signal.

The second line stretcher to the data demodulator LO input is used to maximize the data output level from the demodulator when the tracking loop is in proper lock.

6.5 CALIBRATIONS

6.5.1 Signal Frequency

The frequency to which the receiver backend is tuned is indicated by the panel meter when it is in the "Frequency" position. Figure 6-1 provides this calibration.

6.5.2 Amplifier Output Power Levels

The panel meter calibrations for the (A-2) and (A-3) 1.5 GHz amplifier power output levels are contained in Figure 6-2. They correspond to the panel meter positions L-1 and L-2 respectively.

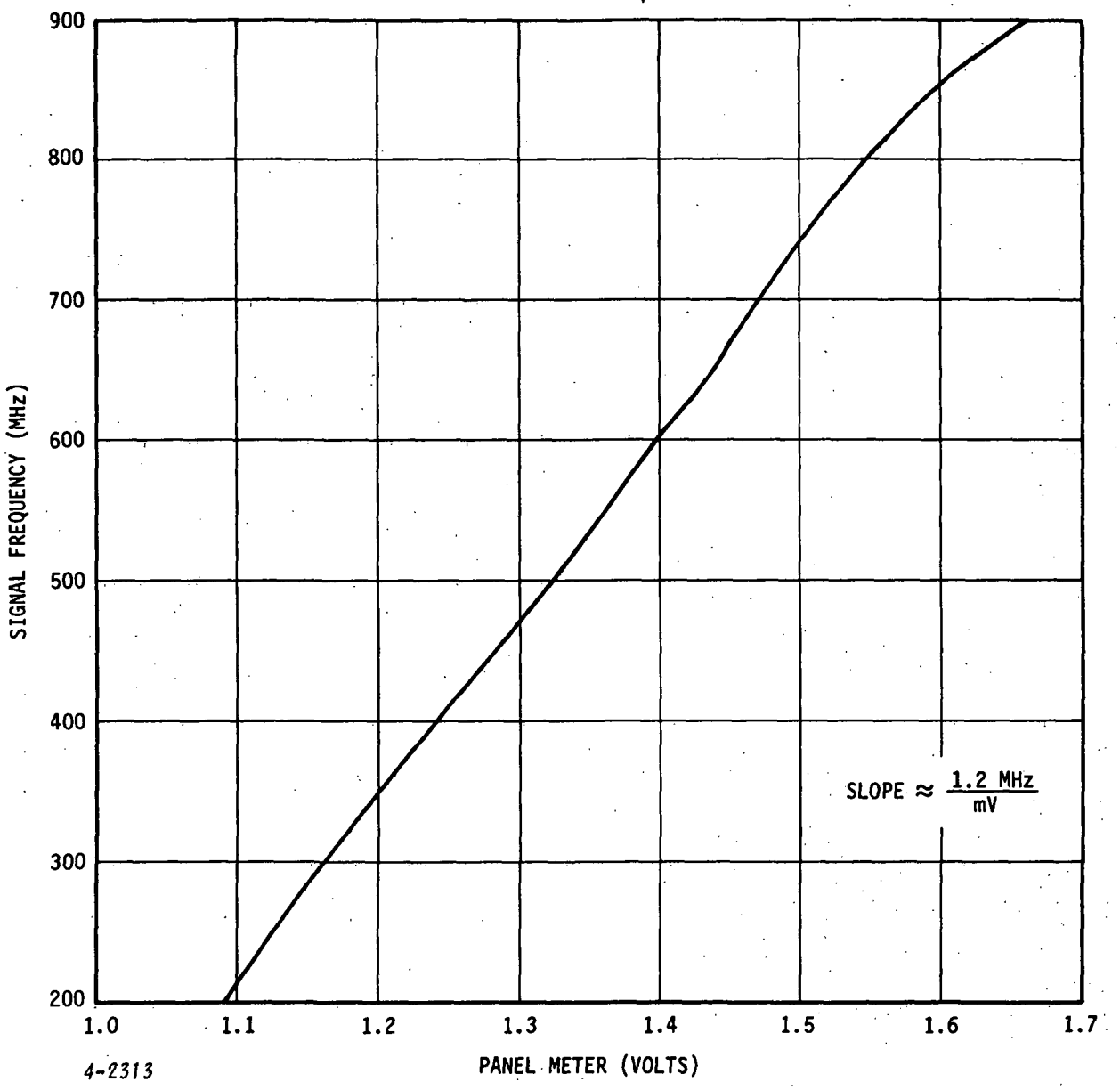


Figure 6-1. Panel Meter Calibration, Signal Frequency

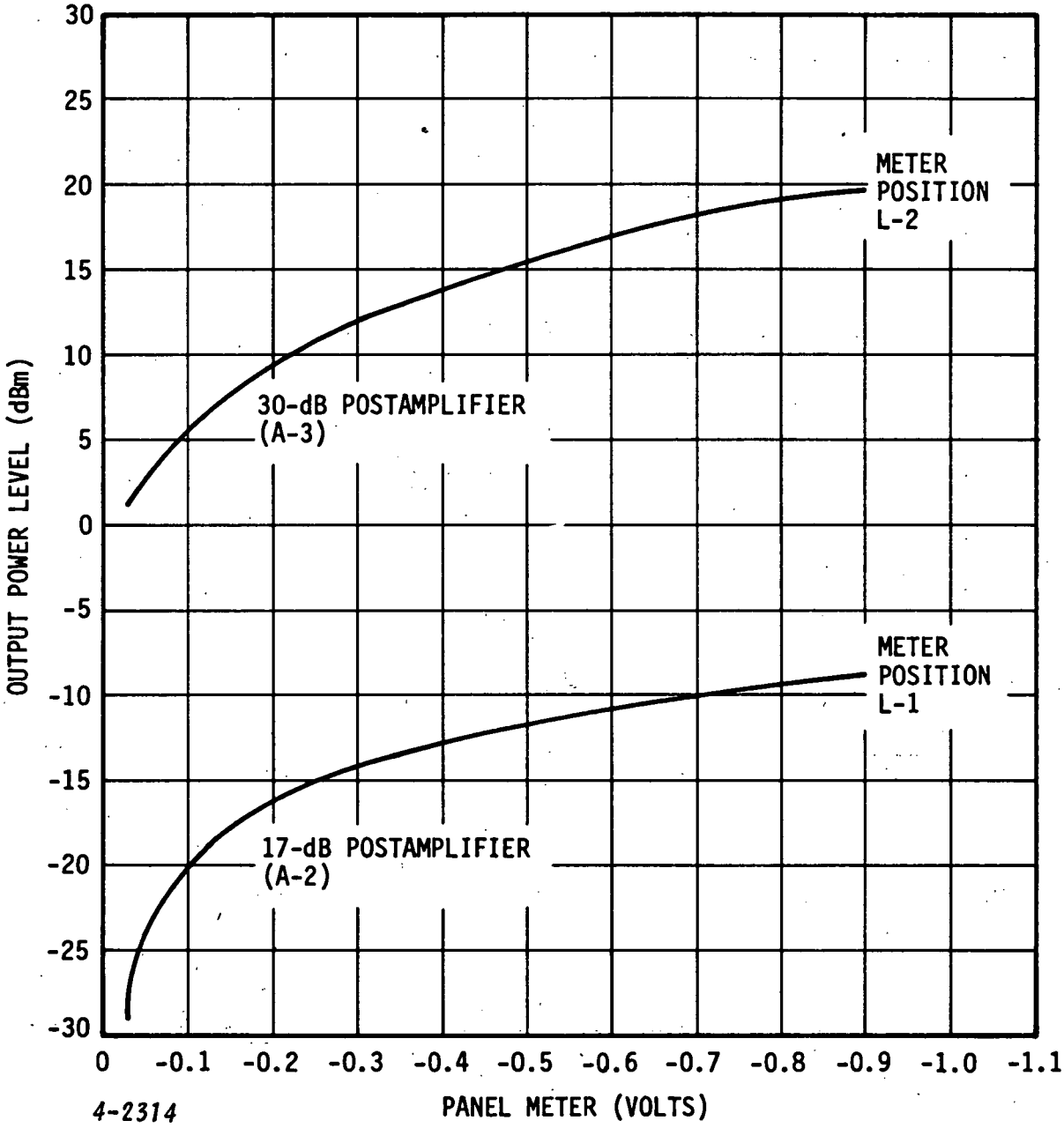


Figure 6-2. Panel Meter Calibration,, Amplifier Power Outputs

6.5.3 Relative Input Signal Power Levels

The panel meter indications for relative input signal powers at 500 MHz are shown on Figure 6-3. They reflect the range over which AGC is maintained and the "noise only" levels when 50 dB of preamp gain is included external to the receiver backend.

6.5.4 Panel Meter as DVM

The front panel jacks marked DVM connect to the panel meter to permit it to function as a digital voltmeter when the meter select switch is in its DVM position. The voltage scale factor when in this position has been adjusted to be 20 to 1.

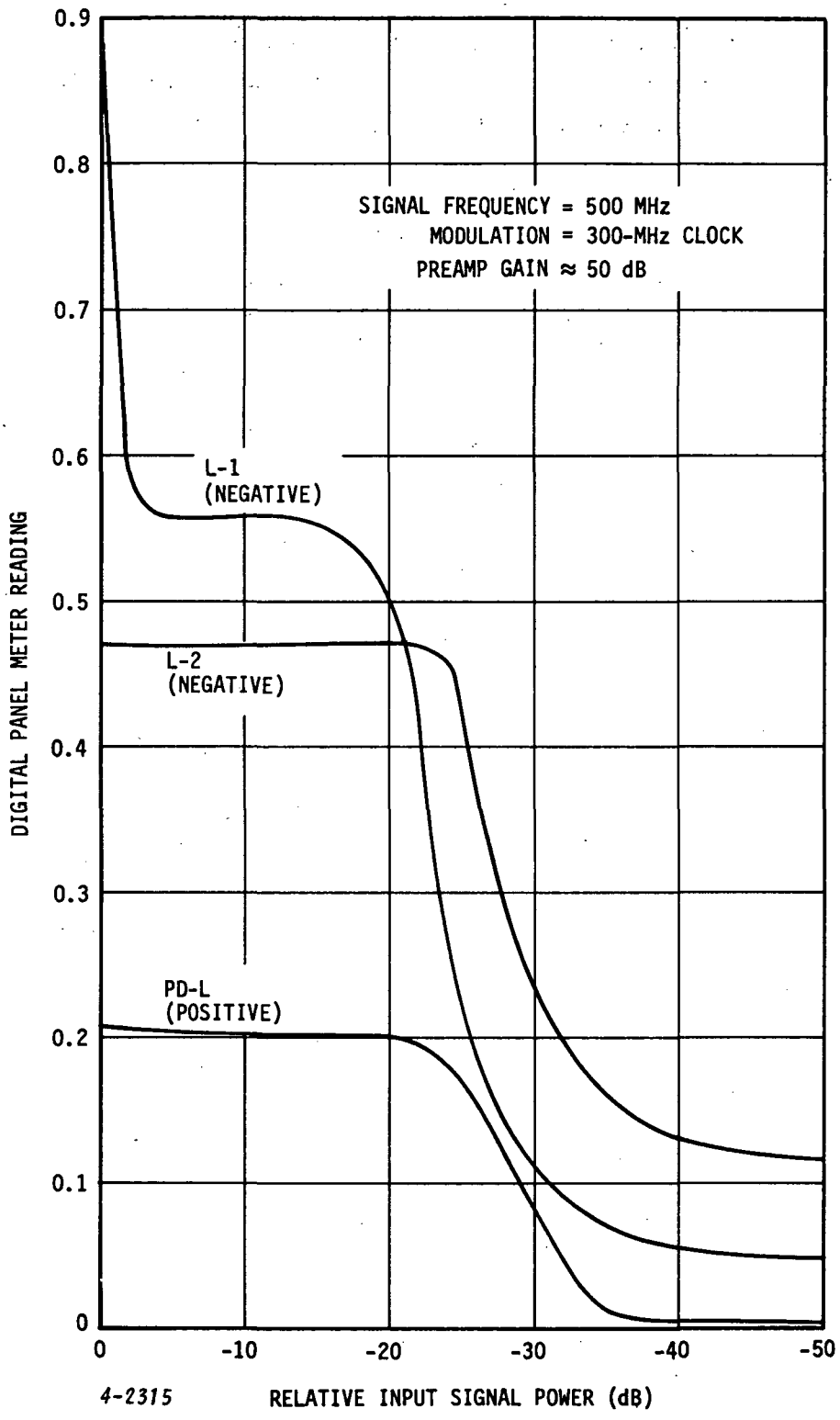


Figure 6-3. Panel Meter Calibration, Relative Signal Input Power

7.0 MECHANICAL CONFIGURATION

7.1 ASSEMBLY LAYOUT PHOTOGRAPHS

Various photographs of the receiver backend and its control panel are shown in Figures 7-1 through 7-6.

7.2 CIRCUIT BOARDS

The circuit board assembly containing the backend control and AGC amplifier components is outlined on Figure 7-7.

The Buffer Amplifier circuit board is contained on Figure 7-8 and the control panel circuit board assembly is shown on Figure 7-9.

7.3 WIRING DIAGRAMS

Wiring diagrams for the backend and its control panel are shown in Figures 7-10 and 7-11, respectively.

The control panel meter select switch wiring is in Figure 7-12 and the control cable diagram is in Figure 7-13.

Figure 7-1. Receiver Control Panel

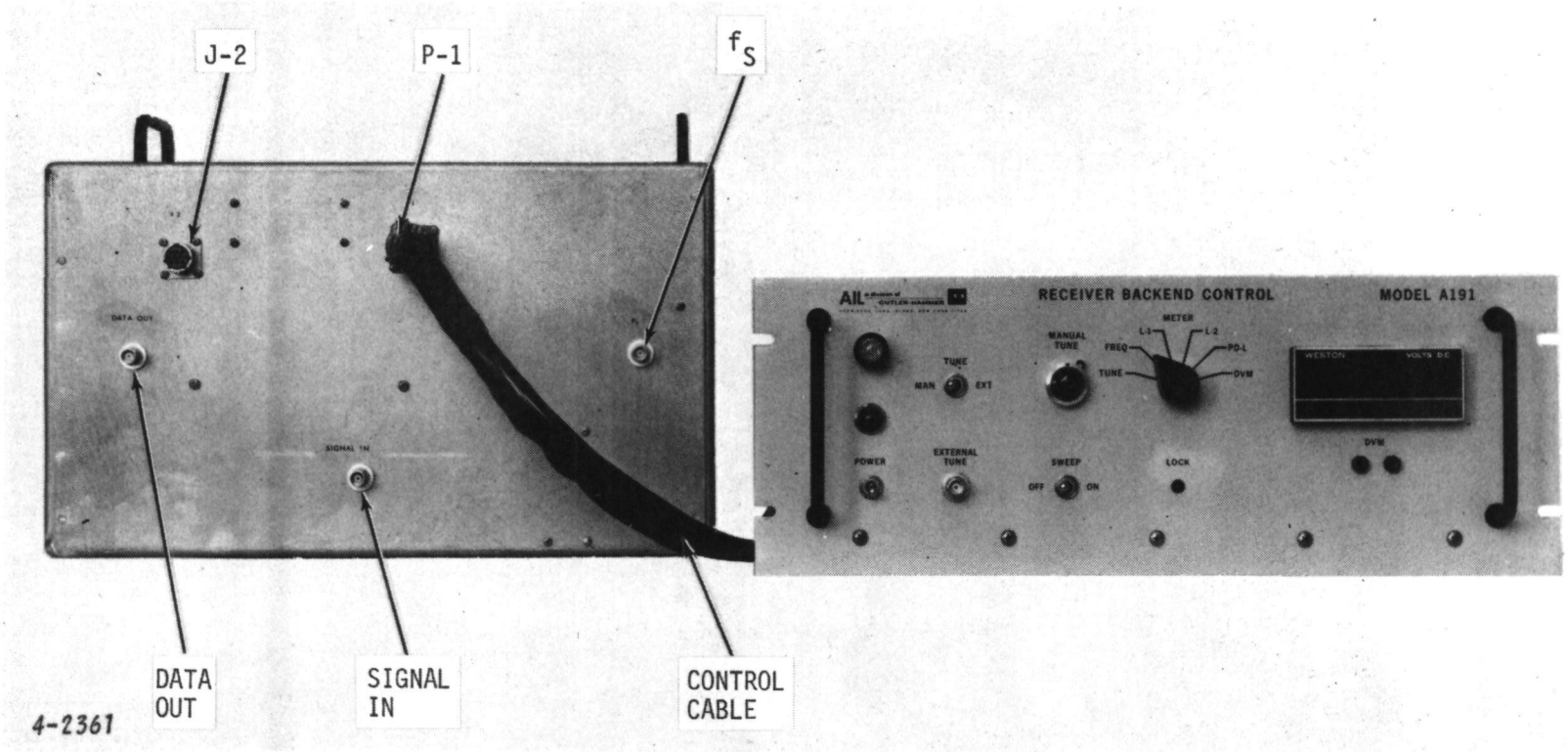


Figure 7-2. Control Panel and Backend

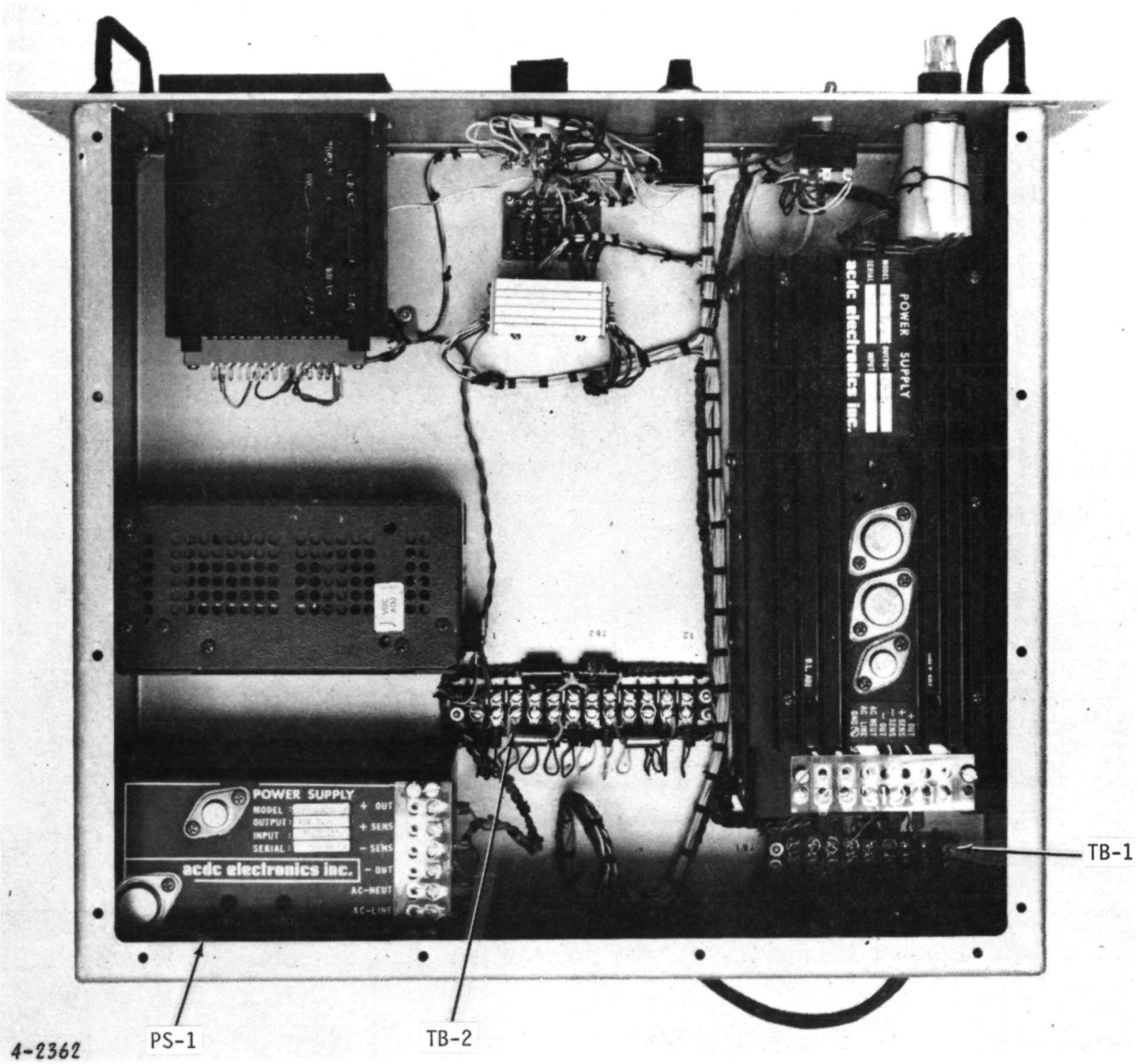


Figure 7-3. Control Panel Top View

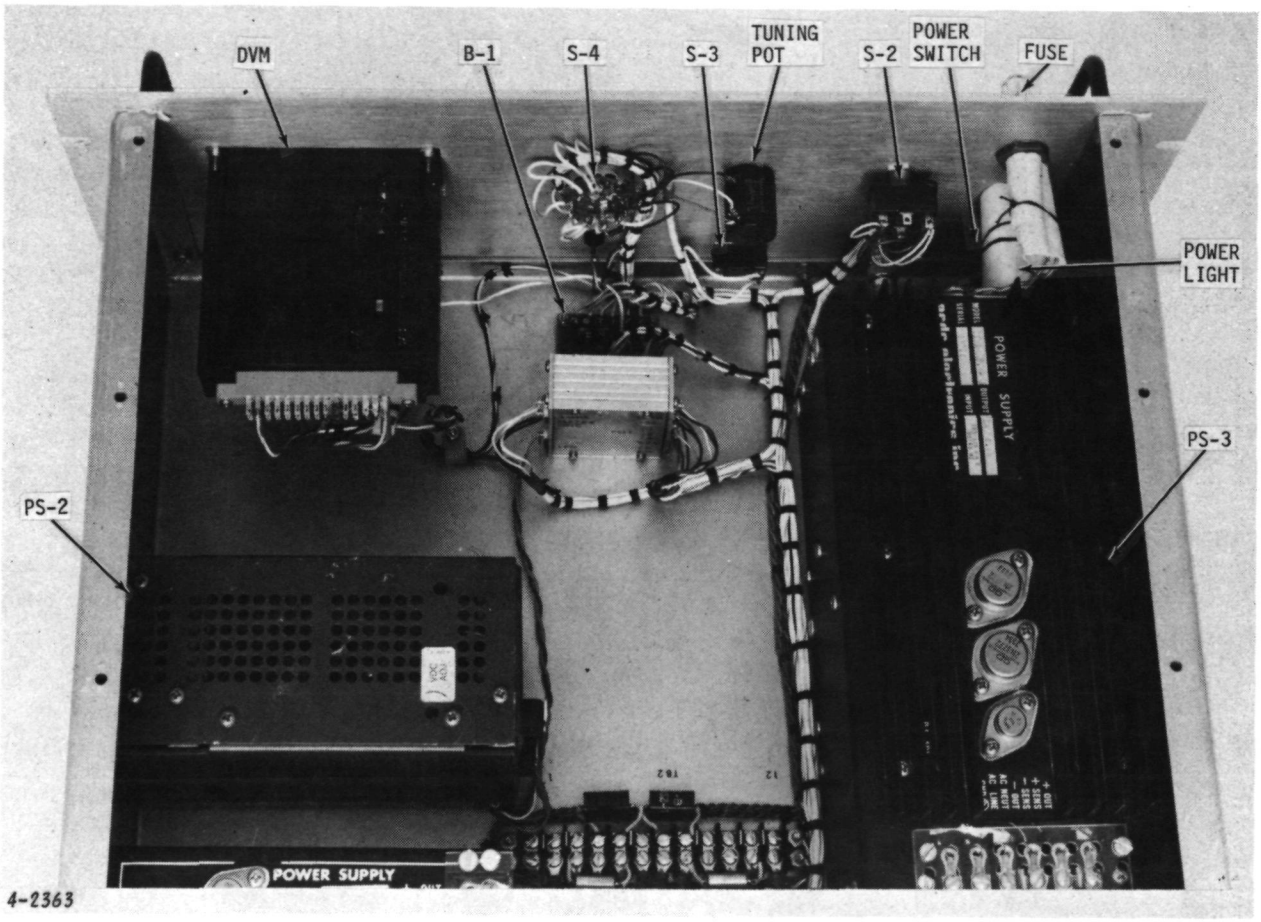


Figure 7-4. Control Panel Forward View

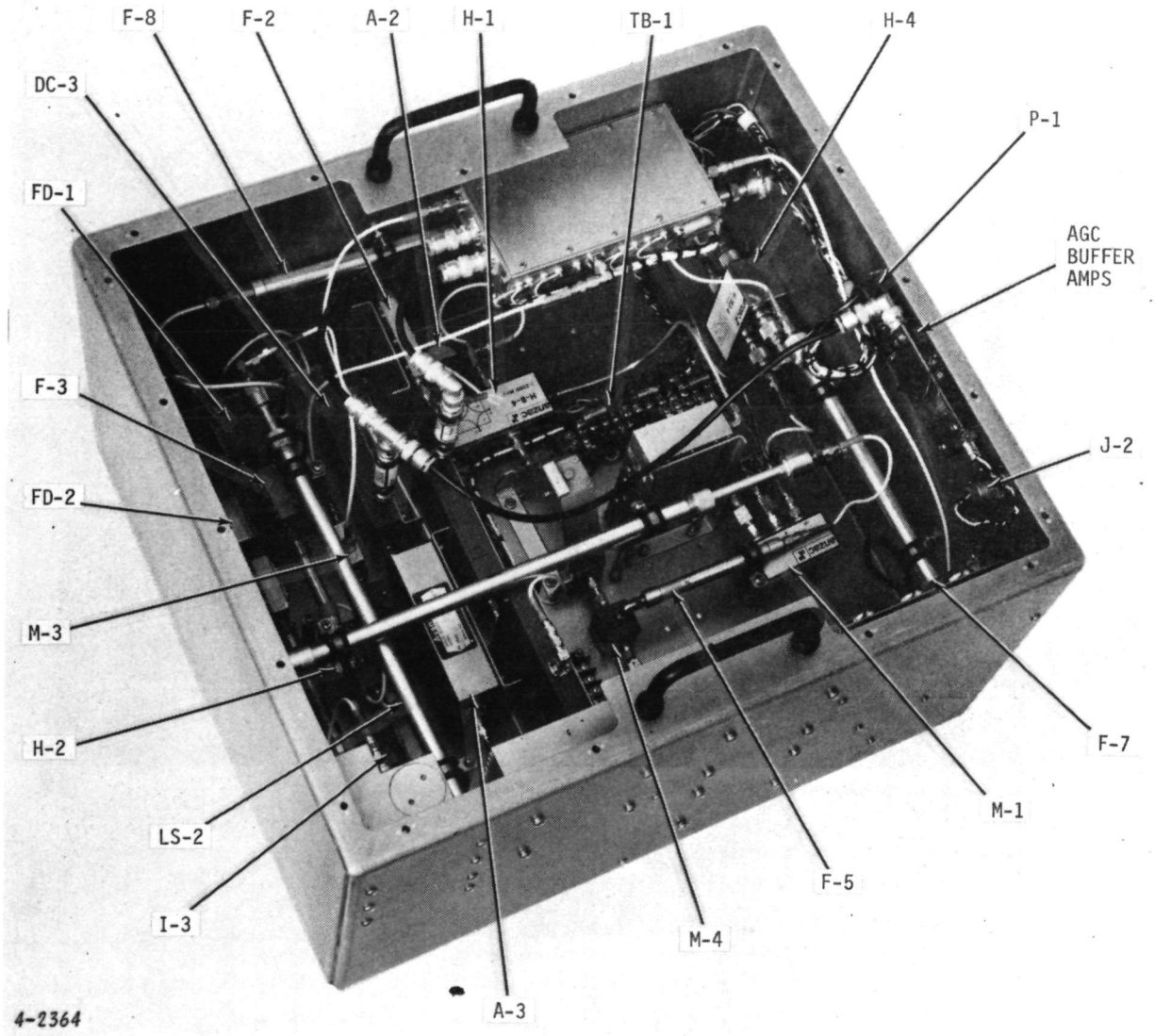


Figure 7-5. Backend View I

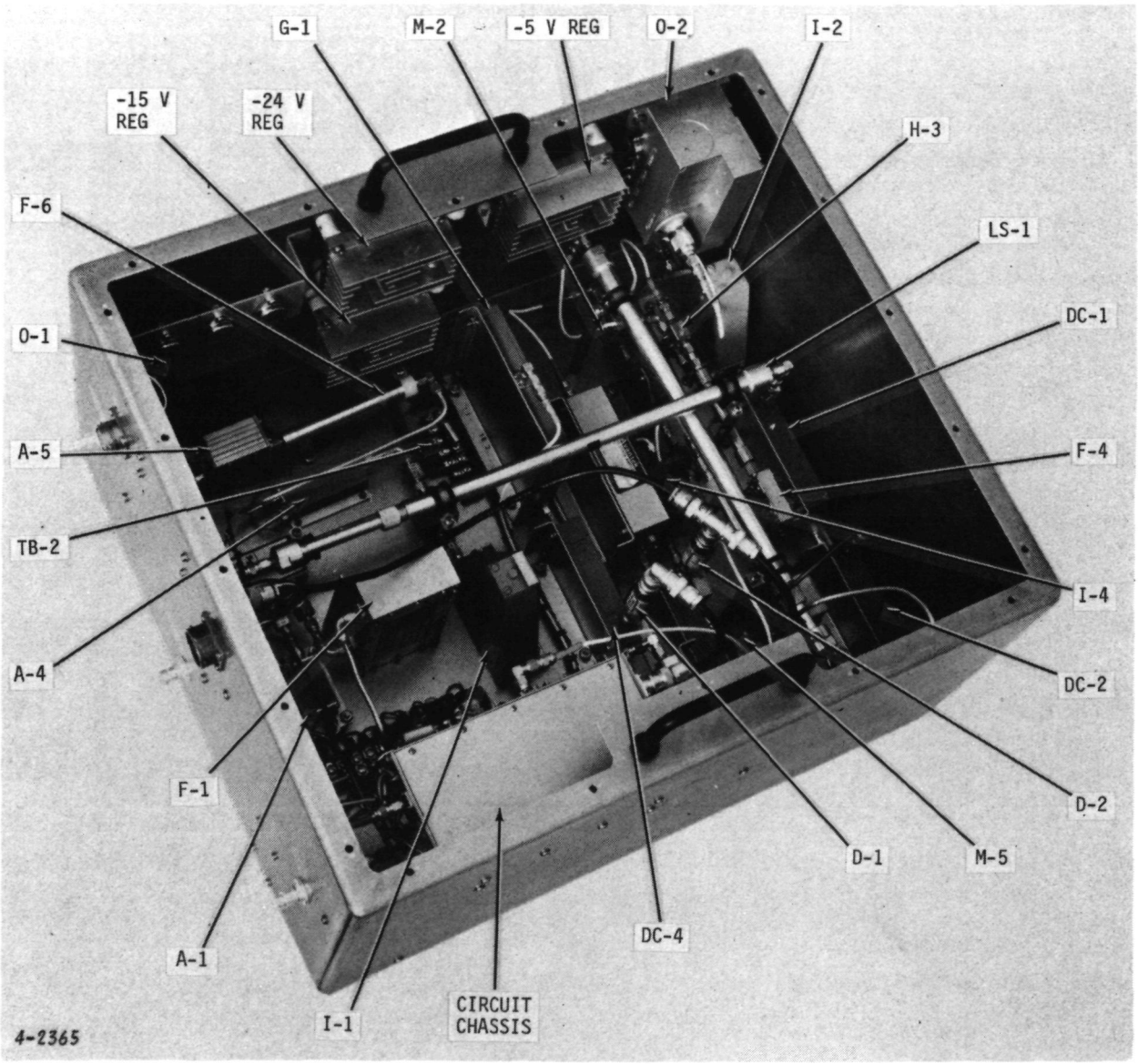


Figure 7-6. Backend View II

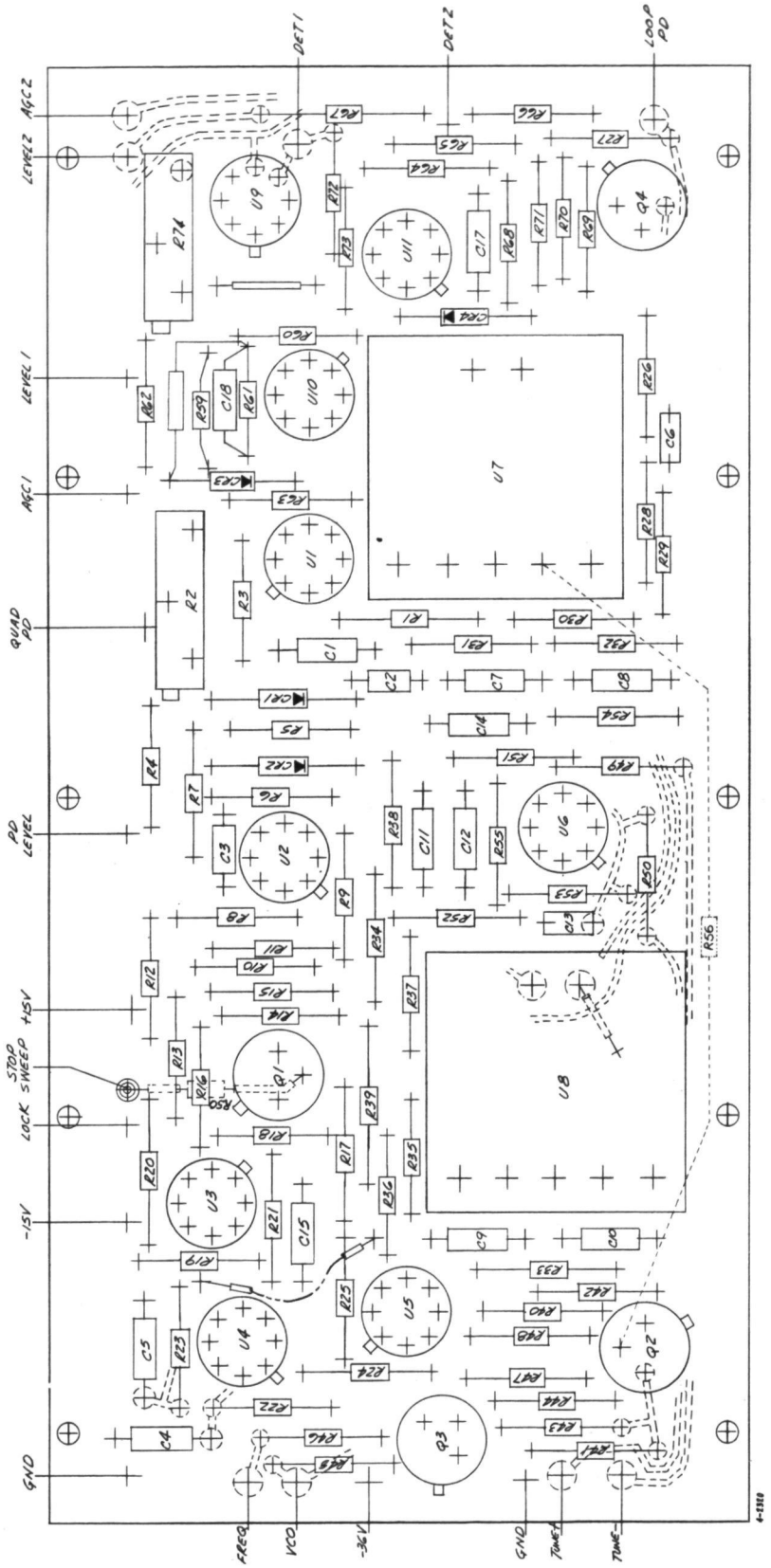


Figure 7-7. Backend Control and AGC Amplifier Circuit Board Assembly

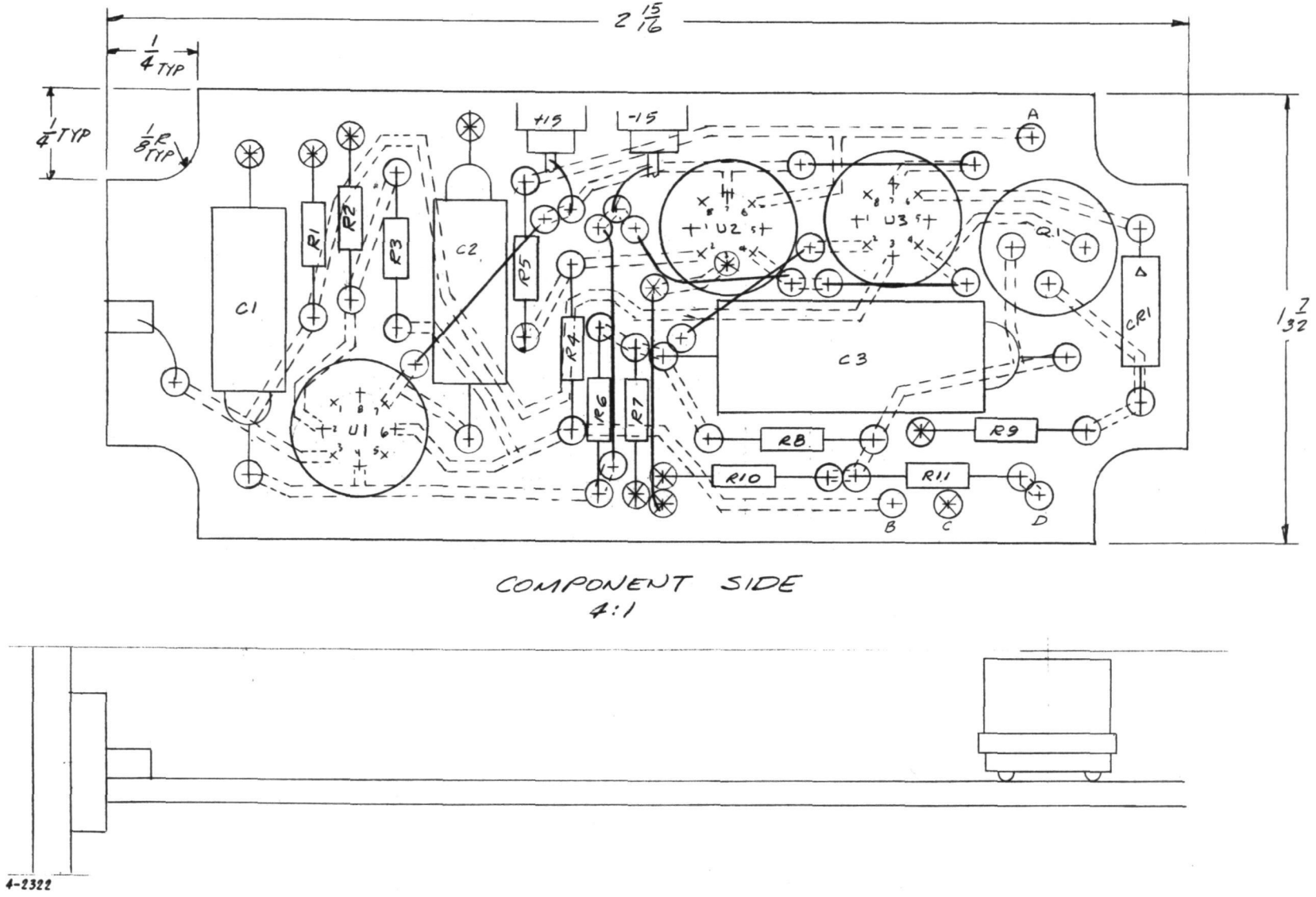


Figure 7-8. Buffer Amplifier Circuit Board Assembly

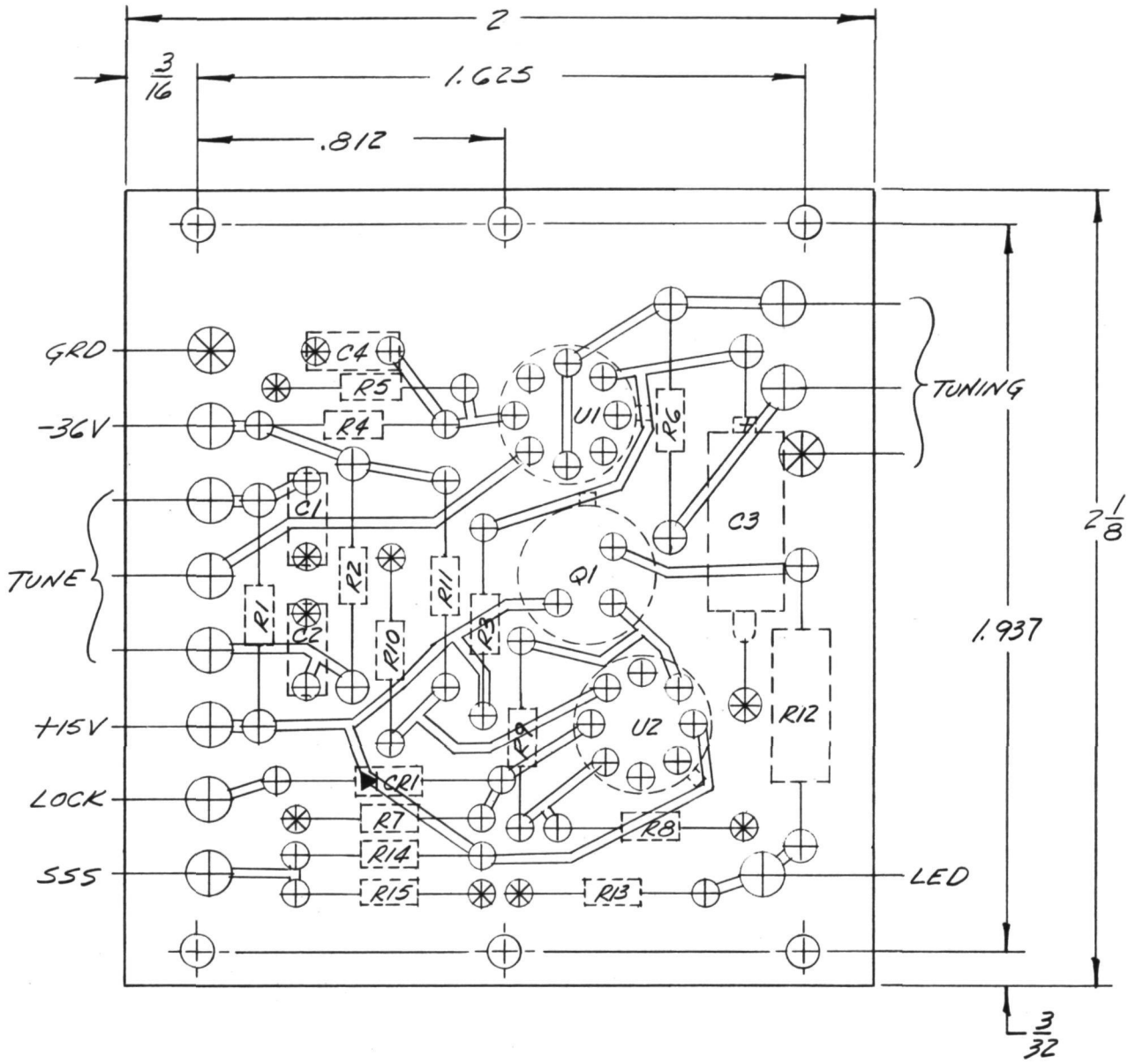


Figure 7-9. Control Panel Circuit Board Assembly

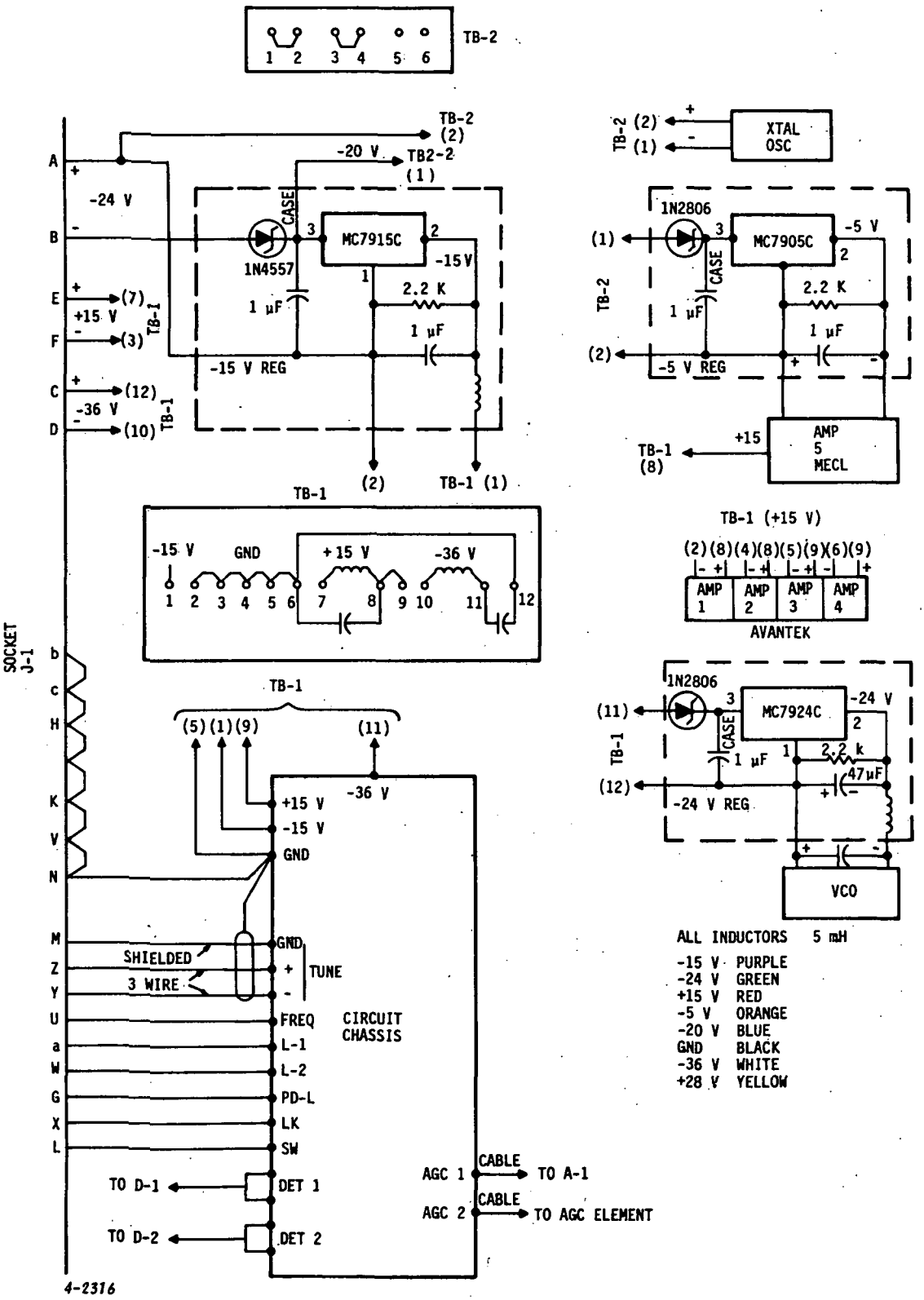


Figure 7-10. Backend Wiring Diagram

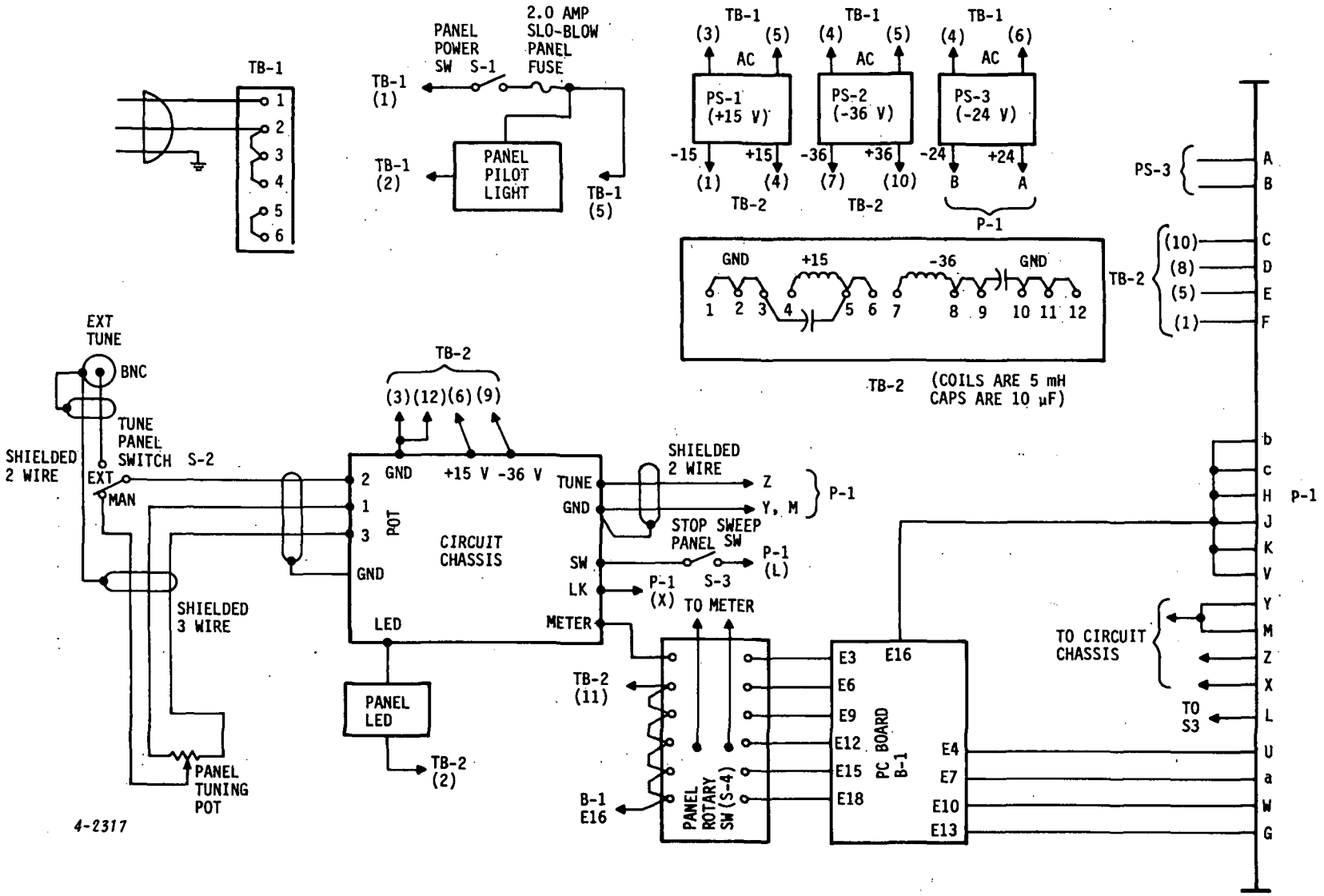


Figure 7-11. Control Panel Wiring Diagram

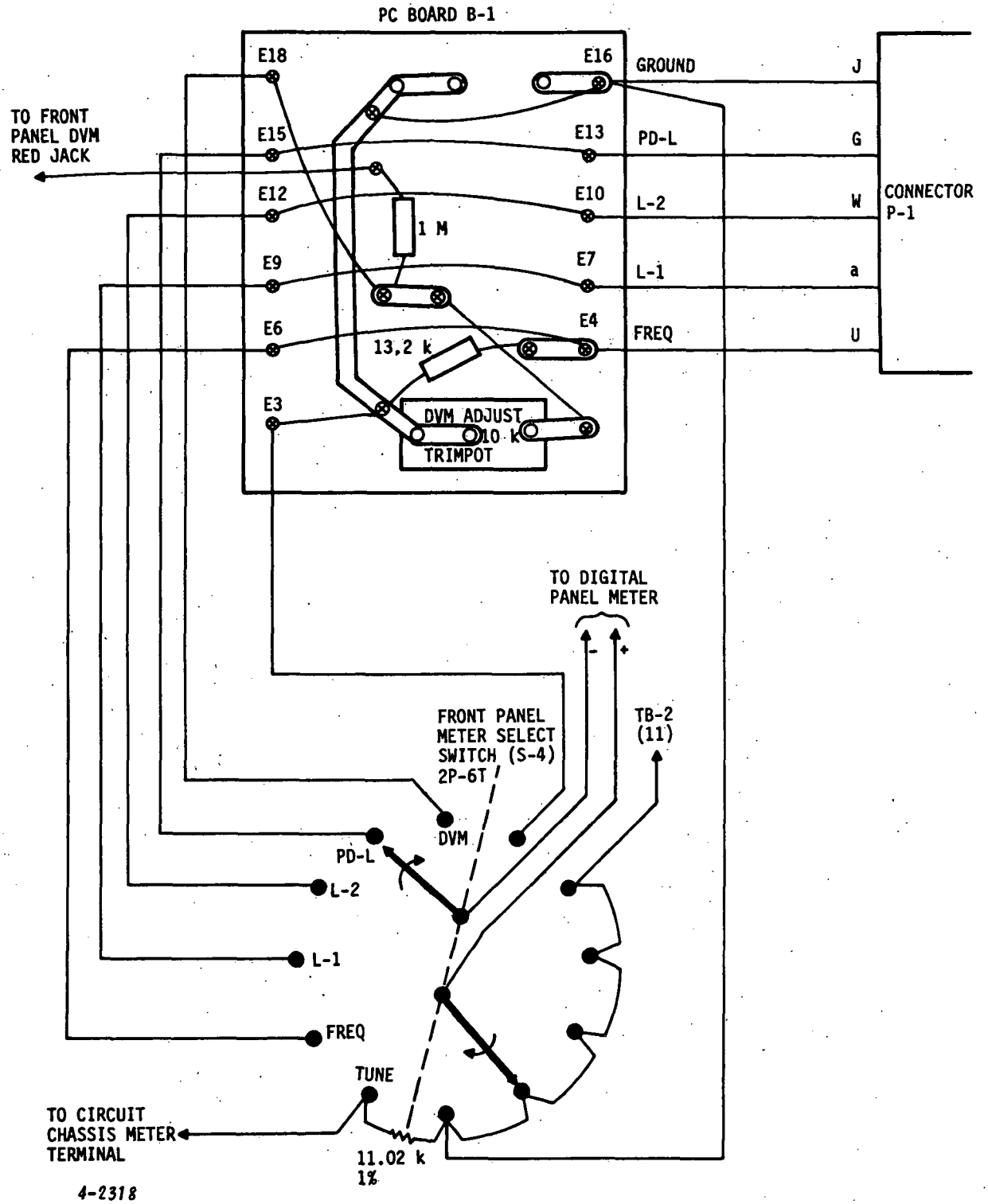


Figure 7-12. Control Panel Meter Select Switch Wiring

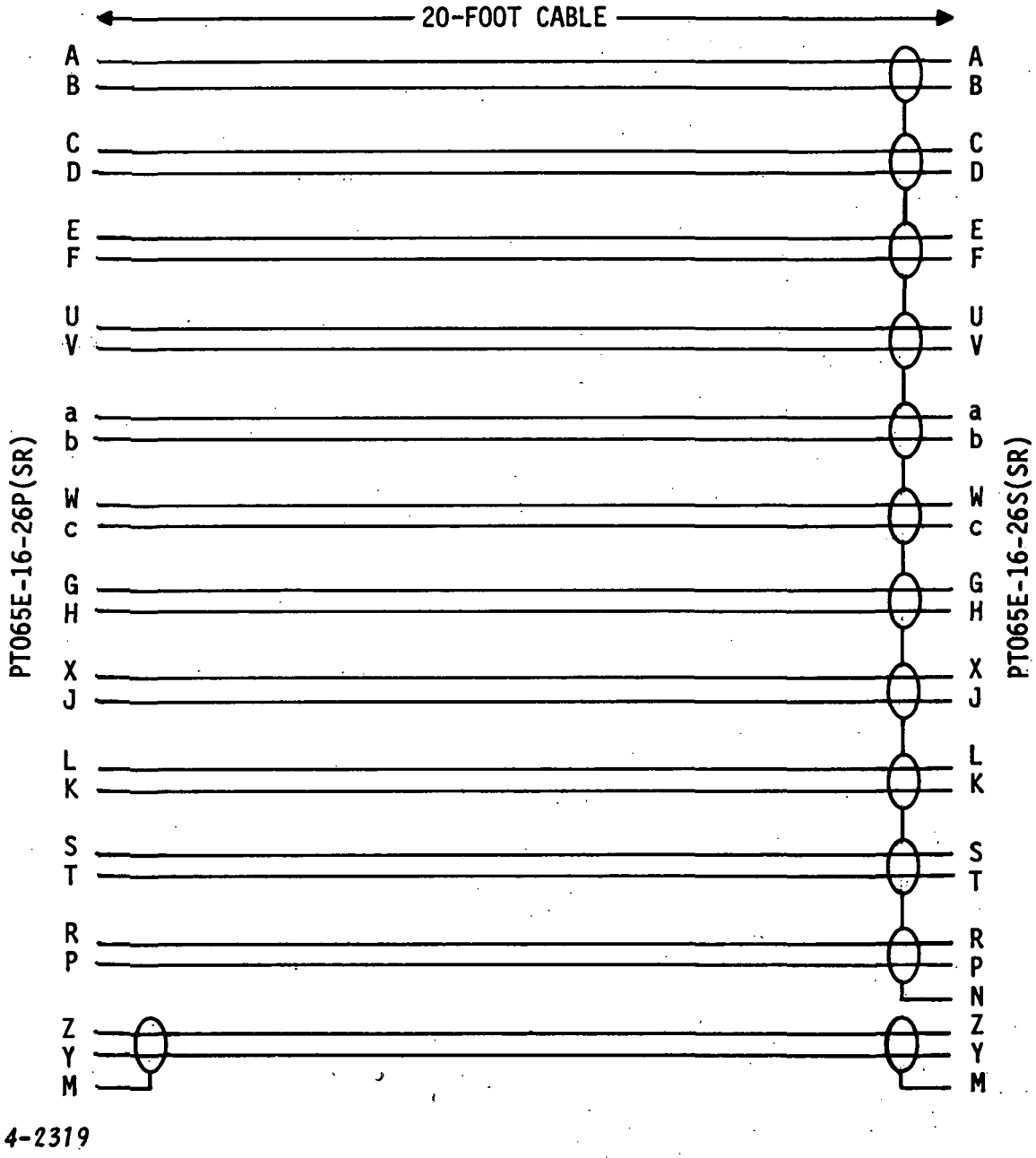


Figure 7-13. Control Cable

8.0 MAINTENANCE

No special maintenance procedures are required.

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