R-798

VOLUME II

MULTIPLE IMU SYSTEM HARDWARE INTERFACE DESIGN

by

Martin Landey
David Brown

December 1974

2c

The Charles Stark Draper Laboratory, Inc.
68 Albany Street, Cambridge, Massachusetts 02139

To NASA
George C. Marshall Space Flight Center
Huntsville, Alabama 35812

ATTN: ~~A&TS MS IP~~ AS61

4200

The Charles Stark Draper Laboratory, Inc.
Cambridge, Massachusetts 02139

R-798

VOLUME II

MULTIPLE IMU SYSTEM HARDWARE INTERFACE DESIGN

by
Martin Landey
David Brown

THE CHARLES STARK DRAPER LABORATORY
CAMBRIDGE, MASSACHUSETTS
02139

Approved: N. E. Sears Date: 12-19-74

ACKNOWLEDGMENT

This report documents the hardware interface design for the redundant IMU laboratory test system. This system was designed, built and delivered under Contract NAS8-27624 with the NASA/George C. Marshall Space Flight Center.

The authors wish to acknowledge significant contributions to this work by several individuals.

Durean Sprague designed the data bus driver and receiver, and provided valuable counsel in other areas. Richard Blaha aided in verification of the hardware. These designs were assembled by members of the CSDL NASA/ARMY Department Inertial Components Division under the direction of Dale Woodbury. Albert DeVito and Albert Moore were largely responsible for mechanical assembly.

The authors further acknowledge contributions of the following to work reported here:

NASA/MSFC	CSDL
Harrold Brown	Richard A. McKern
Lewis Cook	Robert Strong
Billie Doran	
Charles E. Lee	

Support of the CSDL Technical Publications Group is acknowledged.

The publication of this report does not constitute approval by the National Aeronautics and Space Administration of the findings or the conclusions contained herein. It is published only for the exchange and simulation of ideas.

ABSTRACT

Design of each system component is described. Emphasis is placed on functional requirements unique in this system, including data bus communication, data bus transmitters and receivers, and ternary-to-binary torquing decision logic. Mechanization drawings are presented.

TABLE OF CONTENTS

TABLE OF CONTENTS (Cont.)

TABLE OF CONTENTS (Cont.)

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Cont.)

LIST OF TABLES

1.0 INTRODUCTION

This document forms part of the final report on the Space Shuttle Avionics Multiple IMU System, NASA/MSFC Contract NAS8-27624.

The contract was originally awarded to the Charles Stark Draper Laboratory on July 7, 1971. The initial twelve month effort was devoted to the study and definition of failure detection and isolation (FDI) requirements for a multiple gimballed system. It also addressed prelaunch requirements for calibration, ground alignment and gyrocompassing as well as an inertial navigator. Under this task, a preliminary test plan was formulated around the demonstration of FDI development using three redundant KT-70 IMUs and a single 4π-CP2 computer. In interim report covering this work phase (R-733, Space Shuttle Avionics a Redundant IMU On-Board Checkout and Redundancy Management System) was published in September, 1972.

This contract was amended in June, 1972, to add several additional tasks. Detailed electronic design of all system units was to be accomplished. These interface units would be assembled and their designs verified. An integrated, redundant IMU system would be demonstrated and delivered to NASA/MSFC. Software for this system was also specified. Deliverable software included ground alignment and gyrocompassing, an inertial navigator and a full regime of FDI programs (Tape 1). A multi IMU calibration program was also required (Tape 2).

This final report is organized into four volumes which will present in detail all activity under the extension of the original contract which was approved on 3 August, 1972. This extension provides development of both hardware interfaces and software coding for a laboratory demonstration of this redundant IMU system based upon three KT-70 IMUs and a single 4π-CP2 computer.

The four volumes described analytical and developmental activities, hardware design, software design, and a system test plan. Each volume is described briefly below.

Volume I-Multiple IMU System Development

A review of the contract is presented. Analytical work and digital simulations defining system requirements are fully described. Failure detection and isolation algorithms are derived.

Volume II–Multiple IMU System Hardware Interface Design

Design of each system component is described. Emphasis is placed on functional requirements unique in this system, including data bus communication, data bus transmitters and receivers, and ternary-to-binary torquing decision logic. Mechanization drawings are presented.

Volume III–Multiple IMU System Software Design and Coding

Design of system software is explained. Both individual routines and their interplay are described. Executive routines, ground alignment, gyrocompassing, navigation and calibration routines are presented and described using flowcharts. Failure detection and isolation algorithms and system reconfiguration procedures are also presented and described with flowcharts.

Volume IV–Multiple IMU System Test Plan

Operating procedures for this redundant system are described. A test plan is developed with two objectives. First, verification of the hardware and software delivered is demonstrated. Second, applicability of multiple IMU systems to the space shuttle mission is shown through detailed experiments with FDI algorithms and other multiple IMU software: gyrocompassing, calibration, and navigation. Gimbal flip is examined in light of its possible detrimental effects on FDI and navigation.

1.1 Introduction to Volume II

Volume II, Multiple IMU System Hardware Interface Design, of this report draws together a comprehensive description of the hardware designed and delivered by CSDL under contract NAS8-27624.

The system developed under this contract employs three off-the-shelf Singer Kearfott KT-70 IMUs operating under the control of a single IBM 4π-CP2 computer. CSDL designed and built all other system components. Brief descriptions of the IMU and the computer, each with their ancillary equipment, are presented in Chapters 2 and 3.

Chapter 4 comprises a description of the test area and facility at NASA/MSFC.

CSDL designs are then discussed in detail. The processor interface unit is described in Chapter 5. Chapter 6 discusses the data bus. Chapter 7 discusses the IMU interface unit. The system's power distribution system is described in Chapter 8.

1.2 System Overview

An idea of the overall system designed may be gained by examining Figure 1-1, System Interconnect Diagram. Although only a single IMU string is shown, all other components are in place.

The salient hardware feature of this design is the use of a serial data bus (operating at 10MHz) for Computer/IMU communications. The IBM 4π-CP2 computer is interfaced to four bus destinations through a processor interface unit (PIU). Computer/PIU communication utilizes parallel transfer. The PIU encodes and decodes data bus traffic for the computer, routing it as required. It also serves as an I/O buffer for the computer, which cannot operate at the required bit rate. Consequently, a First In First Out memory is incorporated in the PIU to compensate for the disparate data rates.

Three of the bus addresses are IMU interface units (IUs), and the serial bus is used. The fourth destination is an HP2116B computer, an integral part of the test laboratory's SSCMS test facility (described below). Although the 4π-CP2 sees this connection as another equivalent data bus address, the PIU simply routes HP communications onto a parallel bus. No encoding is required.

All communications links are bidirectional.

The IMU and its adaptor power supply are connected through the IU, allowing computer control over several functions left automatic in the normal Kearfott system. In addition, the IU has 14 bit synchro-to-digital converters for the roll, pitch and azimuth axes, gyro torquing logic and ΔV accumulators. It carries a bus receiver/transmitter, and acts to decode commands and encode demanded data for the PIU.

The chapters which follow comprise detailed descriptions of each system component.

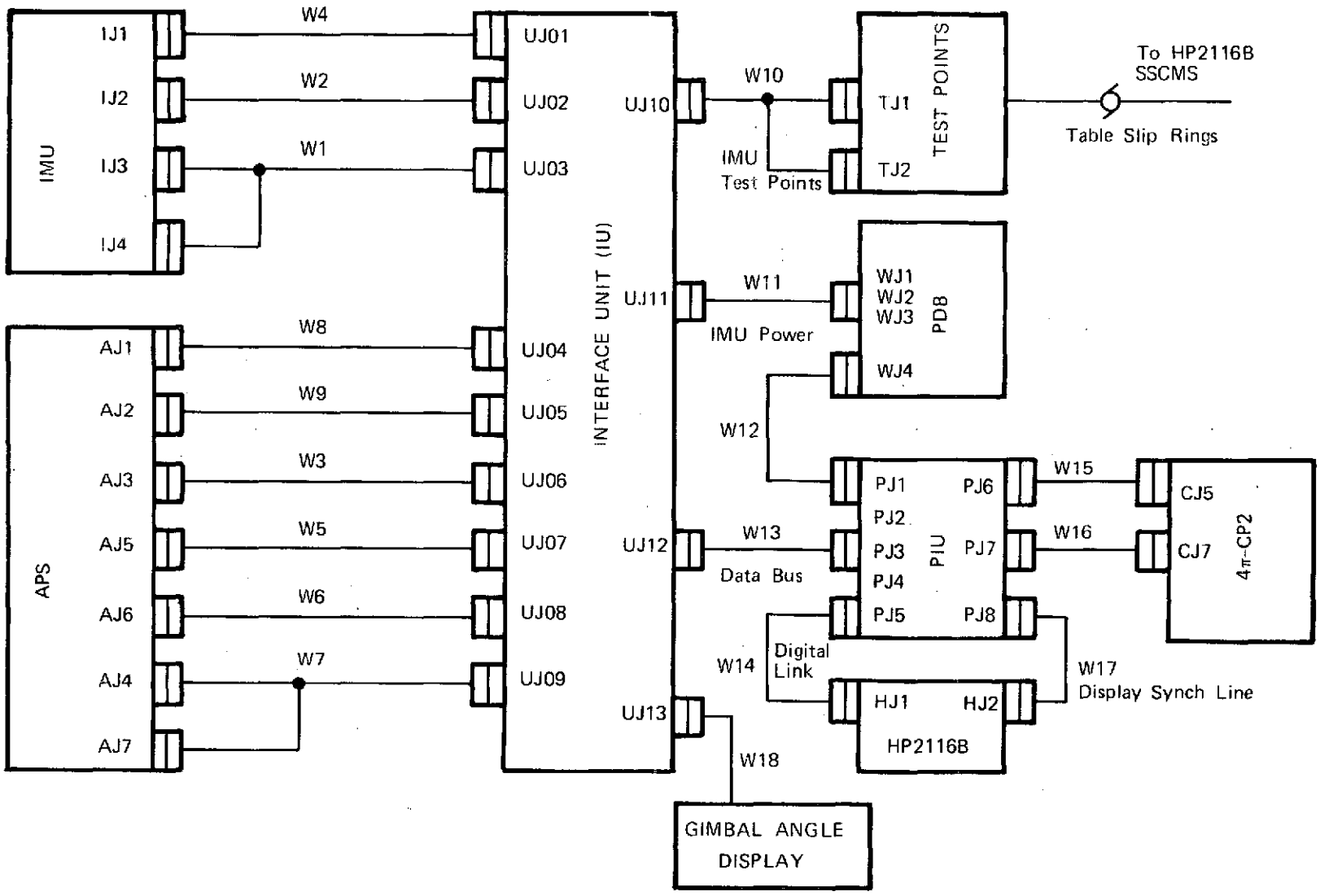


Figure 1-1. System Interconnect Diagram.

2.0 IMU AND ADAPTOR POWER SUPPLY

This redundant IMU system was designed to employ three off-the-shelf Singer Kearfott KT-70 (AN/ASN-90) IMUs and their Adapter Power Supplies (APS). Although these units are fully described elsewhere, a brief review is presented here[1,2].

2.1 Physical Characteristics

The KT-70 IMU carries a four-gimballed platform containing two two-degree-of-freedom dry, flexure-mounted wheel gyros and a single- and a two-degree-of-freedom dry flexure accelerometer. The redundant gyro axis is slaved to null. Three gimbal axes hold single speed synchros. The outer roll is slaved to the inner (redundant) so that the inner roll angle is nulled, and pitch/azimuth gimbal orthogonality is assured. Gimbal angle outputs are considered accurate to $\pm$ 2 $\hat{m}in$ 1σ.

Integrated circuits are employed in the electronics where applicable. Moding is controlled by relays, however, driven by discretes from the APS. (Some moding control has been assumed by the computer in this system implementation.)

Accelerometer output pulses represent quantized decrements of integrated rebalance current, and are asynchronous in nature. There are two computer controllable gain settings. The IMU's electronics also includes BITE circuitry.

Gyros may be torqued either digitally, at 0.4 $\hat{s}ec$/pulse and at a maximum rate of 80°/hr, or by analog signals. The azimuth axis may be analog torqued at 1.5°/s (5400°/hr), while pitch and roll gyros may be torqued at 0.5°/s (1800°/hr).

The APS draws 115v, 3 phase, 400 Hz power from an external source, and provides all DC and AC levels required by the IMU. A battery pack mated to the APS provides transient protection. The APS also contains a sequencer which automatically controls turn on and moding of the IMU in response to application of power.

Physical properties are listed in Table 2-1, KT-70 Physical Characteristics. Table 2-2, Maximum Acceptable Dynamic Inputs, lists limits on operational environments. KT-70 IMU Functional Diagram appears as Figure 2-1.

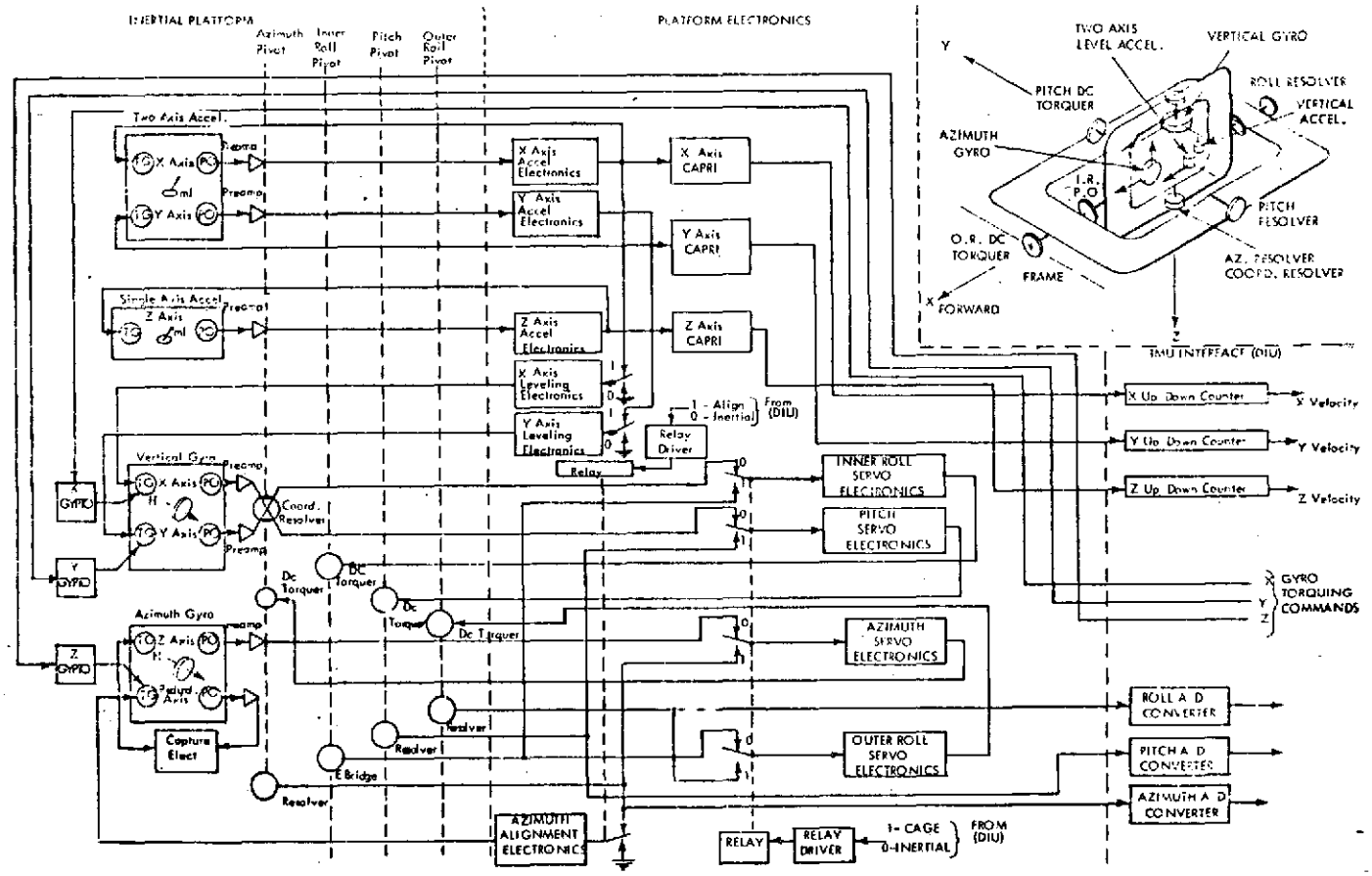


Figure 2-1. KT-70 IMU Functional Diagram

Table 2-1 . KT-70 Physical Characteristics

CHARACTERISTIC	IMU	APS*	TOTAL
Volume (in^3)	650	1000	1650
Weight (lbs)	19	40	59
Avg. Power (va)	70	120	120
Peak power (va)	130	210	210
Turnon Power (va)	830	910	910

*Including battery pack.

Table 2-2. Maximum Acceptable Dynamic Inputs

AXIS	ANGULAR RATE ($^o/s$)	ANGULAR ACCELERATION ($^o/s^2$)	SPECIFIC FORCE (g)
Roll	± 300	±1500	——
Pitch	±60 (< 70^o) ±35 (70-110^o)	± 200	——
Azimuth	±200	± 200	——
X	——	——	± 10
Y	——	——	± 10
Z	——	——	±10

2.2 Modes of Operation

In this system, only one of the built in modes of the KT-70 is enabled. Specifically, automatic turnon and vertical erection moding in response to power on is used. All further moding of the IMU is performed using closed loop programs under computer control.

3.0 IBM 4π-CP2 COMPUTER AND ANCILLARY EQUIPMENT

The computer employed in this system is an IBM 4π-CP2 general purpose computer with auxilliary memory. External control and I/O is accomplished through use of a Field Operating Unit (FOU).

3.1 Field Operating Unit.[1,2]

The FOU is designed to afford a means of testing the 4π-CP2 computer, or of controlling its operation and I/O. This instrument is equipped with a typewriter, paper tape reader and paper tape punch.

Computer control functions available through the FOU include starting/stopping execution, displaying or loading given memory locations and registers and observing the machine's status. CPU control can also be exercised by automatic stops at given instructions, or manual stepping through programs.

When the tape reader is used to load the computer, as in this system, the FOU serves to verify the load.

3.2 4π-CP2 Computer and Auxiliary Memory[3,4]

The 4π-CP2 is a general purpose, stored program, parallel, fixed point, binary computer. The unit stores 8K 32 bit words (or 16K 16 bit words). Auxiliary Memory's capacity doubles this figure.

Memory cycle time is 2.5 us. Typical instruction times are:

Add	3.8 us
Multiply	18.1 us
Divide	46.3 us

In this usage, the computer is configured for externally controlled input and output. That is, the processor interface unit controls all data transfers. I/O rates are 60K words/s.

Discrete in bits are also used, one example being the input parity error bit (IPE2) generated at the PIU. Computer cycle times are determined by an external interrupt driven by the PIU's 10 MHz master oscillator.

Instructions operating on both full (32 bit) and half (16 bit) words are available. Instructions may be storage protected.

There is one dedicated index register in the CPU. Additionally, two "soft" index registers are set up in main storage.

4.0 SYSTEM TEST FACILITY

The laboratory demonstration multiple IMU system is to be tested at NASA/MSFC, using a highly flexible, computerized test facility originally developed for NASA/ERC. The Strapdown System Control and Monitor Station (SSCMS) provides the ability to monitor the redundant system and control its dynamic environment.[1,2] The SSCMS' HP2116B computer is used to control the 36" Goerz test table[3,4] and collect data in real time. The facility also includes magnetic tape storage, a line printer and a plotter, all used in testing this system.

The Goerz table rotary axis is computer controllable (by the HP2116B) with respect to both rates and positions. Pure slews, ramp rates and sinusoidal oscillations about the table's rotary axis may be commanded, and may be superimposed. Oscillatory capabilities are limited by servo characteristics dominated by the mass of the table plate and the redundant system mounted on it. Estimated excursions attainable are 10° p-p at 1 Hz, falling off at approximately 40 db/decade for higher frequencies. Readout accuracies with the table in motion are approximately 10^{-4} degrees at low rates, with accuracies degrading to about 10^{-1} degree at rates greater than 10°/s.

A test point harness has been built to connect each IU's analog test point signals to the SSCMS using the table's sliprings. These signals, as listed in Appendix A of Volume IV of this report, CSDL Avionics Memo #74-3, Analog Test Point Listing for the Laboratory Demonstration Multiple IMU System, could be displayed and recorded at the SSCMS. The signals would be processed by digital voltmeters, ohmeters, ammeters and frequency counters, with sequencing and probable ranges controlled by the HP2116B computer.

The digital downlink from the 4π-CP2 to the HP2116B, using the formats shown in Appendix B of Volume IV, is exercised every 0.2s in all system operational phases. (The formats are also displayed at the FOU typewriter at a lower update rate.)

5.0 PROCESSOR INTERFACE UNIT

The processor interface unit (PIU) is the interface between the 4π-CP2 computer and the four data bus addresses. It functions to encode and decode communications for the computer, and to serve as an I/O buffer. Parallel data transfers, at 60K words/second, are used between the computer and the PIU. Data transfers to one bus address (the HP2116B), are accomplished by a parallel bus at low rate. The other addresses are reached by a 10MHz serial data bus.

5.1 Overview of PIU Functions

An overview of the functions and functional units of the PIU may be gained from PIU Functional Drawing, Figure A-2.

Four tasks are assigned to the PIU: IMU write, IMU read, HP write, HP read. To perform them, the PIU is required to encode and decode data bus communications, perform master timing for the system, including both computers, and control 4π-CP2 I/O.

The PIU's 10 MHz master oscillator provides all timing for the system, from the 10 MHz bus clock to the 50 Hz minor cycle control. The 10 MHz pulse train drives a nine bit (eighteen state) Johnson counter which provides the timing pattern required for data bus encoding and decoding. It also provides the clock for the finite state controller.

The finite state controller directs the PIU in carrying out its assigned tasks. It will be discussed in Section 5.3.

The function register (F) receives instructions from the computer, under direction of the finite state controller, defining tasks to be performed. Its bit pattern largely determines the actions of the finite state controller.

F Register Bit Assignments are presented in Table 5-1. They include the data bus address to be written to or read from, READ/WRITE, PIU TEST/NOTEST, SYNC/NOSYNC and the word count.

Similarly, the address register (A) is loaded by the computer in response to controller commands, indicating the starting data address in the 4π-CP2 to be written out of or read into.

TABLE 5-1. F REGISTER BIT ASSIGNMENTS

Bit	Function if true
16	Bus Address (see below)
15	
14	READ = $\overline{\text{WRITE}}$
13	SYNC = $\overline{\text{NOSYNC}}$
12	TEST = $\overline{\text{NOTEST}}$
11	Not Used
10	
9	
8	
7	
6	
5	Word Counter (all true = WORDØ)
4	
3	
2	
1	

Bus Address:

Bits		Address
16	15	
0	0	HP = $\overline{\text{IMU}}$
0	1	IMU1
1	0	IMU2
1	1	IMU3

Also shown in the functional drawing there is a three word deep First In First Out (FIFO) memory. This memory is used in all PIU/IU I/O, again under control of the state controller. In one task, as an example, IMU write, the three words are loaded with a two or three word message, which is transmitted on command of the controller. Each word is loaded into word 1, and is rolled to the next location as the following word is loaded. The contents of FIFO memory are then encoded and transmitted in sequence. That process is more fully described in Chapter 6, DATA DATA BUS DESIGN. FIFO memory is required to buffer I/O as bus transmissions are 1.8 us/word long while computer/PIU parallel transfers require 16.7 us/word.

5.2 Physical Description of the PIU

The PIU is a rack mounted unit. It carries two control switches, a push-button ABORT, which functions to reset the finite state machine to state 0 and to issue a discrete interrupt to the computer (DINT 3), causing a restart, and a switch which sets a bit of the computer's discrete input register, causing transition from gyrocompassing to navigation. The ABORT switch is physically located at the FOU.

The rear panel of the PIU holds connectors for the 4π-CP2/PIU and HP2116B/PIU parallel interfaces, and the three data buses. A coax connector is used for the timing interface with the HP2116B, and there is a single power connector. Each is shown on the marked photograph in Appendix B, PIU Mechanical Design.

Also indicated in the photograph are the ± 15 VDC supply[1] (required for the bus receiver) and the 10MHz master oscillator.[2] Data bus drivers and receivers are indicated. 5 VDC logic power is provided by the power distribution panel.

The PIU employs TTL logic in standard 14- and 16-pin dual-inline-pack integrated circuits. DipStick[3] mounting hardware has been selected. Its advantages over competing designs include r-f shielding, a unique power and dc ground bus layout and built-in test points for each DIP pin. A board capable of holding 200 DIPs used.

5.3 Finite State Controller

The read/write tasks assigned to the PIU are directed by a Finite State Controller (Figure 5-1). With inputs from the function register and timing signals, distinct paths are traced out in the controller's state space. Each path represents a task or a branch on some condition.

The controller has the property of being either in one state or another. Asynchronous events either arrive in time to affect a transition (that is, before the leading edge of the 900 ns clock) or they are in time for the next clocked transition. Some events are externally synchronized to be out of phase with the state switching clock, i.e., to occur during some state.

Initially, the controller is waiting in state 0. On receiving a start command from the 4π-CP2 (DOT 1), the controller advances to the next required state, staying in it until that state's output conditions are met. Then, on the next clock pulse, the controller advances to the next required state for the chosen path. Each state entails

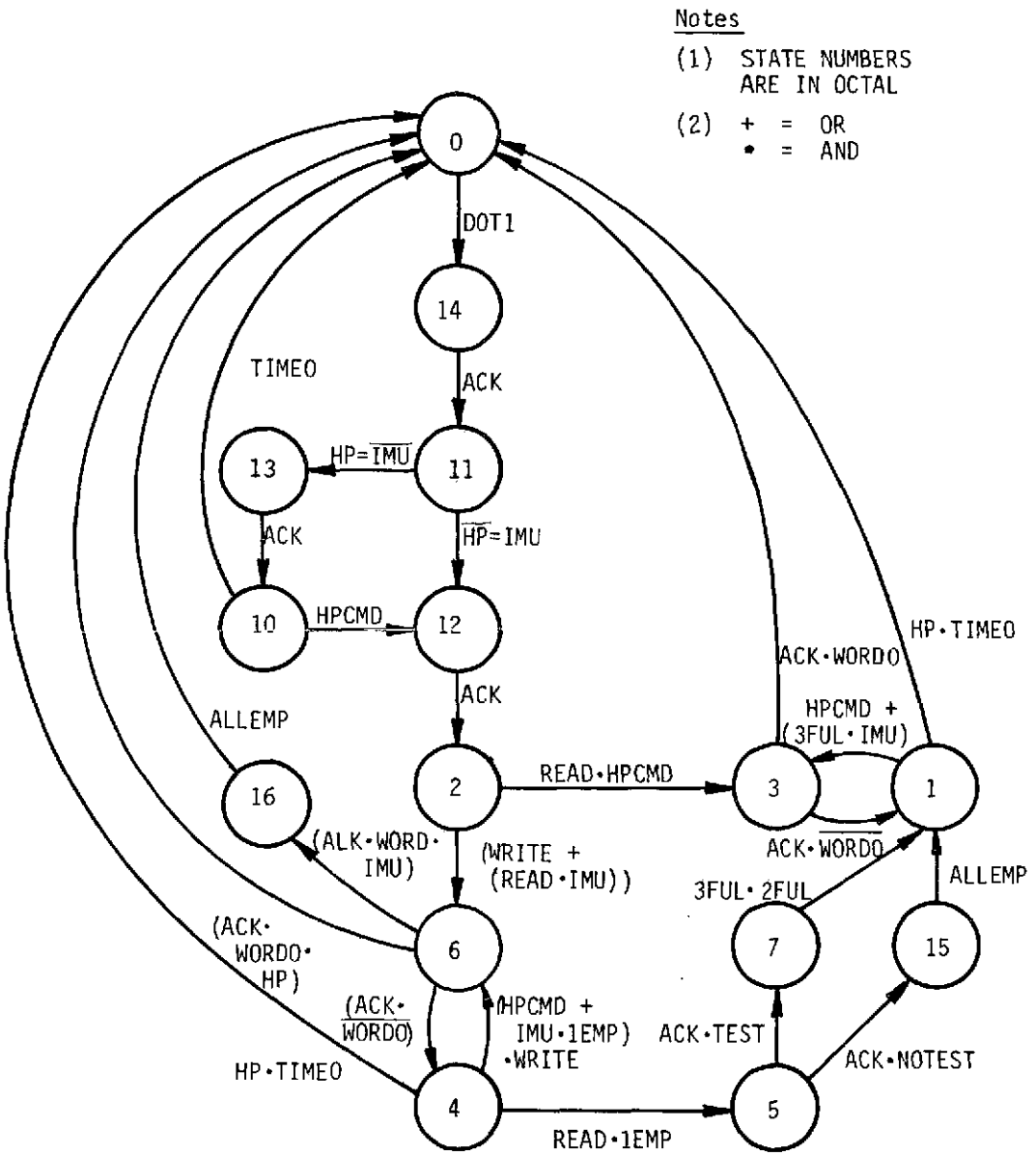


Figure 5-1. Finite State Controller (State Space).

performing a specific function, and is exited on predetermined conditions. A 900 ns (1.1 MHz) clock is used.

As stated above, four tasks were envisioned: IMU write, IMU read, HP write and HP read. The last of these, HP read, was, in fact, not implemented in the delivered hardware. Its path through the controller will be discussed, however, for completeness. One additional path, a computer test of the PIU's FIFO memory, is also discussed.

Several terms used in discussions of these tasks should be defined. These are:

Clock and ACK: the finite state machine is driven by a 900ns pulse train ("clock"), which is used to cause exit from many of the states. These states entail actions within the PIU only, and require times small compared to 900ns. States which involve I/O transfers between the 4π-CP2 and PIU require a minimum of 16.7us - the single word transfer time - and thus require another timing signal. The signal chosen is the computer-originated transfer complete acknowledge (ACK).

DOT 1: 4π-CP2 discrete output, used, in this application, to cause start of finite state machine processing.

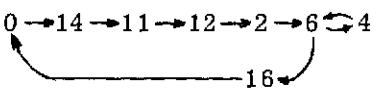
TIME0: time out condition for the return acknowledgement on transfers to the HP2116B. When HPFLAG request is issued, it starts a timer. If the acknowledging signal (HPCMD) is not received in time, TIME0 is issued and an error return to state 0 occurs. (Without this safeguard, the machine could hang up awaiting HPCMD, such as if the HP2116B were off.) The error return sets a discrete to the 4π-CP2.

ECI and ECO: I/O of the 4π-CP2. In this application, externally-(PIU-) controlled transfers are used.

The addresses given for ECI/ECO in the discussions of paths through the finite state machine are relative to location 0800 hex. That is, address = 1 implies reading location 0801.

5.3.1 IMU Write Task

The IMU write (or Command) path passes through these states:

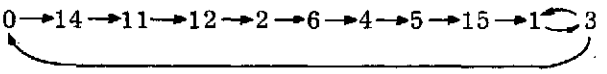


State	Action
0	Wait in IDLE for DOT1 (start command from 4π-CP2). On DOT1, go to 14.
14	Do ECO to load F register (address=0). On acknowledge (ACK) go to 11.
11	Examine bus address in F register. Find IMUi true, i.e., bits 16 and 15 read as a binary number equal i_2. On clock, go to 12.
12	Do ECO to load A register (address=1). Upon ACK, go to 2.
2	Examine bit 14 of F. As WRITE is true, go to 6 on clock.
6	Do ECO (address=A), loading word 1 of FIFO memory with one word from core address A. Wait for ACK. Then, if the word count (F register bits 1-8) is non-zero, go to 4. Otherwise, go to 16.
4	Increment the word count and A by one. Wait for 1EMP; i.e., notice that word one of FIFO is empty, and then go to 6. Processing of the 6⇄4 loop will continue until the word count is zero and the controller enters state 16.
16	Initiate the transfer to the IMU. FIFO is read out serially, one word at a time, and its contents are encoded and transmitted. On ALLEMP, or FIFO empty, go to 0.

IMU write messages are tabulated and explained in Chapter 7. They include the slew and moding command, gyro torquing command, and a Request Accelerometer Update (RAU) command. This command does not carry any data.

5.3.2 IMU Read Task

The IMU read task (data demand) uses this path:

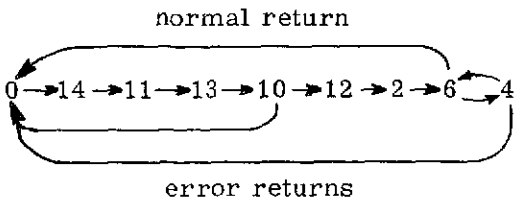


Processing up to the transition to state 2 is identical with that of the IMU write task. This is because the read process (discussed in detail in Chapter 7) requires telling the IU what data is required, which is done by writing that information to the IU.

State	Action
2	There are two conditions causing transfer from 2 to 6. These are WRITE is true, as in the IMU WRITE task, or READ and IMU are true, as in this task. Therefore, on clock, go to 6.
6	Do ECO (address=A), loading FIFO memory with the B word. (The B word is a part of the bus message, which is explained in the next chapter.) As the word count is nonzero, on ACK go to 4.
4	Increment the word count and A. Wait for 1EMP. As READ is true, exit to 5.
5	Do ECO (address=A as incremented), loading FIFO memory with the C word. (The C word also is part of the bus message. See the following chapter.) Upon ACK, as NOTEST is true, go to 15.
15	Initiate the transfer to the IMU. Wait for ALLEMP (transfer complete), and go to 1. Increment A and the word count. Wait for 3FUL (FIFO loaded with at least one data word from the IMU) and on it go to 3.
3	Initiate ECI to address=A (as incremented). Wait for ACK. Then, if the word count is non-zero, go to 1. Otherwise, go to 0. The 1⇄3 loop will be processed until all desired data is transferred, as indicated by WORD0 or word count equal to zero.

5.3.3 HP Write Task

The HP write (downlink) path passes through these states:

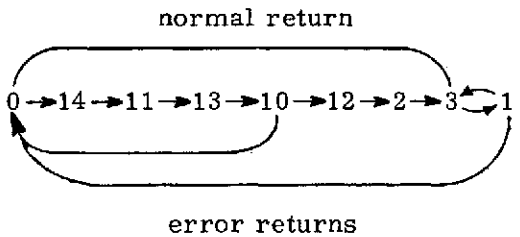


Two error return paths are indicated in the HP write procedure, both caused by TIME0. It might be felt that with the high number of words to be transferred over the downlink (up to sixty-four 16 bit words in the delivered formats), there was some possibility of exceeding allowable time for the transfer. In practice there is no problem. In minor cycles including HP writes, the three IMUs are given their gyro pulse torquing commands first (see Chapter 7, INTERFACE UNIT), which involves three IMU write tasks. The downlink is then entered immediately. Downlink times are dominated by the 16.7us 4π-CP2/PIU transfer time. Sixty-four words require 1.07ms or 5.4% of the minor cycle time.

State	Action
0	Wait in IDLE for DOT1. On DOT1, go to 14.
14	Do ECO to load F (address=0). On ACK, go to 11.
11	As HP is true, on clock go to 13.
13	Do ECO (again with address=0), to transfer the F word to the HP. On ACK, go to 10.
10	Wait for HPCMD. Upon receiving the F word, the HP2116B will issue CMD, indicating readiness to receive formatted data. If HP and CMD are true, HPCMD is formed. If the HP2116B does not answer, TIME0 will eventually cause an error return to 0 without the write task's having been done. On HPCMD, go to 12.
12	Do ECO to load A (address=1). Upon ACK, go to 2.
2	Write is true. Therefore, on clock, go to 6.
6	Initiate ECO (address=A), using the parallel transfer to the HP2116B. FIFO memory is not used. Wait for ACK. On ACK, if the word count is zero, return to 0. Otherwise, go to 4.
4	Increment the word count and A by one. If TIME0 occurs, there will be an error return to 0. Otherwise, on clock, go to 6. The 6⇄4 loop will be processed until one of two return conditions is met: normal return 6→0 on word count=0 or 4→0 on timing out.

5.3.4 HP Read.

The HP read (uplink) task was envisioned as a rapid way to change resident coding in the 4π-CP2, such as in changing compensation parameters. This task was not implemented in the delivered system. Its path would have been:

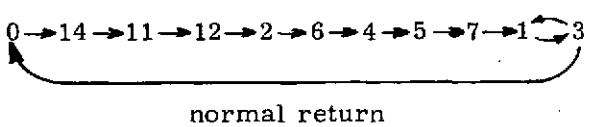


Processing through to the transfer to state 2 would be identical with that of the HP write task. Then:

State	Action
2	As READ and HPCMD are true, on clock, go to 3.
3	Receive word from the HP2116B. Do ECI to address=A. Wait for ACK. If the word count still to be received is zero, go to 0. If the word count is non-zero go to 1.
1	Increment the word count and A by one. If TIME0 is true, return to 0 (error return). Otherwise, on clock go to 3. The 3⟲1 loop is processed until all data is received (3→0 normal return) or time runs out (1→0 error return).

5.3.5 FIFO Memory Test Task

The FIFO memory test task is similar to the IMU read task, except that no data is transferred to either an IMU or the HP2116B. The path is:



This is identical with the IMU read task, except that, as TEST is true, state 15 is bypassed and no bus transmissions occur. ECIs performed at 3 read the same data delivered to the PIU back to the 4π-CP2 for comparison in the order they were originally written out. In effect, then, the test determines that ECO, the FIFO memory and ECI are all functioning.

6.0 DATA BUS DESIGN

CSDL has designed the laboratory demonstration redundant IMU system to be compatible with the NASA/MSFC Type II Data Bus Terminal (DBT) as defined by Document 50M16240, Revised July 17, 1972. The following sections of this chapter describe the data bus, coding and message formats and the bus transmitter and receiver designed as part of this effort.

6.1 Data Bus

The bidirectional data bus envisioned in the referenced specification consists of four twisted shielded wire pairs, each with a single function. Referenced to the PIU (the DBT of the specification), the functions are transmit clock, transmit data, read clock and read data. This design is shown in Figure 6-1, DBT to I/O Channel Interface (Figure 2.1 of the specification).

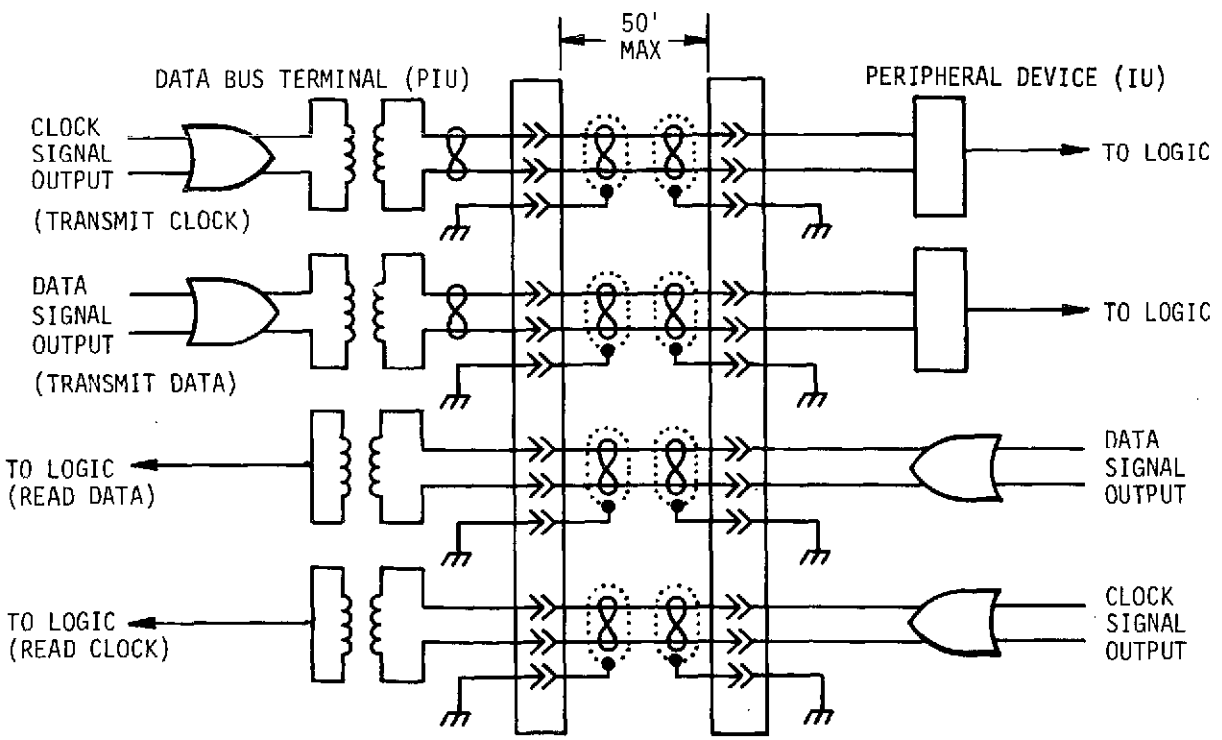


Figure 6-1. DBT to I/O Channel Interface.

In the figure, the DBT is an integral part of the PIU. As designed at CSDL, the PIU simulates three separate DBTs. In fact, it has only a single DBT which feeds the three bus transmitters. The Interface Unit (IU) corresponds to the peripheral device.

The bus is operated at 10MHz, or with a bit length of 100ns.

6.2 Coding and Message Formats

Data bus transmissions are coded in bipolar alternate-mark-inversion (AMI). In this format, each "one" in a data byte is transmitted with opposite polarity to the preceding "one". "Zero" is transmitted as a zero. An example is given in Figure 6-2, Shift Register Output and Bus Format. Given a message at the shift register output (Figure 6-2a), its equivalent in AMI code (Figure 6-2b) is marked by opposite polarity pulses for succeeding "ones".

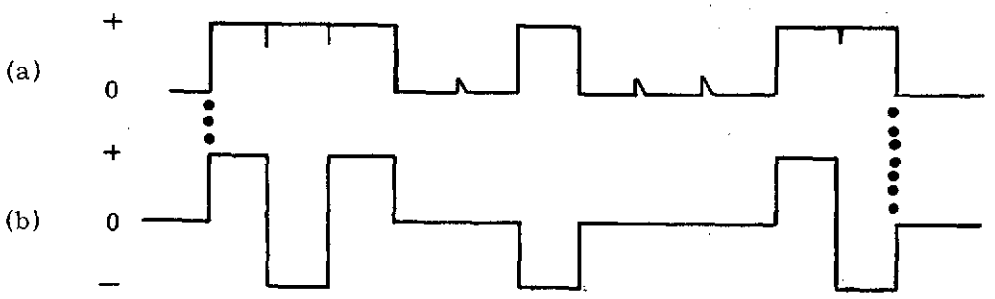


Figure 6-2. Shift Register Output and Bus Format.

AMI coding has certain advantages over a one-sided or non-return-to-zero coding. Among them, AMI requires a smaller bandwidth than one-sided coding (as there are no bursts of pulses requiring lower frequency resolution of the receiver). In addition, transmission line charging is eliminated.

Words in the data bus messages are 18 bits, or 1.8us, long. That is, they comprise a lead bit, sixteen data bits and a parity bit. The data bits are the information transferred.

Bus transmissions from the PIU to the IU consist of two or three words: a B word, possibly a D word and a C word. The B word is a function word or message label, and carries information outlining what is being commanded or demanded. The C word (see Figure 6-3, C Word Format, Figure 1-3 of the specification) is a bus status word, and is used to end all messages. In this system, the C word is received by the IU and is echoed to the PIU without modification.

D words contain the actual commands. Two uplink D words are defined: D_1 contains IMU commands, and D_2 contains GYPTO commands. Uplink RAU messages require no D word.

Data demands also carry no D word, as the B word indicates the desired data.

Downlink messages are of the form D word, C word. The D word is the requested data (status, accelerometer data or gimbal angles). Up to three D words might be required for a message in this implementation.

All bus message formats are listed and explained in the next chapter, INTERFACE UNIT, in terms of the specific actions each requires.

6.3 Data Bus Transmitter

The logic preceding the Data Bus Transmitter (Figure 6-4) formats the data onto two separate signal lines. One line carries those data bits to be transmitted with a positive sense, the other those to be negative-going pulses. Each line drives a transistor attached to one end of a pulse transformer, the two acting as a differential driver. The resulting signal on the transformer secondary is the desired bipolar signal as illustrated in Figure 6-2.

Identical drivers are used for the transmit clock and transmit data lines, both in the PIU and the IU.

It should be noted that the diode in the collector circuit is reverse biased to any signal which might be generated on the bus by another driver, as for another subsystem. An inactive transmitter, therefore, appears as a large impedance in parallel with active devices.

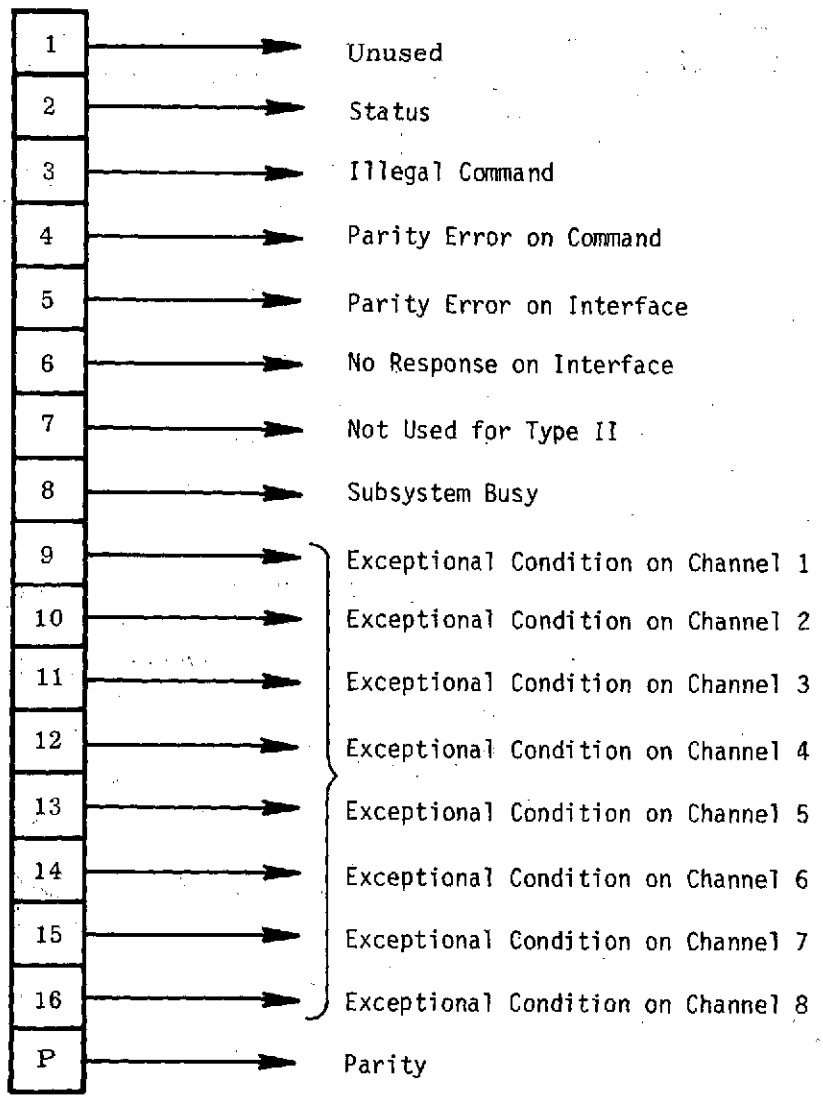


Figure 6-3. C Word Format

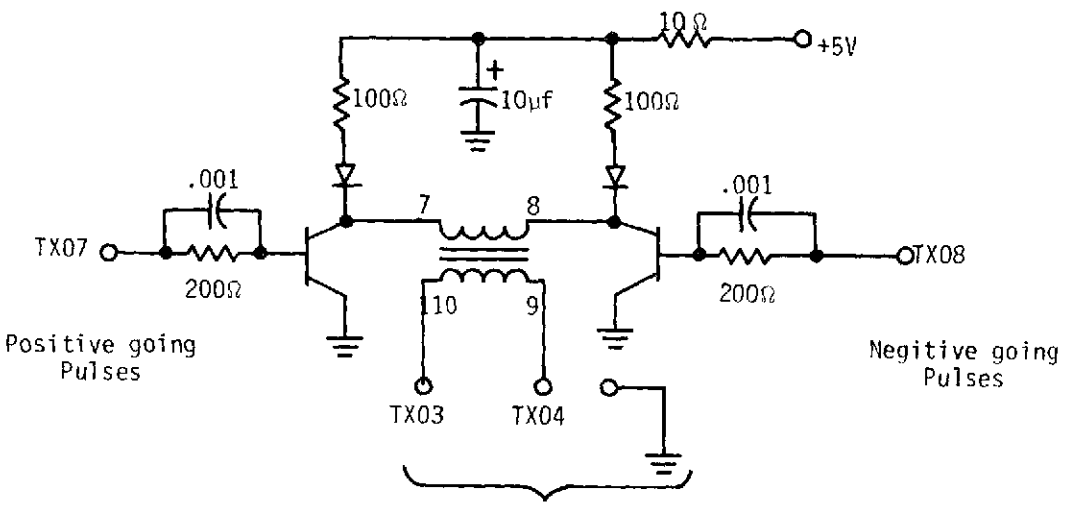


Figure 6-4. Data Bus Transmitter

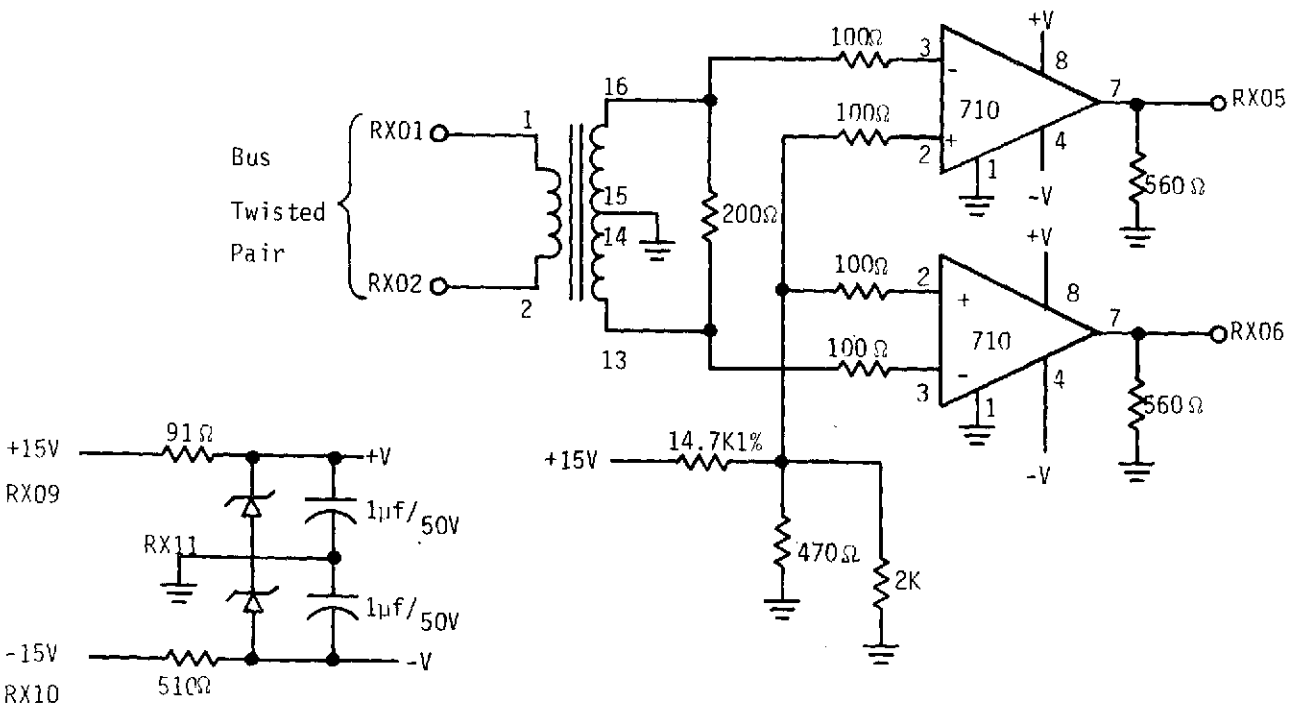


Figure 6-5. Data Bus Receiver

6.4 Data Bus Receiver

The Data Bus Receiver (Figure 6-5) is a center-tapped pulse transformer which forms and sends two signals of opposite phase to two comparators. Each comparator also has as input a small DC voltage to provide some measure of noise immunity. The outputs of the two comparators will be at ground whenever an input pulse exceeds the threshold voltage. The outputs, therefore, appear to be the compliment of the two lines which drive the differential transistors in the transmitter. Their logical OR, then, reconstructs the original message in shift register format (as in Figure 6-2a).

6.5 Summary

CSDL has designed a bidirectional bus operating at 10MHz in concert with NASA/MSFC's breadboard data bus specification. It has been shown that, using a serial bus, a single computer may achieve control over a redundant IMU system in an effective manner.

7.0 INTERFACE UNIT

This chapter describes the Interface Unit (IU). A description of the IU's function is presented and a physical description of the IU follows. Electrical design of the IU is discussed, with detailed references to the functions performed by the device.

7.1 Overview of The Interface Unit's Function

An appreciation of the IU's function may be gained by examining the Interface Unit (IU) Connections, Figure 7-1. The IU serves as the interface between the IMU and the computer and its interface. The IU decodes data bus transmissions from the PIU, determining which are addressed to it. These transmissions can synchronize accelerometer readings, command (IMU command and GYPTO command) or demand (read accelerometers, read S/D converters, read IMU/IU status). On read demands, the IU encodes a reply acknowledging receipt of the message and including any requested data. The IU must also act on commands.

Initial designs of this system included a separate system sync line in the form of a fifth pair in the data bus. Sync signals are required to enable taking simultaneous data which is felt to be essential for FDI and is desirable for navigation. NASA/MSFC initially directed that no separate sync line be used. Therefore, a sync command (RAU) was included. It is a variation of the write command, with an address recognizable by all IUs, which contains no data. This command, in the delivered hardware, also functioned to reset the free-running, 400pps multi-vibrator in each IU used for GYPTO timing. It has been found that this approach resulted in apparent large gyro bias uncertainties, and a retrofit has been made. The change entailed using a system synch line to provide the 400 Hz timing for all IUs' GYPTO electronics from a single source in the PIU.

IMU commands include mode changes (ground align to inertial mode, for instance), resetting discretes (turning off IMU fail indicator to enable looking for a confirming discrete) and analog torquing and torquing sense descretes.

The gyro torquers must be commanded in a binary mode dithering at a 200/s rate. Calculated torquing commands, as for drift compensation, are added to this pattern as net excess pulses. The causes two problems. First, commanding nine axes in this manner carries an intolerable computational burden if done entirely in software. Second, the data bus specification requires that no signal be sent more than 50 times/s. Accordingly, the binary moding is left to hardware in the IU, and the computer delivers commands at a rate of 50/sec, in the form of a torquing

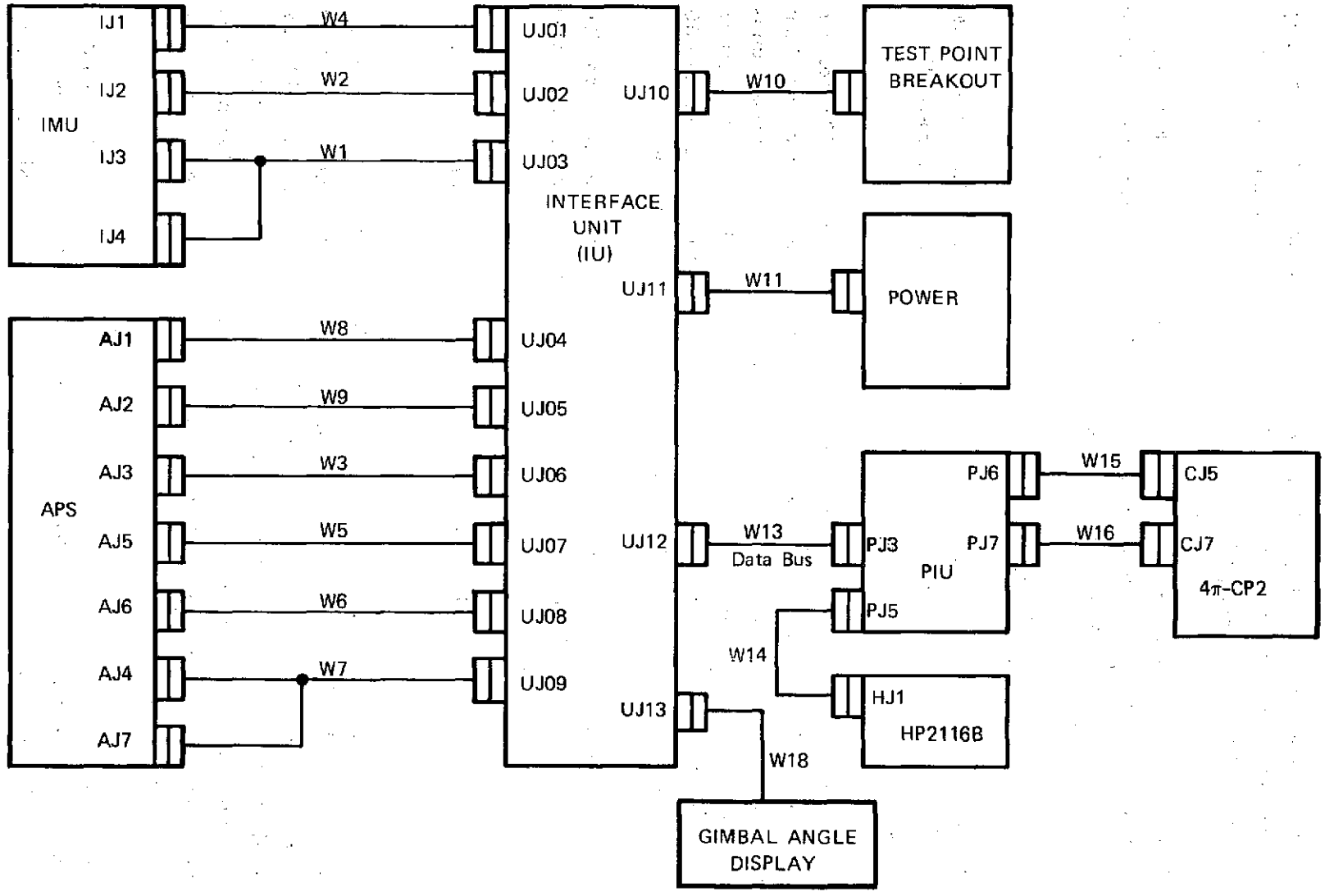


Figure 7-1. Interface Unit (IU) Connections.

pattern for the next four periods. The pattern conveys the information in ternary form: pulse and sign or no pulse in a particular interval. The IU hardware fills in the required background binary pattern.

The Interface Unit also serves to interface the IMU and APS. In this manner, all signals and power lines between them in the off-the-shelf Kearfott system are accessible for monitoring and control purposes.

7.2 Physical Description of The IU.

The present design has been tailored to permit mounting three IUs side-by-side above the heavier IMUs and APSs on the Goerz 500 system test table. Each IU is a rectangular box approximately 8x10x20".

The front panel of the IU carries the nine connectors (UJ01 to UJ09) serving cables to the IMU and APS. Additionally, connectors for the test point breakout and digital gimbal angle display are mounted on this panel. Four discrete lamps are built in: System Ready, IMU Fail, IMS Fail, and IMU BITE Fault. A switch is provided to activate the IMU Fail bit in the status word. It is used to simulate IMU hard failures or to take an IMU offline during certain phases of testing.

The rear panel of the IU holds connectors for the system power cable and the data bus. Fuses for the 115v 60 Hz line and the IU's +5vdc supply are mounted here.

Appendix C, IU Mechanical Design, contains marked photographs of these panels.

While the System Power cable carries other voltages through the IU, the IU itself uses only 115v 60Hz 1ϕ power. Internal +5vdc and ±15vdc supplies[1] provide all DC levels required within the unit. The ±15vdc supply is mounted inside the rear panel, as is the AC power terminal board. The +5vdc supply is side-mounted, along with terminal boards for DC power and test point breakouts. Lamp drivers for the discrete displays are also on the side panel. Each of these items is similarly marked in Appendix C.

The three synchro-to-digital converters are mounted on the bottom plate. These units are Transmagnetic, Inc. Model 1623EC1-01 converters. A full specification of this device is presented in Appendix D, Synchro-to-Digital Converters. Briefly, the 1623EC1-01 is a solid state unit designed to convert 11.8 vrms L-L,

400Hz, three wire synchro signals to 14 bit, parallel output form. Output is TTL compatible. Resolution (one bit) is 1.3 $\widehat{\text{min}}$ and accuracy is ± 4 $\widehat{\text{min}}$. There is a lag error of approximately of 1 $\widehat{\text{min}}$, or one LSB, per RPM. Conversion is made 400 times/s, with the data ready bit off while output bits are being reset. Output of each of the three S/D converters is hard-wired to the gimbal angle display connector, and is accessionable by the logic which updates gimbal angle registers 2.5 times/s.

The IU employs TTL logic in standard 14- and 16-pin dual-inline-pack integrated circuits. DipStik[2] mounting hardware has been selected. Its advantages over competing commercial designs include R-F shielding, a unique power and dc ground bus layout and built-in tests points for every DIP pin. Two boards capable of holding 100 DIPs each are mounted on a hinge (see photographs in Appendix C). These boards also carry the data bus receiver and transmitter. Logic design and bus terminals are discussed below.

7.3 Data Bus Requirements

The data bus, and the bus transmitter and receiver designs, have been presented in Chapter 6, Data Bus Design. This section explores the data bus with specific reference to the IU.

The computer may write to ("command") or read from ("demand") in the IU, using the 10MHz serial data bus. Messages are encoded in bipolar alternate-mark-inversion (AMI).

AMI code is not selfclocking. For this reason, separate clock lines are required in the data bus. The transmitter clock pulse train is always present, interupted only by message sync signals (zeroes), as it is required by the IU. The read clock, normally zero, is present only when data is being read from the IU to the PIU. This line does not carry a message sync signal. Data lines are normally at zero, carrying information only when required.

Data words used on the bus are 18 bits long, containing a lead bit, sixteen data bits, and bus parity bit. With the bus operating at 10MHz, each word takes 1.8us to transmit. There is no space between words of a transmission. Read and write formats are detailed below.

In these formats, the B word is a command, and is read into the 16 bit B register in the IU. The C word carries bus status information. Presently, it is received at the IU and returned unchanged. The D word carries data, whether information written to or read from the IU.

The first word transmitted is loaded into the B register and there examined to determine what function is desired. Bits 1 and 2 are the address of the information to be transferred. Bits 8-10 contain the word count to be transferred, including the C word, and are used to preset a word counter. Bit 11 determines read/write (1=read, 0=write). Bit 12 set indicates a sync signal. Bits 16 and 15=10_2 indicate that the word loaded is, in fact, a B word. Presently used functions are tabulated in Table 7-1, B Word Formats.

Table 7-1. B Word Formats

Function	Abbrev.	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Sync Signal (RAU)	B_{WS}	1	0			1	0	x	x	x						x	x
IMU Command	B_{iWC}	1	0			0	0	x	x	x						0	1
GYPTO Command	B_{iWG}	1	0			0	0	x	x	x						1	0
Read Accel.	B_{iRA}	1	0			0	0	1	0	0						0	1
Read Status	B_{iRS}	1	0			0	0	0	1	0						1	0
Read S/D Conv.	B_{iRSD}	1	0			0	1	1	0	0						1	1

x = don't care. i = IMU number, W =>Write, R =>Read.

The NASA/MSFC specification includes a transfer of the system status word in each data transfer in either direction over the bus. In this design, the C word is unmodified in the IU, and is read out as it is read in. Parity errors are indicated in the D_{STATUS} word. The C word Format is shown in Figure 6-3, C Word Format

The D_i word corresponds to a similarly-named register in the IU, carrying data to be written into it or the data read out of it. These words are tabulated in Table 7-2, D Words.

Table 7-2. D Words

D_1	IMU Commands
D_2	GYPTO Commands
D_{AX}, D_{AY}, D_{AZ}	X, Y and Z Accelerometer Outputs
D_{SD1}, D_{SD2}, D_{SD3}	Pitch, Roll and Azimuth Gimbal S/D Converter Outputs
D_{STATUS}	System Status

Referring to the Formats shown in Tables 7-1 and 7-2, the full list of data bus transmissions may be constructed. Table 7-3, Data Bus Messages, lists them. Bx is the appropriate function word. A full discussion of each message appears below.

Table 7-3. Data Bus Messages

B_{WS} C	RAU	Write Formats (Commands)
B_{iWC} D_1 C	IMU Command	
B_{iWG} D_2 C	GYPTO Command	
B_x C	Data Demand	
D_{AX} D_{AY} D_{AZ} C	Accelerometer Outputs	Read Formats (in reply to Demands)
D_{SD1} D_{SD2} D_{SD3} C	S/D Outputs	
D_{STATUS} C	System Status	

Replies to data demands (using one of the Read Formats) must be sent within one word time (or 1.8 us).

7.4 IU Input Shift Register and Write Controller.

Data written in is processed in the Bus Receiver, which provides three timing signals and the data itself. When DTIME is on, the data word is clocked into the input shift register, MSB first. (The lead bit is stripped off.) A pulse on the PTIME line gates the shift to one of four places, decided by the write controller. These are the B Register, C Register, D_1 Register or D_2 Register.

The IU write controller directs the incoming data to the proper storage register. There are two possible incoming sequences. One is a read demand, Bx C, and the other a write, $BD_{1or2}C$. The proper sequence can be determined by looking at the B word while the second word is arriving. The controller comprises two flip-flops gated to the contents, of B Register bits 1 and 2 (the address). Four states are available:

State	Flipflops	
0	$\overline{W0}$	$\overline{W1}$
1	W0	$\overline{W1}$
2	$\overline{W0}$	W1
3	W0	W1

The four states are reached by use of a two bit Johnson counter. The Write Controller State Transition Diagram (Figure 7-2) shows the functions carried out.

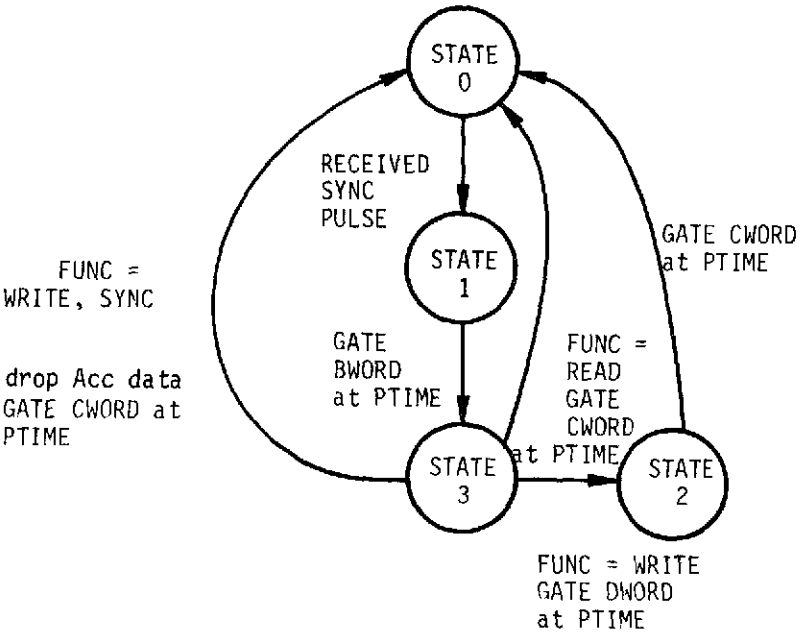


Figure 7-2. Write Controller State Transition Diagram

7.5 B Register Functions

When the computer transmits a message to the IU, the leading word is (if the format is appropriate) loaded into the B register. Bits in this register control further processing. As an example, if the B word is B_{RA}, read accelerometers, bit 11 indicates a read demand, bits 8-10 indicate that four words must be read back (i.e., the word counter is preset to 100_2), and bits 1 and 2 indicate that registers D_{AX}, D_{AY}, D_{AZ}, are wanted. Decoders operating on this address and count would gate the X accelerometer count from its shift register. The word count is decremented to 3 at the end of the shift and, in sequence, the Y accelerometer count is shifted out, the word count decremented to 2, the Z accelerometer count is read, the word count decremented to 1, the C word read out, and the word count decremented to zero causing a return to the idle state.

Data is collected from the various shift registers through a wired-or gate resynchronized with a clock and sent through the bus transmitter.

At the beginning of the proper minor cycle for reading Accelerometer, Synchro-to-Digital Converters, or Status, the appropriate buffer shift registers are updated. This update is independent of the request time and is controlled by the system sync command (RAU).

7.6 Status Register and C Register

A dedicated Status Register, D_{STATUS}, is employed to consolidate system discretes and indicate parity errors. Bit assignments are listed in Table 7-4, Status Register Bit Assignments. This register is updated on demands for status information, in this system 5 times/second. Parity Fail bits are reset on computer command.

TABLE 7-4. STATUS REGISTER BIT ASSIGNMENTS

Bit	Function (when true)
16 (MSB)	System Ready
15	IMS Fail
14	IMS Fault
13	IMU BITE
12	AUTOCAL Mode
11	Not used
10	" "
9	" "
8	" "
7	" "
6	" "
5	" "
4	C Word Format Error
3	B Word Format Error
2	Read Error, Accelerometer or S/D Register
1 (LSB)	Parity Fail on Input

When the system status is transferred to the computer, on demand, the 16 bit register is loaded into word D_{STATUS} for transmission.

The C Register is used primarily by the data bus terminal in the PIU. A format check (the two most significant bits must be zero) determines that a C word has indeed been transferred. In the IU, the register is recirculated during reads for a parity check. In the specification, the C word is not used at all in the peripheral device. It is merely received and returned as read. It appears in this system solely to meed the bus format requirement. (The C word Format appears in Figure 7-3.)

7.7 D_1 Register and IMU Commands

Data writes from the computer to the IU are in either the form BD_1C or BD_2C. B is the function word or address to be read into. D_1 is a word of IMU commands, while D_2 is a word of GYPTO commands.

The D_1 Register consists of "D" type flip-flops. That is, it does not reset if sequential commands are the same. IMU commands consist of discretes (e.g., modes, slew sense and slew on/off) and a single channel fail indicator reset command. These are tabulated in Table 7-5, D1 Register (IMU Commands). The contents of this register reflect the IMU command word (ICMAND) generated in the computer.

7.8 D_2 Register and GYPTO Commands

In the KT-70 IMU, the gyros are dithered with a 200 pps 1:1 binary torquing pattern. In its other applications, with a single unit mated directly to a dedicated computer, each torque pulse is commanded individually. In this system, a single computer services three IMUs using a data bus. Considering the requirements for nine gyro axes, command setup time in the computer, transfer time and the fact that the data bus presumably services other systems, it was felt that direct commands represented an intolerable burden.

Instead, CSDL has designed this system so that each IMU receives a single command containing torquing information for each axis 50 times/s. The torquing information is in ternary form, that is, net torque to be added to the binary pattern. Up to four net pulses may be commanded. It should be noted that, with a gyro torquing scale factor of 0.4$\widehat{sec}$/pulse, a continual command of + 1 pulse/transfer equals 20 $\widehat{sec}$/s, or 1.33 earth rate. Torquing commands, consequently, will virtually never exceed one pulse/update. The primary exception would be use of digital

TABLE 7-5. D_1 REGISTER (IMU COMMANDS)

Bit	Function (when true)
16	Grid Mode
15	Magnetic Slave Mode
14	Inertial Mode
13	Normal Mode
12	Ground Align Mode
11	Reset Fail Flip-flop
10	Reset Parity Fail Flip-flop
9	Computer Control
8	Computer Fail
7	Scale Factor High Gain
6	X Slew Sense Negative
5	X Slew Commanded
4	Y Slew Sense Negative
3	Y Slew Commanded
2	Z Slew Sense Negative
1(LSB)	Z Slew Commanded

torquing to realign the platform, when the binary mode would be overridden by continual one-sense commands.

The format of the command for one IMU is shown below. A sixteen bit data word (D2) carries four bits of torquing commands and a sign (torquing sense) bit for each axis (Figure 7-3, GYPTO Commands, D2 Word)): bits 1-4, X data, bit 5, X sign; bits 6-9, Y data, bit 10, Y sign; bits 11-14, Z data; bit 15, Z sign, bit 16 unused.

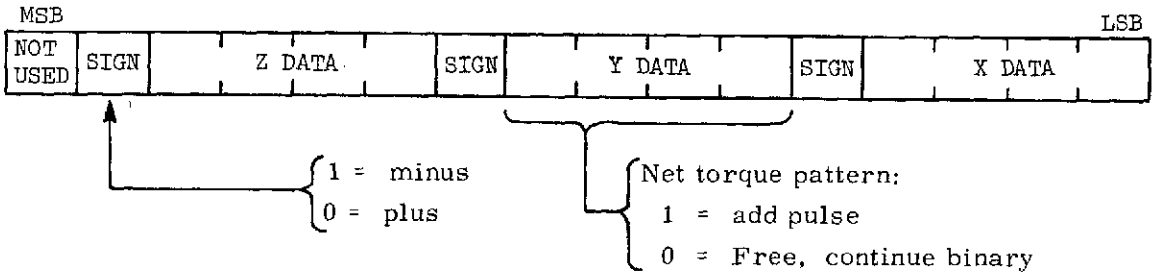


Figure 7-3. GYPTO Commands, D2 Word

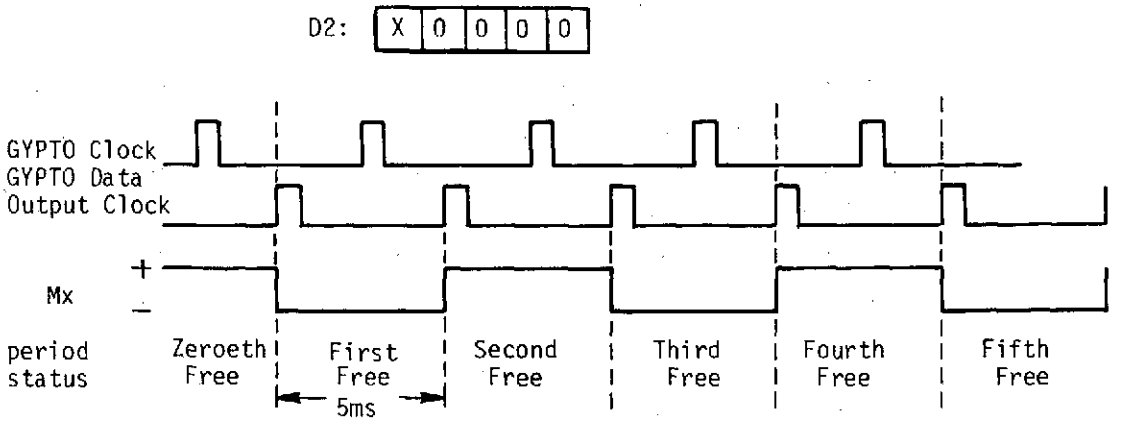
Note that the command is a four bit pulse pattern, not a four bit number of pulses. This permits a fine adjustment (0.4/200 $\widehat{sec}$/s$\sim$0.002°/hr) in compensation rates.

The command word is read into the corresponding 16 bit register (D2) in the IU, which is not automatically reset. Therefore, as long as the desired torque command for all three gyro axes is unchanged, no further GYPTO command need be sent to the IU.

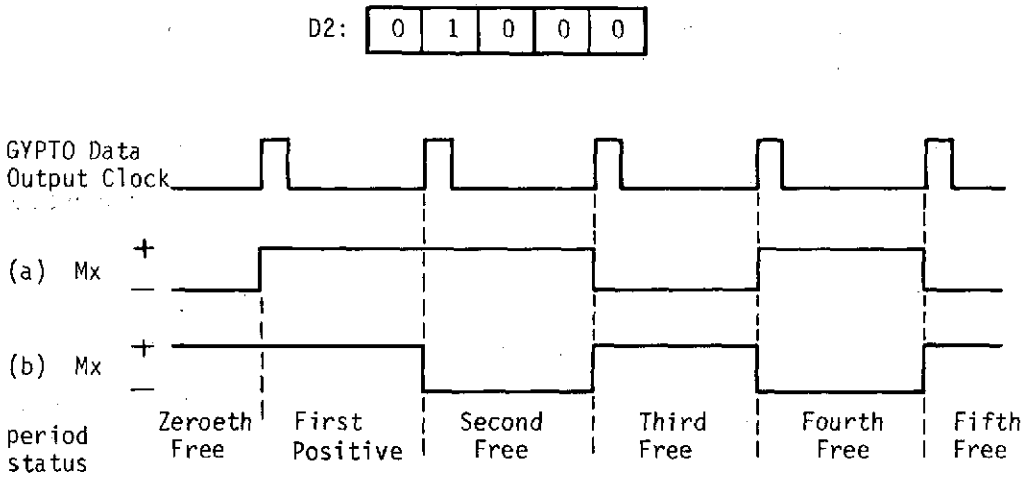
Hardware realization of the command is accomplished using a flipflop with memory of the last free (uncommanded) state. The GYPTO logic in the IU reads the D2 register and makes three torque sense decisions every 5 ms (synchronous with the GYPTO clock) these commands are strobed out to the IMU, every 5 ms, by the GYPTO data output clock. These two clocks are 5ms pulse to pulse trains, displaced by 2.5ms.

Several examples are now discussed (for a single gyro axis). The examples are illustrated in Figure 7-4, GYPTO Ternary- to- Binary Logic Examples.

1. No net torque commanded.



2. One net positive pulse on First period.



3. Net positive pulses First and Third period

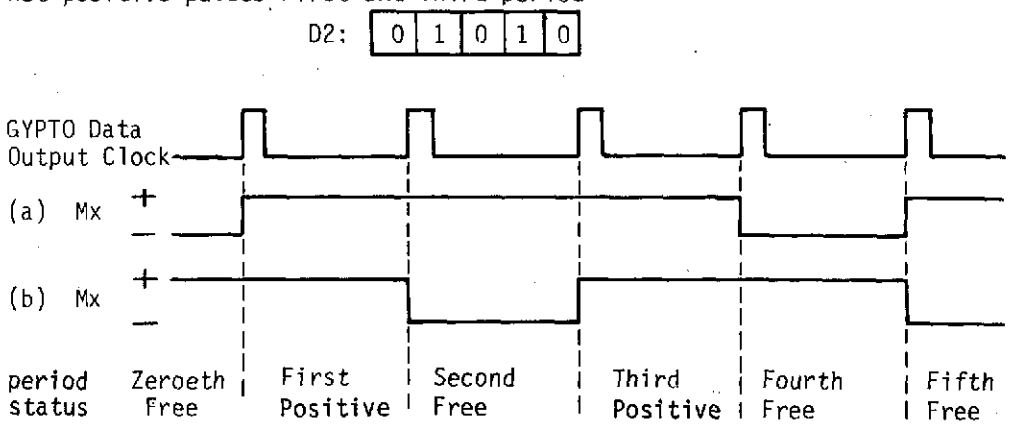


Figure 7-4. GYPTO Ternary-to-Binary Logic Examples.

1. With no net torque commanded, the sign bit is immaterial and binary pattern is not interupted.

2. A single positive pulse is required on the first decision, with (a) a negative free pulse beforehand and (b) a positive free pulse beforehand. The command is reset to zero at the following update: the common factor is that the binary mode is interupted by a positive pulse during the first 5ms. The flip-flop retains memory of the sense of the last free pulse, and resumes the binary mode with a pulse of the opposite sense.

3. Positive pulses are commanded in the first and third positions, again with (a) a negative and (b) a positive preceeding pulse. As shown, the command is reset to zero at the following update. Note that a continual use of this pattern corresponds to nearly + 3 earth rates compensation.

The GYPTO logic ensures the binary mode by alternating torquing sense of the free decision periods.

The logic just described, in practice in the multiple IMU system, has proven a viable alternative to direct compensated binary commands from the computer.

7.9 Accelerometer Output Processing; Registers D_{AX}, D_{AY}, D_{AZ}

Accelerometer output is in the form of CAPRI pulses. These represent quantized amounts of integrated analog rebalance current. The ΔV pulses are asynchronous, $13\mu s \pm 12\mu s$ long, and are instrument limited to a maximum rate of 10^4pps. Positive and negitive ΔV pulses appear as positive going pulses on separate lines.

Because this data is asynchronous, a separate clock sequence is generated for it (ACLK0 through ACLK3). A free running multivibrator is gated to provide this chain of $0.5\mu s$ pulses on four lines (see Figure 7-5, CAPRI Pulse Processing).

The processing of an input ΔV pulse is shown below. Pulse synchronizers are used to process the asynchronous incoming ΔV pulses. The up-down counters must be incremented and read out in synchronization if pulses are not to be lost.

The readout sequence is as follows. A request to update (RAU-) is received. At the next ACLK1 the request is accepted (last data if any was processed at ACLK0) and at ACLK2 the output shift registers are loaded. At ACLK3 the counter is cleared.

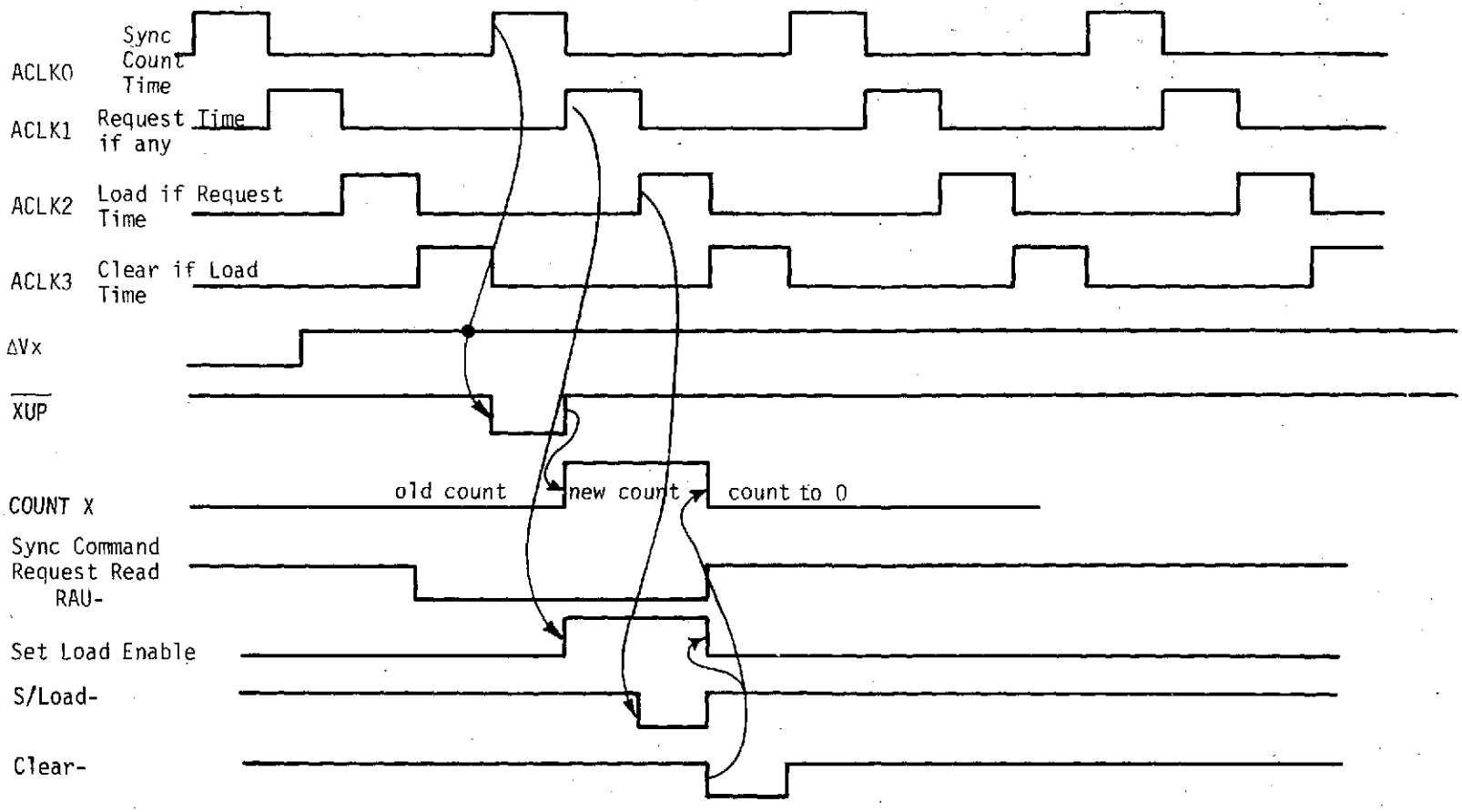


Figure 7-5. CAPRI Pulse Processing (Showing case of ΔVx pulse arriving near SYNC command (drop acc data))

If a new data (ΔV) arrived in this interval it would be counted at the following ACLK0 and no data would be lost. The actual reading of the data is done by a Read Accelerometers command issued in sequence to the three IUs. It will be noticed that processing an input ΔV pulse consumes at most 6.5μs, compared to typically 100 μ s pulse to pulse at maximum rate. Output of this gate is synchronous with counter gating.

Pulses are accumulated in the registers D_{AX},D_{AY},D_{AZ}. These are 12 bit up down counters. At maximum pulse rate (10^4 per second) and minimum algorithm update rate (5 per second), 2000 pulse storage is required. $2^{12} = 4096$.

When the counters are read, in response to the computer's demands, the contents of register D_i are loaded into the 12 low order bits of word D_i. The counters are right justified in the 16 bit data word. The counter cannot be read while it is being updated, guarding against loss of information. During reads, the data is recirculated in the shift register allowing recovery from single parity errors by rereading the data.

7.10 S/D Converters: Registers D_{SD1}, D_{SD2}, D_{SD3}

Off-the-shelf tracking S/D converters are employed in the IU. These are Transmagnetics, Inc. (Farmingdale, NY) Model 1623 EC1-01 14 bit binary converters, permitting 80 $\widehat{\text{sec}}$ resolution. They are updated 400 times/s, with an update of gimbal angle registers made on each even numbered minor cycle (25 times/s). (See Appendix B for technical information on the S/D converters.)

Output of the converters is stored in the appropriate register: pitch axis in D_{SD1}, roll axis in D_{SD2}, azimuth axis in D_{SD3}. When demanded, these registers are read into the shift registers left justified. The data word in the computer is a signed binary fraction representing the gimbal angle. Again, the data is recirculated enabling recovery from single parity errors.

If the system is retrofitted with multiple speed resolvers for the synchros, the S/D converters and their registers will be replaced. Resolver-to-digital converters will load two registers, a single speed register and multiple speed register. The S/D register read demand will instead call for the full six registers:

$$D_{P1X}\ D_{R1X}\ D_{AZ1X}\ D_{P8X}\ D_{R8X}\ D_{AZ8X}\ C$$

7.11 Accelerometer Counter Control, Update Timer, Bus Gating Time Generator

The accelerometer counters are required to deal with asynchronous pulses. Therefore, an unsynchronized, four stage clock is developed from a free runing multivibrator. The counters cannot be run off the Johnson counter as errors could result from dropping pulses while the counter is being reset by the external system sync signal. The accelerometer counter control provides an update request, an update ready flag and looks for read failures.

An update timer is included which provides timing signals for the S/D converter and accelerometer read routines. The timer is based on the 400Hz multivibrator which is reset by the 400Hz GYPTOclock (sync) line. A divide by 8 stage yields a 50pps train which is used to request S/D converter and status register updates. Accelerometer registers are filled from the up/down counters on command of the system sync message (5 times/s). These counters are reset to zero each time they are read.

A 9 bit Johnson counter is used to provide LTIME, DTIME and PTIME signals (shown in Figure 7-6, Bus Gating Times). This counter, which is reset by the external sync, has 18 states (0 to 17). A 1.8μs overall word is produced.

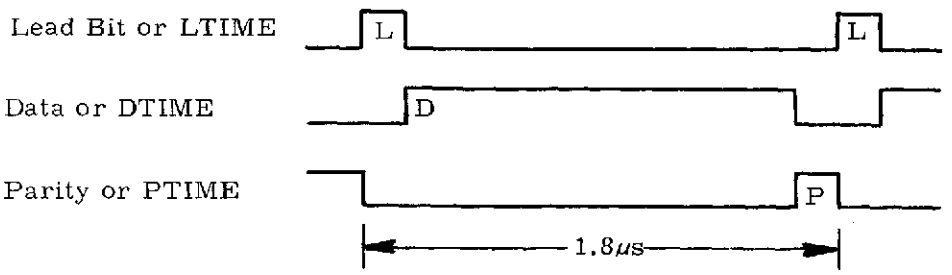


Figure 7-6. Bus Gating Times

These signals are used by the write control and input shift register.

8.0 POWER DISTRIBUTION SYSTEM

This chapter discusses the power distribution system for the redundant IMU system. Power requirements[1] of each unit are described. The power distribution panel (PDB) is presented. System power and ground trees are explained.

8.1 System Power Requirements

Multiple IMU System Power Requirements, Table 8-1, may be broken into three separate trees: SSCMS power, FOU power and power distribution panel (PDB) power,

The SSCMS is an integrated facility with its own power and ground trees tied into the laboratory power system. It is not part of, nor is it controlled in any way by, the multiple IMU system.

The FOU provides and controls power to the 4π-CP2, its auxiliary memory, their cooling units, the tape punch assembly, tape reader and the typewriter. It draws 220V 60 Hz 3 phase power. 115V 60 Hz single phase power is provided internally by an isolation transformer, and is used by DC supplies. It is also available at the FOU front panel (for the tape reader, as one example) and to drive a 115V 400Hz 3 phase motor generator. 400Hz power is used by most components of the computer complex.

All other system power is controlled and distributed by the PDB. Prime power is drawn in two forms: 115V 60 Hz 1 phase and 115V 400 Hz 3 phase. The 60 Hz power is used by an external 28 vdc supply whose output is routed back to the PDB for control and distribution.(The 60 Hz power is also used by the dedicated 5 VDC supply for the PIU, which is physically placed in the PDB.) Phase C of the 400Hz power is used to provide (by means of a transformer) 26V 400Hz phase C power for the synchros and S/D converters.

Specific power requirements have been shown in Table 8-1.

8.2 Power Distribution Panel

The PDB is a rack mounted power control and distribution "box" for the multiple IMU system. It is illustrated by marked photographs in Appendix E, PDB Mechanical Design.

TABLE 8-1. MULTIPLE IMU SYSTEM POWER REQUIREMENTS

Tree	Voltage	Maximum Power Reg.
SSCMS	NA[1]	NA
FOU	220V 60 Hz 3Ø	6 Kw/Ø Max.
PDB	115V 60 Hz 115V 400 Hz 3Ø	4.5 Kw max. 4.5 Kw/Ø max.
Unit	**Voltage**	**Steady State Power Reg.**
PDB	115V 60 Hz[2] 115V 400 Hz ØC	0.02 Kw Negligible
PIU	115V 60 Hz[3] 5 VDC	Negligible 0.02 Kw
IU	115V 60 Hz[4] 115V 400 Hz 3Ø 26V 400 Hz 28 VDC	0.02 Kw 0.1 Kw/Ø[5] 0.1 Kw 0.02 Kw

1) NA = Not Available
2) Power to 5VDC and 28VDC Supplies
3) Power to ±15 VDC Supply
4) Power to 5VDC, ±15 VDC Supplies
5) ØA and ØB: 0.5Kw/Ø during IMU warmup

Prime power is controlled by a ganged four pole breaker. Three poles (at 20 amp/pole) switch the three phase 400Hz power; the fourth (also 20 amp) switches the single phase 60Hz power. The three phases of 400Hz power are passed through hardwired ammeters. These four voltages are monitorable by front panel test points.

All power lines are carried through to terminal blocks (including the 26V 400Hz and 28vdc). Power signals need for each unit (IUs 1, 2, and 3 and the PIU) are drawn off individually, passed through front panel mounted indicating fuses, and brought to one pole of an output relay. There are four dedicated output relays, one for each device.

Output excitation power is doubly controlled. Primary control is exercised by an undervoltage/over voltage protection circuit which monitors these lines to stated tolerances:

115 v	400Hz	± 5 vac	(3 phases)
115 v	60Hz	± 5 vac	
26 v	400Hz	± 1 vac	
28 vdc		± 1 vdc	

Tolerances are set by resistor selection, with an adjustable resistor setting comparator reference voltage. Any out-of-tolerance condition, high or low, opens a control relay on the output relay excitation line. Secondary control is exercised through individual switches on each relay's line, permitting turning on any subset of the IUs.

The PDB also has a switchable ammeter which may be used to measure current on any of the four 115V lines to any selected IU.

8.3 System Ground Trees

The PDB also serves as the connecting point for the system ground trees. Five separate "grounds" are carried through the system. These are:

115 v 400Hz neutral
26 v 400Hz neutral
115 v 60Hz neutral
DC ground
System (chassis) ground

The 115V 400Hz neutral terminal in the PDB is taken as the system ground point, and both DC and chassis grounds are tied to it. 115V 60Hz neutral is carried separately, and is presumed to be tied to the 400Hz neutral at a common building ground at the 400Hz generator. 26VAC is transformer isolated from 115V 400Hz, and its neutral is not carried through to a ground point.

9.0 SUMMARY

The laboratory demonstration multiple IMU system described in this report has been designed to function as a primary tool in evaluating redundant inertial technology. With the system software (documented in Volume III of this report, Multiple IMU System Software Design and Coding) and proposed test plan (Volume IV, Multiple IMU System Test Plan), a broad range of studies may be carried out.

There are two areas of new technology utilized in this system. In the hardware area, use of a data bus for communication with and control of redundant IMUs has been demonstrated. Bus design and coding are similar to those baselined for the space shuttle orbiter. In software, one requirement new to gimballed inertial systems has been shown practical: failure detection and isolation. Its impact on hardware has been an additional requirement for system reconfiguration following isolation.

The system delivered under this contract is expected to operate as a proving ground for new software until laboratory systems of actual shuttle hardware are available. Its potential for more advanced work, with retrofitted hardware and additional software, suggests that its work has just begun.

APPENDIX A

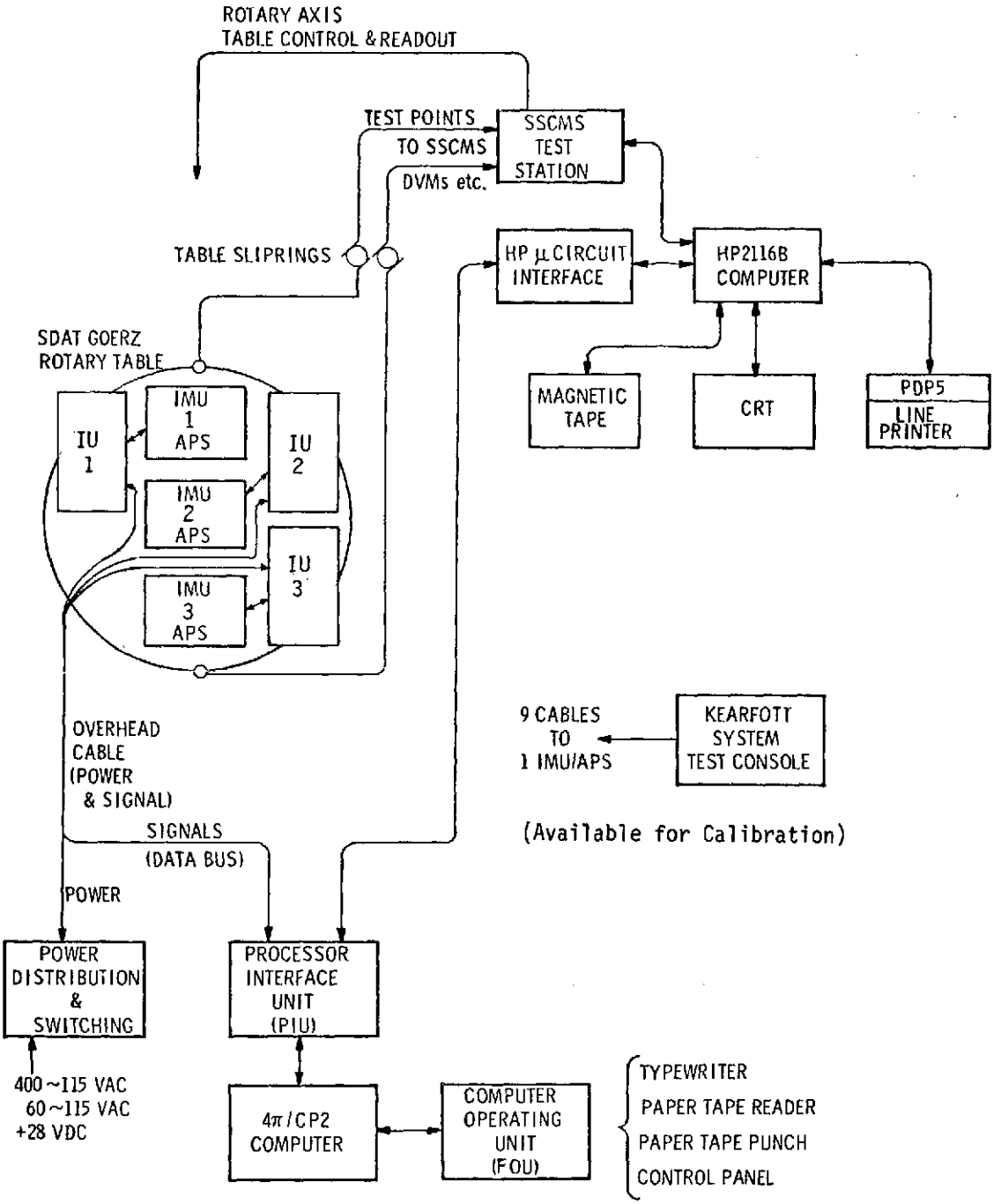
SYSTEM MECHANIZATION DRAWINGS

One line mechanization drawings of the redundant IMU system appear in this appendix.

Figure A-1, Test Configuration, illustrates the complete system including the test Facility.

Figure A-2 is a PIU Functional Drawing.

Figure A-3 is an IU Functional Drawing.



IU - CONTAINS POWER SUPPLIES, SYNCHRO/DIGITAL CONVERTERS, TEST POINTS

IMU/APS - ADAPTER POWER SUPPLY AND IMU

Figure A-1. System Test Configuration.

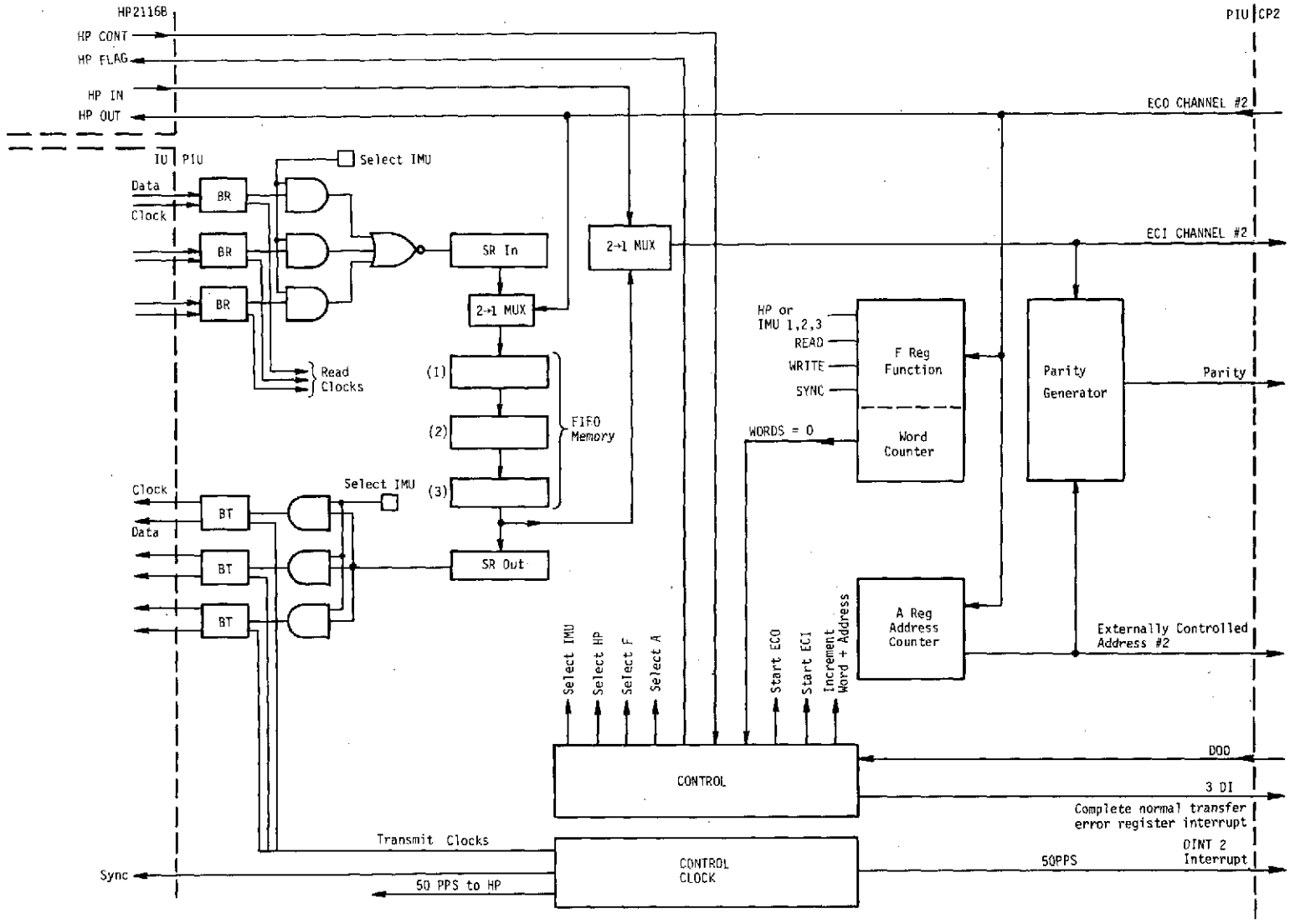


Figure A-2. PIU Functional Drawing.

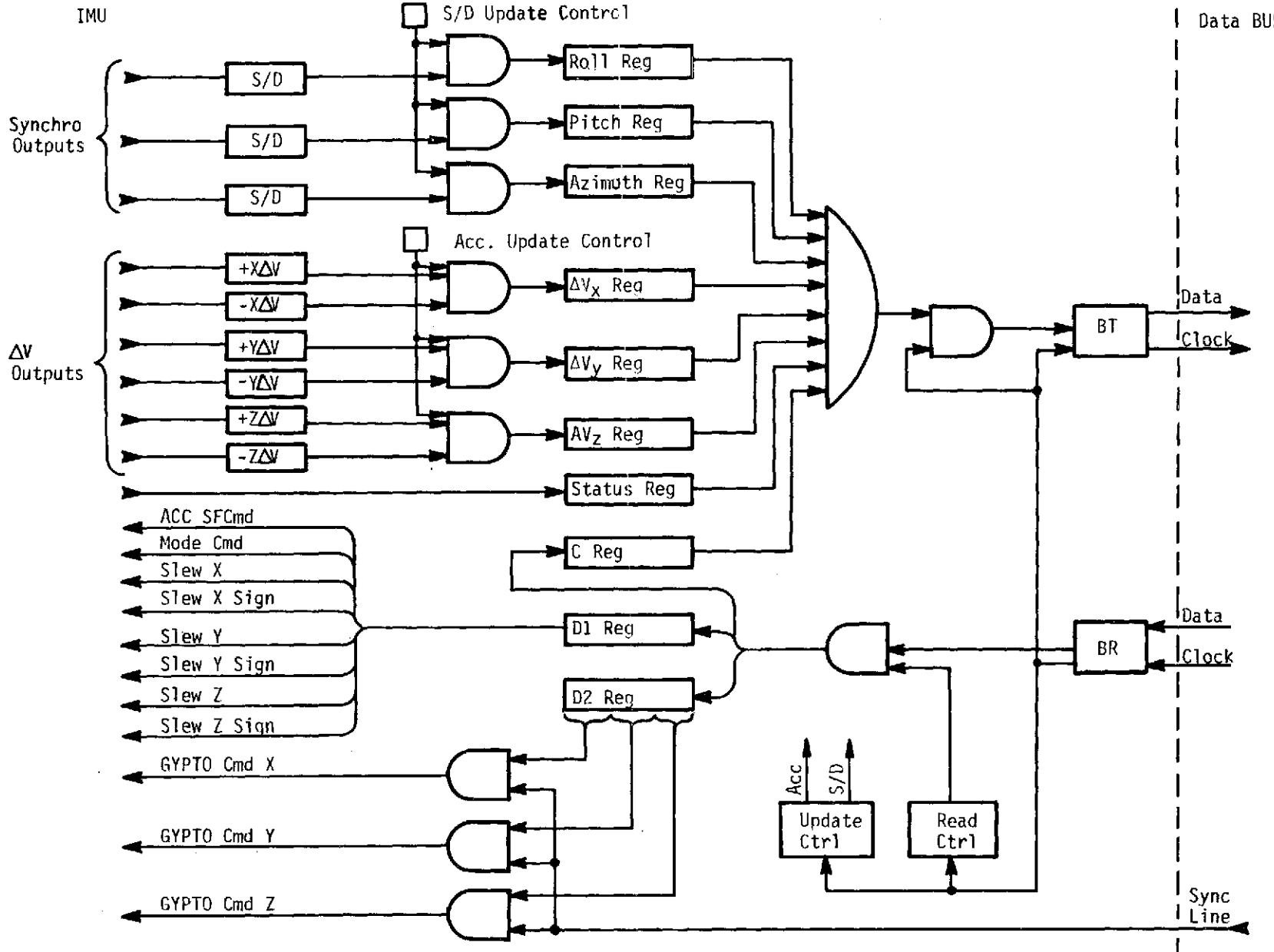


Figure A-3. IV Functional Drawing.

APPENDIX B

PIU MECHANICAL DESIGN

The function of the PIU has been described in Chapter 5. This appendix shows its structure, lists integrated circuits used by board location and lists connectors used in the PIU.

B.1 PIU Mechanical Layout

Figure B-1, PIU Layout, shows the connectors and interior of the unit. Not shown in the photo is the ABORT switch, which is located on the FOU.

B.2 Integrated Circuit Assignments

Figures B-2 and B-3 show the W and X Board Layout, respectively, as seen from the top. All ICs are Texas Instrument 7400 series TTL or their equivalent.

B.3 Connector List

Number	Connector	Function
PJ1	ITT Cannon DE9P	PIU Power
PJ2	" " DA15S	Data Bus, IMU1
PJ3	" " "	" ", IMU2
PJ4	" " "	" ", IMU3
PJ5	" " 2DC79S	HP 2116B Interface
PJ6	" " 2DE19S	4π-CP2 Interface
PJ7	" " 2DD100S	" "
PJ8	BNC	SSCMS Sync Pulse

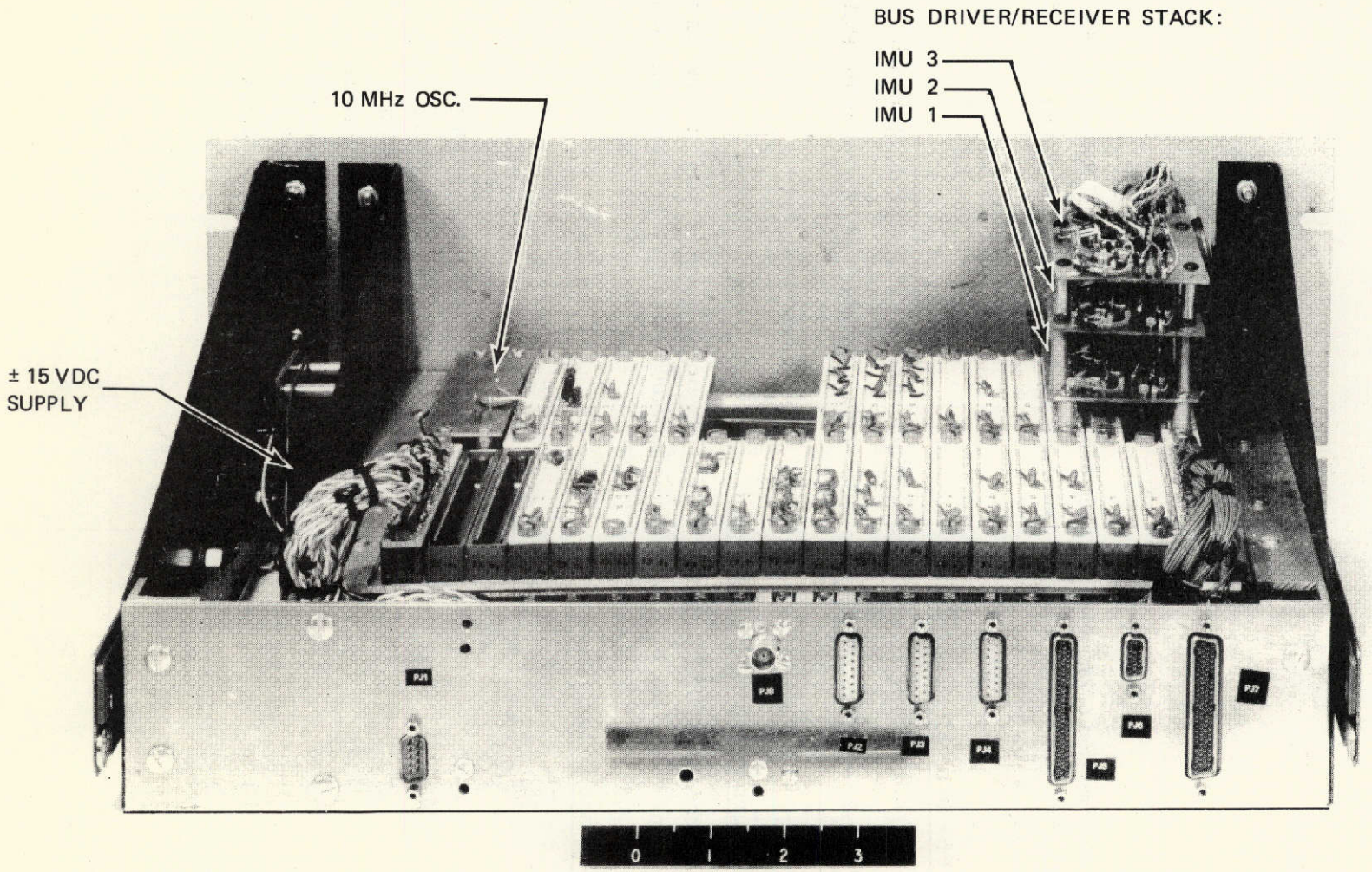


Figure B-1. PIU Layout

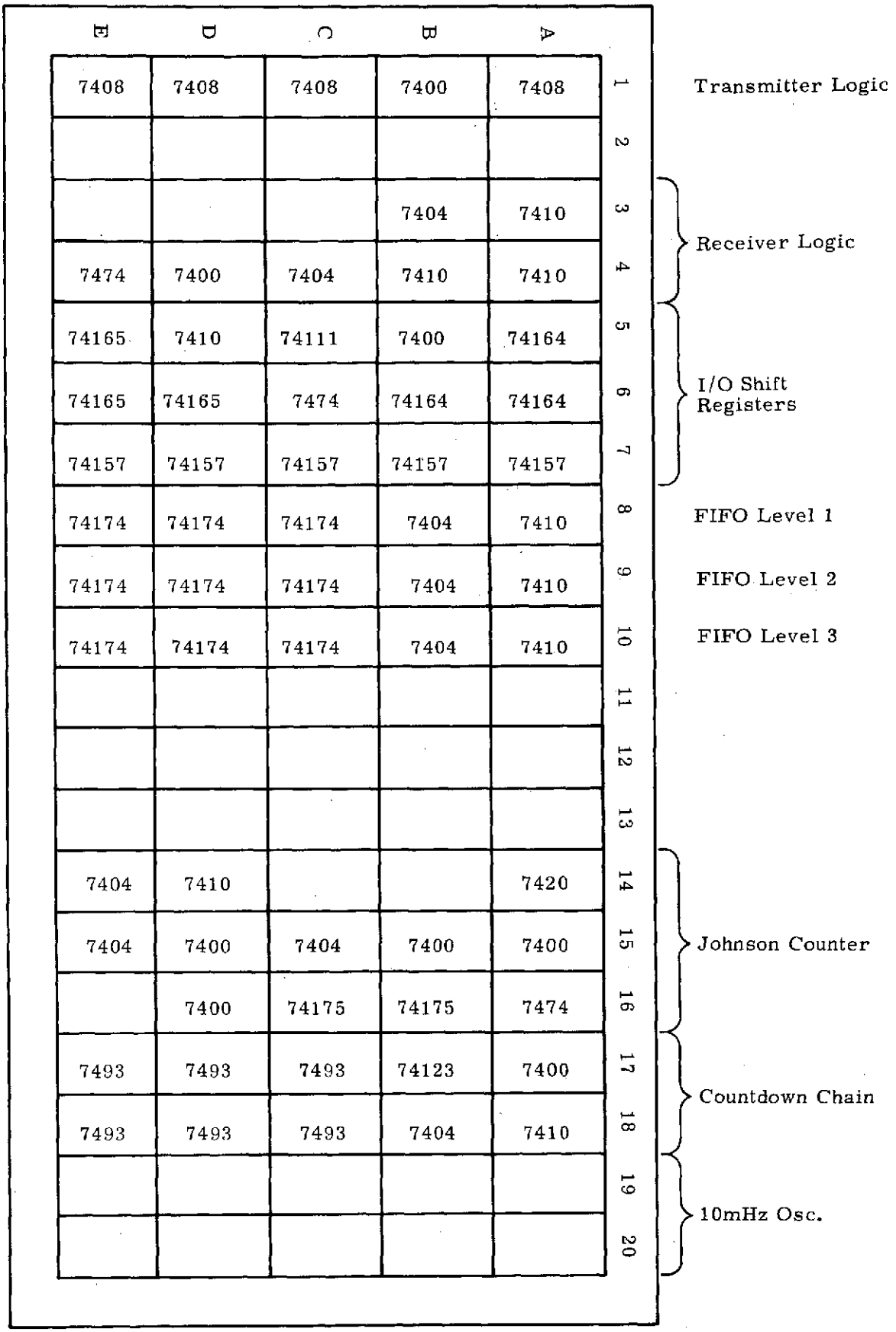
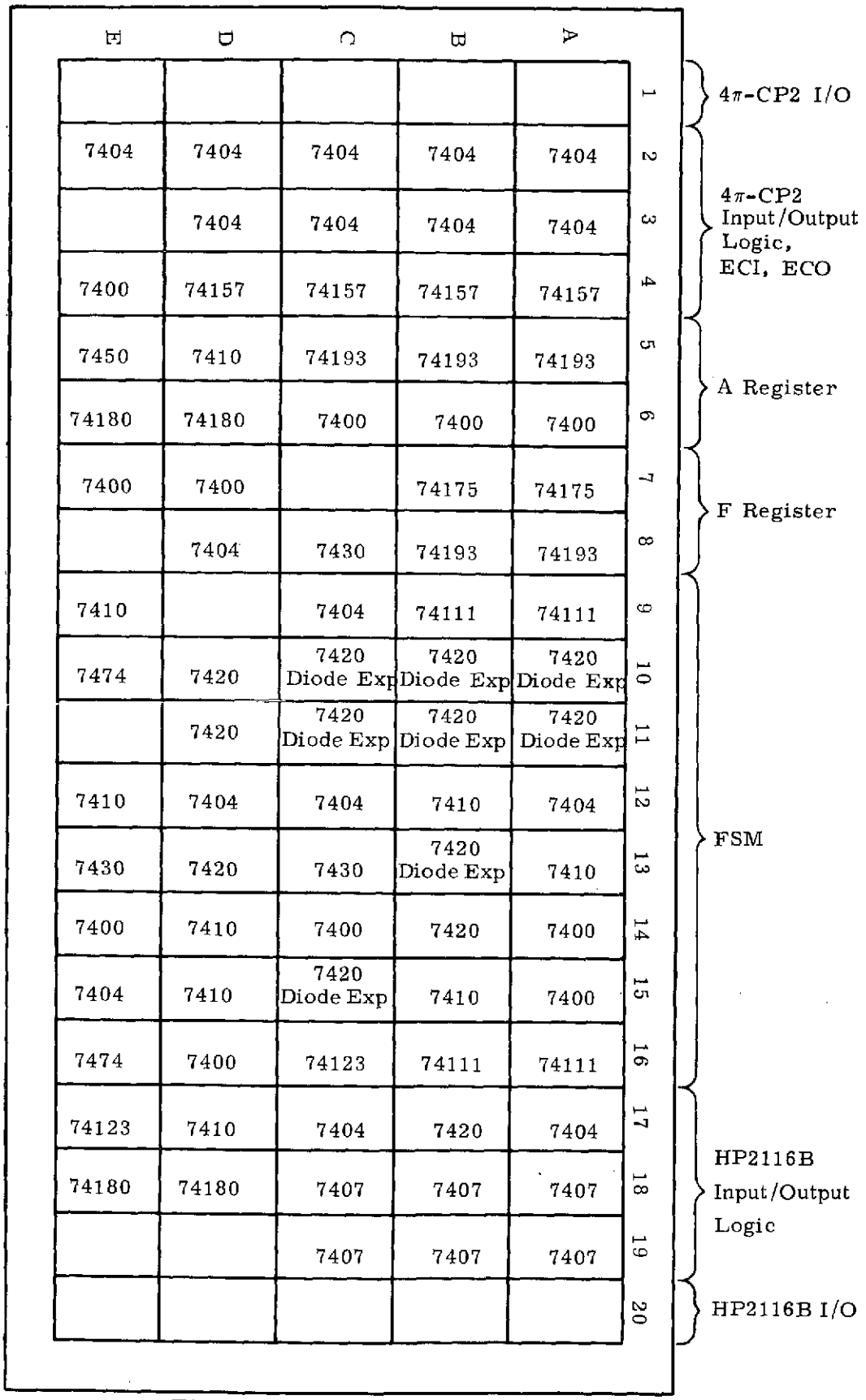


Figure B-2. W Board Layout



E	D	C	B	A	
					1
7404	7404	7404	7404	7404	2
	7404	7404	7404	7404	3
7400	74157	74157	74157	74157	4
7450	7410	74193	74193	74193	5
74180	74180	7400	7400	7400	6
7400	7400		74175	74175	7
	7404	7430	74193	74193	8
7410		7404	74111	74111	9
7474	7420	7420 Diode Exp	7420 Diode Exp	7420 Diode Exp	10
	7420	7420 Diode Exp	7420 Diode Exp	7420 Diode Exp	11
7410	7404	7404	7410	7404	12
7430	7420	7430	7420 Diode Exp	7410	13
7400	7410	7400	7420	7400	14
7404	7410	7420 Diode Exp	7410	7400	15
7474	7400	74123	74111	74111	16
74123	7410	7404	7420	7404	17
74180	74180	7407	7407	7407	18
		7407	7407	7407	19
					20

Figure B-3. X Board Layout

APPENDIX C

IU MECHANICAL DESIGN

The function of the IU has been described in Chapter 7. This appendix shows its structure, lists integrated circuits used by board location and lists connectors used in the IU.

C.1 IU Mechanical Layout

Figures C-1 and C-2 show the IU Front Panel and IU Rear Panel, respectively. Figure C-3 shows IU Interior.

The IU front panel carries connectors UJ1 through UJ10 and UJ13. Four indicator lights show the IMS Fail, IMS Fault, IMU BITE and System Ready bits of the status register (lit when set). Additionally, the IMS fail switch appears. The hole in the IU's side permits access to the voltage adjustment screw of the 5VDC supply.

On the rear panel, there are mounted connectors UJ11 and UJ12, and fuses for the 115 V 60 Hz and 5 VDC lines.

The illustration of the IU interior layout does not clearly show the bus receiver and transmitter, located on the far side of the Z and Y boards, respectively. Also not shown (but mounted on the side panel beside the 5 VDC supply) are the DC terminal strip and the lamp drivers. A synchro follower termination board is also mounted there.

C.2 Integrated Circuit Assignments

The Figures C-4 and C-5 show the Y and Z Board Layout, respectively, as seen from the top. All ICs are Texas Instrument 7400 series TTL or their equivalent, with the exception of a single Signetics 8270 Four Bit Shift Register.

Also shown are the locations of the bus receiver and transmitter.

C.3 Connector List

Number	Connector	Function
UJ01	ITT Cannon 2DB52S	IMU I/O
UJ02	" " "	IMU/APS Signals
UJ03	" " "	IMU Power
UJ04	" " 2DB52P	IMU Power
UJ05	" " 2DB52S	IMU/APS Signals
UJ06	" " "	APS Moding Commands
UJ07	" " "	APS Moding Commands
UJ08	" " "	A/C Systems Data
UJ09	" " 2DE19S	System Power
UJ10	" " 2DB52S	Analog Signal Test Points
UJ11	Bendix MS3102A-28-18P	IU/IMU/APS Power
UJ12	ITT Cannon DA15S	Data Bus
UJ13	" " 2DB52S	Gimbal Angle Display

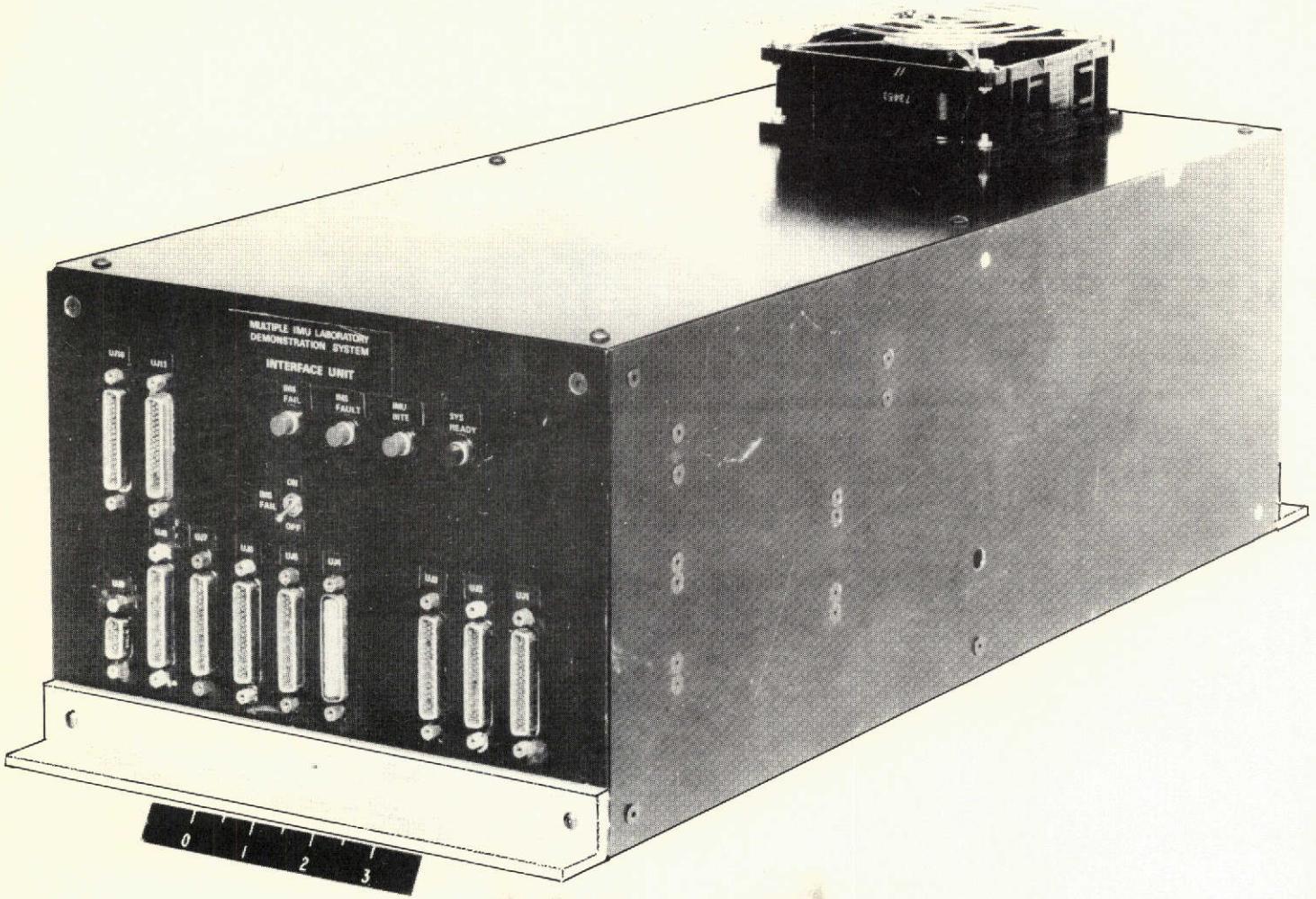


Figure C-1. IU Front Panel

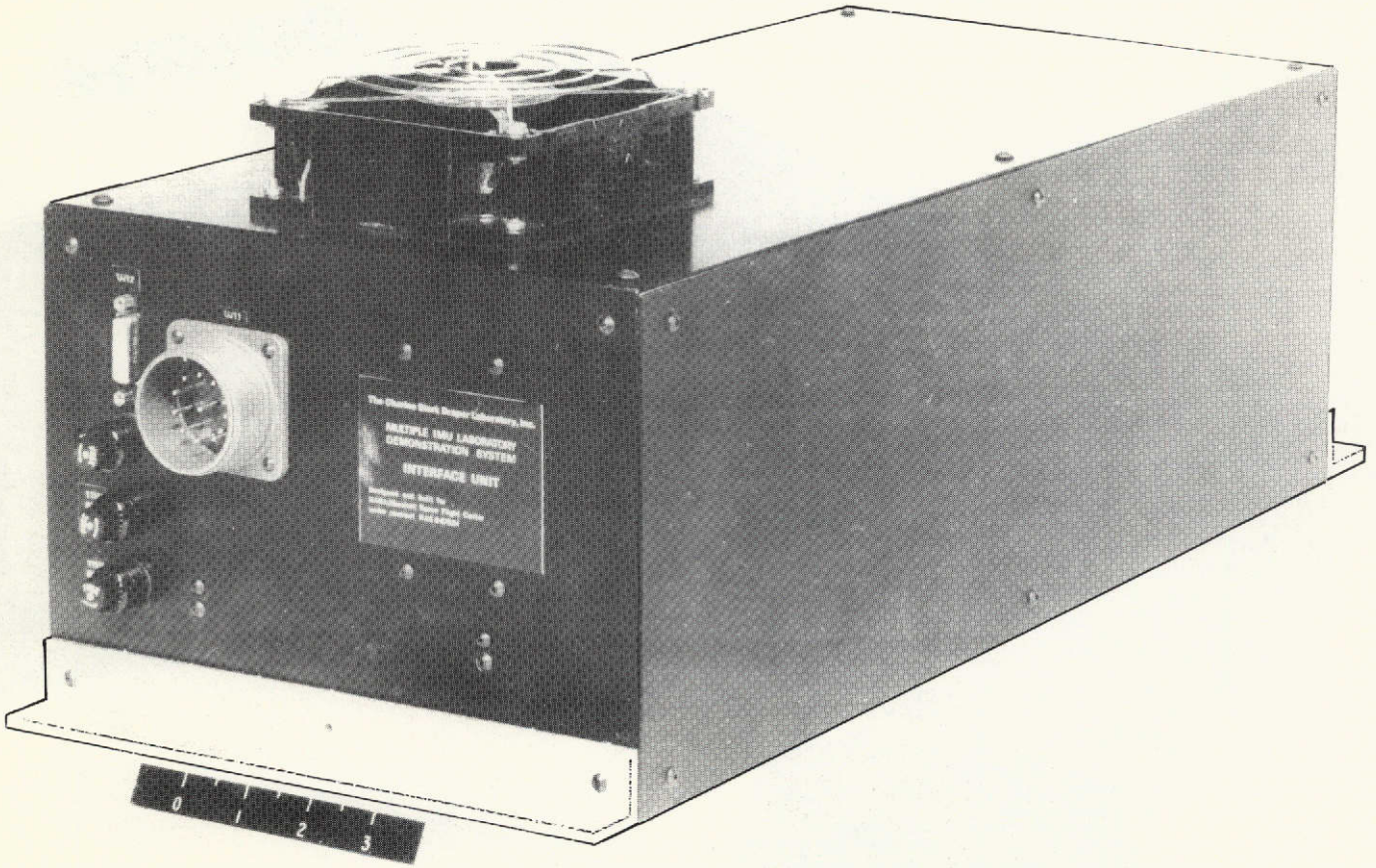


Figure C-2. IU Rear Panel

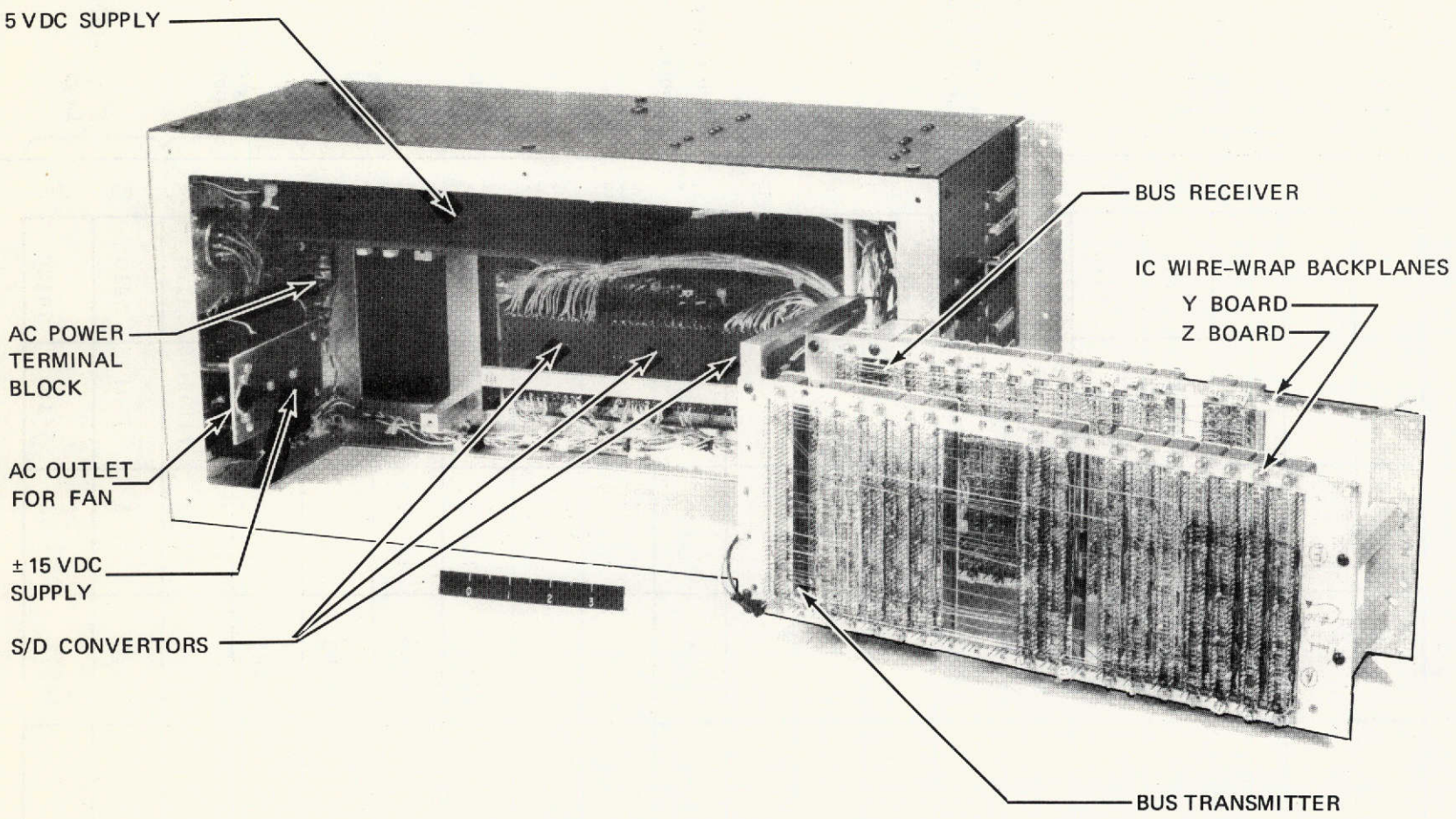
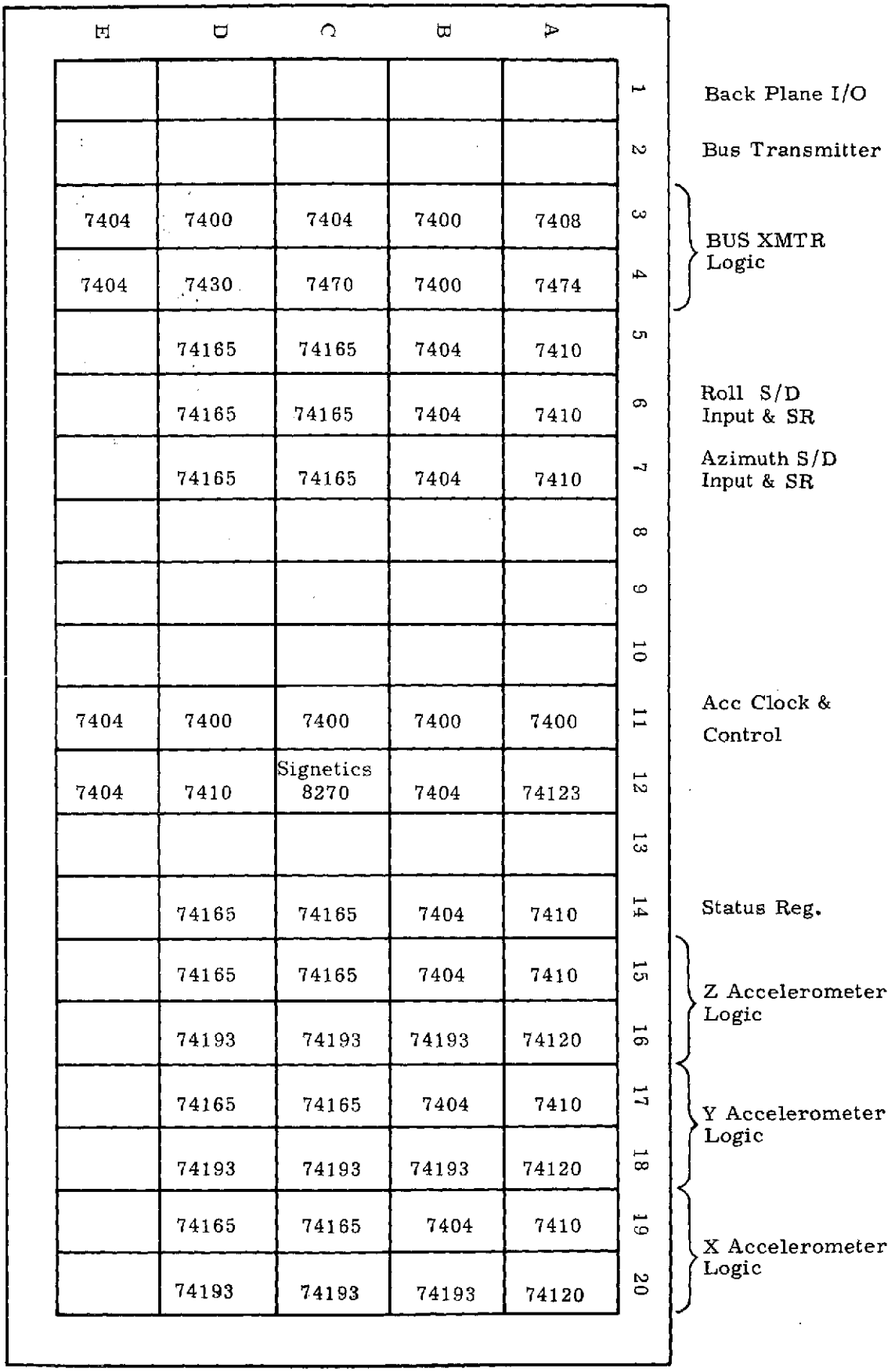


Figure C-3. IU Interior



	E	D	C	B	A		
						1	Back Plane I/O
						2	Bus Transmitter
	7404	7400	7404	7400	7408	3	BUS XMTR Logic
	7404	7430	7470	7400	7474	4	
		74165	74165	7404	7410	5	
		74165	74165	7404	7410	6	Roll S/D Input & SR
		74165	74165	7404	7410	7	Azimuth S/D Input & SR
						8	
						9	
						10	
	7404	7400	7400	7400	7400	11	Acc Clock & Control
	7404	7410	Signetics 8270	7404	74123	12	
						13	
		74165	74165	7404	7410	14	Status Reg.
		74165	74165	7404	7410	15	Z Accelerometer Logic
		74193	74193	74193	74120	16	
		74165	74165	7404	7410	17	Y Accelerometer Logic
		74193	74193	74193	74120	18	
		74165	74165	7404	7410	19	X Accelerometer Logic
		74193	74193	74193	74120	20	

Figure C-4. Y Board Layout

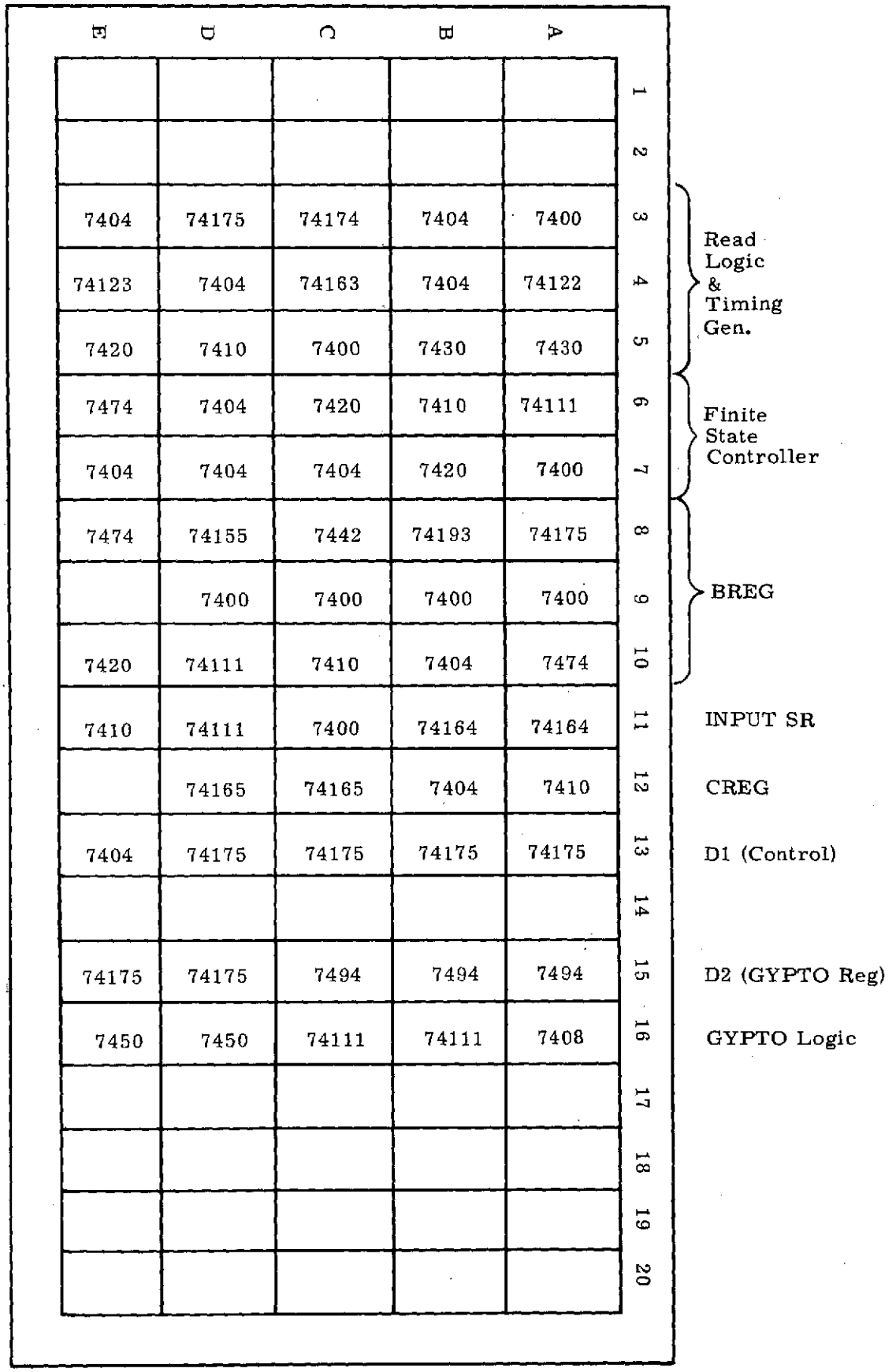


Figure C-5. Z Board Layout

APPENDIX D

SYNCHRO TO DIGITAL CONVERTER

Transmagnetics, Inc., Model 1623EC1-01 synchro-to-digital converters have been employed in this system. The manufacturer's specification is presented in this appendix.

TRANSMAGNETICS

SERIES 1623E 1633E

Revised June 1974

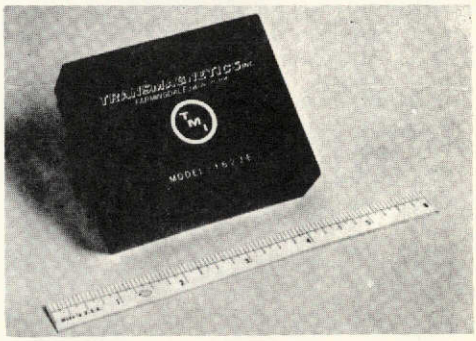
miniature
14 BIT SYNCHRO or RESOLVER TO DIGITAL CONVERTERS

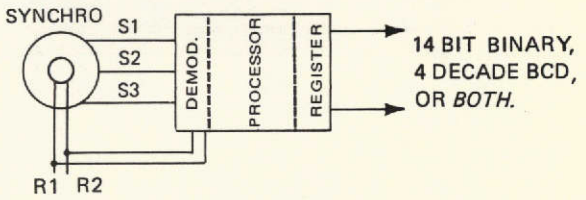
Models 1623E and 1633E are new miniaturized all solid state units that convert 3 wire synchro or 4 wire resolver inputs into binary or BCD outputs. These low cost converters offer high resolution and high accuracy over the temperature range of −55°C to +85°C making these converters desirable for both military and commercial applications. All units have the input transformers packaged internally.

Computer interfacing is easily accomplished because both "Conversion" and "Update" can be externally controlled.

Model 1633E, identical to Model 1623E except for the elimination of the demodulators, requires DC inputs of 10 sin θ and 10 cos θ and has an input impedance of 100K ohms. Among other applications this module is used with TMI multiplexing systems.

Mil Spec and hermetically sealed units are available.





SPECIFICATIONS:

Accuracy: ±4 minutes for parallel output
±0.1° for 4 decade BCD output

Resolution: ±1.318 minutes

DIGITAL DATA OUTPUT CHARACTERISTICS

Code 1: 14 BIT, PARALLEL BINARY OUTPUTS (TTL and DTL compatible.) 10 TTL loads
False (0) = 0 to 0.4 Volts, 16 mA current source
True (1) = +3 to +5 Volts, 400 μA current sink.

Code 2: 4 DECADE BCD (TTL and DTL compatible.) 10 TTL loads
0-359.9°, ±179.9°, 0-999 etc. available
False (0) = 0 to +0.4 Volts, 16 mA current source
True (1) = +3 to +5 Volts, 400 μA current sink.

Code 12: 14 BIT, PARALLEL BINARY *AND* 4 DECADE BCD OUTPUT

On Special Request TMI Will Supply as Model 1624
False (1) = +3 to +5 Volts, 400 μA current sink.
True (0) = 0 to 0.4 Volts, 16 mA current source

SPECIFICATIONS:

Input Code	Input	*Frequency ±5%	Ref. VRMS ±10%	L-L VRMS	L-L IMPED. Min.	Ref. Current (MA)
01:	Synchro	400HZ	26	11.8	50K	30
02:	Synchro	400HZ	115	90	100K	15
03:	Synchro	50/60HZ	115	90	40K	15
05:	Resolver	400HZ	26	11.8	40K	30
07:	Resolver	400HZ	115	11.8	40K	15
09:	Flux Valve	400HZ	26	>1	40K	30
10:	Synchro	50/60HZ	6.3	2.4	40K	30
11:	Synchro	400HZ	115	11.8	40K	15
13:	Resolver	1000HZ	9.0	4.5	40K	30
14:	Synchro	10KHZ	26	11.8	40K	30

*Distortion should not exceed 2%

DYNAMIC RESPONSE:

Units will track input up to 2400°/sec.
400 Hz units will have a lag of 40 sec./rpm maximum.
50/60 Hz units will have a lag of 60 sec./rpm maximum.
Dynamic lag is defined as the delay introduced by the converter that causes the indicated output to lag the input.

ISOLATION:

AC reference and line-to-line inputs are transformer isolated from each other and from D.C. power common. Insulation resistance from any AC input to output is greater than 100 megohms at 200 VDC.

CONVERSION RATE:

Standard: 400/second. Can be factory set to as low as one/3 second.
Special: 800/second. Can be factory set to as low as 1/second.

CONVERSION MODES:

Internal Convert:
Code 1 & 2: Connect pins 21 & 22.
Code 12: Connect pins 28 & 29.

External Convert:
Code 1 & 2: Feed External Command into pin 22 (pin 21 open).
Code 12: Feed External Command into pin 29 (pin 28 open).
This should be a TTL level, positive going pulse, of 250 nanoseconds minimum pulse width. For wider pulse widths a 5 microsecond rise time should not be exceeded. Rates may vary from 0 to 400 pulses per second. When conversion is completed a "Data Ready" pulse appears.

DATA READY PULSE:

(Pin 27 for Codes 1 and 2) (Pin 34 for Code 12) This pulse indicates that conversion is completed and has the following characteristics.
Pulse Level: (1) = +3 to +5 Volts, 400 μA current sink
(0) = 0 to 0.4 V, 16 mA current source.
Pulse Width: 15 microseconds, +5 μsec., −0 μsec.

Output information should be read upon receipt of leading edge of "Data Ready Pulse" and before next conversion has started.

UPDATE MODES:

Internal Update: Connect (Pins 27 and 28 for Codes 1 and 2) (Pins 34 and 35 for Code 12)
External Update: Feed External Command signal into (pin 28, 27 open for Codes 1 and 2) (pin 35, 34 open for Code 12). The External Command signal should be a positive pulse, TTL level, 250 nanoseconds width minimum. The output register will update within 20 nanoseconds of the leading edge and the register will hold data until the next Update Command is received.

POWER REQUIREMENTS: +5 VDC, ±5% at 320 mA max.
±15 VDC, ±5% at 30 mA max.

OPERATING TEMPERATURE: Model C: 0°C to +70°C
Model M: -55°C to +85°C

STORAGE TEMPERATURE: -65°C to +125°C

WEIGHT: CODE 1 and 2: Approximately 6 Oz
CODE 12: Approximately 10 Oz

PART NUMBER DESIGNATION

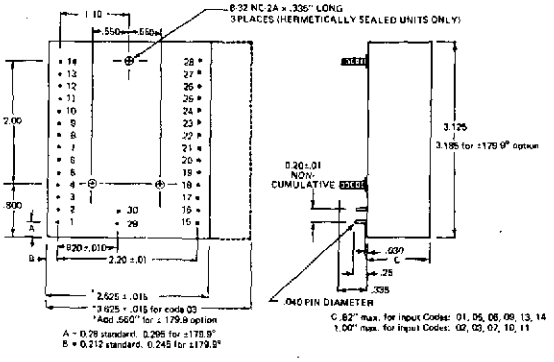
1623E or 1633E / 1624 or 1634 — X X-X X-XXXX

- 0-359.9, ±179.9, 0-9999
- For Hermetic Seal add "H"
- Inputs (01 thru 14)
- Output (Code 1, 2 or 12)
- Temperature Range (C or M)

VARIATIONS TO SPECIFICATIONS ON REQUEST

APPLICATION NOTES

It is desirable to have one Reference phase and one Stator phase connected to DC ground. If your system has free floating AC & DC grounds make certain that grounding is done after all voltages are disconnected or the converter may be damaged because of the potential difference between the two grounds.



Model 1623E, 1624E
14 BIT, PARALLEL BINARY OUTPUT

1	MSB	15	R_1 (LO)
2		16	R_1 (HI)
3		17	+5 VDC
4		18	−15 VDC
5		19	GND
6		20	+15 VDC
7	BINARY	21	INT. CONV.
8	OUTPUTS	22	EXT. CONV.
9		23	S_1
10		24	S_2
11		25	S_4
12		26	S_8
13		27	DATA READY
14	LSB	28	EXT. UPDATE

Model 1623E, 1624E
4 DECADE BCD

1	2 DECADE 4	16	R_1 (HI)
2	1	17	+5 VDC
3	8	18	−15VDC
4	4 DECADE 3	19	GND
5	2	20	+15 VDC
6	1	21	INT. CONV.
7	R	22	EXT. CONV.
8	4 DECADE 2	23	S_1
9	2	24	S_2
10	1	25	S_4
11	8	26	S_8
12	4 DECADE 1	27	DATA READY
13	2	28	EXT. UPDATE
14	1	* 29	8 DECADE 4
15	R_1 (LO)	* 30	4 DECADE 4

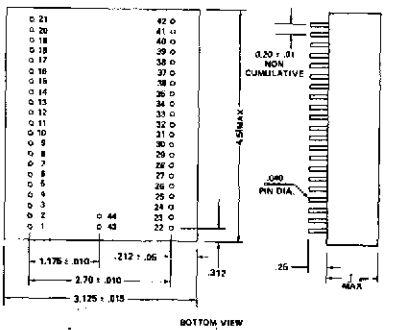
Model 1633E, 1634E
14 BIT, PARALLEL BINARY OUTPUT

1	MSB	15	NC
2		16	NC
3		17	+5 VDC
4		18	−15 VDC
5		19	GND
6		20	+15 VDC
7	BINARY	21	INT. CONV.
8	OUTPUTS	22	EXT. CONV.
9		23	10 sin θ
10		24	10 cos θ
11		25	NC
12		26	NC
13		27	DATA READY
14	LSB	28	EXT. UPDATE

Model 1633E, 1634E
4 DECADE BCD

* 1	2 DECADE 4	16	NC
2	1	17	+5 VDC
3	8	18	−15 VDC
4	4 DECADE 3	19	GND
5	2	20	+15 VDC
6	1	21	INT. CONV.
7	8	22	EXT. CONV.
8	4 DECADE 2	23	10 sin θ
9	2	24	10 cos θ
10	1	25	NC
11	8	26	NC
12	4 DECADE 1	27	DATA READY
13	2	28	EXT. UPDATE
14	1	* 29	8
15	NC	* 30	4 DECADE 4

*For ±179.9° models. Pin 1 NC, pin 29 becomes minus sign, pin 30 becomes plus sign.



1623E Code 12:
14 BIT, PARALLEL BINARY AND 4 DECADE BCD OUTPUT

1	MSB	15	1
2		16	2 DECADE 1
3		17	4
4		18	8
5		19	1
6		20	2 DECADE 2
7	BINARY	21	4
8	OUTPUTS	22	R_1 (LO)
9		23	R_1 (HI)
10		24	+5 VDC
11		25	−15 VDC
12		26	GND
13		27	+15 VDC
14	LSB	28	INT. CONV.
		29	EXT. CONV.
		30	S_1
		31	S_2
		32	S_4
		33	S_8
		34	DATA READY
		35	EXT. UPDATE
		36	2 DECADE 4
		37	1
		38	8
		39	4 DECADE 3
		40	2
		41	1
		42	8 DECADE 2
		43	NC
		44	NC

ALL DIMENSIONS IN INCHES

TRANSMAGNETICS, INC.
210 ADAMS BOULEVARD, FARMINGDALE, NEW YORK 11735
PHONE NO: 516 293-3100 TWX510-224-6420

Printed in USA
1173/1000

APPENDIX E

PDB MECHANICAL DESIGN

The function of the PDB has been described in Chapter 8. This appendix shows its structure and lists the connectors used.

E.1 PDB Mechanical Layout

The PDB is a rack mounted panel, fourteen inches high. Figure E-1, PDB Front Panel, and Figure E-2, PDB Rear View, show its structure.

Not shown (in Figure E-1) are the individual IU Output relay excitation switches, added after these photos were taken. Output relays and monitor pickoff transformers are mounted under the classis, and are not visible. The 28VDC supply its a separate, commercial, rack mounted unit, and is also not shown.

E.2 Connector List

Number	Connector	Function
WJ1	Bendix MS3102A-28-18S	IU1 Power
WJ2	" "	IU2 Power
WJ3	" "	IU3 Power
WJ4	ITT Canon DE-9S	PIU Power
WJ5	Amphenol 160-2	Input from 28VDC Supply
WJ6	Jones S304CCT	115V 60Hz to 28VDC Supply
WJ7	Hubbell 3434NCL	115V 400Hz Prime Power
WJ8	Amphenol 160-5	115V 60Hz Prime Power

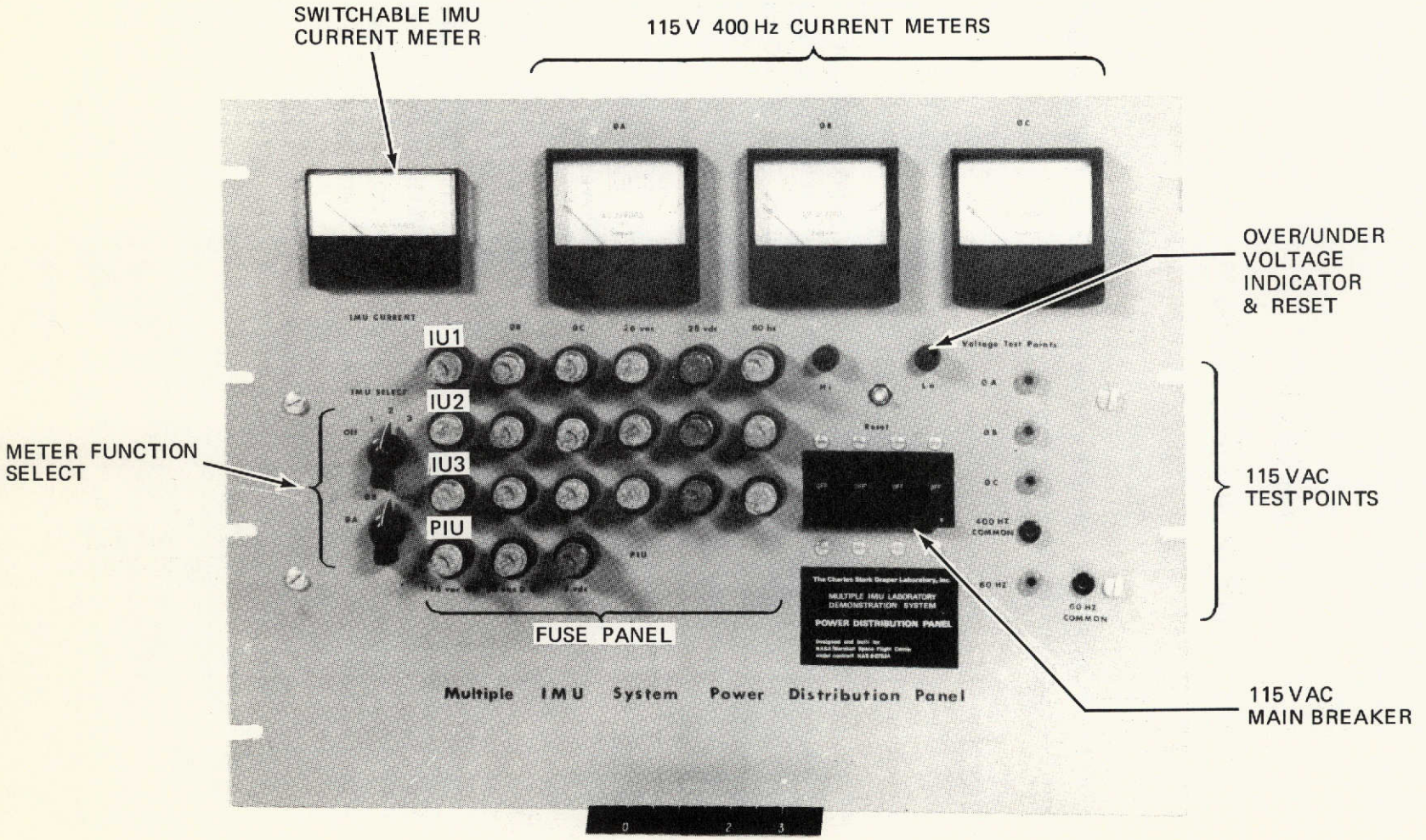


Figure E-1. PDB Front Panel

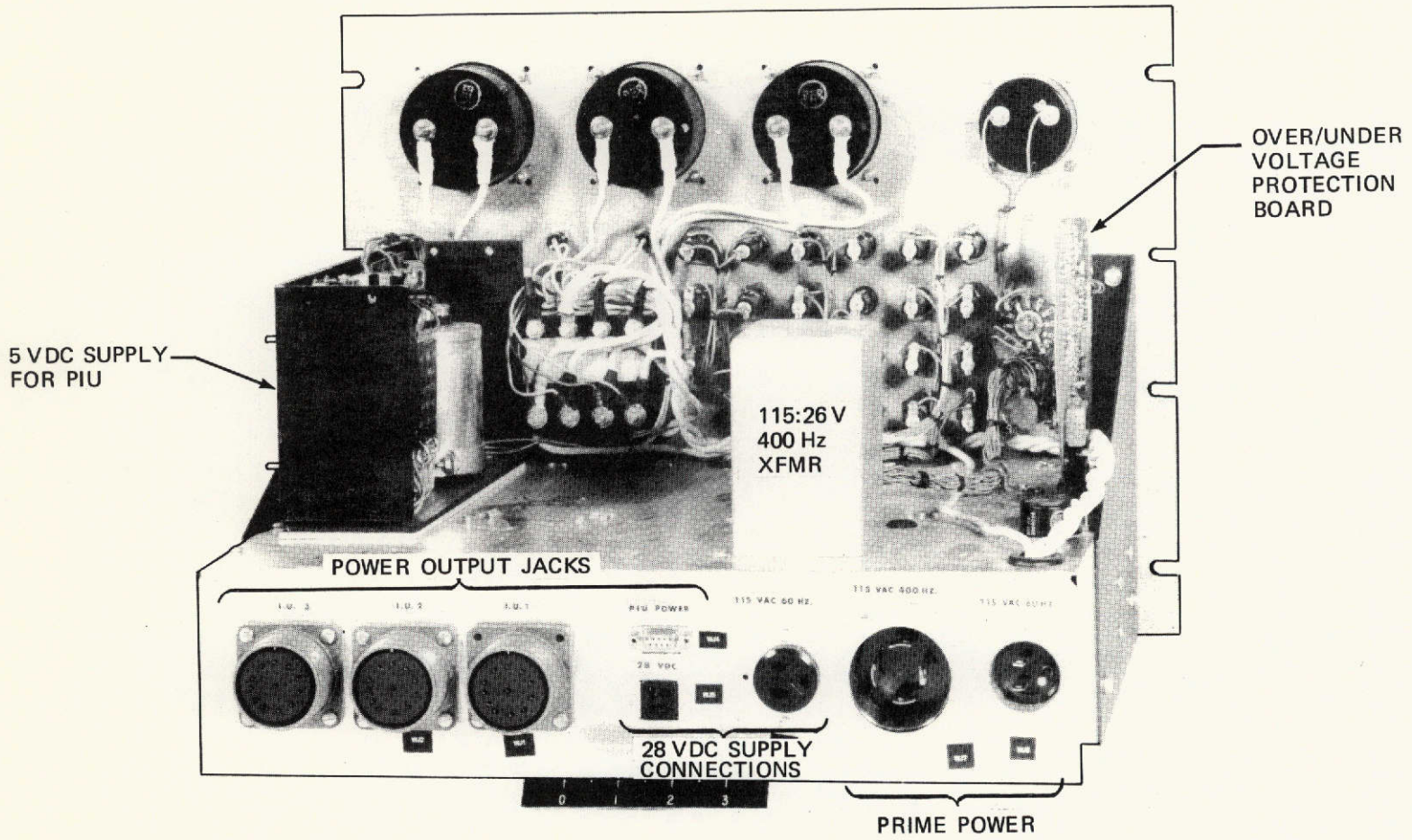


Figure E-2. PDB Rear View

LIST OF REFERENCES

Chapter 2

1. Performance Specification Inertial Measurement Unit and IMU Adjustable Mount, Singer Kearfott Division, CP6K1A100C, Issue G, 1969.

2. Inertial Measurement Unit Study For Space Shuttle Application, Singer Kearfott Division, 1971.

Chapter 3

1. Field Operating Unit Operating and Maintenance Manual, IBM Electronics Systems Center, 69-928-43, 1970.

2. Manual Operating Procedure For Field Operating Unit, IBM Electronics Systems Center, 648099-700, 1968.

3. CP-2 Computer Programmer's Manual, IBM Electronics System Center, 03640FM527022L29-1H, 1969.

4. General Prupose Computer Preliminary Technical Manual, IBM, 03640-REP-914-701X.

Chapter 4

1. McNellis, J.F., W.C. Ruland and D.E. Woods, A Computerized Test System for Strapdown Guidance Systems, AIAA Guidance, Control and Flight Mechanics Conference, Hempstead, NY, August 16-18, 1971 (Paper 71-967).

2. Strapdown System Control and Monitor Station, Hamilton Standard, unnumbered.

3. Acceptance Test Specifications Single Dynamic Axis Test Table, Goerz Optical Company, TS-1501, 1968.

4. S.D.A.T. Instruction Manual, Goerz Optical Company, IM-1524, 1969.

Chapter 5

1. ±15VDC Powertec Model 32C15D Supply. Powertec, Inc. 9168 DeSoto Ave., Chatsworth, CA 91311.
2. Motorola K1087A-1T1B Temperature Compensated Crystal Oscillator. Motorola Communications and Electronics, Inc., 4501 West Augusta Blvd., Chicago, IL 60651.
3. Advanced Packaging, Inc., 2165 South Grand Ave, Santa Ana, CA 92705.

Chapter 7

1. +5VDC Powertec Model 2DD5-12 Supply.
   ±15VDC Powertec Model 32C15D Supply.
   Powertec, Inc., 2165 South Grand Ave, CA 92705.
2. Advanced Packaging, Inc., 2165 South Grand Ave., Santa Ana, CA 92705.

Chapter 8

1. A7 Inertial Measurement Set Interface, Singer Kearfott Division 6K191A010C Issue D, 1968.

DISTRIBUTION LIST (Cont.)

Program:

NASA/MSFC — National Aeronautics and Space Administration (28)
George C. Marshall Space Flight Center
Huntsville, Alabama 35812

Attn:	M. Brooks	S&E-ASTR-SG	
	H. Brown	S&E-ASTR-SGA	
	L. Cook	S&E-ASTR-GD	(5)
	G. Doane	S&E-ASTR-SGA	
	B. Doran	S&E-ASTR-SGA	
	B. Gains	R-ASTR-GCC	
	C. Lee	S&E-ASTR-GD	
	B. Moore	S&E-ASTR-DIR	
	F. Wojtalik	S&E-ASTR-S	

Codes:	A&TS-MS-D	(1)
	A&TS-PR-RS	(1)
	A&TS-PR-M	(1)
	A&TS-MS-IL	(1)
	A&TS-MS-IP	(2)
	A&TS-MS-IP	(2)
	S&E-ASTR-GD	(2)
	S&E-ASTR-ZI	(2)
	S&E-ASTR-S	(2)
	A&TS-TU	(1)

NASA/JSC — National Aeronautics and Space Administration (12)
L.B. Johnson Space Center
APOLLO Document Control Group (BM86)
Houston, Texas 77058

Attn:	A. Turley	EG5
	K. Cox	EG2
	W. Swingle	EG5
	J. Hanaway	EG7
	W. Bradford	EA2
	H. Tindall	FA
	R. Chilton	EG
	R. Nobles	FM7
	J. Thibodeau	FM4
	R. Savely	FM4
	B. Cockrell	FM4
	M. Jones	EG5

NASA/HDQ — National Aeronautics and Space Administration (1)
600 Independence Ave., SW
Washington, D.C. 20546

Attn: R. Murad, MHE

ROCKWELL — Rockwell International Corporation (5)
Space Division
12214 Lakewood Boulevard
Downey, Ca 90241

Attn:	R. Loeliger	041-FC95
	J. Peller	041-FC95
	A. Zeitlin	041-FB75
	M. Campbell	041-FB75
	R. Epple	041-FB75

R-798

DISTRIBUTION LIST

Internal:

R. Ragan
D. Hoag
N. Sears
R. Battin
G. Silver (CSDL/JSC)
R. Cooper
K. Fertig
G. Edmonds
J. Feldman
P. Feileman
J. Gilmore
S. Helfant
R. Hutchinson
R. Booth
K. Vincent
H. Musoff
J. Harper
G. Bukow
G. Schmidt
M. Landey (5)
D. Swanson
R. Whittredge
R. McKern (10)
M. Hamilton
J. Kernan
B. Kriegsman
G. Levine
E. Mueller
T. Chien
D. Brown
R. White
D. Fraser
M. Johnston
R. Millard
W. Tanner
H. McOuat
TIC (5)