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(NASA-CR-141745) IOP MODELING STUDY Final  
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IOP MODELING STUDY  
FINAL REPORT

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IBM FEDERAL SYSTEMS DIVISION  
1322 Space Park Drive  
Houston, TX 77058

## Objectives

The objectives of this study were to develop a more detailed model of the IOP, and to use the model to evaluate IOP performance and its effect on Flight Software performance. These objectives have now been accomplished.

## Results & Recommendations

The current design of the MSC control program, FIOMCNTL, yields an I/O request service time much longer than was previously assumed. The longer service time causes an increase in the GN&C Flight Control transport lag to an average of 14.3 ms and maximum of 16.9 ms; further, the variability of the service time causes an increase in the critical input sampling jitter (see Reference 1).

Several modifications to FIOMCNTL were tested in the model, each of which reduced the average service time for I/O requests. The best case studied would have reduced the transport lag to about 13 ms average, but the worst case would still have occasionally exceeded 15 ms. A redesign of FIOMCNTL therefore appears necessary and is recommended by Systems Analysis.

DMA response time was not a serious problem in the model runs which were made. Average DMA response was 4.4µsec, the maximum number of requests outstanding was 7, and the average number outstanding was less than one.

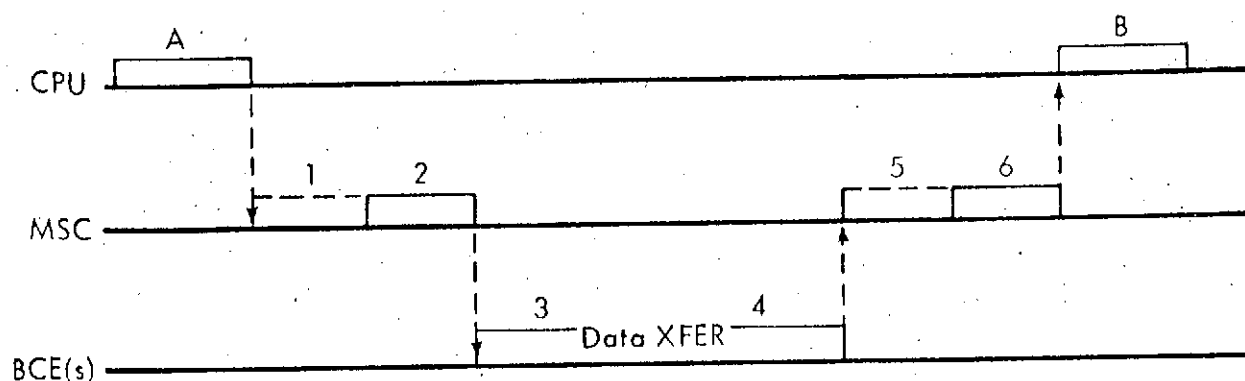
## Findings

The detailed IOP model developed for this task simulates the execution of every MSC and BCE instruction. By defining the MSC control program, FIOMCNTL, and the BCE programs to read and write data, the operation of the IOP in a realistic environment was simulated. The I/O load used to drive the IOP was the profile developed for the Approach and Landing phase of the ALT mission (see References 1 and 2).

A breakdown of an application's request for I/O is shown in Figure 1. Times 1-6 in Figure 1 occur within the IOP, and the primary output of this study is the length of these times for the basic FIOMCNTL program and two other cases with modifications to that program. The primary difference in the three cases was the length of time required for the MSC to recognize a request completion (time 5 in Figure 1). The three cases are defined as follows:

Figure 1

APPLICATION REQUEST FOR I/O  
SEQUENCE OF EVENTS



A. FCOS Starts Request

1. Time From FCOS Ready to The Request Until MSC Starts On Request.

2. MSC Set Up Time

3. BCE Set Up Time

4. BCE Clean-Up Time

5. MSC Recognition Of BCE Completion

6. MSC Clean-Up Time

B. FCOS Services Of I/O Interrupt And Dispatching Of Task If It Waited.

Case 1 - Basic FIOMCNTL. This case assumes that any BCE may be the low BCE in an outstanding request. Therefore, when monitoring for completion of requests, the MSC must step sequentially through all 24 entries (one per BCE) in a 'BCE completion' table. The MSC checks each entry to see if a request is outstanding; if it finds an outstanding request, the MSC issues a Repeat until All Indicators (RAI) instruction for the BCE's involved in the request. This instruction will delay for up to 100µsec; if all BCE's are complete before this time is up, the MSC performs clean-up operations on the request and signals the CPU. When either timeout has occurred or clean-up operations have been done, the MSC increments to the next entry in the table and checks for an outstanding request. As long as there are any active requests, the MSC continues to loop through this table; if a new request comes in from the CPU, the MSC will branch to start that request (time 2 in Figure 1) and return to continue monitoring for completions.

Case 2 - Basic FIOMCNTL modified to check only those table entries for which a BCE is active. This case is the same as Case 1 with the exception that, by using the CPU's table of reserved BCE's, the MSC is able to skip those 'BCE completion table' entries for which the CPU has not initiated a request. Since some requests use multiple BCE's, however, the MSC is still checking superfluous table entries. This case was used in the ALT PDR Analysis to yield a 14.3 ms transport lag (Ref. 1).

Case 3 - Basic FIOMCNTL modified to check only those table entries corresponding to the low BCE of an active request. This case is a further improvement over Cases 1 and 2. It assumes that the CPU will maintain a word with bits set for only those BCE's which are the lowest BCE of an active request, thereby permitting the MSC to eliminate all unnecessary checking of 'BCE completion table' entries.

Table 1 summarizes the results of the three cases. It shows values of times 1-6 in Figure 1 for each case, as well as the minimum, average, and maximum response times for I/O requests. The only difference in the three cases is in the average and maximum values for time 5, MSC recognition of BCE completion. Average DMA response time was the same in all three cases (4.4µsec).

#### Future Plans

FCOS developers are currently studying alternative designs of the MSC control program to reduce both the request service time and the variability in that time. Systems Analysis' modeling support will be provided to evaluate the alternative designs.

Table 1

## Summary of I/O Service Times within the IOP

Time Segment (From Fig. 1)	Case 1	Case 2	Case 3
1 - MSC Recognize new Request	Average 305 $\mu$ sec, Range 0-800 $\mu$ sec		
2 - MSC Set up and Start BCE's	[92+(64*No. of BCE's)+(4*Low BCE ID)] $\frac{*16.5}{8}$ $\mu$ sec		
Request for BCE #10			404 $\mu$ sec
Request for BCE's 10-13			800 $\mu$ sec
3 - BCE Set up Time	165 $\mu$ sec (repeat for each program if chaining)		
4 - BCE Clean up Time	66 $\mu$ sec (at end of last program only, if chaining)		
5 - MSC Recognize BCE's Complete	Average	Average	Average
	3260 $\mu$ sec	2100 $\mu$ sec	1280 $\mu$ sec
	Range	Range	Range
	0-6200 $\mu$ sec	0-4100 $\mu$ sec	0-2850 $\mu$ sec
6 - MSC Clean-up of Request	[112+(51*No. of BCE's)+(4*Low BCE ID)] $\frac{*16.5}{8}$ $\mu$ sec		
Request for BCE #10			419 $\mu$ sec
Request for BCE's 10-13			734 $\mu$ sec
Elapsed time for a Request within the IOP (exclude data Sfer)			
a. 1 BCE, no chaining			
Min	1.05 ms	1.05 ms	1.05 ms
Avg	4.60 ms	3.45 ms	2.65 ms
Max	8.05 ms	5.95 ms	4.70 ms
b. 4 BCE's, no chaining			
Min	1.75 ms	1.75 ms	1.75 ms
Avg	5.30 ms	4.15 ms	3.35 ms
Max	8.75 ms	6.65 ms	5.40 ms

References:

1. "ALT PDR Analysis", report by K. L. Williams, dated 2/24/75.
2. Memo to J. D. Bowman, "I/O and Processing Profiles for GN&C Flight Software," dated 1/28/75.
3. "IOP Modeling Study", interim report by R. W. Burns, Jr., dated 11/15/74.