DESIGN, PROCESSING, AND TESTING OF LSI ARRAYS FOR SPACE STATION

BY

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16. Abstract

Data for the beam-leaded SOS process using the TA5388 dual-complementary pair plus inverted circuit show the stability of the dc device characteristics through the complete beam-lead processing and packaging steps. A more complex circuit, the TA6567 - a silicon-gate, voltage-sense BL/CMOS/SOS 256-bit RAM, has also been made that was functionally perfect at wafer probe. Current efforts are to increase the yield of this circuit and to obtain electrically perfect packaged units.

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SUMMARY

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I. INTRODUCTION

The evolution of the SOS technology at RCA has covered a broad spectrum of research and development into basic materials, and device research and advanced CMOS LSI techniques including computer-aided design, mask-making, circuit design, and processing. The present NASA contract has given partial support to this effort to develop a beam-leaded (BL) silicon-gate CMOS/SOS technology with the 256-word by 1-bit RAM as the demonstration vehicle.

The circuit design and basic processing evolved from an aluminum-gate process to a silicon-gate process and finally included the beam-leads. The beam-lead process incorporated a modified micro-bridge approach to form the beams on SOS and a novel approach to laser-scribing to successfully separate the chips.

Initial beam-lead development was done on the TA5388 dual-complementary pair plus inverter circuit. The 256-word BL/SOS RAM unit, the TA6567, was demonstrated functionally perfect at wafer probe but with low yield. No perfect packaged TA6567 units have been made, but some processing problems have been defined which could affect the yield.

II. PROCESSING PROBLEMS WITH BL/SOS TA6567 256-BIT RAM

In general, the major processing problems were defined and resolved for the beam-leaded SOS processing by using the TA5388 dual-complementary pair plus inverted circuit. Data have been given (Ref. 1 and this report) to show that good electrical results were obtained on this simple circuit. Certain processing problems can be expected to arise when a more complex circuit with more stringent design rules is substituted. One such problem was encountered in the BL processing of the TA6567 circuit. The difficulty is basically overetching the contacts and hence not getting complete coverage of metal over the contact area or junction passivation.

Figure 1 shows an area of the TA6567 with overetched contacts and the metal that does not completely cover the contact area. This invites a problem of inadequate passivation and possible contamination

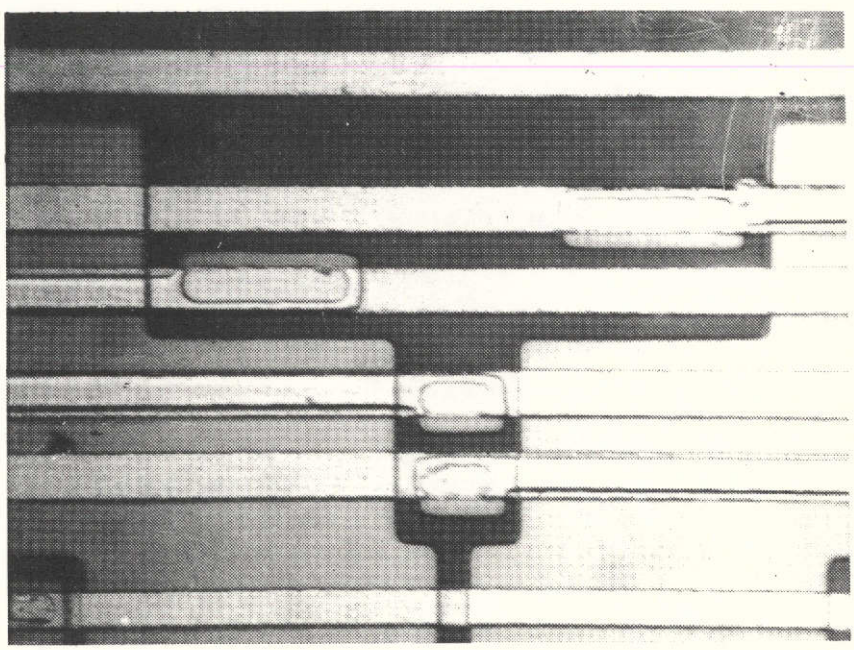

Figure 1. Contact opening and metal coverage on the TA6567 circuit.

of the device silicon during the beam-lead processing. The larger contacts in this circuit were designed as 0.2 mil wide and measure 0.3 mil wide, and the 0.5-mil metal measured 0.45 to 0.48 mil wide. This problem becomes more serious when we attempt to align all the chips across a 2-in.-diameter wafer. The overetching is more likely to happen with the beam-lead processing because the contact etching requires etching through the Si_3N_4 passivation layer as well as the SiO_2 layer, thus increasing the chance of undercutting and enlarging the contact area.

Two solutions to this problem are being explored. First, we are trying for better control of the contact dimensions by improving the etching techniques. Second, for the same purpose, a new contact mask with smaller dimensions will be available shortly.

III. BEAM-LEADED SOS PUSH-OFF TESTS

A measure of the mechanical strength of the beam-leaded TA5388 SOS chips was made using the standard push-off test. This test involves bonding the beam-leaded chip to a metallized ceramic and measuring the force necessary to cause mechanical failure of the bonds. The force is applied by a plunger passing through a hole in the ceramic to the circuit area of the pellet. The data presented in Table 1 are in 'grams' of push-off strength and the general type of failure observed. The bottom line of Table 1 gives data for a 14-lead BL bulk chip for comparison with the BL/SOS. The 'Location of Failure' refers only to the general area of failure in the bulk because of the differences between bulk and SOS BL processing.

Table 1. 14-Lead Beam-Lead SOS Push-Off Test Failures

	Number of Failures				'grams'
Location of Failure	Beam-to-Substrate Metal	Beam at Pillar	Base Metal (Au I) to Beam (Au II)	Broken Beam	Push-off Strength
Wafer No.					
SW27-1	33	16	3	6	69
SW28-3	40	11	3	-	53
Master 5959	4	2	55	7	83

It should be emphasized that these values are from initial tests on the BL/SOS devices and that the processing has not been optimized for beam strength.

The predominant BL/SOS failure mechanism is the beam-to-substrate bond; it differs from the bulk-failure mechanism. The push-off strength values for the SOS are well above the minimum acceptable strength of 32 grams for a 14-lead device. Again, the SOS processing is not optimized and the SOS push-off strength is lower than the bulk push-off strength.

IV. ELECTRICAL RESULTS ON PACKAGED BEAM-LEADED SOS DEVICES

The discussion of electrical results in this section is a continuation of the experiment using the TA5388 circuit, as described in the previous report [Ref. 1]. The data presented in that report compared the TA5388 wafer probe average dc device parameters after the base metal processing and after the beam formation with the aluminum metal control wafers for various thicknesses of the Si_3N_4 passivation layer. This update is to check the effect of laser-scribing, separating, and packaging on the device parameters. The data are presented in Table 2 for the TA5388 circuits at wafer probe and after packaging. For ease of comparison the wafer probe data labeled Au I and Au II are repeated from Ref. 1. The data for 1200 Å of Si_3N_4 are omitted because too few chips from this wafer were packaged.

The parameters are leakage current (I_L) measured in nA/mil, threshold voltage (V_T) at 10 μA in volts, transconductance (g_m) in μmhos, and source-to-drain breakdown voltage (V_{BD}) in volts, measured at 50 μA. The subscripts P and N are for the PMOS and NMOS transistors, respectively. The alphanumeric designation for the wafer is given in parentheses on the left of the I_{LP} values. The values for the other device parameters are listed in the same order as for I_{LP}.

The histograms of V_T for wafer SW27-1 of both the NMOST- and PMOST-packaged devices are shown in Figs. 2 and 3, respectively, and agree closely with those published as Figs. 12 and 3 in Ref. 1 for Au I and Au II wafer probe.

The comparison of the data in Table 2 with these histograms shows that the dc device parameters are not changed drastically through the entire beam-lead processing and packaging steps.

The first lot of beam-leaded packaged TA6567 circuits, the BL/SOS/CMOS 256-word by 1-bit RAM, was completed and is undergoing extensive electrical testing. Initial testing of the first packaged units shows that the circuit is functioning but generally not as well as it did

Table 2. BL/SOS TA5388 Average DC Device Parameters, V_{DD} = 10 Volts

	Si_3N_4 Thickness (Å)	Wafer Probe Au I		Wafer Probe Au II		Packaged Au II
I_{LP} (nA/mil)	500	(SW27-1)	0.8	(SW27-1)	0.9	1.19
	2000	(SW28-3)	0.7	(SW28-3)	1.0	0.40
I_{LN} (nA/mil)	500		-0.7		-0.6	0.81
	2000		-3.9		-2.9	4.1
V_{TP} (volts) @ 50 µA	500		-0.86		-0.84	-0.82
	2000		-0.87		-0.87	-0.81
V_{TN} (volts)	500		1.53		1.55	1.57
	2000		1.41		1.19	1.44
g_{mP} (µmhos)	500		1164		1177	1195
	2000		1240		1245	1176
g_{mN} (µmhos)	500		768		760	760
	2000		950		910	813
$V_{BD(P)}$ (volts) @ 50 µA	500		-29.0		-28.9	29.5
	2000		-28.1		-27.5	27.1
$V_{BD(N)}$ (volts)	500		25.8		25.8	25.9
	2000		26.2		26.5	25.1

at wafer probe. The total circuit current has increased compared with the value measured at wafer probe, and the cause is being investigated. The initial measurement of the read access time as a function of output load capacitance on these units compares closely with the data measured

for this circuit with aluminum metal, as was expected (see page 31, Ref. 1).

Efforts to improve the yield and obtain more packaged TA6567s for evaluation are under way. A description of processing problems is given in Section III of this report.

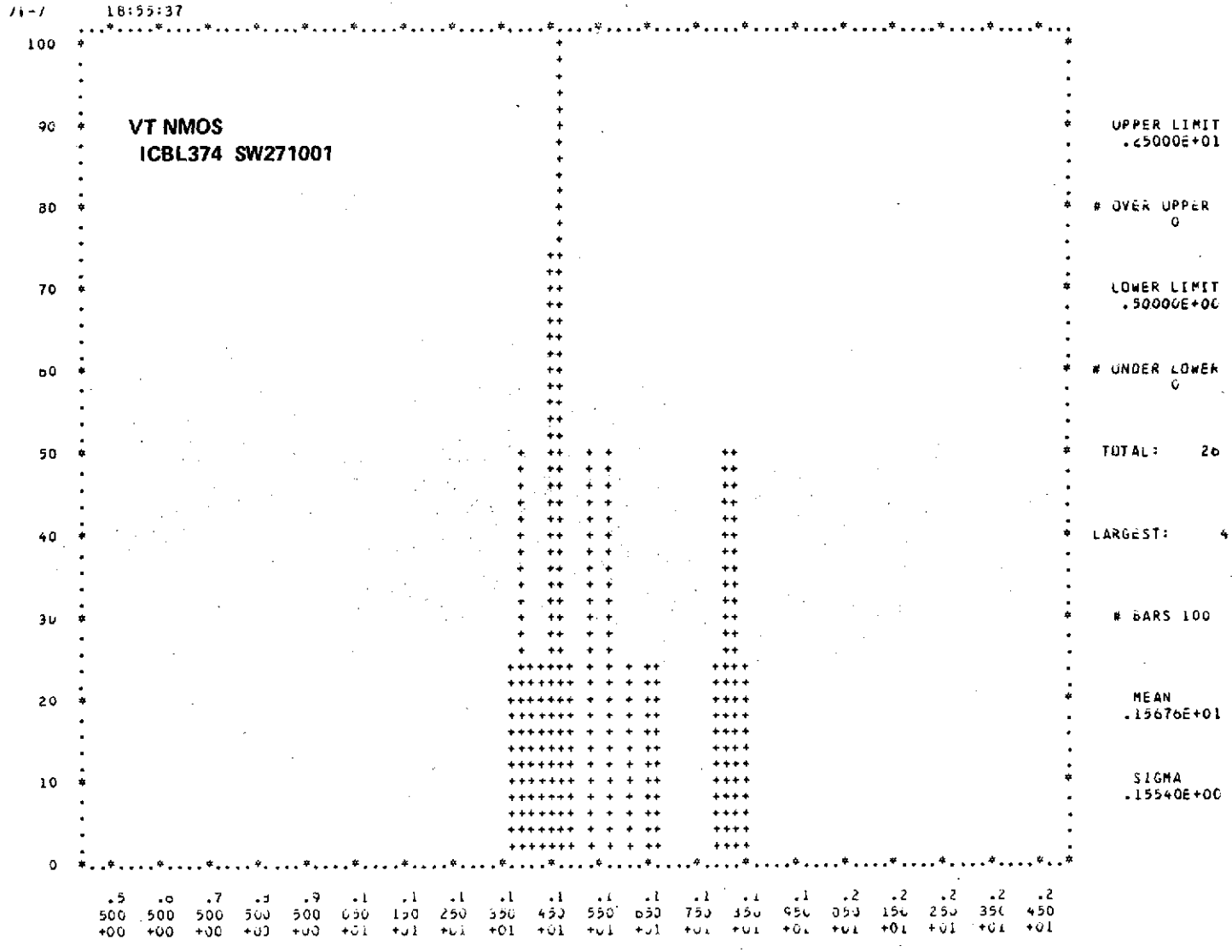

Figure 2. V_{TN} values of TA5388 BL/SOS packaged units from SW27-1, 500-Å Si_3N_4.

Figure 3. V_{TP} values of TA5388 BL/SOS packaged units from SW27-1, 500-Å Si_3N_4.

V. PERSONNEL AND EXPENDITURES

During the quarter (10/1/74 to 12/31/74) reported herein the following personnel contributed to the contract:

W. C. Schneider	Project Scientist

Total expenditures through December 31, 1974 have been $256,648, including profit. Problem areas that may create an overrun: none at this time.

VI. NEW TECHNOLOGY APPENDIX

It was concluded from the review of the work that there were no reportable items of New Technology under the contract during the period covered by this report.

ACKNOWLEDGMENTS

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REFERENCES

1. W. C. Schneider, *Design, Processing, and Testing of LSI Arrays for Space Station*, Quarterly Technical Report No. 15, Contract NAS12-2207, November 1974.