EE-MSFC-1888

Final Report

STANDARDIZED MULTIPLE OUTPUT

POWER SUPPLY

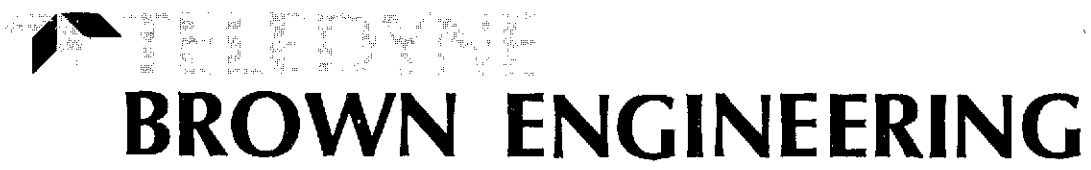## by E. V. Ragusa

PRICES SUBJECT TO

April 1975

TELEDYNE
BROWN ENGINEERING

Cummings Research Park• Huntsville, Alabama 35807

FINAL REPORT
EE-MSFC-1888

STANDARDIZED MULTIPLE OUTPUT POWER SUPPLY

By

E. V. Ragusa

April 1975

Prepared For

Contract No. NAS8-29770

Prepared By

ELECTRONICS AND ENGINEERING
TELEDYNE BROWN ENGINEERING
HUNTSVILLE, ALABAMA

i

ABSTRACT

This report describes a comprehensive program to develop a prototype model of a standardized multiple output power supply for use in space flight applications. The prototype unit was tested and evaluated to assure that the design would provide near optimum performance for the planned application.

The prototype design uses a dc-to-dc converter incorporating regenerative current feedback with a time-ratio controlled duty cycle to achieve high efficiency over a wide variation of input voltage and output loads. The packaging concept uses a mainframe capable of accommodating up to four inverter/regulator modules with one common input filter and housekeeping module. The packaged configuration is designed to meet the EMC requirements of MIL-STD-461A, Notice 3. Each inverter/regulator module provides a maximum of 100 watts or 10 amperes. Each module is adaptable to operate at any voltage between 4.0 volts and 108 volts. The prototype unit contains +5, ±15 and +28 volt modules.
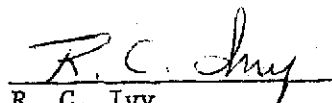
Pertinent characteristics and features of the power supply are:

- Input Voltage Range: 24 to 36 volts, steady-state
- Efficiency: 78%
- Regulation Line and Load: 0.002% of the output voltage
- Temperature Coefficient: 0.0003%/°C of the output voltage
- Ripple: 0.825% of the output voltage peak-to-peak
- Step Load Response: 10.5% over or undershoot with a recovery time of 0.875 msec
- Isolation: 200 Mohms
- Programmable Current Limit
- Remote Startup/Shutdown
- Remote Sense
- Overvoltage/Undervoltage Protection and Monitoring
- Fault Indication
- Short-Circuit Protection
- Weight: 20.6 lb
- Volume: 410 in^3, including carrier
- Output Power: 350 watts
- Output Voltage: Four Isolated Outputs: 4.0 volts to 108 volts.

APPROVED:

H. O. McCrory
Manager
Manufacturing & Engineering Support

R. C. Ivy
Director
Electronics & Engineering

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

1. INTRODUCTION

Teledyne Brown Engineering's (TBE's) effort to fabricate a prototype model of a standardized multiple output power supply is a direct result of an earlier study performed by TBE. This study performed under Contract No. NAS8-27798 resulted in the establishment of preliminary design requirements for an airborne power supply which would satisfy most of the needs of future manned space vehicles and the development of a design for a power supply which fulfills those requirements.

This contract, NAS8-29770, utilizes these study results to develop and fabricate a working prototype power supply.

2. OBJECTIVE AND ORGANIZATION

2.1 OBJECTIVE

The primary objective of this effort is the fabrication and delivery of a working breadboard model and a prototype model multiple output power supply as defined in Contract No. NAS8-27798. The results of this fabrication process are documented in this final report.

2.2 ORGANIZATION

The fabrication effort was divided into three tasks. These tasks were:

- Task I - Fabricate and deliver a 5-volt, 50-watt breadboard power supply in general compliance with the design goals generated during Contract NAS8-27798. The breadboard was to be tested electrically to evaluate compliance with the design goals (Ref. 1).

- Task II - Fabricate and deliver a prototype model of a multiple output power supply tested to show compliance with the specifications. The prototype was to contain four power modules with the following output voltages and power:

VOLTAGE (V)	POWER (W)
+28	100
+ 5	50
+15	100
-15	100

- Task III - Submission of a final report which documents and summarizes the results of the contracts including recommendations and conclusions based on the results obtained.

The following sections of this final report present a detailed description of the activities and accomplishments of each task of the fabrication effort as well as a summary of the events which preceded this effort.

3. ACTIVITIES AND ACCOMPLISHMENTS

As noted, the general objective of this contract was to fabricate a multiple output power supply which would satisfy a majority of the requirements of future manned space vehicles. To give an account of the activities and accomplishments of this effort, it is first necessary to summarize the activities and conclusions of Contract NAS8-27798.

3.1   "THE POWER SUPPLY STANDARDIZATION AND OPTIMIZATION STUDY" - SUMMARY

The objective of this study was to develop a design for a standard power supply for manned space vehicles.

3.1.1 Activities

The study effort was divided into four phases to accomplish the objective:

- Phase I - Definition of Requirements - During this phase the requirements for conditioned power in the Space Shuttle and Manned Space Station were reviewed and analyzed. The information obtained from these reviews and analyses was supplemented with known performance characteristics for existing power supplies, and a preliminary design specification was prepared for the standard power supply. When necessary, tradeoff studies were performed to establish the best overall configuration for the supply.

- Phase II - Design Electrical Circuits - The preliminary design specifications and the recommendations of the tradeoff studies performed in Phase I were used as the criteria for designing a power supply. In this phase, candidate circuits which were capable of providing the necessary performance, as defined in the preliminary design specification, were analyzed and a preferred design was developed.

- Phase III - Identification of Potential Hybrid Microcircuits - The preferred circuit design for the power supply developed during Phase II was analyzed to determine those circuit functions which could be packaged as hybrid microcircuits. Preliminary specifications for each of the candidate circuits were prepared and submitted to hybrid vendors for review and pricing.

- <u>Phase IV - Packaging</u> - The design for the power supply was packaged and documented. Assembly drawings were generated for several of the various components and sub-assemblies in the power supply. A thermal analysis of the package was performed to assure that excessive temperatures were not possible under worst case operating conditions.

In addition to and concurrent with Phases II and III of the study, a breadboard of a single regulator was constructed. This effort was undertaken to verify the analysis and predicted performance of the power supply, and to authenticate the circuit such that the efforts of Phases III and IV could be supported by actual data.

Throughout the study a number of guidelines were used in order to give direction to and a means of measuring the success of the effort. These guidelines are shown, in the order of importance, below:

- The selected power supply design must be suitable for uses in man-rated spacecraft.

- The design must be readily adaptable to changes in load requirements.

- Efficiency must be maximized.

- The power supply must be maintainable using spares, tools, and test equipment available in large orbital vehicles.

- The design must be cost-effective.

- Size and weight must be minimum, consistent with the other guidelines.

3.1.2 <u>Conclusions</u>

The results of each phase of the study effort are given below.

3.1.2.1 <u>Phase I</u> -

- A set of requirements was established for conditioned power in the Space Shuttle. While these requirements do not represent the exact, detailed requirement for power in future space applications, they do form a sufficient base for sizing functional elements for a power supply for future space vehicles. The output

power level requirement for the supply was established as being a range between 10 and 150 watts. Recently available data on the electrical power loads in the Manned Space Station was compatible with these requirements.

● The pertinent power system parameters and constraints which affect the design of an optimum power supply were defined as:

   ▲ The steady-state input voltage from the power system will be between 90 and 125 Vdc.

   ▲ Voltage transients on the input of the supply will not exceed those defined by MIL-STD-704A. Most of the transients to which the power supply will be exposed are expected to be much less severe than those specified by the military standard.

   ▲ The primary voltage source characteristics will be those of a large aerospace power system which uses solar array and batteries, fuel cells, or ac generators with a transformer-rectifier to provide the dc voltages.

   ▲ The output voltage range of 5 to 108 volts would provide for in excess of 95 percent of the power requirements utilized by future space vehicles.

● A tradeoff study was performed to determine the optimum overall configuration for the power supply. The results of the tradeoff study showed that a separate power supply for each of the definable loads (LRUs) would provide the best overall performance.

● A preliminary design specification was prepared for the power supply. The specification contains sufficient detail to allow circuits to be designed for the various functional elements of the power supply.

3.1.2.2 Phase II - After considerable tradeoff studies to analyze and evaluate design approaches, circuit configurations, and components for the power supply design, an optimum design was developed. The resulting design selected was basically a push-pull, regulating converter.

This converter has the following features:

● Unique Control Concept - The inverter uses a pulsewidth modulator with current feedback. This forces the inverter and rectifier to appear as a current source. In turn,

3-3

this effectively removes the high-Q, low-frequency resonances of the output filter. Thus, the control loop poles are determined by the load resistance and output filter capacitance, and a very stable 6-kilohertz regulating bandwidth is obtained.

- Unique Base Drive Circuit - The base drive circuit is a current source with no power-wasting series resistors. The base current is controlled by feedback from the collector current, providing a constant forced beta which is determined by the turns ratio of a drive transformer. Thus, only the necessary base drive is applied, as needed, increasing the efficiency of the base drive circuit. Additionally, the base drive transformer is capable of duty cycle control of zero to nearly 95 percent without saturating.

- Very Low Standby Power Consumption - The control circuits have a very low power requirement which allows high efficiency at power outputs down to 5 to 10 percent of full load.

3.1.2.3 Phase III - The relative complexity of a high performance power supply led to the investigation of utilizing hybrid integrated circuits. Hybrids offer greatly increased component packaging densities with a resulting reduction in overall size and weight and improved reliability of the circuit. The approach used to select the hybrid circuits, although simple, was based on subdividing the electrical schematics of the power supply into usable, functional blocks resulting in five candidate hybrid circuits.

In addition, a preliminary specification describing the hybrids was written. The specification included a list of discrete device and component types to be used in the hybrids, general component performance criteria, hybrid size and quality specifications, and areas of special attention such as transistor matching requirements, and active and passive component trimming requirements. This specification was sent to 17 qualified hybrid vendors for preliminary quotation. The response to this preliminary quotation confirmed that the design was compatible with current hybrid techniques and that these hybrids could be produced at reasonable costs and within the size requirements specified.

3.1.2.4 <u>Phase IV</u> - The advantages of size and weight offered by the custom-design approach were more than offset by the significant cost savings possible in the modular configuration. A modular packaging concept for the power supply provides maximum flexibility in adapting the unit to various applications.

3.1.3 Recommendations

The results of the study effort indicated that an optimum, standard design is practical for airborne power supplies. The work performed has been based on analytical calculations and breadboard results. It is recommended that a nonflight prototype of a power supply similar to that discussed in the report be fabricated and tested using the concepts and designs developed. This prototype will prove to be of considerable value in establishing the standard power supply design as a viable concept for future aerospace programs.

3.2 TASK I ACTIVITIES AND ACCOMPLISHMENTS

The objective of Task I was to fabricate a 5-volt, 50-watt breadboard power supply. The breadboard was to be tested electrically to evaluate compliance with the design specification (see Appendix A). This task proceeded in several steps:

- Review the preliminary design specification and breadboard results that were obtained during "The Power Supply Standardization Study" to establish a design specification

- Generate a firm electrical design incorporating hybrid integrated circuits

- Review the packaging concept developed during the "Power Supply Standardization and Optimization Study" to establish a preliminary package design

- Fabricate and test the hybridized breadboard power supply to show compliance with the design specification.

3.2.1 Review of Preliminary Design Specification and Breadboard Results

The breadboard performance characteristics met and in many instances exceeded the design goals contained in the preliminary design specification. These results supported by the worst case design analysis performed during the study proved that this original design would satisfy the objectives and requirements of the preliminary specification (Ref. 1).

A summary of these performance characteristics are shown in Appendix A.

Due to a directive by MSFC, the preliminary design specification was modified. MSFC felt that the input voltage should be reduced from 100 to 28 Vdc since a large percentage of the available power would be 28 Vdc.

3.2.2 Generation of a Firm Electrical Design

The only design requirement modification made to the preliminary specification was for the prime power utilized by the power supply to be 28 Vdc. This being true, only a redesign of the input filter, rescaling of the inverter power transformer, and selection of suitable power switching transistors would be required to accommodate this specification change.

The reduction of the power supply input operating voltage, however, affects the overall power supply efficiency. The reason for this is due to the increase in the required input current at lower voltages. Since the prime power was reduced from a nominal of 100 to 28 Vdc, the required input current for a given power output increases as the ratio of these voltages:

$$I_{in} = \frac{P_{out}}{n\ E_{in}}$$

where

I_{in} — required input current

P_{out} — required output power

n   —   efficiency of the power supply

E_{in} —   input voltage.

This reduction in input voltage increased the input current by 3.6, resulting in higher switching transistor conduction losses and higher diode conduction losses in the reverse polarity protection circuit (see Appendix C-5, Note 1 of Ref. 1).

The increase in current necessitates increased filtering on the input power to meet the requirements of MIL-STD-461A. Therefore, for the same size input filter, the losses in the filter section increase. These increased losses, due primarily to the choke losses, are copper-related losses. The required inductance increases since

$$L \frac{di}{dt} = \text{constant}.$$

The required number of turns required increased inductance increases since

$$N^2 = \frac{L \; M1}{0.4} \times 10^8$$

where

N   —   number of turns

L   —   inductance required

M1   —   magnetic length of the core

      —   core cross sectional area

      —   core permeability

and since the copper resistance is directly related to the number of turns squared, as

$$R_{copper} \propto N^2 \quad ,$$

then the copper resistance can be related to the input current as

$$R_{copper} \propto I_{in}$$

and the power loss may be related as

$$P_{copper} = R_{copper} I_{in}^2$$

or

$$P_{copper} \propto I_{in}^3 \quad .$$

Thus the copper losses would increase as the cube of input current (see Appendix C-7, Note 1 of Ref. 1). This is correct, however, if the value of capacitance remains the same.

The reduction in voltage allows the use of a higher value of capacitance for the same volume

$$C \, V^2 \times \text{Volume of capacitor.}$$

The increase in capacitance corresponds to a reduction in the value of required inductance. The power lost in the copper then reduces to

$$P_{copper} \propto \frac{I_{in}^3}{V_{in}^2}$$

and since $V_{in} \propto I_{in}$

$$P_{copper} \propto I_{in} \propto \frac{1}{V_{in}} \quad .$$

The corresponding degradation in efficiency may then be calculated, the results of which are tabulated as follows:

TYPE OF LOSS	LOSS IN WATTS	
	INPUT VOLTAGE 100 VOLTS	INPUT VOLTAGE 28 VOLTS
Transistor Conduction	1.00	4.43
Diode Conduction	1.23	6.33
Input Filter Copper	1.00	3.60
TOTAL	3.23	14.36

The calculated efficiency at 28 volts is then

$$N = \frac{P_{out}}{\dfrac{P_{out}}{N_1} + P_{in}}$$

where

N   — new efficiency (28 volts)

N_1 — old efficiency (86 percent at 100 volts)

P_{in} — increase in power loss

N   = 80.8 percent.

Although the calculated efficiency was marginally within the design goal of 80 percent, the redesign of the input filter was restricted to the same volume constraints as the preliminary circuit design, in lieu of increasing the size, weight, and cost to obtain higher efficiency.

This design, incorporating hybrid integrated circuits, is shown in Appendix B.

It was necessary to generate a Manufacturing Design and Test Specification for the hybrid integrated circuits. This specification is shown in Appendix C.

3.2.3 Review and Generation of a Preliminary Package Design

The recommendations of the "Power Supply Standardization and Optimization Study" are that the most likely optimum overall configuration of power supplies used in space flight applications would have a separate supply for each of the definable loads, or LRUs, in a space vehicle.
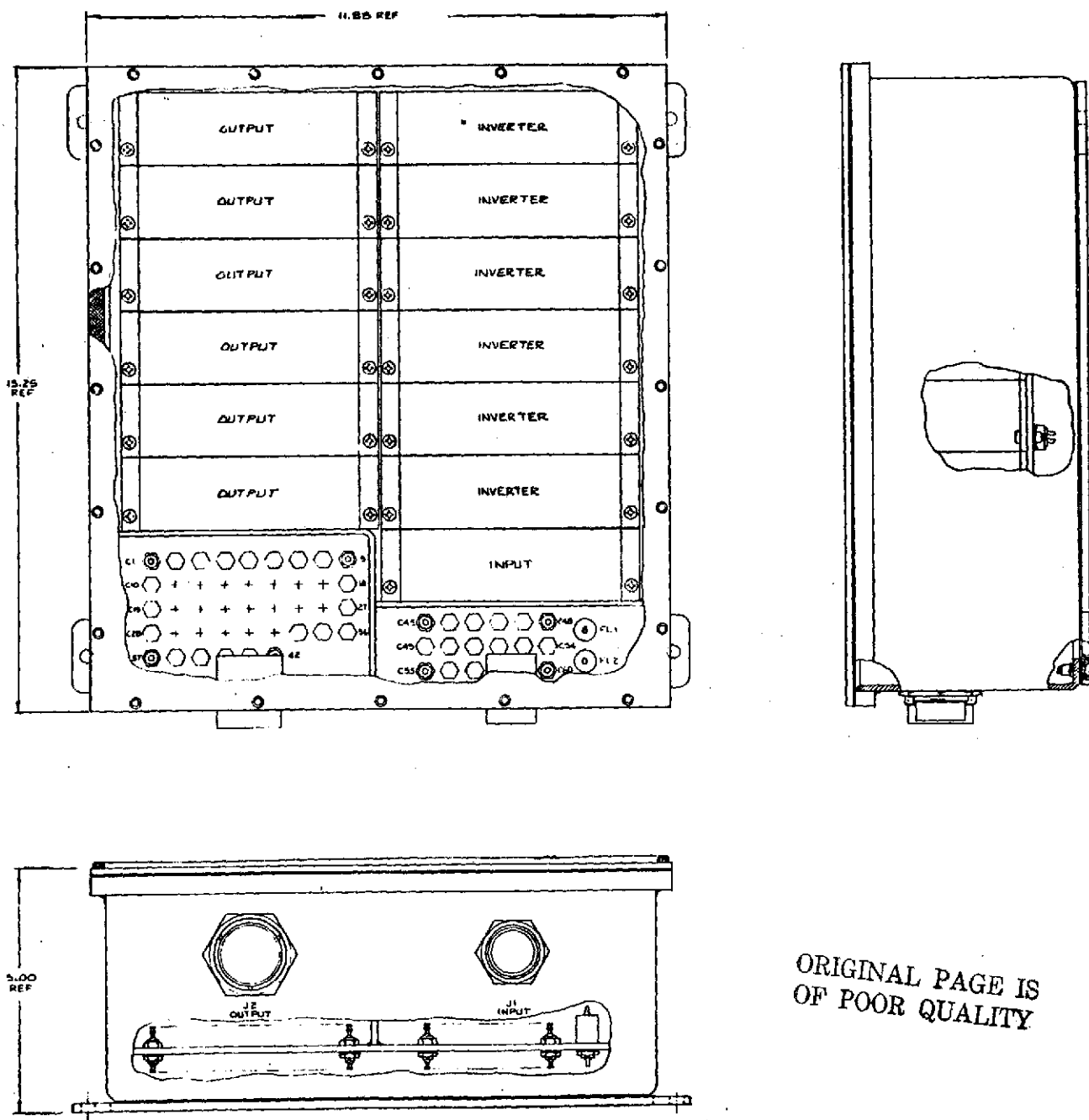
It further recommends that the power supply be designed in a modular family configuration. Based on these recommendations, a package design was presented (Figure 3-1) whereby various power modules are contained in a customized housing. This is only one of the many configurations that may be used for packaging the power supply. User requirements could dictate many different configurations.

If the power supply is intended for use inside another electronic black box, it might be desirable for the modules to be separable for versatility in layout of that black box. Each power supply module in this case could be of open frame construction since the chassis in which it is used would provide whatever level of environmental protection is required. However, even though this is a possible application, the guidelines for the power supply design, such as specifications MIL-E-5400, MIL-STD-461, and MIL-STD-202, imply that the supply will need to have a certain level of environmental resistance. Therefore, the modules require a configuration that would allow the overall package to have, as a minimum, a dust and moisture resistant container with RFI shielding capability.

The closed container configuration shown in Figure 3-1 requires either a single box design large enough to accept the maximum possible number of modules or a different box size for each quantity of modules. The maximum box obviously creates volumetric inefficiencies if less than the maximum number of modules is used. A more versatile package can be obtained by the use of a piggy-back, or strap-together, arrangement of the modules. A design concept such as is shown in Figure 3-2 is one way of accomplishing this.
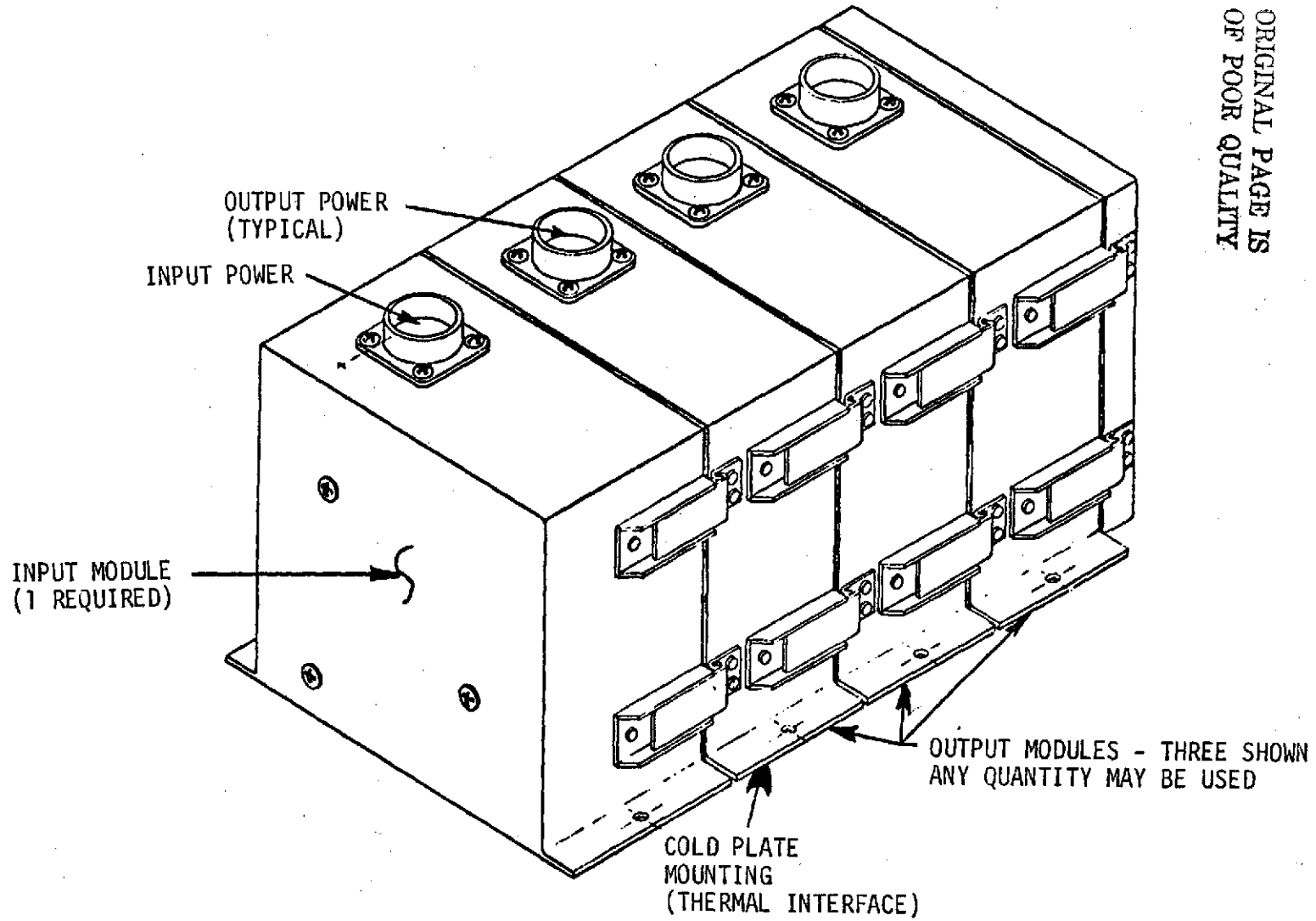
Both the single box and the strap-together arrangements require some power distribution interconnections. The power distribution can be designed and built into the single box or some other type of carrier configuration, whereas the strap-together harnessing needs to be user-designed.

Although the strap-together method is more versatile, the internal busing requirements through the modules becomes a serious problem. The problem of accomplishing alignment and mechanical strength, which is necessary for maintaining RFI and environmental integrity, becomes an overwhelming disadvantage.

FIGURE 3-1. TYPICAL OVERALL PACKAGE ASSEMBLY CLOSED
CONTAINER CONFIGURATION

OUTPUT POWER
(TYPICAL)

INPUT POWER

INPUT MODULE
(1 REQUIRED)

OUTPUT MODULES - THREE SHOWN
ANY QUANTITY MAY BE USED

COLD PLATE
MOUNTING
(THERMAL INTERFACE)

FIGURE 3-2.   OVERALL PACKAGE ASSEMBLY (PIGGY-BACK) CONFIGURATION

Both of these package configurations have advantages which could be obtained by incorporating both approaches. The result is a package concept utilizing an expandable mainframe capable of accommodating a number of modules. This package maintains mechanical integrity while still offering the versatility of use without the carrier, as in the black box. This configuration is shown in detail in Appendix C.

3.2.4 Evaluation of the Hybridized Breadboard

The test results demonstrated compliance with design goals with the exception of the desired efficiency. The efficiency measured was 76.6 percent, 3.4 percent below the design specification and 4.0 percent below the calculated efficiency. This unaccounted-for loss, amounting to approximately 3 watts, is due to the increased switching losses of the power transistors selected.

Interference measurements were performed on the input power lines to the optimum power supply breadboard. Measurements were made with the power operating at full load at input voltage levels of +24, +30, and +36 Vdc. MIL-STD-461 was used as a guide in performing these measurements.

Test results indicate that the power supply meets the requirements of MIL-STD-461 for conducted interference on the input power lines with the exception of a CW signal present at approximately 30 megahertz. This signal exceeds specification limits by 8 decibels. The broadband noise level also peaks at about 30 megahertz and exceeds specification limits by 3 decibels.

The final version of the power supply will utilize input power connectors with filters built into the connectors. These should provide sufficient attenuation at 30 megahertz to reduce the conducted emissions within specification limits.

The complete results of these tests are shown in Appendix E.

3-13

3.2.5 Recommendations

- For the input steady-state voltage requirements for the power supply being reduced, it is recommended that the specification efficiency be reduced from 80 to 75 percent in lieu of increasing the overall power supply size.

- The use of hybrid integrated circuits did not significantly reduce the overall size of the power supply. The cost of utilizing hybrids is high when compared to using dicrete integrated circuits. It is not felt that these costs are justifiable when traded off with improved reliability, since the complexity of the design could be reduced by sacrificing efficiency to a small extent. It is recommended that a discrete component design should be pursued to effect a cost reduction.

- There was no significant size difference between a 10- and 50-watt power supply module maintaining constant efficiency. It is recommended that only 50-watt and possibly 100-watt power supply modules be employed in the design. This would reduce the number of modules required to implement a design for a particular requirement.

  A 100-watt power module would increase the power per unit volume ratio two-fold and the requirements for modules to be parallelable could be deleted since 100 watts would be the largest power that a user would want to bus together. This would also reduce the overall complexity of the power module.

- The power supply output voltages should be defined in discrete steps rather than voltage ranges to reduce the number of different configurations. There is a need to standardize the voltages available to power uses in order to accomplish this.

- The output ripple and impedance requirements are much too severe when considering the volume and efficiency improvements of a relaxed specification. It is recommended that the ripple requirement of 1 percent of the output voltage and output impedance requirement between 100 hertz and 100 kilohertz be increased by a factor of two.

- The input reverse polarity protection diode is the single most dissipative element in the power supply. Although this diode offers protection during test, it affords no meaningful protection during normal operation. It is recommended that this diode be removed to improve the power supply efficiency.

- This package design has a disadvantage in that the conduction cooling path is through the wiring plane surface decreasing the thermal conductivity from each power module to the cold plate. It is recommended that a design be implemented such that the cold plate surface be configured on adjacent planes, greatly increasing the thermal conductivity required at the proposed higher power levels.

3.3 TASK II ACTIVITIES AND ACCOMPLISHMENTS

The objective of Task II was to fabricate and deliver a prototype model of a multiple output power supply. This prototype was tested electrically to show compliance with the specification. This task proceeded in several steps:

- Review of Task I recommendations and establishment of a firm specification

- Modification of the electrical and mechanical design consistent with the specification

- Fabricate and test the prototype multiple output power supply.

3.3.1 Establish Firm Specification

A design review was conducted by MSFC at TBE during which the recommendations made during Phase I were considered. The significant cost, volume, and weight savings afforded by the proposed recommendations led to these recommendations being incorporated into the preliminary design specification. This specification is shown in Appendix F.

3.3.2 Modification of the Electrical and Mechanical Design

An extensive design effort to reduce the complexity of cost and volume without affecting performance of the power supply design was made. The effort resulted in the following design modificatons:

- All hybrid integrated circuits were replaced with relatively low cost, standard, discrete components and integrated circuits.

- The incorporation of a common housekeeping supply. This removed the need for each power module to contain an input ground reference and an output ground referenced housekeeping regulator. Since ground isolation could be maintained by the one housekeeping supply, the need for an optical coupler and associated circuitry was removed. Also a synchronizing pulse could be obtained from the housekeeping inverter and thus the requirement for a clock for each power module was not necessary.

- The permalloy powder cores used previously in the inductor design were replaced with laminated iron, effecting a cost and volume reduction.

- A current transformer was utilized to measure load current permitting a conventional integrated circuit comparator to be used in place of a discrete component design.

- The mechanical configuration was modified such that the wiring plane and the heat sink surface were located on adjacent surfaces on the carrier.

- Each power module was designed to accommodate 100 watts, with the exception of the 5-volt output designed to furnish 50 watts, increasing the watts per unit volume ratio.

The resulting prototype design is shown in Appendix G.

3.3.3 Fabrication and Test of the Prototype

A multiple output, modular power supply prototype was fabricated. This prototype is shown in Figures 3-3 and 3-4. The prototype was tested and in general meets and in many cases exceeds the design goals and specifications. The results of these tests are shown in Appendix H. The pertinent characteristics of the power supply are:

- Input Voltage Range: 24 to 36 volts steady-state
- Efficiency: 78 percent
- Regulation Line and Load: 0.002 percent
- Temperature Coefficient: 0.0003%/°C
- Ripple: 0.825 percent
- Step Load Response: 10.5 percent with 0.875 msec
- EMC: Compatible with MIL-STD-461A, Notice 3
- Isolation: 200 Mohm
- Programmable Current Limit
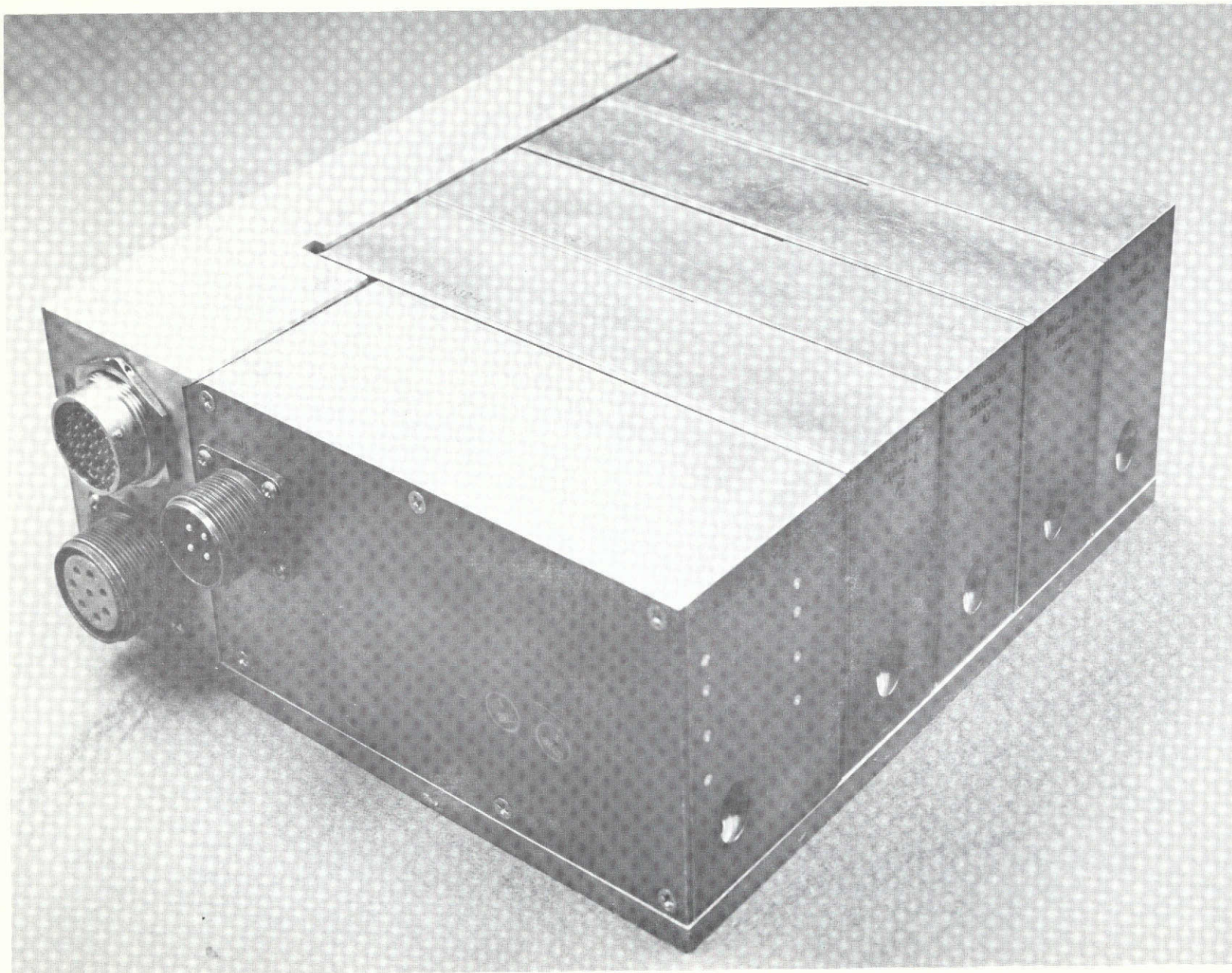- Remote Startup/Shutdown
- Remote Sense

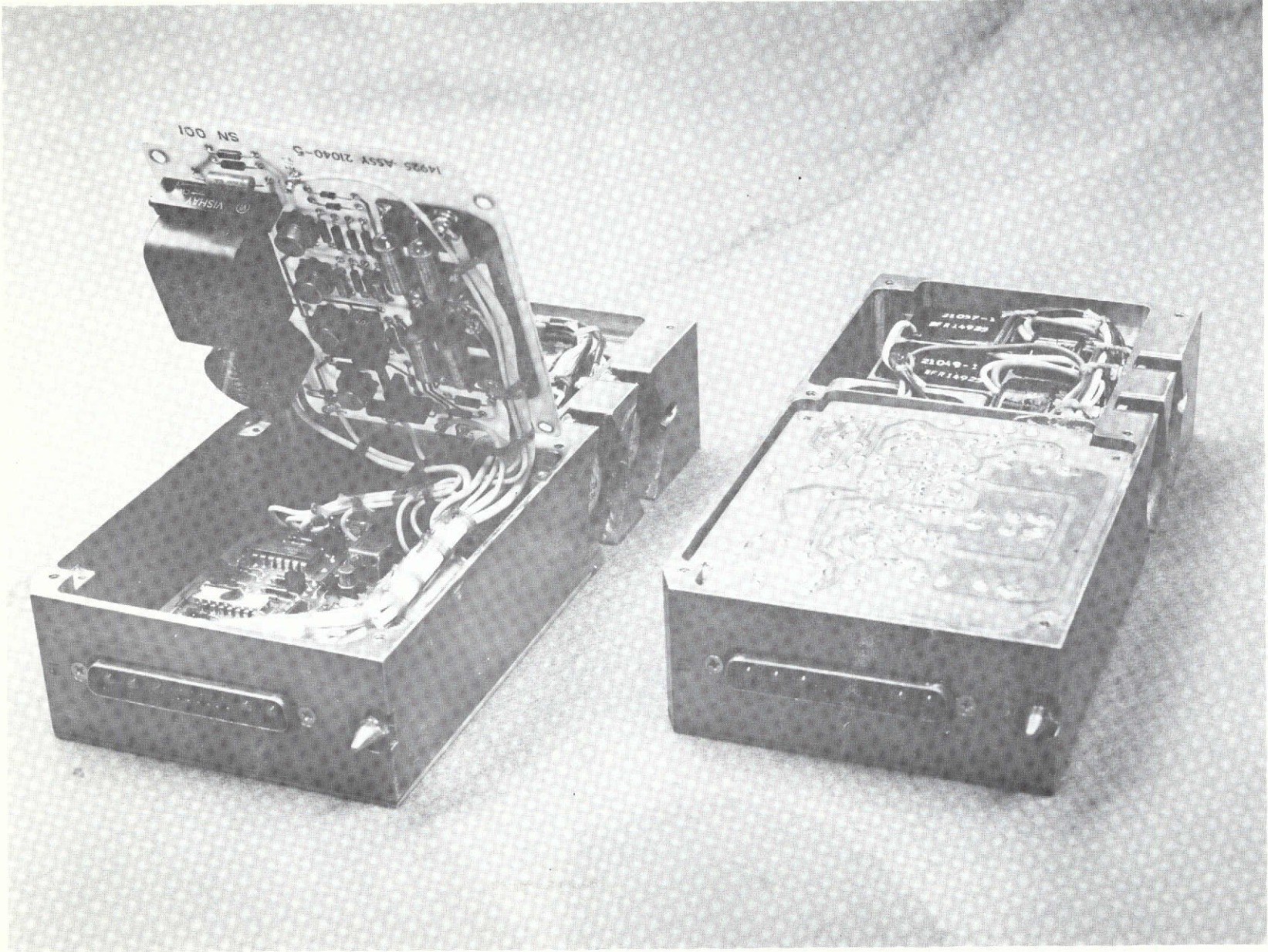FIGURE 3-3.   MULTIPLE OUTPUT POWER SUPPLY PROTOTYPE

FIGURE 3-4. OUTPUT POWER MODULE PROTOTYPE

- Overvoltage/Undervoltage Protection and Monitoring
- Fault Indication
- Short-Circuit Protection
- Weight: 20.6 pounds
- Volume: 410 in^3 including carrier.

3.3.4 Power Supply Operation

The detailed description of the design for the power supply can best be presented by describing its individual elements and their relationship to the operation of the supply. Figures 3-5 and 3-6 show the complete schematic diagrams of a regulator module and the input module. The basic power supply circuit is a push-pull switching regulator. The operation of the regulator module is as follows. The output load current is monitored at the primary winding of the power transformer, T3, via current at transformer CT1. This current is compared at a comparator, U1, with an error feedback voltage. This error voltage, at the output of U2, is proportional to the difference between the output voltage and a reference voltage generated by the reference supply U5. When the load current, which is proportional to the voltage at the comparator across resistor R2, exceeds this error voltage, a pulse is generated at the output of the comparator and supplied to the control logic. This pulse causes the control logic to inhibit the power switch drive for the rest of the cycle. The control logic is then reset by the next clock pulse and the cycle repeats, providing pulsewidth modulation. In essence, the control loop forces the load current to be that value necessary to produce an output voltage equal to the reference voltage.

A more detailed description of each element in the supply is given below.

3.3.4.1 Regulator Module - The regulator module, shown in Figure 3-5, consists of several functional elements which are discussed in the following paragraphs.

3.3.4.1.1 Control Logic - The control logic consists of basically eight nand gates and two J-K flip-flops, shown in Figure 3-5 as U1, U3, and U2. The operation of the circuit is as follows.
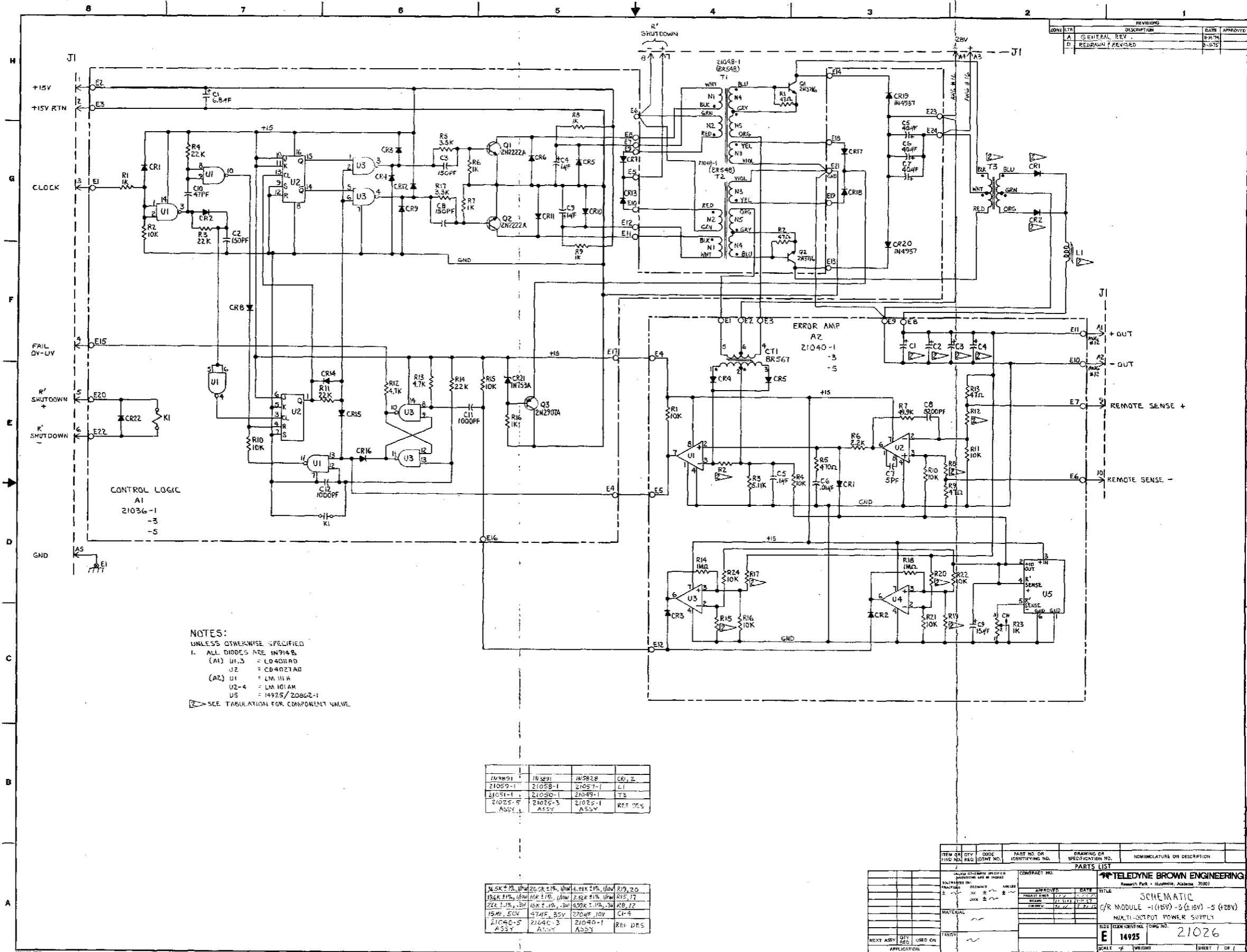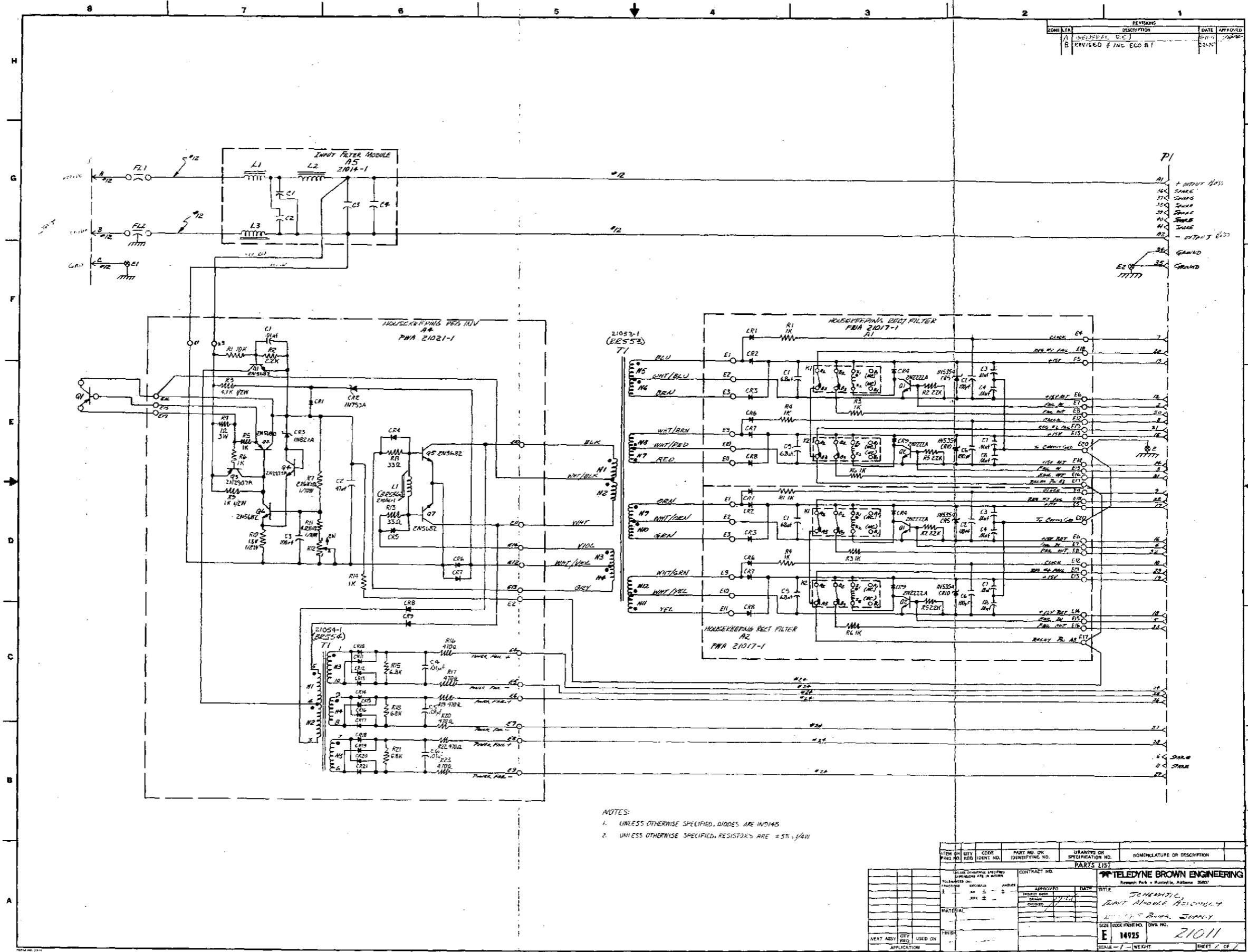
FIGURE 3-5. SCHEMATIC, REGULATOR MODULE, MULTIPLE OUTPUT POWER SUPPLY

FIGURE 3-6. SCHEMATIC, INPUT MODULE, MULTIPLE OUTPUT POWER SUPPLY

FOLDOUT FRAME 1

FOLDOUT FRAME 2

Upon receipt of a positive-going clock at E1, the output of U1 at Pin 3 goes to 0 volt, coupling a negative-going pulse through C10. U1 output responds by providing a positive-going pulse, approximately 1.0 microsecond wide, at Pin 10 which resets flip-flop U2 Pin 1 to 0 volt, causing the outputs of U3 Pins 3 and 4 to become high, inhibiting the base drive to the inverter power switches. Concurrently with this action, C2 discharges through R3 until the threshold voltage of U1 is reached at which time U1 Pin 4 goes high. The time required for this to occur is approximately 3 microseconds. This represents the time delay necessary before the inverter transistor may be turned on after a subsequent cycle assuring that both power transistors will not be on at the same time due to the storage time of these transistors.

When U1 Pin 4 goes high, it clocks the J-K flip-flop U2 Pin 1 high, toggling U2 Pins 15 and 14 and also enables gates U3 such that either Pin 3 or Pin 4 may go to 0 volt, depending on the previous status of U2 Pins 15 and 14, enabling drive to the inverter power transistors. Upon receipt of zero level command from the regulating loop inputted at E4, U1 Pin 11 goes high resetting U2 Pin 1 to 0 volt which inhibits drive to the power transistors for the reset of the clock cycle.

This process is repeated each clock cycle, alternating drive to the two power transistors.

The cross coupled gates U3 Pin 10 and U3 Pin 11 provide the latching function necessary to shut down the supply when an over- or under-voltage command is inputted into E16. When Pin 11 of U3 is in the zero state, the output of Pin 11 is ORed through diode CR16 and thus inhibits the base drive when activated. This latch is reset by initiating the remote shutdown command, energizing relay K1 which closes contact K1.

Transistor Q3 and associated circuitry functions to inhibit the power transistor base drive by shorting the base drive transformer until sufficient voltage is supplied to the control circuitry to assure proper operation during power up or during failures which would cause a loss of this housekeeping voltage.

3.3.4.1.2 <u>Pre-Driver and Driver</u> - The pre-driver and driver cir-
cuitry, shown in Figure 3-5 as part of the control logic section, is
designed around transistors Q1 and Q2 and power transistors Q1 and Q2.
Since this element contains two identical and independent circuits, the
explanation of only one of these circuits will be given, simplifying the
discussion. One of these circuits is redrawn in Figure 3-7 and, for the
purpose of this discussion, is shown with the magnetizing inductance repre-
sented by the base drive transformer (T1) modeled as L_m.

The circuit operation is described as follows. Initially, with
transistor Q1 conducting, the secondary winding is essentially open cir-
cuited, since the base-to-emitter terminals of transistor Q2 are reverse
biased, and current flows in the primary winding (N1). This current,
assuming zero initial conditions, increases at a rate determined by the
inductance of primary winding (N1) and circuit resistance; i.e.,

$$i_m(t) \simeq \frac{V_{in}}{R8} \left\{ [1 - \exp{(-R8/L_m t)}] \right\}$$

where

$\qquad i_m(t)$ -   the magnetizing current flowing in the primary winding
(N1), when Q1 is conducting

$\qquad V_{in}$ -   input voltage to drive circuit

$\qquad t$ -   time.

When Q1 is turned off, which open-circuits the primary winding, the energy
which was stored in the primary magnetizing inductance (L_m) discharges into
the secondary winding. This may be represented as a current flowing out
of the magnetizing inductance, L_m, into the primary winding N1 (into point
3 in Figure 3-7), which causes a current from the secondary winding (N4)
to flow into the base of Q2. This current decays at a rate proportional
to the base-to-emitter voltage of Q2 and can be expressed as

$$i(t) \simeq \left[I_o - \frac{V_{BE}(Q2) \frac{N_1}{N_2}}{L_m} \times t \right] \frac{N_1}{N_2}$$
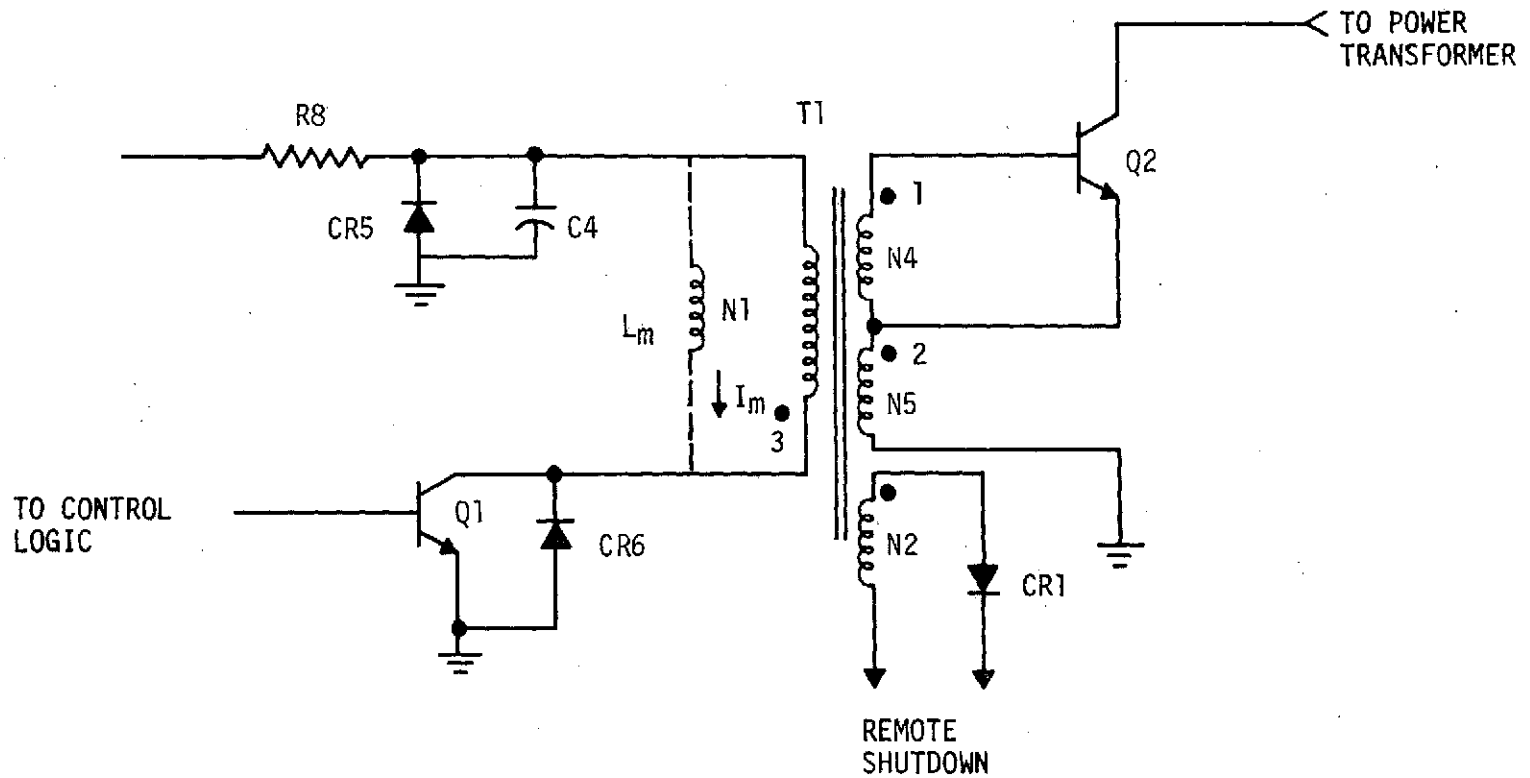
FIGURE 3-7. PRE-DRIVER AND DRIVER CIRCUIT DIAGRAM

where

I_o — value of the magnetizing current immediately before transistor Q1 is turned off [measured at the primary winding (N1)]

$V_{BE(Q2)}$ — base-to-emitter voltage of transistor Q2

L_m — magnetizing inductance measured at the primary winding (N1)

t — time

N_1/N_2 — ratio of the primary to secondary winding

i(t) — the base current flowing into transistor Q2, due to the energy stored in the magnetizing inductance.

The base current into transistor Q2 turns this transistor on, causing collector current to flow through winding N5 of the base drive transformer (T1). This current, flowing in winding N5, causes additional current to flow in the base winding which is proportional to the turns ratio of windings N4 to N5 and the collector current, or

$$I_{b(Q2)} = \frac{N_1}{N_2} (IC_{Q2})$$

where

$I_{b(Q2)}$ — base current of transistor Q2 due to current flow in winding N4

IC_{Q7} — collector current of transistor Q2.

The total current flowing into the base circuit is then the sum of the current provided by the collector current flowing in winding N4 and the current provided by the energy stored in the magnetizing inductance L_m. While transistor Q2 is conducting, the resultant current in the emitted winding of the base drive transformer (N5) causes the voltage measured across the primary winding to be positive at point 3 (Figure 3-7) and capacitor C4 charges toward the input voltage (V_{in}) through resistor R8. When transistor Q1 is turned on, current flows through the primary winding [out of point 3 (Figure 3-7)], from capacitor C4 and resistor R8, drawing

current out of the base of transistor Q2 and turning Q2 off. At the instant that transistor Q1 turns on, this current is large, limited only by the winding resistances, leakage inductances, and impedance of capacitor C4, and provides a large turn-off current at the base of Q1. During the time that transistor Q1 conducts, the magnetizing current again increases, recharging the magnetizing inductance; thus, the cycle repeats.

Diode CR6 is included to protect the circuit for the case when the magnetizing current may reverse direction during operation. Such reverse direction would be caused by start-up transients or during long duty cycle operation at reduced frequencies. If the magnetizing current is flowing in the reverse direction (toward capacitor C4) when transistor Q1 is conducting, diode CR5 provides a path to ground such that this current will discharge into capacitor C4.

Diode CR5 is provided to prevent the inductor-capacitor network formed by the magnetizing inductance (L_m) and capacitor C4 from ringing, which would cause faulty triggering of the output power transistor Q2. Diode CR5 protects the network by preventing the capacitor voltage from going negative, due to magnetizing current; a negative voltage would result in a current flow in the direction to provide base drive for transistor Q2.

3.3.4.1.3 Reference Module - The reference module, shown in Figure 3-5 as U5, consists of a precision series regulator module. This module provides the accurate and extremely stable +10-volt reference source utilized by the error amplifier U2, comparator U1, and overvoltage and undervoltage sensing circuits U4 and U3.

3.3.4.1.4 Error Amplifier and Comparator - The error amplifier and comparator circuitry is shown in Figure 3-5 as operational amplifiers U2 and U1. The error amplifier U2 is operated in the inverting mode. The gain of this amplifier is determined by the ratio of the impedance of the feedback network, R7 and C8, and input resistor R12. This amplifier compares the reference voltage, conditioned by resistors R10 and R8, with the power supply output voltage, which is conditioned by resistor network R12

and R11. This amplifier provides the error feedback voltage, equal to the amplifier gain times the difference between the reference and the output voltage, which is applied to the comparator amplifier U1. The comparator compares this error voltage with the input current to the power transformer, measured by the current transformer CT1 and measured across resistor R2. When this current exceeds the error voltage, the comparator output, Pin 7 of U1, goes low and provides the signal to the control logic necessary to inhibit the drive to the inverter power transistors.

3.3.4.1.5 <u>Overvoltage and Undervoltage Detectors</u> - The fault protection circuitry in the regulator module consists of the overvoltage and undervoltage detectors. This circuit is shown in Figure 3-5 as part of the error amplifier and consists of operational amplifiers U4 and U3.

The overvoltage circuitry, U4, compares the output voltage, conditioned by resistor network R20 and R21, with the reference voltages conditioned by resistor network R22 and R19. When the output voltage exceeds a predetermined value, adjusted by the resistor networks, the output of the operational amplifier, U4, is driven from saturation in the positive direction to saturation in the negative (ground) direction. When this amplifier is driven to ground, it couples a pulse through diode CR2 and capacitor C11 to the shutdown latch in the control logic, initiating a shutdown command.

The undervoltage detector, comprised of operational amplifier U3, operates in a manner similar to the overvoltage circuit. When the output voltage of the power supply decreases below a predetermined value, adjusted by resistors R15, R16, R17, and R24, the output of the operational amplifier is driven to ground initiating a shutdown command to the inverter.

3.3.4.2 <u>Input Module</u> - The input module, shown in Figure 3-6, consists of several functional elements which are discussed in the following paragraphs.

3.3.4.2.1 <u>Input Filter</u> - The input filter is contained in the input module. The filter consists of components L1 through L3, C1 through C4, and feedthrough capacitors FL1 and FL2. This filter is so designed

as to provide the attenuation of the inverter ripple currents necessary to comply with MIL-STD-461, Notice 3.

3.3.4.2.2 Housekeeping Supply - The housekeeping supply is shown in Figure 3-6 as part of the input module. It consists of a series regulator and self-oscillating inverter. The series regulator, consisting of transistors Q2, Q3, Q4, and Q6 and power transistor Q1, preregulates the input line voltage to approximately 20.5 volts, conditioning the power delivered to the housekeeping inverter. The inverter is a self-oscillating, regenerative type, utilizing a pacing core, L1, as the saturating element. This configuration allows relatively high efficiencies as well as a precise switching frequency to be maintained. The inverter provides the four isolated +15-volt supplies as well as the clock signals required by each of the regulator modules. Two of the four clock signals are 180 degrees out of phase with the remaining two which in turn offsets two of the four regulator module switching times, reducing the magnitude of the rms ripple current.

3.3.4.2.3 Fail Circuitry - The failure monitoring circuitry for the input power line as well as the buffer circuitry for the overvoltage and undervoltage monitor is contained in the input module. The input power failure circuitry consists of transistor Q1 and transformer T1 in the housekeeping regulator and inverter section. This circuit monitors the input voltage sensed by resistor network R1 and R2 and transistor Q1 and compares it to the regulated voltage provided at the output of the series regulator. When this voltage is above approximately 22 volts, transistor Q1 turns on, permitting current flow in transformer T1, which is driven by the housekeeping inverter through diodes CR8 and CR9. This transformer provides three isolated +15-volt signals, indicating proper operation of the housekeeping supply as well as the indication that the input power is above the minimum acceptable limit.

The overvoltage and undervoltage buffer circuits are contained in the housekeeping, rectifier, and filter section of the input module. Since the four circuits are identical, it is sufficient to discuss only one.

During an overvoltage/undervoltage condition, a signal is provided by the regulator module, inputted at terminal E7, which turns on transistor Q1, energizing relay K1. With K1 energized, the normally closed contacts open, removing the +15-volt signal (referenced to that regulator module ground) from terminal E8 as well as removing the +20.5-volt signal (referenced to the input ground) from terminal E18, indicating an overvoltage or undervoltage shutdown has occurred to that regulator module.

3.3.5 Recommendations

As noted earlier, the prototype power supply met and in many cases exceeded the design goals established. However, there are several recommendations, based on the evaluation of this prototype, which will improve the general usability and performance of the production power supply. These recommendations are as follows:

- There is a need for a positive alignment of the modules in the carrier to prevent alignment tolerance buildup.

- There is a need for a method of removing the modules from the carrier such as an extraction notch or recessed handle.

- A package redesign to eliminate wasted space and reduce the package wall thickness would significantly reduce the size and weight of the power supply approximately 30 percent.

- EMI filter connectors should be incorporated in order to satisfactorily remove the conducted emissions above 1.0-megahertz frequency range.

- Modification to the overvoltage and undervoltage failure circuit should be made such that any out-of-tolerance of the voltage at the output of the supply should output a fail signal. The fail signal, as presently configured, is not present during initial startup when a short circuit exists.

- Higher current switching transistors should be incorporated into the design to afford higher efficiency, due to improved saturation losses, and improved reliability, due to a reduced stress factor.

- The design specification limits for the power
  supply performance can be improved as follows:

  ▲ Initial Tolerance (output voltage):
     ± 0.1% max.

  ▲ Maximum Allowable Transient Voltage:
     20% max.

  ▲ Maximum Allowable Transient Recovery Time:
     2.0 msec

  ▲ Line Regulation: ± 0.05% max.

  ▲ Load Regulation: ± 0.05% max.

  ▲ Temperature Coefficient: 0.001%/°C

  ▲ Maximum Allowable Output Voltage Error:
     ± 0.5%

  ▲ Input/Output Isolation: 200 Mohm

  ▲ Isolation Between Output Commons: 200 Mohm.

3.3.6 Conclusions

Most of the existing power supplies are of antiquated designs
which are not compatible with the requirements of modern electronic equip-
ment. In recent years, however, some of these supplies have achieved a
high degree of performance improvement and miniaturization through the
use of solid-state and integrated circuits. Although design variations
are unlimited, most of these designs incorporate power conversion circuits
which are conventional. Also, as new user requirements are established,
new power supplies are developed, causing a proliferation of hardware,
having no commonality, which places a burden on the logistics system and
amplifier problems in maintenance and supply.

To correct these deficiencies in the supply system, a new genera-
tion of power supply equipment must be made available. Design of this
new power conversion equipment must utilize advanced power processing tech-
niques capable of size, weight, cost, and performance improvement consis-
tent with gains achieved in the design utilization equipment.

The establishment of a standard power supply, whereby a few general purpose power supply units could satisfy a significant portion of the power needs of user systems, would reduce supply and support problems and afford the general economic advantages of standardization to the logistics system.

To realize the advantages of the standardization concept, a standard power supply concept was proposed by MSFC. A study program was initiated by MSFC to develop a design concept for a fully militarized standard general purpose power unit. This study effort was extended, by this contract, to develop a prototype of a power supply which would fulfill these requirements. The effort has shown that a standard design configuration for a universal power supply would fulfill the needs of a high percentage of users in future programs. The resulting standard design demonstrated that a significant reduction in cost and weight and an increase in reliability and performance would be realized by such an approach.

Classification of this power supply will permit standardization for assignment of equipment to systems and equipment applications and will reduce the proliferation of special purpose units abounding in the supply system.

REFERENCE

1.   "Power Supply Standardization and Optimization Study", Teledyne
      Brown Engineering Final Report SE-MSFC-1600, July 1972

APPENDIX A.   SUMMARY OF PERFORMANCE
CHARACTERISTICS OF "THE POWER SUPPLY
STANDARDIZATION AND OPTIMIZATION
STUDY" BREADBOARD

TABLE A-1. POWER SUPPLY PERFORMANCE CHARACTERISTICS

ITEM	DATA
Efficiency	86%[1]
Line Regulation	< 0.02%
Load Regulation	< 0.02%
Output Ripple and Noise	25 mV p-p
Input Ripple and Noise	6 mA p-p[2]
Worst-Case Step Load Transient	1.2 V [3]

NOTES:

[1]Measured at full load, 80-volt input
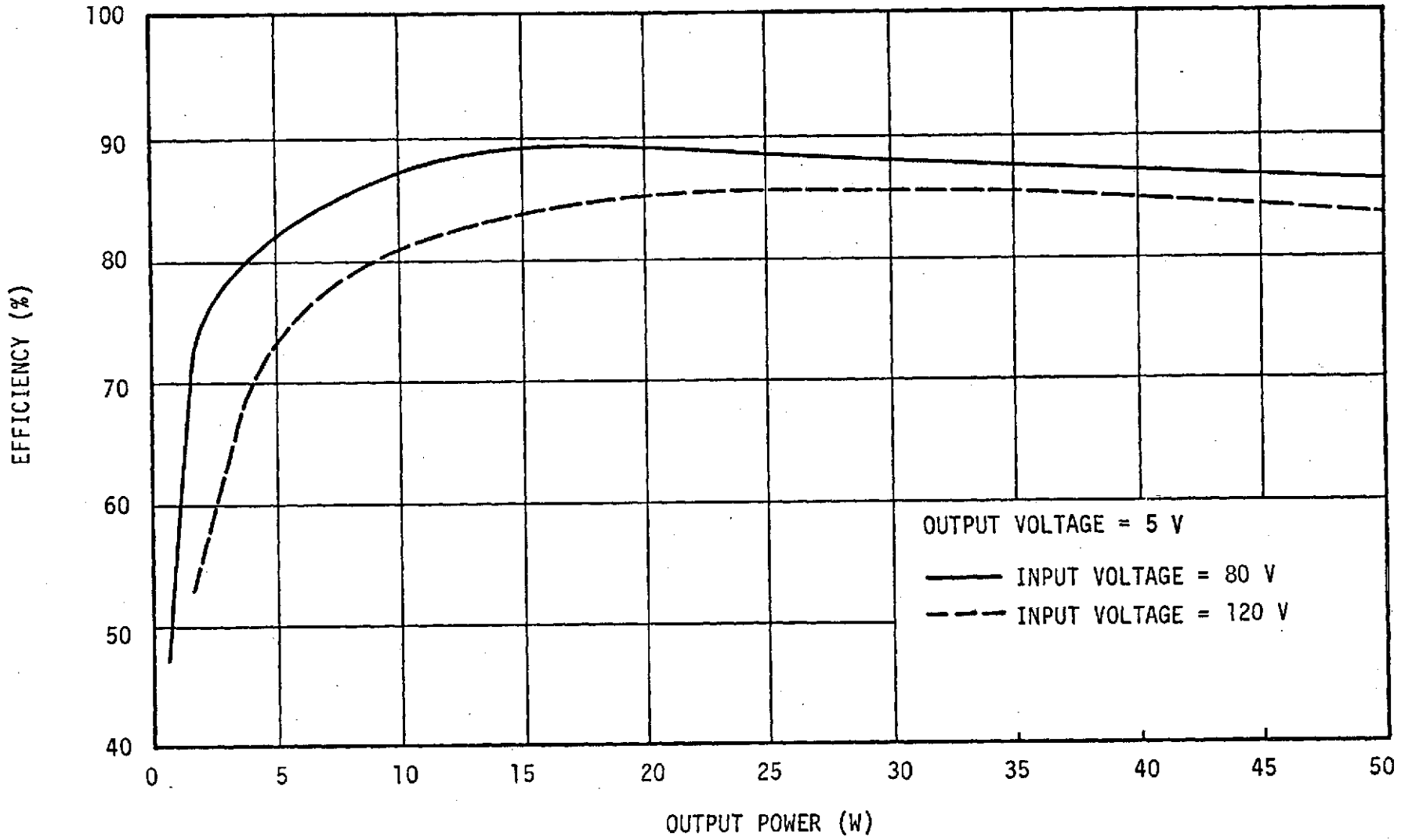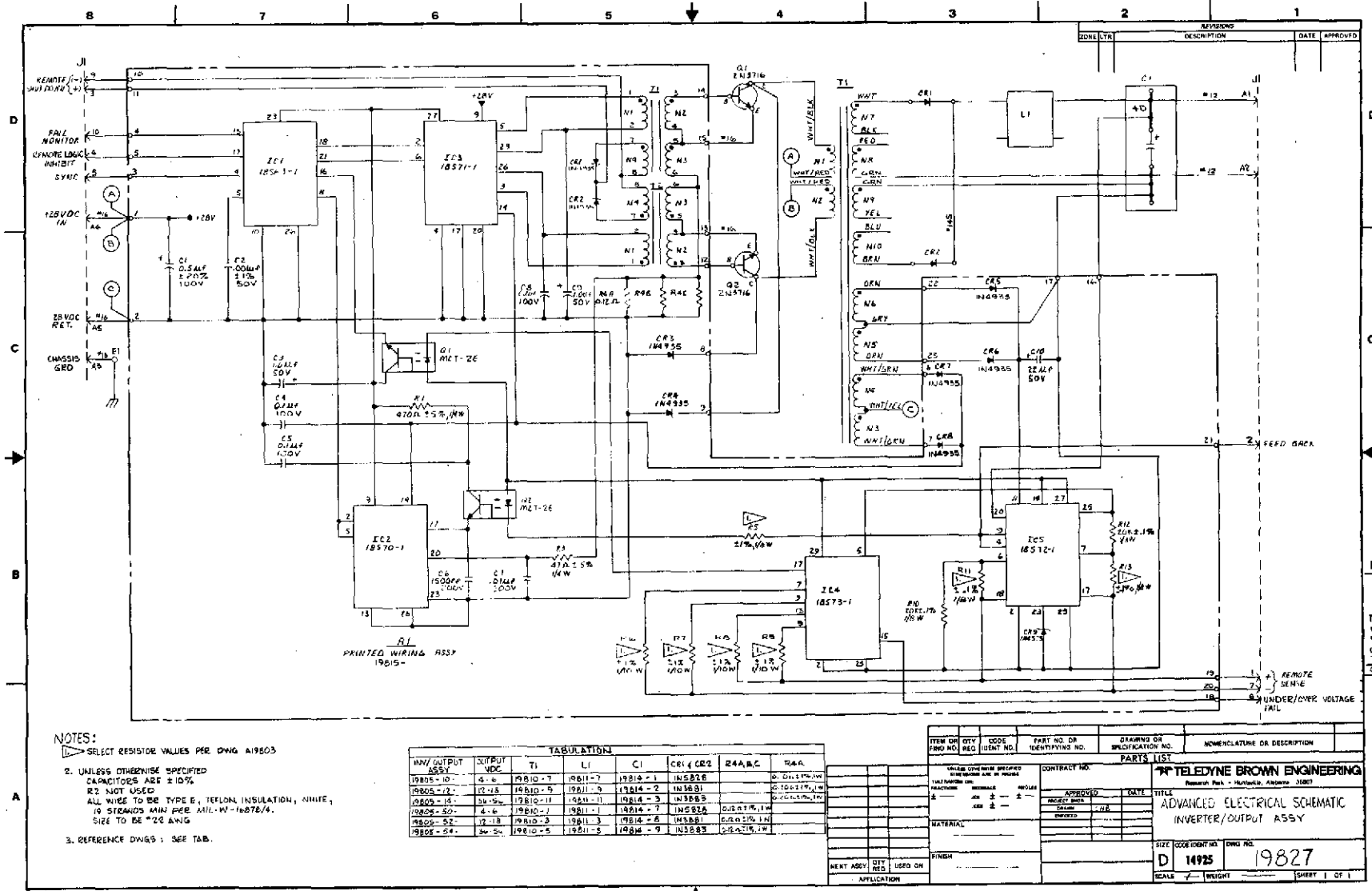[2]Without input EMI filter
[3]No load to full load (settling time 1.0 msec)

FIGURE A-1. EFFICIENCY AS A FUNCTION OF OUTPUT POWER LEVEL

APPENDIX B. HYBRIDIZE POWER SUPPLY
CIRCUIT DESIGN

NOTES:
1. SELECT RESISTOR VALUES PER DWG A19803

2. UNLESS OTHERWISE SPECIFIED
   CAPACITORS ARE ±10%
   R2 NOT USED
   ALL WIRE TO BE TYPE E, TEFLON INSULATION, WHITE,
   19 STRANDS MIN PER MIL-W-16878/4.
   SIZE TO BE #22 AWG

3. REFERENCE DWGS: SEE TAB.

TABULATION

INV/OUTPUT ASSY	OUTPUT VDC	T1	L1	C1	CR1 & CR2	Z4 A,B,C	R4A
19805-10-	4-6	19810-7	19811-7	19814-1	1N5826		0.1±2.1%,1W
19805-12-	12-18	19810-9	19811-9	19814-2	1N3881		0.1±2.1%,1W
19805-14-	50-54	19810-11	19811-11	19814-3	1N3883		0.20±2.1%,1W
19805-50-	4-6	19810-1	19811-1	19814-7	1N5826	0.18±1%,1W	
19805-52-	12-18	19810-3	19811-3	19814-8	1N3881	0.20±1%,1W	
19805-54-	50-54	19810-5	19811-5	19814-9	1N3883	0.20±1%,1W	

PARTS LIST

TELEDYNE BROWN ENGINEERING
Research Park - Huntsville, Alabama 35807

TITLE
ADVANCED ELECTRICAL SCHEMATIC
INVERTER/OUTPUT ASSY

SIZE	CODE IDENT NO.	DWG NO.
D	14925	19827

SCALE / WEIGHT —— SHEET 1 OF 1

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	GENERAL CHANGES	1-8-74	

DISCRETE COMPONENT LIST
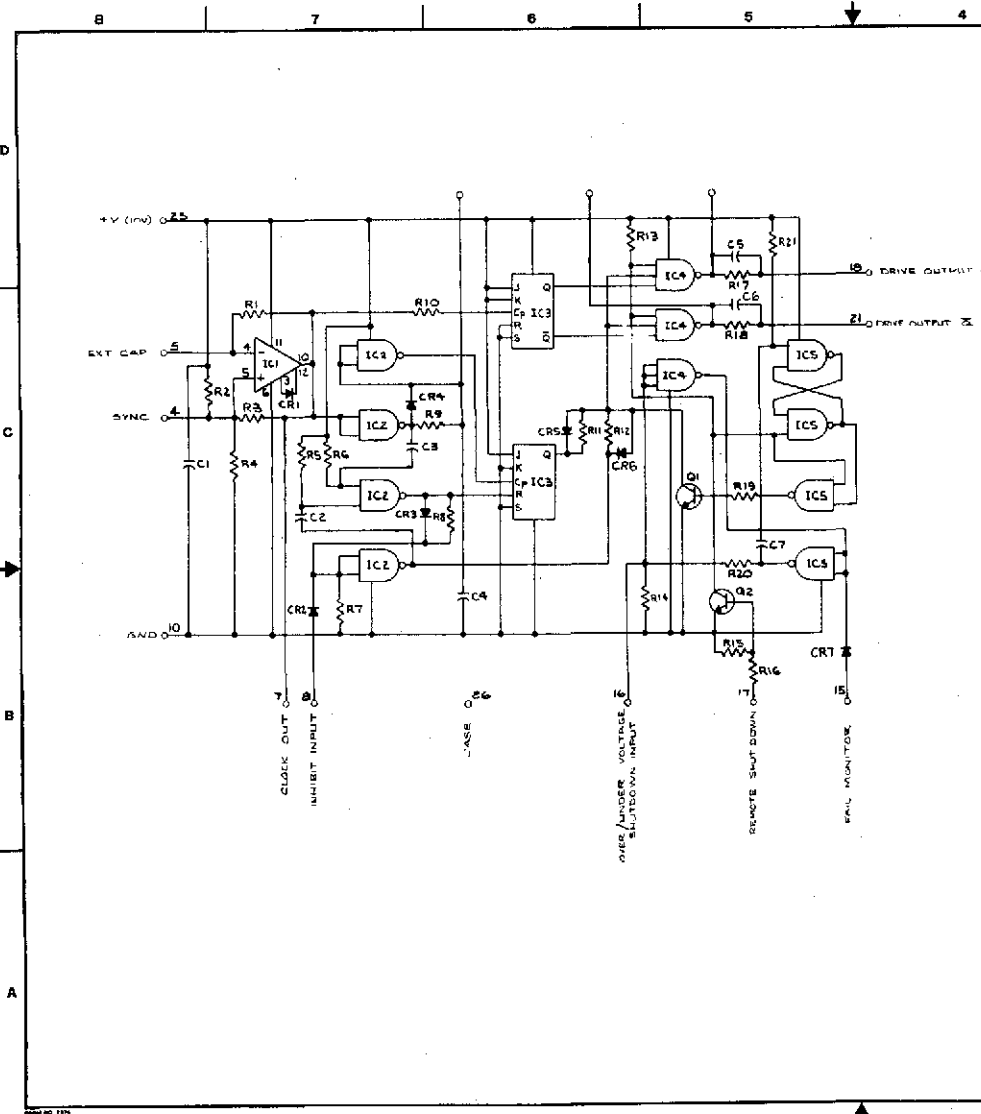
REF DES	PART NO.	MFR.	DESCRIPTION	MAX POWER DISS.
C1			CAP, .01uF, ±20, 25V	
C2			50PF ± 20%, 25V	
C3			50PF ± 20%, 25V	
C4			75 PF ± 20%, 25V	
C5			50PF ± 20%, 25V	
C6			50PF ± 20%, 25V	
C7			CAP, 150PF ± 20%, 25V	
CR1	1N3604	G.E.	DIODE	1.0 MW
CR2				
CR3				
CR4				
CR5				
CR6				
CR7	1N3604	G.E.	DIODE	1.0MW
IC1	HGA77N851L	FAIRCHILD	INTEGRATED CIRCUIT	21 MW
IC2	CD4011AD	RCA		1.0MW
IC3	CD4027AD			1.2 MW
IC4	CD4023AD			1.0 MW
IC5	CD4011AD	RCA	INTEGRATED CIRCUIT	1.0MW
Q1	2N2222A	MOT	TRANSISTOR	1.0MW
Q2	2N2222A	MOT	TRANSISTOR	1.0 MW
R1			RES, 14K ± 1%	70 MW
R2			20K ± 1%	2.25MW
R3			20K ± 1%	2.25MW
R4			70K ± 1%	1.9 MW
R5			20K ± 5%	1.0 MW
R6			20K ± 5%	1.0MW
R7			20K ± 10%	5.0MW
R8			10K ± 10%	1.0MW
R9			51K ± 5%	1.0MW
R10			20K ± 10%	1.0MW
R11			20K ± 10%	5.0MW
R12			20K ± 10%	5.0MW
R13			20K ± 10%	5.0MW
R14			51K ± 5%	1.0MW
R15			4.7K ± 10%	1.0MW
R16			4.7K ± 10%	5.0MW
R17			4.7K ± 5%	21 MW
R18			4.7K ± 5%	21 MW
R19			20K ± 10%	5.0MW
R20			RES, 1.0M ± 10%	1.0MW

NOTES:
1. SOURCE:
   APPLIED TECHNOLOGY
   PALO ALTO, CAL
2. APPLIED TECHNOLOGY DWG
   22-026708

+V (10V)
EXT CAP
SYNC
GND
CLOCK OUT
INHIBIT INPUT
CASE
OVER/UNDER VOLTAGE SHUTDOWN INPUT
REMOTE SHUT DOWN
FAIL MONITOR
DRIVE OUTPUT ɸ
DRIVE OUTPUT ɸ̄

PARTS LIST

ITEM OR FIND NO.	QTY REQD	CODE IDENT NO.	PART NO. OR IDENTIFYING NO.	DRAWING OR SPECIFICATION NO.	NOMENCLATURE OR DESCRIPTION

TELEDYNE BROWN ENGINEERING
Research Park – Huntsville, Alabama 35807

TITLE: INTEGRATED CIRCUIT OSCILLATOR & CONTROL LOGIC

SIZE	CODE IDENT NO.	DWG NO.
D	14925	18569
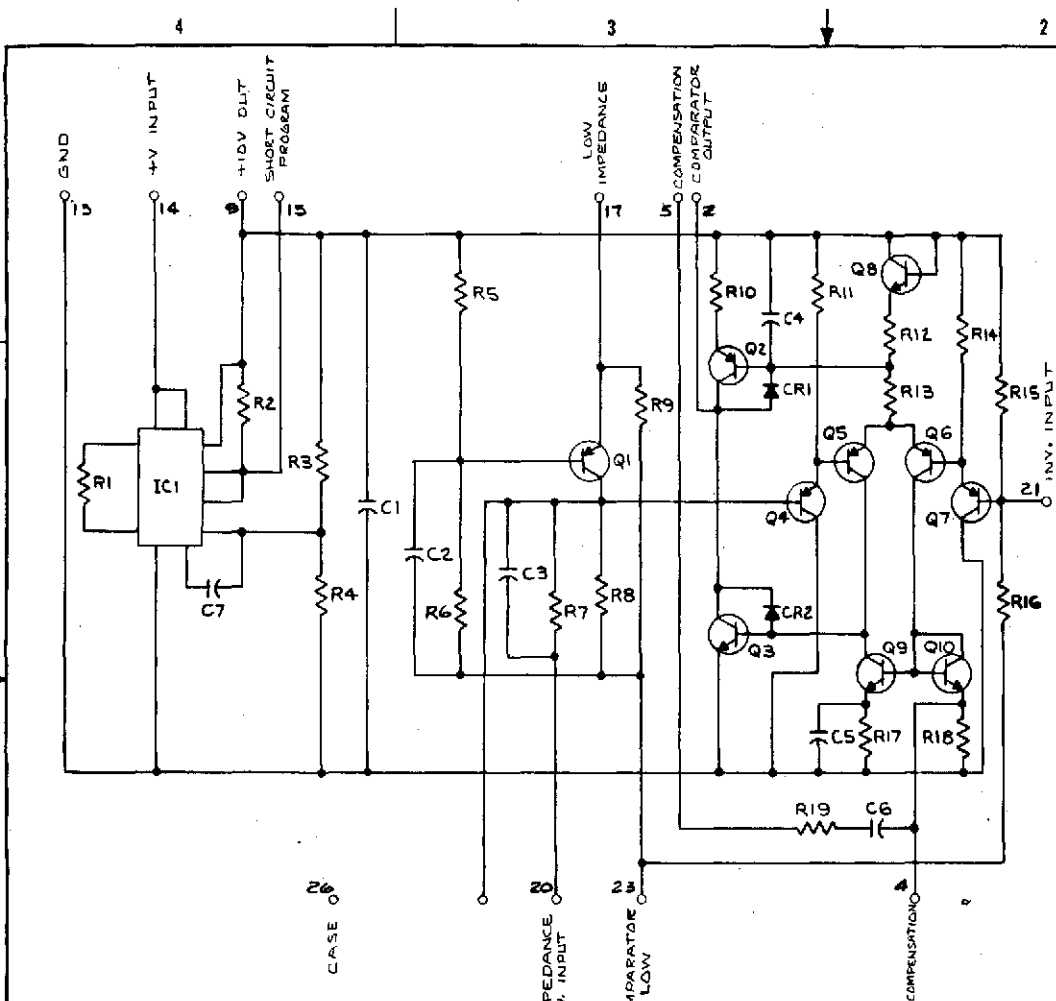
SCALE - / WEIGHT — SHEET 1 OF 1

DISCRETE COMPONENT LIST

REF DES	PART NO.	MFR	DESCRIPTION	MAX POWER DISS.
C1			CAP.,.01µf±20%,25V	
C2			.01µf±20%,25V	
C3			100pf±20%,25V	
C4			1800pf±20%,25V	
C5			150pf±20%,25V	
C6			500pf±20%,25V	
C7			CAP.,100pf±20%,25V	
CR1	FH1200	FAIRCHILD	DIODE	5.0 MW
CR2	FH1200	FAIRCHILD	DIODE	5.0 MW
IC1	USR7723312	FAIRCHILD	INTEGRATED CIRCUIT	380 MW
Q1	2N2907A	MOT	TRANSISTOR	1.5 MW
Q2	2N2907A	MOT		50 MW
Q3	CA3045(1/5)	RCA		5.0 MW
Q4	2N2907A	MOT		140 µW
Q5	2N4959	MOT		1.6 MW
Q6	2N4959	MOT		1.6 MW
Q7	2N2907A	MOT		140 µW
Q8	CA3045(1/5)	RCA		820 µW
Q9	CA3045(1/5)	RCA		820 µW
Q10	CA3045(1/5)	RCA	TRANSISTOR	820 µW
R1			RES.,5.6K±10%	1.0 MW
R2			15Ω±2%	43 MW
R3			7.5K±1%	1.5 MW
R4			22K±1%	2.2 MW
R5			75K±5%	800 µW
R6			20K±5%	200 µW
R7			1.0K±1%	40 µW
R8			49K±1%	100 µW
R9			52K±5%	18 µW
R10			120Ω±5%	720 µW
R11			150K±10%	660 µW
R12			510Ω±5%	180 µW
R13			10K±5%	4.5 MW
R14			150K±10%	660 µW
R15			49K±1%	2.0 MW
R16			1.0K±1%	40 µW
R17			510Ω±5%	45 µW
R18			510Ω±5%	45 MW
R19			RES.,33K±10%	1.0 MW

NOTES:
1. SOURCE:
   APPLIED TECHNOLOGY
   PALO ALTO, CAL
2. APPLIED TECHNOLOGY DWG
   32-026710

B-4

C 18570

B-5

NOTES:

1. SOURCE:
   APPLIED TECHNOLOGY
   PALO ALTO, CAL
2. APPLIED TECHNOLOGY DWG 32-026712

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	GENERAL CHANGES	1-8-74	

DISCRETE COMPONENT LIST

REF DES	PART NO.	MFR	DESCRIPTION	MAX POWER DISS.
CR1	1N3604	G.E.	DIODE	30 MW
CR2	1N5231B	MOT	DIODE, ZENER	5.0 MW
CR3	1N3604	G.E.	DIODE	9.0 MW
CR4	1N3604	G.E.	DIODE	7.5 MW
CR5	1N3604	G.E.	DIODE	9.0 MW
CR6	1N3604	G.E.	DIODE	7.5 MW
CR7	1N3604	G.E.	DIODE	2.0 MW
CR8	1N3604	G.E.	DIODE	2.0 MW
Q1	2N3439	RCA	TRANSISTOR	65 MW
Q2	2N3439	RCA	TRANSISTOR	3.6 W
Q3	2N3439	RCA	TRANSISTOR	1.0 MW
Q4	2N3439	RCA	TRANSISTOR	3.0 MW
Q5	2N2222A	MOT	TRANSISTOR	9.6 MW
Q6	2N2222A	MOT	TRANSISTOR	9.6 MW
R1			RES., 68K ±10%	10 MW
R2			RES., 12Ω ±5%	30 MW
R3			RES., 12K ±10%	18 MW
R4			RES., 13.3K ±1%	20 MW
R5			RES., 10.5K ±1%	3.0 MW
R6			RES., 1.5K ±10%	66 MW
R7			RES., 1.5K ±10%	66 MW

C18571

PARTS LIST

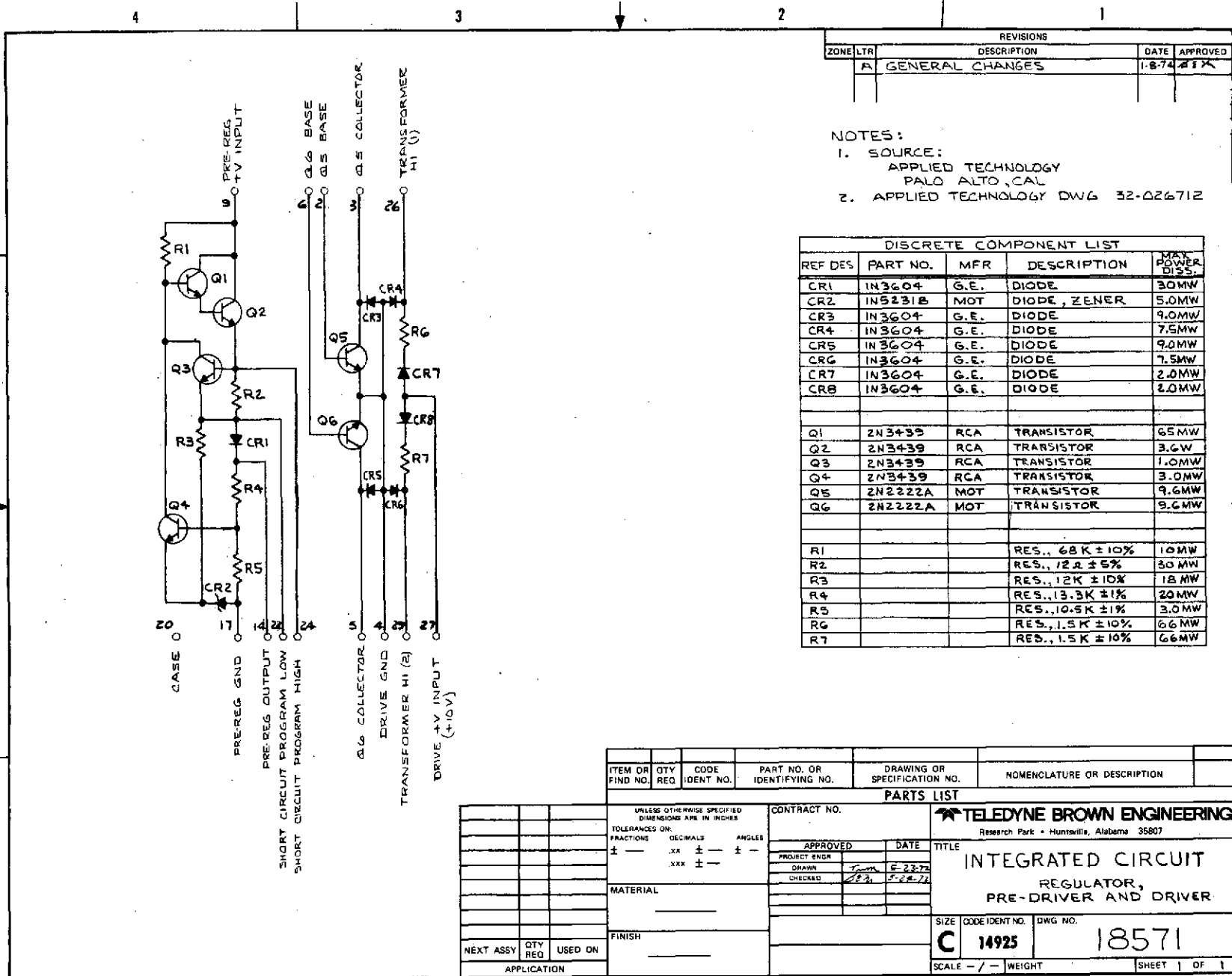| ITEM OR FIND NO.	QTY REQ	CODE IDENT NO.	PART NO. OR IDENTIFYING NO.	DRAWING OR SPECIFICATION NO.	NOMENCLATURE OR DESCRIPTION

TELEDYNE BROWN ENGINEERING
Research Park • Huntsville, Alabama 35807

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON:
FRACTIONS ± — DECIMALS .XX ± — .XXX ± — ANGLES ± —

CONTRACT NO.

APPROVED	DATE
PROJECT ENGR	
DRAWN	6-23-72
CHECKED	5-28-74

TITLE

INTEGRATED CIRCUIT
REGULATOR,
PRE-DRIVER AND DRIVER

MATERIAL

FINISH

SIZE	CODE IDENT NO.	DWG NO.
C	14925	18571

SCALE — / — | WEIGHT | SHEET 1 OF 1
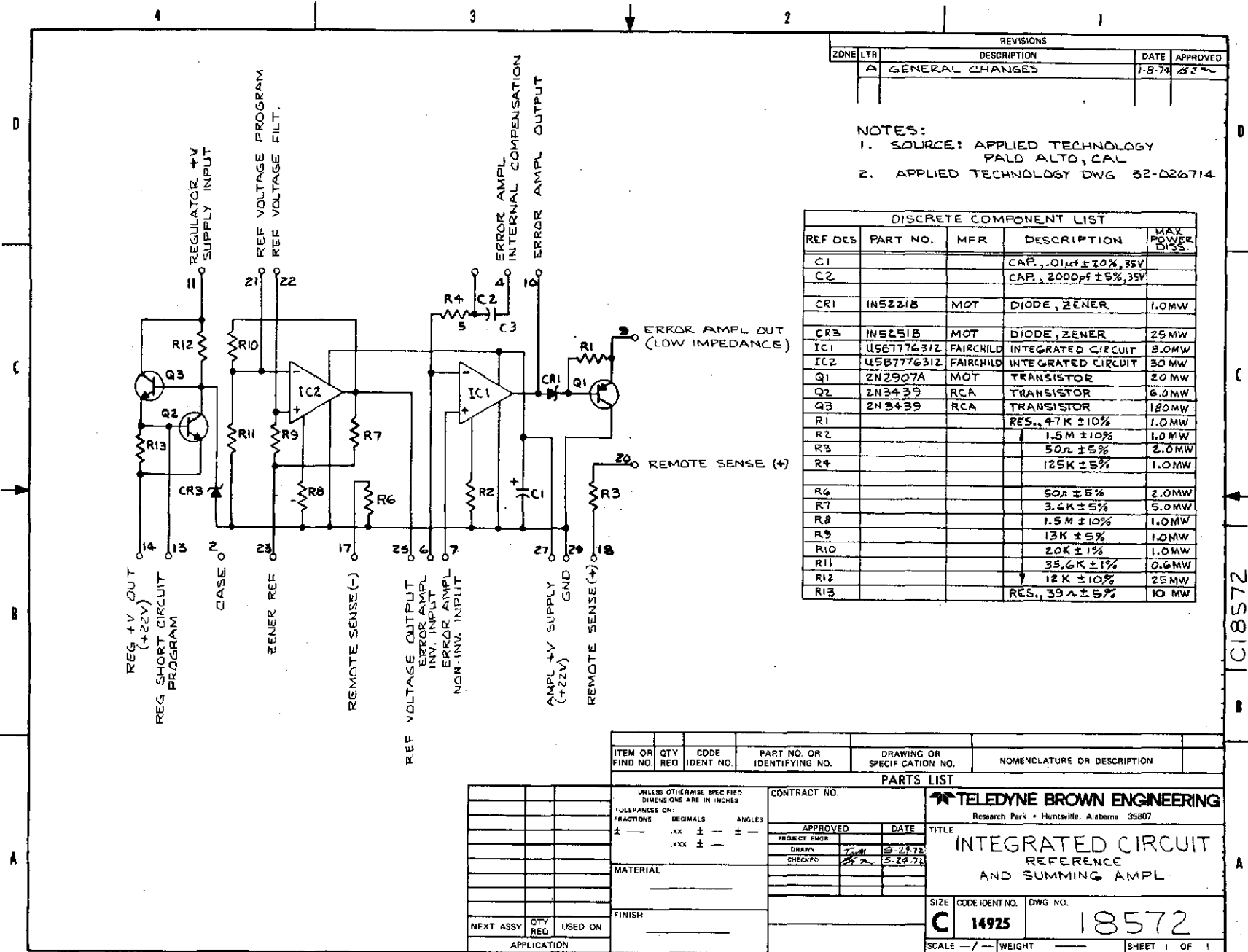
NEXT ASSY | QTY REQ | USED ON
APPLICATION

FORM NO. 2372

B-6

IC18572

NOTES:
1. SOURCE: APPLIED TECHNOLOGY PALO ALTO, CAL
2. APPLIED TECHNOLOGY DWG 32-026714

DISCRETE COMPONENT LIST				
REF DES	PART NO.	MFR	DESCRIPTION	MAX POWER DISS.
C1			CAP., .01µf ±20%, 35V	
C2			CAP., 2000pf ±5%, 35V	
CR1	1N5221B	MOT	DIODE, ZENER	1.0 MW
CR3	1N5251B	MOT	DIODE, ZENER	25 MW
IC1	USB7776312	FAIRCHILD	INTEGRATED CIRCUIT	8.0 MW
IC2	USB7776312	FAIRCHILD	INTEGRATED CIRCUIT	30 MW
Q1	2N2907A	MOT	TRANSISTOR	20 MW
Q2	2N3439	RCA	TRANSISTOR	6.0 MW
Q3	2N3439	RCA	TRANSISTOR	180 MW
R1			RES., 47K ±10%	1.0 MW
R2			1.5M ±10%	1.0 MW
R3			50Ω ±5%	2.0 MW
R4			125K ±5%	1.0 MW
R6			50Ω ±5%	2.0 MW
R7			3.6K ±5%	5.0 MW
R8			1.5M ±10%	1.0 MW
R9			13K ±5%	1.0 MW
R10			20K ±1%	1.0 MW
R11			35.6K ±1%	0.6 MW
R12			12K ±10%	25 MW
R13			RES., 39Ω ±5%	10 MW

Schematic labels:

REGULATOR +V SUPPLY INPUT
REF VOLTAGE PROGRAM
REF VOLTAGE FILT.
ERROR AMPL INTERNAL COMPENSATION
ERROR AMPL OUTPUT
ERROR AMPL OUT (LOW IMPEDANCE)
REMOTE SENSE (+)

REG +V OUT (+22V)
REG SHORT CIRCUIT PROGRAM
CASE
ZENER REF
REMOTE SENSE (-)
REF VOLTAGE OUTPUT
ERROR AMPL INV. INPUT
ERROR AMPL NON-INV. INPUT
AMPL +V SUPPLY (+22V)
GND
REMOTE SENSE (+)

Components: R12, R10, R11, R9, R8, R7, R6, R13, CR3, Q3, Q2, IC2, IC1, R4, C2, C3, R2, C1, CR1, Q1, R1, R3

4　　　3　　　2　　　1

NOTES:
1. SOURCE: APPLIED TECHNOLOGY
　　　　　　　PALO ALTO, CAL
2. APPLIED TECHNOLOGY DWG 32-026716

+V REF
OVERVOLTAGE PROGRAM
OVERVOLTAGE OUTPUT
UNDERVOLTAGE PROGRAM (+)
+V INPUT (+22V)
UNDERVOLTAGE OUTPUT
OVER/UNDER-VOLTAGE FAIL INPUT

OVERVOLTAGE PROGRAM (-)
UNDERVOLTAGE PROGRAM (-)
FAIL MONITOR
CASE

GND

DISCRETE COMPONENT LIST				
REF DES	PART NO.	MFR	DESCRIPTION	MAX POWER DISS
C1			CAP, .01μF ±20%, 35V	
C2			CAP, 100pF ±5%, 35V	
CR1	1N5231B	MOT	DIODE, ZENER	2.5MW
CR2	1N3604	G.E.	DIODE	1.0MW
CR3	1N3604	G.E.	DIODE	1.0MW
CR4	1N5231B	MOT	DIODE, ZENER	2.0MW
IC1	USB7776312	FAIRCHILD	INTEGRATED CIRCUIT	12MW
IC2	USB7776312	FAIRCHILD	INTEGRATED CIRCUIT	20MW
Q1	2N2222A	MOT	TRANSISTOR	2.0MW
Q2	2N2222A	MOT	TRANSISTOR	2.0MW
R1			RES, 60K ±10%	5.0MW
R2			7.5K ±5%	70MW
R3			30K ±10%	12MW
R4			10M ±10%	1.0MW
R5			50K ±10%	12MW
R6			20K ±1%	5.0MW
R7			10M ±10%	1.0MW
R8			20K ±1%	5.0MW
R9			20K ±1%	1.6MW
R10			20K ±1%	1.6MW
R11			60K ±10%	1.0MW
R12			RES, 30K ±5%	16MW

C 18573

PRE-REGULATOR AND COMPARATOR HYBRID
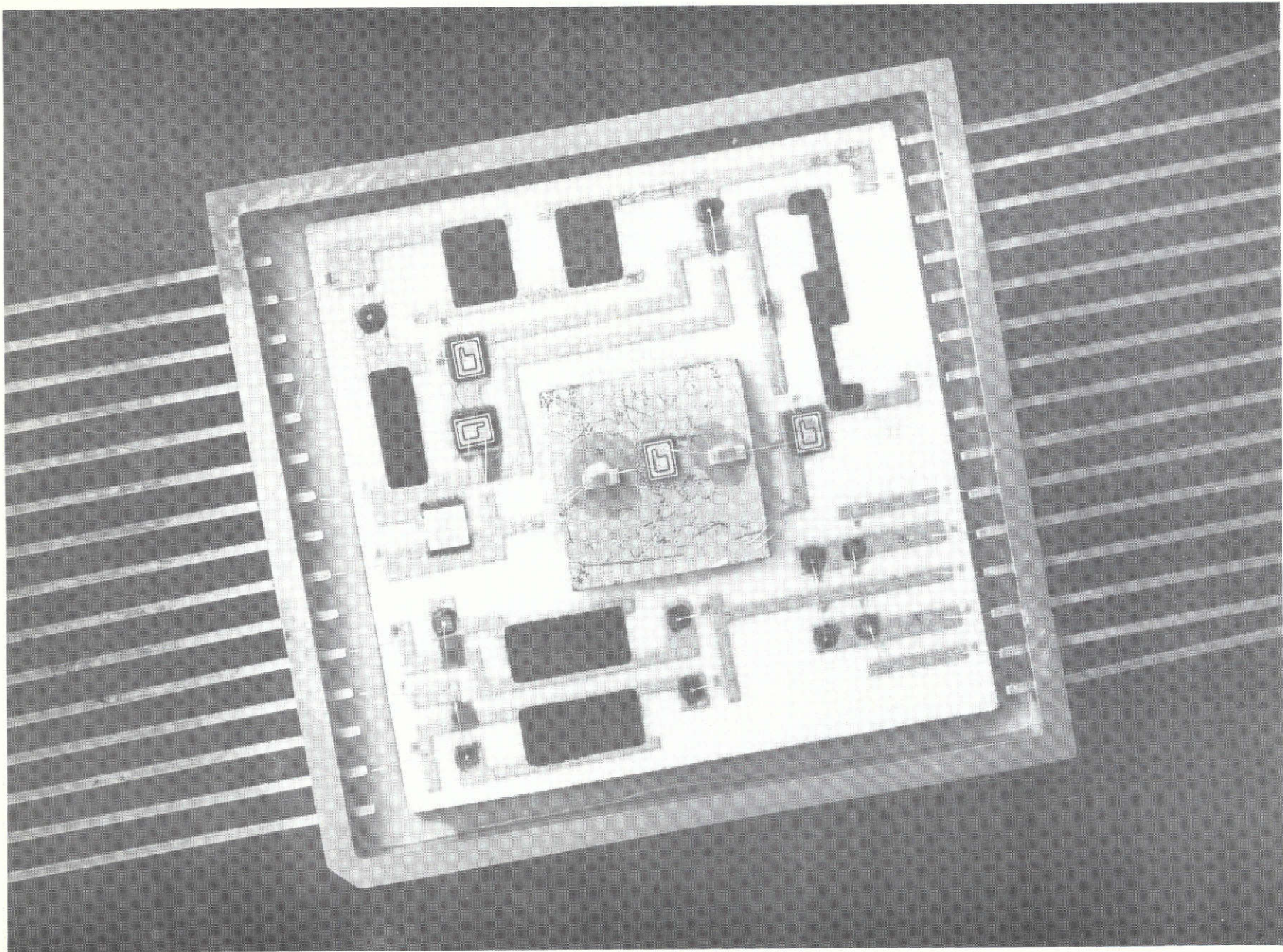
REGULATOR, PRE-DRIVER AND DRIVER HYBRID
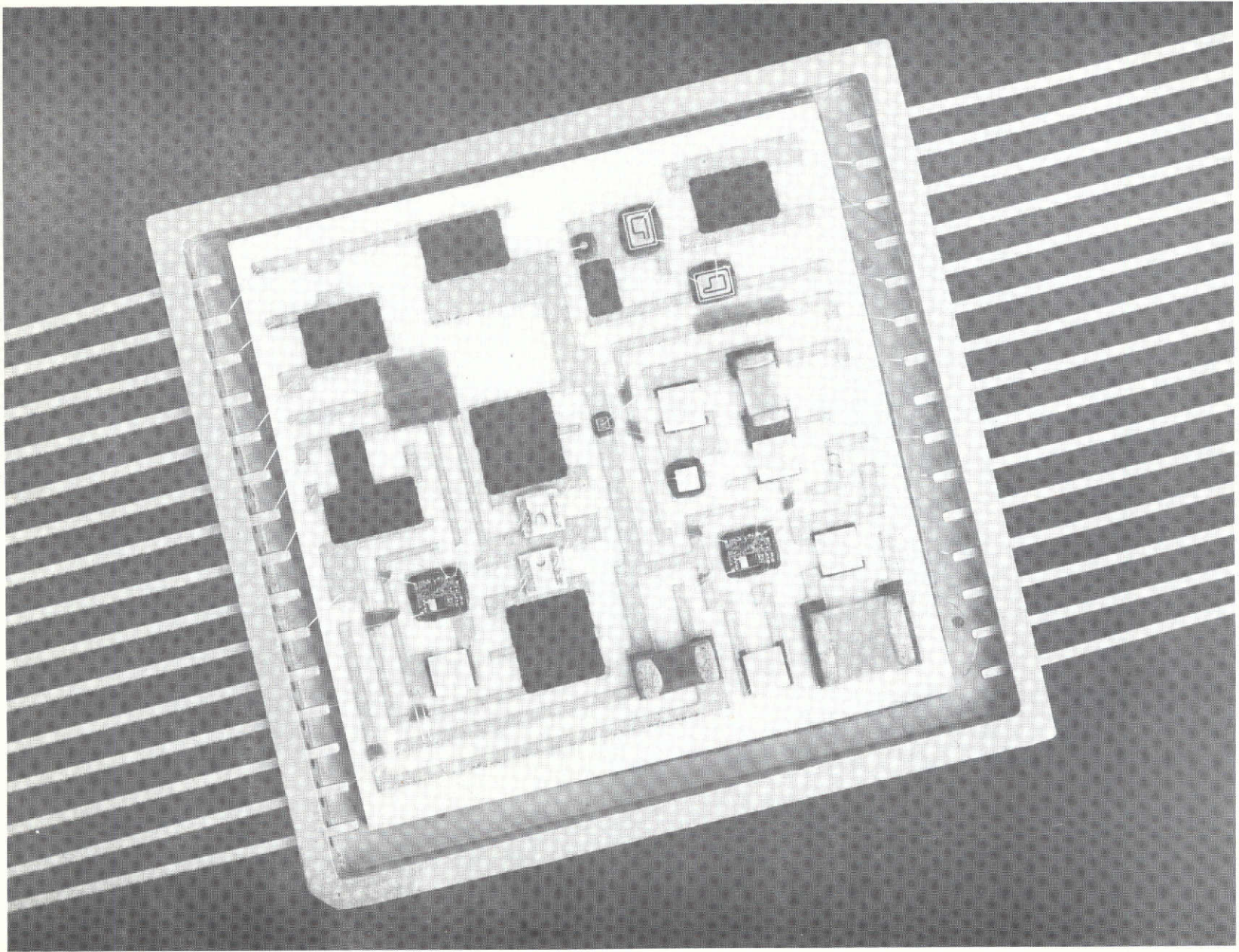
REFERENCE AND SUMMING AMPLIFIER HYBRID
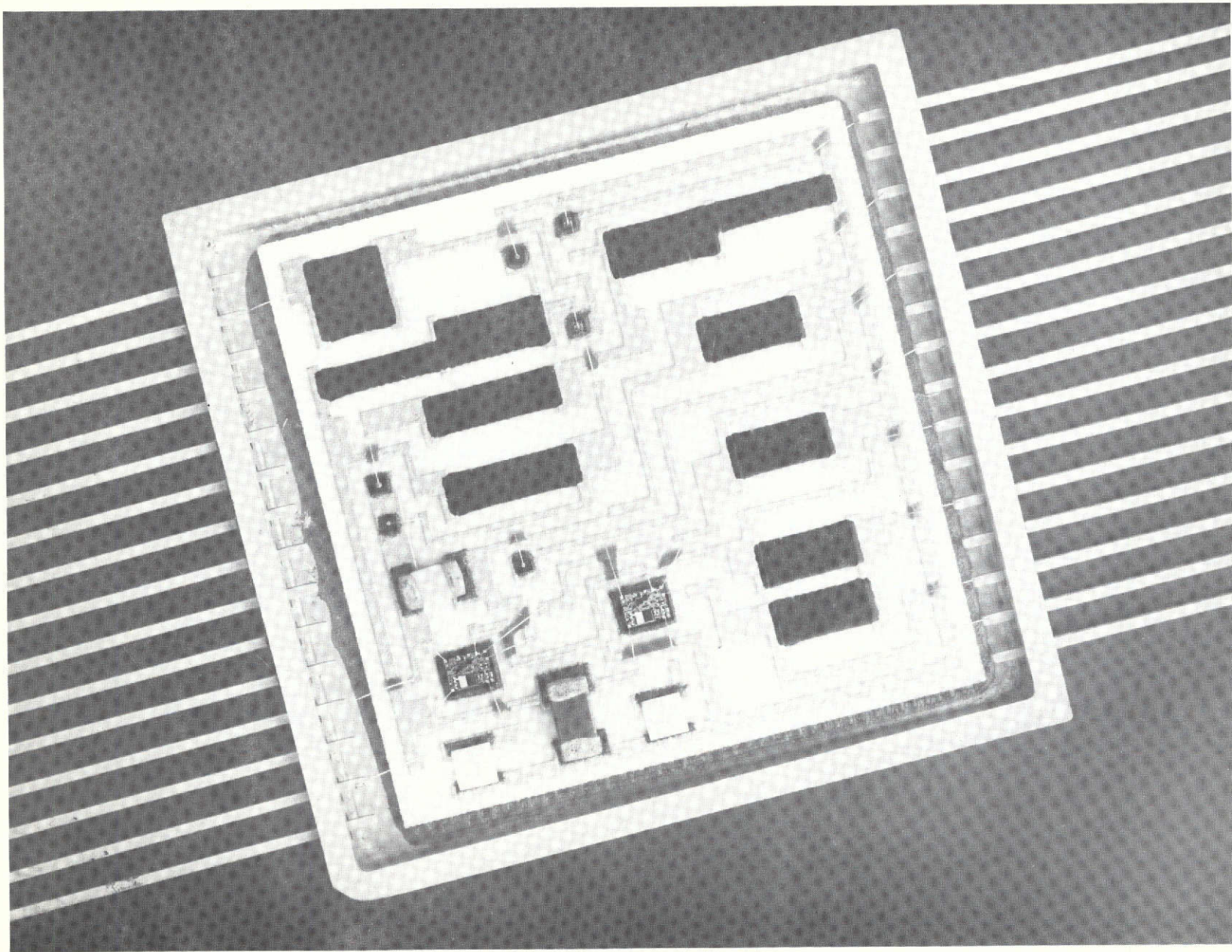
OVERVOLTAGE AND UNDERVOLTAGE DETECTOR HYBRID

APPENDIX C. HYBRID DESIGN SPECIFICATIONS

1. GENERAL DESIGN SPECIFICATIONS

1.1 Components

1.1.1 Resistors - All resistors specified in the parts list as being ± 1% tolerance shall have a ratio of ± 1% with an absolute value tolerance of ± 10%, unless otherwise specified.

Unless otherwise specified, the temperature coefficient of resistors shall be:

- ± 1% tolerance resistors shall track within 50 ppm

- ± 5% tolerance resistors shall have an absolute TCR of less than 150 ppm

- Megohm-type resistors shall have a basic value and a TCR such that the net reistor value does not exceed the tolerance specified over temperature.

1.1.2 Capacitors - Capacitors specified by ± 5% tolerance shall have a temperature coefficient of $\leq$ 200 ppm/°C.

1.1.3 Transistors and Integrated Circuits - The vendors specified in the parts list are for convenience and it is not required that the devices manufactured by these vendors be purchased. The devices purchased, however, must be compatible with the specifications designated by these specified vendors.

1.1.4 Diodes - The 1N3604 diodes specified in the parts list may be substituted by 1N914 diodes. Substitutions for diodes (zeners) may be made, provided equivalent devices are utilized.

NOTE

All device substitutions are subject to TBE approval.

1.2 Operating Temperature

- Storage Temperature: -55°C to +125°C
- Operating Temperature: -20°C to + 100°C.

Heat sink tabs on hybrids shall be adequately heat sunk such as to provide $T_{case} \leq 100$ °C.

1.3 Packaging - All hybrid microcircuits shall be packaged in a 0.890-by 0.945-by-0.170-inch (maximum) metal flatpack.

The hybrid defined in Drawing 18571
(Regulator, Pre-Driver, and Driver) shall
be packaged excluding transistors Q7 and
Q8 and diodes CR9 and CR10.

TBE shall furnish a set of test fixtures
for the electrical test of each hybrid, as
defined under the "Electrical Test Procedure"
heading of Section 2.

LEAD BENDING

$$\frac{0.08}{0.10} \text{ TYP} \qquad \frac{0.21}{0.23} \text{ TYP}$$
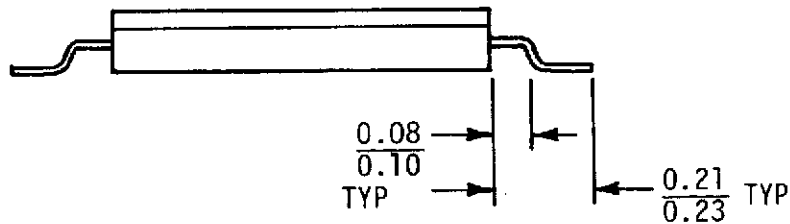
2. MANUFACTURING DESIGN AND TEST SPECIFICATIONS

2.1 Oscillator and Control Logic (TBE Drawing 18569)

2.1.1 Active Trimming

1. Apply +10 Vdc ± 2% to Pin 23.

2. Ground Pin 10.

3. Connect a 1,000-pF capacitor (± 1%) from Pin 5 to ground
   (Pin 10).

4. Trim resistor R1 such that the frequency of the square wave
   appearing at Pin 7 equals to 40 kHz ± 2%.

<div align="center">NOTES</div>

Resistors R2, R3, and R4 shall have a ratio
of 1:1:1 ± 1% with an absolute value tolerance
of 20 kilohms ± 10%.

Diodes CR1 through CR7, which are specified as
1N3604, may be substituted by 1N914 diodes.

2.1.2 Electrical Test

2.1.2.1 Materials

2.1.2.1.1 Power Supply - One power supply is required to perform the necessary testing. This supply is required to deliver 10 Vdc ± 2% at a current drain of less than 10 mA.

2.1.2.1.2 Test Instruments

- One Dual Trace Oscilloscope
- One Digital Voltmeter (0.05% of reading).

2.1.2.1.3 Test Fixture - The test fixture is shown in Figure C-1.

2.1.2.2 Procedure

1. With power removed, switch S1 in position 2, and switch S2 open (OFF), insert the UUT into the test fixture.

2. Apply ±10 Vdc ± 2% to the $+V_{INPUT}$ indicated in Figure C-1.

   a. Observe the waveform present at TP4 with respect to ground.

      Result: A square wave whose

      - Frequency = 40 kHz ±5%
      - Amplitude = 7 V p-p min.
      - Rise and Fall Time < 1 μsec
      - Symmetry: 30% to 70%.

   b. Observe the waveforms present at TP2 and TP3 using a dual trace oscilloscope.

      Result: See Figure C-2.

   c. Observe TP1 using the oscilloscope.

      Result: Output will be high (+9.5 V min.).

   d. With switch S1 in position 3, observe TP1 using the oscilloscope.

      Result: Output will be low (1 V max.).

   e. Return switch S1 to position 2 and observe TP2 and TP3.

      Result: Readings at both test points will be high (+9.5 V min.).

   f. With switch S1 in position 1, observe TP2 and TP3.

      Result: Readings at both test points will be high (+9.5 V min.)

C-4
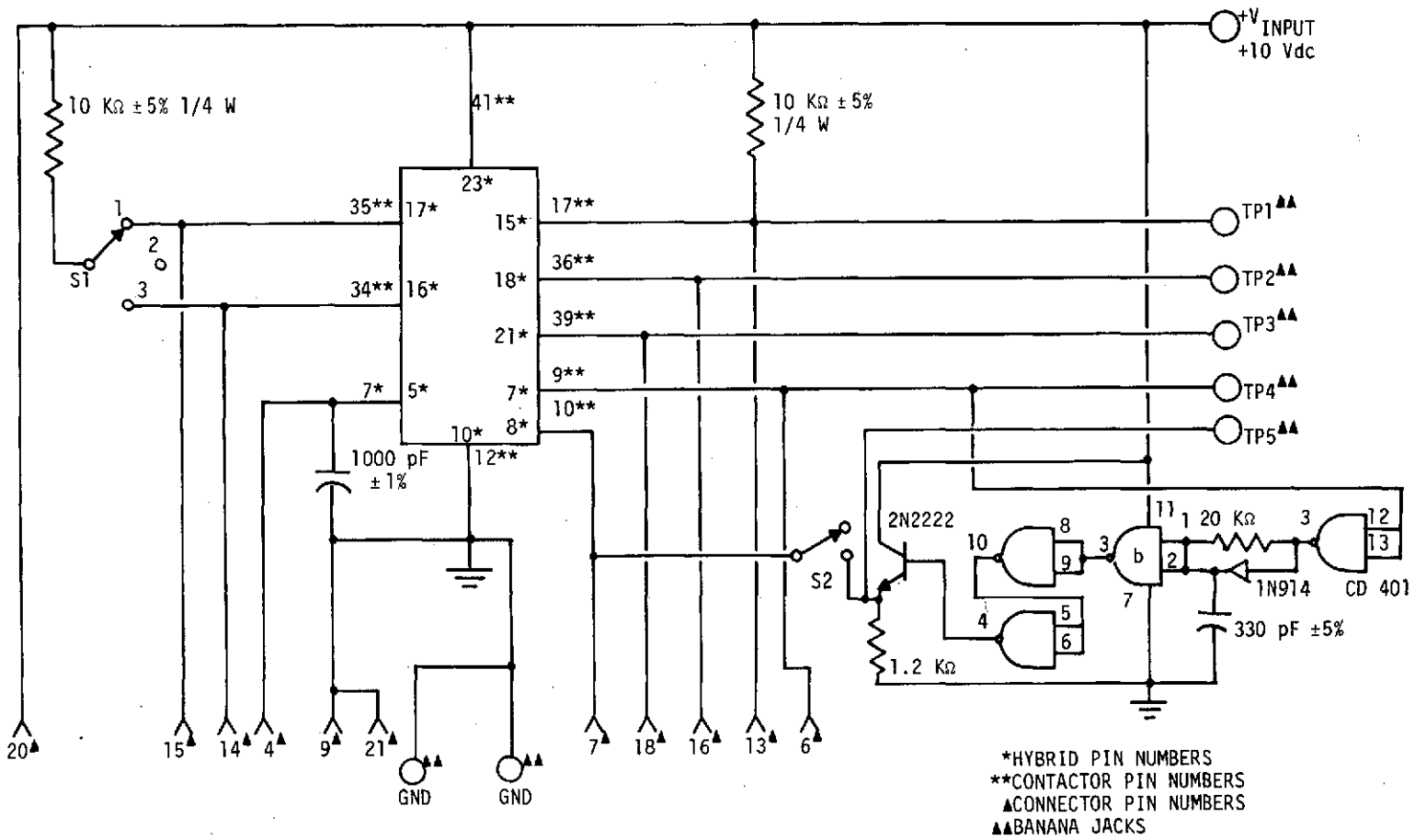
FIGURE C-1.   OSCILLATOR AND CONTROL LOGIC (18569) TEST FIXTURE

C-5

$$t_1 = t_2 = 2.0 \text{ to } 3.5 \text{ } \mu sec$$
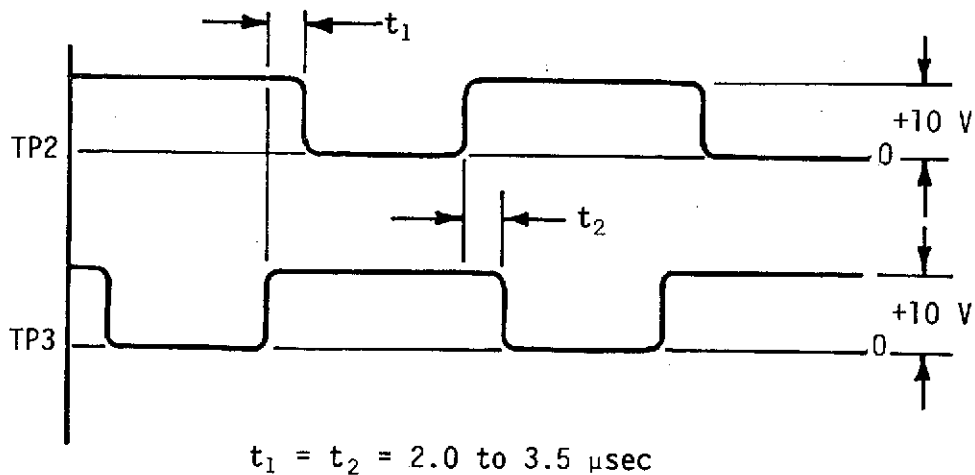
FIGURE C-2.   WAVEFORMS AT TP2 AND TP3

g. Return switch S1 to position 2 and observe TP2 and TP3.

Result: See Figure C-2.

NOTE

If no output appears in step b. above, momentarily place switch S1 in position 1 and return to position 2.

h. With switch S1 in position 2, close switch S2 and observe TP2, TP3, and TP5, utilizing a dual trace oscilloscope.

Result: See Figure C-3.

i. Measure the delay time from the initiation of the positive trigger pulse present at TP5 until the output triggers high at TP2 and TP3.

Result: Delay $\leq$ 150 nsec.

2.2 Pre-Regulator and Comparator (TBE Drawing 18570)

2.2.1 Active Trimming

1.

a. Apply +13 Vdc ± 2% to Pin 14.

b. Ground Pin 13 (Resistor R3 = 7.5 kilohms ± 10%).

C-6
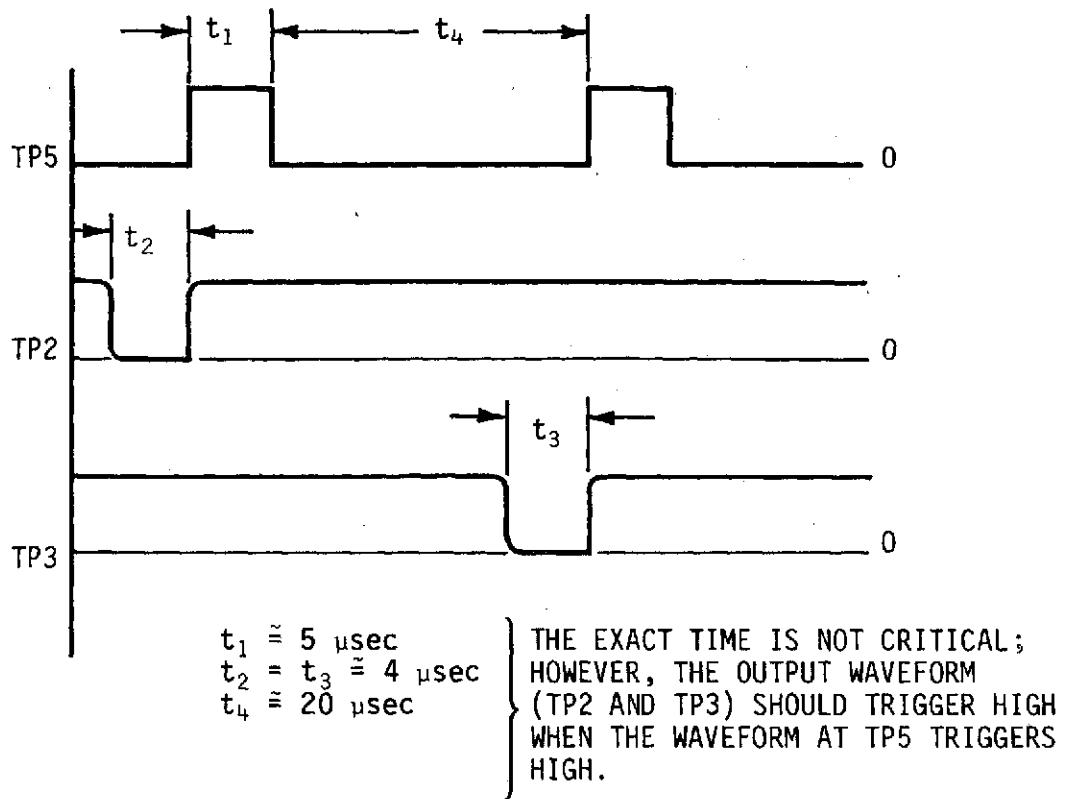
FIGURE C-3. WAVEFORMS AT TP2, TP3, AND TP5

c. Trim resistor R4 such that the voltage measured at
    Pin 9 with respect to ground (Pin 13) equals + 10 V
    ± 2%.

2.

a. Apply +13 Vdc ± 2% to Pin 14.

b. Ground Pin 13 and Pin 23 (Resistor R8 = 49
    kilohms ± 10%.

c. Trim resistor R7 such that when 215 mVdc ± 5% is
    applied to Pin 20 the output appearing at Pin 2 is
    high (8.5 V min.), and with 210 mVdc applied to Pin 20
    the output appearing at Pin 2 is low (1 V max.).

NOTES

Trim the ratio of resistors R15 to R16, 49:1
± 1%, with an absolute value of resistor R15
equal to 49 kilohms ± 10%.

Transistors Q4 and Q7 and Q5 and Q6 must be
selected such that

$$\left| V_{BE} (Q5) - V_{BE} (Q6) \right| \leq 5 \text{ mV at } 25°C$$

$$\left| V_{BE} (Q4) - V_{BE} (Q7) \right| \leq 5 \text{ mV at } 25°C$$

Transistors Q3, Q8, Q9, and Q10 are con-
tained on a single chip in a CA3045
integrated circuit (RCA).

2.2.2 Electrical Test

2.2.2.1 Materials

2.2.2.1.1 Power Supply - Two power supplies are required to perform
the necessary electrical tests:

- Power supply which will deliver +13 to +30 Vdc variable
  at a current drain of less than 30 mA

- Power supply which will deliver 0 to +5 Vdc variable
  at a current drain of less than 5 mA.

2.2.2.1.2 Test Instruments

- One Dual Trace Oscilloscope

- One Digital Voltmeter (0.05% of reading)

- One Pulse Generator capable of providing a 250-mV, 100-nsec
  pulse at a repetition rate of 40 kHz.

2.2.2.1.3 Test Fixture - The test fixture is shown in Figure C-4.

2.2.2.2 Procedure

1. With power removed and switch S1 in position 2, insert
   the UUT into the test fixture.

2. Apply +13 Vdc ± 2% to $+V_{INPUT}$ as indicated in Figure C-4.
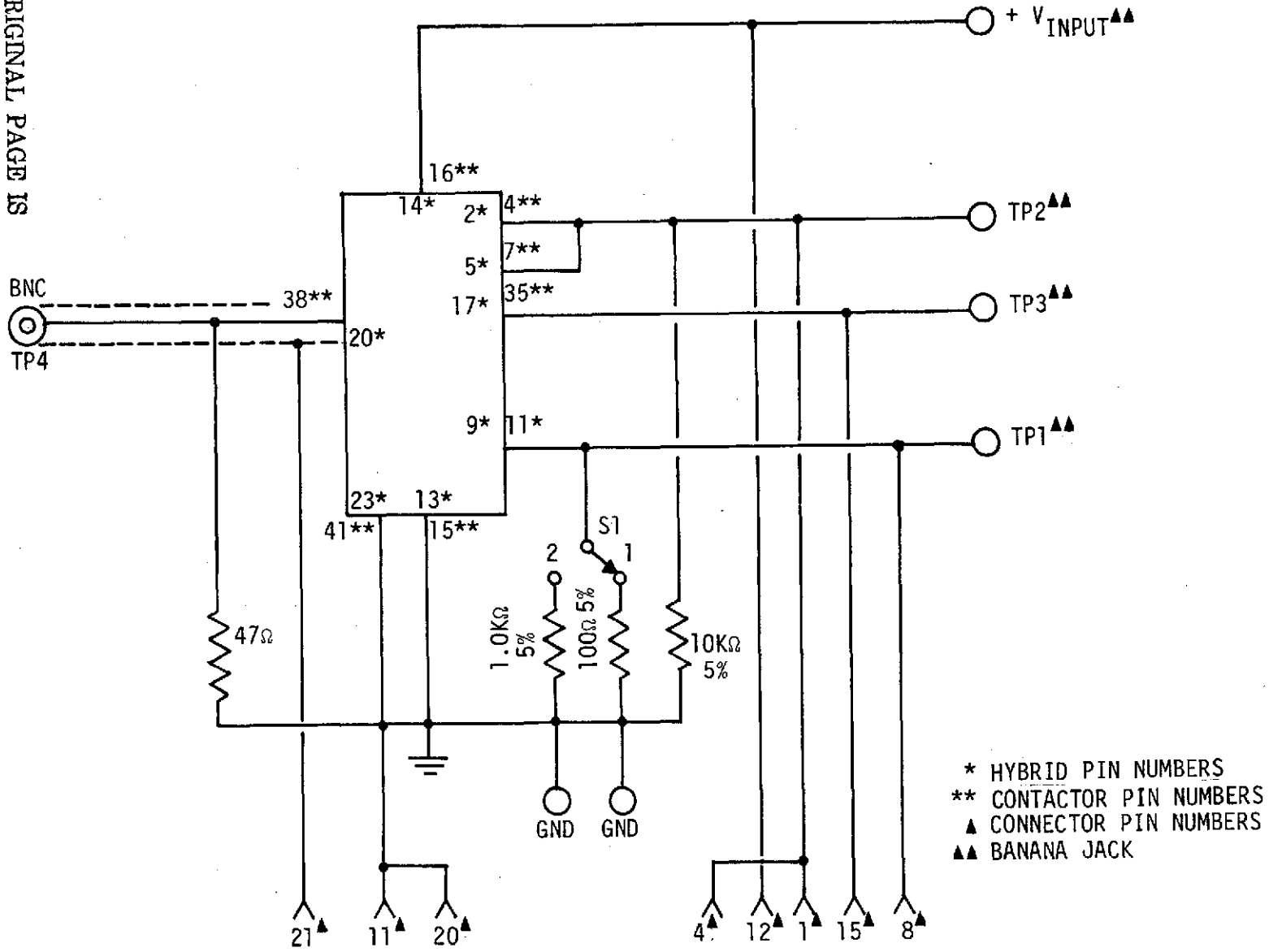
FIGURE C-4.   PRE-REGULATOR AND COMPARATOR (18570) TEST FIXTURE

a. Measure the voltage present at TP1 with respect to ground.

   Result: Voltage measure +10 V ± 2%

b. With switch S1 in position 1, repeat step a. above (make this measurement rapidly).

   Result: Voltage measures +4.50 V max.

3. Apply +30 Vdc to $+V_{INPUT}$ and repeat steps a and b above.

   Result: Same as in steps a and b.

4.

    a.

        (1) Apply +30 Vdc to $+V_{INPUT}$ with switch S1 in position 2.

        (2) Connect variable power supply (0 to 5 V) to TP3, positive at TP3 with respect to ground.

        (3) Monitor TP2 using the oscilloscope.

    b. With variable supply adjusted for +2 V, observe the condition of TP2 with respect to ground.

       Result: Reading at TP2 will be low (+1 V max.).

    c. With the variable supply adjusted for +2.75 V, repeat step b above.

       Result: Reading at TP2 will be high (+8.5 V min.).

5.

    a.

        (1) With +30 Vdc applied to $+V_{INPUT}$, switch S1 in position 2, and TP3 open (remove variable supply), connect the pulse generator to TP4 (BNC), positive-going with respect to ground at TP4 (use a coax for this connection).

        (2) Monitor TP2 and TP4 using a dual trace oscilloscope and an X10 probe.

b. With the pulse generator set at 40-kHz repetition rate, 500-nsec pulse width, and rise and fall time of the pulse of < 20 nsec, adjust the amplitude of the output pulse from the pulse generator to +200 mV peak and observe TP2.

   Result: TP2 will remain in a low state.

c. Repeat step 5.b., with the output of the pulse generator set for 230 mV.

   Result: TP2 will trigger high on application of an input pulse.

d. Repeat step 5.c., with the output of the pulse generator set for +300 mV peak at a pulse width of 200 nsec.

   (1) Observe the delay time between 50% of the peak of the input pulse (TP4) and 50% of the peak of the output pulse (TP2).

      Result: Delay $\leq$ 120 nsec.

   (2) Observe the rise and fall time of the output pulse (TP2).

      Result: Rise time $\leq$ 60 nsec and fall time $\leq$ 60 nsec.

   (3) Observe the pulse width of the output pulse (TP2) from 50% peak to 50% peak.

      Result: Pulse width $\geq$ 200 nsec.

2.3 Regulator, Pre-Driver, and Driver (TBE Drawing 18571)

2.3.1 Active Trimming

1. Apply 60 Vdc to Pin 9.

2. Ground Pin 17.

3. Load Pin 14 such that the load current is approximately 9 mA (1.5 kilohms ± 5%) (resistor R5 = 10.5 kilohms ± 5%).

4. Trim resistor R4 such that the voltage measured at the output (Pin 14) equals +13 V ± 2% with respect to ground.

NOTES

The maximum voltage appearing at Pin 1 shall
be less than 250 V.

Diodes CR1, CR3, CR4, CR5, CR6, CR7, and CR8
specified as 1N3604 may be replaced by 1N914
diodes.

The hybrid shown in TBE Drawing 18571 shall
be fabricated excluding components Q7, Q8,
CR9, and CR10.

2.3.2 Electrical Test

2.3.2.1 Materials

2.3.2.1.1 Power Supply — Two power supplies are required to perform the
necessary electrical tests:

- Power supply which will deliver +22 to +50 Vdc variable
at a current drain of less than 50 mA

- Power supply which will deliver +10 Vdc ± 2% at a current
drain of less than 50 mA.

2.3.2.1.2 Test Instruments

- One Dual Trace Oscilloscope

- One Digital Voltmeter (0.05% of reading).

2.3.2.1.3 Test Fixture — The test fixture is shown in Figure C-5.

2.3.2.2 Procedure

1. With power removed and switch S1 in position 1, insert
the UUT into the test fixture.

2.

a. Apply +22 Vdc to $+V_{HIGH\ INPUT}$, as indicated in Figure C-5,
with switch S1 in position 1.

b. Measure the voltage at TP1 with respect to ground
(momentarily press switch S2 for this measurement).

Result: Voltage measured = +13 Vdc ± 650 mV.

c. With switch S2 in position 2, measure the voltage at
TP1 with respect to ground (momentarily press switch
S2 for this measurement) (make measurement rapidly).

Result: Voltage measured = 5 Vdc max.

FIGURE C-5. REGULATOR, PRE-DRIVER, AND DRIVER (18571) TEST FIXTURE
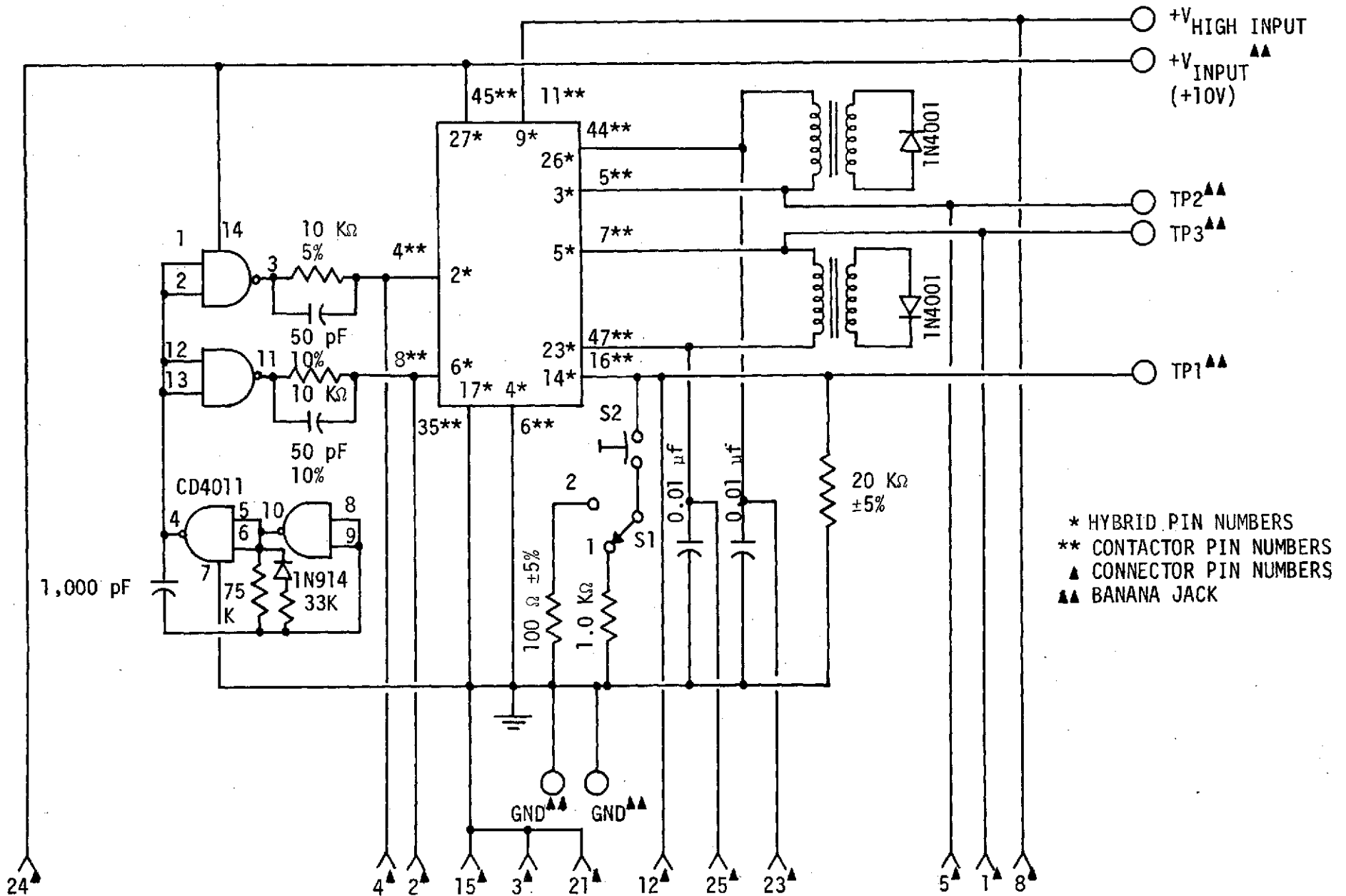
* HYBRID PIN NUMBERS
** CONTACTOR PIN NUMBERS
▲ CONNECTOR PIN NUMBERS
▲▲ BANANA JACK

3. Apply +36 Vdc to $+V_{HIGH\ INPUT}$, as indicated in Figure C-5, and measure the voltage at TP1 with respect to ground (momentarily press switch S2 for this measurement).

Result: Voltage measured = +13 Vdc ± 650 mV.

4. With switch S1 in position 1, apply 50 Vdc to $+V_{HIGH\ INPUT}$, as indicated in Figure C-5, and measure the voltage at TP1 with respect to ground (do not press switch S2 during this measurement).

Result: Voltage measured = +13 Vdc ± 1 Vdc.

5.

    a. Remove the high voltage supply (+22 to +50 Vdc) and apply +10 Vdc ± 2%, as indicated in Figure C-5.

    b. Observe waveforms present at TP2 and TP3 with respect to ground.

        Result: See Figure C-6.
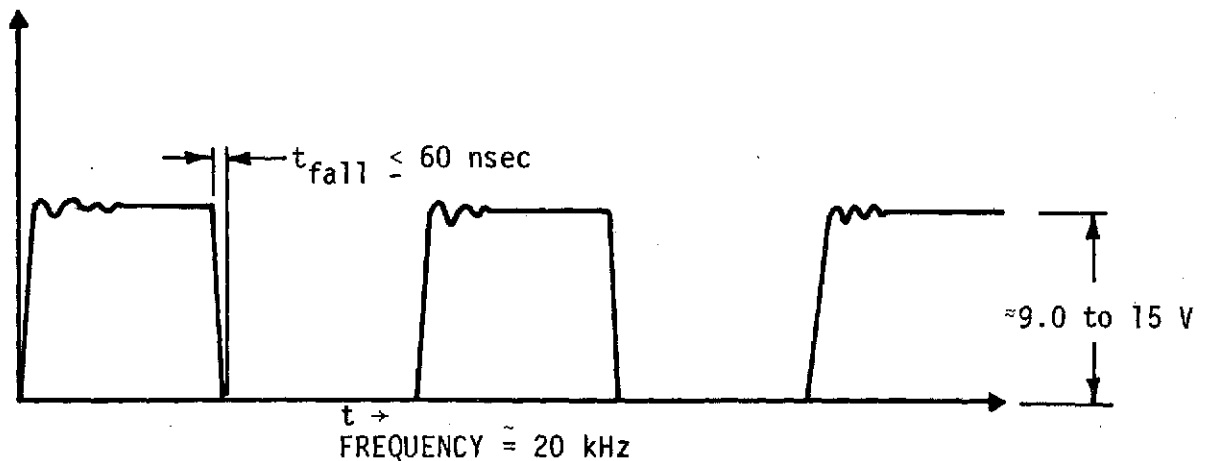
FIGURE C-6. WAVEFORMS AT TP2 AND TP3

2.4 Reference and Summing Amplifier (TBE Drawing 18572)

2.4.1 Active Trimming

1. Apply +20 Vdc to Pin 11.

2. Ground Pin 29 (resistor R10 = 20 kilohms ± 5%).

3. Trim resistor R11 such that the voltage appearing at
    Pin 25 with respect to ground equals +10 Vdc ± 10 mV.

NOTES

The temperature coefficients of resistors
R10 and R11 shall be matched such that

$$|TC \text{ of } R10 - TC \text{ of } R11| \leq 10 \text{ ppm/°C.}$$

2.4.2 Electrical Test

2.4.2.1 Materials

2.4.2.1.1 Power Supply – One power supply is required to perform the
electrical tests. This supply is required to supply a
variable +24 to +40 Vdc at a current drain of less than
+40 mA.

2.4.2.1.2 Test Instruments

- One Oscilloscope
- One Digital Voltmeter (0.05% of reading)
- One Sine Wave Signal Generator.

2.4.2.1.3 Test Fixture – The test fixture is shown in Figure C-7.

2.4.2.2 Procedure

1. With power removed, switch S1 in position 1, and switches
    S2 and S3 open (OFF), insert the UUT into the test fixture.

2.

   a. Apply +24 Vdc to $+V_{INPUT}$, as indicated in Figure C-7.

   b. Place switch S1 in position 1.

   c. Position switches S2 and S3 open (OFF).

   d. Measure the voltage at TP1 with respect to ground.

       Result: Voltage measured = +18 to +24 Vdc.

C-15
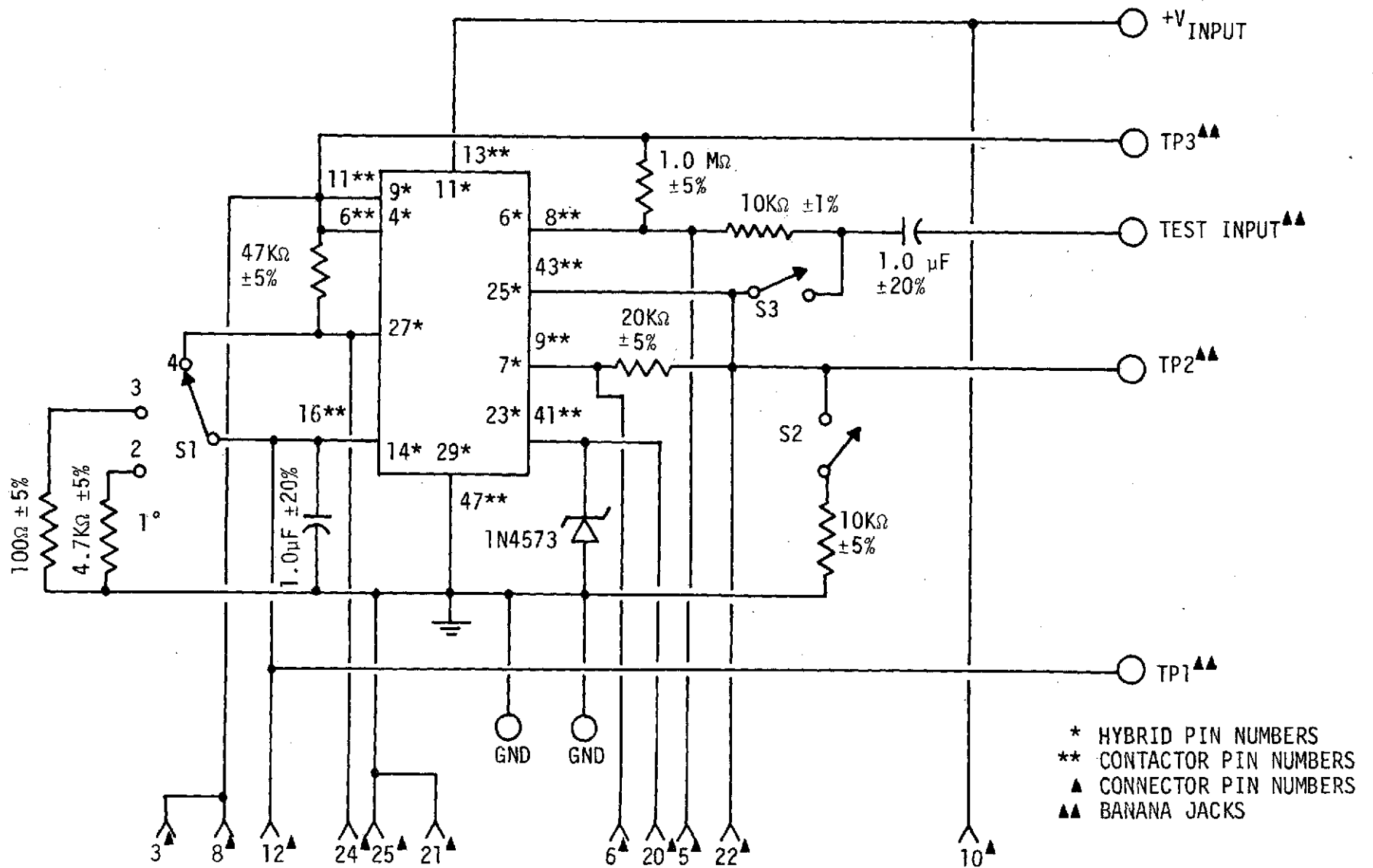
FIGURE C-7. REFERENCE AND SUMMING AMPLIFIER (18572) TEST FIXTURE

3.

    a.   Apply +40 Vdc to $+V_{INPUT}$, as indicated in Figure C-7, and position switches S2 and S3 open (OFF).

    b.   With switch S1 in position 1, measure the voltage at TP1 with respect to ground.

        Result: Voltage measured = +18 to +24 Vdc.

    c.   With switch S1 in position 2, measure the voltage at TP1 with respect to ground.

        Result: Voltage measured = +18 to +24 Vdc.

    d.   With switch S1 in position 3, measure the voltage at TP1 with respect to ground (place switch S1 in position 4 immediately after the measurement).

        Result: Voltage measured = +1.6 to +0.8 Vdc.

4.

    a.   Apply +40 Vdc to $+V_{INPUT}$, as indicated in Figure C-7, place switch S1 in position 4, and position switch S3 open (OFF).

    b.   With switch S2 open (OFF), measure the voltage at TP2 with respect to ground.

        Result: Voltage measured = +10 V ± 10 mV.

    c.   Repeat step 4.b., with switch S2 closed (ON).

        Result: Voltage measured = +10 V ± 10 mV.

NOTE

The maximum temperature coefficient of the voltage measured at TP2 is 0.0027%/°C.

5.

    a.   Apply +40 Vdc to $+V_{INPUT}$, as indicated in Figure C-7, place switch S1 in position 4, and position switch S2 closed (ON).

    b.   With switch S3 open (OFF), apply a +0.2 - V p-p sine wave signal at a frequency of 10 kHz into the test input shown in Figure C-7 and measure the output at TP3 with respect to ground (use oscilloscope).

        Result: Voltage measured = +2 V p-p ± 15%.

c. With switch S3 open (OFF), apply a +0.3 - V p-p sine wave signal at a frequency of 640 Hz and repeat step 5.b.

Result: Voltage measured = 4.5 V p-p ± 15%.

d. With switch S3 closed (ON), measure the output voltage measured at TP3 with respect to ground (use digital voltmeter).

Result: Voltage measured = +10 V ± 600 mV.

2.5 Overvoltage and Undervoltage Detector (TBE Drawing 18573)

NOTES

Resistors R6, R8, R9, and R10 should be trimmed to an absolute value of 20 kilohms ± 1%.

Diodes CR2 and CR3 specified as 1N3604 may be replaced by 1N914 diodes.

2.5.1 Electrical Test

2.5.1.1 Materials

2.5.1.1.1 Power Supply - Three power supplies are required to perform the necessary electrical tests.

- Power supply which will deliver +22 Vdc ± 5% at a current drain of less than +10 mA

- Power supply which will deliver a variable 0 to +30 Vdc at a current drain of less than +2 mA.

2.5.1.1.2 Test Instrument - One Digital Voltmeter (0.05% of reading)

2.5.1.1.3 Test Fixture - The test fixture is shown in Figure C-8.

2.5.1.2 Procedure

1. With power removed, insert the UUT into the test fixture.

2.

a. Apply +22 Vdc to V_{INPUT}, as indicated in Figure C-8.
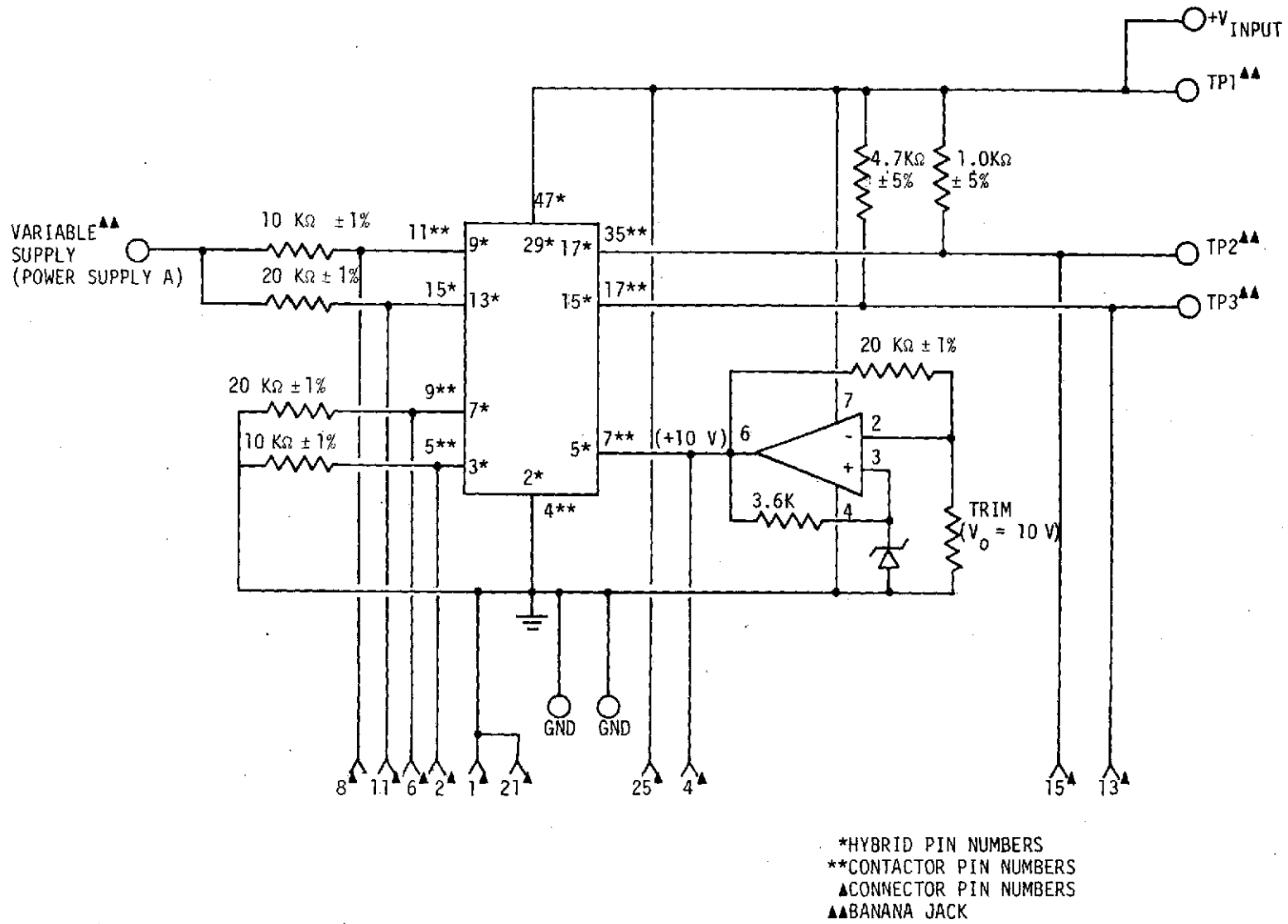
FIGURE C-8. OVERVOLTAGE AND UNDERVOLTAGE DETECTOR (18573) TEST FIXTURE

b.

    (1)   Adjust the variable supply to +4.75 Vdc and
             apply voltage as indicated in Figure C-8
             (Power Supply A)

    (2)   Measure the voltage present at TP1 with
             respect to TP2.

             Result: Voltage measured $= \leq$ +2 mV.

    (3)   Measure the voltage present at TP3 with respect
             to ground.

             Result: Voltage measured $= \leq$ +0.5 Vdc.

c.

    (1)   Adjust the variable supply to +5.25 Vdc and
             apply voltage as indicated in Figure C-8 (Power
             Supply A).

    (2)   Measure the voltage present at TP1 with respect
             to TP2.

             Result: Voltage measured $= +2 \text{ V} \pm 20\%$.

    (3)   Measure the voltage present at TP3 with respect
             to ground.

             Result: Voltage measured $= \leq$ +0.5 Vdc.

d. Adjust the variable supply to +9.5 Vdc, apply voltage
as indicated in Figure C-8 (Power Supply A), and
measure voltage as in steps c.(2) and c.(3).

e.

    (1)   Adjust the variable supply to +10.5 Vdc and
             apply voltage as indicated in Figure C-8 (Power
             Supply A).

    (2)   Measure the voltage present at TP1 with respect
             to TP2.

             Result: Voltage measured $= \leq$ + 2 mV.

    (3)   Measure the voltage present at TP3 with respect
             to ground.

             Result: Voltage measured $= +22 \text{ V} \pm 5\%$.

3. HYBRID CIRCUIT CHANGES

3.1 Oscillator and Control Logic (TBE Drawing 18569, Revision A)

- The nominal value of resistor R1 (previously 18 kilohms) is 14 kilohms.

- Connect leads linking U4A (Pin 9) and U4B (Pin 10) to hybrid terminals.

- Change the resistance of resistors R17 and R18 from 10 kilohms to 4.7 kilohms.

- Connect the positive side of capacitor C4 to hybrid terminal.

- Change the value of capacitor C4 from 100 pF to 75 pF.

- Change designations on schematics as shown below:

Pin No.	Old Designation	New Designation
4	TP5	Sync
5	Ext Cap.	Ext Cap
7	TP4	Clock Out
8	Ext S2	Inhibit Input
10	GND	GND
15	TP1	Fail Monitor
16	Ext S1-3	Over-Undervoltage Shut-down Input
17	Ext S1-2	Remote Shutdown
18	TP2	Drive Output Q
21	TP3	Drive Output $\overline{Q}$
23	+10 V	+V (+10 V)

3.2 Pre-Regulator and Comparator (TBE Drawing 18570, Revision A)

- Connect lead from the collector of Q1 to a hybrid terminal.

- Change the resistance of resistor R2 from 22 ohms ± 2% to 15 ohms ± 2%.

- Change designations on schematics as shown below.

Pin No.	Old Designation	New Designation
2	To TP2	Comparator Output
4	To Q3-10	Compensation
5	To TP2	Compensation
9	+10 V	+10 V Out
13	Ground	Ground
14	+ Vdc	+V Input
15	To Volt Reg	Short Circuit Program
17	To TP3	Low Impedance
20	2.5 mV	High Impedance Non-Invert Input
21	Output (Q7 Base)	Invert - Input
23	Ground	Comparator Low
26	Case Contact	Case Contact

3.3 Regulator, Pre-Driver, and Driver (TBE Drawing 18571, Revision A)

- Change the resistance of resistor R1 from 620 kilohms to 68 kilohms ± 10%.

- Change the resistance of resistor R2 from 20 ohms ± 5% to 12 ohms ± 5%.

- Change the resistance of resistor R3 from 27 kilohms to 12 kilohms

- Change the resistance of resistors R6 and R7 from 3.3 kilohms to 1.5 kilohms

- Change designations on schematics as shown below.

Pin No.	Old Designation	New Designation
2	TP3	Q5 Base
3	R2	Q5 Collector
4	Ground	Drive Ground

Pin No.	Old Designation	New Designation
5	R3	Q6 Collector
6	TP2	Q6 Base
9	Hi V	Pre-Reg + V Input
14	TP1	Pre-Reg Output
17	Ground	Pre-Reg Ground
20	Case Contact	Case Contact
22	Q3 Emitter	Short Circuit Program Low
24	Q3 Emitter	Short Circuit Program High
26	+1	Transformer Hi (1)
27	+10 V	Drive +V Input (+10 V)
29	T2	Transformer Hi (2)

3.4 Reference and Summing Amplifier (TBE Drawing 18572, Revision A)

- Change the resistance of resistors R8 and R2 from 5.1 megohms to 1.5 megohms.

- Delete the network consisting of resistor R5 (1.25 megohms) and capacitor C3 (200 pF)

- Connect a lead from the junction of resistor R4 (125 kilohms) and capacitor C2 (2,000 pF) to a hybrid pin.

- Change the resistance of resistor R13 from 50 megohms to 39 megohms.

- Change designations on schematics as shown below:

Pin No.	Old Designation	New Designation
2	Case Contact	Case Ground
4	U1 Input	Error Amp - Internal Compensation
6	U1 Invert Input	Error Amp - Invert Input

Pin No.	Old Designation	New Designation
7	U1 Non-Invert	Error Amp - Non-Invert Input
9	Q1 Output	Error Amp - Out (Low Impedance)
10	U1 Output	Error Amp Output
11	V Supply	Regulator + V Supply Input
13	Q2 Base	Regulator Short Circuit Program
14	Q2 Emitter	Regulator + V Out (+22 V)
17	R6	Remote Sense (-)
18	R3A	Remote Sense (+)
20	R3B	Remote Sense (+)
21	U2 ± I	Ref Volt Program
22	U2 NI	Ref Volt Filt.
23	VR2 Input	Zener Ref
25	U2 Out	Ref Volt Output
27	+20 V	Amp + V Supply (+22 V)
29	Ground	Ground

3.5 Overvoltage and Undervoltage Detector (TBE Drawing 18573, Revision A)

- Add a 30-kilohm ± 5% resistor from the U2 output (Pin 6 of U2) and +V input (Pin 29 of the hybrid)

- Change desigations on schematics as shown below:

Pin No.	Old Designation	New Designation
2	Ground	Ground
3	Ext Rd	Undervolt Program (−)
5	+V Ref	+V Ref
7	Ext RC	Overvolt Program (−)
9	Ext RA	Undervolt Program (+)
11	U1 Out	Undervolt Output
13	Ext RB	Overvolt Program
15	TP3	Fail Monitor
17	TP2	Over-Under Volt Fail Output
23	Case Contact	Case Contact
27	U2 Out	Overvolt Output
29	TP1 +22 V	+V Input (+22 V)

NOTE

Hybrid Pins 1, 12, 19, 28, and 30 are not to be used. TBE will furnish a set of test fixtures for the electrical test of each hybrid as defined under the Manufacturing Design and Test Specifications.

OSCILLATOR CONTROL LOGIC (18569) TEST RESULTS   SN _____

SPEC. PARA.	CHARACTERISTIC	ACCEPT. RANGE	MEASURED $T_{AMB.}$ = °C	MEASURED $T_{AMB.}$ = °C	MEASURED $T_{AMB.}$ = °C
2.1.2.2 2.a.	Freq.	38 to 42 kHz			
	Amp. (p-p)	7 V min.			
	t_{rise}/t_{fall}	$\leq$ 1 μsec			
	Symmetry	30% to 70%			
2.b	t_1 and t_2/Ref. Figure C-2	2 to 3.5 μsec			
2.c.	TP1	9.5 V min.			
2.d.	TP1	1 V max.			
2.e.	TP2/TP3	9.5 V min.			
2.f.	TP2/TP3	9.5 V min.			
2.g.	TP2/TP3	Ref. Figure C-2			
2.h.	TP2/TP3/TP5	Ref. Figure C-3			
2.i.	t_{delay}	$\leq$ 150 nsec			

DATE: _____

PERFORMED BY: _____

APPROVED: _____

PRE-REGULATOR AND COMPARATOR (18570)   SN _____
TEST RESULTS

SPEC. PARA.	CHARACTERISTIC	ACCEPT. RANGE	MEASURED $T_{AMB.}$ = °C	MEASURED $T_{AMB.}$ = °C	MEASURED $T_{AMB.}$ = °C
2.2.2.2 2.a.	TP1	+9.8 to 10.2 V			
2.b.	TP1	4.5 V max.			
3.a.	TP1	9.8 to 10.2 V			
3.b.	TP2	3.4 V max.			
4.b.	TP2	1.0 V max.			
4.c.	TP2	8.5 V max.			
5.b.	TP2	1.0 V			
5.c.	TP2	Switch			
5.d. (1)	Delay	$\leq$ 120 nsec			
(2)	t_{rise}/t_{fall}	$\leq$ 60 nsec			
(3)	Pulsewidth	$\geq$ 200 nsec			

DATE: _____

PREPARED BY: _____

APPROVED: _____

REGULATOR, PRE-DRIVER, AND DRIVER (18571) TEST RESULTS   SN_____

SPEC. PARA.	CHARAC- TERISTIC	ACCEPT. RANGE	MEASURED $T_{AMB.}$ = °C	MEASURED $T_{AMB.}$ = °C	MEASURED $T_{AMB.}$ = °C
2.3.2.2 2.b.	TP1	12.35 to 13.65 V			
2.c.	TP1	5 V max.			
3.a.	TP1	12.35 to 13.65 V			
b.	TP1	4 V max.			
4.	TP1	12 to 14 V			
5.	TP2/TP3	Ref. Figure C-5			

DATE: _____

PREPARED BY: _____

APPROVED: _____

REFERENCE AND SUMMING AMPLIFIER (18572) TEST RESULTS   SN _____

SPEC. PARA.	CHARAC- TERISTIC	ACCEPT. RANGE	MEASURED $T_{AMB.}$ = °C	MEASURED $T_{AMB.}$ = °C	MEASURED $T_{AMB.}$ = °C
2.4.2.2 2.	TP1	18 to 24 V			
3.b.	TP1	18 to 24 V			
c.	TP1	18 to 24 V			
d.	TP1	1.6 to 0.8 V			
4.b.	TP2	+10 V ± 10 mV			
c.	TP2	+10 V ± 10 mV			
5.b.	TP3	1.7 to 2.3 V p-p			
5.c.	TP3	3.825 to 5.175 V			
5.d.	TP3	9.4 to 10.6 V			

DATE: _____

PREPARED BY: _____

APPROVED: _____

OVERVOLTAGE AND UNDERVOLTAGE DETECTOR (18573)   SN _____

TEST RESULTS

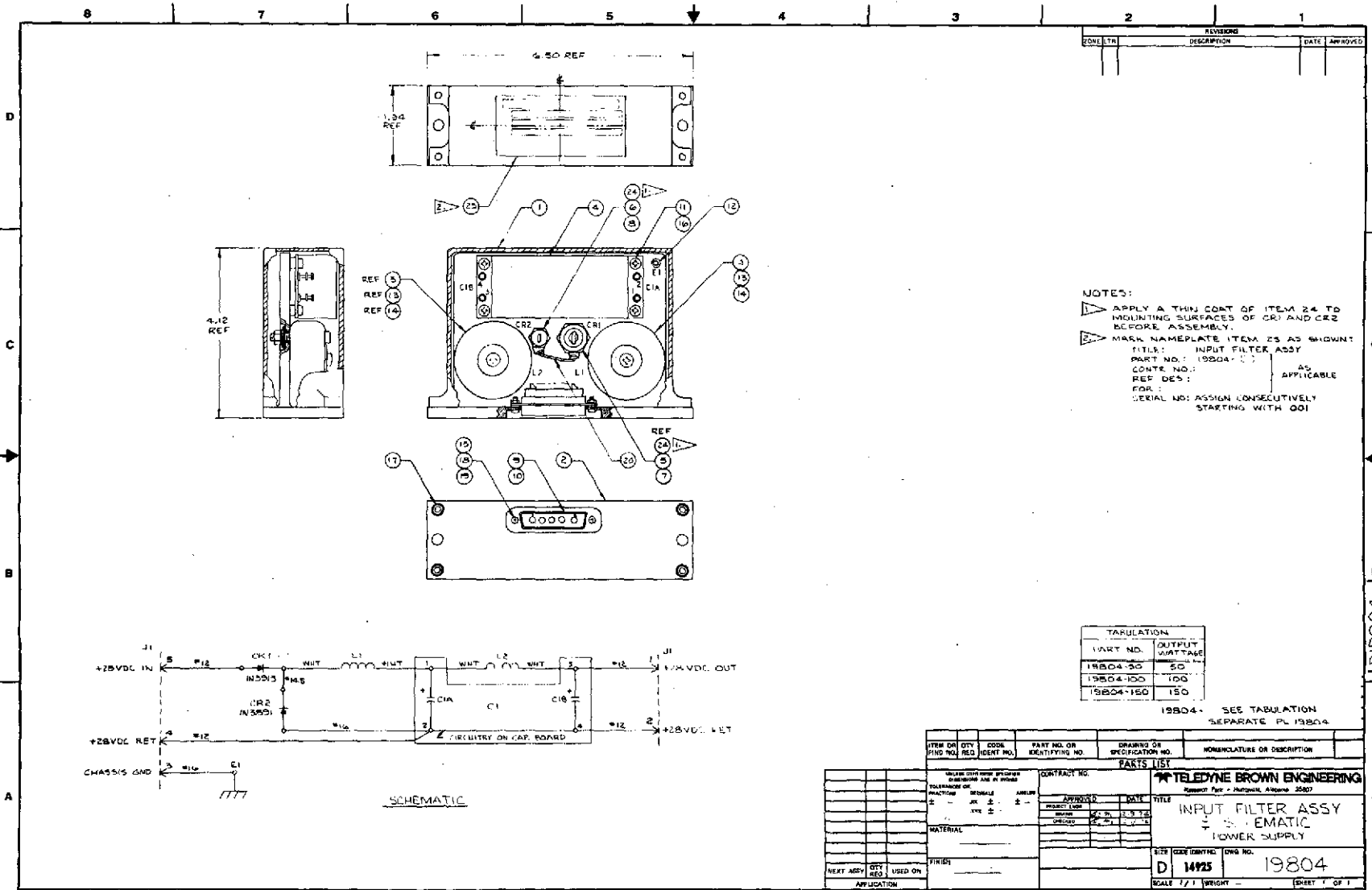| SPEC. PARA.	CHARAC- TERISTIC	ACCEPT. RANGE	MEASURED $T_{AMB.} =$ ^{O}C	MEASURED $T_{AMB.} =$ ^{O}C	MEASURED $T_{AMB.} =$ ^{O}C
2.5.1.2 2.b.(2)	TP1	$\leq$ 2 mV			
2.b.(3)	TP3	$\leq$ 0.5 V			
2.c.(2)	TP1	1.6 to 2.4 V			
2.c.(3)	TP3	$\leq$ 0.5 V			
2.d.(1)	TP1	1.6 to 2.4 V			
2.d.(2)	TP3	$\leq$ 0.5 V			
2.e.(1)	TP1	$\leq$ 2 mV			
2.e.(2)	TP3	20.8 to 23.1 V			

DATE: _____

PREPARED BY: _____

APPROVED: _____

APPENDIX D. EXPANDABLE MAIN FRAME POWER SUPPLY MECHANICAL DESIGN

MOUNTING HOLES
.281 DIA C.BORE .438 DIA X .50 DEEP
REF

"L" REF

"N" EQ SP @ 5.000 REF
TYP

1.92
REF
TYP

INPUT
FILTER
ASSY

INVERTER/OUTPUT
ASSY

INPUT/OUTPUT

6.56
REF
6.000
REF

J2
CONTROL

.78
REF

SECTION A-A

5.66
REF

1.50
REF

6 REF
7 REF
11 REF
12 REF

A1 A2 A3 A4 A5 A6 A7

A

VIEW 13-13

TABULATION

ASSY PART NO.	WATTAGE OUTPUT	INVERTER/OUTPUT POSITIONS	N	"L"	WIRING DIAGRAM
19801-51	50	1	A2	1	7.00	E19821
-52		A2, A3	2	1	9.50	E19822
-53		A2, A3, A4	2	12.00	E19823
-54		A2, A3, A4, A5	2	14.50	E19824
19801-55	50	A2, A3, A4, A5, A6	3	17.00	E19825
19801-102	100	2	A2, A3	1	9.50	E19822
-103		A2, A3, A4	2	12.00	E19823
-104		A2, A3, A4, A5	2	14.50	E19824
-105		A2, A3, A4, A5, A6	3	17.00	E19825
19801-106	100	6	A2, A3, A4, A5, A6, A7	3	19.50	E19826
19801-153	150	3	A2, A3, A4	2	12.00	E19823
-154		A2, A3, A4, A5	2	14.50	E19824
-155		A2, A3, A4, A5, A6	3	17.00	E19825
19801-156	150	6	A2, A3, A4, A5, A6, A7	3	19.50	E19826

19801- SEE TABULATION

SEPARATE PL 19801

PARTS LIST

ITEM FIND NO.	QTY REQ'D	CODE IDENT NO.	PART NO. OR IDENTIFYING NO.	DRAWING OR SPECIFICATION NO.	NOMENCLATURE OR DESCRIPTION		

TELEDYNE BROWN ENGINEERING
Research Park • Huntsville, Alabama 35807

TITLE
POWER SUPPLY ASSY

SIZE E CODE IDENT NO. 14925 DWG NO. 19801

SCALE 1/1 WEIGHT SHEET 1 OF 1

REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED

4.50
REF

2.44
REF

4.12
REF

2 PLCS

31
REF

NOTES:

1. APPLY A THIN COAT OF ITEM 31 TO MOUNTING SURFACES OF Q1,Q2,CR1 AND CR2 BEFORE ASSEMBLY.

2. LAST THREE DIGITS OF PART NO. ARE SIGNIFICANT AND EQUAL TO THE OUTPUT VOLTAGE OF MODULE. COMPLETE PART NO. TO BE GIVEN WHEN ORDERING.
   EXAMPLE #1:
   19805-12-015 IS AN INVERTER/OUTPUT ASSY WITH AN OUTPUT OF 15VDC.
   EXAMPLE #2:
   19805-10-005 IS AN INVERTER/OUTPUT ASSY WITH AN OUTPUT OF 5VDC.

3. MARK NAMEPLATE, ITEM 32, AS SHOWN:
   TITLE: INVERTER/OUTPUT ASSY
   PART NO.: 19805-( )
   CONTR NO.:   AS
   REF DES: APPLICABLE
   FOR:
   SERIAL NO.: ASSIGN CONSECUTIVELY STARTING WITH 001

4. REFERENCE DRAWINGS:
   ADVANCED ELECTRICAL SCHEMATIC-SEE TAB.

TABULATION

PART NO.	OUTPUT WATTAGE	OUTPUT RANGE	ADVANCED ELECTRICAL SCHEMATIC
19805-10-	10	4-6	D19B27
-11-		8-11	D19B28
-12-		12-18	D19B27
-13-		24-35	D19B28
-14-	1	36-56	D19B27
19805-15-	10	72-108	D19B28
19805-50-	50	4-6	D19B27
-51-		8-11	D19B28
-52-		12-18	D19B27
-53-		24-35	D19B28
-54-		36-56	D19B27
19805-55-	50	72-108	D19B28

19805- SEE TABULATION
SEPARATE PL 19805

ITEM OR FIND NO. | QTY REQD | CODE IDENT NO. | PART NO. OR IDENTIFYING NO. | DRAWING OR SPECIFICATION NO. | NOMENCLATURE OR DESCRIPTION

PARTS LIST

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPROVED

4.50 REF

1.34 REF

4.12 REF

NOTES:

1. APPLY A THIN COAT OF ITEM 24 TO MOUNTING SURFACES OF CR1 AND CR2 BEFORE ASSEMBLY.

2. MARK NAMEPLATE ITEM 25 AS SHOWN:
   TITLE: INPUT FILTER ASSY
   PART NO.: 19804- ( )
   CONTR NO.:   AS
   REF DES: APPLICABLE
   FOR:
   SERIAL NO: ASSIGN CONSECUTIVELY
         STARTING WITH 001

TABULATION	
PART NO.	OUTPUT WATTAGE
19804-50	50
19804-100	100
19804-150	150

19804- SEE TABULATION
SEPARATE PL 19804

SCHEMATIC

+28VDC IN

+28VDC RET

CHASSIS GND

+28VDC OUT

+28VDC RET

CIRCUITRY ON CAP. BOARD

ITEM OR FIND NO.	QTY REQ.	CODE IDENT NO.	PART NO. OR IDENTIFYING NO.	DRAWING OR SPECIFICATION NO.	NOMENCLATURE OR DESCRIPTION

PARTS LIST

TELEDYNE BROWN ENGINEERING
Research Park · Huntsville, Alabama 35807

TITLE: INPUT FILTER ASSY
& SCHEMATIC
POWER SUPPLY

SIZE	CODE IDENT NO.	DWG NO.
D	14925	19804

SCALE 1/1   WEIGHT —   SHEET 1 OF 1

APPENDIX E. HYBRID BREADBOARD POWER
SUPPLY TEST DATA
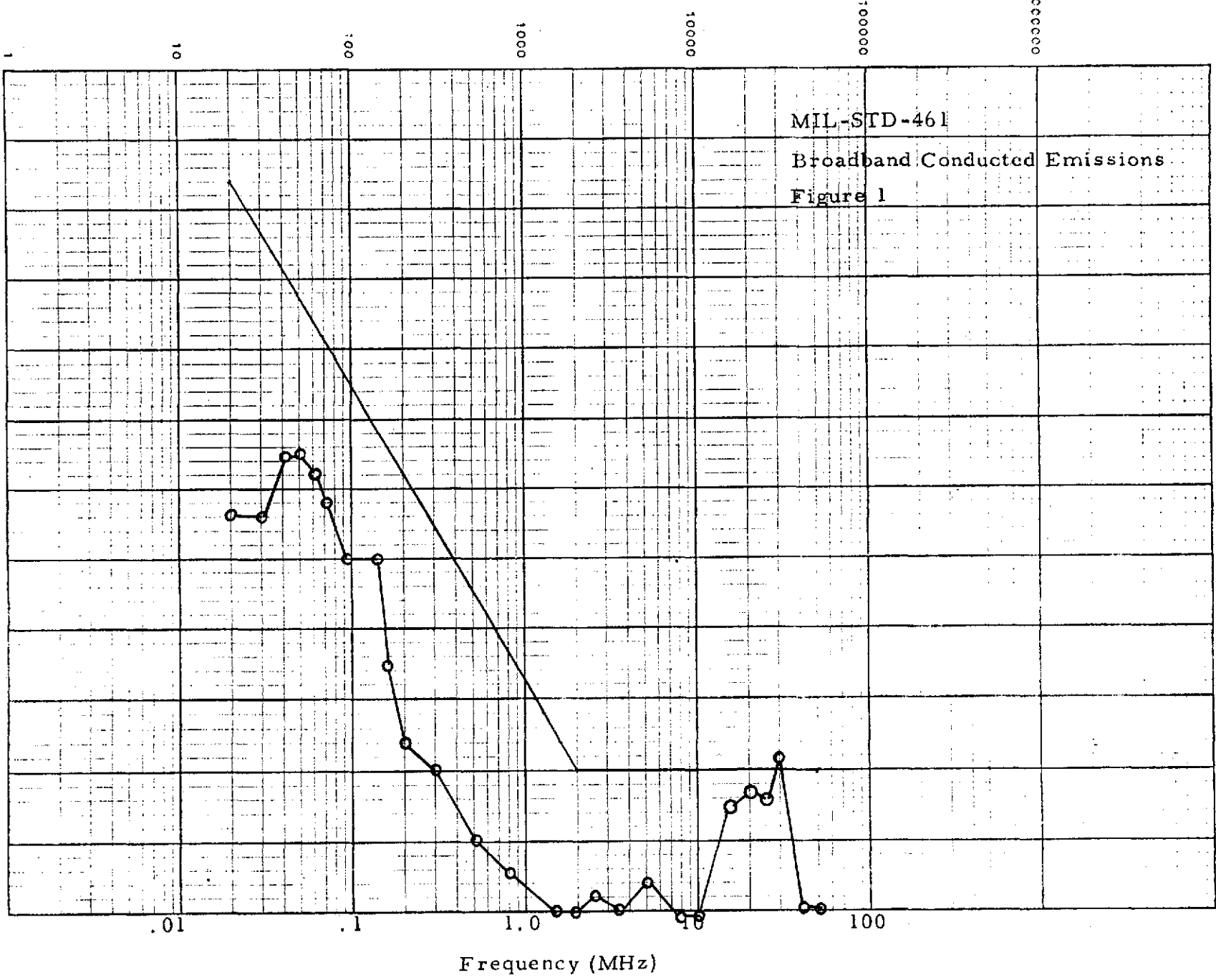
+24 Vdc Input Power

MIL-STD-461

Broadband Conducted Emissions

Figure 1

Frequency (MHz)

dB μV/MHz

E-2

MODEL

DATE

+30 Vdc Input Power

MIL-STD-461

Broadband Conducted Emissions
Figure 2

MODEL

DATE

E-3

dB/μA/MHz

Frequency (MHz)

+30 Vdc Input Power

MIL-STD-461

Broadband Conducted Emissions
Figure 3

Frequency (MHz)

+24 Vdc Input Power

MIL-STD-461
Narrowband Conducted Emissions
Figure 4

E-5

dB/µA

Frequency (Hz)

MODEL

DATE

+30 Vdc Input Power

MIL-STD-461
Narrowband Conducted Emissions
Figure 5

Frequency (Hz)

dB/µA

E-6

+36 Vdc Input Power

MIL-STD-461
Narrowband Conducted Emissions
Figure 6

E-7

dB/μA

Frequency (Hz)
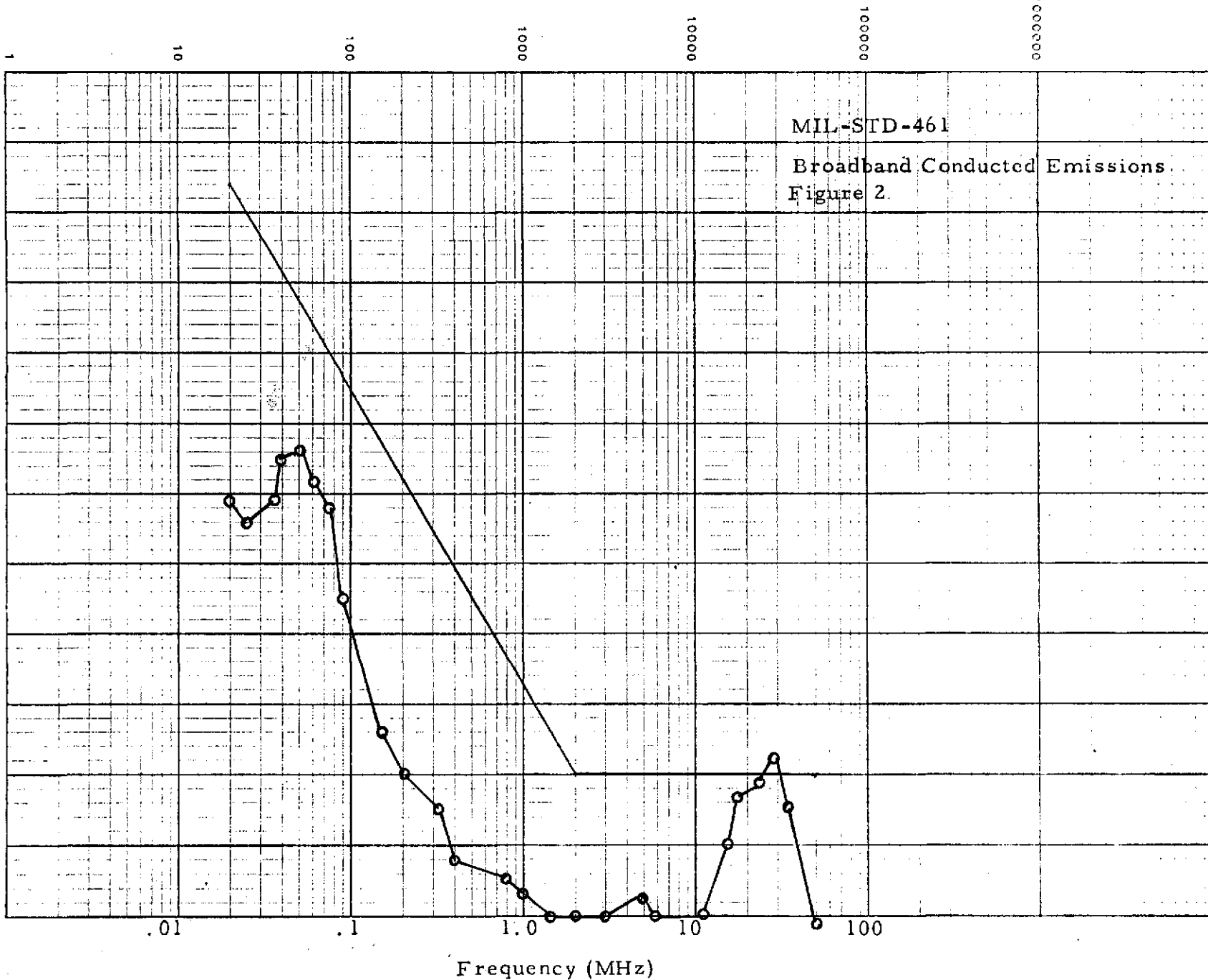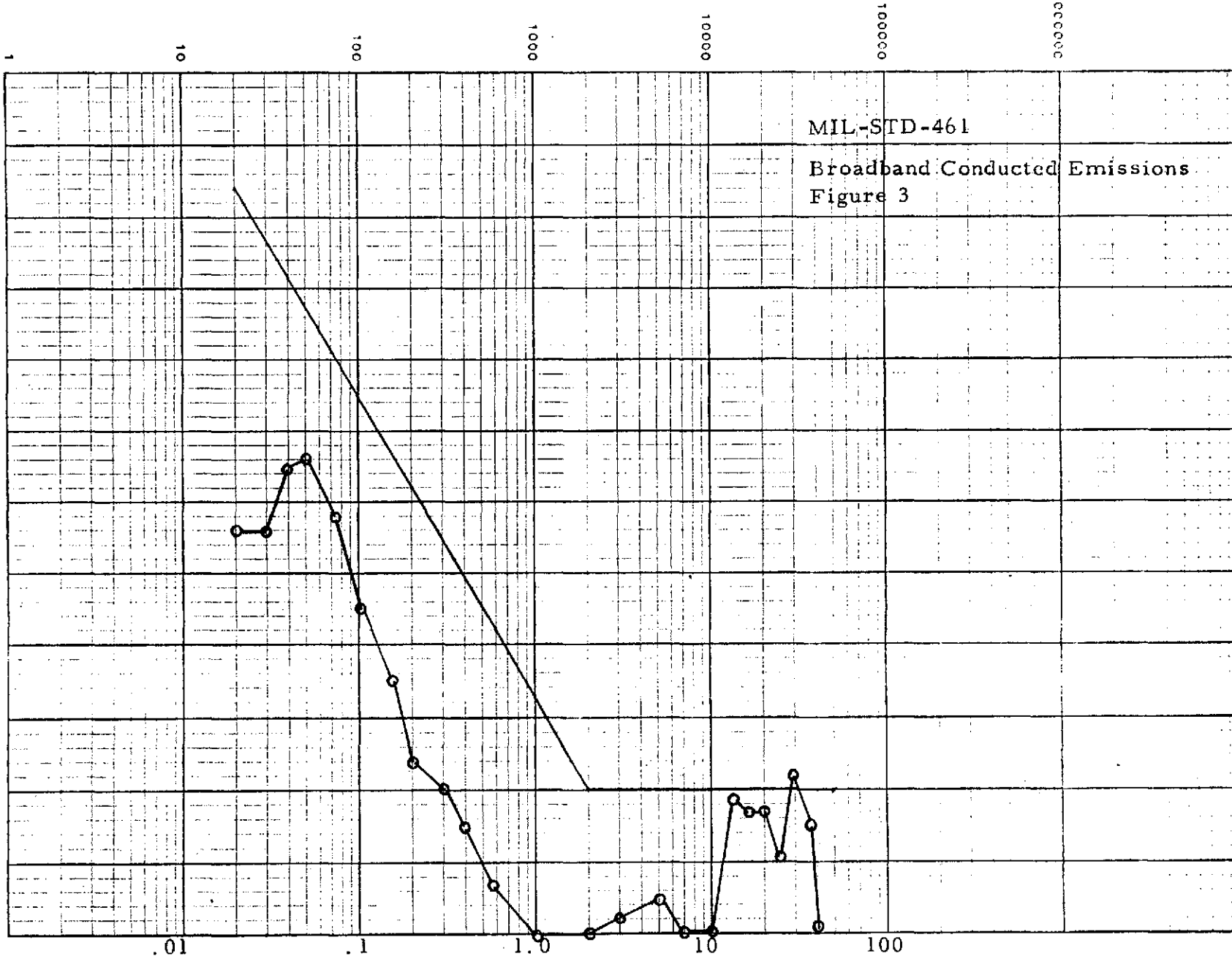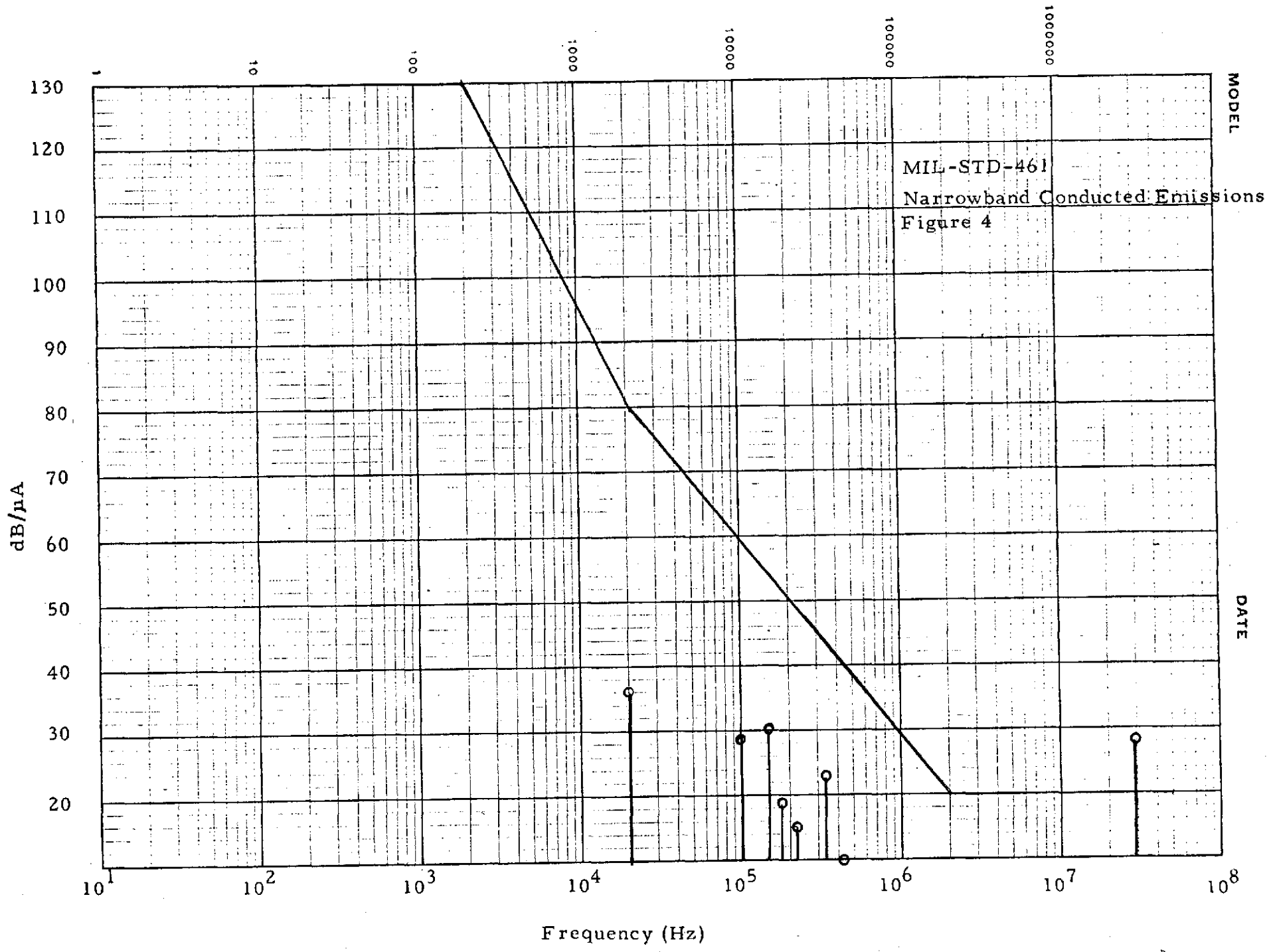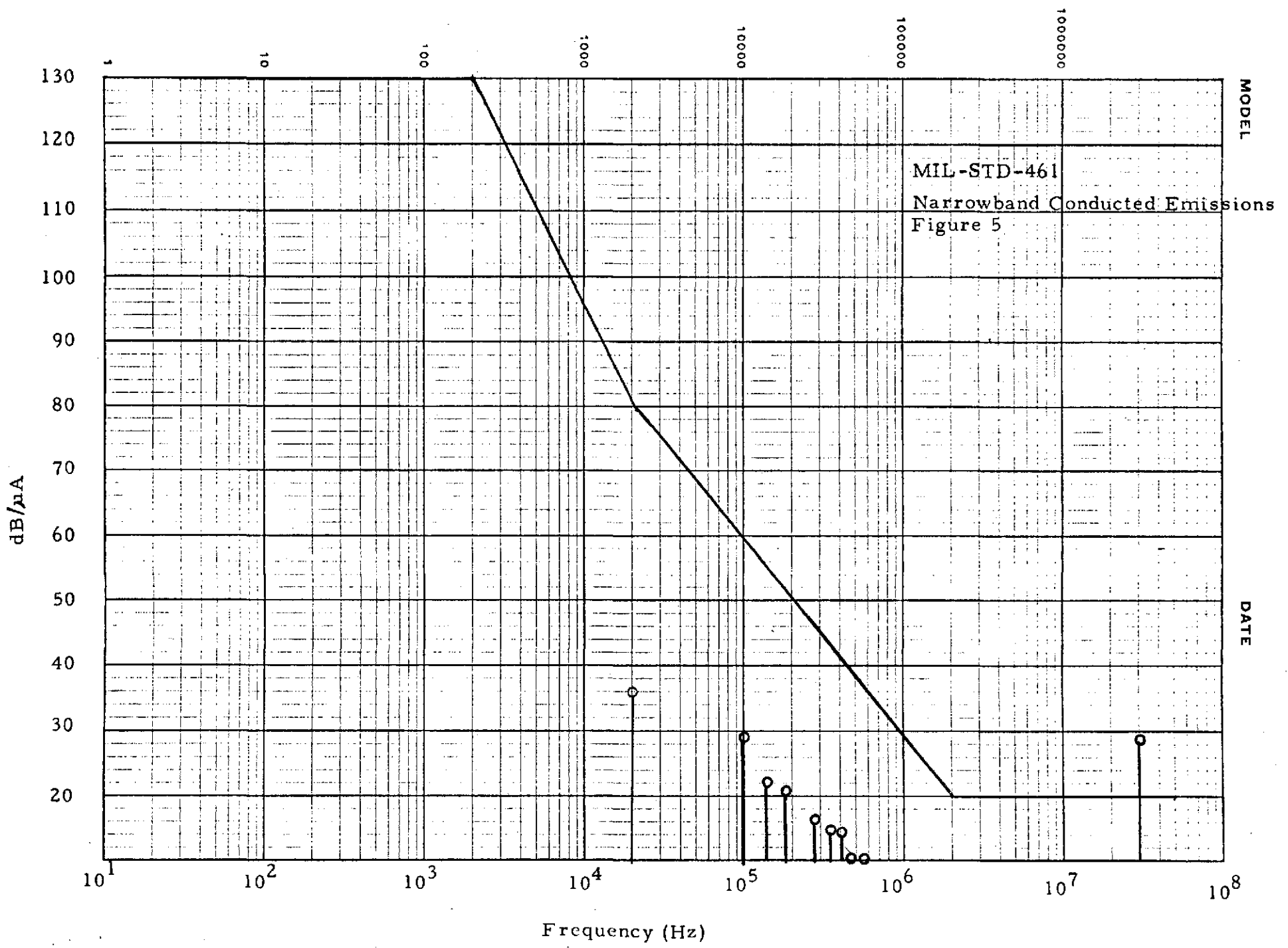
MODEL

DATE
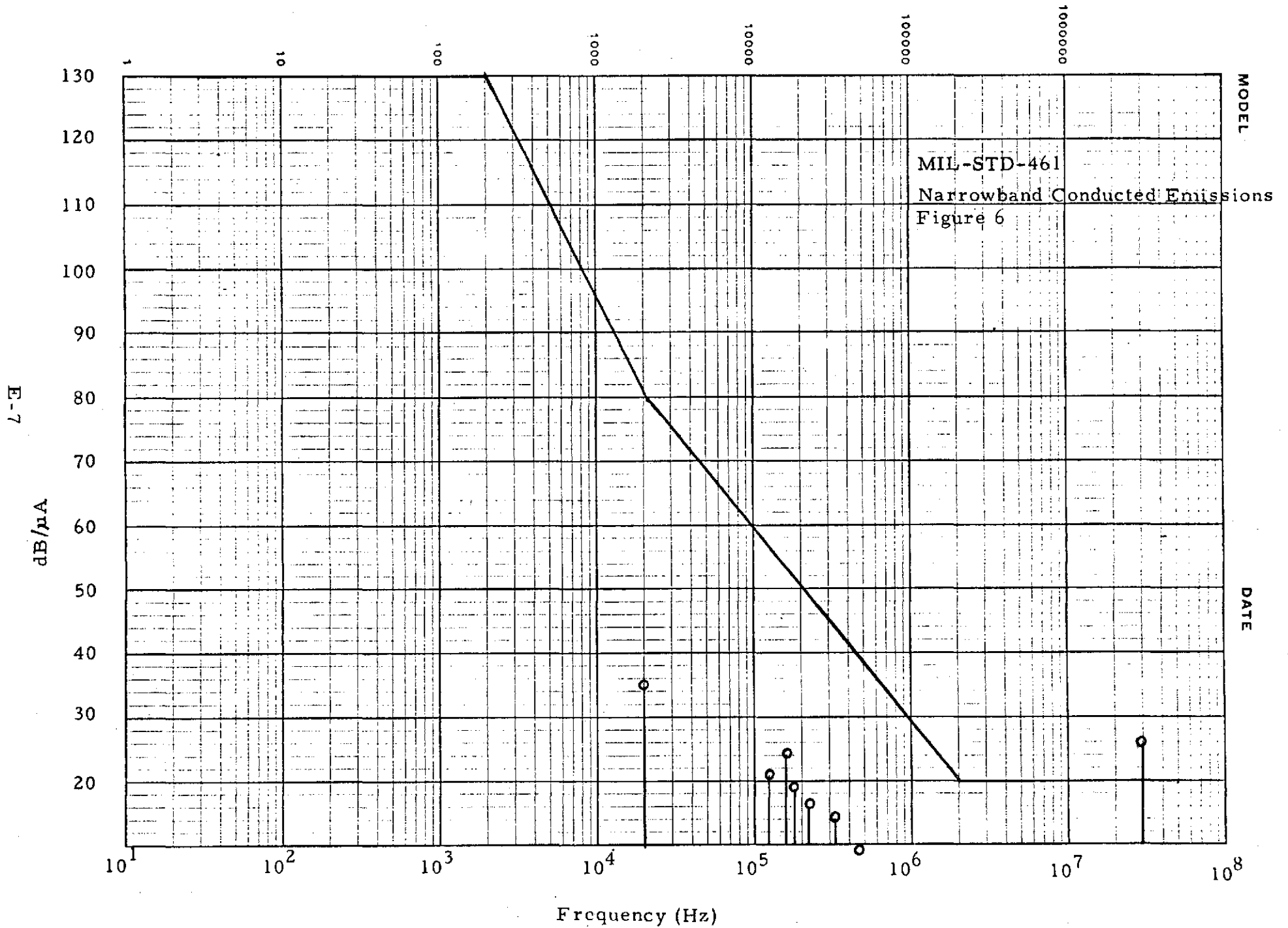
POWER SUPPLY PERFORMANCE CHARACTERISTICS

Line Regulation	±0.01%
Load Regulation	±0.01%
Overvoltage Trip	6.15 V
Undervoltage Trip	4.00 V
Worst Case Step Load Transient	0.75 V^2
Input Ripple	
Output Ripple	25 mV
Efficiency	76.6%

NOTES:

1. Measured utilizing remote sense

2. 0.5 to 100 percent load settling time   1.0 msec

3. Measured at full load, 24-volt input, with reverse polarity diode.
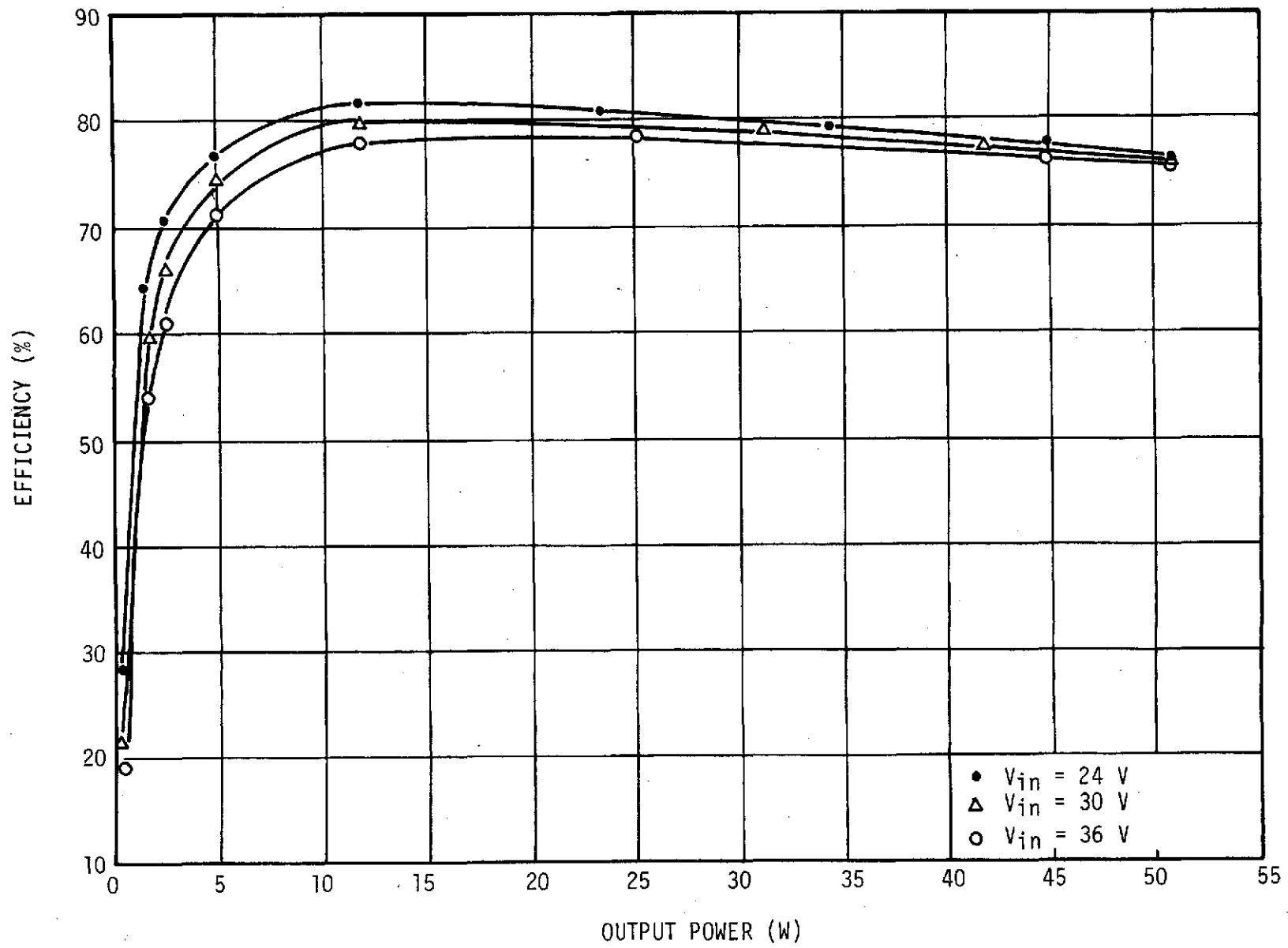
POWER SUPPLY STATIC PERFORMANCE DATA
INPUT VOLTAGE 24 VOLTS

INPUT CURRENT (A)	INPUT POWER (W)	OUTPUT VOLTAGE (V)	OUTPUT CURRENT (A)	OUTPUT POWER (W)	EFFICIENCY (%)
0.0325	0.780	5.044	0.0438	0.220	28.32
0.1086	2.606	5.044	0.3338	1.683	64.59
0.1480	3.552	5.044	0.4994	2.518	70.92
0.2703	6.487	5.044	0.991	4.998	77.05
0.6178	14.827	5.044	2.393	12.070	81.41
1.220	29.280	5.044	4.692	23.666	80.83
1.816	43.584	5.044	6.858	34.591	79.36
2.416	57.984	5.044	8.923	45.087	77.62
2.772	66.528	5.044	10.103	59.959	76.60
0.693	16.632	Short Circuit	11.420	-	-
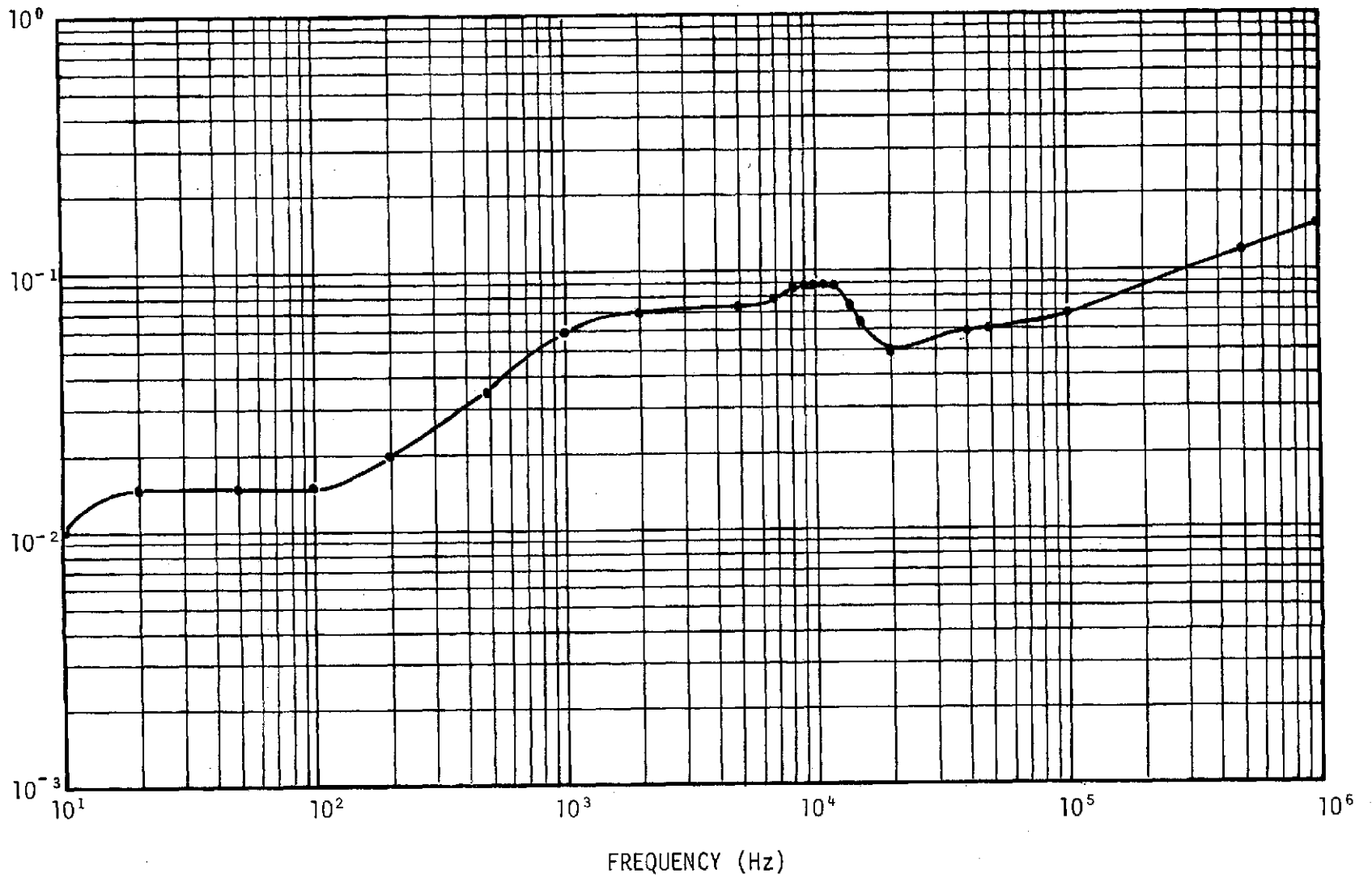
FREQUENCY (Hz)

OUTPUT IMPEDANCE AS A FUNCTION OF FREQUENCY

E-11

POWER SUPPLY STATIC PERFORMANCE DATA
INPUT VOLTAGE 30 VOLTS

INPUT CURRENT (A)	INPUT POWER (W)	OUTPUT VOLTAGE (V)	OUTPUT CURRENT (A)	OUTPUT POWER (W)	EFFICIENCY (%)
0.0343	1.029	5.044	0.0438	0.2209	21.47
0.0944	2.832	5.044	0.3336	1.6827	59.41
0.1275	3.825	5.044	0.4991	2.5175	65.81
0.2230	6.690	5.044	0.9914	5.0006	74.75
0.5033	15.044	5.044	2.393	12.0703	79.94
1.3287	39.861	5.044	6.250	31,5250	79.08
1.7995	53.985	5.044	8.334	42.0367	77.87
2.2220	66.660	5.044	10.100	50.9545	76.44
0.700	21.00	Short Circuit	11.92	-	-

POWER SUPPLY STATIC PERFORMANCE DATA
INPUT VOLTAGE 36 VOLTS

INPUT CURRENT (A)	INPUT POWER (W)	OUTPUT VOLTAGE (V)	OUTPUT CURRENT (A)	OUTPUT POWER (W)	EFFICIENCY (%)
0.0339	1.220	5.044	0.0437	0.2207	18.08
0.0856	3.083	5.044	0.3350	1.6822	54.55
0.1139	4.100	5.044	0.4989	2.4967	60.89
0.1946	7.006	5.044	0.9903	4.9951	71.29
0.4304	15.495	5.044	2.393	12.070	77.90
0.8903	32.051	5.044	5.011	25.277	78.86
1.6355	58.878	5.044	8.922	45.002	76.43
1.8638	67.097	5.044	10.100	50.944	75.92
0.683	24.59	Short Circuit	12.46	-	-
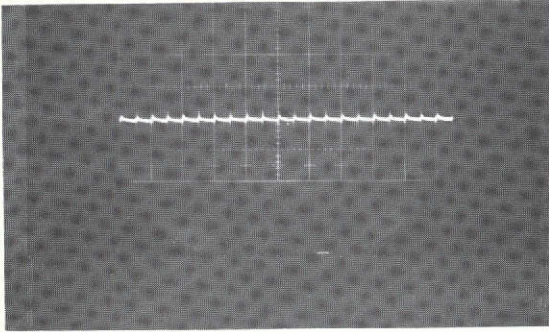
OUTPUT RIPPLE
VOLTAGE WAVEFORM AT 0.5% LOAD
50 mV/cm

TIME (50 μsec/cm)
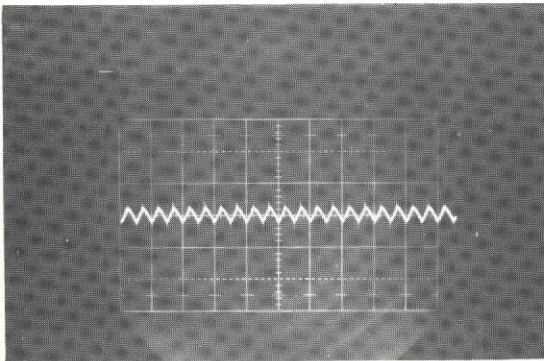
OUTPUT RIPPLE
VOLTAGE WAVEFORM AT 100% LOAD
50 mV/cm

TIME (50 μsec/cm)
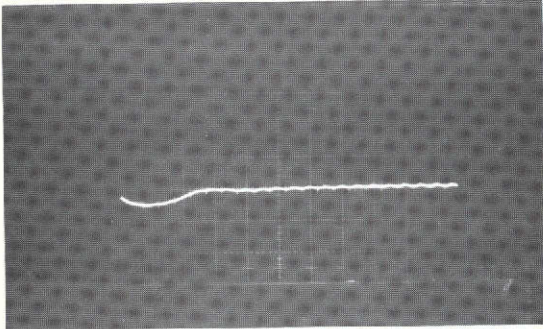
0.50 TO 50% LOAD
OUTPUT VOLTAGE
TRANSIENT WAVEFORM
(0.5 V/cm)

TIME (50 µsec/cm)
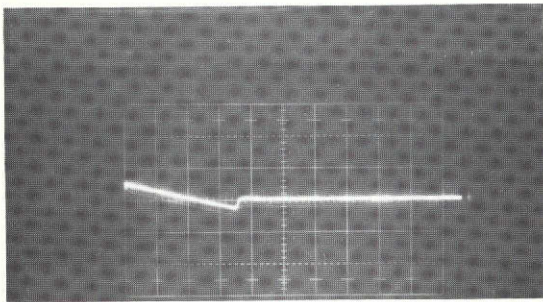
50 TO 0.5% LOAD
OUTPUT VOLTAGE
TRANSIENT WAVEFORM
(0.5 V/cm)

TIME (20 msec/cm)
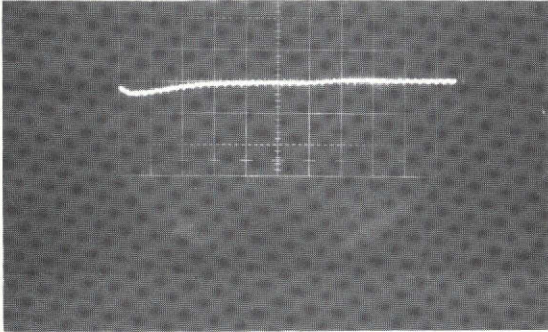
50 TO 100% LOAD
OUTPUT VOLTAGE
TRANSIENT WAVEFORM
(0.5 V/cm)

TIME (100 μsec/cm)
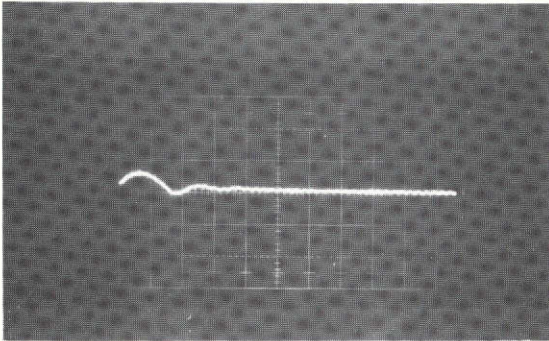
100 TO 50% LOAD
OUTPUT VOLTAGE
TRANSIENT WAVEFORM
(10.5 V/cm)

TIME (100 μsec/cm)
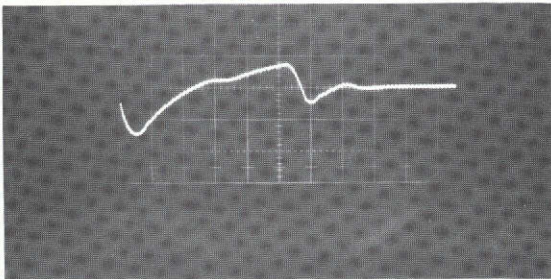
TIME (100 μsec/cm)

0.5 TO 100% LOAD
OUTPUT VOLTAGE
TRANSIENT WAVEFORM
(0.5 V/cm)
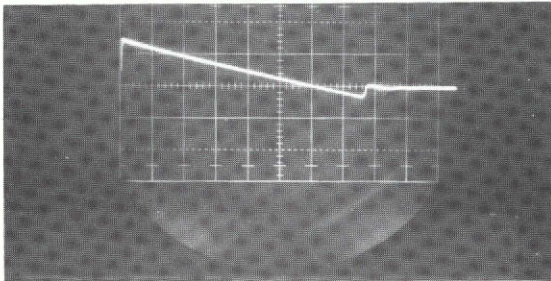
TIME (2 msec/cm)

100 TO 0.5% LOAD
OUTPUT VOLTAGE
TRANSIENT WAVEFORM
(0.5 V/cm)

APPENDIX F. MULTIPLE OUTPUT POWER SUPPLY DESIGN SPECIFICATION

EXHIBIT A - STATEMENT OF WORK

OBJECTIVE

The objective of this effort is the fabrication and delivery of a working breadboard model and a prototype model multiple output power supply.

APPROACH

The contractor shall supply the necessary personnel, services, materials, and facilities required to accomplish this effort.

- Task 1 - Fabricate and deliver a 5-volt, 50-watt bread-board power supply in general compliance with design goals contained herein. The breadboard shall be tested electrically to evaluate compliance with applicable portions of this Statement of Work. Results and data from this test shall be recorded and delivered to MSFC with the breadboard.

- Task 2 - Fabricate and deliver a prototype model of a multiple output power supply in accordance with specifications contained herein. The prototype model shall consist of four power modules with the following output voltages and power:

Modules	Voltage (V)	Power (W)
1 each	+28	100
1 each	+ 5	50
1 each	+15	100
1 each	-15	100

The prototype model shall be tested electrically to show compliance with applicable portions of this Statement of Work. Results and data from this test shall be recorded and delivered to MSFC with the prototype model.

Fault Detection and Indication

Provisions shall be incorporated into the power supply design to monitor those functions which would indicate that an internal failure has occurred or is likely to occur. In the event that a failure occurs, a

F-2

signal shall be generated by the supply to indicate that the failed supply is nonoperational. A failure is defined here as an undervoltage, out-of-tolerance of one or more output voltages, or a total loss of one or more voltages.

Orderly Startup and/or Shutdown

Some of the loads which the power supply will service must have operating voltage applied in a prescribed sequence. Also, in the event of a long duration primary power dropout wherein the output voltages of the power supply exceed allowable limits, it is necessary that the operating voltages be quickly removed from these loads in an orderly sequence. The design of the power supply shall include provisions to apply and/or remove the output voltages from loads such as those described above.

The shutdown shall be initiated by either of two events:

- Upon receipt of a logical zero volt at 100 mA with source impedance of 10 ohm and open circuit 15 volts

- Upon receipt of a +5-volt relay contact shutdown command from the LRU.

Reliability

The power supply shall provide highly reliable operation when used in any application for which it is designed. The supply shall have an analytically demonstrated mean-time-between-failure (MTBF) of 10,000 hours when operating in the environment defined herein.

Maintainability

The power supply will be used in large, manned space vehicles. Special attention shall be given to incorporating features into the design which will enhance the onboard maintainability of the units, using only those items of tools and test equipment which are available in the spacecraft. Replaceable subassemblies or modules shall be used to the greatest practical extent.

It is likely that ground tests and possibly in-flight tests which will be performed on the power supply will utilize automatic test equipment.

The design of the power supply shall incorporate those features which will enhance this type of checkout. Among other features which shall be considered are:

- Sufficient number of test points which indicate the status of various operating elements of the supply. All test points shall be protected against faults to each other and to ground.

- Test connectors which may provide quick access to the unit under test during checkout.

Electromagnetic Compatibility

The power supply shall be electromagnetically compatible with all equipment with which it interfaces. MIL-STD-461 and MIL-STD-462 shall be used as guidelines to establish the EMI limitations and test methods for the design of the supply.

ELECTRICAL REQUIREMENTS

Input Voltage Range

- Steady-state   24 to 36 Vdc
- Transient   Per MIL-STD-704A, except 50-V peak.

Ripple Feedback

When operating at full load, the power supply shall not cause a ripple current greater than that allowed by MIL-STD-461 to flow in the input lines.

Efficiency

The efficiency of the power supply shall be greater than 75 percent for full load operating conditions. A design goal for the efficiency shall be 85 percent under the same conditions.

The efficiency of the supply shall be determined by the following relation:

$$E_{ff} = \frac{P_{out}}{P_{in}} \times 100\%$$

where

$$P_{out} = P_{out_1} + P_{out_2} \cdots P_{out_n}$$

$$= (E_{out_1})\,(1_{out_1}) + (E_{out_2})\,(1_{out_2}) + \cdots (E_{out_n})(1_{out_n})$$

$$P_{in} = (E_{in})\,(1_{in}).$$

All voltages are measured at the power supply terminals.

OUTPUT CHARACTERISTICS

Output Power

The power supply shall be one design which is capable of supplying between 50 and 350 watts in the form of one or more output voltages, to multiple loads. The design shall be such that any load power which lies in the above-mentioned range can be serviced by one basic design which has modules or circuit cards added (or deleted) as necessary.

Output Voltages

The power supply shall have the output voltages shown in Table F-1. Since the outputs may be developed by circuits which have no provisions for precise adjustment, the output voltage may deviate from the nominal value by the tolerances shown in Table 1.

TABLE F-1. OUTPUT VOLTAGES

Output Number	1	2	3	4
Output Voltage, V	+15	-15	+28	+5
Initial Tolerance, %	±0.25	±0.25	±0.25	±0.25

Remote Sensing

A means shall be provided on each output of the supply by which the output voltage may be determined at either the load terminal or at the power supply output terminals. In the event that one or both of the

conductors which are used to sense the load voltage should fail open, the voltage of that output shall not rise more than 1 percent above the normal steady-state value. For purposes of circuit design and/or component selection, it may be assumed that the total voltage drop along any pair of power-carrying conductors will not exceed 1 volt.

Overvoltage Protection

Each of the outputs of the power supply shall have a means of detecting an overvoltage condition, which might cause damage to sensitive circuits in the loads, and immediately disabling the failed output. The allowable limits for the amplitude and duration of any output disturbance is shown in Table F-2.

TABLE F-2. MAXIMUM ALLOWABLE TRANSIENT VOLTAGE FOR
DURATION FOR OVERVOLTAGE PROTECTION

OUTPUT VOLTAGE (Vdc)	MAXIMUM VOLTAGE (V)	DURATION (msec)
+15	+5	5
-15	±5	5
+28	±9	5
+ 5	±1.7	5

Output Power Levels

The appropriate power allocation for each output voltage of the power supply is shown in Table F-3. The total output power from the supply will not exceed 350 watts.

TABLE F-3. POWER ALLOCATIONS FOR EACH OUTPUT WATT

Output, V	15	-15	+28	+5
Power, W	100	100	100	50

Load Transient Response

A step change (0 to 100 percent or 100 to 1 percent) in the load which is connected to any output of the power supply shall not cause a transient (overvoltage or undervoltage) which exceeds the nominal steady-state output voltage by more than the values shown in Table F-2. Any output voltage which is subjected to such a load transient shall recover to the allowed tolerance range (see Table F-4) within the time shown in Table F-2.

TABLE F-4. MAXIMUM ALLOWABLE ERROR FOR OUTPUT VOLTAGE

Output, V	+15	-15	+28	+5
Maximum Error, %	±2	±2	±2	±2

Voltage Tolerances

The steady-state output voltages of the power supply shall not vary from the nominal value by a deviation greater than the percentage shown in Table F-4. These deviations shall be the total of all error contributions from all possible steady-state sources, including the initial tolerances listed in Tables F-2 and F-3.

In the following paragraphs the tolerances specified for line regulation, load regulation, and temperature coefficients of the power supply outputs shall be used as design goals.

Line Regulation - When the input voltage is varied over the range of +24 to +36 volts, the change in the voltage of any output of the power supply shall not exceed the tolerance shown in Table F-5 for any load current within power limits of the supply.

TABLE F-5. LINE REGULATION

Voltage, V	+15	-15	+28	+5
Output Change (Percent of Nominal)	±0.2	±0.2	±0.2	±0.2

Load Regulation - When the load current of any output of the power
supply changes from the minimum value to the maximum value, the output
voltage change shall not exceed the tolerances shown in Table F-6. All out-
puts other than the test output shall be subjected to nominal loading.

TABLE F-6. STATIC LOAD REGULATION

Output, V	+15	-15	+28	+5
Voltage Change (Percent of Nominal Value)	±1	±1	±1	±1

Temperature Coefficients - The change in any of the output voltages
due to change in the ambient temperature shall not exceed 0.005 %/°C over
the temperature range of -20°C to +85°C.

Output Ripple Voltage

The ripple and noise voltage present on any of the outputs of the
power supply shall not exceed the values shown in Table F-7. The ripple and
noise voltages shall include any components due to switching transients
caused by preregulators and dc-to-dc converters, including "spikes" and
any other noise source except load transients. Measurement of the ripple
will be made with a wide bandwidth (dc to 50 MHz) oscilloscope and high
impedance probe at the output terminals of the power supply. Any compo-
nent of the ripple which appears on the common line shall be included in
the peak-to-peak measurement. This output shall be supplying full load
current to a fixed resistive load and the input voltage shall be adjusted
to +36 volts for this measurement.

TABLE F-7. OUTPUT RIPPLE

OUTPUT	+15 V	-15 V	+28 V	+5 V
Output Ripple Voltage Peak-to-Peak, mV	150	150	280	50

Output Impedance

For frequencies from 1 hertz (dc) to 100 hertz the output impedance of the power supply outputs shall not exceed the values shown in Table F-8. For frequencies from 100 hertz to 100 kilohertz, these output impedances shall not exceed six time the values shown in Table F-8.

TABLE F-8. OUTPUT IMPEDANCE (ohms)

Output	+15 V	-15 V	+28 V	+5 V
Maximum Output Impedance	(0.04)(Load Resistance) for each module over the operating range specified herein.			

Short Circuit Protection

Each of the outputs of the power supply shall be capable of withstanding a continuous short circuit or overcurrent load for any period of time at any specified operating temperature. When any one output is subjected to such a condition, the internal power dissipation of the supply shall not exceed that experienced during normal full load operation of the power supply by more than 10 percent. The values of current at which the outputs shall enter the current limiting mode will be 140 percent maximum of rated load. When the fault condition is removed, the voltage of the faulted output shall automatically recover to its steady-state value upon initiation of remote shutdown signal.

Output Commons

The common returns (grounds) for all outputs shall be isolated from each other by at least 20 kilohms. All commons shall be isolated from case ground. Each of the commons, including case ground, shall be brought out on a separate pin in the appropriate connector.

Input/Output Isolation - The power supply input common shall be isolated from all output commons by at least 10 megohms.

Power Supply Duty Cycle - The power supply shall be required to operate continuously under any combination of input/output conditions specified herein.

Environmental Conditions - The power supply shall provide the performance characteristics defined above when exposed to any combination of the following environmental factors. The power supply shall operate as defined herein when exposed to steady-state temperatures which lie in a range between -20°C to +85°C. The power supply shall be capable of withstanding storage temperatures which lie in a range between -55°C and +100°C without incurring damage.

REPORTING REQUIREMENTS

The Contractor shall submit a final report which documents and summarizes the results of the entire contract work, including recommendations and conclusions based on the experience and results obtained. The final report shall include tables, graphs, diagrams, curves, sketches, photographs, and drawings in sufficient detail to comprehensively explain the results achieved under the contract. This report shall be distributed to the addressees and in the quantities as cited below:

ORGANIZATION	NUMBER OF COPIES
A&PS-PR-RD	1
A&PS-MS-D	5
A&PS-TU	1
S&E-ASTR-EPC	2*
S&E-ASTR-RMH	1
S&E-ASTR-ZIR	1
TOTAL COPIES	11

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*This requirement in addition to one (1) reproducible master copy.

APPENDIX G. PROTOTYPE POWER SUPPLY DESIGN

NOTES:
1. UNLESS OTHERWISE SPECIFIED, DIODES ARE 1N5148.
2. UNLESS OTHERWISE SPECIFIED, RESISTORS ARE ±5%, 1/4W.

TELEDYNE BROWN ENGINEERING
Research Park • Huntsville, Alabama 35807

SCHEMATIC,
INPUT MODULE ASSEMBLY
& ... POWER SUPPLY

SIZE E   CODE IDENT NO. 14925   DWG NO. 21011

G-3
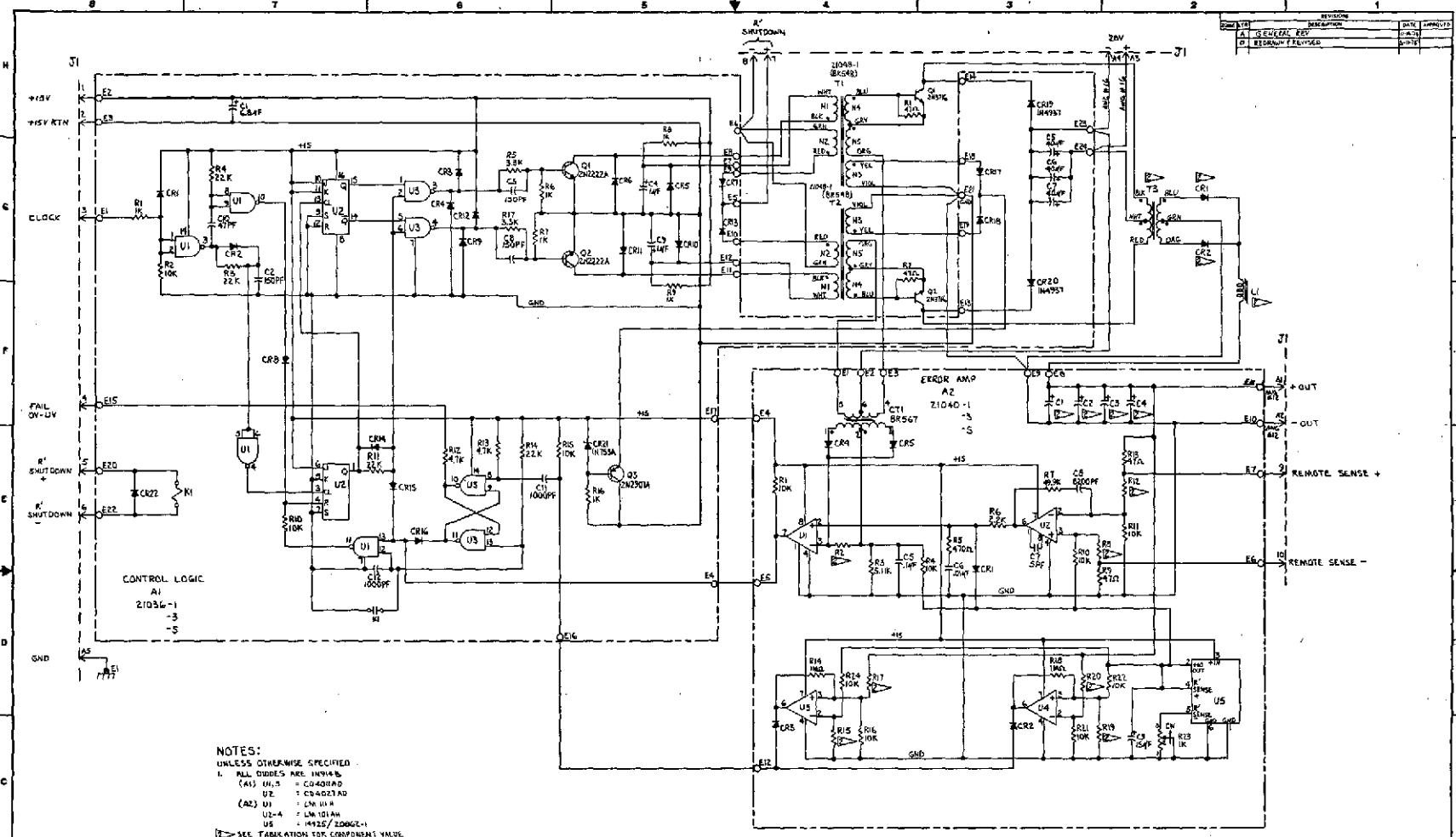
NOTES:
UNLESS OTHERWISE SPECIFIED:
1. ALL WIRE TO BE AWG #20

CONTROL

ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	REVISED	2-26-76	

REVISIONS

TELEDYNE BROWN ENGINEERING
Research Park • Huntsville, Alabama 35807

TITLE: SCHEMATIC

MULTI-OUTPUT POWER SUPPLY

SIZE	CODE IDENT NO.	DWG. NO.
D	14925	21003

ZONE	LTR	DESCRIPTION	DATE	APPROVED
		REVISIONS		

4.80 REF

2.53 REF

14925 ASSY 21021-1

27 7 PLACES

NOTES:

1. PRINTED WIRING ASSEMBLY SHALL BE CONSTRUCTED PER GOOD COMMERCIAL PRACTICE

2. PARTIAL REF DES ARE SHOWN, FOR COMPLETE REF DES PREFIX WITH ASSEMBLY NO.

3. REFERENCE DRAWINGS:
   SCHEMATIC E21011
   PRINTED WIRING BOARD C21023

4. RUBBER STAMP MFG CODE AND ASSY NO. APPROX AS SHOWN USING .12 HIGH CHARACTERS
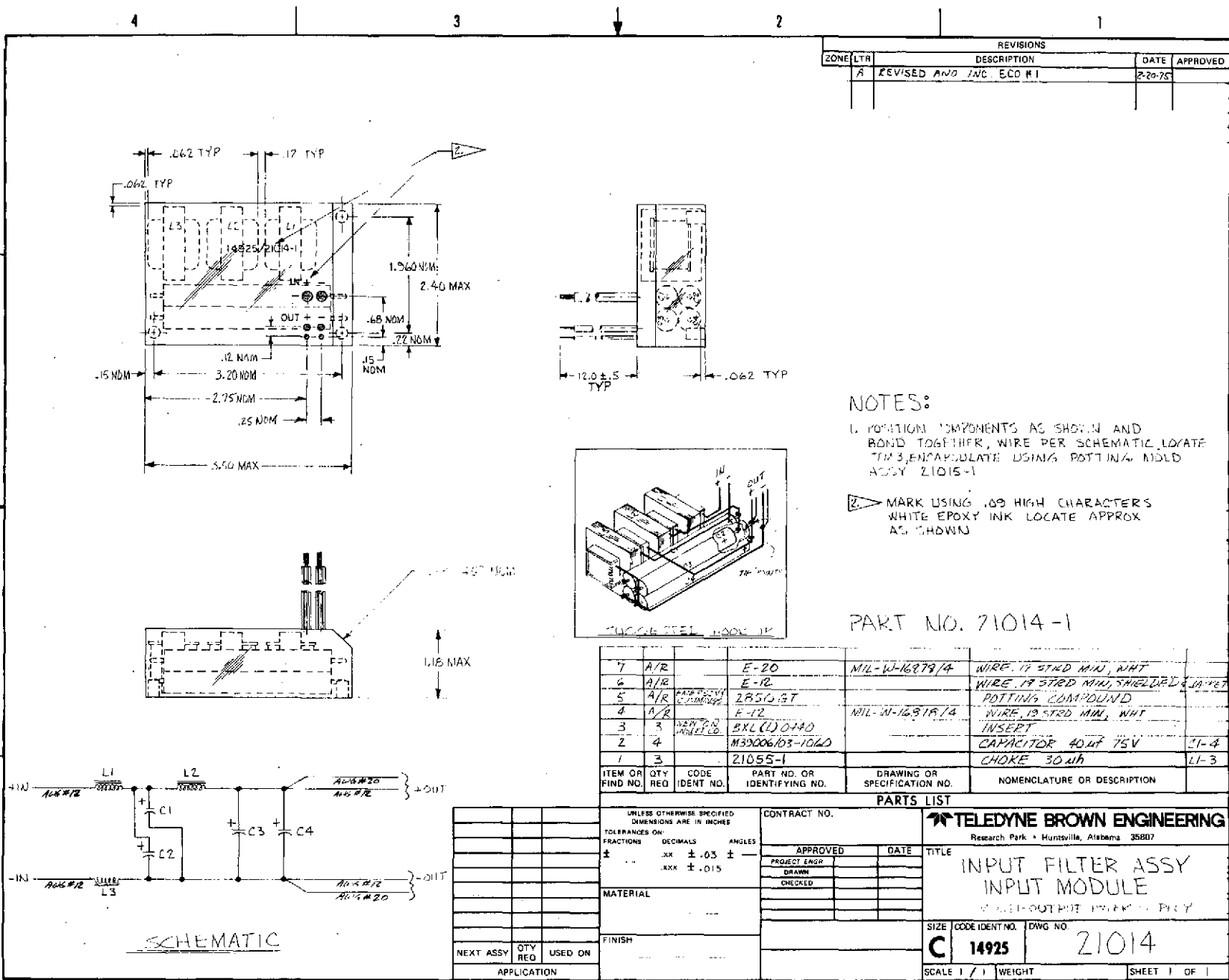
5. BOND ITEM 8 TO ITEM 1 USING ITEM 28 PER MFG INSTRUCTIONS
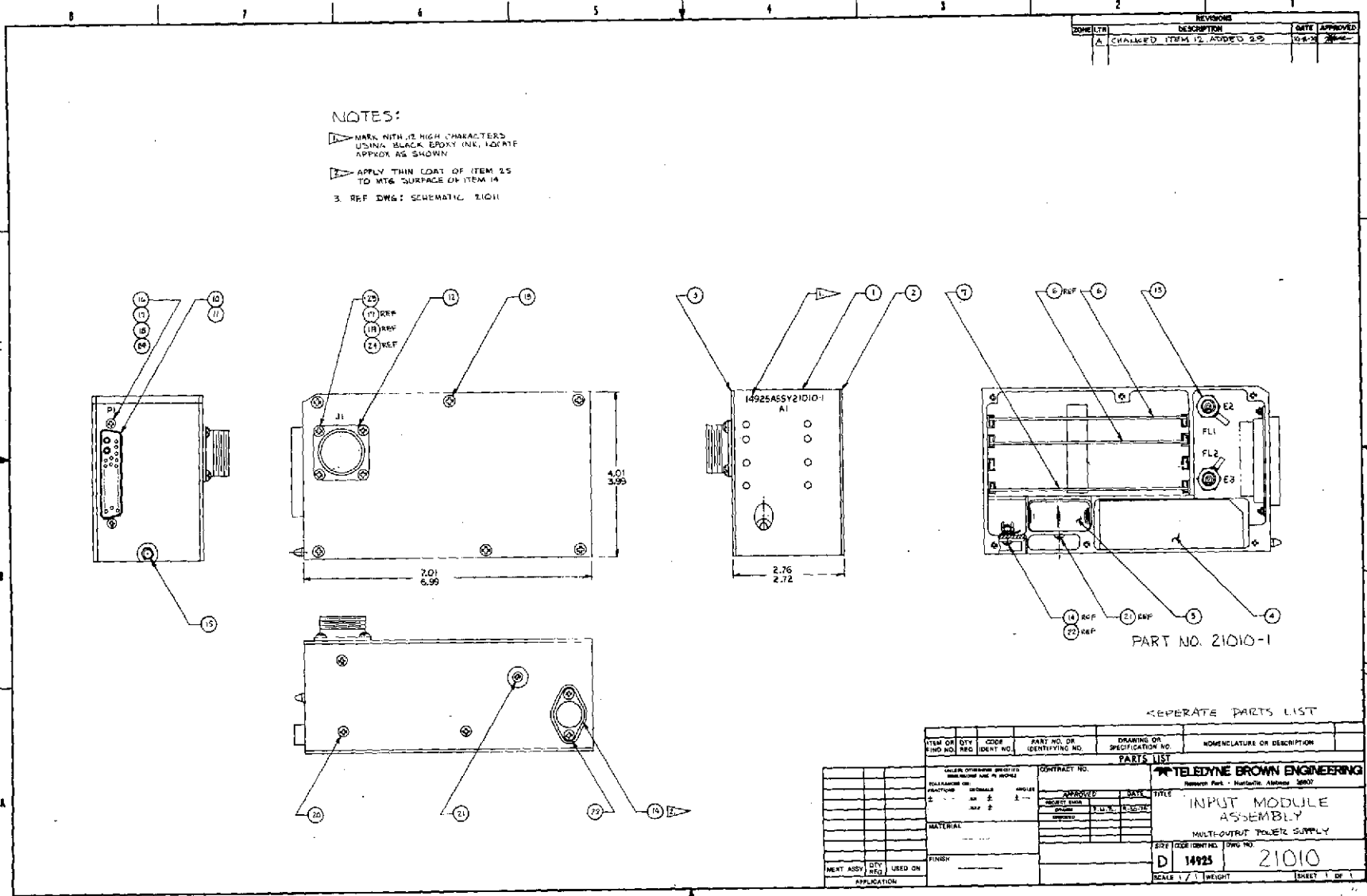
−1 SHOWN

SEPARATE PARTS LIST SEE APL 21021

ITEM OR FIND NO.	QTY REQ	CODE IDENT NO.	PART NO. OR IDENTIFYING NO.	DRAWING OR SPECIFICATION NO.	NOMENCLATURE OR DESCRIPTION
				PARTS LIST	

TELEDYNE BROWN ENGINEERING

Research Park • Huntsville, Alabama 35807

TITLE

PRINTED WIRING ASSEMBLY

HOUSEKEEPING REG INV

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CONTRACT NO.
TOLERANCES ON:	
FRACTIONS DECIMALS ANGLES	
± ~ xx ± ~ ± ~	APPROVED DATE
xxx ± ~	PROJECT ENGR
	DRAWN BB 10-27-74
MATERIAL	CHECKED
~	

SIZE	CODE IDENT NO.	DWG NO.
C	14925	21021

| SCALE 2/1 | WEIGHT ~ | SHEET 1 OF 1 |

FINISH ~

NEXT ASSY   QTY REQ   USED ON

APPLICATION

FORM NO. 2372

4   3   2   1

ZONE	LTR	REVISIONS DESCRIPTION	DATE	APPROVED

4.80 REF

2.53 REF

E1
E3
E8
E5
E18
E7 E6
E2
E4 E9 E11 E16 E17 E13
E19
E15 E14
E10
E12
E20

R2
R5

K1
K2

CR3
R3
CR4
C1
CR5
C3
C4
C2
Q1

CR6
CR7
CR8
R6
C5
CR10
C7
C8
R8
Q2

R1
R4

CR2
CR1

14925 ASSY 21017-1

1

11 2 PLACES

NOTES:

1. PRINTED WIRING ASSEMBLY SHALL BE CONSTRUCTED PER GOOD COMMERCIAL PRACTICE

2. PARTIAL REF DES ARE SHOWN, FOR COMPLETE REF DES PREFIX WITH ASSEMBLY NO.

3. REFERENCE DRAWINGS:
   SCHEMATIC E21011
   PRINTED WIRING BOARD C21019

-1 SHOWN
SEPARATE PARTS LIST SEE APL 21017

ITEM OR FIND NO.	QTY REQ	CODE IDENT NO.	PART NO. OR IDENTIFYING NO.	DRAWING OR SPECIFICATION NO.	NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON:
FRACTIONS   DECIMALS   ANGLES
± ~   .xx ± ~   ± ~
.xxx ± ~

MATERIAL ~

FINISH ~

NEXT ASSY | QTY REQ | USED ON

APPLICATION

CONTRACT NO.

APPROVED	DATE
PROJECT ENGR	
DRAWN	10-27-74
CHECKED	

TELEDYNE BROWN ENGINEERING
Research Park • Huntsville, Alabama 35807

TITLE
PRINTED WIRING ASSEMBLY
HOUSEKEEPING RECT FILTER

SIZE	CODE IDENT NO.	DWG NO.
C	14925	21017

SCALE 2/1 | WEIGHT ~ | SHEET 1 OF 1

FORM NO. 332

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

4.380 REF

3.75 REF

14925 ASSY 21036-[ ]

22

21 3 PLACES

NOTES:

1. PRINTED WIRING ASSEMBLY SHALL BE CONSTRUCTED PER GOOD COMMERCIAL PRACTICE
2. PARTIAL REF DES ARE SHOWN, FOR COMPLETE REF DES PREFIX WITH ASSEMBLY NO.
3. REFERENCE DRAWINGS:
    SCHEMATIC E21026
    PRINTED WIRING BOARD C21038
4. RUBBER STAMP APPROPRIATE DASH NO. USING .12 HIGH CHARACTERS

-1,-3,-5 SHOWN

ASSEMBLE PER SEPARATE PARTS LIST SEE APL 21036

ITEM OR FIND NO.	QTY REQ	CODE IDENT NO.	PART NO. OR IDENTIFYING NO.	DRAWING OR SPECIFICATION NO.	NOMENCLATURE OR DESCRIPTION	
				PARTS LIST		

CONTRACT NO.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON:
FRACTIONS   DECIMALS   ANGLES
± ~   .xx ± ~   ± ~
.xxx ± ~

APPROVED	DATE
PROJECT ENGR	
DRAWN	10-21-74
CHECKED	

TELEDYNE BROWN ENGINEERING
Research Park • Huntsville, Alabama 35807

TITLE
PRINTED WIRING ASSEMBLY
CONTROL LOGIC

MATERIAL ~

FINISH ~

SIZE	CODE IDENT NO.	DWG NO.
C	14925	21036

SCALE 2/1   WEIGHT ~   SHEET 1 OF 1

NEXT ASSY | QTY REQ | USED ON
APPLICATION

FORM NO. 2272

4   3   2   1

ZONE	LTR	DESCRIPTION	DATE	APPROVED

4.445 REF

3.75 REF

14925 ASSY 21040-

E1
E2
E3
CT1
U5
R23
C9
R24 R22
35
E4   CR4 CR5
R7
34 4 PLACES
E5   U1   R1 R6   C7   U2   U3   U4   E12
R2   R5   R15   R18
C6   C8 R11 R12 R8 R10   R14   R19   CR2 CR3
R9   R16   R21
CR1   R13   R17   R20
E6   R14
E7   R4   R3   C1   +   −   C3   +
C2   +   −   C4   +
E8   E9 E10   E11

NOTES:

1. PRINTED WIRING ASSEMBLY SHALL BE
   CONSTRUCTED PER GOOD COMMERCIAL
   PRACTICE

2. PARTIAL REF DES ARE SHOWN, FOR
   COMPLETE REF DES PREFIX WITH
   ASSEMBLY NO.

3. REFERENCE DRAWINGS:
        SCHEMATIC E21026
        PRINTED WIRING BOARD C21042

4. RUBBER STAMP APPROPRIATE DASH NO.
   USING .12 HIGH CHARACTERS

-1, -3, -5 SHOWN

ASSEMBLE PER SEPARATE PARTS LIST SEE APL 21040

ITEM OR FIND NO.	QTY REQ	CODE IDENT NO.	PART NO. OR IDENTIFYING NO.	DRAWING OR SPECIFICATION NO.	NOMENCLATURE OR DESCRIPTION	

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

TOLERANCES ON:
FRACTIONS   DECIMALS   ANGLES
±～   .XX ±～   ±～
            .XXX ±～

CONTRACT NO.

APPROVED	DATE
PROJECT ENGR	
DRAWN	10-27-74
CHECKED	

MATERIAL   ～

FINISH   ～

TELEDYNE BROWN ENGINEERING
Research Park • Huntsville, Alabama 35807

TITLE

PRINTED WIRING ASSEMBLY
ERROR AMPLIFIER

SIZE	CODE IDENT NO.	DWG NO.
C	14925	21040

SCALE 2/1   WEIGHT ～   SHEET   OF

NEXT ASSY	QTY REQ	USED ON

APPLICATION

G-9

TELEDYNE BROWN ENGINEERING

PART NO.
2100 2-1

PARTS LIST

SEPARATE PARTS LIST

PART NO. 21008-1

NOTES:
1. REMOVE BURRS AND BREAK ALL SHARP EDGES
2. RUBBER STAMP OR STENCIL WITH .12 HIGH CHARACTERS USING BLACK EPOXY INK. LOCATE APPROX AS SHOWN

| 4 | 3 | 2 | 1 |

ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	REVISED AND INC. ECO #1	2-20-75	

.062 TYP   .17 TYP

.062 TYP

14925/21014-1

IN ±

OUT +

1.060 NOM
2.40 MAX

.68 NOM
.22 NOM

.15 NOM
.12 NOM
3.20 NOM
2.75 NOM
.25 NOM
.15 NOM

5.50 MAX

12.0 ±.5 TYP   .062 TYP

1.18 MAX

NOTES:

1. POSITION COMPONENTS AS SHOWN AND BOND TOGETHER, WIRE PER SCHEMATIC. LOCATE ITM 3, ENCAPSULATE USING POTTING MOLD ASSY 21015-1

2. MARK USING .09 HIGH CHARACTERS WHITE EPOXY INK LOCATE APPROX AS SHOWN

PART NO. 21014-1

ITEM OR FIND NO.	QTY REQ	CODE IDENT NO.	PART NO. OR IDENTIFYING NO.	DRAWING OR SPECIFICATION NO.	NOMENCLATURE OR DESCRIPTION	
7	A/R		E-20	MIL-W-16878/4	WIRE, 19 STRD MIN, WHT	
6	A/R		E-12		WIRE, 19 STRD MIN, SHIELDED JACKET	
5	A/R		2850 GT		POTTING COMPOUND	
4	A/R		E-12	MIL-W-16878/4	WIRE, 19 STRD MIN, WHT	
3	3		BXL(1) 0440		INSERT	
2	4		M39006/03-1060		CAPACITOR 40 uf 75V	J1-4
1	3		21055-1		CHOKE 30 uh	L1-3

PARTS LIST

SCHEMATIC

+IN L1 L2 +OUT
C1 C3 C4
C2
-IN L3 -OUT

TELEDYNE BROWN ENGINEERING
Research Park • Huntsville, Alabama 35807

TITLE: INPUT FILTER ASSY INPUT MODULE

SIZE	CODE IDENT NO.	DWG NO.
C	14925	21014

SCALE 1/1 | WEIGHT | SHEET 1 OF 1

NOTES:

1. MARK WITH .12 HIGH CHARACTERS USING BLACK EPOXY INK, LOCATE APPROX AS SHOWN

2. APPLY THIN COAT OF ITEM 25 TO MTG SURFACE OF ITEM 14

3. REF DWG: SCHEMATIC 21011

14925 ASSY 21010-1
A1

PART NO. 21010-1

4.01 / 3.99
2.01 / 6.99
2.76 / 2.72

E2
FL1
FL2
E3

SEPERATE PARTS LIST

ITEM OR FIND NO.	QTY REQ	CODE IDENT NO.	PART NO. OR IDENTIFYING NO.	DRAWING OR SPECIFICATION NO.	NOMENCLATURE OR DESCRIPTION
				PARTS LIST	

TELEDYNE BROWN ENGINEERING
Research Park · Huntsville, Alabama 35807

TITLE
INPUT MODULE ASSEMBLY
MULTI-OUTPUT POWER SUPPLY

SIZE	CODE IDENT NO.	DWG NO.
D	14925	21010

SCALE 1/1   WEIGHT   SHEET 1 OF 1

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	CHANGED ITEM 12, ADDED 25		

NOTES:
1. REMOVE BURRS AND BREAK SHARP EDGES
2. ALL RADII .12 UNLESS OTHERWISE SPECIFIED
3. INTERNAL CORNERS EQUAL TOOL RADII
4. INSTALL PER MSFC-STD-156
5. MARK WITH .12 HIGH CHARACTERS USING
   BLACK EPOXY INK LOCATE APPROX AS SHOWN
   ☐ INDICATES FARSIDE

PART NO. 21013-1

ITEM OR FIND NO	QTY REQ	CODE IDENT NO	PART NO. OR IDENTIFYING NO.	DRAWING OR SPECIFICATION NO.	NOMENCLATURE OR DESCRIPTION
3	16		MS20426ADZ-3		RIVET
2	8	07387	35-25-2-4		CARD GUIDE
1	1		21013-3		CHASSIS

PARTS LIST

TELEDYNE BROWN ENGINEERING
Research Park · Huntsville, Alabama 35807

TITLE
CHASSIS ASSY
INPUT MODULE
MULTI OUTPUT POWER SUPPLY

SIZE	CODE IDENT NO.	DWG NO
D	14925	21013

SCALE 1/1   WEIGHT   SHEET 1 OF 1

MATERIAL
AL ALY 6061-T6
PER QQ-A-250/11

FINISH
7.3.1 PER MIL-STD-171
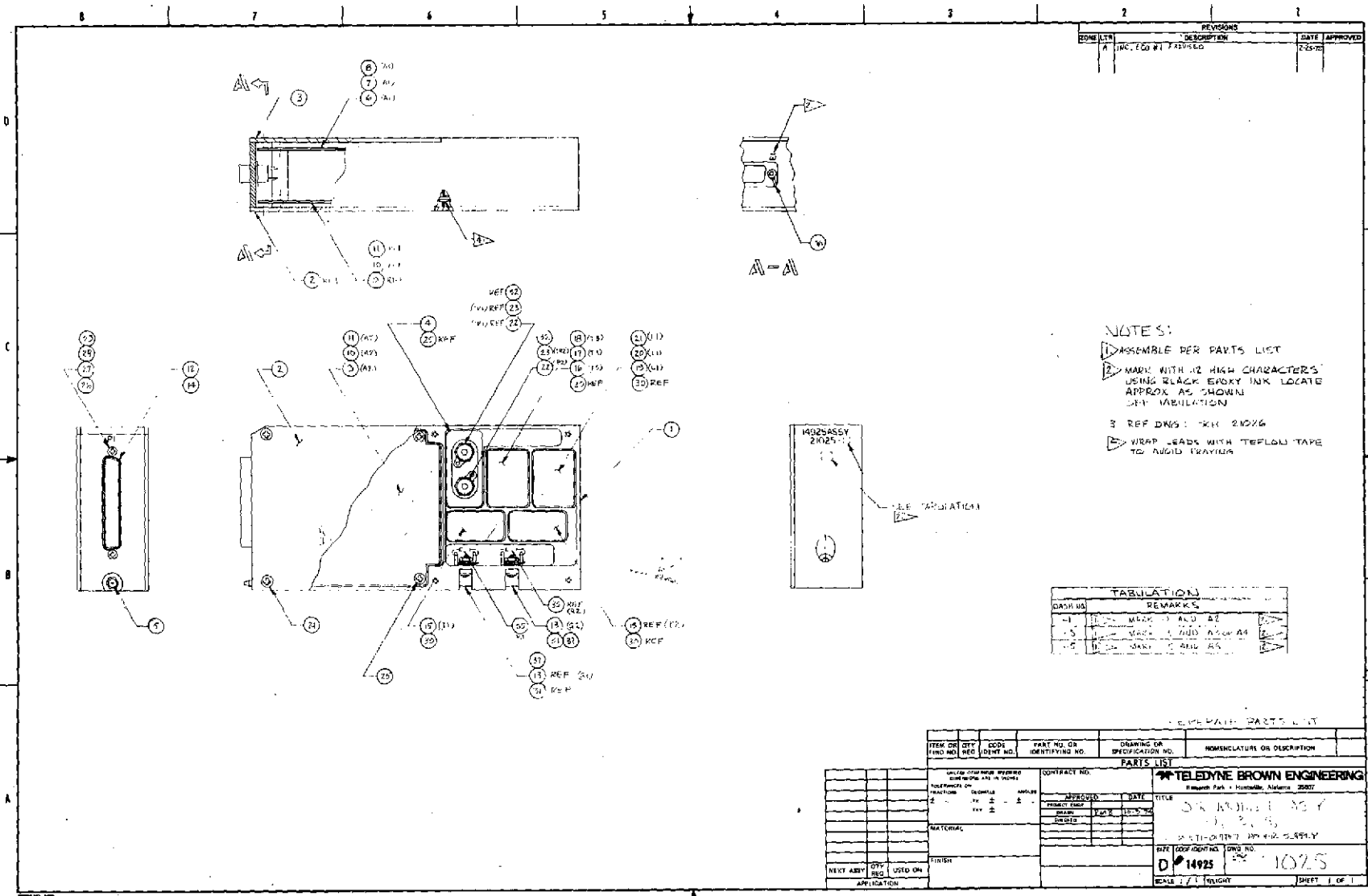
NOTES:
1. ASSEMBLE PER PARTS LIST
2. MARK WITH .12 HIGH CHARACTERS USING BLACK EPOXY INK LOCATE APPROX AS SHOWN SEE TABULATION
3. REF DWG: SCH 21026
4. WRAP LEADS WITH TEFLON TAPE TO AVOID FRAYING

14925 ASSY 21025

SEE TABULATION

A-A

TABULATION		
DASH NO.	REMARKS	
-1	MARK -1 AND A2	
-3	MARK -3 AND A3 & A4	
-5	MARK -5 AND A5	

SEPARATE PARTS LIST

PARTS LIST

ITEM OR FIND NO.	QTY REQD	CODE IDENT NO.	PART NO. OR IDENTIFYING NO.	DRAWING OR SPECIFICATION NO.	NOMENCLATURE OR DESCRIPTION

TITLE

SIZE	CODE IDENT NO.	DWG NO.
D	14925	21025

SCALE	WEIGHT	SHEET 1 OF 1

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	INC. ECO #1 REVISED	2-25-75	

A-A

B-B

PART NO. 21032-1

NOTES:

1. REMOVE BURRS AND BREAK SHARP EDGES

PARTS LIST

TELEDYNE BROWN ENGINEERING
Research Park • Huntsville, Alabama 35807

| D | 14925 | 21032 |

APPENDIX H.   PROTOTYPE POWER SUPPLY
TEST REPORT

I. EMI TEST

Interference tests were run on the NASA power supply. The line voltage input was 28 volts and the supply was operated at full load. MIL-STD-461 was used as a reference guide to performance.

TEST RESULTS

Broadband Conducted Emissions (CE03) Input Power Lines

The test results are shown in Figure H-1. The power supply is well within the required limits of either Notice 1 or Notice 3.

Narrowband Conducted Emissions (CE03)

The test results are shown for the 28-volt input and 28-volt return in Figures H-2 and H-3. The results show that the supply is over the limit specified in MIL-STD-461 by about 14 decibels at 150 kilohertz and 7 decibels at 100 kilohertz. Emissions at either frequency are within the specification.

Broadband Radiated Emissions (RE02)

The broadband emission measured from the supply are shown in Figure H-4. There were no measurable responses in the required passband.

Narrowband Emissions (RE02)

The narrowband emissions are shown in Figure H-5. The tests indicate an out-of-specification response of 4 decibels at 38 kilohertz and 6 decibels at 14 megahertz. Acceptable performances were achieved at all other frequencies. It would appear from the data that the cause of the radiated emissions was due to the unshielded load bank present with the power supply. A more favorable test would be to shield the load bank.
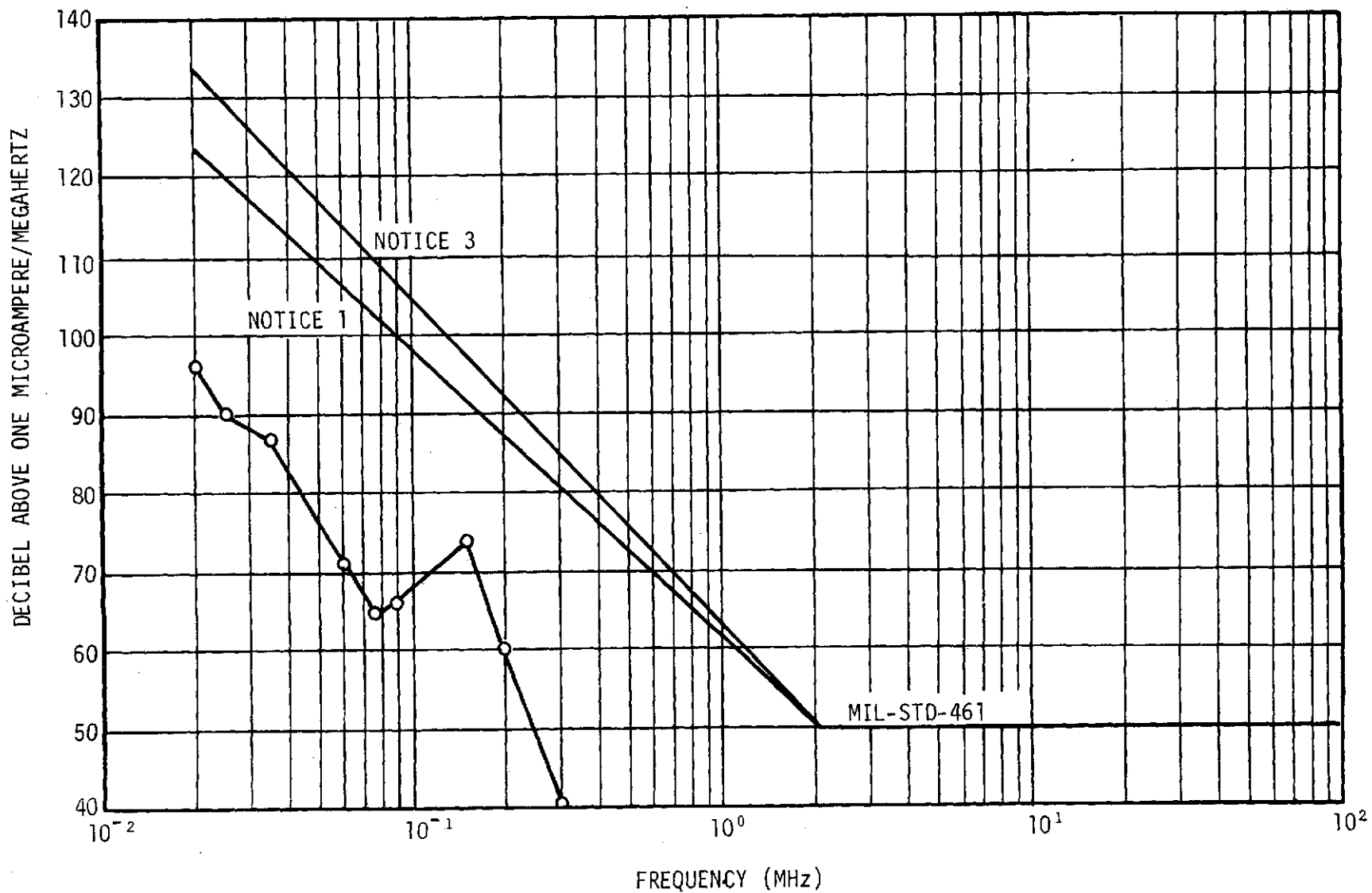
FIGURE H-1. CONDUCTED INTERFERENCE LIMITS, 20 KILOHERTZ TO 50 MEGAHERTZ

FIGURE H-2

FIGURE H-3

TEST ITEM: OPTIMUM POWER SUPPLY
TEST DESCRIPTION: BROADBAND RADIATED EMISSIONS
TEST METHOD RE02
MIL-STD-461
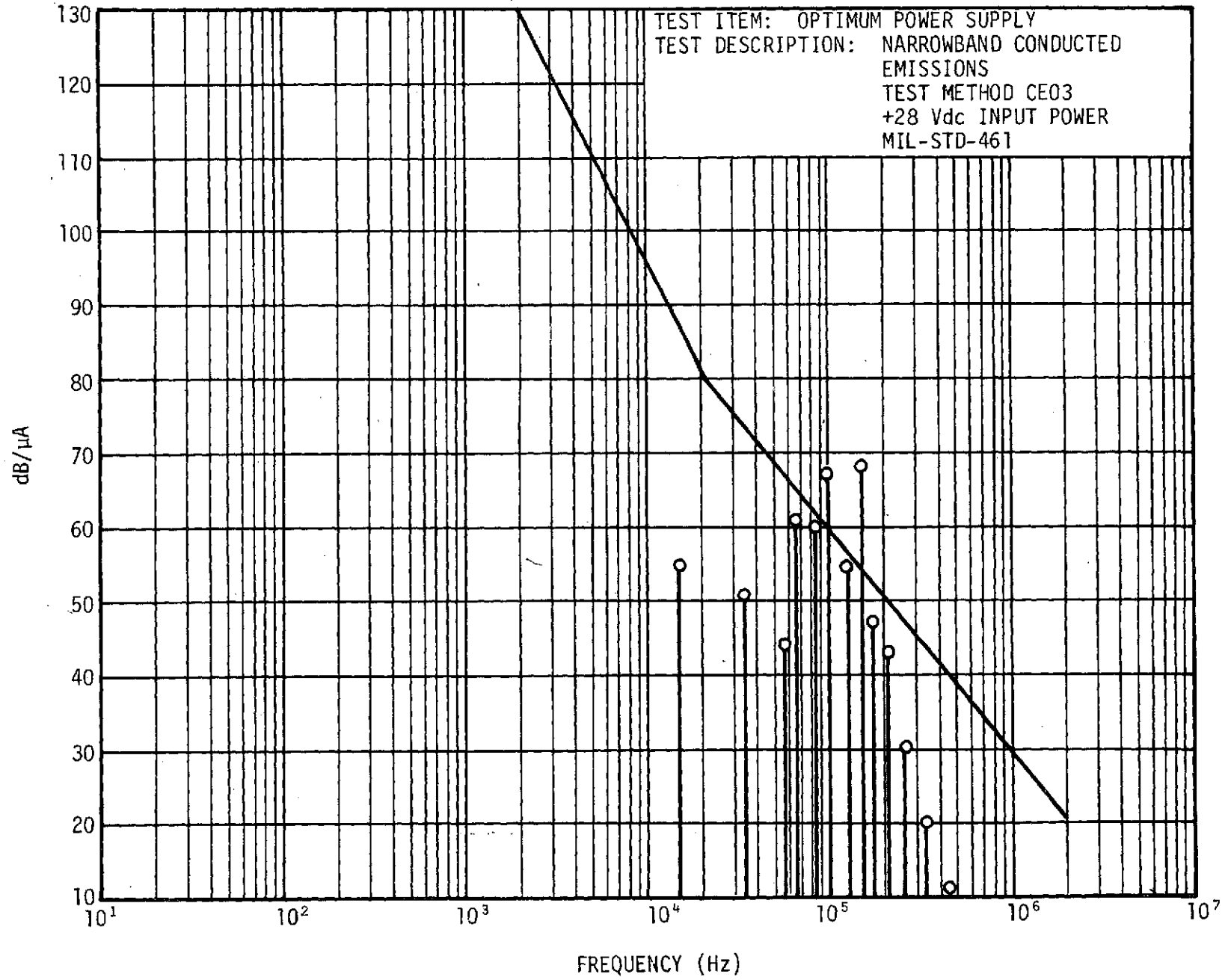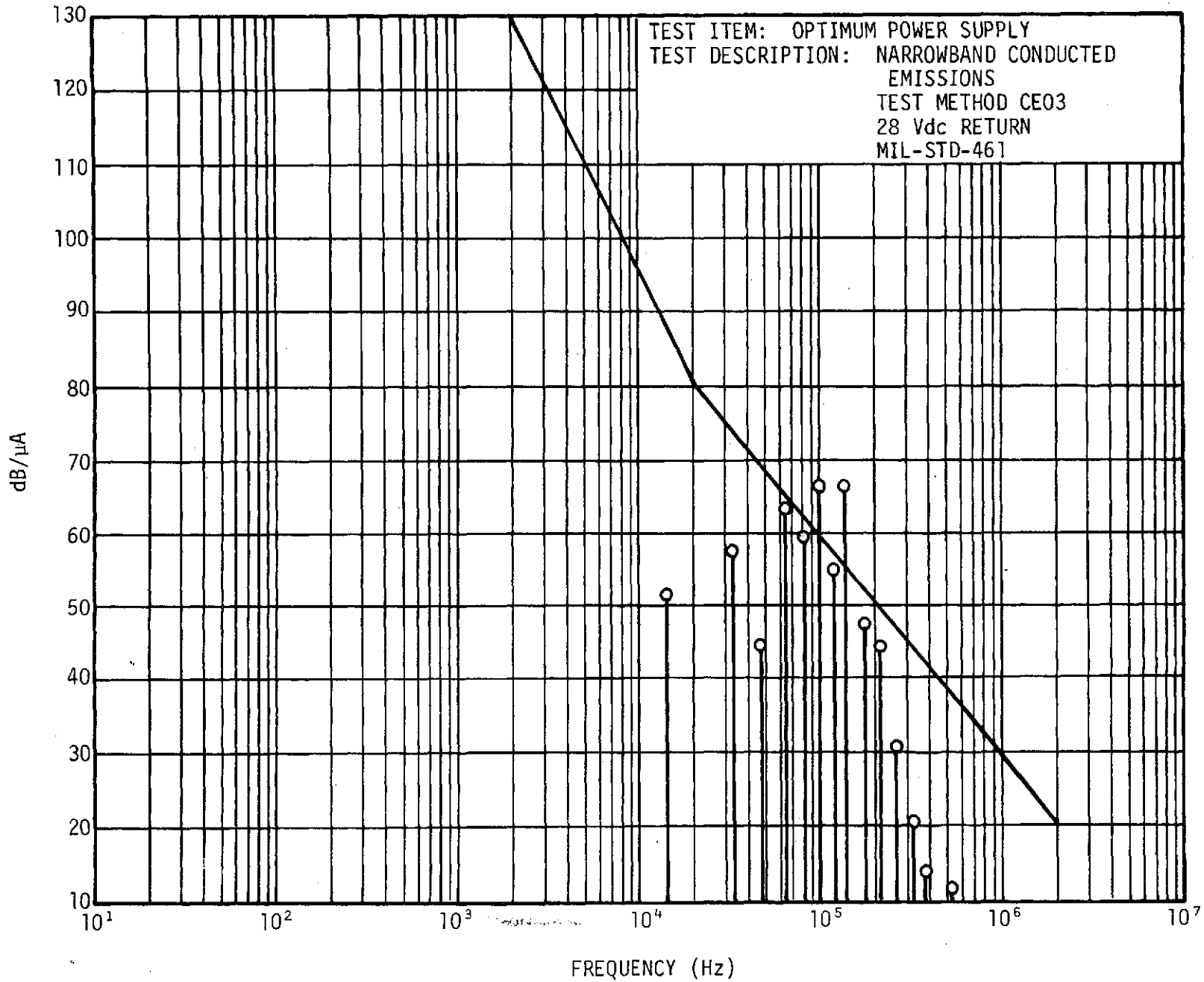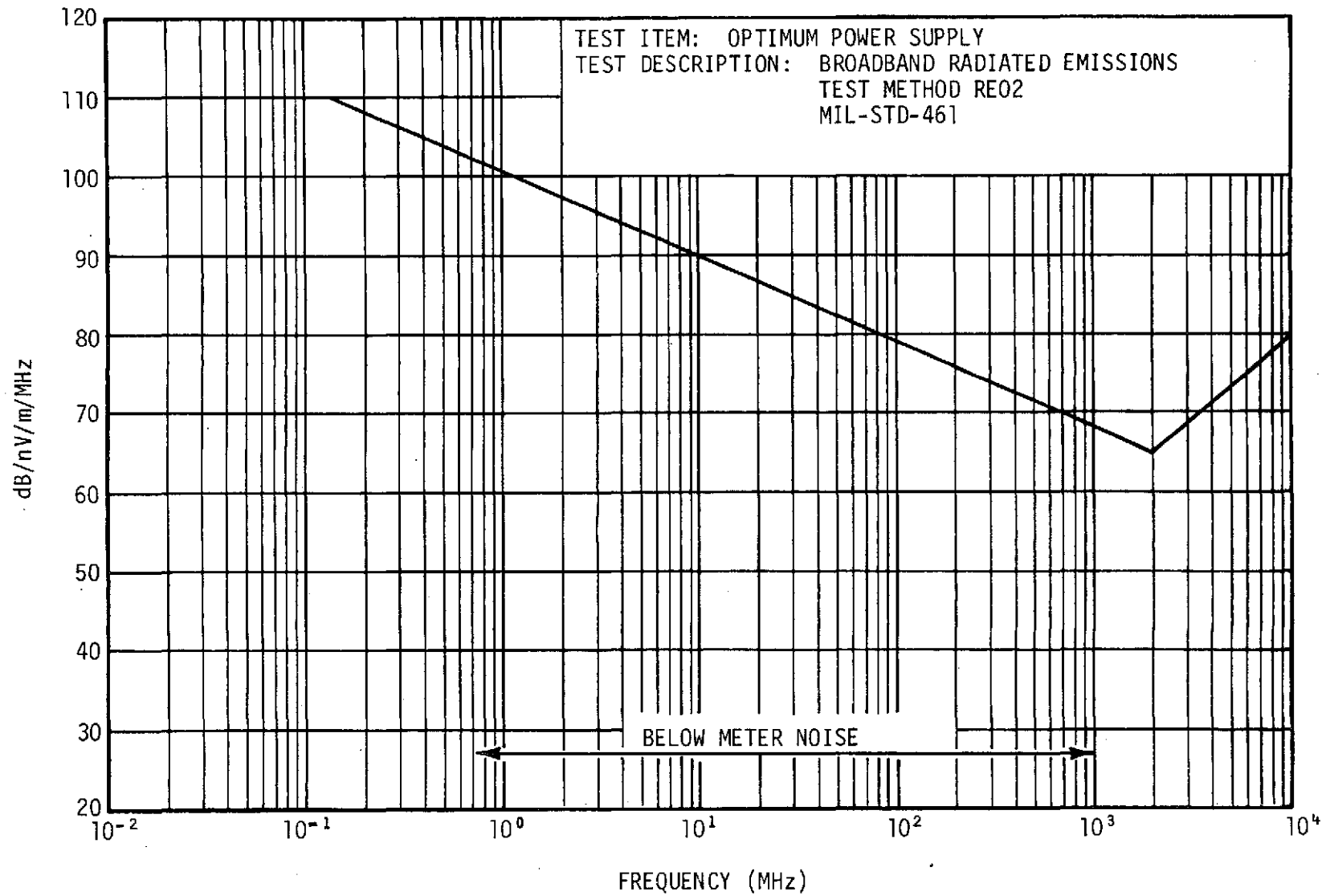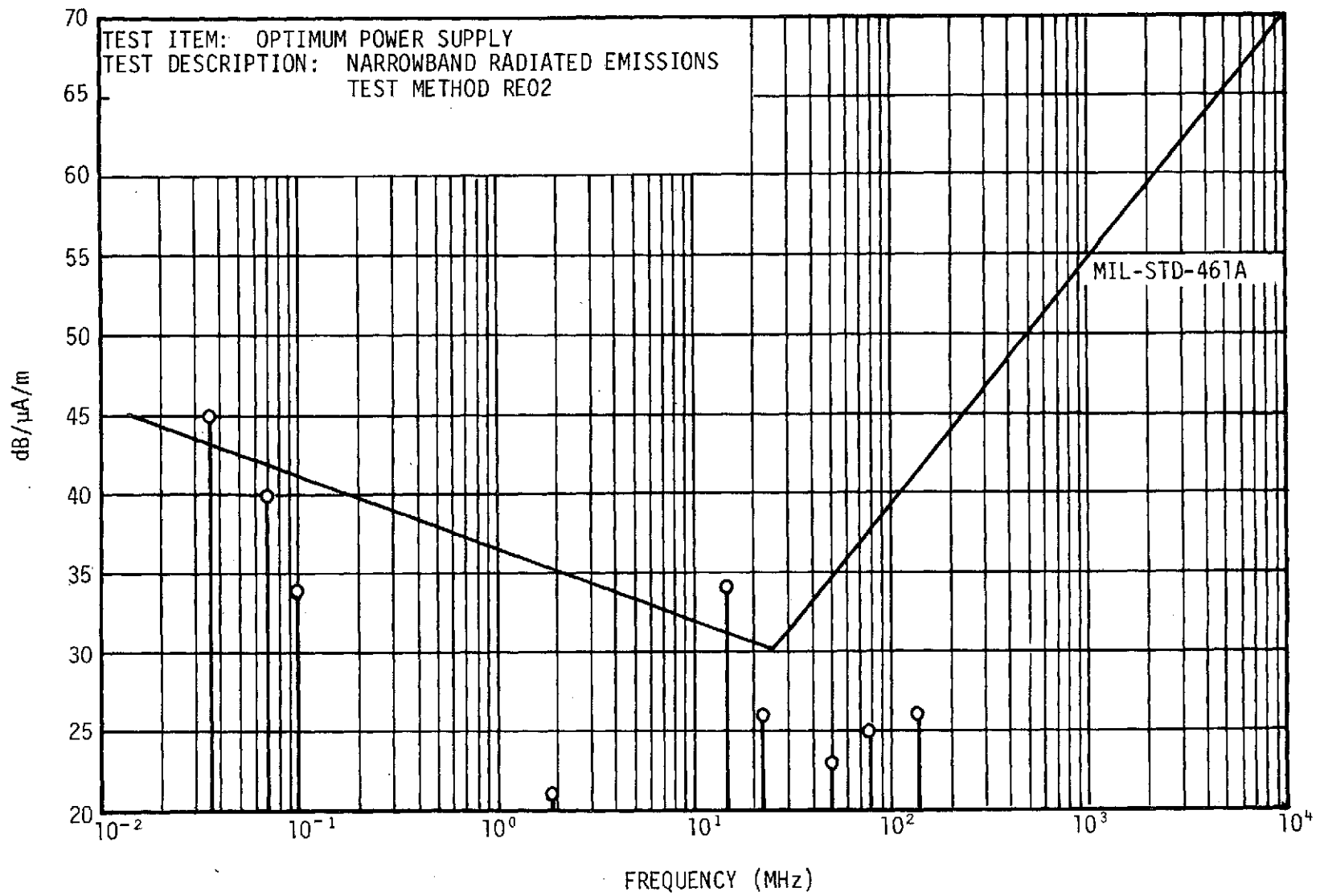
FIGURE H-4

FIGURE H-5

II. LOAD REGULATION

The power supply was tested for line regulation with each supply fully loaded. The supply tested was unloaded, then reloaded to determine the response. The line voltage was 28 volts. The following data was taken:

SUPPLY (V)	FULL LOAD (V)	NO LOAD (V)	% LOAD REGULATION
+28	+28.0042	+28.0042	<0.001
+15	+15.0068	+15.0068	<0.001
+ 5	+ 5.0057	+ 5.00591	0.003
-15	-15.0000	-15.0000	<0.001

III. LINE VOLTAGE REGULATION

The power supply was subjected to a line variation of 24 to 36 volts input and the outputs of the supply were measured. Each supply was fully loaded. The following data was taken:

SUPPLY (V)	+24-V INPUT (V)	+36-V INPUT (V)	% LINE REGULATION
+28	+28.00042	+28.0042	<0.001
+15	+15.0068	+15.0068	<0.001
+ 5	+ 5.00576	+ 5.00576	<0.001
-15	-15.0000	-15.0000	<0.001

IV. TEMPERATURE COEFFICIENT

The power supply was placed in a temperature chamber and allowed to soak for 4 hours at −20°C and +85°C. The supply was turned on to a full load and allowed to stabilize for 5 minutes. The output voltages were then measured. The input power was 28 Vdc. The following data was taken:

SUPPLY (V)	−20°C (V)	+85°C (V)	TEMPERATURE COEFFICIENT (%/°C)
+28	+28.0100	+27.9975	0.000323
+15	+15.0105	+15.0070	0.000349
+ 5	+ 5.00615	+ 5.0056	0.000276
−15	−14.9960	−14.9965	0.000253

V. OUTPUT RIPPLE

The power supply was operated at full load and 28-volt input and the output ripple including noise spikes were measured. The following data was taken:

SUPPLY (V)	OUTPUT RIPPLE (mV pp)	% RIPPLE
+28	180	0.64
+15	140	0.93
+ 5	50	1.0
-15	110	0.73

VI.   STEP LOAD RESPONSE

The power supply was fully loaded and each output was step-loaded from no load to full load. The amplitude and the settling time was measured and recorded. The power input was 28 Vdc. The following data was taken:

SUPPLY (V)	AMPLITUDE (V)	RECOVERY TIME (msec)	% AMPLITUDE
+28	3.0 peak	0.75	10.7
+15	1.75 peak	1.0	11.6
+ 5	0.50 peak	0.75	10.0
-15	1.50 peak	1.0	10.0

VIII. EFFICIENCY TESTS

The power supply was loaded at approximately 0, 25, 50, and 100 percent load on each output voltage. The output voltage and current as well as input voltage and current were measured for line voltages of 24-, 28-, and 36-volt inputs. The following data was taken:

Output Voltages

+28 V = +28.0060 V

+15 V = +15.0090 V

+ 5 V = + 5.0058 V

-15 V = -14.997 V

	INPUT CURRENT (A)			OUTPUT CURRENT (A)				P_{out}
	+24 V	+28 V	+36 V	+28 V	+15 V	+5 V	-15 V	(W)
0% Load	0.27	0.28	0.28	0.00	0.00	0.00	0.00	0.00
25% Load	4.56	4.01	3.33	0.80	1.56	2.49	1.67	84.82
50% Load	10.02	8.67	6.94	2.48	3.35	5.09	3.22	193.50
100% Load	18.72	16.09	12.67	3.60	6.70	9.95	6.70	351.68

EFFICIENCY (all output loaded)

LOAD (%)	+24 V_{in}	+28 V_{in}	+36 V_{in}
25	0.774	0.744	0.708
50	0.805	0.797	0.775
100	0.783	0.780	0.771

Additionally, each output module was plugged into the corridor and the efficiency as a function of input voltage and load was recorded. The static power loss with no modules in place is given below:

V_{in}	STATIC POWER LOSS (NO MODULES) (W)
+24	1.92
+28	2.24
+36	2.88

+28-V REGULATION

The following data was taken on the +28-volt regulation.

	INPUT CURRENT (A)			OUTPUT CURRENT (A)	
LOAD (%)	24 V	28 V	36 V	V_{out} = 28.0042	P_{out} (W)
0	0.09	0.09	0.09	0.00	0.00
25	1.23	1.09	0.86	0.80	22.40
70	3.48	3.02	2.41	2.48	69.45
100	5.29	4.58	3.66	3.60	100.82

EFFICIENCY (+28 V Regulator Only)

LOAD (%)	+24 V_{in}	+28 V_{in}	+36 V_{in}
25	0.758	0.734	0.724
70	0.832	0.821	0.800
100	0.794	0.786	0.772

+5-VOLT REGULATOR

The +5-volt regulator was tested alone and the following data was taken:

	INPUT CURRENT (A)			OUTPUT CURRENT (A)	
LOAD (%)	+24 V_{in}	+28 V_{in}	+36 V_{in}	V_{out} = 5.00576 V	P_{out} (W)
0	0.09	0.09	0.09	0.0	0.0
25	0.73	0.64	0.52	2.502	12.524
50	1.36	1.18	0.95	5.085	25.454
75	1.98	1.70	1.37	7.542	37.753
100	2.63	2.28	1.79	9.927	49.692

EFFICIENCY (+5 V REGULATOR ONLY)

LOAD (%)	+24 V_{in}	+28 V_{in}	+36 V_{in}
25	0.715	0.698	0.669
50	0.780	0.770	0.744
75	0.794	0.793	0.765
100	0.787	0.778	0.771

-15-VOLT REGULATOR

The -15-volt regulator was tested alone and the following data was taken:

	INPUT CURRENT (A)			OUTPUT CURRENT (A)	
LOAD (%)	+24 V_{in}	+28 V_{in}	+36 V_{in}	V_{out} = -14.9970	P_{out} (W)
0	0.11	0.11	0.11	0.0	0.0
25	1.38	1.28	1.02	1.66	24.895
50	2.61	2.28	1.84	3.22	48.290
100	5.34	4.61	3.66	6.70	100.48

EFFICIENCY (-15 V REGULATOR ONLY)

LOAD (%)	+24 V_{in}	+28 V_{in}	+36 V_{in}
25	0.752	0.695	0.678
50	0.771	0.756	0.729
100	0.784	0.778	0.763

VIII. CURRENT LIMIT

The power supply was tested for the start of current limit and the short circuit current. All of the outputs were at full load and the input voltage was +28 volts. The following data was generated:

SUPPLY (V)	START OF CURRENT TIME (A)	SHORT CIRCUIT CURRENT (A)
+28	4.30	5.55
+15	8.20	7.60
+ 5	12.75	15.135
-15	8.55	7.6

IX. INPUT OVERVOLTAGE

The power supply was subjected to an input overvoltage of +50 volts for a period of several minutes. There was no change in performance either during the overvoltage or after.

X. SUMMARY OF TEST DATA

The following is a summary of the salient test data taken on the supply. The data is an average of all four supplies:

- Load Regulation   <0.0015% (0 to full load)

- Line Regulation   <0.001% (24 to 36 V_{in})

- Temperature Coefficient 0.0003%/°C (-20°C to +85°C)

- Ripple   0.835% (full load)

- Stepload   10.5% (amplitude)
                           0.875 msec (settling time)

- Overall Efficiency   78% (full load, 28 V_{in})