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POWER PROCESSOR FOR A 30CM ION THRUSTER

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16. Abstract

A thermal vacuum power processor for the NASA Lewis 30CM Mercury Ion Engine was designed, fabricated and tested to determine compliance with the electrical specification. The power processor breadboard used the silicon controlled rectifier (SCR) Series Resonant Inverter as the basic power stage to process all the power to the ion engine. The power processor included a digital interface unit to process all input commands and internal telemetry signals so that operation would be compatible with a central computer system.

The breadboard was tested in a thermal vacuum environment. Integration tests were performed with a 30CM Mercury Ion Engine and demonstrated operational compatibility and reliable operation without any component failures. Electromagnetic interference data was also recorded on the design to provide information on the interaction with total spacecraft.

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FORWARD

This work is a continuation of effort on the development work reported in NASA CR-120928, "Development of Multikilowatt Ion Thruster Power Processor" and NASA CR-121160 "Power Processor for a 20CM Ion Thruster."

We thank Pierre Thollot, Jack Shank and Robert Frye of NASA Lewis' Power Electronics Branch for their support during the design and testing phase of the thermal vacuum power processor breadboard, and the NASA Lewis' Electric Propulsion Branch for the loan of the 30CM Mercury ion engine and their support during ion engine/power processor integration test.

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1.0 SUMMARY

A thermal vacuum breadboard power processor was designed, developed, fabricated, and tested for use with a 30cm ion thruster. The ion engine was operated with the power processor for over one hundred (100) hours under all operating conditions - start, shutdown, arcing, steady-state at voltage and beam current extremes - with no operational problems.

There was no failure of any kind of the power silicon-controlled rectifier during these tests, thereby demonstrating the ruggedness of the SCR series resonant inverter stage.

The basic power stage is a silicon-controlled rectifier series resonant inverter with the excessive series resonant capacitor energy circulated through the load and returned to the source. Two series resonant inverter power stages were used. One inverter provided power to the screen and accelerator outputs and the other inverter provided power to the ten other outputs. The maximum frequency of operation was 20kHz.

A digital interface unit was included so that a computer could be directly coupled to the power processor to provide automatic computer controlled operation.

All digital logic circuits were implemented with high threshold family of logic elements to obtain high noise immunity during arcing of the ion engine.

The two-loop control system has been incorporated in all critical regulators to maintain high regulation accuracy. It also provides fast dynamic response so that perturbations on the power processor output are minimized during dynamic variations of the power source or during dynamic variations of the ion thruster loading on the power processor.

The following is a summary of the 30cm ion engine power processor breadboard characteristics including digital interface unit:

- Input: 200 to 400Vdc
- Output: 12 outputs per requirements of Appendix A
- Output Power: 3.6kW maximum

o	Commands:	5 on/off plus four analog signals per requirements of Appendix A
o	Telemetry:	16 channels
o	Size:	145cm (57in) x 65cm (26in) x 13.6cm (5.38in)
o	Weight of Components:	19.2 kilograms (42.24 lbs)
o	Efficiency:	84% at full power to 65% at 1/4 power
o	Total Part Count:	3044
o	Total in Line Components for Reliability Analysis:	2041

The breadboard power processor was checked out with a resistive load bank to simulate the range of ion engine static loading and fault characteristics. After room ambient tests were completed, the breadboard was tested in a thermal vacuum environment with the resistive load bank. The following functional tests were conducted:

- Startup of the power processor at 0°F baseplate temperature
- Operation of the power processor until temperature stability was obtained and the thermocouple readings recorded to assure safe operating temperatures for all components.
- Shutdown and startup of the power processor at high baseplate temperature.

The effort on the thermal vacuum breadboard power processor program was concluded with the aforementioned highly successful, over one hundred (100) hours, integration test with the 30cm ion thruster at TRW Systems.

2.0 INTRODUCTION

During the past few years, NASA, TRW and other government contractors have performed studies on solar-powered electric spacecraft. The results of these studies indicate that the development of a lightweight SCR series resonant power processor could greatly enhance spacecraft performance and reliability. Thus, the NASA Lewis "Electric Propulsion Power Processor" program is recognized as an important link in the development of a truly flightworthy, electrically-propelled spacecraft.

High power silicon-controlled rectifiers (SCR's) or thyristors have been used in high voltage and high power equipment for industrial applications for many years. The design objectives in industry were primarily low cost and low maintenance whereas the design requirements for space equipment are low weight and high efficiency. Power processor inefficiency results in spacecraft weight penalties due to increased power source capacity and heat rejection capability.

Future high power spacecraft will be using high voltage distribution to minimize the cable weight and losses and will have high power loads such as electric propulsion, direct broadcast communications and other high power loads or experiments.

The "Electric Propulsion Power Processor" program's objective was to design, construct and test a power processor breadboard designed to operate in a thermal vacuum environment. The SCR series resonant inverter was used as the basic power stage for inverting the input power from a solar array, and an analog signal to discrete time interval converter (ASDTIC) was used as the low level amplifier and control stage for regulated current and voltage outputs. These basic circuits, which were initially developed at NASA ERC, were applied by TRW to the design of a power processing system capable of meeting the load requirements of a 30CM hollow cathode mercury ion engine.

3.0 30CM ION ENGINE POWER PROCESSOR THERMAL-VACUUM BREADBOARD

The 30CM Ion Engine Power Processor Thermal-Vacuum Breadboard was designed to operate the 30CM hollow cathode mercury ion engine in a vacuum environment. The 30CM ion engine power processor design is based on work performed on the 20CM power processor breadboard design, fabrication, test and integration with JPL's 20CM ion engine and system studies in support of solar electric propulsion spacecraft. The detail requirement specification is included in Appendix A, 30CM Ion Thruster Power Processor Specification.

A detailed electrical design was performed and a complete power processor thermal-vacuum breadboard was fabricated. Testing was performed with a simulated resistive load at room ambient and in a vacuum environment to demonstrate compliance with the power processor specification over the load range and overload conditions. The power processor was integration tested with a 30CM ion engine to demonstrate compatibility with engine operation.

An analysis of the power processor design is presented in order to indicate where penalties exist and where improvements can be made.

A summary of the test data is presented to verify power processor operation.

3.1 Power Processor System Block Diagram

A block diagram of the ion thruster power processor is shown in Figure 3.1. The power processor can be divided into five basic groups.

- The power circuit
- The output regulator circuitry
- The command and protection circuit
- The telemetry circuit
- The digital interface unit

The mechanization of the system is influenced by the following items:

- Engine Control functions during startup, during normal operation and during overload
- Use of the SCR series resonant inverter power stage
- Maximize efficiency
- Maintaining all control electronics at ground potential
- System grounding philosophy

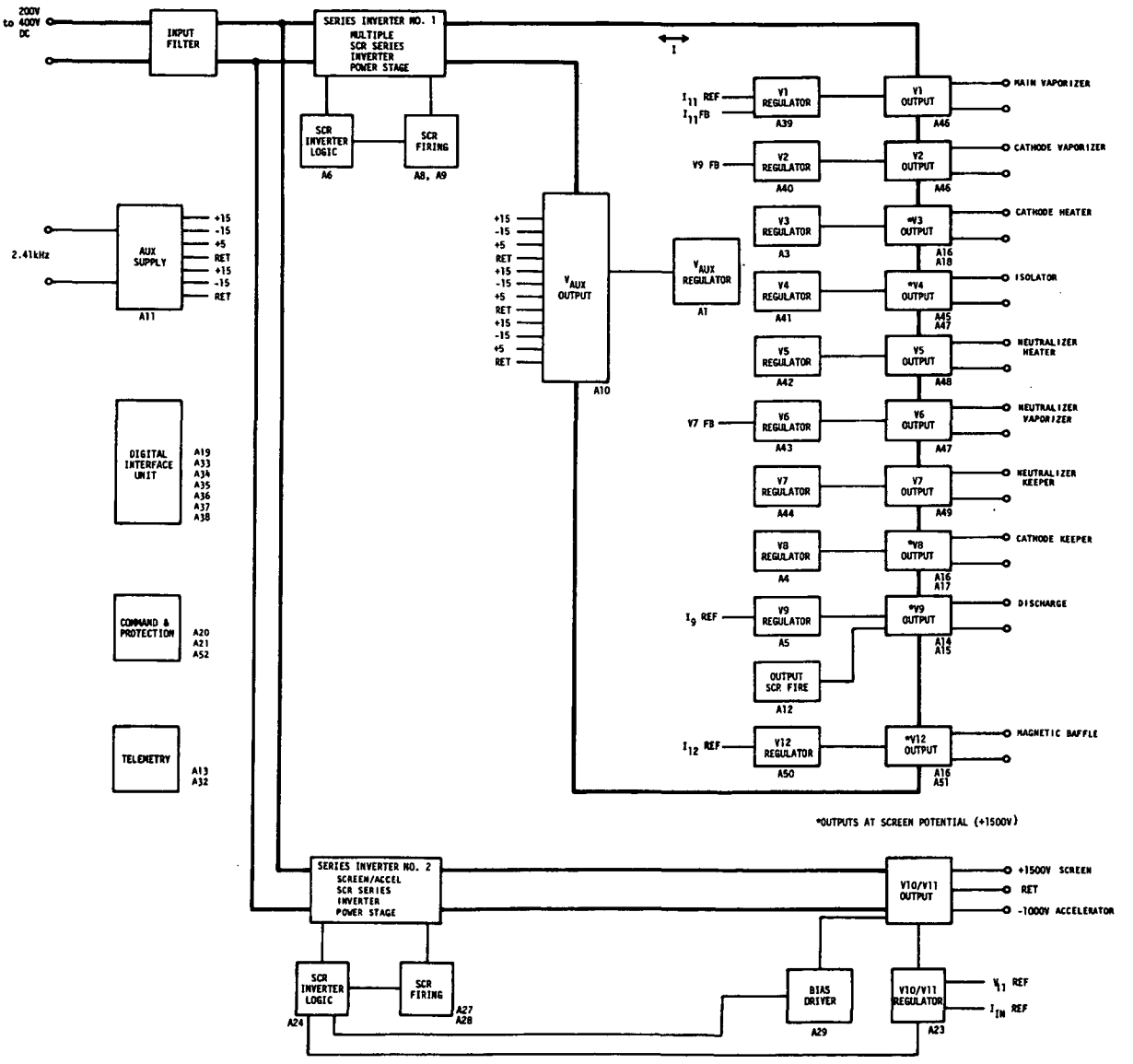


FIGURE 3.1. 30CM ION ENGINE POWER PROCESSOR BLOCK DIAGRAM

The power processor must include the following in the design of the power stage: (1) methods of isolating the input power bus from effects of output voltage and/or power variations; (2) methods of preventing output fault conditions being directly fed back to the power source thereby avoiding collapse of the power source; and, (3) methods of controlling the operational conditons of the semiconductor components to avoid their overstress during startup, input voltage variations, and output fault conditions. The basic design of this power processor uses a L-C series resonant inverter which acts as a current limiting impedance between the power source and ion engine load. The L-C tank provides the instantaneous current limiting protection and the control electronics provides the long term protection or current limiting by adjusting the duty cycle modulation of the inverter stage.

The L-C series resonant inverter has another basic advantage in that the semiconductor current is a sinewave which reduces the power semiconductor switching losses and which eliminates the higher order harmonics. These higher order harmonics contribute to electromagnetic interference both in the power processor and in other equipment on the spacecraft.

The 30CM power processor is designed with two series resonant inverter power stages using a total of eight high power semiconductor switching elements to process all the power to the ion engine. One inverter supplies 2.62KW of output power for the ion engine screen and accelerator outputs. The second inverter is designed for about 1KW to supply the power for the remaining ion engine outputs and for the internal power for control electronics and the digital interface unit.

The two stage L-C input filter acts as a two way filter: (1) it maintains the current reflected from the power processor back into the source at a level required to meet the EMI requirements, and, (2) it minimizes the effects on the power processor of any perturbations caused by other equipment being fed from the primary power bus.

The ASDTIC has been incorporated in all critical regulators in order to maintain close static regulation around the set points, and thus the calculated propulsion error shall be minimized despite power source and load variations. The ASDTIC also provides fast dynamic performance so that perturbations on the power processor output are minimized during dynamic variations of the power source or during dynamic variations of the ion thruster loading on the power processor. This fast dynamic response reduces power processor output voltage overshoots and overstress on power circuit components. This fast dynamic response reduces the current transient reflected to the power source during load transients thereby protecting the high impedance primary power bus from collapse or wide voltage variations with the coupling effect on other equipment.

Series Inverter No. 1 is the multiple output inverter. This inverter which runs at a constant frequency provides a constant current source to its series connected loads. This inverter supplies the following seriesed transformers whose secondaries can supply current directly to the outputs or can be shorted resulting in zero power being delivered to the outputs.

- PS1 - Main Vaporizer Supply
- PS2 - Cathode Vaporizer Supply
- PS3 - Cathode Heater Supply
- PS4 - Isolator Supply
- PS5 - Neutralizer Heater Supply
- PS6 - Neutralizer Vaporizer Supply
- PS7 - Neutralizer Keeper Supply
- PS8 - Cathode Keeper Supply
- PS9 - Discharge Supply
- PS12- Magnetic Baffle Supply
- Internal Auxiliary Supply

The total power rating of the multiple inverter is about 1KW.

SCR series inverter No. 2 supplies the PS10 and PS11 outputs (accelerator and screen outputs) and has a power rating of 2.62KW. Its duty cycle of modulation varies proportional to the output power.

The command and protection circuitry of the power processing units provides all the necessary commands to startup and shutdown the processing unit. It also provides automatic recycling of the power processor in the event of any arcs that occur within the thruster or between the thruster and the facility ground.

All telemetry outputs of the power processor are analog voltage signals having an amplitude from 0 to 5VDC. The telemetry signals are isolated from all other ground systems in the power processing unit.

The digital interface unit is designed to transfer 16 bit digital words between a computer and the power processor. The input and output data from digitized command and telemetry units will be in 16-bit parallel format where the first 6 bits will be the address or identification and the last 10 bits will be data bits.

Detail block diagrams of each section are included in Appendix B.

3.2 Electrical Design

A brief summary of the electrical design is presented for the two inverters in Figure 3.1.

3.2.1 The Accelerator and Screen Supplies

In the following sections, the power stage design, the inverter control logic and the regulator control system are discussed.

3.2.1.1 Power Stage

The schematic of the V10, V11 series inverter power stage is shown in Figure 3.2. The inverter consists of the main SCR's (SCR1 and SCR2), auxiliary SCR's (SCR3 and SCR4), the series resonant inductors (L1, L2, L3, L4, L5), the series resonant capacitors (C1, C2), the suppression networks for the main and auxiliary SCR's, and the output circuitry.

Circuit operation is as follows:

- With C1 charged to V > 450V and C2 charged to V < 0 auxiliary SCR (SCR4) is turned on to circulate energy in C2 into transformer T and energy in C1 back to the source.
- When the voltage on C1 reaches 450V, SCR1 is turned on causing an oscillatory current to flow through the series combination of L1, L5, T, C1 and C2.
- As the current passes through zero, SCR1 is turned off and C2 is charged to a voltage higher than the supply voltage.
- Auxiliary SCR (SCR3) is next turned on to circulate energy in C1 into transformer T and energy in C2 back to the source.
- When the voltage on C2 reaches 450V, SCR2 is turned on causing current to flow through L2, L5, T, C1 and C2. The turning off of SCR2 completes one full cycle.

The current flowing through transformer T when the SCR's are conducting develops a voltage which is rectified, filtered and delivered to the load. Regulation is achieved by sensing the output voltage and then controlling the repetition rate of the SCR's.

3.2.1.2 SCR Series Inverter Control Logic

The SCR series inverter control logic has the following requirements:

- Limiting of the series capacitor voltage
- Detection of the end of a power half-cycle
- Starting procedure
- Regulation requirement
- Sequencing of SCR's for different half-cycles.

The SCR series inverter control logic block diagram is shown in Figure 3.3. A capacitor voltage sensor continuously monitors the voltages

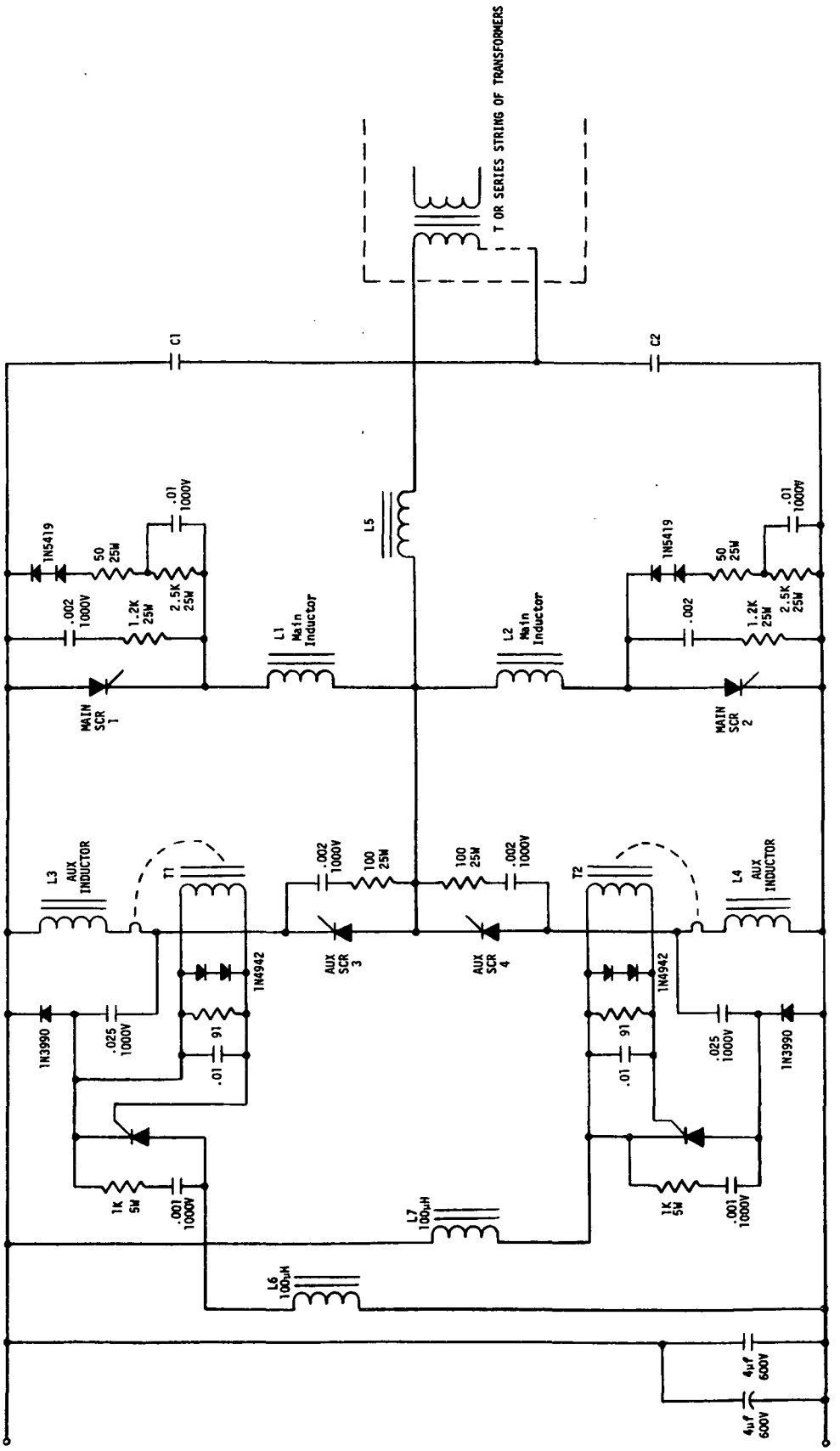


FIGURE 3.2. SCR SERIES INVERTER POWER STAGE SCHEMATIC

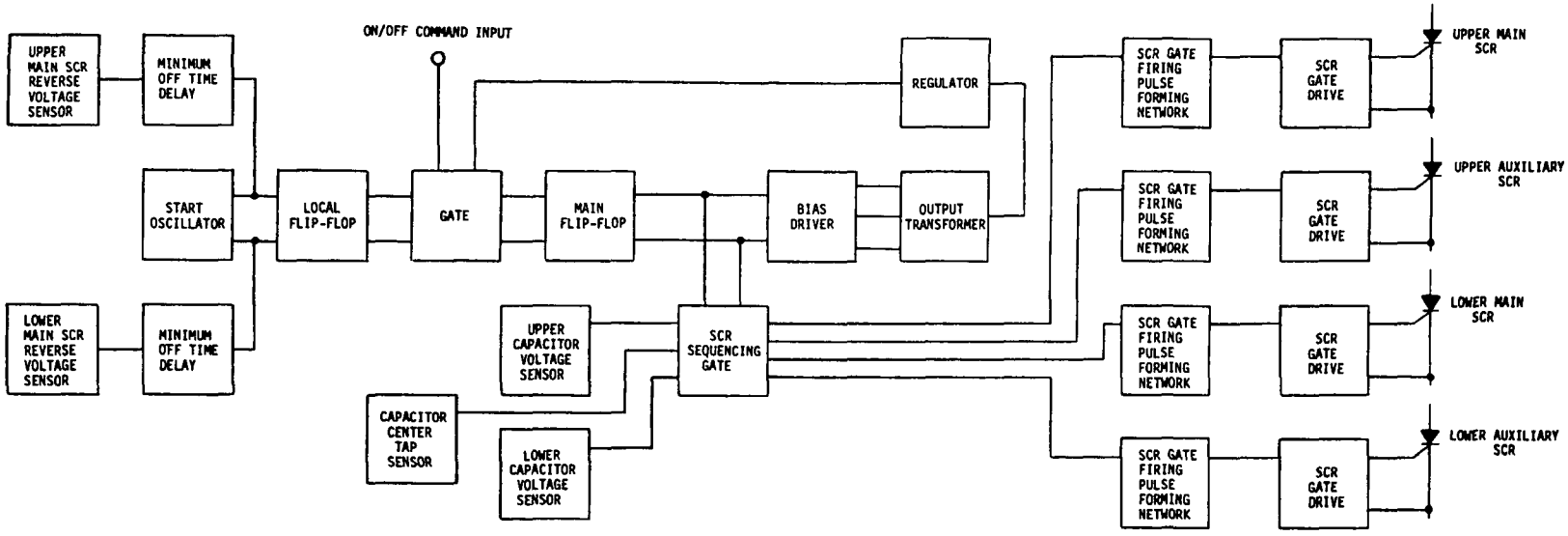


FIGURE 3.3. SCR SERIES INVERTER CONTROL BLOCK DIAGRAM

on the series resonant inverter capacitors and programs the firing of the main line power SCR's in such a manner that the voltage rating of the components in the circuit are never exceeded.

The next protection function is to determine when the current in the main power SCR has gone to zero so that the next power half-cycle can be initiated. This function is mechanized by sensing that a reverse voltage condition has existed on the power SCR for at least the minimum off time to guarantee that the power SCR is off.

Now that the normal running protection functions have been identified, it is necessary to provide the correct starting procedure. When the system is initially activated, reverse voltage condition does not exist on either of the two main line power SCR's. To start the series resonant inverter, a low frequency oscillator becomes active and causes the control logic to switch and current to flow in the power SCR. Once the system is running normally, the low frequency oscillator is disabled.

The output regulator control signal determines the repetition rate of the SCR's by inhibiting the SCR firing signals.

Figure 3.4 shows the detail schematic of the SCR series inverter control logic. High threshold logic digital circuits are used because of their high noise immunity (about 6V) and therefore are immune to high EMI noise generated by the switching noise of high current circuits. U1 and U9 are the voltage comparators which sense reverse voltage on the main SCR's. U2 is a pulse stretcher which provides the minimum off time before another half-cycle can commence. U4 is the start oscillator, U5 is the local bistable, U6 is a Nand gate which couples the regulator signal into the control logic, U7 is the main bistable which commands the SCR firing, U8 is a buffer stage to drive the bias driver circuit. U12 is an optical isolator to isolate the ON/OFF command signal to the inverter. U13 and U14 provide the ON/OFF command interface. U16 and U17 are the voltage comparators which sense the capacitor voltages. U18 and U19 are Nand gates which determine which SCR is to be fired. U20, U21, U22, U23, U24, U26, and U27 form the SCR gate firing pulse forming network.

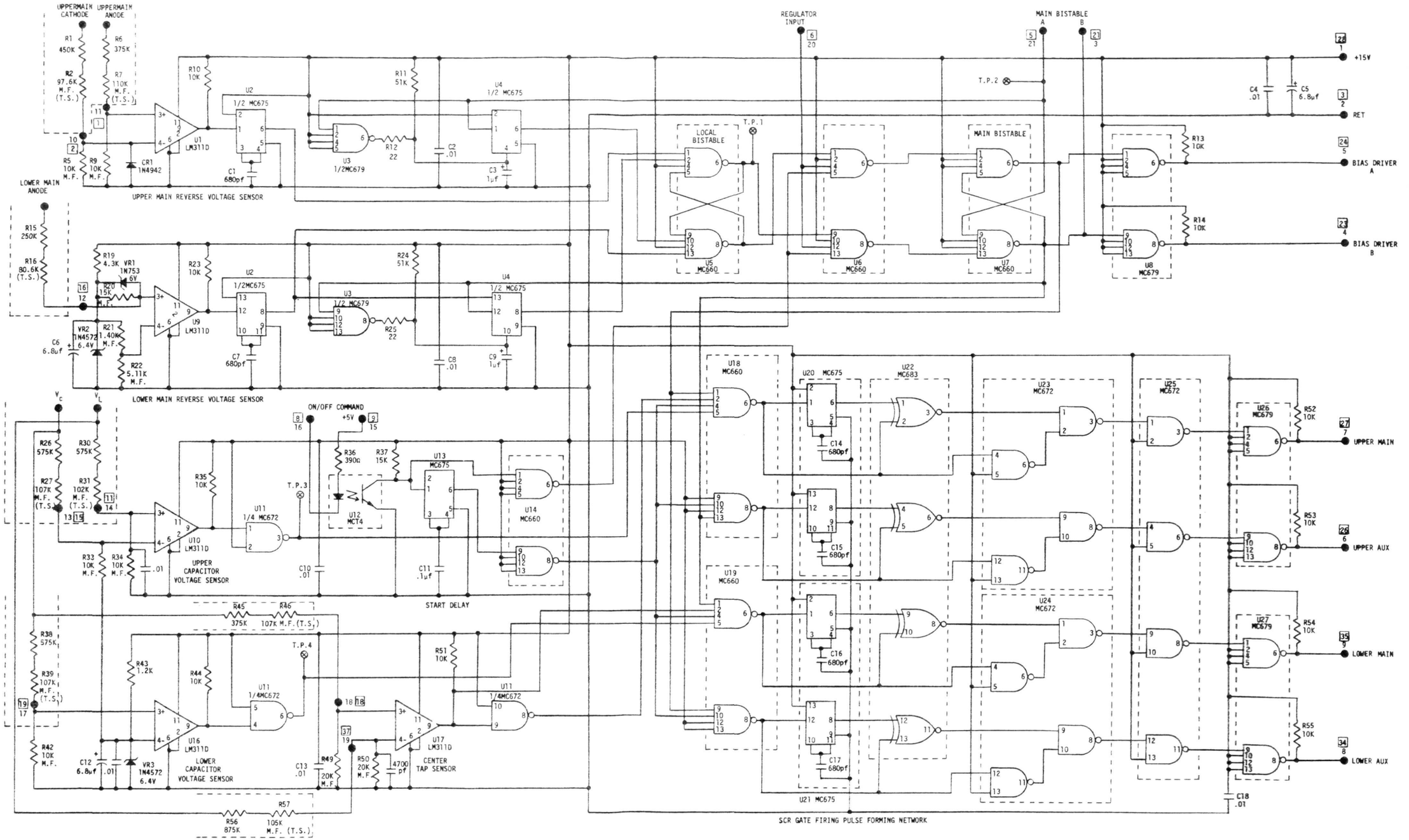


FIGURE 3.4. SCR SERIES INVERTER CONTROL LOGIC SCHEMATIC

The SCR firing circuit is shown in Figure 3.5. The SCR firing circuit takes the low level signal from the control logic and converts it into a high level current pulse to trigger the SCR. The current pulse is coupled through a pulse transformer to isolate the control circuitry from the SCR which is elevated at a few hundred volts. The series connected diodes across the secondary of the transformer provides reverse bias to the gate during the transformer flyback period. This reverse bias prevents noise from firing the SCR.

3.2.1.3 V10, V11 Regulator and Output Circuitry

The block diagram for the V10 and V11 output circuitry is shown in Figure 3.6. Both high voltage outputs are combined into a single power stage in order to reduce overall part count. The current flowing through transformer T1 when the SCR's are conducting develops a voltage which is rectified, filtered and delivered to the load. Regulation is achieved by sensing the V11 output and then controlling the repetition rate of the SCR's. Output limiting resistors RL1 and RL2 control the peak current that can flow from the output filter capacitors C1, C2 and C3. The limiting resistors not only limit the peak output current, but they also control the transient voltage that can appear on the cabling to the engine and the transient voltage between the output ground and engine ground.

The supply has two regulating loops in addition to a series regulator for the accelerator output.

- o V11 output regulation by means of operational amplifier U1
- o I10 overload control by means of operational amplifier U2

The voltage regulating loop incorporates the ASDTIC control system to maintain output regulation accuracy and regulator stability. The DC loop senses the V11 output voltage and the AC loop senses the stored energy in the output capacitor C1 by means of a current transformer. The I10 overload control comes into action during shorts on the V10 output and protects the N3 winding from damage since it is designed to pass only 200mA instead of 2.2A which is the total capacity of the series resonant inverter. The output signals from the operational amplifiers control the

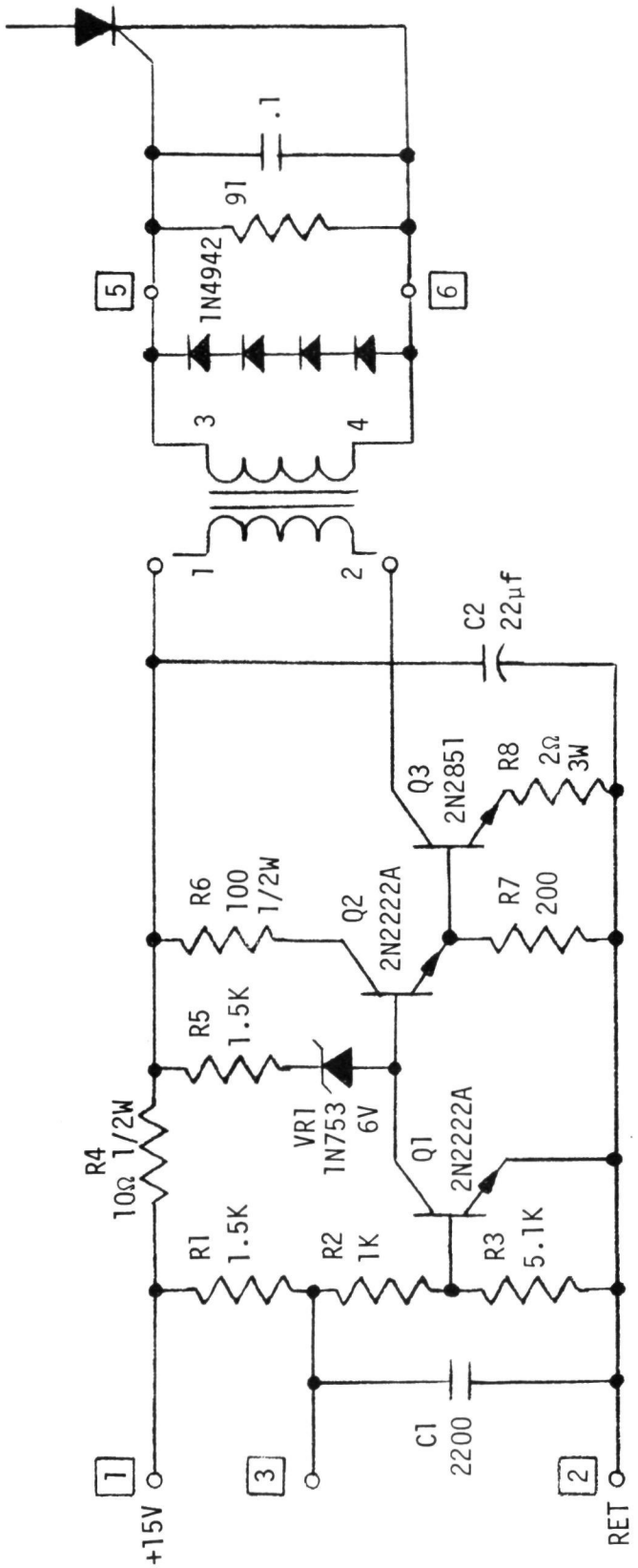


FIGURE 3.5. SCR FIRING CIRCUIT SCHEMATIC

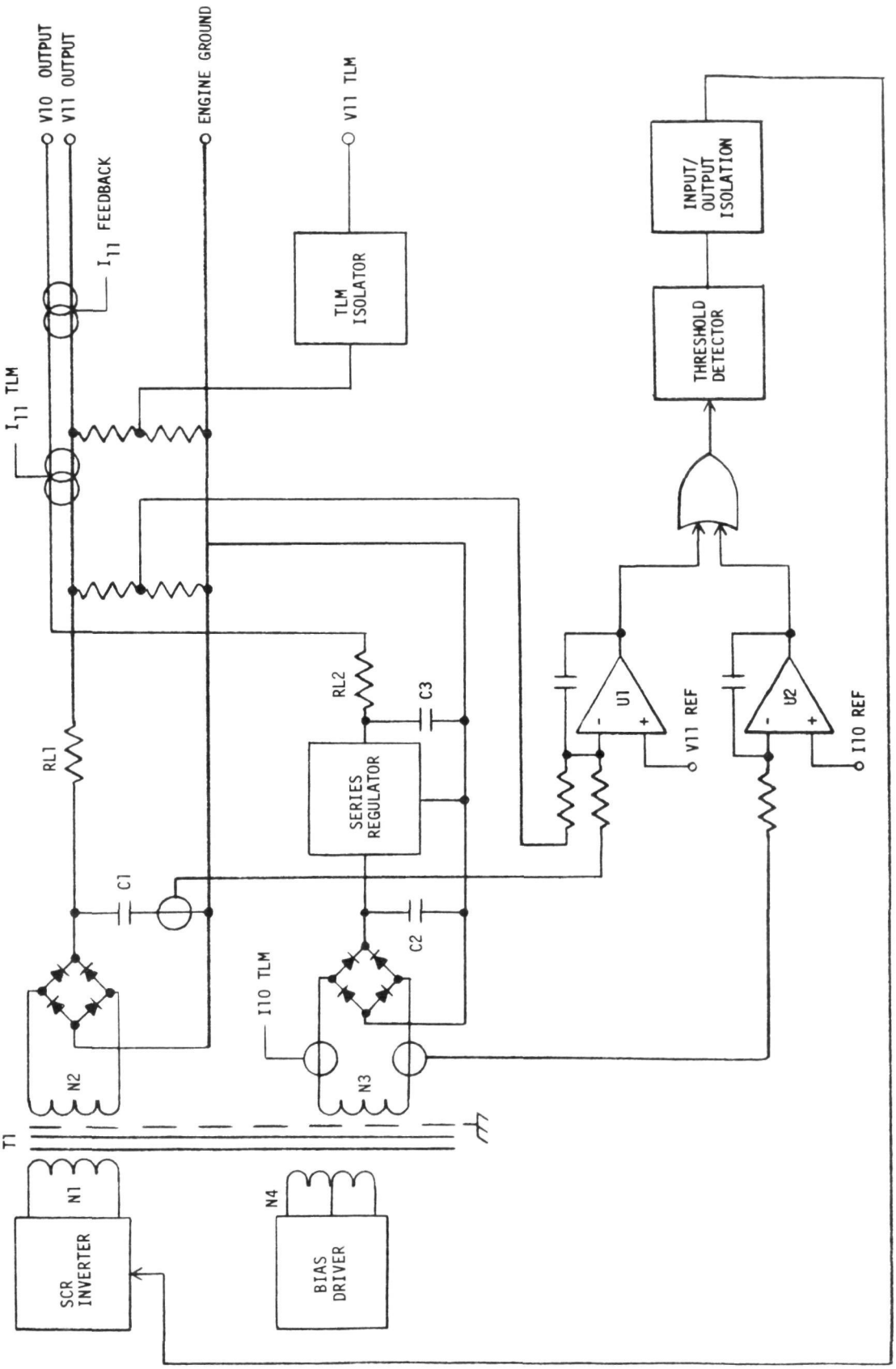


FIGURE 3.6. V10, V11, ACCELERATOR AND SCREEN SUPPLY BLOCK DIAGRAM

threshold detector, the input/output ground isolation circuit, and the control logic for the SCR series inverter. The input/output ground isolation separates the output ground return from the input power ground return for the SCR series inverter control logic.

Since the output voltage of V11 is variable from 1100VDC to 1500VDC, a series regulator was incorporated into the -1000VDC, V_{10}, supply. The series regulator is short circuit protected by the fact that it is driven from a current limited source.

Schematics of the V10/V11 regulator output stage are shown in Figure 3.7 and 3.8.

The circuits for the bias driver and the V11 telemetry isolator are shown in Figure 3.9, and 3.10 respectively. The bias driver is used to hold the transformer core flux at either end of its excursion during the time when no power current is flowing. This provides maximum flux capability for the next half-cycle and insures that the core will not saturate. If the bias driver was not used, the unbalance in alternate half-cycles would tend to drive the flux toward one end and eventually saturate the core. The circuit consists of a constant current source and two transistor switches activated by commands from the inverter control logic to drive current into the transformer in the proper direction.

The V11 telemetry isolator is used to isolate the V11 telemetry ground from the output ground. The V11 output is sensed and then converted into a current signal in the operational amplifier which is then fed to a magnetic amplifier. The output of the magnetic amplifier is rectified and the current is converted back to a voltage across resistor Ro. The magnetic amplifier provides the ground isolation.

3.2.2 The Multiple Output Inverter

The multiple output inverter uses the same series resonant power stage as the screen and accelerator inverter. The output stage shown in dashed lines in Figure 3.2 is replaced by the output stage shown in Figure 3.11.

The sinusoidal current I flowing through the series connected output transformer string shown in Figure 3.11 is a constant frequency, constant amplitude current. The turns ratio of the series connected transformers

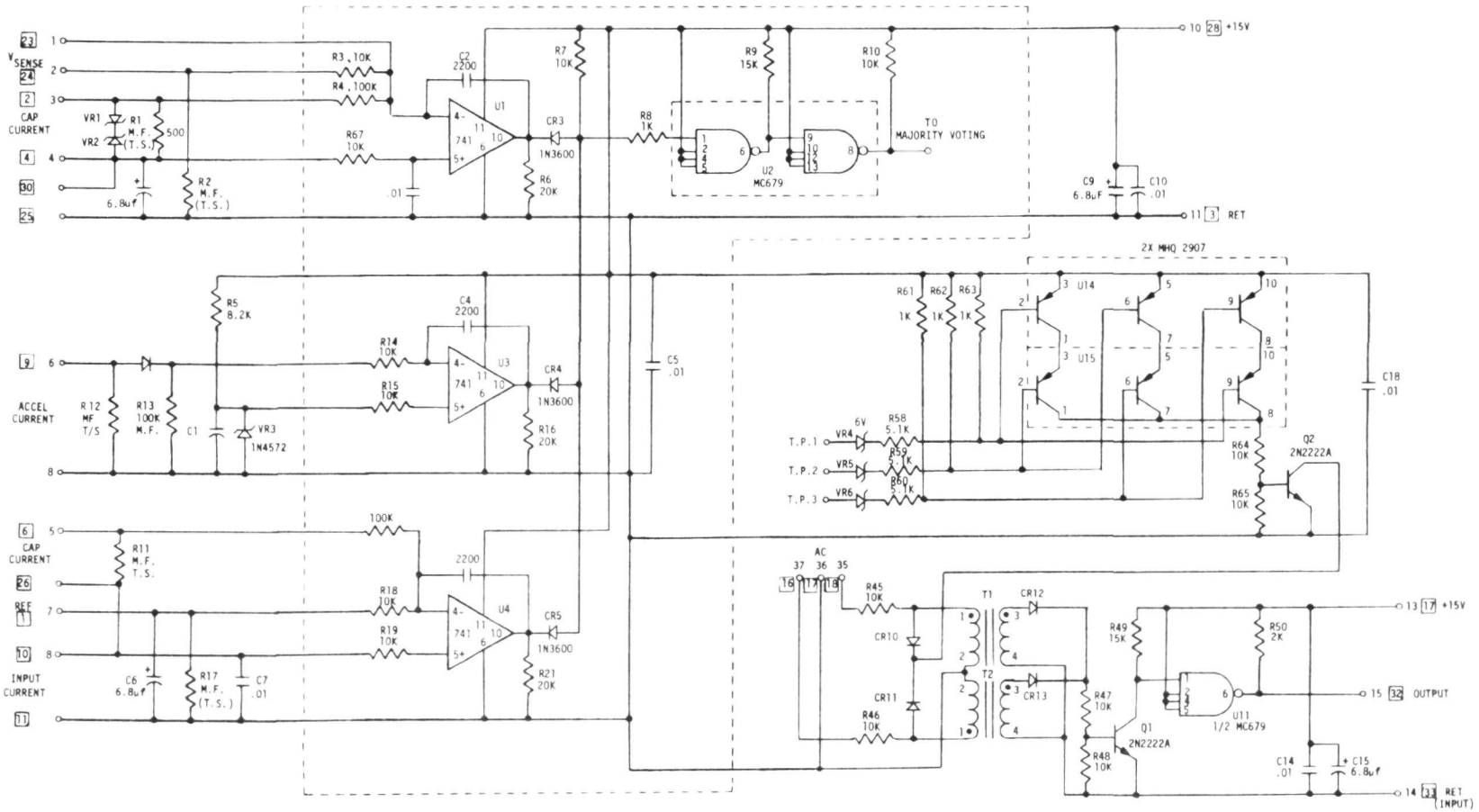


FIGURE 3.7. V10/V11 BEAM REGULATOR SCHEMATIC

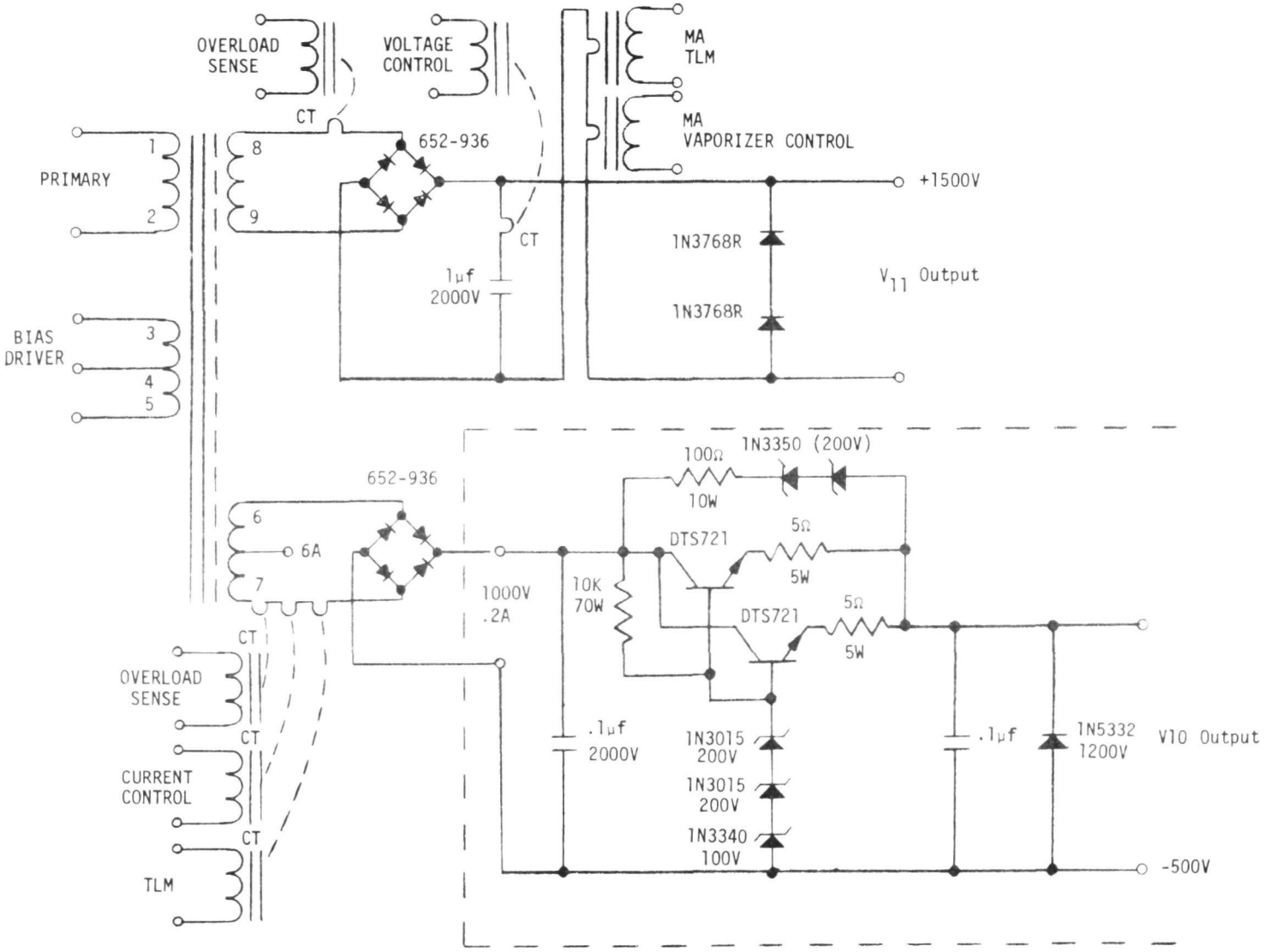


FIGURE 3.8. V10/V11 BEAM OUTPUT CIRCUIT SCHEMATIC

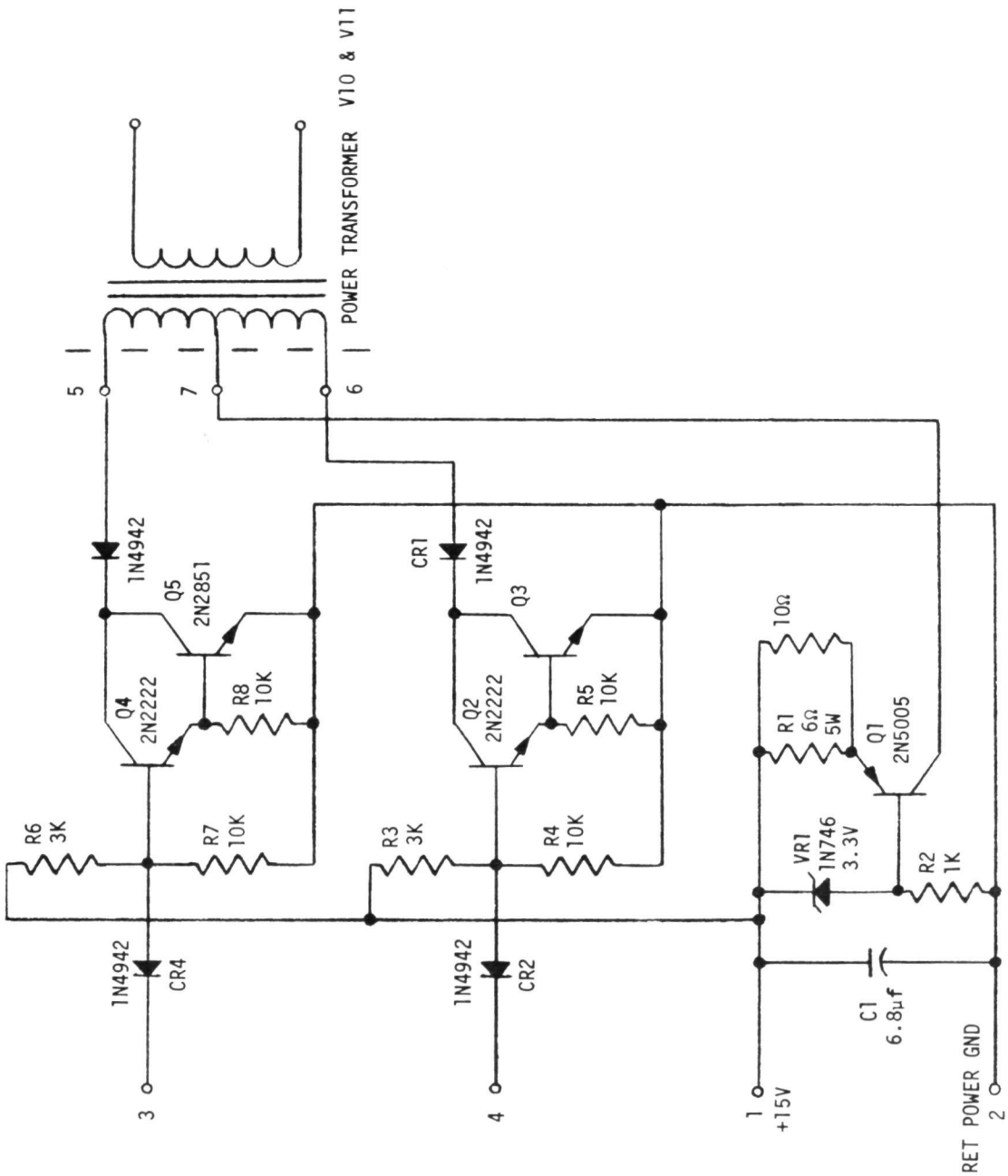


FIGURE 3.9. BIAS DRIVER CIRCUIT

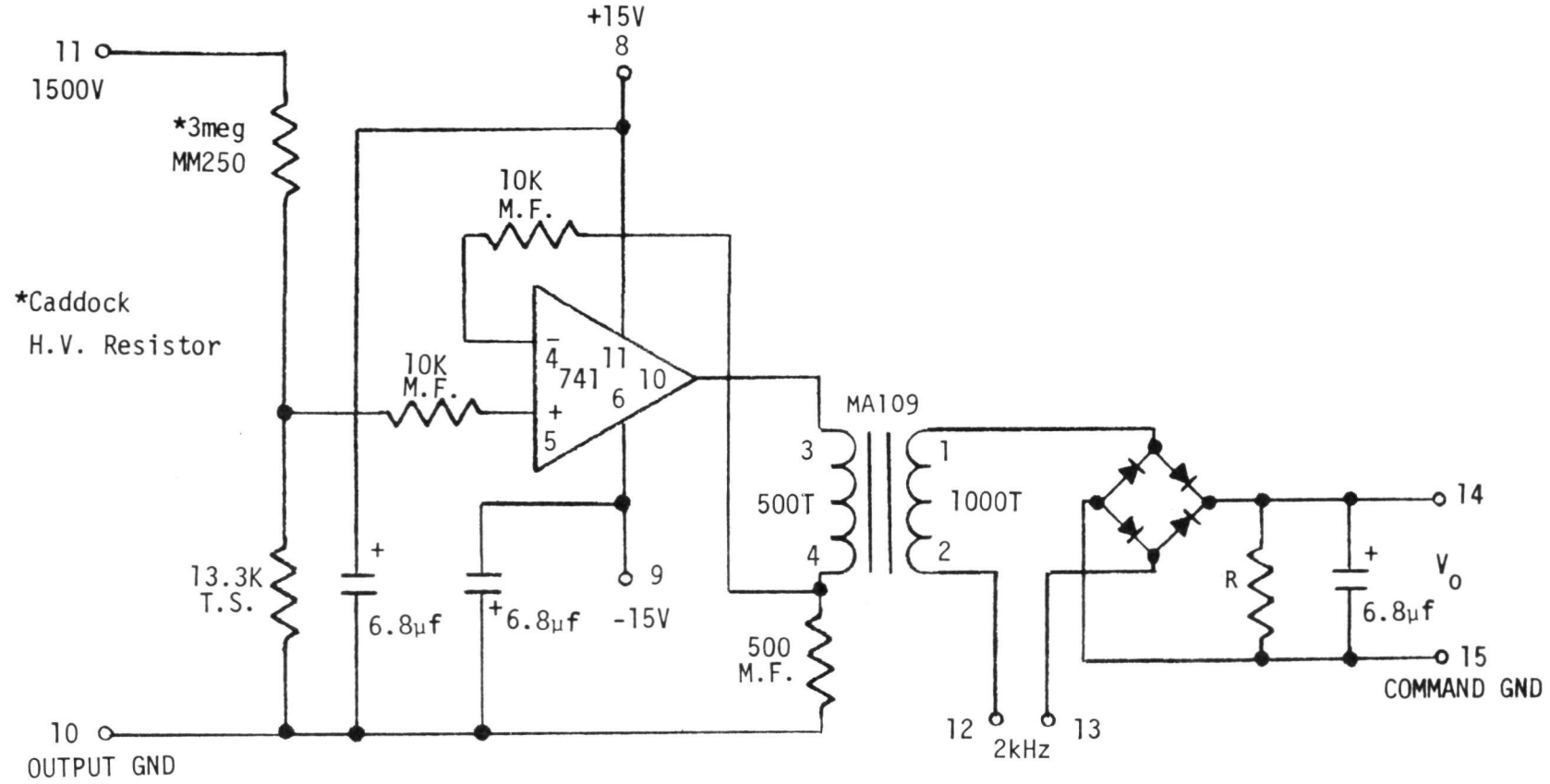


FIGURE 3.10. V11 TLM ISOLATOR SCHEMATIC

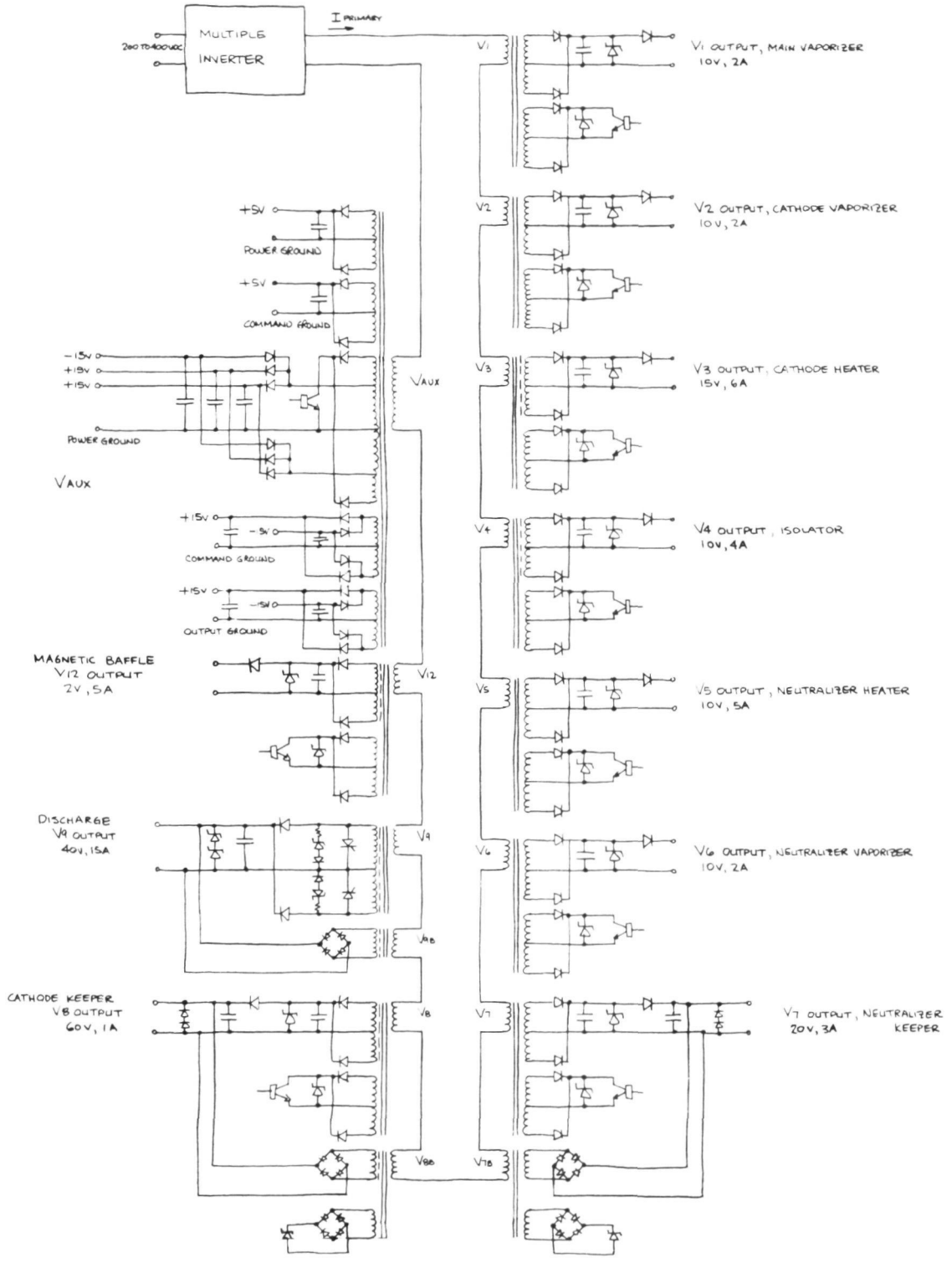


FIGURE 3.11. MULTIPLE OUTPUT POWER STAGES

determine the power sharing of the series string. Regulation of each output is achieved by phase firing of the shunt transistor which shunts the transformer secondary current thus regulating the output.

3.2.2.1 Multiple Inverter Output Regulator and Output Stage

A block diagram of the Main Vaporizer Supply (V1) is shown in Figure 3.12 and it shall be discussed as a typical multiple inverter output. Detail block diagrams of all the multiple inverter outputs are presented in Appendix B, Section 7.0.

Constant frequency current of 20kHz from the multiple output inverter excites the primary of the current transformer T1. The primary current in N1 is allowed to flow in winding N2 to the output filter capacitor Co. To control the output current and voltage amplitudes, shorting transistor Q is turned on thereby placing a short across winding N3 with the result that all secondary current transfers from winding N2 to winding N3 and zero power is transferred through winding N2. The only losses are those to satisfy magnetic and shorting transistor losses.

There are three regulating loops:

- o V1 voltage limiting by means of T2 and operational amplifier U1.
- o I1 current limiting by means of operational amplifier U2.
- o Beam current control by means of operational amplifier U3.

The first two loops are for maximum voltage and current limiting. The current loop has three externally selectable reference levels for varying the current limit points. The third loop is unique to the three vaporizer supplies (Main, Cathode, and Neutralizer), and in the Main Vaporizer controls the ion engine beam current flow by varying the power applied to the vaporizer. The current regulating loops utilize the ASDTIC principle to perform the system regulation. The ramp function is added to the output of the operational amplifier to obtain regulator stability when operating in a constant frequency system.

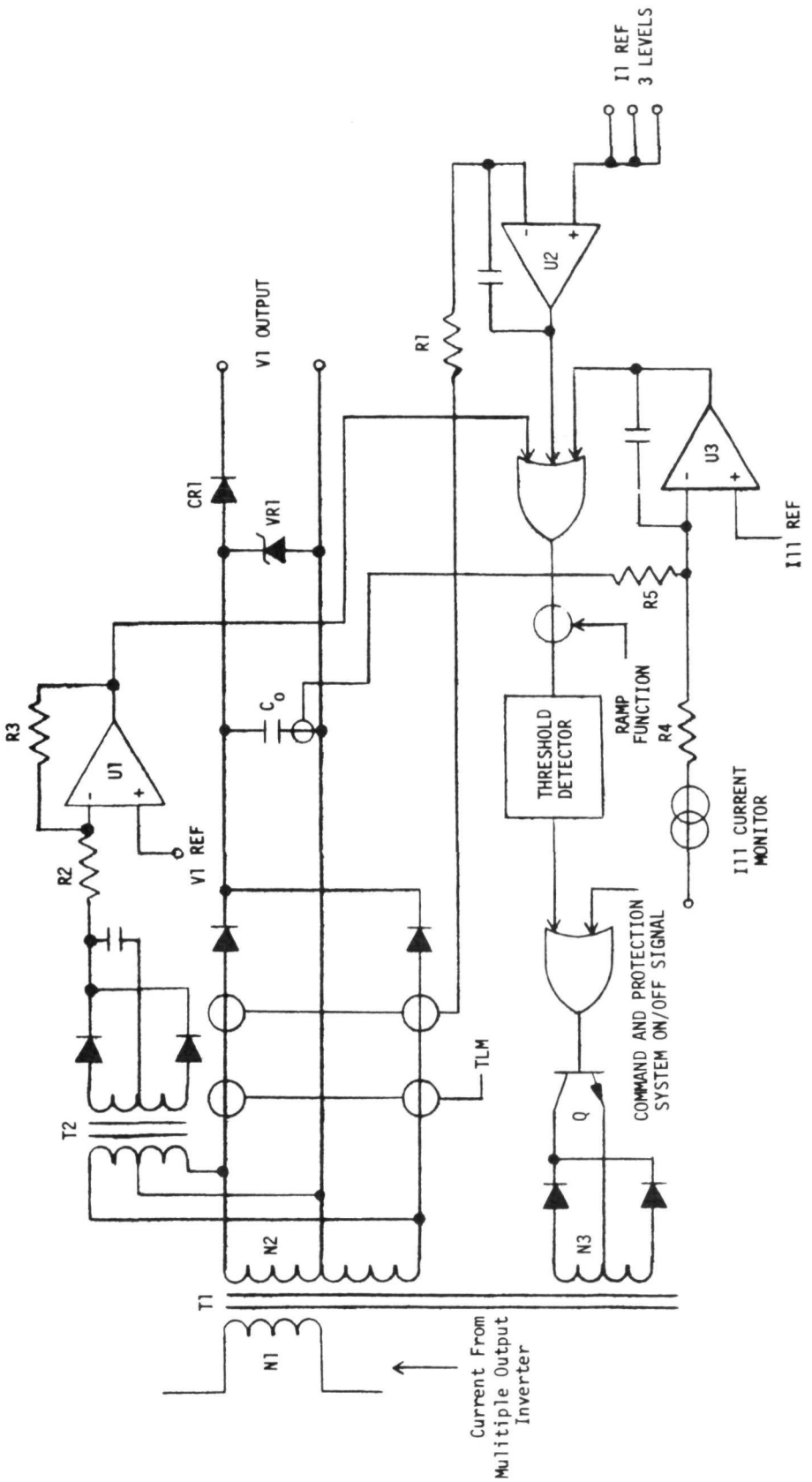


FIGURE 3.12. V1, MAIN VAPORIZER SUPPLY BLOCK DIAGRAM

To limit the output at no load operation a power zener diode VR1 conducts and clamps the maximum output voltage. Because the V1 otuput is referenced to ion engine ground, the 1.5KV output can arc over to the V1 output and cause excessive voltage. To protect the output power components, blocking diode CR1 is inserted in series with the output line.

Schematics of the V1 regulator and V1 output stage are shown in Figures 3.13 and 3.14 respectively.

The schematics of the other regulators and output stages are similar depending on the number of control loops, output power and filtering requirements.

3.2.2.2 Ramp Generator

In a constant frequency system, it was found that an inherent instability was caused by an increase of the ratio B/M, where B is the average load current, and M is the peak current. It was found that, when the ratio exceeds a certain critical value, the regulated system becomes unstable. The desired stability was acquired by adding another ramp function to the existing integrator ramp during the on-time. Figure 3.15 is the schematic of the ramp generator that is used to inject a ramp function in the regulators.

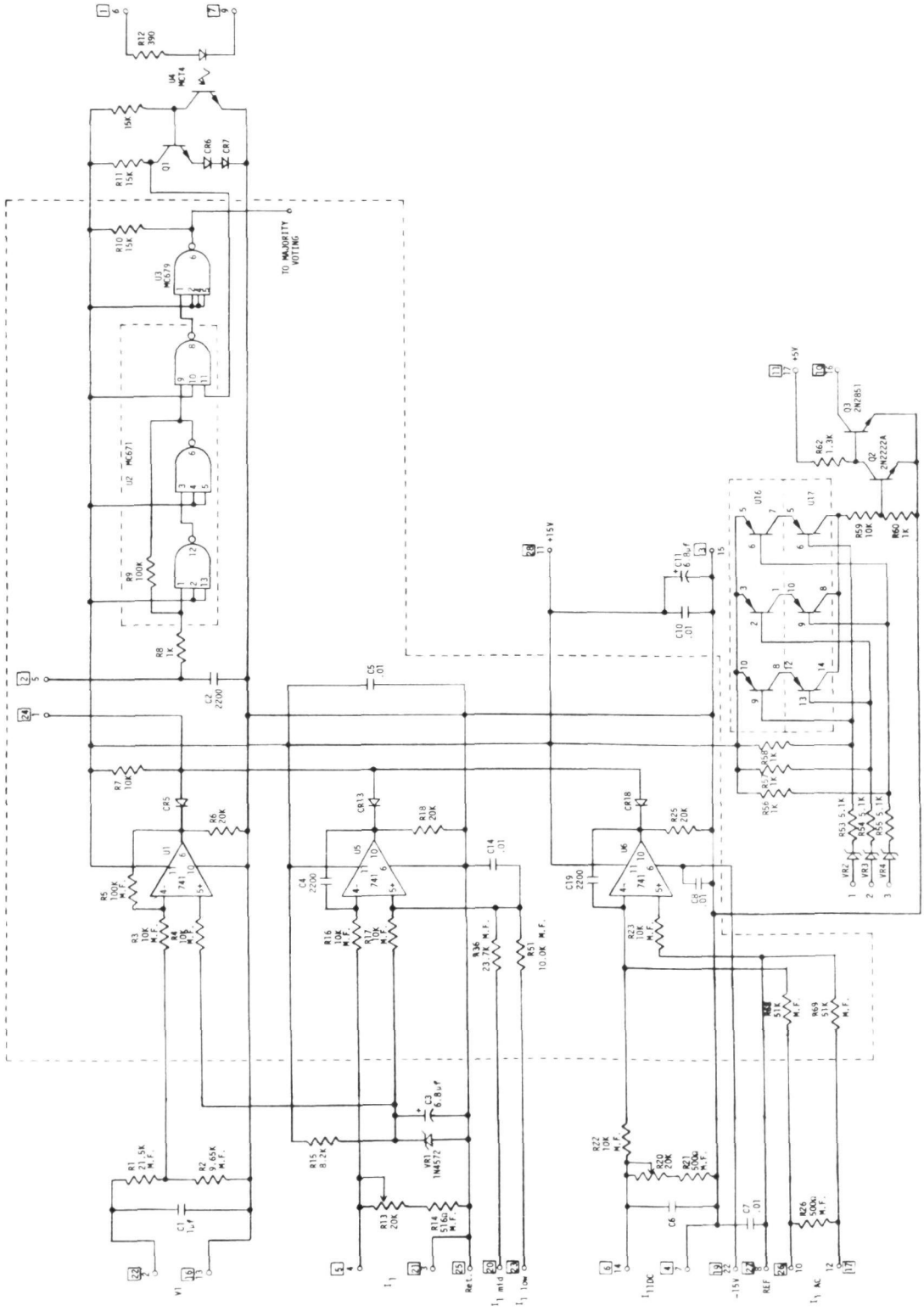


FIGURE 3.13. V1, MAIN VAPORIZER REGULATOR SCHEMATIC

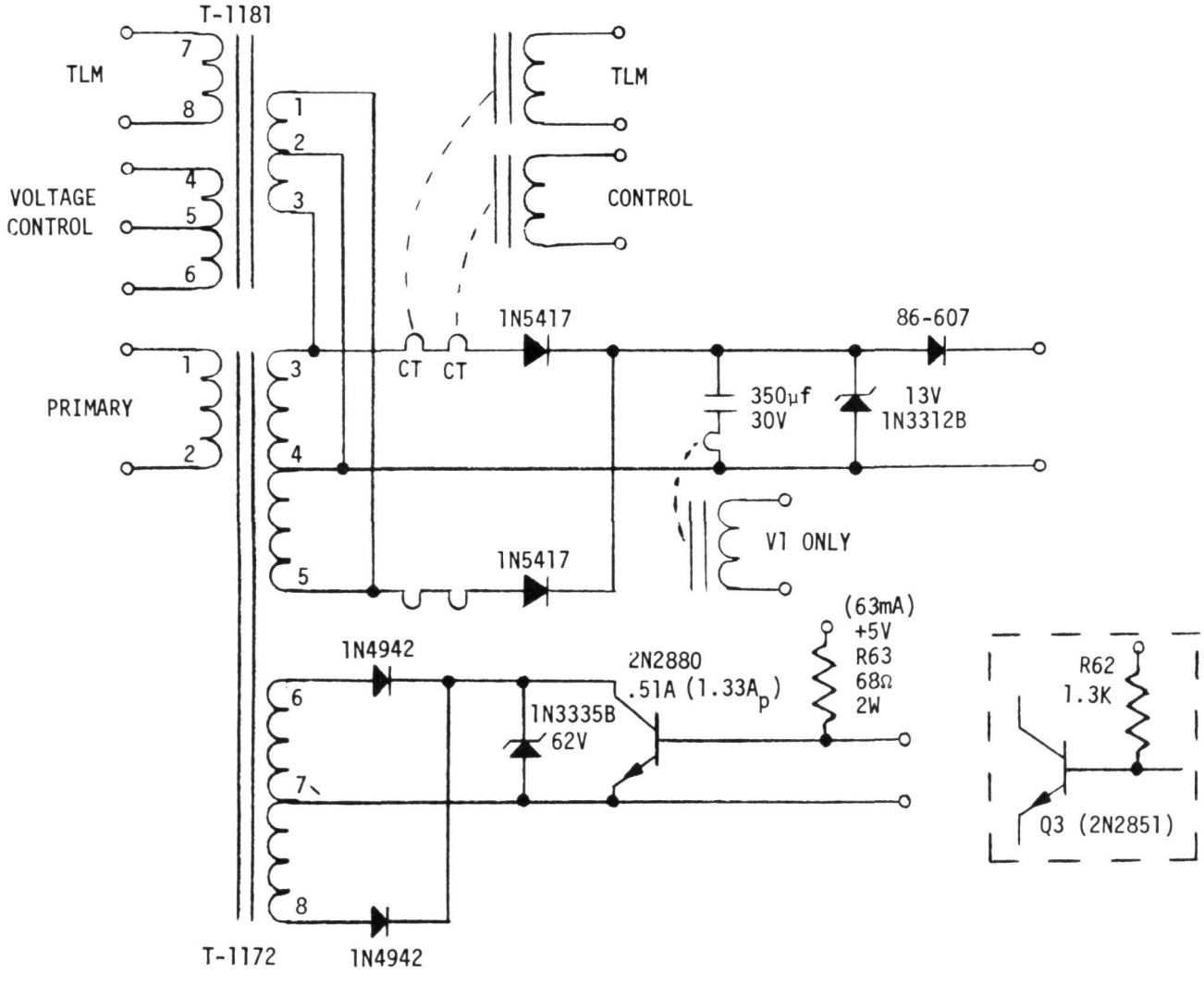


FIGURE 3.14. V1, MAIN VAPORIZER OUTPUT SCHEMATIC

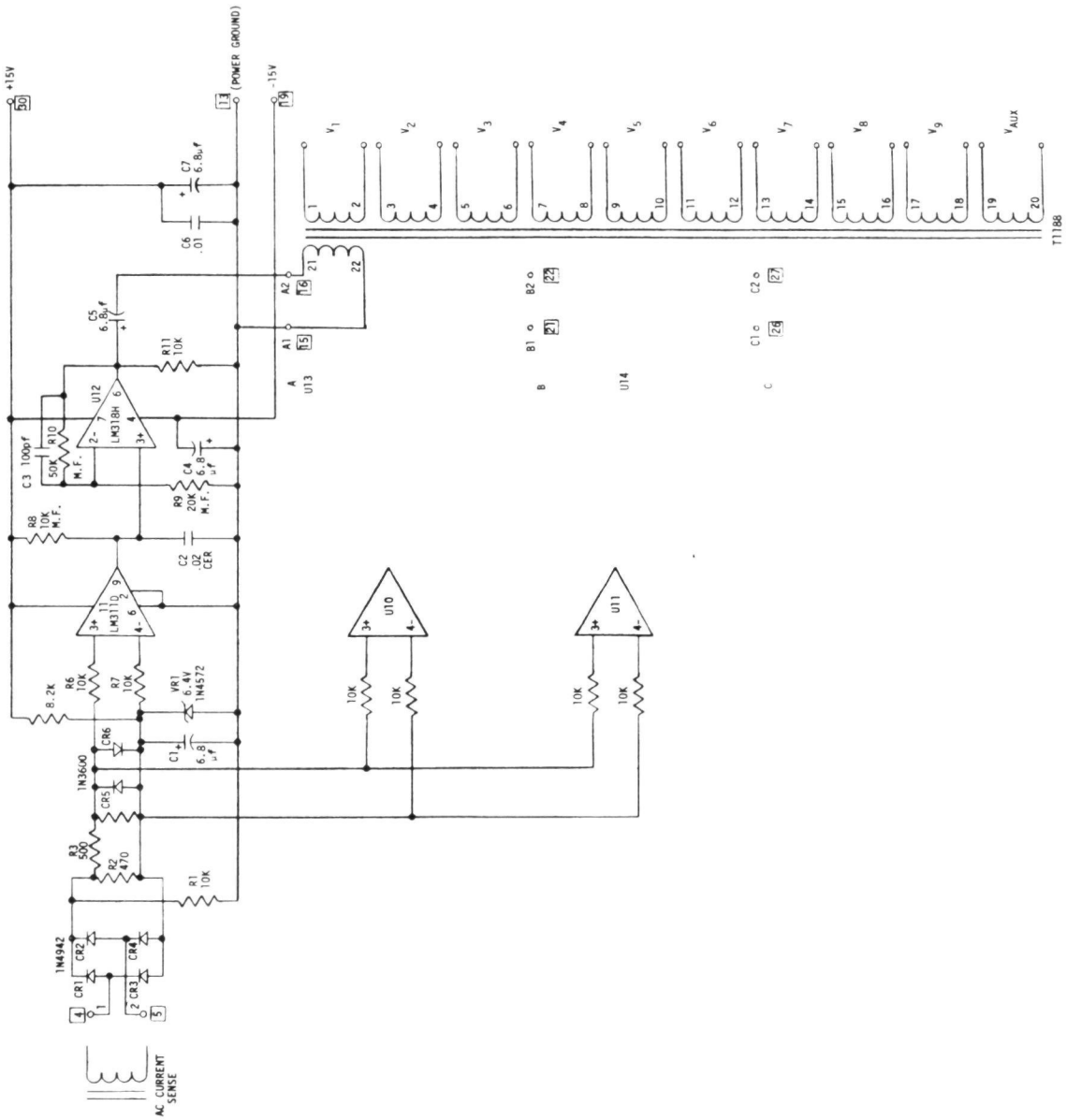


FIGURE 3.15. RAMP GENERATOR SCHEMATIC

3.3 Mechanical Design

The 30CM ion engine power processor breadboard mechanical design includes the following features:

- Packaging technique to provide for operation in a thermal vacuum environment
- Separation of control circuit, power circuits and high voltage circuits
- Grouping of control circuit components into removable modules for maintainability and tests
- Layout of power components and component mounting procedure to minimize component temperature rise
- Separation of signal lines from power lines for noise isolation
- Separation of the input and output connectors to provide isolation of functions
- Packaging technique to control electromagnetic conducted and radiated interference.

The size of the baseplate has been selected to control the maximum baseplate temperature to 140°F.

3.3.1 Mechanical Layout

Figure 3.16 shows the mechanical layout of the power processor. Its overall envelope dimensions are 145cm (57in) x 66cm (26in) x 13.6cm (5.38in) high. The unit is designed to operate in a thermal vacuum environment.

The breadboard was laid out in such a fashion so as to optimize the power flow from input to output, to separate the high voltage circuitry from the low voltage circuitry, to determine optimum grouping of components so that noise coupling from the high power circuitry to the control circuitry would be minimized and to determine the interwiring between functions.

The baseplate of the unit is a sheet of 60 mil aluminum 57in long by 26in wide. A rib one inch in from the edge is welded completely around the baseplate to give it structural rigidity. The outside rib is also used to mount the input and output connectors to the power processor. Five cross-ribs are welded onto the baseplate to give additional rigidity for the center of the baseplate.

Referring to Figure 3.16, the input power comes into the input filter area at the top of the baseplate through connector J1 and then into the beam supply inverter. The multiple output inverter is on the right side of the breadboard. All of the output circuitry is located near the bottom of the breadboard close to the output connectors. The high voltage outputs are on the right side and the low voltage outputs are on the left side of the power processor breadboard. The low level control cards are mounted near the top and left side of the breadboard away from the high power circuitry which is located near the center and bottom.

Figure 3.17 shows a typical output board. This board is for an output referenced at engine ground. The aluminum plate acts as a heat sink to conduct the heat dissipated by the power components on the board to the baseplate where it is radiated.

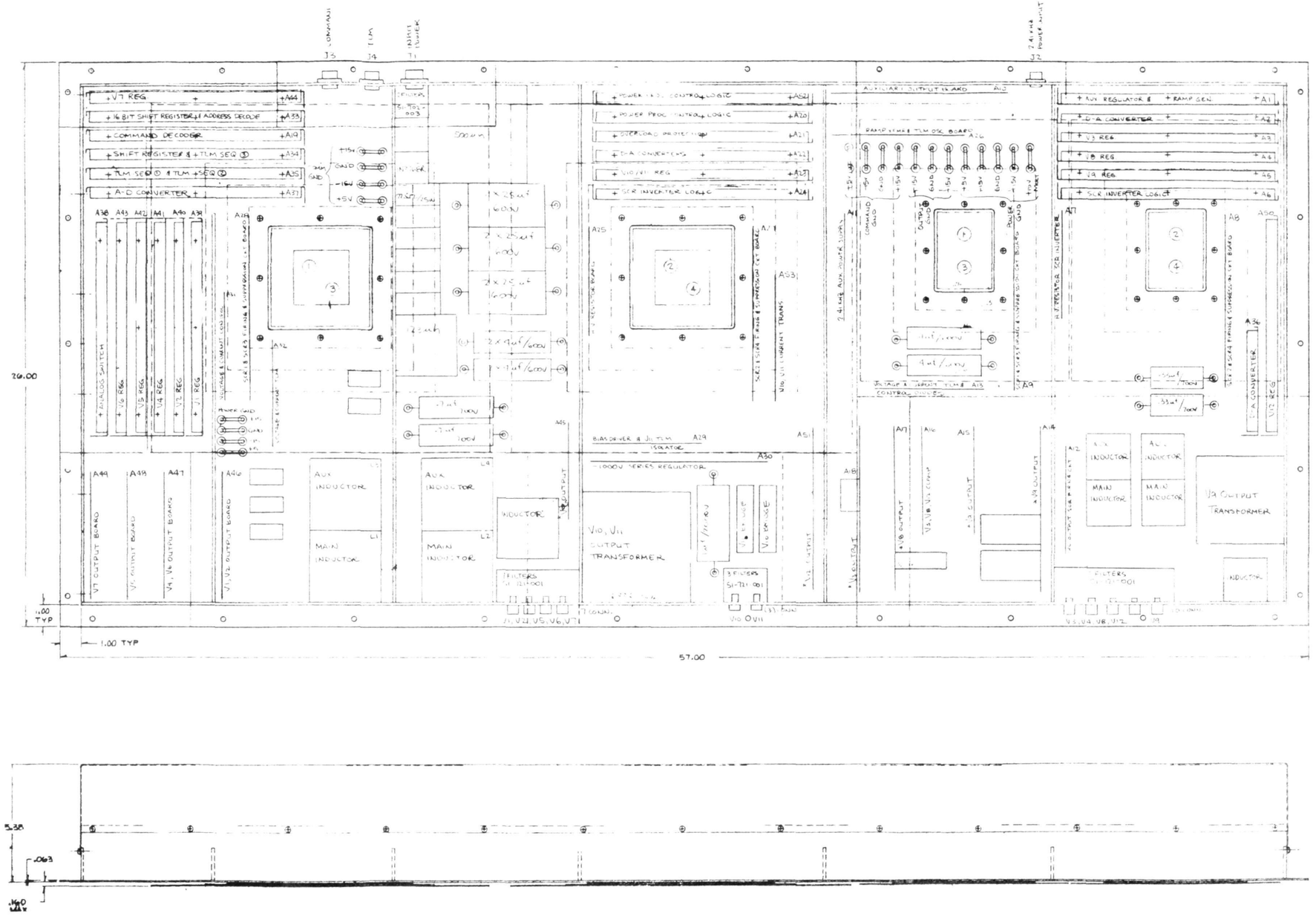


FIGURE 3.16. 30CM ION ENGINE POWER PROCESSOR
THERMAL VACUUM BREADBOARD LAYOUT

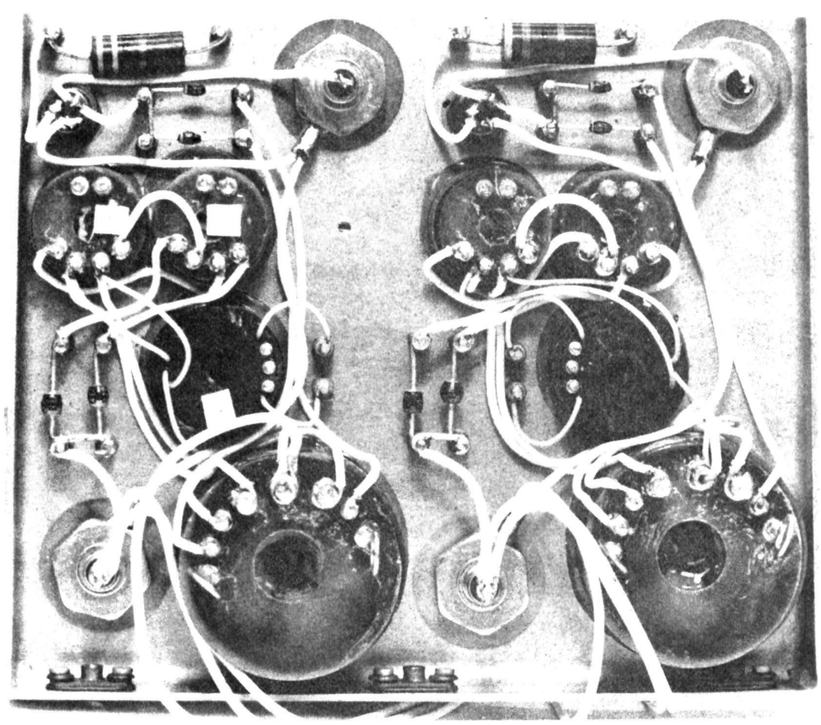


FIGURE 3.17. OUTPUT BOARD (OUTPUT AT GROUND POTENTIAL)

Figure 3.18 shows an output board where the output is referenced at the screen potential. The components mounted on the board are isolated with beryllium oxide washers for high voltage insulation. The output board itself is further isolated from the baseplate by the use of beryllium oxide insulators.

Figure 3.19 shows a photograph of the power processor breadboard.

3.3.2 Control Electronic Cards

The control electronic cards are fabricated on 5in x 10in and 5in x 5in assemblies with Cannon D type connectors for easy removal. An aluminum frame around the card provides a means for mounting the assembly to the baseplate and also provides mounting for the Cannon connector. Two types of control cards were fabricated. Printed circuit cards were used where circuit commonality enabled several cards of one type to be used i.e., the inverter logic cards and all the output regulator cards. The output regulator cards were made for the worst case design for parts deleted in the construction of the board for a particular regulator. Figure 3.20 shows a typical printed circuit card, in this case an inverter logic card. Where there was no commonality, hard wiring was used to fabricate the cards. The control logic and digital interface cards were constructed in this manner. Figure 3.21 and 3.22 are typical hard wired cards for the different frame sizes.

3.4 30CM Power Processor Test Results

Tests were performed on the 30CM Power Processor Breadboard driving a resistive load bank to check regulation, efficiency, command and protection circuit operation, telemetry circuit operation and digital interface circuit operation.

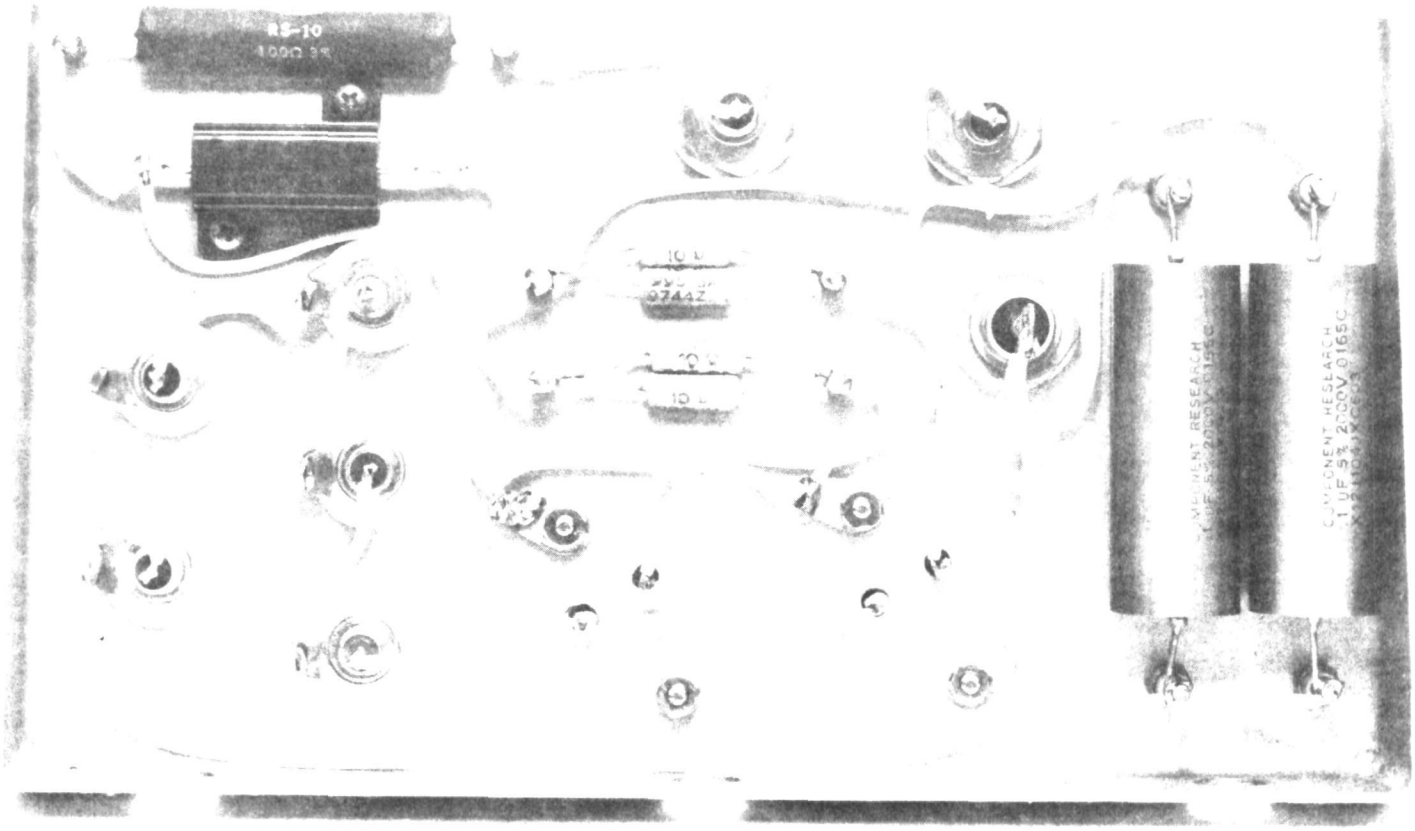


FIGURE 3.18. OUTPUT BOARD (OUTPUT AT SCREEN POTENTIAL)

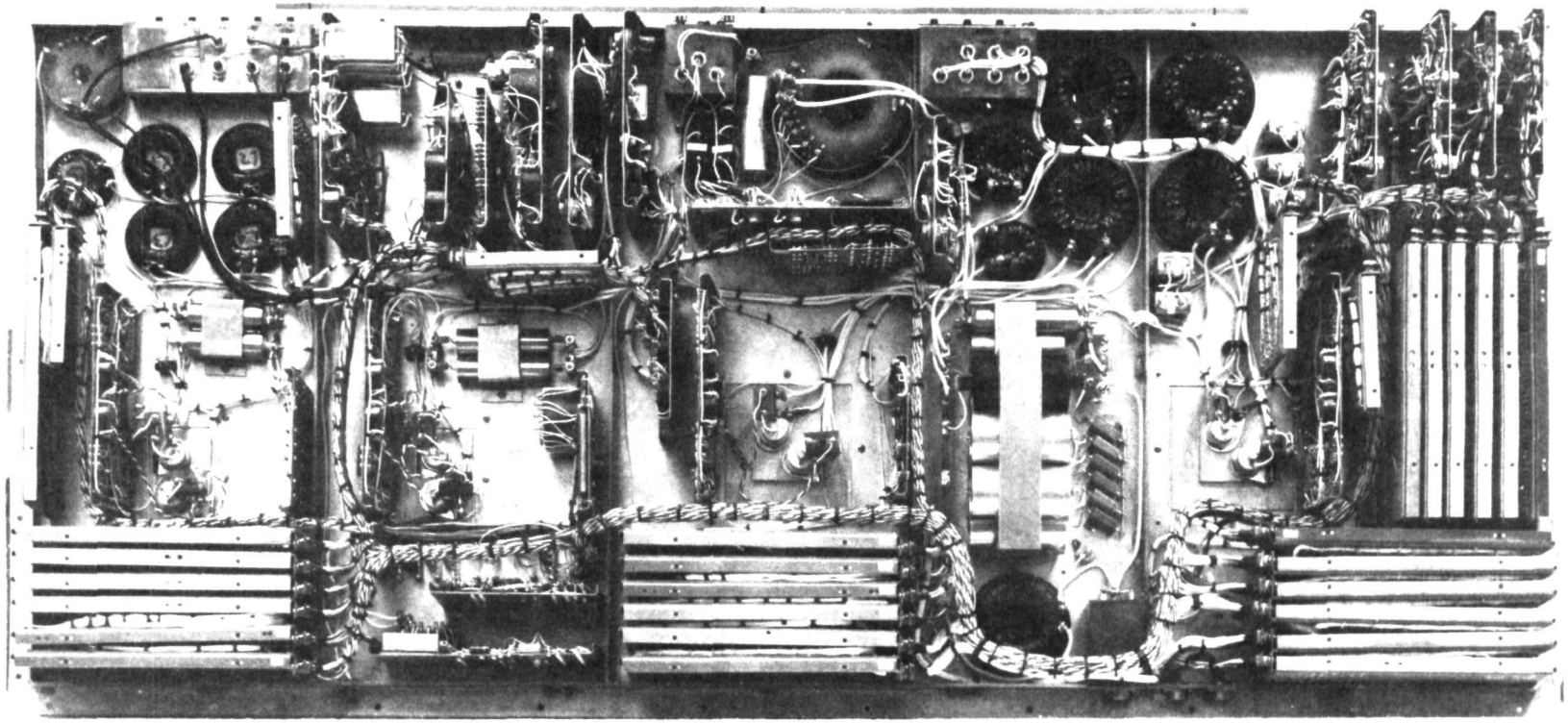


FIGURE 3.19. 30CM POWER PROCESSOR BREADBOARD

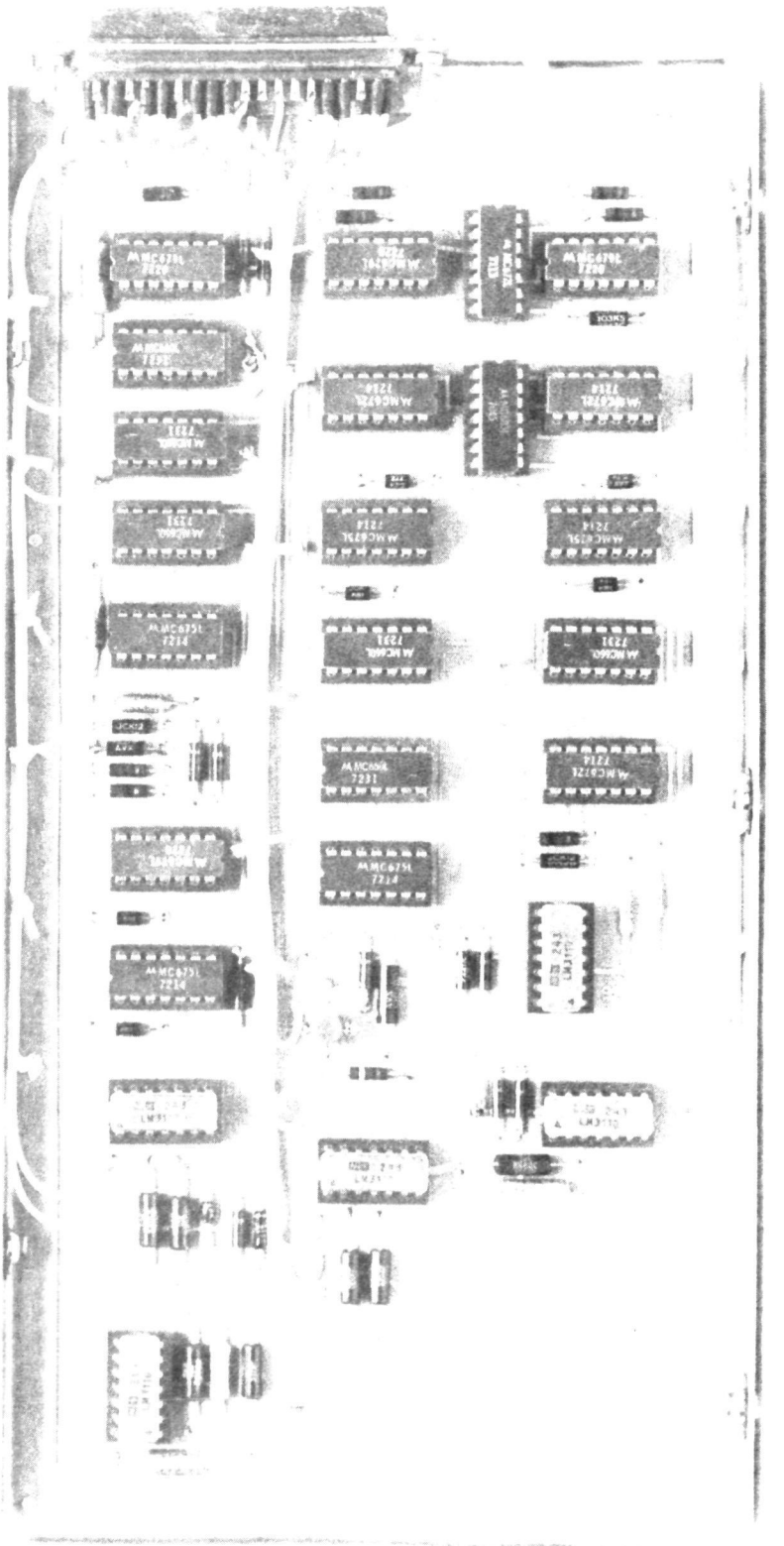


FIGURE 3.20. PRINTED CIRCUIT CONTROL CARD

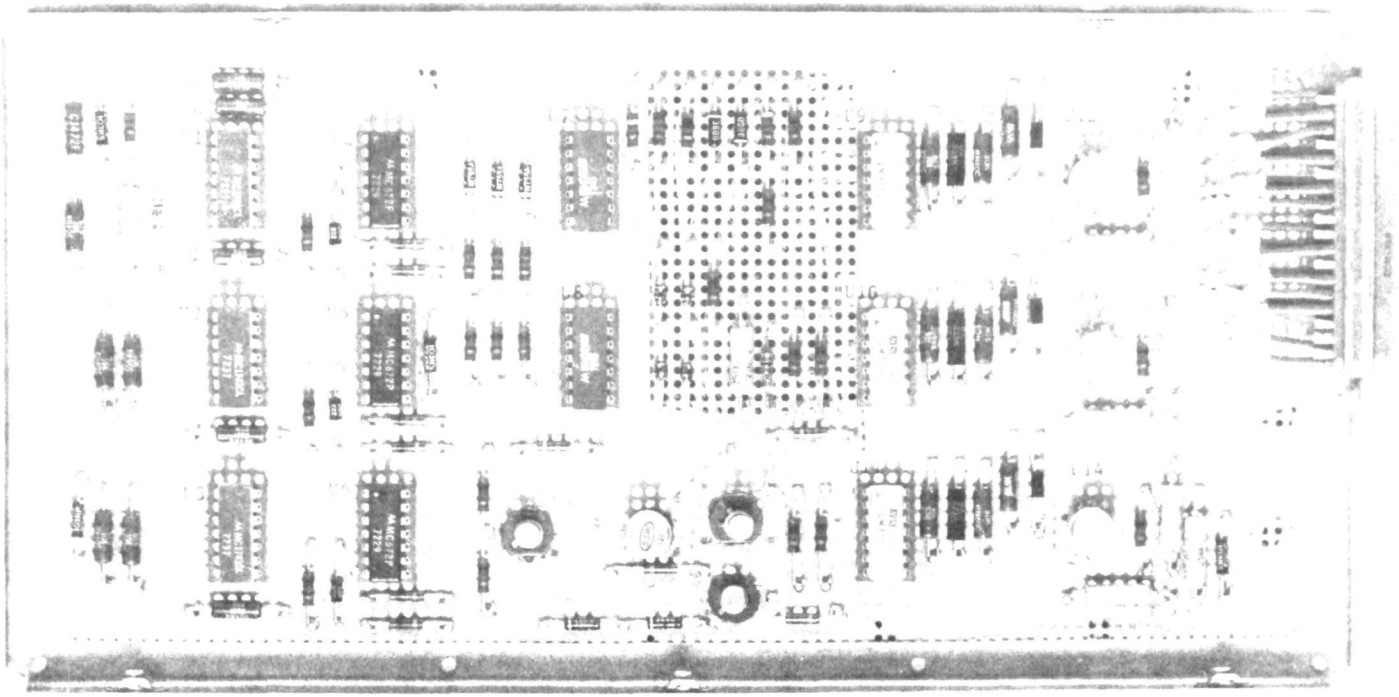


FIGURE 3.21. HARD WIRED CONTROL CARD (5in x 10in)

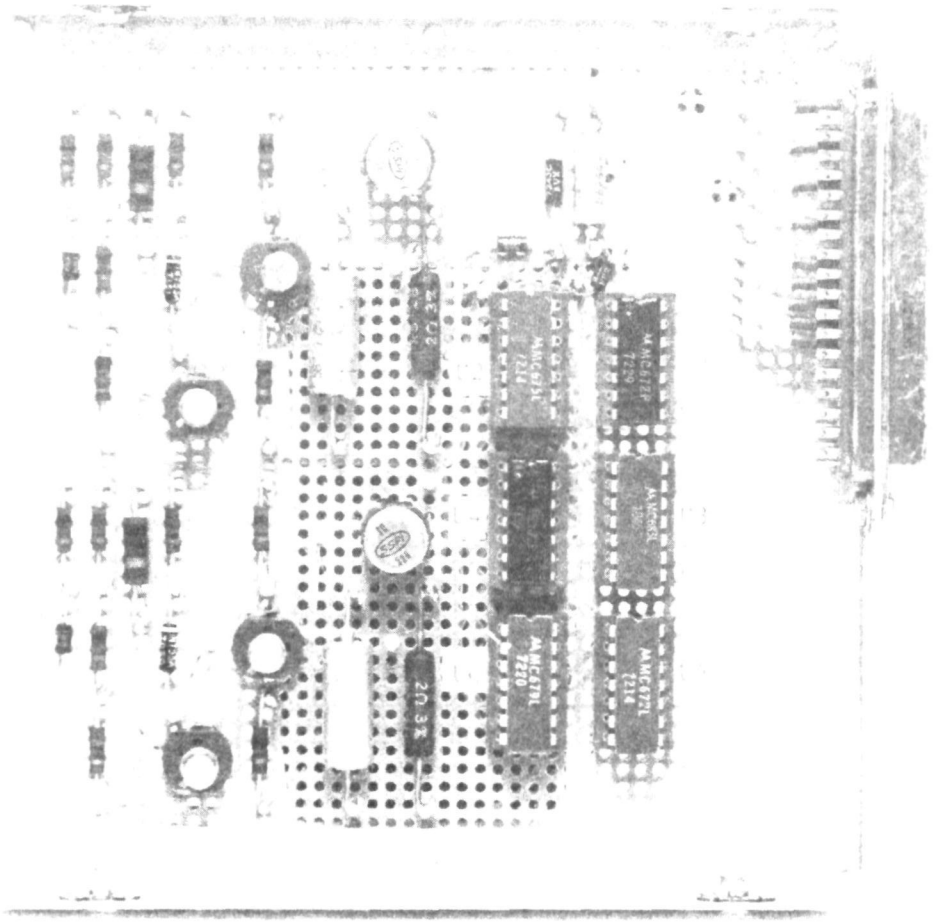


FIGURE 3.22. HARD WIRED CONTROL CARD (5in x 5in)

The breadboard operated normally during command and protection circuitry tests and digital interface circuitry tests. High circulating currents were noticed when shorts were applied to the screen supply output. The high currents are a result of the capacitors in the output EMI filters discharging when a short is applied to the output of the screen supply. This current causes high transient voltages to appear across the output and input ground returns. To decrease the transient voltage to a safe level, capacitors were added from the input ground to chassis and from the output ground to chassis.

The screen supply uses the ASDTIC principle for its regulating loop. The screen supply output voltage is tabulated below as a function of input line voltage and output current. The screen supply output voltage variation was 2v or 0.18%. The specification requirement is 1%.

SCREEN SUPPLY OUTPUT VOLTAGE-VOLTS DC				
	I_{Out} - Amps			
Vin	2.0	1.5	1.0	0.5
200	1101.9	1103.2	1103.9	1104.4
300	1100.4	1101.7	1102.2	1102.5
400	1100.6	1101.6	1102.0	1103.3

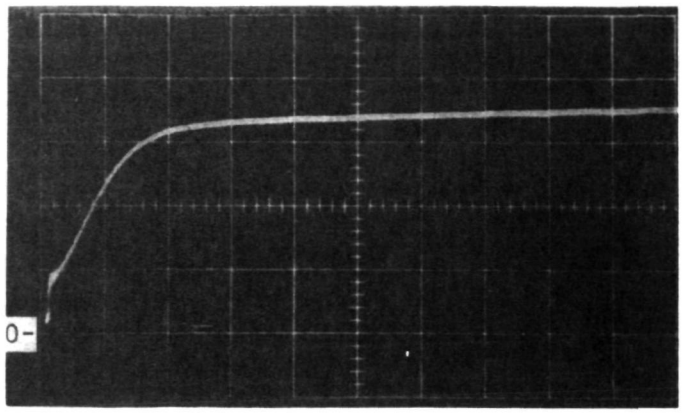
The main advantage of the series resonant inverter is that it is a current source and does not reflect a high peak surge current back to the power source. Figure 3.23 is an oscilloscope photo of the input current during turn on of the high power screen supply.

Figure 3.24 is an oscilloscope photo of the input current upon application and release of a short on the output of the screen supply.

Figure 3.25 is the screen voltage waveform at turn on. Figure 3.26 is the screen voltage waveform during an output short.

During all of these transient conditions, no large current surge was drawn from the dc power bus that could cause collapse of the current limited solar array source. No additional current regulator circuitry was needed to provide this protection feature which is inherent in the series resonant inverter design.

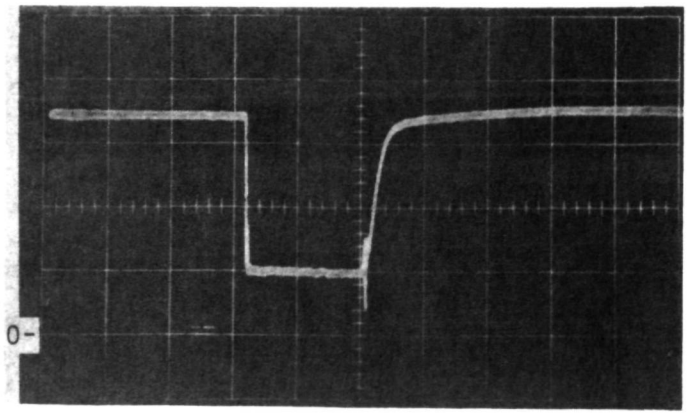
The power processor electrical performance data with V input = 300v and all outputs operating at maximum power is presented in TABLE 3-1. This is an unrealistic condition.



I = 2A/div

T = 20ms/div

FIGURE 3.23. INPUT CURRENT DURING TURN-ON



I = 2A/div

T = 5ms/div

FIGURE 3.24. INPUT CURRENT DURING SHORT

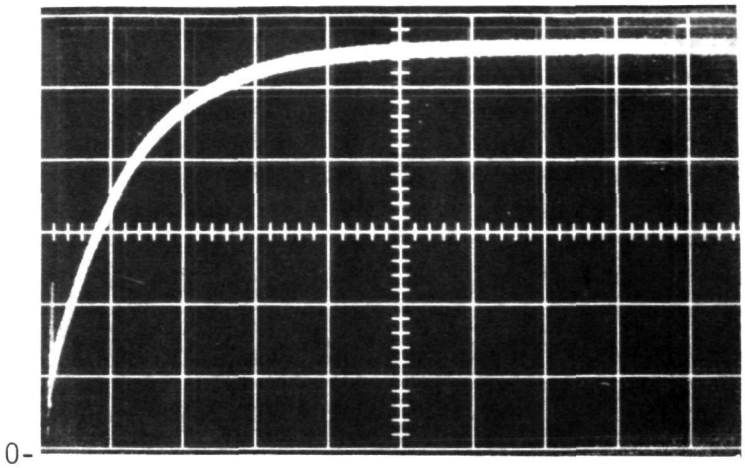


FIGURE 3.25. SCREEN VOLTAGE DURING TURN-ON

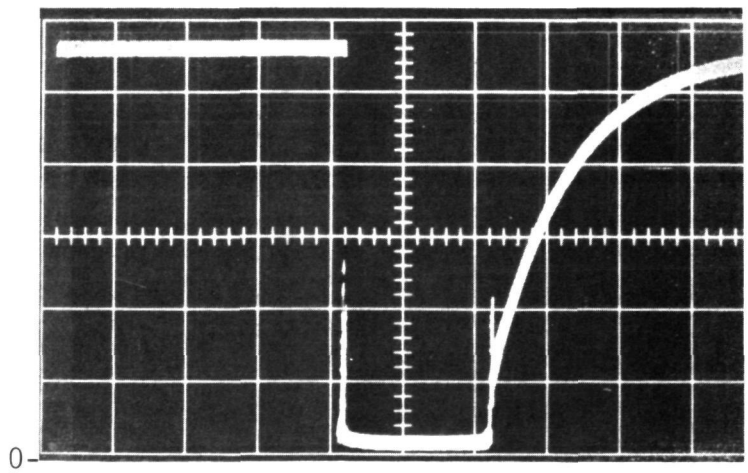


FIGURE 3.26. SCREEN VOLTAGE DURING SHORT

The input and output data over the input line range of +200v to +400vdc when operating at 2 Amps beam current is presented in Tables 3-II, 3-III, and 3-IV. Tables 3-V through 3-XIII present the data when operating at 1.5, 1.0, and 0.5 Amps beam current. Efficiency ranged from 82.35% to 84.13% at 2 Amps beam current and 60.19% to 63.80% at 0.5 Amps beam current. The VII regulation is ±2v out of 1100v (±0.18%) for all conditions of line and load variations.

Overall efficiency of the 30cm power processor as a function of input voltage and beam current is plotted in Figure 3.27.

TABLE 3-I 30cm POWER PROCESSOR ELECTRICAL PERFORMANCE WITH RESISTIVE LOAD BANK OPERATING AT MAXIMUM POWER

I Beam = 2AMP Vin = 300V

FUNCTION	VOLTAGE VOLTS	CURRENT AMPS	RIPPLE MAP-P	POWER WATTS
Vin (Main)	300.5	11.56		3473.697
Vin (Aux.)	33	0.55		18.150
V1	8.839	1.824		16.122
V2	8.770	1.821		15.970
V3	13.46	5.553		74.783
V4	8.603	3.692		31.762
V5	7.949	4.644		36.915
V6	8.974	1.821		16.342
V7	17.74	2.791		49.512
V8	50.92	0.930		47.356
V9	37.15	14.08		523.072
V10	-497.5	10 ma		4.975
V11	1095	1.949		2134.155
V12	0.749	2.220		1.663
			TOTAL OUTPUT POWER	2952.587
			EFFICIENCY	84.56% Max Power

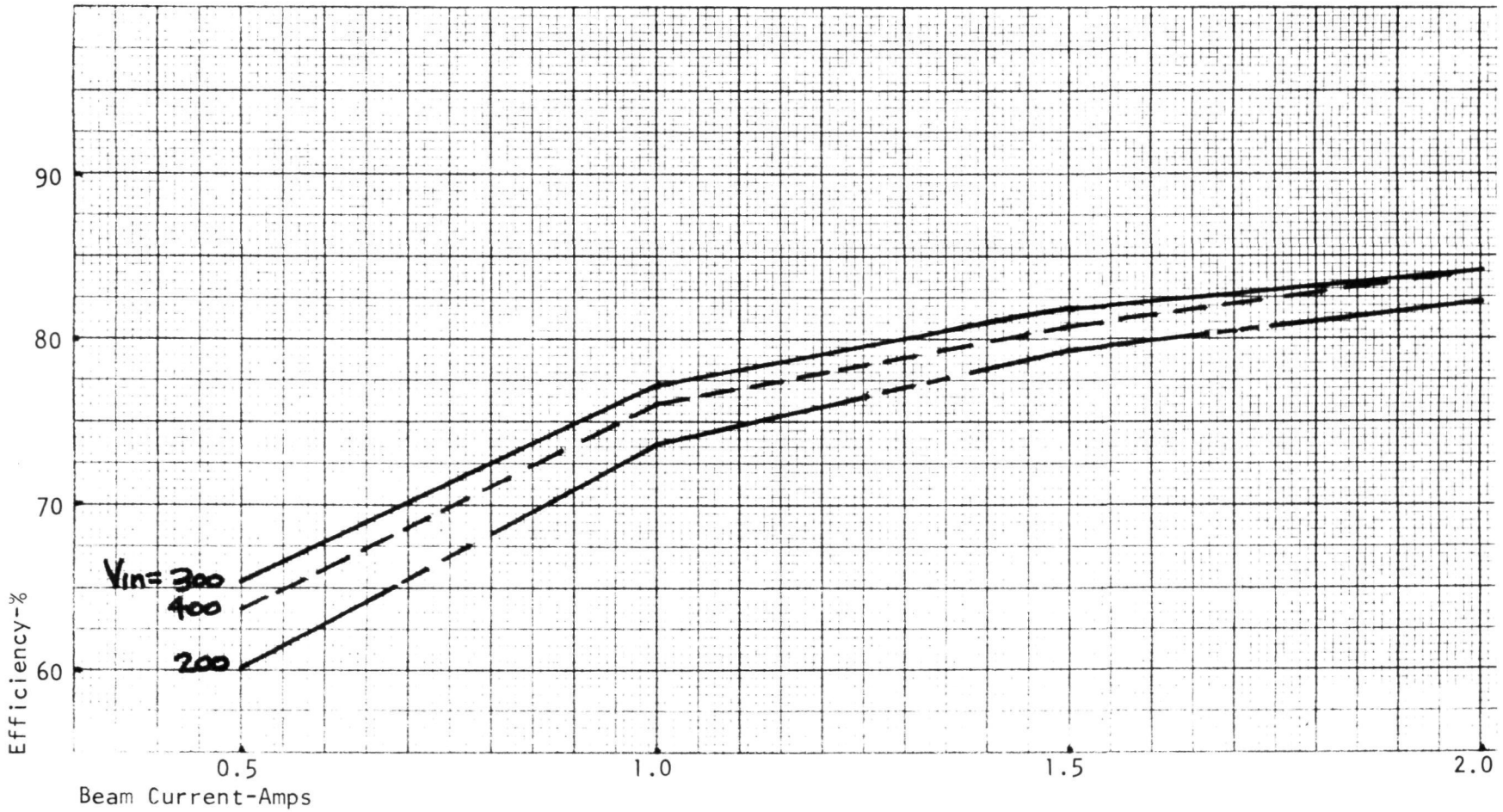


FIGURE 3.27. EFFICIENCY OF 30CM POWER PROCESSOR BREADBOARD

TABLE 3-11 30CM POWER PROCESSOR ELECTRICAL PERFORMANCE
WITH RESISTIVE LOAD BANK

I Beam = 2 AMP Vin = 200V

FUNCTION	VOLTAGE VOLTS	CURRENT AMPS	RIPPLE MAP-P	POWER WATTS
Vin (Main)	204.7	16.46	200	3368.56
V1	7.215	1.062	100	7.66
V2	3.569	1.090	85	3.89
V3	---	---	---	--
V4	---	---	---	--
V5	---	---	---	--
V6	3.445	1.135	170	3.91
V7	11.858	1.995	140	23.69
V8	10.555	.735	28	7.76
V9	39.41	13.96	310	550.16
V10	-503.9	10.398 ma		5.24
V11	1101.9	1.971	55v	2171.84
V12	.09	.46	380	.04
			TOTAL OUTPUT POWER	2774.19
			EFFICIENCY	82.35%

TABLE 3-III 30CM POWER PROCESSOR ELECTRICAL PERFORMANCE WITH RESISTIVE LOAD BANK

I Beam = 2AMP Vin = 300V

FUNCTION	VOLTAGE VOLTS	CURRENT AMPS	RIPPLE MAP-P	POWER WATTS
Vin	309.1	10.672	210	3298.79
V1	7.138	1.0583	80	7.55
V2	3.529	1.087	72	3.84
V3	---	---	---	---
V4	---	---	---	---
V5	---	---	---	---
V6	3.439	1.137	140	3.91
V7	11.942	2.014	100	24.05
V8	10.527	.7362	26	7.75
V9	39.46	13.98	300	551.65
V10	-498.9	10.3 ma		5.14
V11	1100.4	1.972	50V	2169.99
V12	.091	.46	200	.04
			TOTAL OUTPUT POWER	2773.92
			EFFICIENCY	84.09%

TABLE 3-IV 30CM POWER PROCESSOR ELECTRICAL PERFORMANCE
WITH RESISTIVE LOAD BANK

I Beam = 2AMP Vin - 400V

FUNCTION	VOLTAGE VOLTS	CURRENT AMPS	RIPPLE MAP-P	POWER WATTS
Vin	391.9	8.390	210	3288.01
V1	7.195	1.0596	56	7.62
V2	3.387	1.032	70	3.49
V3	---	---	---	---
V4	---	---	---	---
V5	---	---	---	---
V6	3.435	1.130	120	3.88
V7	11.94	2.011	110	24.01
V8	10.308	.7181	24	7.40
V9	39.06	13.89	340	542.54
V10	-503.6	10.39 ma		5.32
V11	1100.6	1.964	50V	2171.85
V12	.0915	.46	220	.04
			TOTAL OUTPUT POWER	2766.15
			EFFICIENCY	84.13%

TABLE 3-V 30CM POWER PROCESSOR ELECTRICAL PERFORMANCE
WITH RESISTIVE LOAD BANK

I Beam = 1.5AMP Vin = 200V

FUNCTION	VOLTAGE VOLTS	CURRENT AMPS	RIPPLE MAP-P	POWER WATTS
Vin	202.5	13.11	400	2654.77
V1	7.226	1.0629	100	7.68
V2	3.567	1.087	90	3.88
V3	---	---	---	---
V4	---	---	---	---
V5	---	---	---	---
V6	3.446	1.135	160	3.91
V7	11.894	2.007	150	23.87
V8	10.690	.7418	32	7.93
V9	40.18	10.58	240	425.10
V10	-502.6	10.38 ma		5.22
V11	1103.2	1.477	60V	1629.43
V12	.353	2.05	780	.72
		TOTAL OUTPUT POWER		2107.74
			EFFICIENCY	79.39%

TABLE 3-VI 30CM POWER PROCESSOR ELECTRICAL PERFORMANCE WITH RESISTIVE LOAD BANK

I Beam - 1.5AMPS Vin = 300V

FUNCTION	VOLTAGE VOLTS	CURRENT AMPS	RIPPLE MAP-P	POWER WATTS
Vin	303.7	8.492	420	2579.02
V1	7.177	1.059	90	7.60
V2	3.556	1.087	80	3.86
V3	---	---	---	---
V4	---	---	---	---
V5	---	---	---	---
V6	3.438	1.134	160	3.90
V7	11.984	2.025	120	24.27
V8	10.56	.733	30	7.74
V9	40.02	10.58	240	423.41
V10	-498.2	10.286 ma		5.12
V11	1101.7	1.482	50V	1632.72
V12	.35	2.05	7.0	.72
			TOTAL OUTPUT POWER	2109.34
			EFFICIENCY	81.79%

TABLE 3-VII 30CM POWER PROCESSOR ELECTRICAL PERFORMANCE WITH RESISTIVE LOAD BANK

I Beam = 1.5AMP Vin = 400V

FUNCTION	VOLTAGE VOLTS	CURRENT AMPS	RIPPLE MAP-P	POWER WATTS
Vin	393.1	6.581	380	2587.16
V1	7.191	1.059	70	7.61
V2	3.565	1.090	64	3.88
V3	---	---	---	---
V4	---	---	---	---
V5	---	---	---	---
V6	3.428	1.128	140	3.87
V7	11.887	2.005	110	23.83
V8	10.467	.7223	26	7.56
V9	40.02	10.48	300	419.41
V10	-501.8	10.355 ma		5.20
V11	1101.6	1.471	60V	1620.45
V12	.35	2.04	680	.72
			TOTAL OUTPUT POWER	2092.53
			EFFICIENCY	80.88%

TABLE 3-VIII 30CM POWER PROCESSOR ELECTRICAL PERFORMANCE
WITH RESISTIVE LOAD BANK
I Beam = 1AMP Vin = 200V

FUNCTION	VOLTAGE VOLTS	CURRENT AMPS	RIPPLE MAP-P	POWER WATTS
Vin	202.5	9.690	480	1962.22
V1	7.242	1.065	100	7.71
V2	3.570	1.096	100	3.91
V3	---	---	---	---
V4	---	---	---	---
V5	---	---	---	---
V6	3.393	1.119	180	3.80
V7	11.948	2.015	160	24.07
V8	10.778	.7442	30	8.02
V9	39.97	6.98	200	278.99
V10	-502.1	10.35 ma		5.20
V11	1103.9	1.0091	65V	1113.94
V12	.35	2.04	1.3	.72
			TOTAL OUTPUT POWER	1446.36
			EFFICIENCY	73.71%

TABLE 3-IX 30CM POWER PROCESSOR ELECTRICAL PERFORMANCE
WITH RESISTIVE LOAD BANK

I Beam = 1AMP Vin = 300V

FUNCTION	VOLTAGE VOLTS	CURRENT AMPS	RIPPLE MAP-P	POWER WATTS
Vin	303.5	6.168	370	1871.93
V1	7.193	1.0607	95	7.63
V2	3.565	1.090	90	3.88
V3	---	---	---	---
V4	---	---	---	---
V5	---	---	---	---
V6	3.431	1.129	170	3.87
V7	11.891	2.007	125	23.86
V8	10.748	.7425	32	7.98
V9	39,90	6.98	210	278.50
V10	-499.0	10.29 ma		5.13
V11	1102.2	1.0075	65V	1110.47
V12	.35	2.04	780	.72
		TOTAL OUTPUT POWER		1442.04
		EFFICIENCY		77.03%

TABLE 3-X 30CM POWER PROCESSOR ELECTRICAL PERFORMANCE
WITH RESISTIVE LOAD BANK

I Beam = 1AMP Vin = 400V

FUNCTION	VOLTAGE VOLTS	CURRENT AMPS	RIPPLE MAP-P	POWER WATTS
Vin	392.3	4.835	400	1896.83
V1	7.194	1.060	95	7.62
V2	3.564	1.089	80	3.88
V3	---	---	---	---
V4	---	---	---	---
V5	---	---	---	---
V6	3.390	1.116	150	3.78
V7	11.945	2.014	125	24.06
V8	10.579	.7326	32	7.75
V9	39.98	6.98	150	279.06
V10	-501.0	10.33 ma		6.66
V11	1102.0	1.007	70V	1109.71
V12	.35	2.04	740	.72
			TOTAL OUTPUT POWER	1443.24
			EFFICIENCY	76.09%

TABLE 3-XI 30CM POWER PROCESSOR ELECTRICAL PERFORMANCE
WITH RESISTIVE LOAD BANK

I Beam = 0.5AMP Vin = 200V

FUNCTION	VOLTAGE VOLTS	CURRENT AMPS	RIPPLE MAP-P	POWER WATTS
Vin	203.1	6.094	600	1237.65
V1	7.249	1.068	100	7.74
V2	3.567	1.092	90	3.89
V3	---	---	---	---
V4	---	---	---	---
V5	---	---	---	---
V6	3.392	1.119	160	3.79
V7	11.905	2.010	160	23.93
V8	10.736	.7426	30	7.97
V9	39.69	3.49	120	138.52
V10	-499.7	10.31 ma		5.15
V11	1104.4	.501	70V	553.30
V12	.35	2.04	900	.71
			TOTAL OUTPUT POWER	745.0
			EFFICIENCY	60.19%

TABLE 3-XII 30CM POWER PROCESSOR ELECTRICAL PERFORMANCE
WITH RESISTIVE LOAD BANK

I Beam = 0.5AMP Vin = 300V

FUNCTION	VOLTAGE VOLTS	CURRENT AMPS	RIPPLE MAP-P	POWER WATTS
Vin	302.8	3.758	500	1137.97
V1	7.196	1.061	95	7.63
V2	3.564	1.090	90	3.88
V3	---	---	---	---
V4	---	---	---	---
V5	---	---	---	---
V6	3.392	1.117	150	3.79
V7	11.994	2.023	135	24.26
V8	10.725	.740	28	7.94
V9	39.58	3.49	84	138.13
V10	-497.3	10.26 ma		5.10
V11	1102.5	.5019	70V	553.34
V12	.35	2.04	640	.72
			TOTAL OUTPUT POWER	744.79
			EFFICIENCY	65.45%

TABLE 3-XIII 30CM POWER PROCESSOR ELECTRICAL PERFORMANCE WITH RESISTIVE LOAD BANK

I Beam = 0.5AMP Vin = 400V

FUNCTION	VOLTAGE VOLTS	CURRENT AMPS	RIPPLE MAP-P	POWER WATTS
Vin	393.5	2.957		1163.80
V1	7.001	1.110		7.71
V2	3.597	1.131		4.07
V3	---	---		---
V4	---	---		---
V5	---	---		---
V6	3.466	1.003		3.48
V7	11.71	1.995		23.36
V8	10.24	.728		7.45
V9	40.1	3.50		140.35
V10	-494	10.20 ma		5.04
V11	1101.3	.4974		547.79
V12	.73	4.4		3.21
			TOTAL OUTPUT POWER	742.46
			EFFICIENCY	63.80%

3.5 Design Analysis

An analysis of the 30CM ion thruster power processor was conducted to give more details of the characteristics and performance of the power processor. The following analyses were performed to establish the power processor's characteristics:

- o Efficiency Analysis
- o Weight Analysis
- o Part Count Analysis
- o Reliability Analysis

3.5.1 Efficiency Analysis

Table 3-XIV lists the estimated losses in all the functions of the power processor. The major loss is in the screen and multiple power SCR's. Other major contributors are the power inductors, the power transformers, and the SCR suppression networks which control the dv/dt.

The efficiency of the multiple output inverter is lower due to the large number of output voltages and the losses of the output rectifiers. The losses due to the output series diodes for arcing protection also contribute to the lower efficiency of the multiple output inverter.

3.5.2 Weight Analysis

Table 3-XV lists the different component weights for each function in the 30CM ion thruster power processor. Circuit redundancy is included in the weight analysis.

Table 3-XVI summarizes as power processor functions, the information contained in Table 3-XV.

The multiple output supply (39.4%), the screen/accelerator supply (37.2%), and the input filter (17.8%) account for 94.4% of the total weight.

The multiplicity of parts in the multiple output supply contributes to its high weight (more than four times the components in the screen/accelerator supply). The screen/accelerator supply is the principle supplier of power (2.6kw) with the resultant heavier components. The input filter

TABLE 3-XIV 30CM POWER PROCESSOR TVBB EFFICIENCY AND LOSSES AT 2AMP BEAM

Screen Inverter	Watts	Multiple Inverter	Watts
Output Power	2200	Output Power	563
Losses		Losses	
SCR's	172.7	SCR's	76.6
Inductors	16.4	Inductors	8.2
Capacitors	4.5	Capacitors	2.3
Suppression	32.6	Suppression	16.3
Output Transformer	17.7	(11) Output Transformers	34.3
Output Diodes	7.5	(11) Output Diodes	32.5
Output Capacitors	2.0	(11) Output Capacitors	12.7
Subtotal	253.4	Series Diodes	11.2
		(11) Regulators	12.5
Controls		Subtotal	206.6
Power Processor	38.9		
Digital Interface Unit	31.7	Σ Output Power	2763
Input Filter		Σ Losses	540.8
Due to Screen	6.8	Input Power	3303.8
Due to Multiple	3.4	Efficiency	83.6%

(Estimated) Calculated Efficiency
(less than measured)

TABLE 3-XV 30CM POWER PROCESSOR TVBB COMPONENT WEIGHTS

FUNCTION	ITEM	WEIGHT-gms
Input Filter	Inductor a) 1st Stage	1450
	b) 2nd Stage	320
	Capacitors 1st Stage	1552
	Resistors	80
	Diode	17
	Subtotal	3419
Beam Supply	1. Inverter power stage	
	Capacitor-input	302
	Capacitor-series	177
	Inductor-series	4130
	SCR's	434
	Suppression	228
	2. SCR firing	39
	3. Inverter control logic	80
	4. Output power circuits	
	Transformer-output	1370
	Output rectifiers	198
	Output capacitors	208
	Zener diodes	77
	Power transistors	34
	Resistors	27
	Bias driver	17
	5. Regulator controls	
	Controls	74
	Transformers	48
	Subtotal	7215
Multiple Output Inverter	1. Inverter power stage	
	Capacitor-input	151
	Capacitor-series	135
	Inductor-series	1093
	SCR's	434
	Suppression	228
	2. SCR firing	39
	3. Inverter control logic	80
	4. Output power circuits	
	Transformers	1635
	Capacitors	926
	Diodes	672
	Transistors	66
	Resistors	16
	Zener diodes	477
	5. Output regulators	587
	6. Auxiliary output power	830
	7. Auxiliary output regulator	202
	Subtotal	7571
Command & Protection	Command logic	83
	Protection	92
	Subtotal	175
Telemetry	Telemetry	305
Digital Interface	Digital Interface	537

TABLE 3-XVI SUMMARY OF 30CM POWER PROCESSOR TVBB COMPONENT WEIGHTS

ITEM	WEIGHT GRAMS	PERCENTAGE OF TOTAL WT.
Input Filter	3419	17.8
Beam Supply	7215	37.5
Multiple Output Supply	7571	39.4
Command & Protection	175	.9
Telemetry	305	1.6
Digital Interface	537	2.8
TOTAL	19,222	100%

is designed to meet the input ripple and EMI requirements with a resultant heavy input filter.

3.5.3 Part Count Analysis

Table 3-XVII lists the detail analysis of the part count for the basic functions of the 30CM ion thruster power processor breadboard. Redundancy is noted in the different areas and increases the total part count. Table 3-XVIII summarizes the part count for the different functions. The number of in-line components that can contribute to failure and have no redundancy are also tabulated.

The total part count is 3044 components of which 2041 can contribute to the power processor failure. Of the 2041 parts, 674 parts are in the digital interface unit. The resultant part count is therefore 1367 parts which can contribute to the power processor failure.

TABLE 3-XVII 30CM POWER PROCESSOR TVBB COMPONENT WEIGHTS

FUNCTION	ITEM	NO.
Input Filter	Inductors	2
	Capacitors	6
	Resistors	6
	Diode	1
	Subtotal	15
Beam Supply	1. Inverter Power Stage	
	Capacitor-input	4
	Capacitor-series	2
	Inductor-series	5
	SCR's	4
	Suppression	36
	2. SCR Firing	76
	3. Inverter Control Logic	92
	4. Output Power Circuits	
	Transformer-output	1
	Output rectifiers	5
	Output capacitors	3
	Zener diodes	7
	Power Transistors	2
	Resistors	4
	Bias Driver	19
	5. Regulator Controls	
	Controls	121
	Transformers	4
	Subtotal	385
Multiple Output Inverter	1. Inverter Power Stage	
	Capacitor-input	2
	Capacitor-series	2
	Inductor-series	5
	SCR's	4
	Suppression	36
	2. SCR Firing	76
	3. Inverter Control Logic	92
	4. Output Power Circuits	
	Transformers	38
	Capacitors	17
	Diodes	64
	Transistors	9
	Resistors	11
	Zener diodes	25
	5. Output Regulators	1135
	6. Auxiliary Output	68
	7. Auxiliary Output Regulator	87
	Subtotal	1671
Command & Protection	Command Logic	84
	Protection	78
	Subtotal	162
Telemetry	Telemetry	137
Digital Interface	Digital Interface	674

TABLE 3-XVIII SUMMARY OF 30CM POWER PROCESSOR TVBB PARTS COUNT

ITEM	TOTAL NO. OF PARTS	IN-LINE FAILURE PARTS
Input Filter	15	15
Beam Supply	385	299
Multiple Output Supply	1671	754
Command & Protection	162	162
Telemetry	137	137
Digital Interface	674	674
TOTAL	3044	2041

3.5.4 Reliability Analysis

Table 3-XIX lists the summary of the failure rate for the power processor, digital interface unit and telemetry conditioners. The detail reliability analysis per function including reliability block diagram is also presented.

The component failure rate is based on present flight data where possible and does not include any long term projection of component improvement. In comparing power processor designs, the componenent failure rate data for the analysis should be the same.

Majority voting (2 out of 3) circuits have been used in the output regulator control electronics in the present design. Redundancy circuit techniques can also be used in the command and protection system and greatly improve the basic power processor reliability without any large penalty in weight or efficiency.

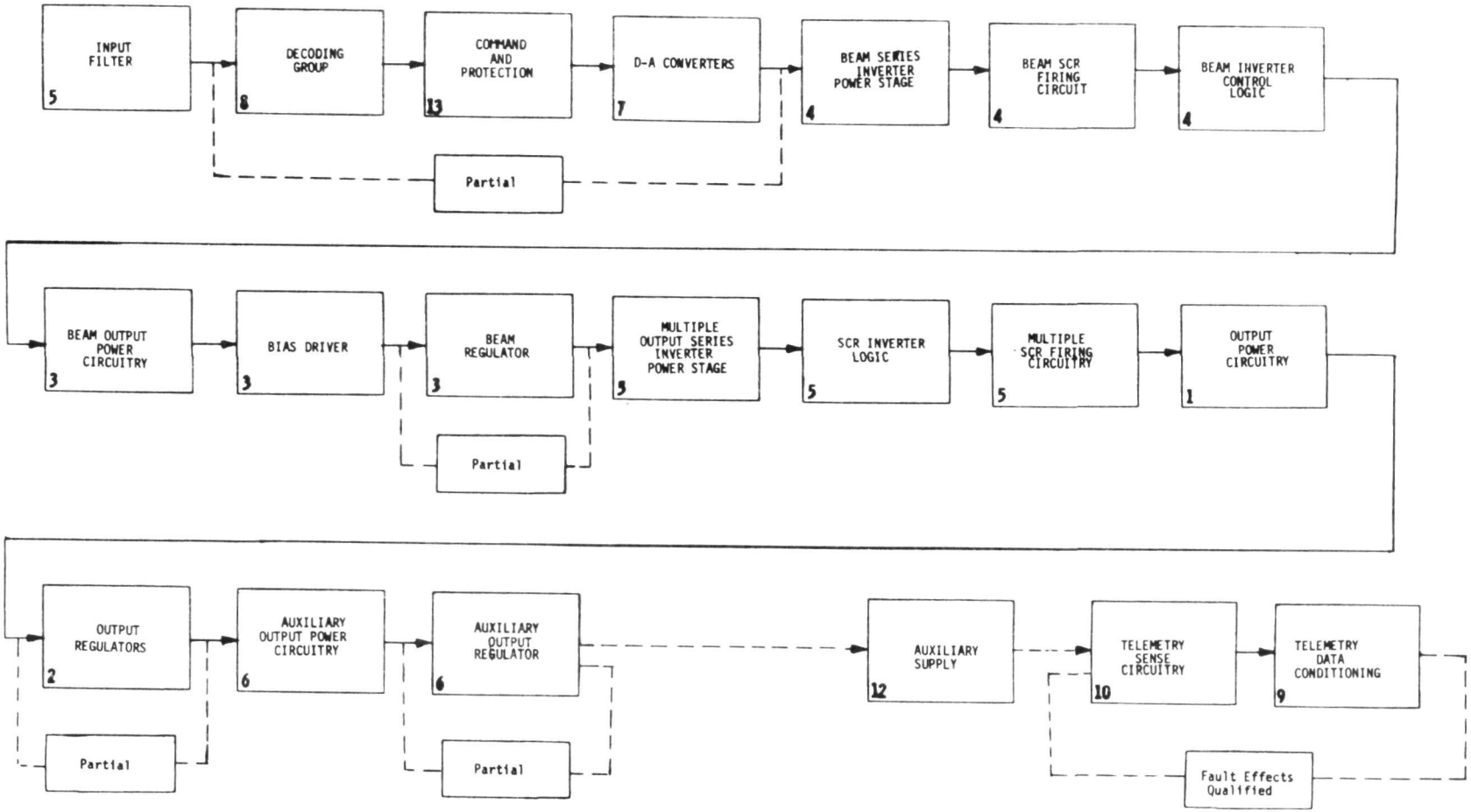
Figure 3.28 is a system reliability flow diagram for the ion engine power processor. For convenience in parts failure rate analysis, the parts have been organized into arrays representing functional groups of modules.

The parts and component failure rates (Table 3-XX) were determined in several steps. Failure rates were first associated with parts from lists (primarily the TRW internal applicable list). The TRW list was considered primary since (1) it basically reflects one of the best experience samples in the industry, (2) it incorporates other experience samples in the industry, (3) it includes a general application adjustment for spacecraft, and (4) internal data exist for computing or adjusting for suspected inapplicable or small sample size cases. Other internal and external sources were also used. A few such typical sources are listed in Table 3-XXI Sources of Reliability Failure Rate Data. The effect of existing local and component redundancy has been included in the failure rates in accordance with the diagram.

TABLE 3-XIX. 30CM ION ENGINE THERMAL VACUUM ENGINE POWER PROCESSOR BREADBOARD

FAILURE RATES

FUNCTION	F.R. PARTS PER 10^9 HOURS	PARTS	AV. F.R. PER PART PARTS PER 10^9 HOURS	RELIABILITY FOR 10,000 HRS.
Power System: (Ref. Groups 1-6, & 11-13)	18,477	1230	15.0	.83
Digital Interface: (Ref. Groups 7-9)	9,339	674	13.8	.91
Telemetry (Ref. Group 10)	1,557	137	11.4	.985
TOTALS	29,373	2,041	14.4	



Notes: (1) "Partial": all parts do not lead to engine power failure due to redundancy.

(2) "Fault Effects Qualified": all parts failure do not cause an immediate power failure.

FIGURE 3.28. 30CM ION ENGINE POWER PROCESSOR RELIABILITY DIAGRAM

SOURCE CODES
1. TRW Current Handbook values (Draws from best source)
2. No Change
3. Composite

TABLE 3-XX

COMPONENT FAILURE RATES

Components	Failure Rate per 10^9 Hours	Source
Capacitors:		
Ceramic	1	1
Ceramic 1000V MICA	10	1
Polycarbonate	27	1
Polypropeline	27	1
Tantalum	22	1
Tantalum - Solid	9	1
Diodes:		
Signal	1.4	2
Power	26	1
Zener	15	1
Zener - Power	115	2
High Voltage	82	2
Integrated Circuits:		
Digital	25	
Linear	50.4	3
Magnetics:		
Inductors	1	2
Inductors - AC Voltage	7.7	2
Transformer Signal	1.3	2
Transformer - Med Power	10.8	2
Transformer - High Power	35	2
Transformer - High Power & High Voltage	65	2
Relays:		
Magnetic Latch (Less than 10,000 cycles)	5	2
Non-Latch (Less than 10,000 cycles)	60	2
Resistors:		
Carbon Composition	1	2
Metal Film	.1	1
Power Wire Wound	15	1
Potentiometer	1.4	2
High Voltage	18	2
SCR:		
Low Power	26	1
High Power	45	1
Transistors:		
Signal	3.6	2
Medium Power	7.2	2
High Power	30.0	3

TABLE XXI. SOURCES OF RELIABILITY FAILURE RATE DATA

1. "Reliability Data From In-Flight Spacecraft; 1958-1970", Planning Research Corporation, PRC R-1453, 30 November 1971.

2. "More Reliability Data From In-Flight Spacecraft; Planning Research Corporation, Index Serial No. - 1071, E. E. Bean and C. E. Bloomquist, October 1971.

3. "Addendum to Reliability Data From In-Flight Spacecraft; 1958-1970", PRC Systems Sciences Company, PRC D-1864, 30 November 1972.

4. "Minuteman Preferred Parts List (MPPL)", TRW Systems Group, 30 May 1973.

5. "Reliability Planning and Management", General Electric Company, Aerospace Electronics Systems Department, J. D. Selby and S. G. Miller, 26 September 1970.

6. "Demonstrated Orbital Reliability of TRW Spacecraft", TRW Systems Group, Reliability Assurance Department, Space Vehicles Division Product Assurance, D-00532, 72-2286-.257, December 1972.

7. "Electronic Parts Failure Rates Demonstrated By Spacecraft In Orbit" TRW Systems Group, Reliability Department,SVD, R.C. Billups, E.H. Barnett, and S.F. Bergen, December 1971

The failure rates used at present do not include growth projections except that in three cases the parts are already highly mature and low in failure rate.

Table 3-XXIIidentifies the failure rate of the different functional elements using the component failure rates given in Table 3-XX.

TABLE 3-XXII

Analysis of Power Processor Failure Rate
per Functional Elements

Function	Circuit Description	Failure Rate Part per 10^9 Hours
A. Power Processor	1) Output Power Circuitry A12, A14-A18, A45-A49, A51	4130
	2) Output Regulators A3-A5, A39-A44, A50	1101
	3) Beam Output A23, A29	1699
	4) Beam Inverter A24, A27, A28	2656
	5) Multiple Inverter A6, A8, A9	3571
	6) Auxiliary Output Power A1, A10	1482
	11) Ramp & TLM Oscillator A26	86
	12) Auxiliary Supply A11	494
	13) Command & Protection A20, A21, A52	3258
	Subtotal	18,477
B. Digital Interface Unit	7) D-A Converters A2, A22, A36	3344
	8) Decoder A19, A33	2220
	9) Telemetry Data Conditioning A34, A35, A37, A38	3775
	Subtotal	9,339
C. Telemetry	10) Telemetry Sense Circuitry A13, A32	1557
	Subtotal	1,557
	Total F.R.	29,373

4.0 30CM ION ENGINE POWER PROCESSOR THERMAL-VACUUM TEST

The 30CM Ion Engine Power Processor was installed in the thermal vacuum chamber and electrically operated to check the cable connections and instrumentation. The chamber door was then closed and the chamber brought to high vacuum. The cold wall was turned on and after the temperature had stabilized, the power processor was turned on. The load was the resistive load bank located external to the chamber. After initial problems were identified and resolved, a complete thermal-vacuum test was performed. The following functional tests were conducted:

- Start-up of the power processor at 0°F baseplate temperature
- Operation of the power processor until temperature stability was obtained and the thermocouple readings recorded to assure safe operating temperatures for all components.
- Shut-down and start-up of the power processor at high baseplate temperature.

4.1 Thermal Vacuum Test Facility

The thermal vacuum test of the power processor was conducted in a horizontal vacuum chamber, 6 ft in diameter by 8 ft in length. The breadboard was suspended from overhead rails by four wires, one at each corner. An LN_2 cooled cold plate was positioned directly underneath the breadboard to simulate radiation into deep space. Lamps were positioned above the breadboard to control the baseplate temperature during cool-down of the unit to 0°F.

Twenty thermocouples were mounted on the breadboard and four thermo couples were mounted on the chamber. The thermocouples were monitored on a strip chart recorder for a permanent record.

The load bank and control unit were placed alongside the vacuum chamber and connections to the breadboard made through feed-thru connectors on two access ports of the chamber.

Table 4-1 lists the thermocouple numbers and their locations.

TABLE 4-1 THERMAL VACUUM TEST
THERMOCOUPLE LOCATIONS

T.C. No.	Location
1	SCR1 Heat Sink (Beam)
2	SCR2 Ceramic (Multiple)
3	Beam Transformer
4	SCR2 Case (Beam)
5	V11 Output Rectifier
6	V5 Output Series Diode
7	SCR1 Bracket (Beam)
8	SCR2 Bracket (Beam)
9	Baseplate (End)
10	Baseplate (Center)
11	Baseplate (End)
12	A36 D-A Converter (Copper Strip on I.C.)
13	A37 A-D Converter (Copper Strip on I.C.)
14	A1 Aux. Reg. & Ramp Gen. (Frame)
15	V3 Output Transformer
16	Beam Suppression Resistor (50Ω)
17	SCR1 Heat Sink (Multiple)
18	Avc Transformer
19	SCR1 Case (Beam)
20	SCR1 Ceramic (Multiple)
21	Upper Shroud
22	Cold Plate - inlet } Chamber
23	Cold Plate - center } Chamber
24	Cold Plate - outlet } Chamber

4.2 Thermal Vacuum Test Results

The unit was turned ON after temperature stability of the baseplate of 0°F was obtained. The unit responded to all input commands. The output voltages were normal on all outputs. After ten minutes of operation, an inverter hang-up occurred which turned the system OFF. All the temperatures were reviewed to determine if any SCR's had overheated. The SCR temperatures were normal. Several additional attempts were made with similar results, i.e., the unit would operate for a few minutes and then an inverter would experience a hang-up.

In order to isolate the problem, the multiple inverter was run by itself. The hang-up problem remained. The chamber was brought to ambient conditions and sense leads were brought to the outside in order to be able to monitor the multiple inverter mainline SCR voltages and currents and SCR gate currents. After the chamber was evacuated, the multiple inverter was switched ON. It was observed that the lower main SCR turned on prematurely for no apparent reason after approximately ten minutes of operation. The lower main SCR was replaced and the test repeated with no problems encountered.

The SCR's used in the inverters are constructed with no bonding between the silicon chip and the heat sink or leads. The contacts on the chip is held by spring tension alone. The SCR package is pressurized with 40 psi of dry nitrogen which provides the heat conducting medium for the chip. A leak in the case of the device would result in minimal heat sinking capability of the chip under vacuum conditions and consequent overheating of the junctions. The junction would operate in room ambient environment but in a vacuum environment, it would overheat.

A complete operational test was carried out under high vacuum conditions and the detail test results are presented in Tables 4-II thru 4-V . After operating for a few hours, V11 output transformer temperature did not stabilize but kept on increasing. All other temperatures stabilized and were within safe operating regions. The test was continued for a few more hours to observe the V11 output transformer temperature. The test terminated when the V11 transformer reached 350°F. Post thermal vacuum test inspection

revealed that the V11 output transformer bond between the transformer and heat sink had parted leaving the transformer with very little heat dissipation capability which resulted in an excessive temperature rise. The transformer was replaced with a new unit and the bonding changed. No further problems were encountered.

TABLE 4-11 30CM POWER PROCESSOR ELECTRICAL PERFORMANCE
THERMAL VACUUM TEST
COLD START; BASEPLATE<-10°C (2°F)

Function	Voltage Volts	Current Amps	Power Watts	T.C. No.	Temp. °F	T.C. No.	Temp. °F
Vin	320.7	10.65	3415.94				
V1	8.019	1.181	9.47	1	-11	13	24
V2	3.751	1.138	4.27	2	- 9	14	29
V3	9.481	4.283	40.61	3	31	15	41
V4	8.565	2.176	18.64	4	- 6	16	17
V5	8.493	4.273	36.29	5	11	17	-10
V6	3.512	1.156	4.06	6	15	18	9
V7	11.89	1.998	23.76	7	- 4	19	- 7
V8	10.80	0.733	7.92	8	- 6	20	- 3
V9	39.93	12.56	501.52	9	0	21	34
V10	-489.6	10.12 ma	4.95	10	1	22	-290
V11	1099.9	1.987	2185.50	11	0	23	-290
V12	0.509	2.00	1.02	12	21	24	-295

TABLE 4-III 30CM POWER PROCESSOR ELECTRICAL PERFORMANCE THERMAL VACUUM TEST 210V OPERATION

Function	Voltage Volts	Current Amps	Power Watts	T.C. No.	Temp. °F	T.C. No.	Temp. °F
Vin	210.0	17.05	3580.16				
V1	8.019	1.180	9.46	1	115	13	97
V2	3.757	1.139	4.28	2	137	14	58
V3	9.708	4.384	42.56	3	206	15	197
V4	8.280	2.093	17.33	4	160	16	178
V5	8.630	4.334	37.40	5	179	17	87
V6	3.483	1.145	3.99	6	150	18	106
V7	11.87	1.994	23.67	7	146	19	168
V8	10.49	0.733	7.69	8	147	20	110
V9	40.14	12.60	505.76	9	93	21	30
V10	-506.9	10.47 ma	5.31	10	110	22	-290
V11	1101.9	1.986	2188.37	11	95	23	-290
V12	0.627	2.00	1.25	12	99	24	-290

TABLE 4-IV 30CM POWER PROCESSOR ELECTRICAL PERFORMANCE THERMAL VACUUM TEST 315V OPERATION

Function	Voltage Volts	Current Amps	Power Watts	T.C. No.	Temp. °F	T.C. No.	Temp. °F
Vin	315.0	10.85	3418.67				
V1	7.960	1.171	9.32	1	116	13	103
V2	3.759	1.139	4.28	2	114	14	65
V3	9.516	4.304	40.96	3	219	15	194
V4	8.233	2.095	17.25	4	156	16	176
V5	7.822	3.932	30.76	5	180	17	104
V6	3.476	1.143	3.97	6	152	18	110
V7	11.83	1.988	23.52	7	138	19	155
V8	10.44	0.732	7.64	8	144	20	123
V9	39.71	12.46	494.79	9	99	21	40
V10	-506	10.47 ma	5.30	10	116	22	-285
V11	1100.4	1.984	2183.19	11	99	23	-278
V12	0.526	2.00	1.05	12	100	24	-280

TABLE 4-V 30CM POWER PROCESSOR ELECTRICAL PERFORMANCE
THERMAL VACUUM TEST
390V OPERATION

Function	Voltage Volts	Current Amps	Power Watts	T.C. No.	Temp. °F	T.C. No.	Temp. °F
Vin	390.1	8.817	3439.66				
V1	8.013	1.179	9.45	1	111	13	100
V2	3.756	1.138	4.27	2	116	14	62
V3	9.463	4.283	40.53	3	212	15	199
V4	8.223	2.090	17.19	4	152	16	174
V5	8.207	4.124	33.84	5	177	17	106
V6	3.473	1.142	3.97	6	152	18	110
V7	11.72	1.969	23.08	7	133	19	149
V8	10.35	0.726	7.51	8	140	20	126
V9	39.76	12.49	496.60	9	94	21	33
V10	-508	10.5 ma	5.33	10	114	22	-290
V11	1101.3	1.984	2184.98	11	100	23	-290
V12	0.497	2.00	0.99	12	100	24	-293

5.0 30CM ION ENGINE POWER PROCESSOR INTEGRATION TEST

The 30CM hollow cathode ion engine was installed in the test facility and operated with laboratory power supplies to determine engine operating parameters. The power processor was then integrated with the ion engine. After minor problems were identified and resolved, the ion engine was operated with the power processor for over 100 hours with numerous cold engine startups. The following functional operations were demonstrated:

1. Neutralizer keeper ignition
2. Neutralizer keeper voltage regulation
3. Cathode keeper ignition
4. Discharge ignition
5. Discharge voltage-cathode vaporizer control loop
6. High voltage application to accelerator and screen
7. Beam current regulation from 0.6 to 2.0A
8. Recovery from internal engine arcs
9. Shutdown of ion engine.

5.1 Ion Engine Test Facility

Ion engine performance test were conducted in a vertical vacuum chamber which has been specifically instrumented for performing life and performance testing on complete ion engine propulsion systems. The engine is mounted at the top of the chamber and exhausted vertically downward. Provisions are made to operate the collector and shrouds at ground potential or floating at the beam exhaust potential.

The ion engine test facility instrument console is shown in Figure 5.1. It has the the following functional units:

1. Top, panel meters for all currents and voltages to the ion engine.
2. Center section-left side panel, AC power control vacuum tank controls, facility monitoring and emergency shutdown if failure occurs in the faility equipment.
3. Center section-center panel, low voltage supply operating at ground potential and low voltage instrumentation.

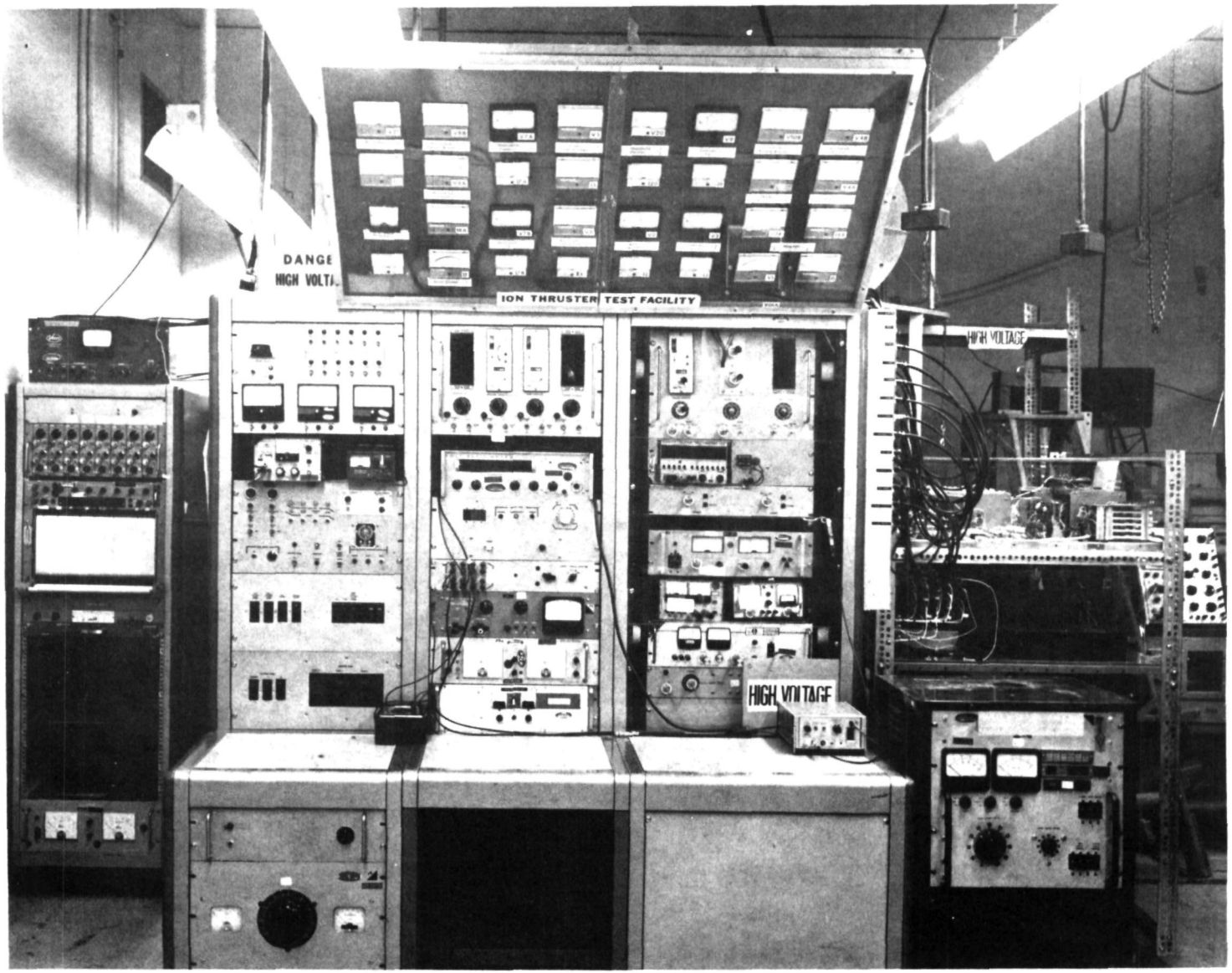


FIGURE 5-1. ION ENGINE TEST FACILITY CONSOLE

4. Center section-right side panel, all power supplies floating at screen potential and high voltage instrumentation. This equipment is shielded by a plexiglas front panel for personnel safety.
5. Bottom section-left side, accelerator power supply.
6. Bottom section-right side, screen power supply.

The ion engine/power supply wiring diagram for the test facility is shown in Figure 5.2

5.2 Power Processor Test Fixture

A special test fixture, shown in Figure 5.3 was fabricated to facilitate the testing of the power processor. The test fixture was constructed to provide safety for the test personnel, to position the power processor in the engine test facility and to monitor the performance of the power processor.

The test fixture is covered by plexiglas on all sides to provide high voltage isolation. The power processor is located in the top section. Output power connectors are located on the left side. The bottom section of the test fixture includes all the output and input instrumentation. The DVM on the left side monitors all potentials floating at the screen supply output and the DVM on the right monitors all potentials referenced to ground. The command and reference generator is mounted below the DVM on the right. It provides all the operating commands and reference voltage levels for the power processor.

5.3 Ion Engine Integration Test Results

The 30CM hollow cathode ion thruster was operated initially using test facility power supplies in order to check out the ion thruster and the test facility. Several modifications to the facilities were required such as moving the facility current meters from the return leg of each supply to the "positive" lead because some of the output returns were common internal to the power processor causing erroneous meter readings. In addition, the facility supply furnishing the 200-400V power to the power processor was improperly grounded with resulting high transient voltages appearing on the control ground line.

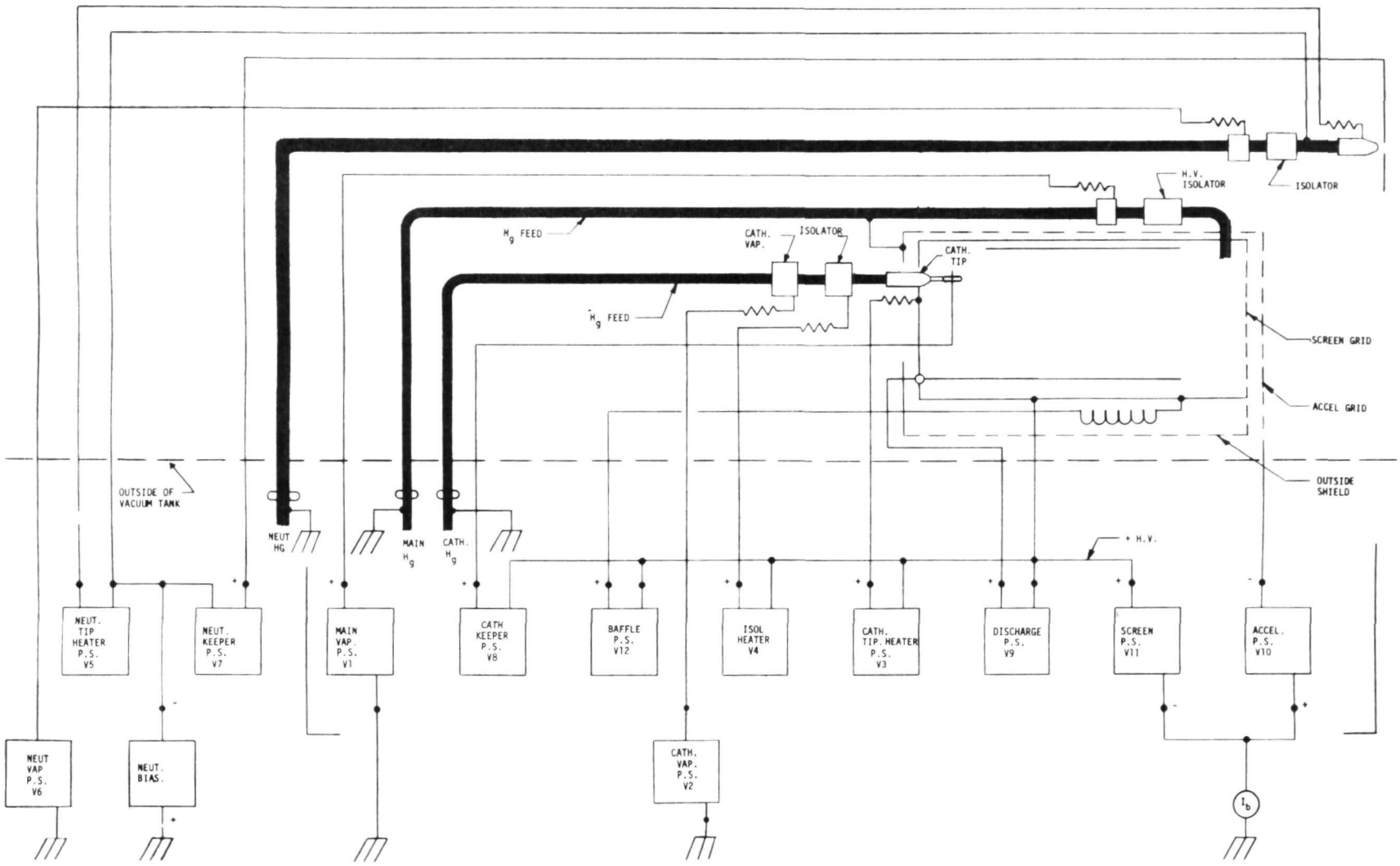


FIGURE 5.2. ION ENGINE BLOCK DIAGRAM

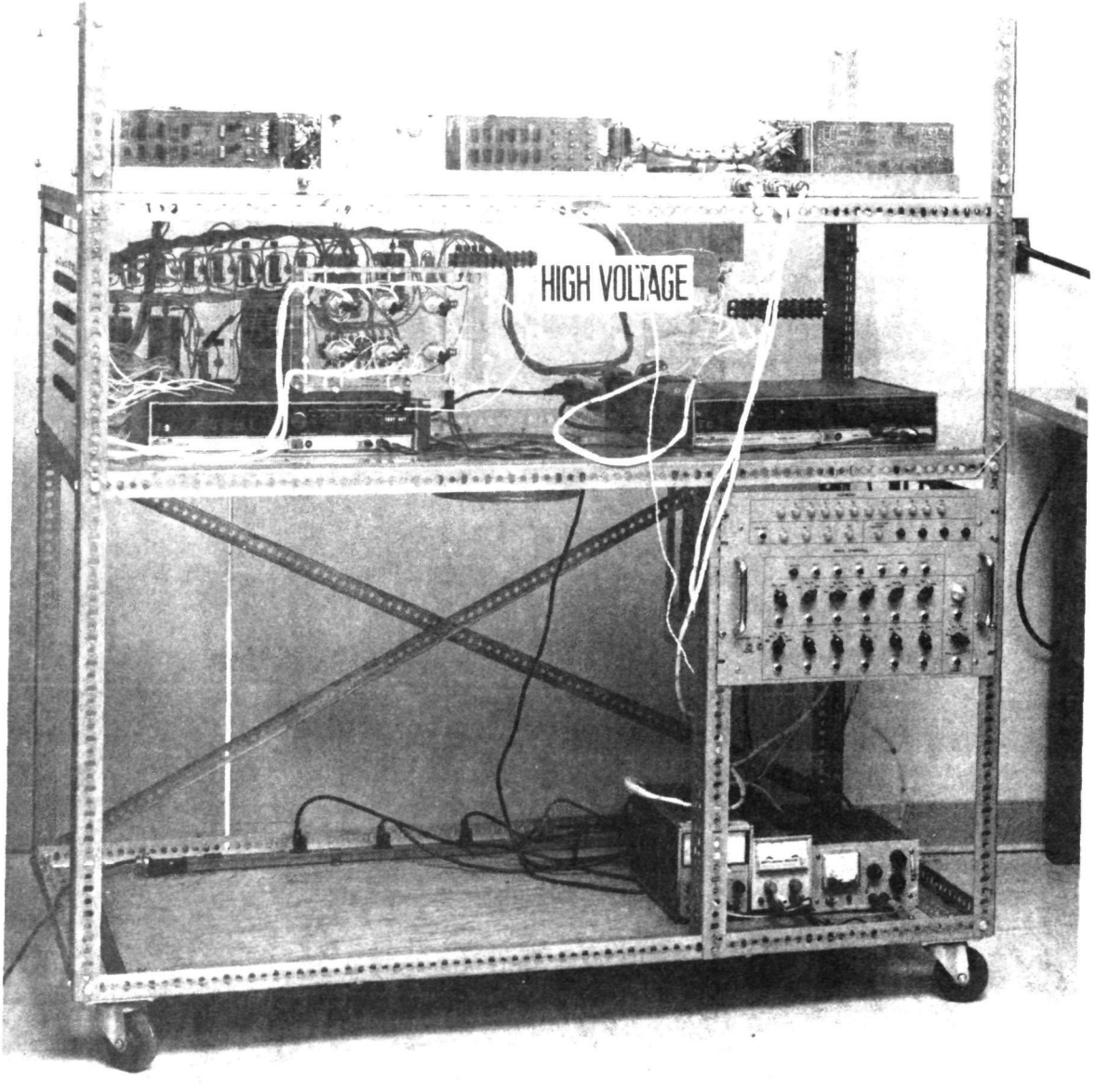


FIGURE 5-3. POWER PROCESSOR TEST FIXTURE

Once the facility problems were eliminated the integration of the power processor proceded with only one problem area identified. This problem was the inability to maintain proper operation above approximately 1.6A beam current. After numerous attempts at corrective action it was found that the output voltage specified for the Discharge Supply (V9) was too low. Once the output voltage of the Discharge Supply was raised the problem no longer existed.

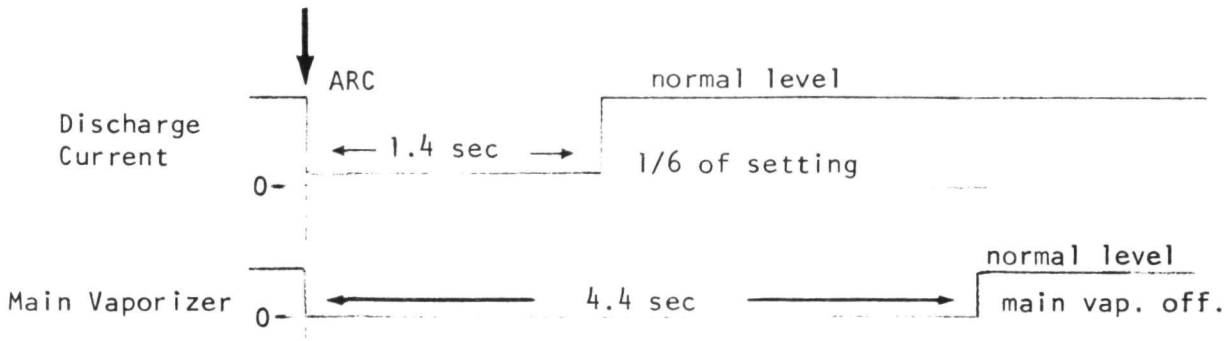
The power processor and the ion thruster were run together for over one hundred (100) hours under all operating conditions - start, shutdown, arcing, steady-state at voltage and beam current extremes - with no operational problems.

The recycle procedure following an arcing condition between points of high potential difference within the thruster was thoroughly investigated. The evolved procedure is a simplified sequence compared to those procedures generally advocated by other investigators. The following recycle sequence provided the optimum restart:

A. For arc duration less than 100ms.

1.) Discharge current cutback to 1/6 of normal setting for 1.4 seconds.

2.) Main vaporizer off for 4.4 seconds.

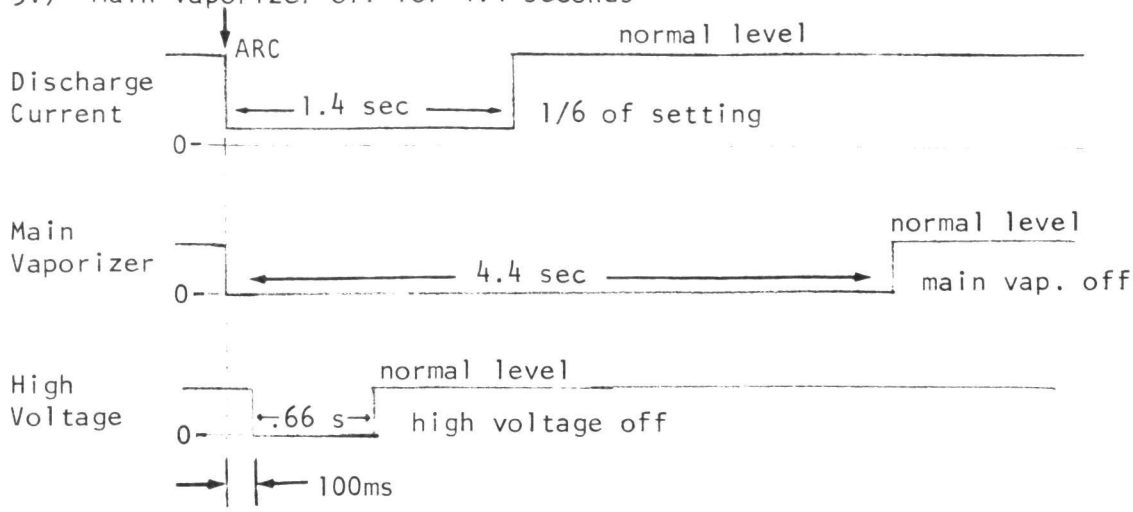


B. For arc duration longer than 100ms.

1.) High voltage (screen and accelerator) off for 0.66 sec.

2.) Discharge current cutback to 1/6 of normal setting for 1.4 sec.

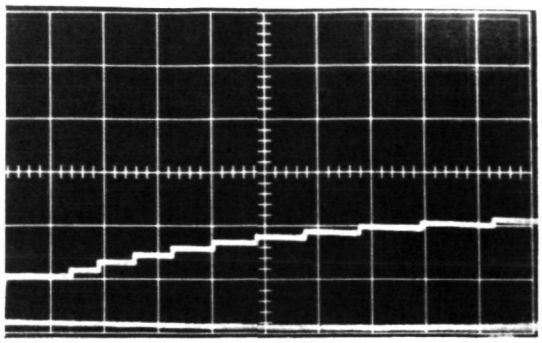
3.) Main vaporizer off for 4.4 seconds



The control loops for the neutralizer vaporizer-neutralizer keeper voltage, the cathode vaporizer-discharge voltage, and the main vaporizer-beam current were optimized for the most stable engine operation.

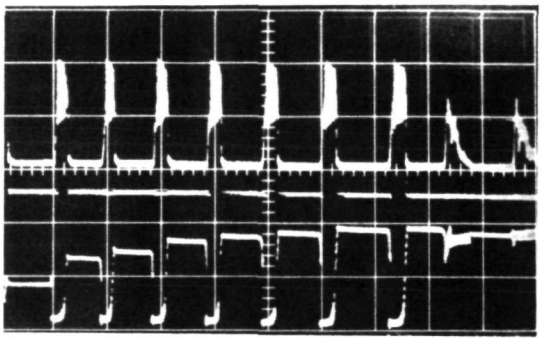
An oscilloscope photograph of the screen supply startup voltage into a high impedance load is shown in Figure 5.4. The voltage is controlled with no spikes or overshoots. Figure 5.5 shows the screen supply startup into an arcing ion engine load. During the arcing period, no high current or voltage transients were present. Figures 5.6 and 5.7 show the interaction between the screen and accelerator currents during the startup interval.

The high frequency noise on the power processor and ion engine was investigated to identify any problem areas. Figure 5.8 shows the ripple on the input and output lines of the power processor when operating into a resistive load bank. The outputs were all operating at maximum levels. Figure 5.9 shows the ripple on the input and output lines of the power processor when operating the ion engine at a beam current of 1.5A. Figures 5.10 through 5.13 show ripple currents for input current, beam current and discharge current for beam currents of 0.768A, 1.01A, 1.505A and 2.04A.



Screen Voltage
V = 500v/div
T = 10ms/div

Figure 5-4. SCREEN VOLTAGE DURING TURN ON - STARTUP INTO NO LOAD

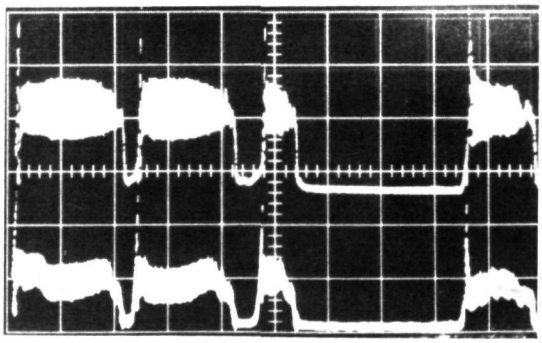


Screen Current
I = 2A/div

T = 10ms/div

Screen Voltage
V = 500v/div

Figure 5-5. SCREEN CURRENT AND VOLTAGE DURING TURN ON -STARTUP INTO ARCING LOAD

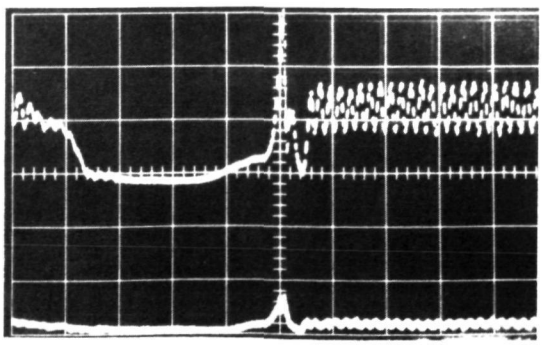


Screen Current
I = 2A/div

T = 2ms/div

Accel Current
I = 200ma/div

Figure 5-6. SCREEN AND ACCELERATOR CURRENT DURING TURN ON



Screen Current
I = 2A/div

T = 0.2ms/div

Accel Current
I = 1A/div

Figure 5-7. SCREEN AND ACCELERATOR CURRENT DURING TURN ON

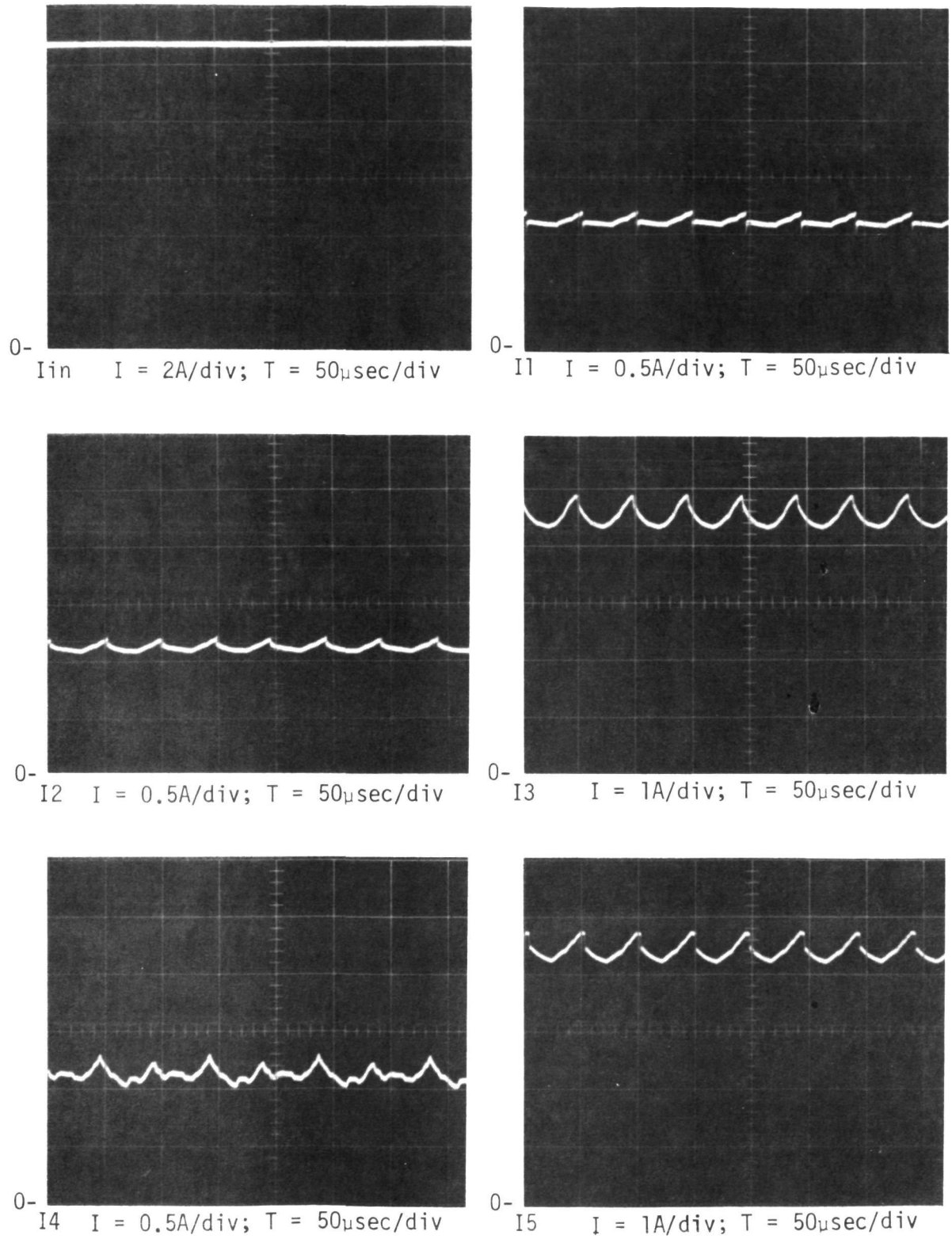


FIGURE 5.8. POWER PROCESSOR CURRENT WAVEFORMS (WITH LOADBANK)
Page 1 of 2

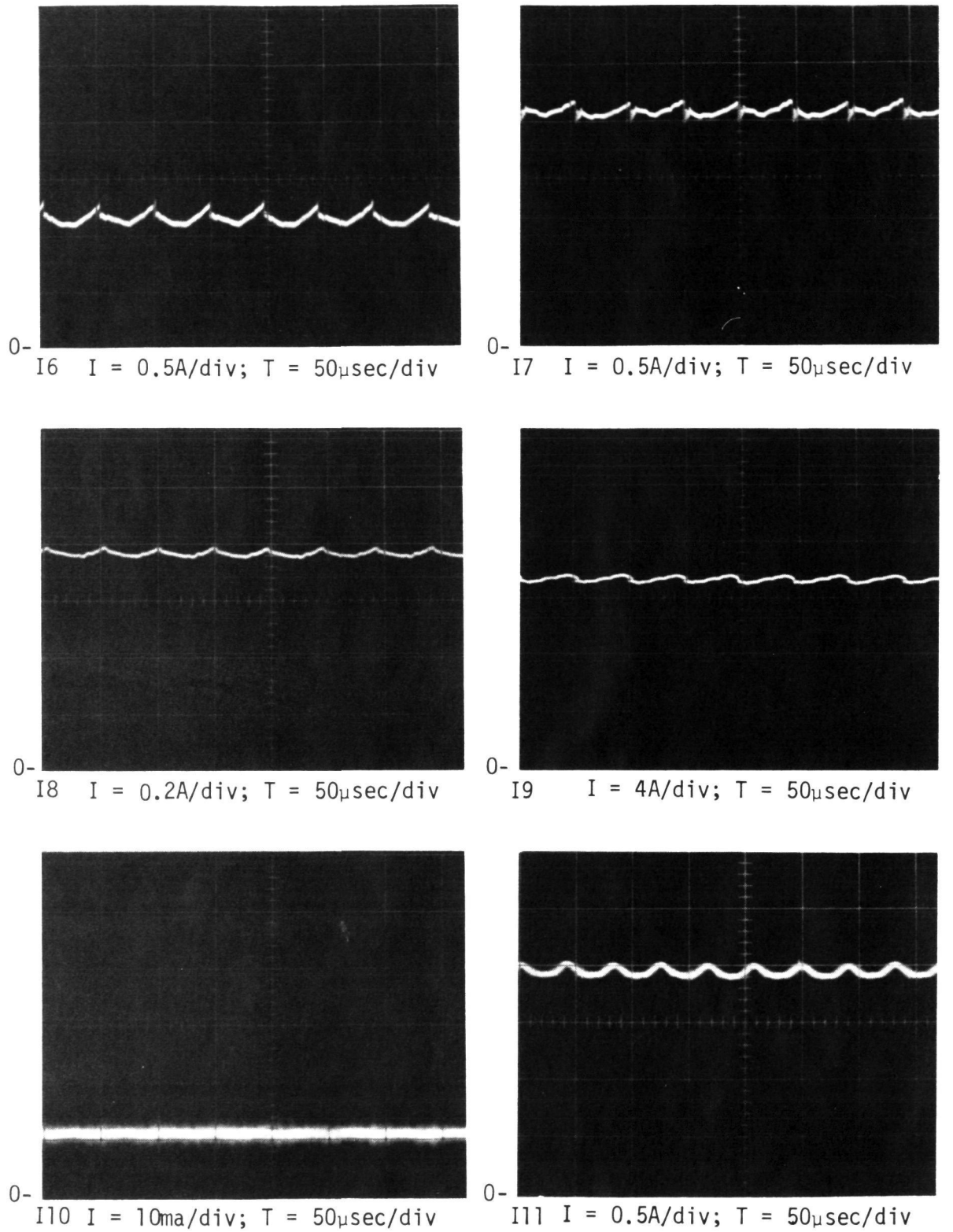


FIGURE 5.8. POWER PROCESSOR CURRENT WAVEFORMS (WITH LOADBANK)
Page 2 of 2

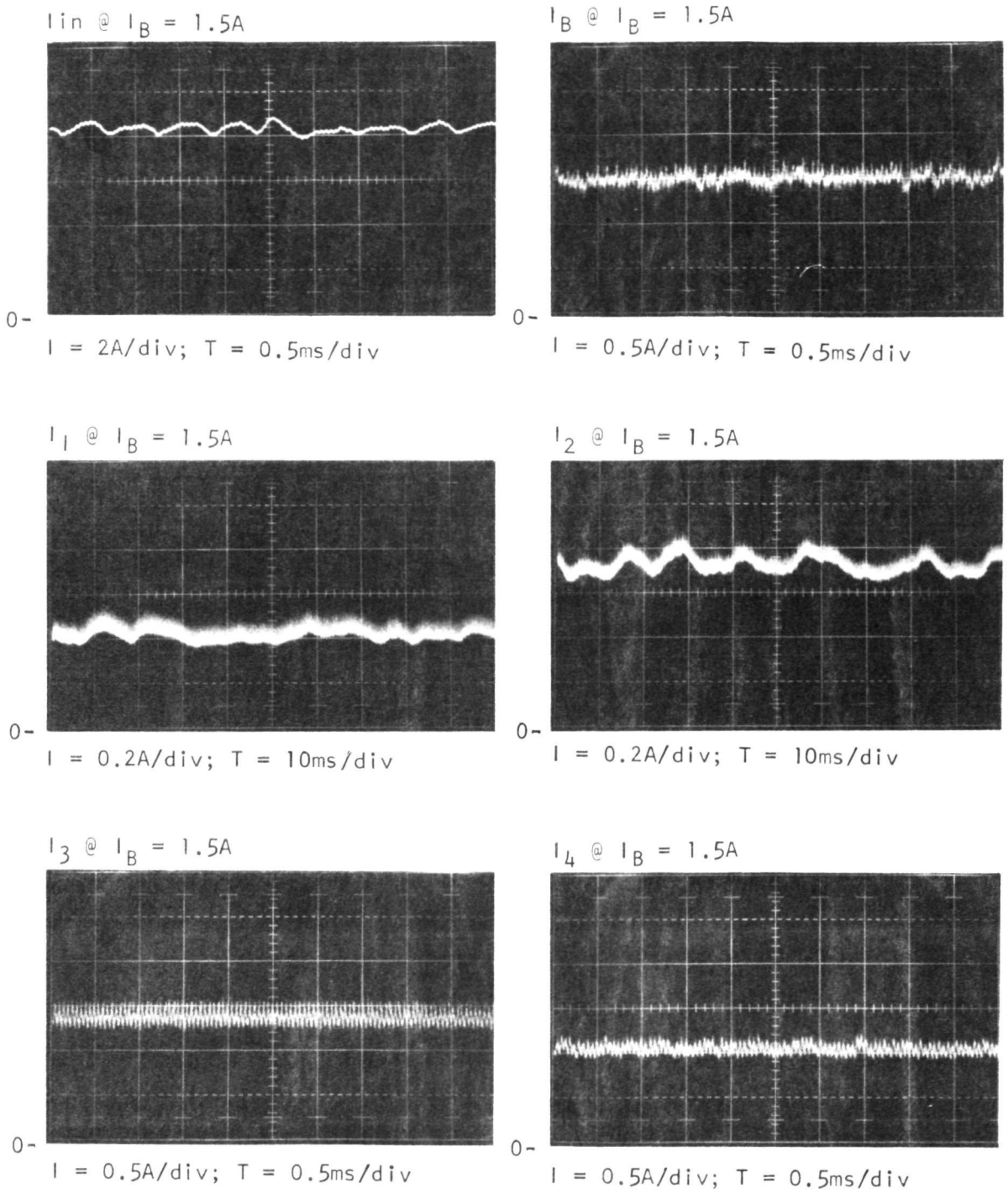


FIGURE 5.9. POWER PROCESSOR CURRENT WAVEFORMS (WITH ENGINE)
Page 1 of 2

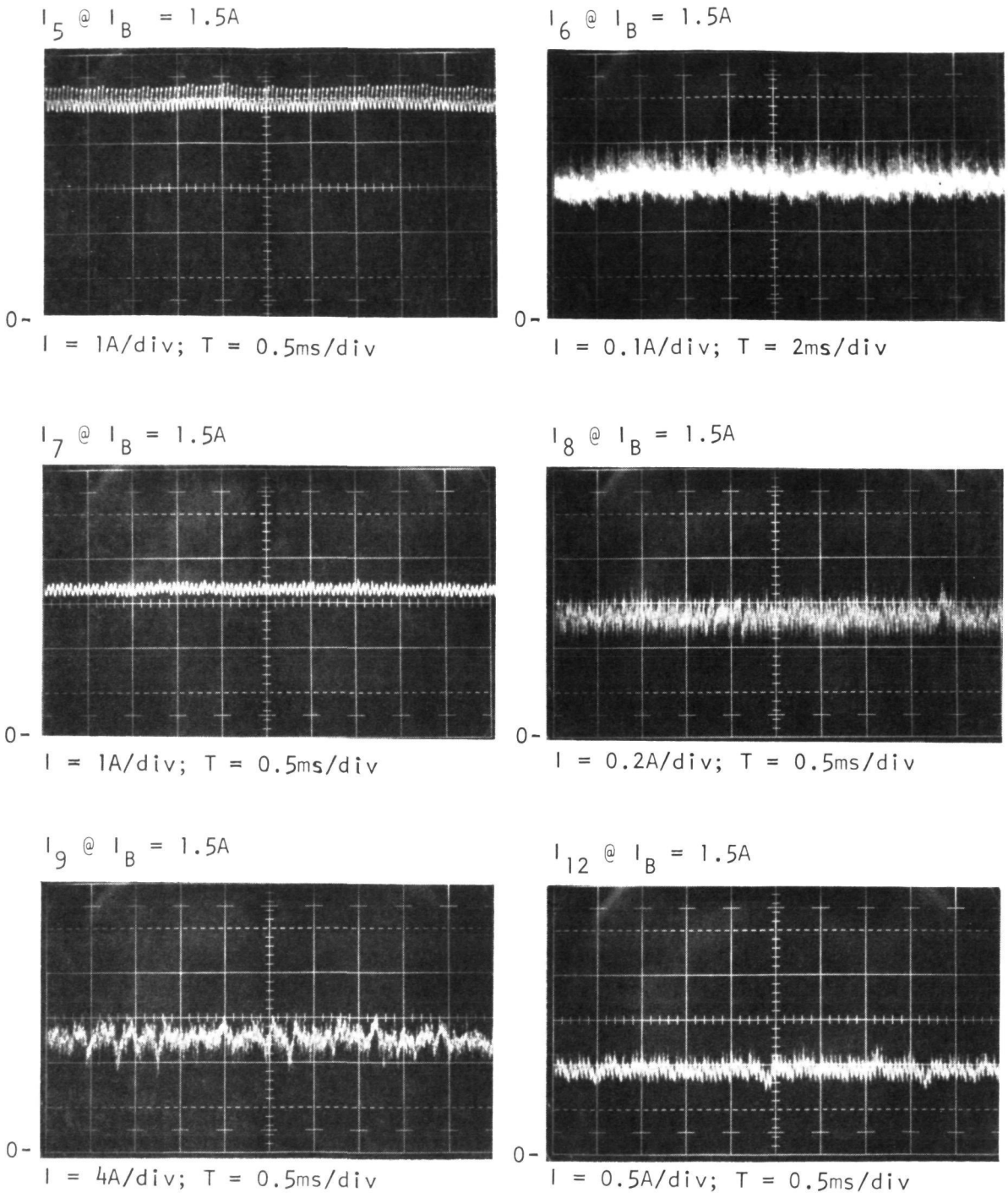


FIGURE 5.9. POWER PROCESSOR CURRENT WAVEFORMS (WITH ENGINE)
Page 2 of 2

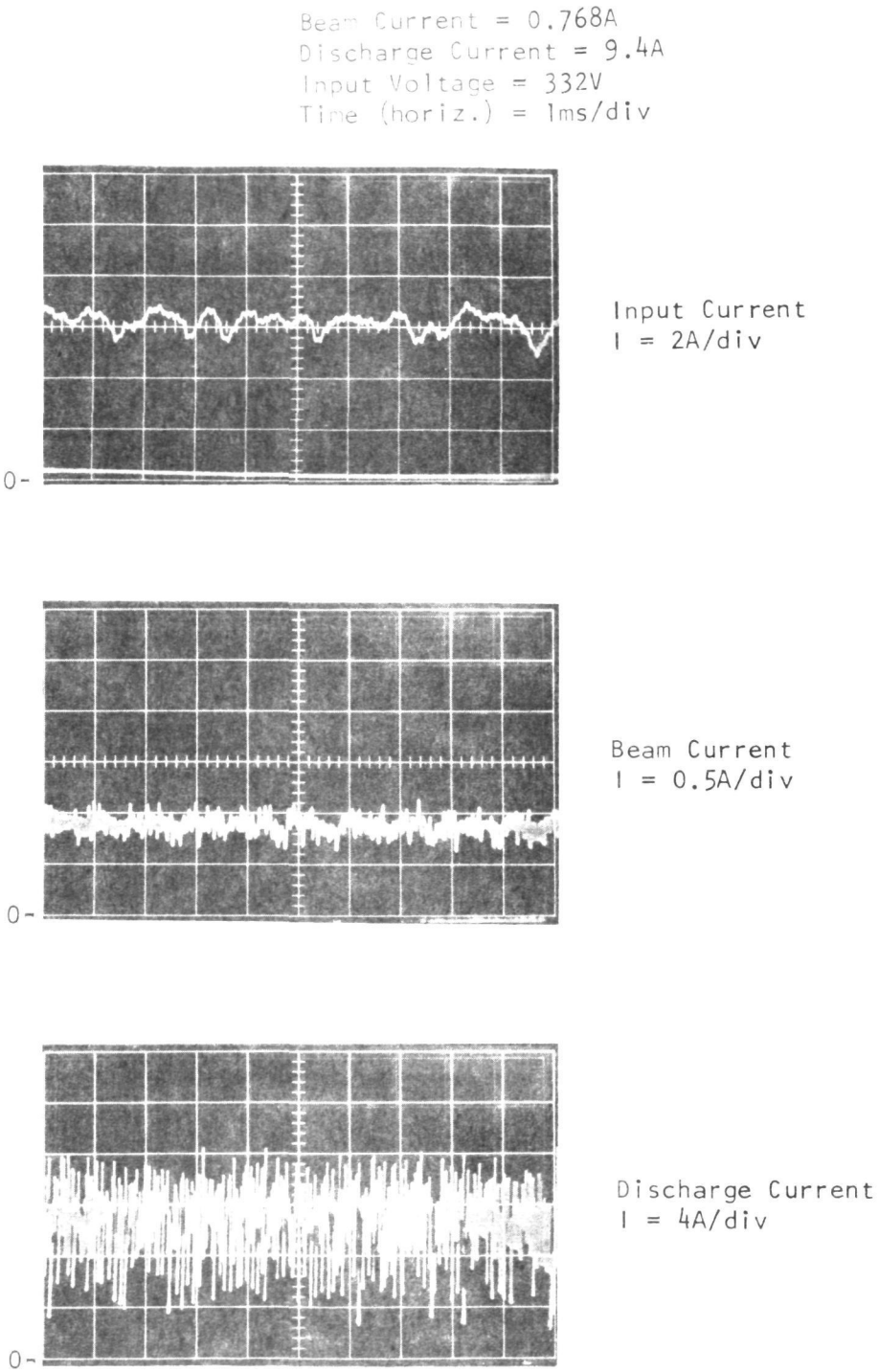


FIGURE 5.10. POWER PROCESSOR CURRENT WAVEFORMS (WITH ENGINE); I_B=0.768A

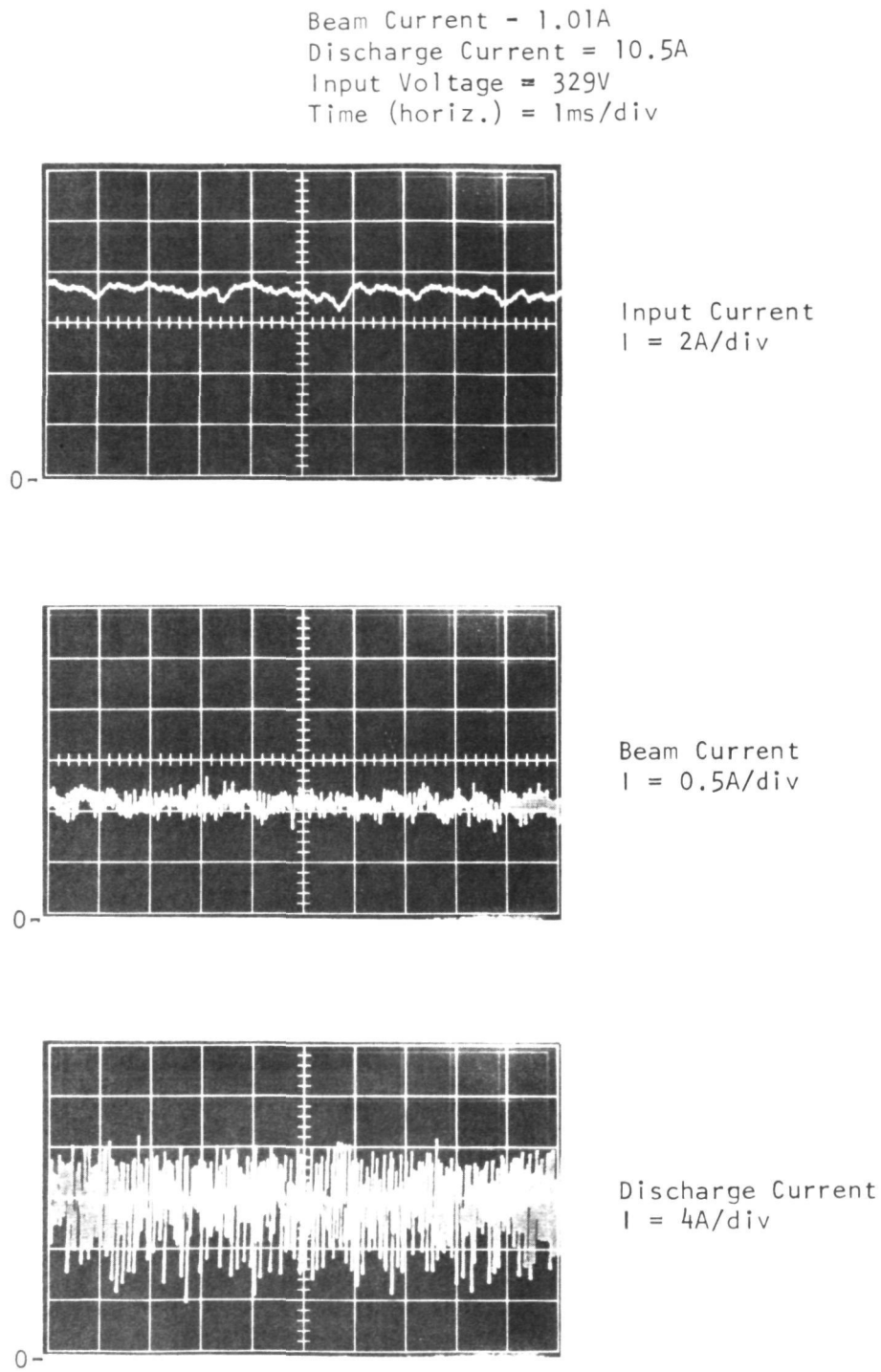
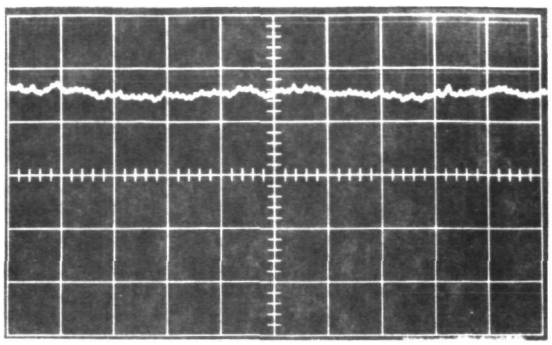
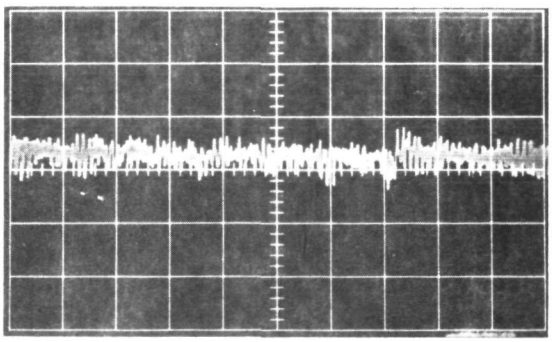


FIGURE 5.11. POWER PROCESSOR CURRENT WAVEFORMS (WITH ENGINE); I_B=1.01A

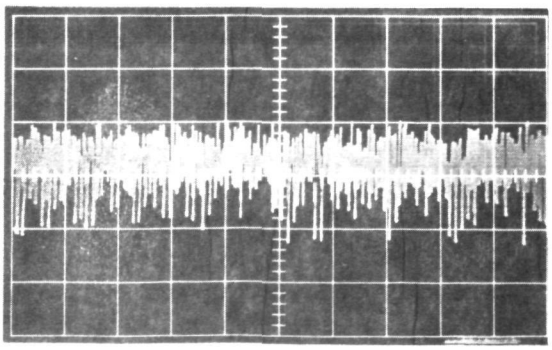
Beam Current = 1.505A
Discharge Current = 12.5A
Input Voltage = 325V
Time (horiz.) = 1ms/div



Input Current
I = 2A/div



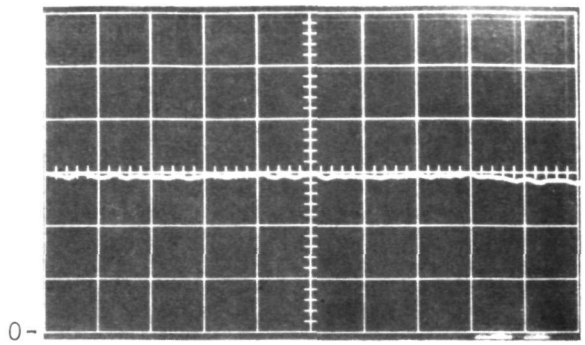
Beam Current
I = 0.5A/div



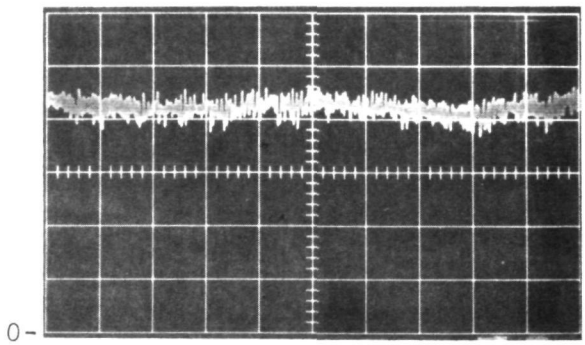
Discharge Current
I = 4A/div

FIGURE 5.12. POWER PROCESSOR CURRENT WAVEFORMS (WITH ENGINE); I_B=1.505A

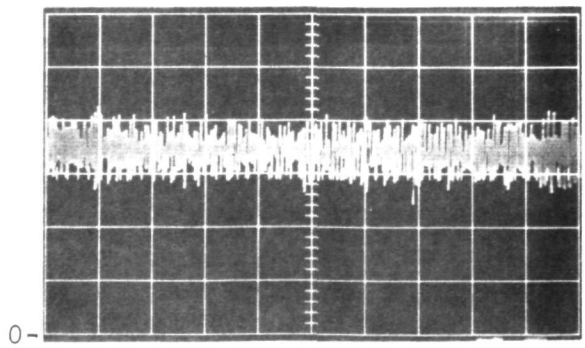
Beam Current = 2.04A
Discharge Current - 14.3A
Input Voltage = 316V
Time (horiz.) = 1ms/div



Input Current
I = 4A/div



Beam Current
I = 0.5A/div



Discharge Current
I = 4A/div

FIGURE 5.13. POWER PROCESSOR CURRENT WAVEFORMS (WITH ENGINE); I_B=2.04A

Tables 5-I through 5-III show typical power processor characteristics when operating an ion engine at a beam current of 0.68A which was the lowest current attainable with this particular ion engine. Tables 5-IV thru 5-VI show typical power processor characteristics at a beam current of 2A.

The very satisfactory performance of the power processor-ion thruster combination during the integration tests emphasizes the importance of integration testing. Only by running an ion thruster could the dynamic characteristics associated with the improperly defined Discharge Supply output voltage, the simplification of the recycle sequence, and the optimization of the three control loops have been identified.

TABLE 5-I 30CM POWER PROCESSOR ELECTRICAL PERFORMANCE
ENGINE INTEGRATION TEST
0.68 AMP BEAM CURRENT
200 V INPUT

FUNCTION	VOLTAGE VOLTS	CURRENT AMPS	POWER WATTS
Vin	201.1	8.065	1621.90
V1	6.5	0.93	6.04
V2	6.37	2.19	13.95
V3	--	--	--
V4	--	--	--
V5	--	--	--
V6	3.64	1.22	4.44
V7	13.00	1.87	24.31
V8	8.18	0.74	6.05
V9	42.1	7.50	315.75
V10	-502	2.05 ma	1.03
V11	1101	0.683	751.98
V12	1.64	4.6	7.54
		OUTPUT POWER	1131.09
		EFFICIENCY	69.74%

TABLE 5-11 30CM POWER PROCESSOR ELECTRICAL PERFORMANCE
ENGINE INTEGRATION TEST
0.68 AMP BEAM CURRENT
300 V INPUT

FUNCTION	VOLTAGE VOLTS	CURRENT AMPS	POWER WATTS
Vin	302.2	5.11	1545.30
V1	6.50	0.93	6.04
V2	6.04	2.07	12.50
V3	--	--	--
V4	--	--	--
V5	--	--	--
V6	3.31	1.14	3.77
V7	13.5	1.88	25.38
V8	8.13	0.736	5.98
V9	42.1	7.60	319.96
V10	-500	1.91 ma	0.95
V11	1100	0.683	751.3
V12	1.70	4.6	7.82
		OUTPUT POWER	1133.70
		EFFICIENCY	73.36%

TABLE 5-III 30CM POWER PROCESSOR ELECTRICAL PERFORMANCE
ENGINE INTEGRATION TEST
0.68 AMP BEAM CURRENT
375 V INPUT

FUNCTION	VOLTAGE VOLTS	CURRENT AMPS	POWER WATTS
Vin	375.4	4.146	1556.44
V1	6.60	0.94	6.20
V2	5.95	2.04	12.14
V3	--	--	--
V4	--	--	--
V5	--	--	--
V6	3.32	1.11	3.68
V7	13.7	1.87	25.62
V8	8.11	0.723	5.86
V9	42.1	7.60	319.96
V10	-500	1.93 ma	0.96
V11	1100	0.683	751.3
V12	1.66	4.6	7.64
		OUTPUT POWER	1133.36
		EFFICIENCY	72.82%

TABLE 5-IV 30CM POWER PROCESSOR ELECTRICAL PERFORMANCE
ENGINE INTEGRATION TEST
2 AMP BEAM CURRENT
200 V INPUT

FUNCTION	VOLTAGE VOLTS	CURRENT AMPS	POWER WATTS
Vin	201.7	17.147	3458.57
V1	8.20	1.20	9.84
V2	4.18	1.42	5.93
V3	--	--	--
V4	--	--	--
V5	--	--	--
V6	3.20	1.07	3.42
V7	13.1	1.86	24.37
V8	6.67	0.733	4.89
V9	37.6	14.5	595.2
V10	-503	9.5 ma	4.78
V11	1100	2.02	2222.00
V12	2.03	4.4	8.93
		OUTPUT POWER	2829.36
		EFFICIENCY	81.82%

TABLE 5-V 30CM POWER PROCESSOR ELECTRICAL PERFORMANCE
ENGINE INTEGRATION TEST
2 AMP BEAM CURRENT
300 V INPUT

FUNCTION	VOLTAGE VOLTS	CURRENT AMPS	POWER WATTS
Vin	301.4	11.263	3394.84
V1	7.80	1.17	9.13
V2	4.15	1.37	5.68
V3	--	--	--
V4	--	--	--
V5	--	--	--
V6	3.04	1.04	3.16
V7	13.7	1.84	25.21
V8	6.52	0.731	4.77
V9	39.6	14.4	570.24
V10	-500	9.02 ma	4.51
V11	1099.5	2.03	2231.98
V12	2.01	4.5	9.04
		OUTPUT POWER	2863.72
		EFFICIENCY	84.35%

TABLE 5-VI 30CM POWER PROCESSOR ELECTRICAL PERFORMANCE
ENGINE INTEGRATION TEST
2 AMP BEAM CURRENT
375 V INPUT

FUNCTION	VOLTAGE VOLTS	CURRENT AMPS	POWER WATTS
Vin	376.2	9.057	3407.34
V1	6.60	1.04	6.86
V2	3.40	1.30	4.42
V3	--	--	--
V4	--	--	--
V5	--	--	--
V6	2.82	1.01	2.85
V7	13.9	1.87	25.99
V8	6.42	0.719	4.61
V9	40.2	14.5	582.9
V10	-500	9.16 ma	4.58
V11	1099.5	2.02	2220.99
V12	1.95	4.5	8.77
		OUTPUT POWER	2861.97
		EFFICIENCY	83.99%

6.0 30CM ION ENGINE POWER PROCESSOR EMI TESTS

Electromagnetic interference tests were performed on the 30cm power processor thermal vacuum breadboard so that some baseline information would be available for the spacecraft system engineers to perform interaction studies for the spacecraft and for the scientific experiments.

There was no extensive effort to design into the power processor the capability to meet the full specification of MIL-STD 461, Electromagnetic Interference Characteristics Requirements for Equipment. Good engineering practices were used in the design of the input power filter and the application of EMI feedthrough filters.

Two basic tests were performed and summary data are presented of the results:

(1) Radiated narrowband and broadband of the power processor operating with load bank simulation.

(2) Conducted narrowband and broadband interference with the power processor and ion engine operating near the full power conditions.

Figure 6-1 illustrates the schematic of the test setup used during the conducted emission tests. In the radiation test, the cabling between the power processor and load bank simulator was about 10 feet, while the remainder of the setup was as illustrated in Figure 6-1.

Figure 6-2 shows the narrowband radiated test data for the power processor operating at nominal full power load condition per the specifications contained in Appendix A into a load bank simulator. The low frequency data points are due to the switching

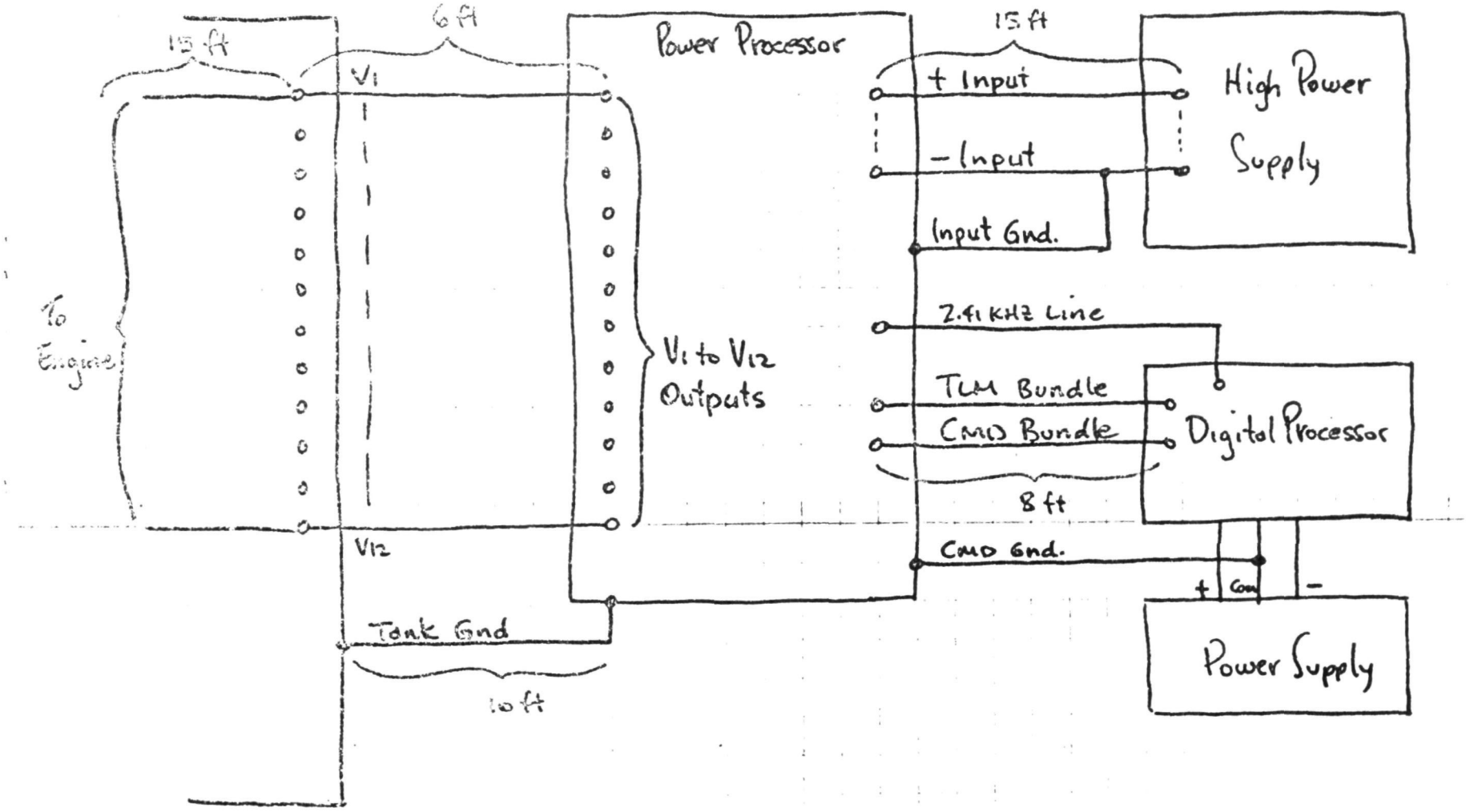


Figure 6.1. Schematic of Power Processor Test Setup During Conducted Interference Tests

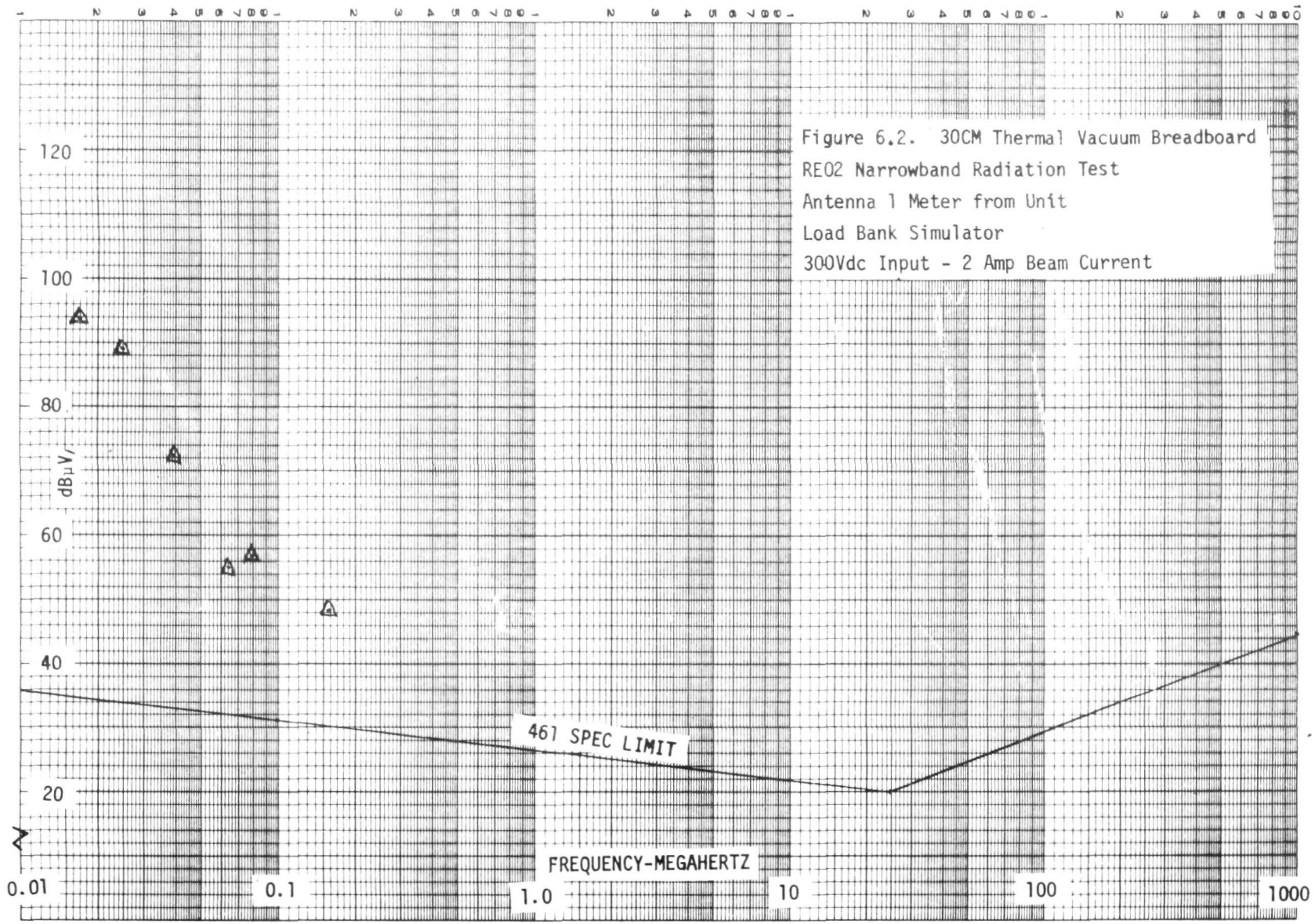


Figure 6.2. 30CM Thermal Vacuum Breadboard
RE02 Narrowband Radiation Test
Antenna 1 Meter from Unit
Load Bank Simulator
300Vdc Input - 2 Amp Beam Current

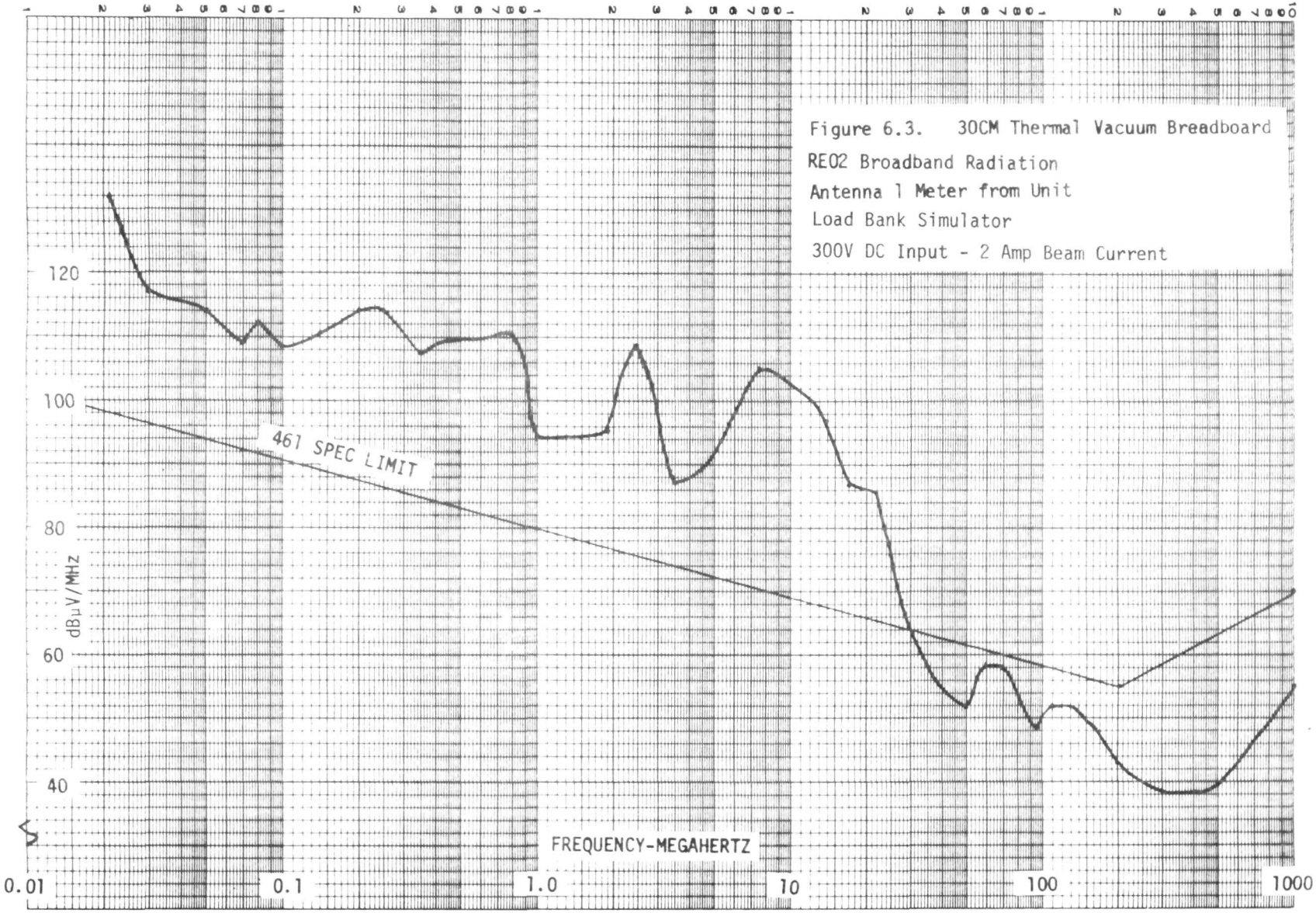


Figure 6.3. 30CM Thermal Vacuum Breadboard
RE02 Broadband Radiation
Antenna 1 Meter from Unit
Load Bank Simulator
300V DC Input - 2 Amp Beam Current

frequency of the screen inverter and its harmonics. Figure 6.3 shows the test data for the broadband radiation emission test and includes some of the effects due to 2.41KHz oscillator and measurement equipment in the power processor test stand.

Radiation emission tests were not taken with power processor/ ion engine combinations due to the high ambient noise level in the ion engine test facility from the vacuum pumps and solenoid operation. A special test facility must be developed in order to take meaningful radiation test data.

Selected test data is presented for the narrowband conducted emission test and includes the following lines:

- DC input power, Figure 6-4.
- Command Cable Bundle, Figure 6-5.
- Discharge Output (1/9), Figure 6-6.
- Screen Output (VII), Figure 6-7.

This data includes both the power processor and 30cm ion engine operating together. Both MIL-STD 461, Notice 1, and Notice 3 specification limits are shown in Figures 6-4 through 6-7, and the test data shows that Notice 3 specification is met in most cases.

Output ripple photographs of the associated lines are presented in Figure 5-8 for the operation into a resistive load bank simulator and Figure 5-9 for the operation of the power processor and 30cm ion engine. Comparison of this data shows the penalty the 30cm ion engine presents on the power processor and the reflected ripple into the power source. Continued development work is in progress on the 30cm ion engine to reduce this noise level basically being generated by the discharge chamber.

The broadband conducted emission data is present in the following figures:

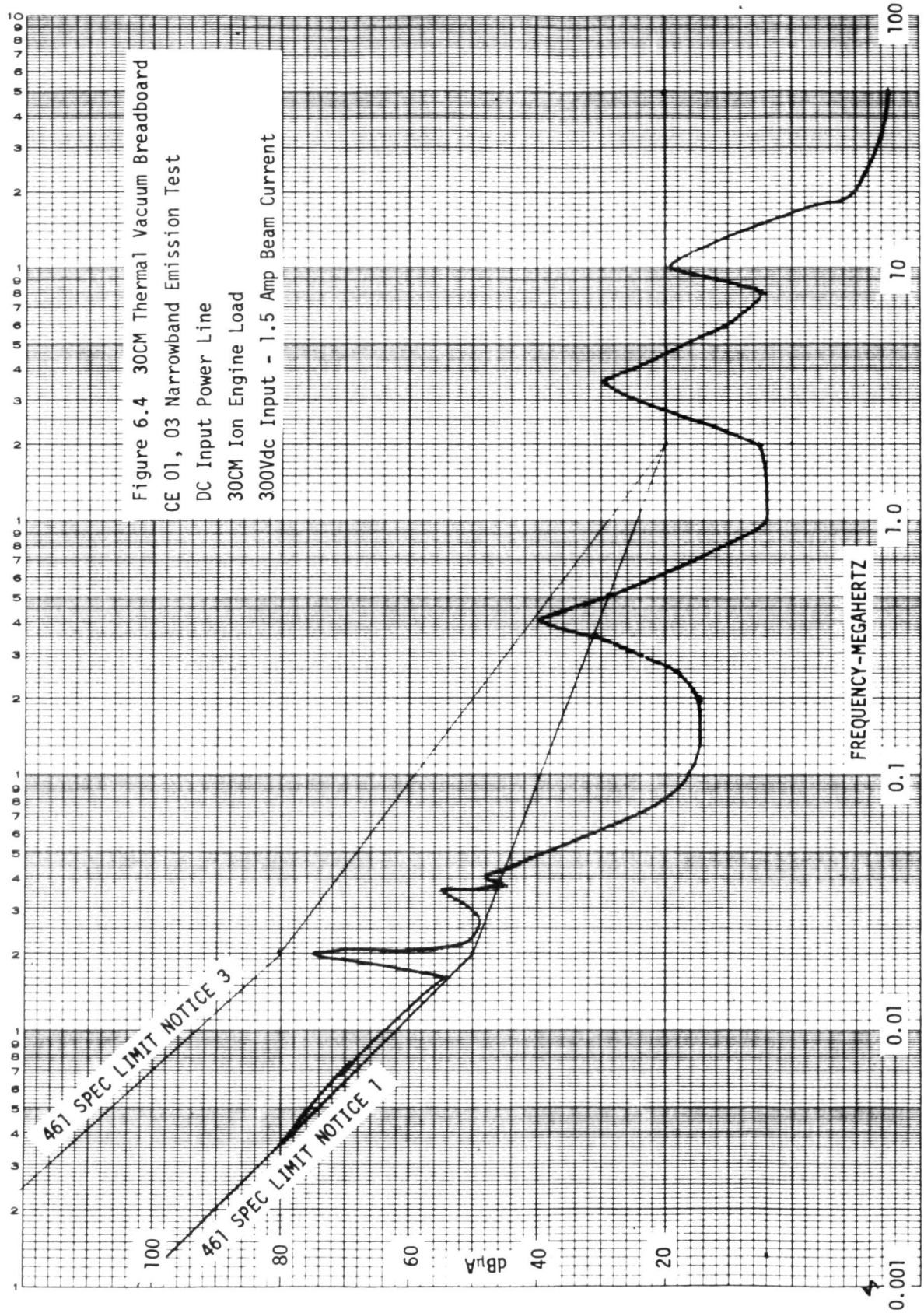


Figure 6.4 30CM Thermal Vacuum Breadboard
CE 01, 03 Narrowband Emission Test
DC Input Power Line
30CM Ion Engine Load
300Vdc Input - 1.5 Amp Beam Current
461 SPEC LIMIT NOTICE 3
461 SPEC LIMIT NOTICE 1
dBμA
FREQUENCY-MEGAHERTZ
0.001
0.01
0.1
1.0
10
100
20
40
60
80
100

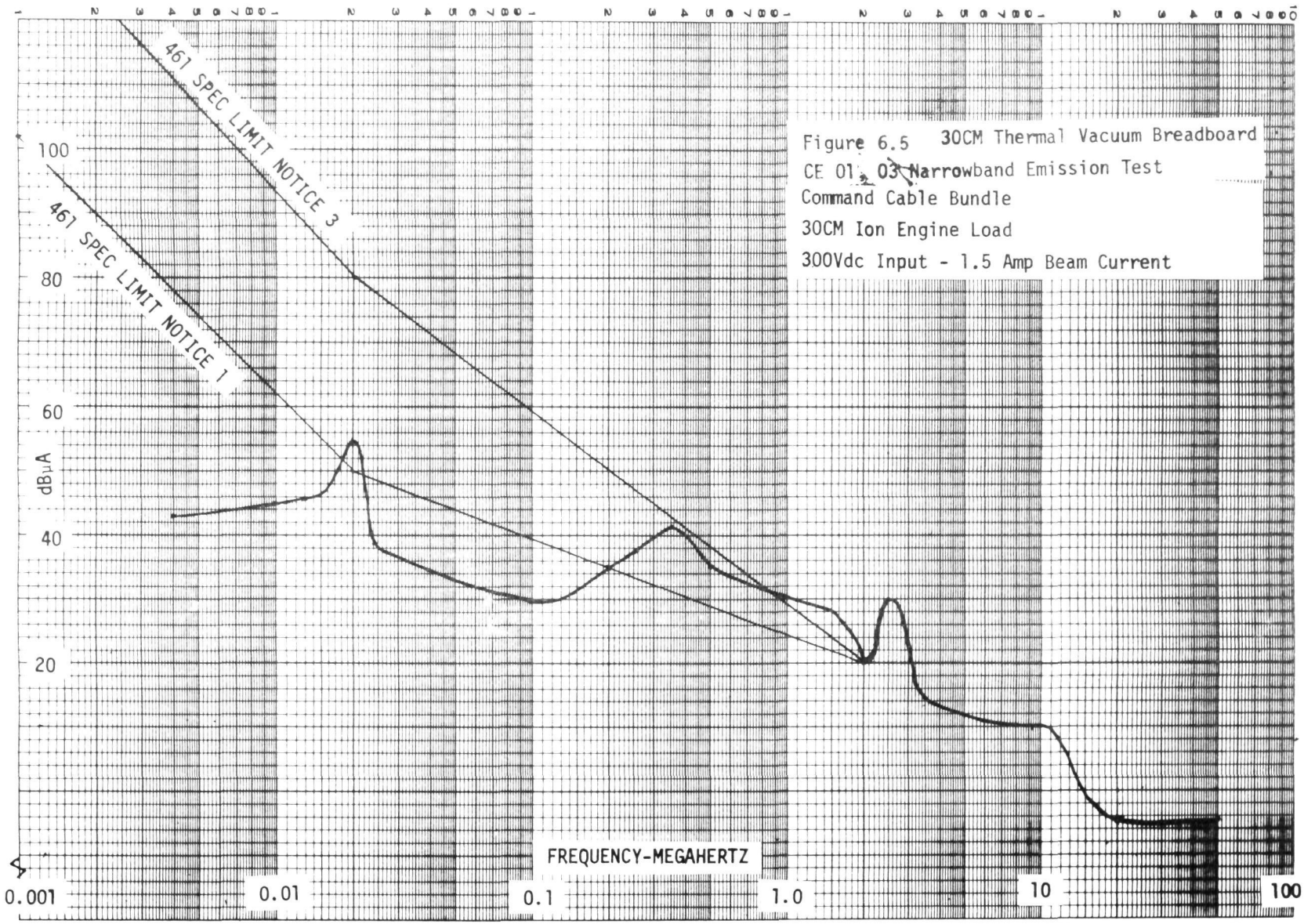


Figure 6.5 30CM Thermal Vacuum Breadboard
CE 01, ~~03~~ Narrowband Emission Test
Command Cable Bundle
30CM Ion Engine Load
300Vdc Input - 1.5 Amp Beam Current

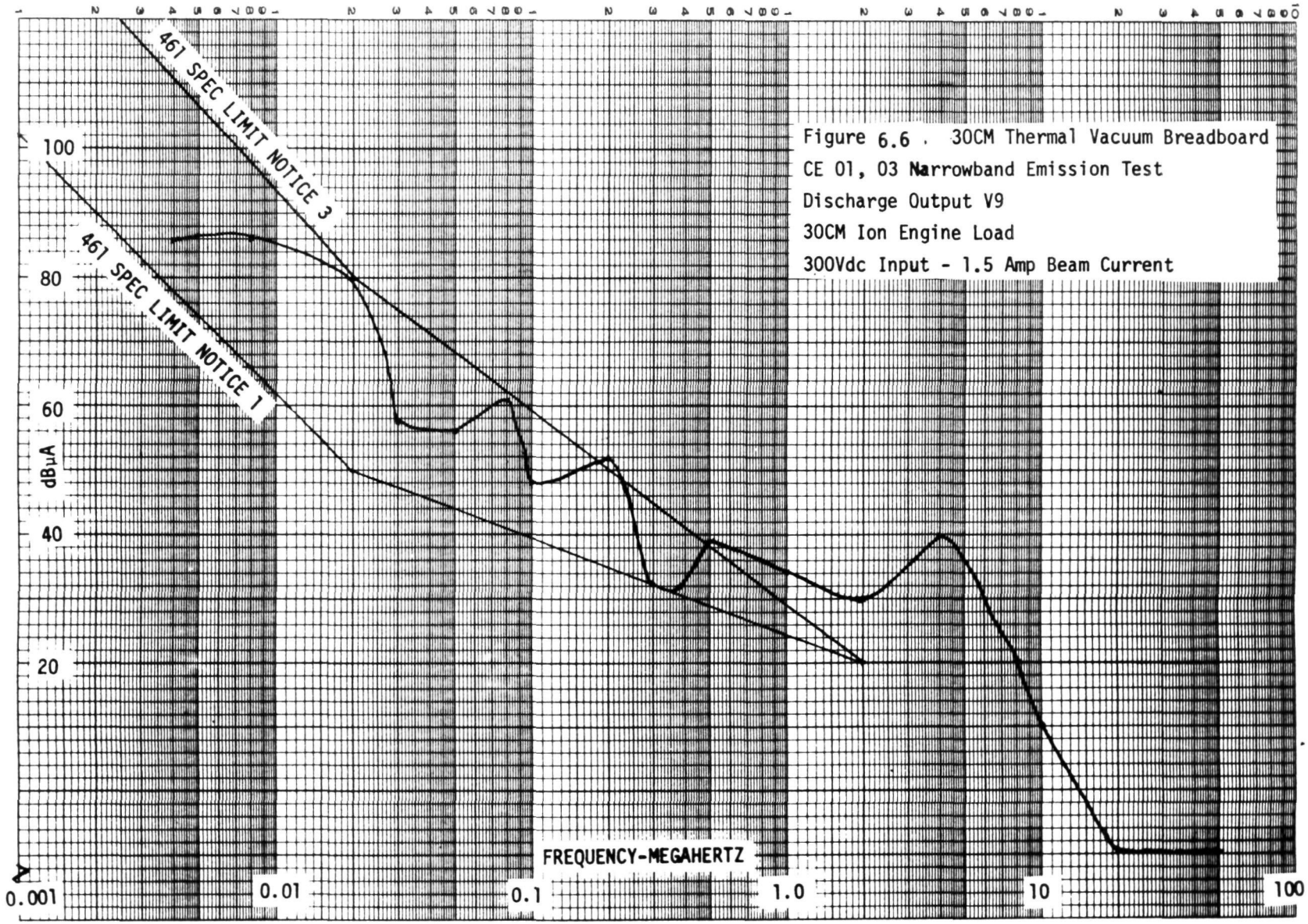


Figure 6.6 . 30CM Thermal Vacuum Breadboard
CE 01, 03 Narrowband Emission Test
Discharge Output V9
30CM Ion Engine Load
300Vdc Input - 1.5 Amp Beam Current

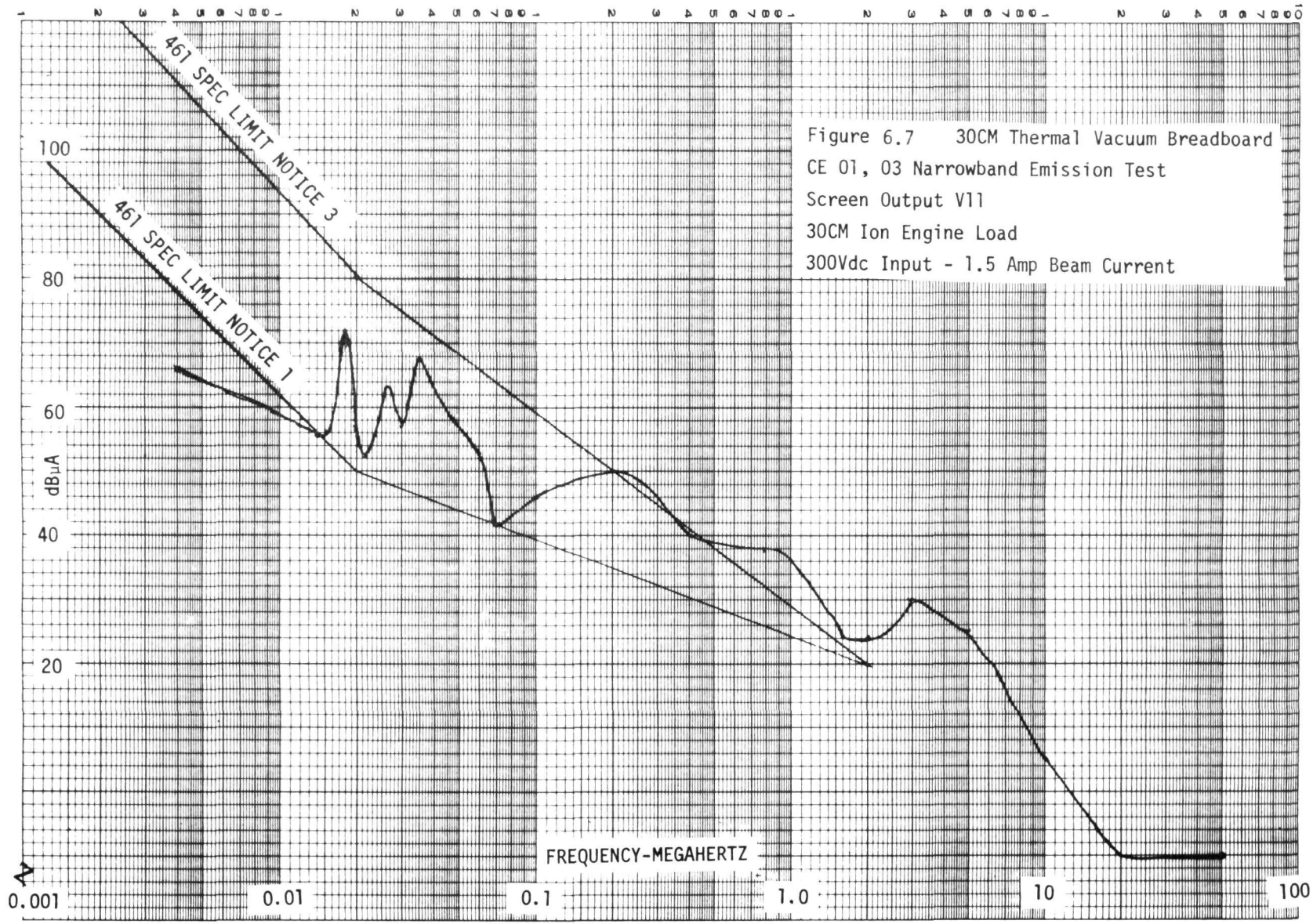


Figure 6.7 30CM Thermal Vacuum Breadboard
CE 01, 03 Narrowband Emission Test
Screen Output V11
30CM Ion Engine Load
300Vdc Input - 1.5 Amp Beam Current

- DC Input Power Line, Figure 6-8.
- Command Cable Bundle, Figure 6-9.
- Discharge Output (V9), Figure 6-10.
- Screen Output (V11), Figure 6-11.

Both the discharge and screen output lines are above MIL-STD 461 specification limit due to the noise being generated by the discharge chamber of the ion engine.

Copies of the data on other output lines can be obtained from NASA Lewis Research Center, 21000 Brookpard Road, Cleveland, Ohio, 44135, Attention Mr. J. H. Shank, Mail Station 54-4.

The conducted emission data is greatly influenced by the ion engine operation and it is expected that with the final design configuration of the 30cm ion engine, that the out-of-tolerance conditions will be minimized.

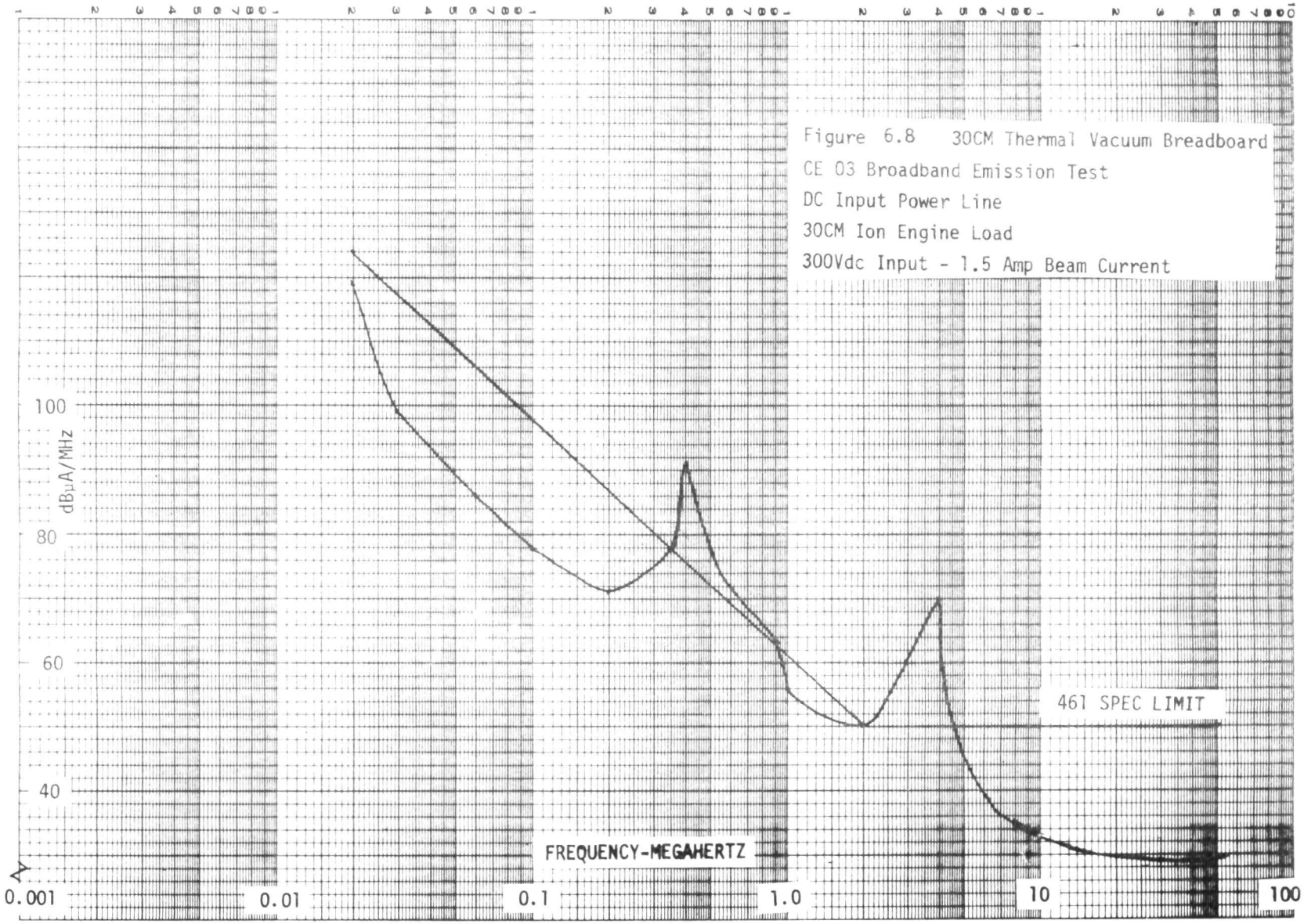


Figure 6.8 30CM Thermal Vacuum Breadboard
CE 03 Broadband Emission Test
DC Input Power Line
30CM Ion Engine Load
300Vdc Input - 1.5 Amp Beam Current

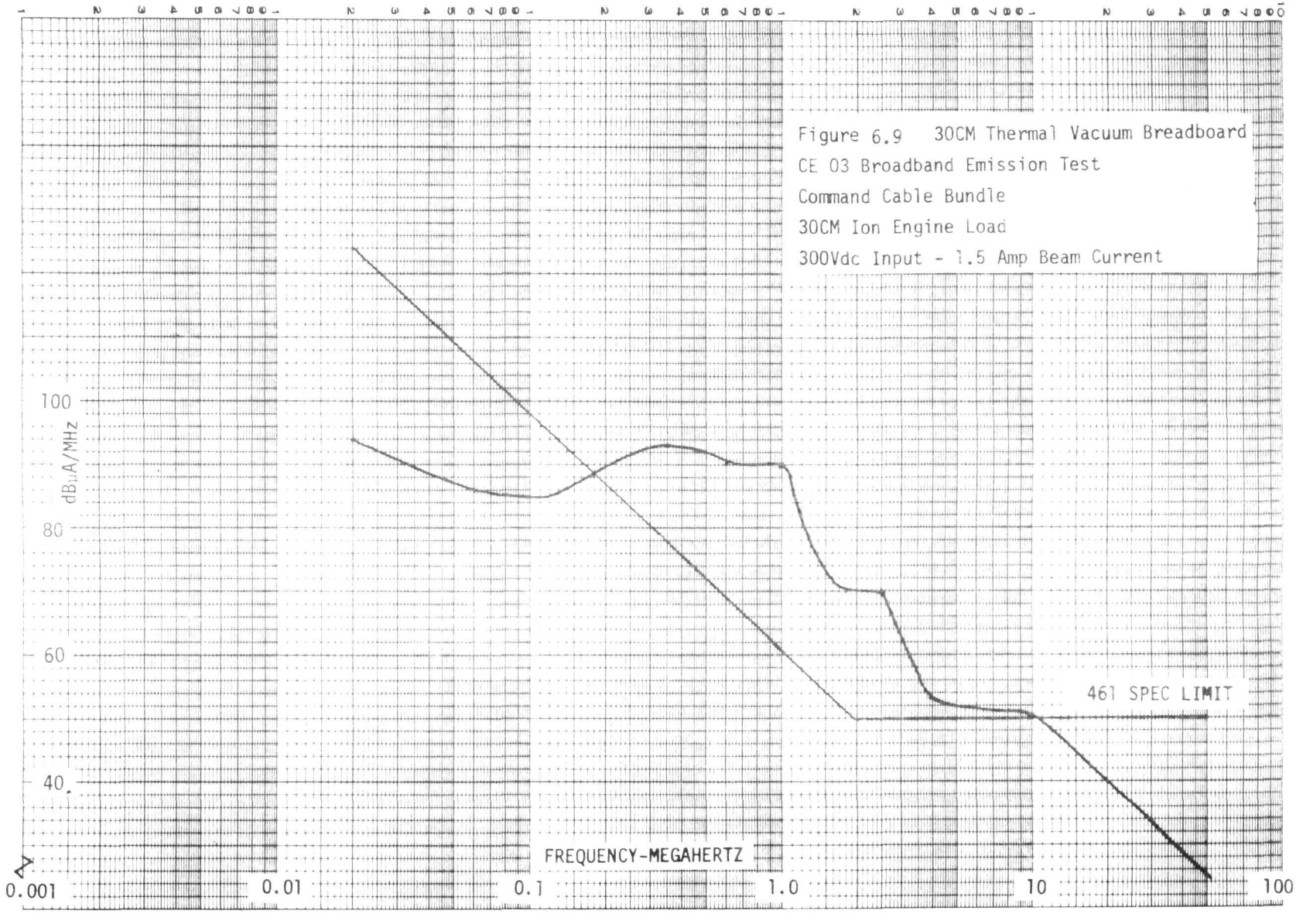


Figure 6.9 30CM Thermal Vacuum Breadboard
CE 03 Broadband Emission Test
Command Cable Bundle
30CM Ion Engine Load
300Vdc Input - 1.5 Amp Beam Current
100
80
60
40
dBμA/MHz
461 SPEC LIMIT
FREQUENCY-MEGAHERTZ
0.001
0.01
0.1
1.0
10
100

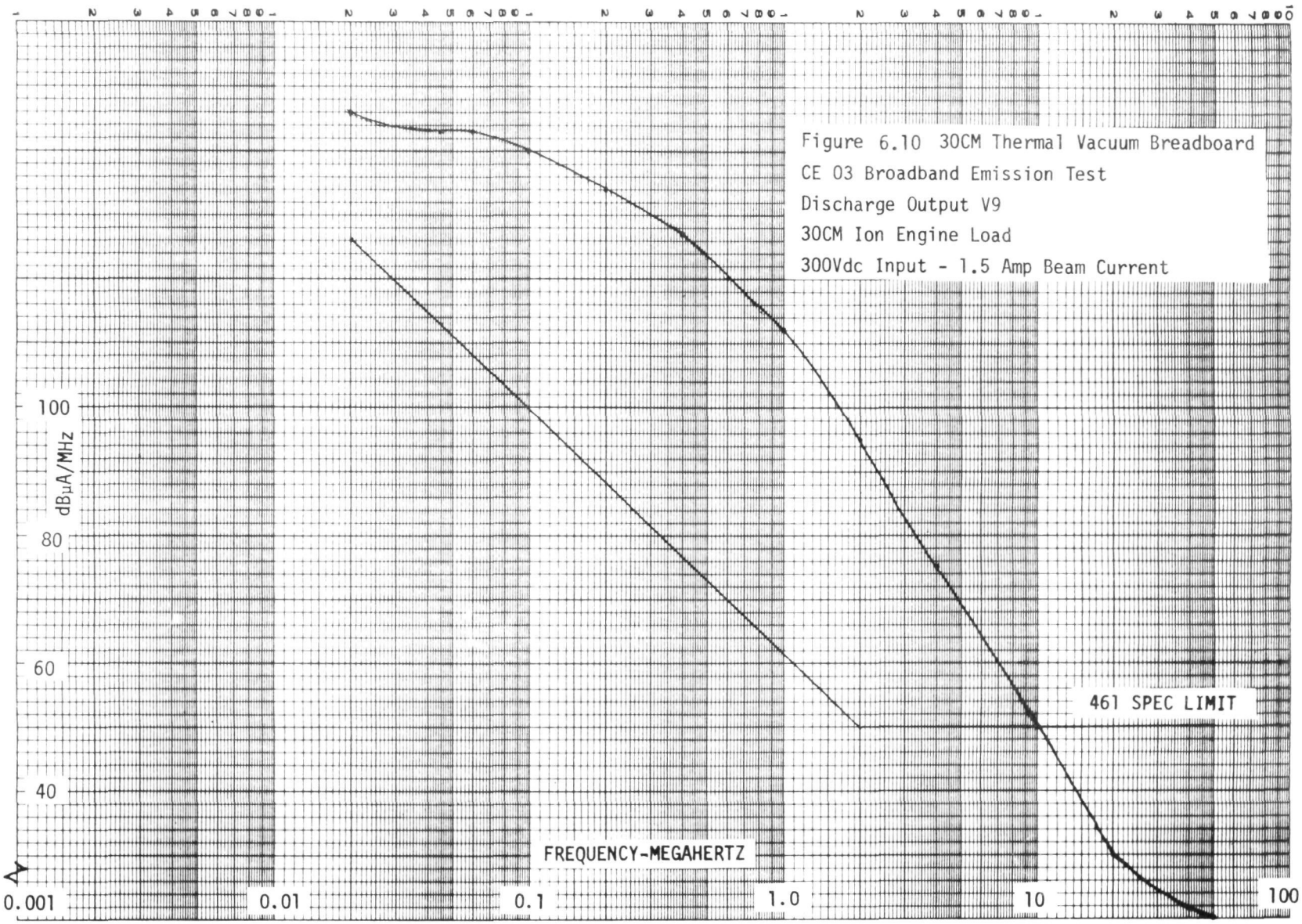


Figure 6.10 30CM Thermal Vacuum Breadboard
CE 03 Broadband Emission Test
Discharge Output V9
30CM Ion Engine Load
300Vdc Input - 1.5 Amp Beam Current

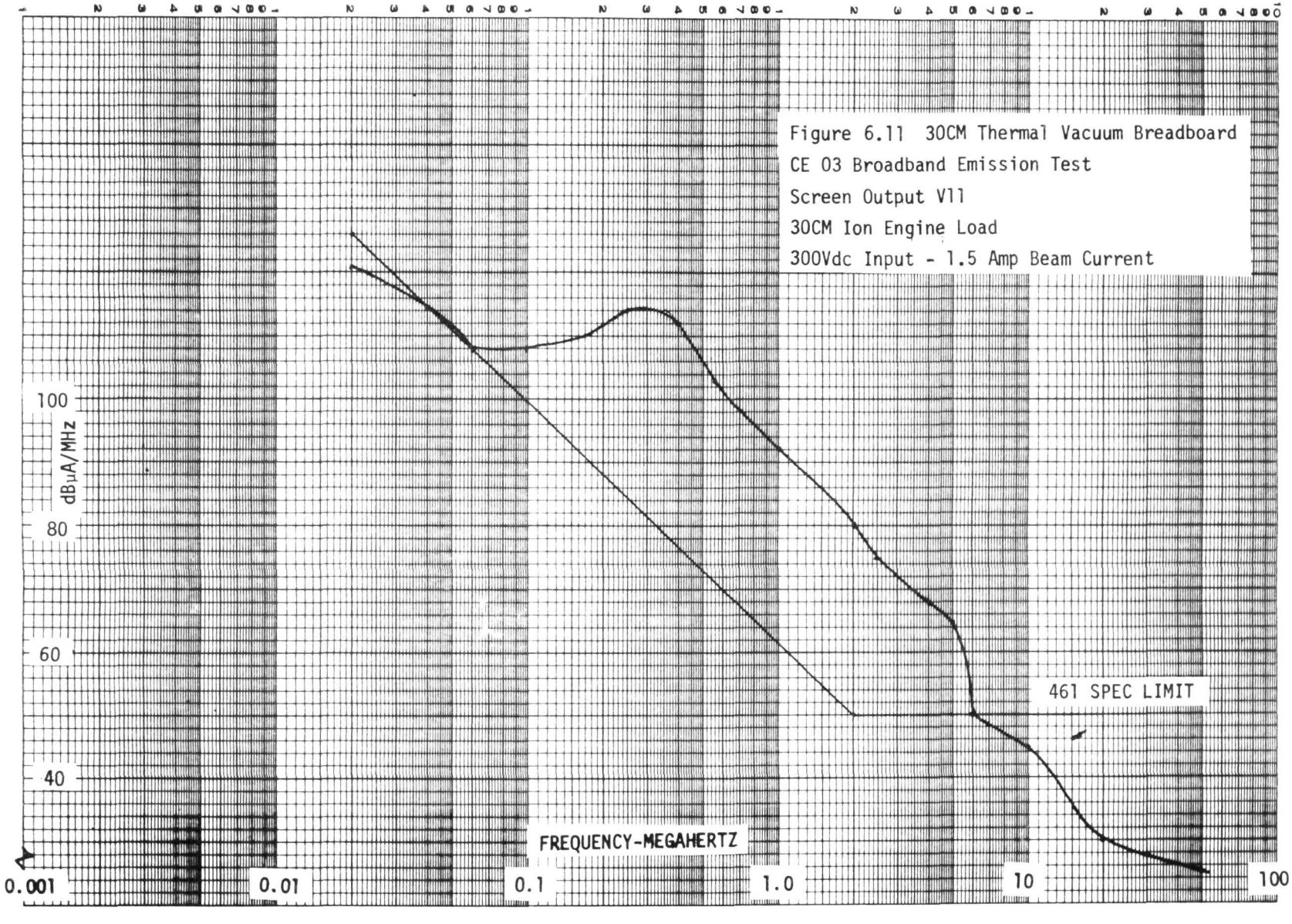


Figure 6.11 30CM Thermal Vacuum Breadboard
CE 03 Broadband Emission Test
Screen Output V11
30CM Ion Engine Load
300Vdc Input - 1.5 Amp Beam Current

7.0 CONCLUSIONS

The adaptability of the SCR series resonant inverter as the basic power stage of an ion thruster power processor has been demonstrated.

The ion thruster was operated with the SCR series resonant inverter power processor for over one hundred (100) hours under all operating conditions - start, shutdown, arcing, and steady-state at voltage and current extremes - with no operational problems and no power component failure.

Important attributes demonstrated by the SCR series resonant inverter are (1) ruggedness, (2) clearance of shorts within the ion thruster, (3) adaptability to input voltages as high as 400Vdc, (4) simplicity of design due to power handling capability, and (5) potential compliance with EMI requirements.

The SCR power processor for an ion engine also has the ability to: (1) isolate the input power bus from the effects of output voltage and/or power variations; (2) prevent output fault conditions from being fed directly back to the power source thereby avoiding collapse of the power source; and (3) control the operational conditions of the components to avoid their overstress during startup, input voltage variations, and output fault conditions.

The basic design of this power processor uses a L-C series resonant inverter which acts as a current limiting impedance between the power source and ion engine load. The L-C tank provides the instantaneous current limiting protection and the control electronics provides the long term protection or current limiting by adjusting the duty cycle modulation of the inverter stage.

The L-C series resonant inverter has another basic advantage in that the semiconductor current is a sinewave which reduces the power semiconductor switching losses and which eliminates the higher order harmonics. These higher order harmonics contribute to electromagnetic interference both in the power processor and in other equipment on the spacecraft.

Thermal vaccum testing of the power processor breadboard was conducted and the following functional tests were successfully performed.

- Startup of the power processor at 0°F baseplate temperature
- Operation of the power processor until temperature stability was obtained and the thermocouple readings recorded to assure safe operating temperatures for all components
- Shutdown and startup of the power processor at high baseplate temperature.

The power processor was integrated with the 30cm ion thruster. The following functional operations were demonstrated:

1. Neutralizer keeper ignition
2. Neutralizer keeper voltage regulation
3. Cathode keeper ignition
4. Discharge ignition
5. Discharge voltage - cathode vaporizer control loop
6. High voltage application to accelerator and screen
7. Beam current regulation from 0.6 to 2.0A
8. Recovery from internal engine arcs
9. Shutdown of ion engine.

8.0 APPENDICES

The following appendices are included:

Appendix A - 30cm Ion Thruster Power Processor Specification

Appendix B - Detail Block Diagram of 30cm Ion Thruster Power Processor

Appendix C - Mechanical Design of 30cm Ion Thruster Power Processor

APPENDIX A

A. 30CM Ion Thruster Power Processor Specification

The original design requirements for the 30CM ion engine power processor contained in Amendment 1, dated 1 June 1972, were modified by a revised requirement Amendment 3, dated 3 August 1973. The electrical design of the 30CM ion engine power processor is being designed to these revised specifications.

A.1 30CM Ion Thruster Power Processor Requirements

A.1.1 Electrical Requirements

A.1.1.1. Power Input - The thermal vacuum breadboard (TVBB) shall incorporate designs leading to eventual compatible operation with a spacecraft solar array power source consisting of series-parallel combinations of Non P silicon solar cells connected to provide a positive 200-400Vdc output. The maximum no-load voltage is 420Vdc. The solar cell array output characteristics will be influenced by power conditioner loads, radiation damage, temperatures, distance from the Sun and Sunline orientation. The TVBB shall provide stable operation on these static curves with an expected transient response of the solar cells to range between 20 to 60 μs.

For design purposes 300 volts input is considered the normal operating voltage. The input voltage variation for which the TVBB shall satisfy the output requirement is 200 to 400 volts. The TVBB shall remain operating below 200 volts (with out-of-tolerance outputs permissible) but will qutomatically shut off at or below 180 volts.

a. Input Filtering - The solar cell array is an inherent unidirectional power source and is current limited. The TVBB shall not supply reverse current to the input power source. Any network of filtering necessary to assure compatibility with the solar cell array power source shall be part of the TVBB.

b. Input Ripple - The current ripple (zero to peak) generated by the TVBB on the solar panel line shall be not greater than one percent of the average input current

c. An auxiliary housekeeping supply (for startup only) shall be included as a part of a TVBB test support equipment. The supply shall be 50 volts rms at 2.4KHz. Current requirements shall be determined by the Contractor before the TVBB design review.

A.1.1.2. Power Outputs - The TVBB electrical output requirements given in TableA-Iand Fig.A-1are based on ion thruster input requirements and the thruster operating characteristics. Interconnections of the thruster and the individual supplies of the TVBB shall be identical to those shown on Fig. 45(b) of NASA CR-120919. All outputs shall be capable of operation between no load, full load, overload, or short condition without any component overstress, or excessive output voltage overshoot during both the transient and steady-state operation.

Power matching of the TVBB load to the solar array (or solar array simulator) will be accomplished by a central computer external to the TVBB. For back-up purposes, the TVBB shall contain an undervoltage circuit which automatically shuts off the TVBB at or below 180 volts bus voltage within 1 msec.

The following paragraphs present the detailed TVBB output requirements. Turn-on and turn-off requirements are specified in Paragraph A.1.1.4. Throttling capability over a range of 5:1 input power shall be demonstrated. In order to avoid transient overloading of the solar panel, the TVBB peak power demand shall not exceed the steady-state demand by more than 1.0 percent.

TABLE A-I. 30CM THRUSTER POWER SUPPLY REQUIREMENT

Supply No.	Supply	Maximum	Nominal Level	Regulation Type and %	Ripple % p-p
1	Main vaporizer	10V at 2A	7V at 1A	I, 5%	
2	Cathode vaporizer	10V at 2A	3.5V at 1A	I, 5%	
3	Cathode heater	15V at 6A	9V at 4.5A		
		(On at start only)			
4	Main isolator	10V at 4A	4.5V at 2A	I, 5%	
5	Neutralizer heater	10V at 5A	8.5V at 4.2A	I, 5%	
		(On at start only)			
6	Neutralizer vaporizer	10V at 2A	3.5V at 1A	I, 5%	
7	Neutralizer keeper[1]	20V at 3A	12V at 2A	I, 5%	2%
8	Cathode keeper	60V at 1A	10V at 0.5A	I, 5%	2%
9	Discharge [2]	40V at 17A	37V at 14A	I, 1%	2%
10	Accelerator	1000V at 0.2A	500V at 0.008A	V, 2%	3%
11	Screen	1100V at 2.2A	1100V at 2A	V, 1%	1%
12	Magnetic Baffle	4V at 5A	4V at 5A	I, 5%	5%

[1] H.V. Section 1kV at 20mA (or special designs to assure starting of HRL 30cm thruster).

[2] Open circuit voltage $\geq$60V < 100V.

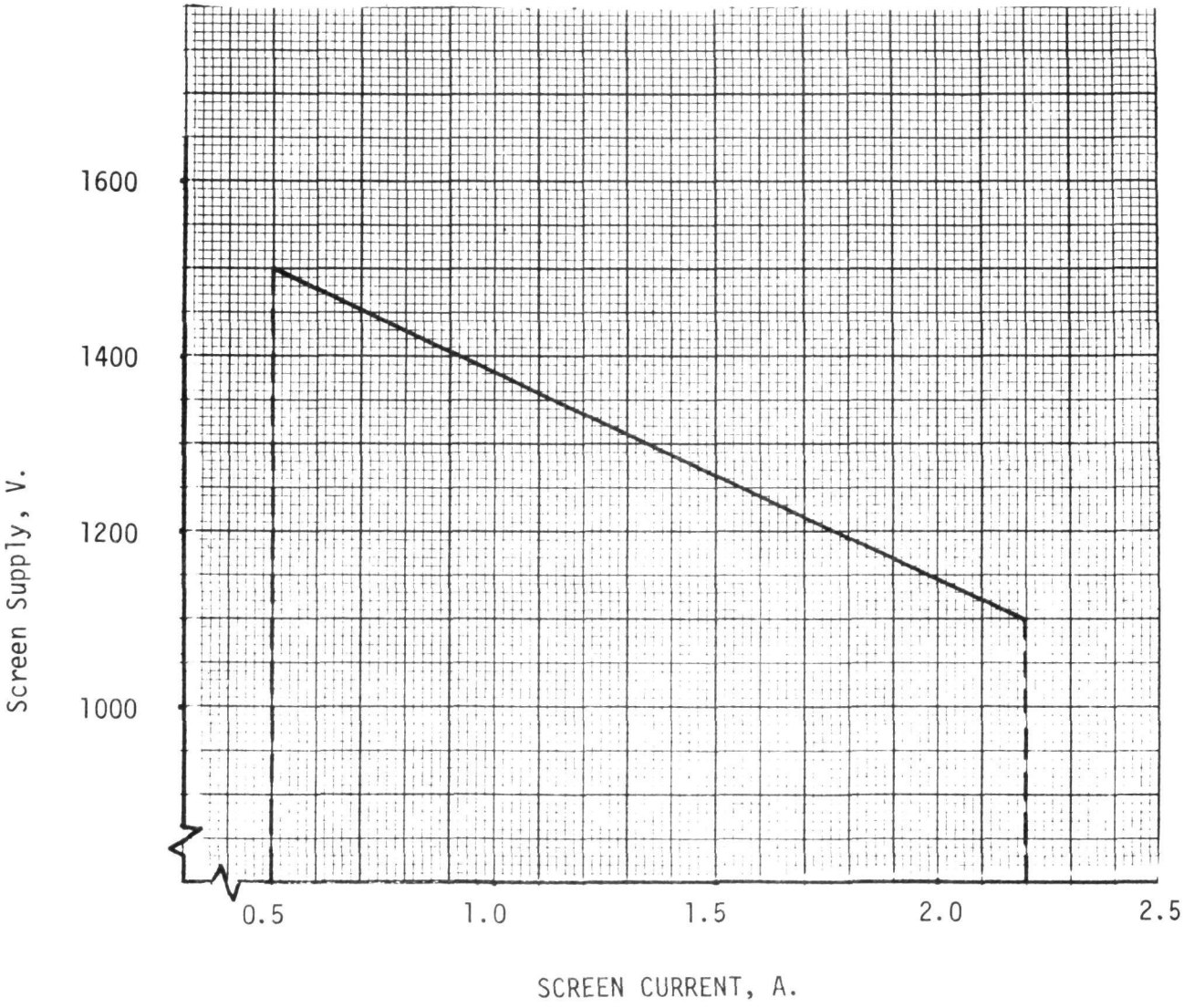


Figure A-1. Screen Supply Power Envelope for 2A Thruster (Max. Power, 2420 Watts)

a. Power Supply No.1 - Main Vaporizer - The output requirements for Supply No. 1 are listed in Table A-I. This supply for the thruster run mode shall operate closed looped with the screen power supply (No. 11). The feedback signal in this loop shall be derived by sensing beam current (screen current I_{11} compensated by the removal of accelerator current I_{10}). An externally supplied signal I_{11R} will be compared with the feedback current I_{11} and the positive error signal ΔI_{11} will control the input of the No. 1 supply.

The power supply shall be current limited and shall be self-protected against overloads. The supply will operate at spacecraft ground potential.

The transfer gain from the sensed beam current to main vaporizer current shall be determined by the following goal. Measured beam current shall be within $\pm$0.5 percent of I_{11R}. This constraint shall be satisfied over 2:1 excursions in main vaporizer current which may be encountered due to vaporizer aging or unusual thermal environment. Tradeoffs with respect to this goal will be considered during integration test should instabilities exist due to control loop interaction or high voltage recycling. This goal shall be attained over a range of beam current set points from 1.0 to 2.0 amperes.

b. Power Supply No. 2 - Cathode Vaporizer - The supply shall be capable of providing the output requirements listed in Table A-I. The supply shall be current limited and self-protected against overloads. The supply will operate at spacecraft ground potential.

During the thruster run mode, this supply shall operate in closed loop with the discharge supply (No. 9) in order to control discharge voltage. This loop is the supply major servo-loop. An internal minor loop is to be provided to limit the output current to a value proportional to a reference setpoint I_{2R}.

Initially, the major servo-loop is open (discharge voltage E9 > major loop setpoint E_{9R}) and supply No. 2 operates at the constant current mode. The major servo-loop closes when E_9 drops below E_{9R} because the discharge current I_9 has reached the level of reference I_{9R} and Power Supply No. 9 starts to operate in the current limited mode. This loop is self-compensating, which means that lowering E_9 causes a reduction in I_2 and a reduction of Hg vapor flow to the discharge, resulting in a rise in E_9.

c. Power Supply No. 3 - Cathode Heater - The Supply shall be capable of providing the requirements listed in Table A-I. The output of the supply output is referenced at the screen potential above ground.

This supply is required to operate only during startup. Its output power shall be reduced (or turned off) once full discharge current operation level has been achieved. The supply shall be current limited and self-protected against overloads.

d. Power Supply No. 4 - Main Isolator and Cathode Heater - The supply shall be capable of providing the output power requirements listed in Table A-I. The supply shall be limited and self-protected against overloads.

e. Power Supply No. 5 - Neutralizer Heater - The supply shall be capable of providing the output power requirements listed in Table A-I. The supply shall be self-protecting and current limited with an adjustment to allow presetting to a level in its dynamic range.

Output insulation of 200V between input and output shall be provided for bias operation.

f. Power Supply No. 6 - Neutralizer Vaporizer - The supply shall be capable of providing the output power requirements listed in Table A-I. The supply shall be self-protected and current limited with a preset internal adjustment. The supply will operate at spacecraft ground potential.

The output of Supply No. 6 shall be controlled by a voltage feedback signal from the output of the Neutralizer keeper supply (No. 7). This signal shall be compared to a voltage reference (E_{7R}) and the error signal generated shall be used to control the output current. E_{7R} shall be internally adjustable to allow presetting E_7 within the range of 10 to 20V.

The control characteristic shall be such that the constant current I_6 will be maintained until E_7 drops below E_{7R}. Below this value of E_7, the current I_6 will be reduced proportionally with a control characteristic slope of 0.8A/V approximately.

g. Power Supply No. 7 - Neutralizer Keeper

The supply shall be capable of providing the output power requirements listed in Table A-I. The supply shall be self-protecting and current limited, and have output isolation of 200V for biased operation.

The characteristics of the supply shall be such as to provide 1000V open circuit section with sufficient current capability to assure transition to the low voltage keeper section following keeper ignition. The low voltage sec-

tion shall be current regulated with an internally adjustable preset reference I_{7R}.

This supply operates in a closed loop mode with supply No. 6 as described in Paragraph A.1.1.2.f.

h. Power Supply No. 8 - Cathode Keeper - The supply shall be capable of providing the output power requirements listed in Table A-I. The supply shall provide 1000V open circuit with sufficient current capability to allow transition to low voltage. The low voltage section shall be current adjustable with an internally preset reference I_{8R}.

Output isolation shall be provided to allow floating at screen potential. The supply shall be self-protected.

i. Power Supply No. 9 - Discharge Supply - The discharge supply shall be capable of providing the output requirements listed in Table A-I. The supply shall be self-protecting and current limited, and be capable of supplying the output at screen potential.

The discharge supply output shall be regulated (setpoint 32-40V) for discharge currents up to 17A. The output voltage at the output terminals shall not be lower than 40V at 17A, and a minimum open circuit voltage of 60V. A variable current limit shall be provided by means of an external setpoint I_{9R}. I_9 shall be sensed on the negative side of the discharge supply.

This supply operates in a closed loop mode with the cathode vaporizer supply (No. 2) as discussed in Paragraph A.1.1.2.b.

j. Power Supply No. 10 - Accel - The supply shall be capable of providing the power o utput requirements listed in Table A-I. It shall be self-protected and capable of delivering 20mA in steady-state operation and up to 200mA for adjustable durations not exceeding 1sec. The positive terminal of this supply will be tied to the power processor common.

k. Power Supply No. 11 - Screen - The screen supply shall be capable of providing the requirements listed in Table A-I. and Fig. A-1. This supply shall be self-protecting against shorts to ground and shorts to supply No. 10. Circuitry shall be provided such that the capability for supplying high current at low voltage (to clear shorts between screen and accel) may be experimentally examined.

l. Power Supply No. 12 - Magnetic Baffle - This supply shall be capable of providing the requirement listed in Table 1. This supply shall be self-protecting and current limited, and be capable of supplying the output at screen potential. A reference signal from external to the power processor shall regulate I_{12} between 0 and 5A.

A.1.1.3. Operational Requirements

a. Overload Response - It is necessary that each individual supply shall be protected against excessive current. It shall be the design objective that supplies 1 through 9 be short-circuit proof and shall not be damaged even by a permanent short. Each supply should be capable of operating with such a load condition without causing any component to exceed the temperature allowed by reliability assessment of the component.

Supplies 10 and 11 shall be equipped with overload tripping. If current in either of these supplies exceeds its specified trip value, various supplies shall be turned off or set to appropriate limits at a rate and for a duration which is sufficient to prevent damage to the thruster and the TVBB. The overload protection shall not be disabled by the reset command. The TVBB shall not be damaged by external shorts or overloads on any output, between outputs or from outputs to ground. Sequencing circuitry shall be provided to assure the proper reapplication of these supplies following the removal of the overcurrent.

b. Protection Against Low Mode Operation - Under certain conditions the beam current - main vaporizer loop gain becomes negative such that an increase in main propellant flow reduces the beam current. This condition may be caused by transients, excessive thermal feedback to the vaporizer, or errors in reference signals. The Contractor shall provide the necessary controls to prevent the occurrence of low mode during thruster startup, throttling, or steady-state operation. Guidelines for the design of such controls will be sent to the Contractor by the NASA Program Manager within one month after date of contract.

c. PS 3, 4 5 shall be operated at the startup power levels up to emission currents of 5 amperes. Above 5 amperes emission, PS3, 4, 5 shall be turned off. The emission current reference point shall be adjustable such that changes may be made to insure cathode integrity and prevent propellant condensations.

d. The TVBB input power lines shall be electrically isolated from the output power lines.

e. The TVBB shall have separate cable harnessing of input power, output power, logic, and telemetry lines.

f. Neutralizer common shall be allowed to float with respect to spacecraft or facility ground.

g. For a TVBB employing transistor switching inverters, failure detection circuitry shall be provided for PS9 and 11. When a failure is detected, the standby inverter shall be driven at the phase of the failed inverter.

   Failure detection circuits shall insure continuous regulated output and also protect the main bus from sustained shorts through the power circuit.

h. Direct current heaters shall be limited to $\pm$ 10% ripple.

A.1.1.4

Command Telemetry Transfer and Computer Interfacing

The TVBB system shall be composed of an interact unit (IU) and a power processing unit (PPU). A flow diagram (Fig. A-2) describes the TVBB system. The interfaces are generally defined below. Other details are itemized in paragraphs A.1.1.4.1, 4.2, and 4.3.

a. Interface Unit - Power Processing Unit

(1) PPU turn-on and off shall be by discrete digital commands.

(2) Reference signals shall be 0-5V analog.

(3) Telemetry shall be 0-5V analog.

(4) The IU shall use the same power bus as the PPU.

(5) The IU shall be removable from the TVBB system. Electrical connectors from IU to PPU shall be provided.

(6) Input and output to the PPU shall be referenced to S/C or laboratory ground (i.e., electrical isolation shall be performed in the PPU).

(7) The contractor shall identify the set points which shall be variable. A minimum of four choices (including Power Supply off) shall be included for each of the selected set points and one of the choices in each instance shall be a potentiometer. The choice shall be selected external to the power processor.

b. Computer - Interface Unit

(1) The input and output to the computer shall employ parallel digital logic. Signals shall be referenced to S/C or laboratory ground.

(2) The interconnection between a computer and the interface unit shall be made with 32 lines (sixteen parallel in and sixteen parallel out). The interface unit shall generate a flag command to signal the computer that data has been digitized and is ready for transfer. The IU shall be provided with 32 lines (20 feet long) which shall be terminated at the IU with connectors. The computer to be employed at LeRC for integration test will be limited to a data rate of 200,000 words per minute. Each word is defined to be 16 bits long.

(3) The Contractor shall submit to LeRC a plan for digital encoding between the computer and IU. This plan shall be submitted for LeRC review and approval within four months after date of contract.

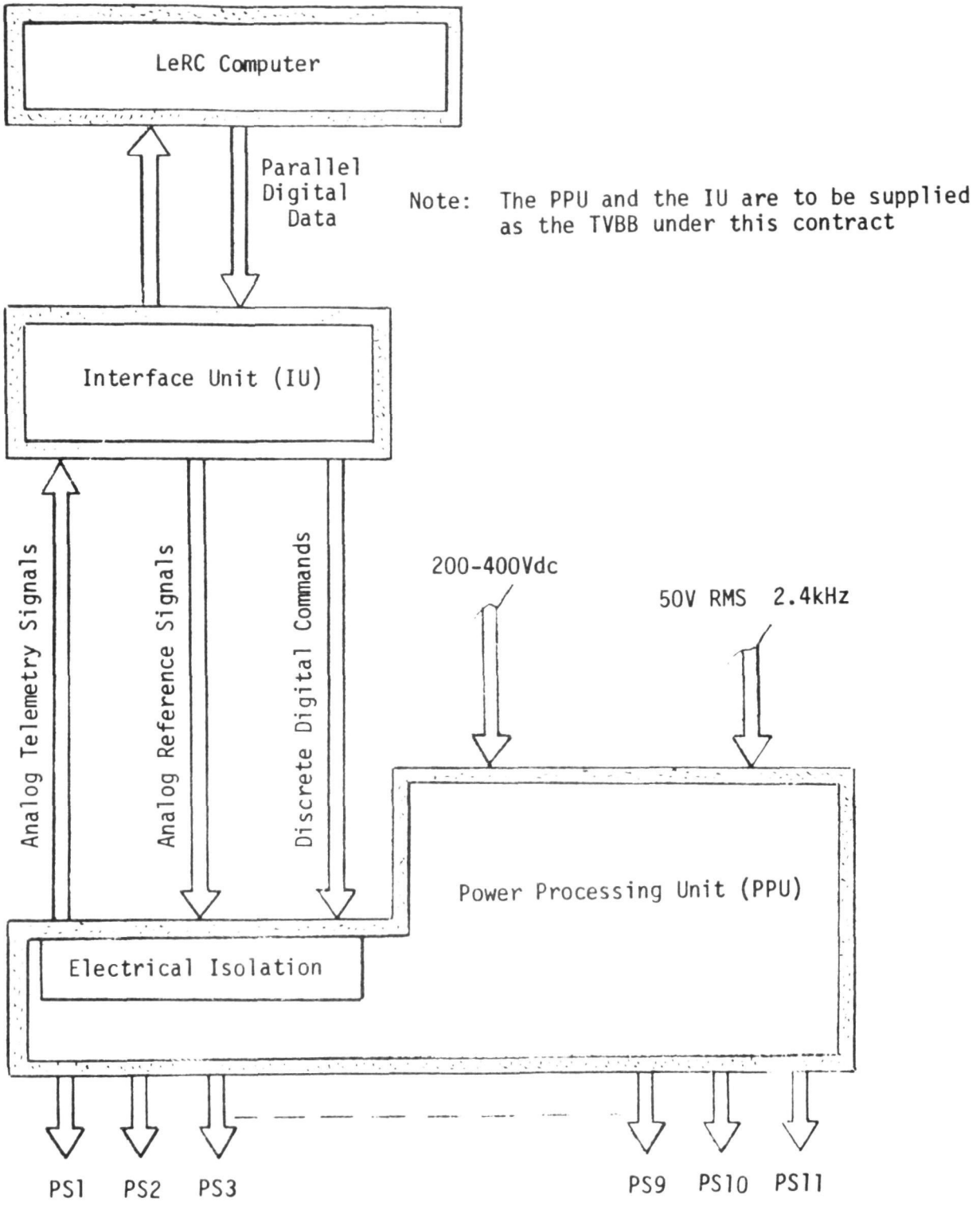


Figure A-2. Electrical Flow Diagram

A.1.1.4.1

PPU Turn-On and Off

a. General - The command words from the computer (16 bit parallel digital) shall be decoded in the IU and supplied to the PPU in the form of discrete digital commands. Command lines to the IU and PPU shall be referenced to S/C or laboratory ground. Digital control electronics are required to provide timing functions for startup, shutdown and high voltage recycling.

b. Turn-On Commands - The PPU shall be commanded on using the following sequence and nomenclature.

(1) ON-1 command turns on PS 3, 4, 5, 7, 8 and 9.
(2) ON-2 command turns on PS 1, 2 and 6.
(3) ON-3 command turns on PS 10 and 11.
(4) Ready to respond to I_{11R} signals.

The time intervals between commands will be determined by thruster characteristics and will be established external to the TVBB.

c. Turn-Off Commands - The PPU shall be commanded off using the following sequence and nomenclature.

(1) OFF-1 command turns off vaporizer supply No. 1 only.
(2) OFF-2 command turns off all power supplies.

The OFF-1 command shall not be nullified by overload tripping. The capability shall be provided to nullify the OFF-1 command by sending the ON-2 command only.

d. Recycle Procedure - Some of the arcs that occur within the thruster or between the thruster and the facility ground will not extinguish and must be interrupted artificially. A mechanization of PPU shutdown and restart is as follows: Shutdown of the thruster shall be initiated by one of the overcurrent trips as defined in NASA CR-120919, page 109. Modifications may be made to protect the thruster

and power processing units. Such a signal shall turn off supplies Nos. 10 and 11, reduce supply No. 9 to a preset current level in the range of 3 to 15A, and set supplies 2 and 3 to their trip levels. After a delay (that can be adjusted by changing fixed resistors) power supplies Nos. 10 and 11 will be turned on.

Following HV on, the discharge is ramped to its run current setpoint and the cathode vaporizer loop released to reestablish discharge voltage. The main vaporizer is then released to a closed loop configuration. Should the arcing and restart occur after "OFF-1" command was applied, the restarting sequence shall not nullify the command.

An alternate recycle sequence might be as follows:

"Some of the arcs that occur within the thruster or between the thruster and the facility ground will not extinguish and must be interrupted artificially. The mechanization of PPU shutdown and restart shall be as follows: Shutdown of the thruster shall be initiated by one of the overcurrent sensors on PS10 - Accelerator of PS 11 - Screen. After an adjustable time limit (approximately 5 ms) after sensing an overload condition, PS 9 - Discharge Current Reference will be reduced to a preset current level in the range of 5 to 15A and PS 1 - Main Vaporizer will be turned off. If the overload clears, return PS 9 - Discharge Current Reference and PS 1 - Main Vaporizer back to normal level. But if the overload lasts for a longer period (approximately 0.5sec, adjustable), turn-off PS 10 - Accelerator and PS 11 - Screen. After 0.5sec (adjustable), turn PS 10 and PS 11 back on and after 2 sec, return PS 9 - Discharge Current Reference and PS 1 - Main Vaporizer back to normal, if overload is cleared."

Should the arcing and restart occur after "OFF-1" command was applied, the recycle procedure shall not nullify the command and restart PS 1 - Main Vaporizer.

(The PS 8 - Cathode Keeper, and PS 2 - Cathode Vaporizer control loop shall not be disabled during the overload condition.)

e. Recycle Counter - A circuit shall be provided to count the number of recycles (trips). A 4.5 ±0.5V signal shall be telemetered if the trip rate exceeds 10 trips per minute. This signal shall turn off PS 10 and 11. This signal shall be an output similar to the telemetry data.

A.1.1.4.2 Reference Signals

a. General

All reference signals shall come to the PPU interface in the form of 0-5V analog signals. Electrical isolation shall be provided within the PPU.

b. Beam Current Reference

The analog signal required to set the ion beam current level will be supplied in the form of I_{11R} from the IU. The value of this reference signal will be continuously varied from 1.13Vdc (I_{11} = 0.5A) to +5Vdc (I_{11} = 2.2A). The PPU shall not respond to a reference signal greater than 5.1V.

c. Discharge Current Reference

The analog signal required to set the discharge current I_{9R} shall be derived from the IU. The value of this reference normally will be continuously varied from +1V (3A) to +5V (17A). The PPU shall not respond to a reference signal greater than 5.1V.

d. Screen Voltage Reference

A computer external to the TVBB will be programmed to provide the appropriate reference signal to the PPU via the IU to insure constant thruster effective specific impulse over the throttling range. The analog reference to the PPU shall be varied from 0V (0V) to +5V (1500V). The PPU shall not respond to a reference signal greater than 5.1V.

e. Magnetic baffle current: 0 to 5A

A.1.1.4.3 Telemetry Outputs

a. Digital telemetry (TM) outputs (from the interface unit) shall be provided to monitor supply outputs shown in Table A-II Emission current and beam current shall be telemetered rather than I_9 and I_{11}. The analog TM output from the PPU shall be isolated in the PPU.

b. Amplitude - The PPU shall provide analog signals to the interface unit. The analog signals shall continuously and linearly represent a given parameter from 0Vdc to 5Vdc as described in Table A-II Analog signals shall not, under any condition, exceed the range -1V to 7Vdc.

c. Telemetry Source Impedance and Loading - The source impedance of telemetry signals shall be 10KΩ or less. The PPU shall not be inhibited from proper operation by TM loads (such as short-circuit) or by externally-induced TM line noise or EMI.

d. Normal Telemetry Accuracy - Calibration accuracy of +5 percent of full scale setting will be provided, with a maximum design drift of 2 percent over 10,000 hours of operation for all TM signals, except as noted below.

TABLE A-II TELEMETRY

(Prior to A/D conversion; 0-5V range)

Supply		Current (A)	Voltage (V)	
1	Main vap.	0-2		
2	Cathode vap.	0-2		
3	Cath. heat.	0-10		
4a	Main isolator	0-2		
4b	Cathode isolator	0-2		
5	Neut. heat.	0-10		
6	Neut. keeper	0-2		
7	Neut. keeper	0-4	0-30 30-1030	(0-3V) (3-5V)
8	Cathode keeper	0-1	0-30 30-1030	(0-3V) (3-5V)
9	Discharge	0-20(1)	0-50	
10	Accelerator	0-0.05	0-1000	
11	Screen	0-2.5(2)	0-1500	
12	Recycle counter		4.5	
13	Magnetic baffle	0-5		

(1) Must measure emission current.

(2) Must measure beam current.

e. High Accuracy TM Signals - Telemetry data from I_9, I_{11}, E_9, E_{10} and E_{11} must be of high accuracy. Over the temperature range 15°C to 75°C, these signals shall have a calibration accuracy equal to or better than 0.5 percent of actual value plus 0.5 percent of full scale.

f. Telemetry Grounding - A separate TM signal return line shall be provided at ground potential.

A.1.1.5. PPU Internal Grounding - The PPU internal grounding shall be designed to minimize all interactions which are not a part of the primary conditioning or control function. Specifically, integrated circuits, referenced internal bus voltages, feedback circuits and telemetry data shall be protected from power transients. Separate (parallel) "power" and "signal" ground points shall be used to prevent power transient currents from passing through the signal ground point. The telemetry "return" or ground sha shall be connected to the signal ground at the PPU. Power returns shall be floating with respect to system ground (spacecraft or laboratory grounds). Power supplies shall not use signal or telemetry return lines for power returns. A voltage detection circuit shall be provided to clamp between neutralizer common and system ground when the voltage exceeds 75 volts.

A.1.1.6. Design Breadboard Model Reliability - Based on the thermal environment defined in this specification, the contractor shall compute the expected reliability for 10,000-hour operation. This computation shall be documented along with assumed failure rates and parts count. Methods for improving reliability shall be made a part of the reliability analysis. A design goal for the reliability "improvement" analysis is the reliability value specified for the engineering model of 0.96 for 10,000 hours.

A.1.1.7. Efficiency

a. Average Volt-Ampere Efficiency - This is based on the ratio of average power in. In this case, the "average" is based on average reading dc meters for dc input and output and on rms meters for ac outputs measured at the PPU. If the ac component (ripple) imposed on the dc values is reasonably small, and if the ripple current and voltage are in phase (nonreactive), this average E-I efficiency is identical with the thermal efficiency based on the ratios of output power to output power and dissipation.

b. Breadboard Model Efficiency - The PPU shall be evaluated per paragraph A.1.1.7a. Using this definition of efficiency, the design goal for the "average volt-ampere" efficiency is 91 percent at full power and 400V input. The contractor shall measure the efficiency at various conditions over the operating range of input and output power. Efficiency tradeoffs, particularly with cost, shall be noted in the efficiency analysis.

APPENDIX B

B. Detail Block Diagram of 30CM Ion Thruster Power Processor

Figure B-1 illustrates the block diagram of the 30CM ion thruster power processor. Power flow of the 200V to 400Vdc solar array is through a common input filter into two SCR series inverters.

The input filter is a two-stage LC network for filtering the high ac current drawn by the inverters. A common input filter is used to reduce the total filter weight of the power processor.

Series Inverter No. 1 is the multiple output inverter. It provides a constant current source to all its loads which are connected in series and runs at a constant frequency. The multiple output inverter supplies the following transformers.

- o V1 Main Vaporizer supply
- o V2 Cathode Vaporizer supply
- o V3 Cathode Heater supply
- o V4 Isolator supply
- o V5 Neutralizer Heater supply
- o V6 Neutralizer Vaporizer supply
- o V7 Neutralizer Keeper supply
- o V8 Cathode Keeper supply
- o V9 Discharge supply
- o V12 Magnetic Baffle supply
- o V_{Aux} Auxiliary supply

Series Inverter No. 2 supplies the V10 and V11 outputs (screen and accelerator). Its operating frequency varies proportional to the output power.

B.1 Multiple Output Inverter

The sinusoidal current I flowing through the series connected output transformer string is a constant frequency, constant amplitude current. The turns ratio of the series connected transformers determine the power sharing of the series string. Regulation of each output is achieved by phase firing of the shunt transistor or SCR which shunts the transformer secondary current thus regulating the output.

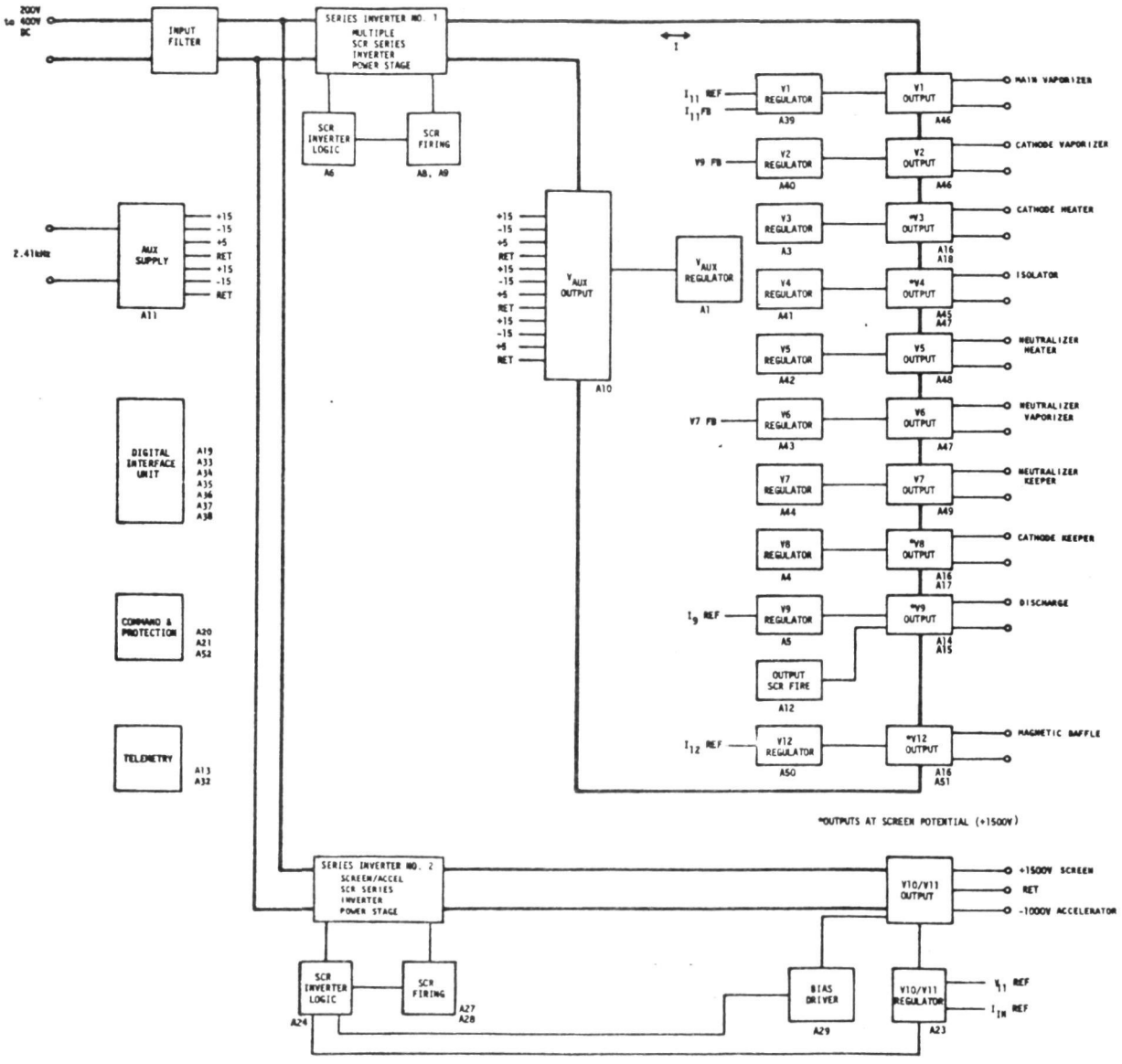


FIGURE B.1. 30CM ION ENGINE POWER PROCESSOR BLOCK DIAGRAM

B.1.1 Output Regulators

Detail block diagrams are given in the following sections for all the regulating loops. The ASDTIC control system is applied wherever possible to improve both regulation accuracy and regulator feedback control loop stability.

B.1.1.1 V1, Main Vaporizer Supply

Figure B.2 shows the detail block diagram for the V1 supply. Constant frequency of 20kHz from the multiple output inverter excites the primary of the current transformer T1. To control the output current and voltage, shorting transistor Q is turned on which places a short across winding N3 and all the secondary current transfers from winding N2 to winding N3 and zero power flows in winding N2.

Three regulating loops control the V1 power.

- o V1 voltage limiting by means of T2 and operational amplifier U1
- o I_1 current limiting by means of operational amplifier U2
- o Screen current control by means of operational amplifier U3.

The first two loops are for maximum current and voltage limiting. The current loop has three externally selectable reference levels for varying the current limit points. The third loop controls the ion engine beam current flow by varying the power applied to the vaporizer. The current regulating loops utilize the ASDTIC principle for regulation. The ramp function is added to the output of the operational amplifier to obtain regulator stability when operating in a constant frequency system.

To limit the output at no load operation, a power zener diode VR1 conducts and clamps the maximum output voltage. Because the V1 output is referenced to ion engine ground, the +1.5KV output can arc over to the V1 output and cause excessive voltage to appear on the output power components. To protect the output power components, blocking diode CR1 is inserted in series with the output line.

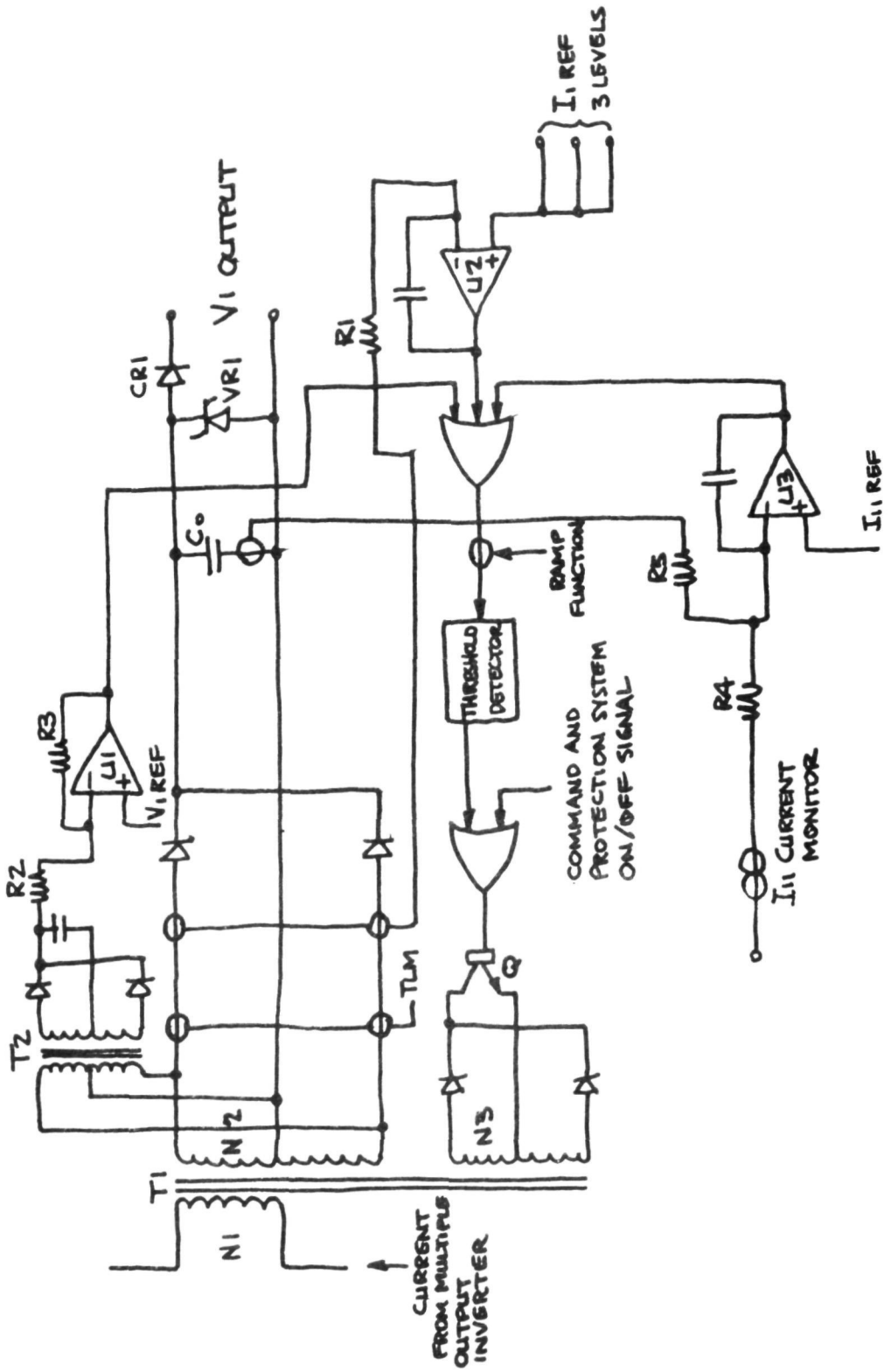


FIGURE B.2. V1, MAIN VAPORIZER SUPPLY BLOCK DIAGRAM

B.1.1.2 V2, Cathode Vaporizer Supply

Figure B.3 is the block diagram for the V2 supply. The supply has three control loops.

- o V2 voltage limiting by means of T2 and operational amplifier U1
- o I2 current limiting by means of operational amplifier U2
- o V9 voltage control by means of operational amplifier U3.

The first two loops control the maximum output voltage and output current. The current limit point is externally adjustable in three discrete steps. The third loop controls the discharge voltage of the ion engine arc source by varying the cathode vaporizer output power. The discharge voltage level is externally adjustable in three steps.

Output zener diode VR1 limits the maximum no load output voltage and CR1 protects the output circuitry from overstress during arc over of the beam supply.

B.1.1.3 V3, Cathode Heater Supply

Figure B.4 is the block diagram for the V3 supply. Voltage and current limiting is provided with three externally adjustable current limit points. The output of the V3 supply floats at the 1.5KV screen potential. Transformers T1 and T2 have shields between the high voltage winding and the rest of the transformer for isolation purposes.

Output zener diode VR1 limits the maximum no load output voltage and CR1 and VR2 protect the output circuitry from overstress during arcs.

B.1.1.4 V4, Isolator Supply

Figure B.5 is the block diagram for the V4 supply. Voltage and current limiting is provided with three externally adjustable current limit points. The output of the V4 supply floats at the 1.5KV screen potential. Transformers T1 and T2 have shields between the high voltage winding and the rest of the transformer.

Output zener diode VR1 limits the maximum no load output voltage and CR1 and VR2 protect the output circuitry from overstress during arcs.

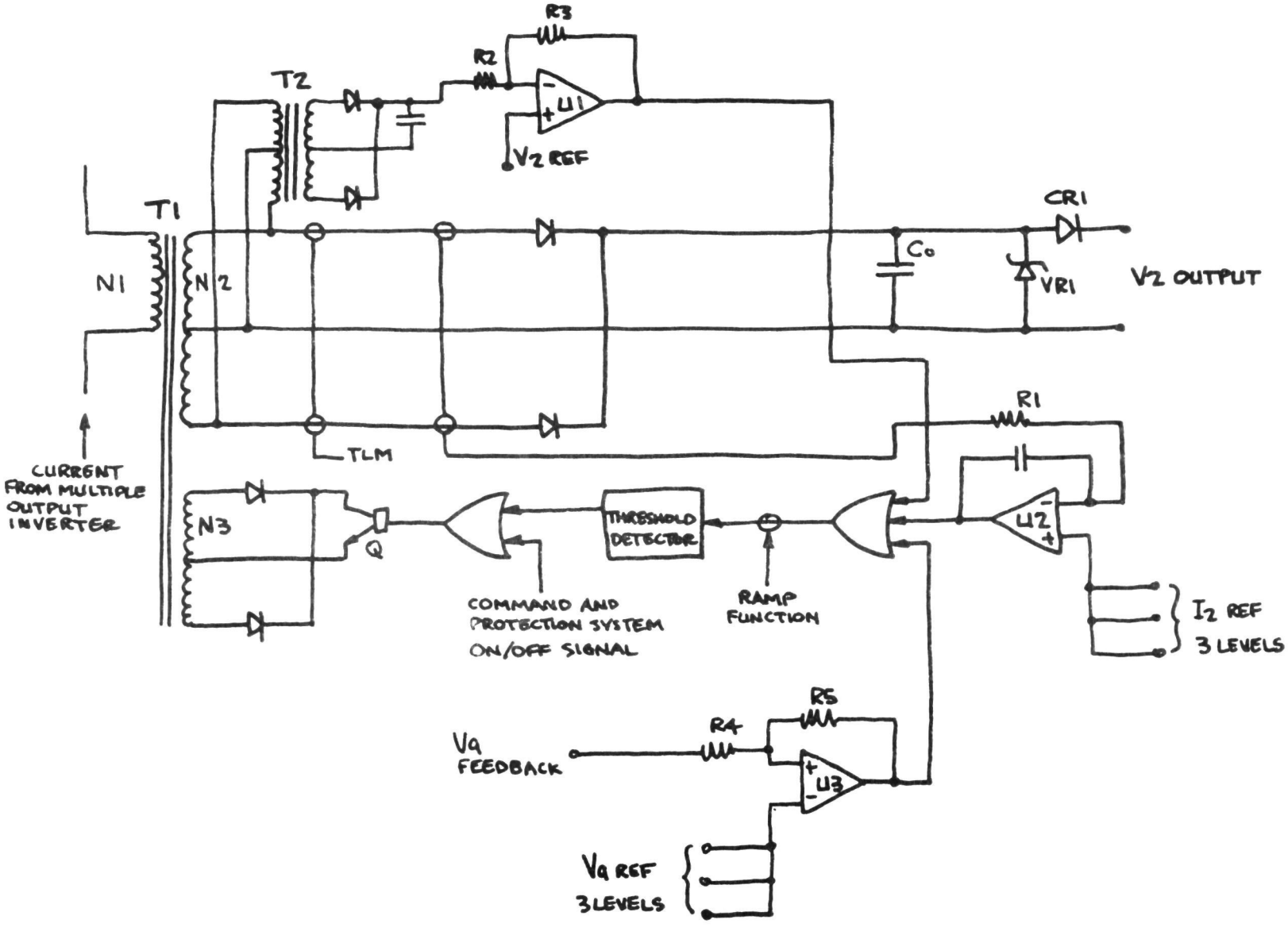


FIGURE B.3. V2, CATHODE VAPORIZER SUPPLY BLOCK DIAGRAM

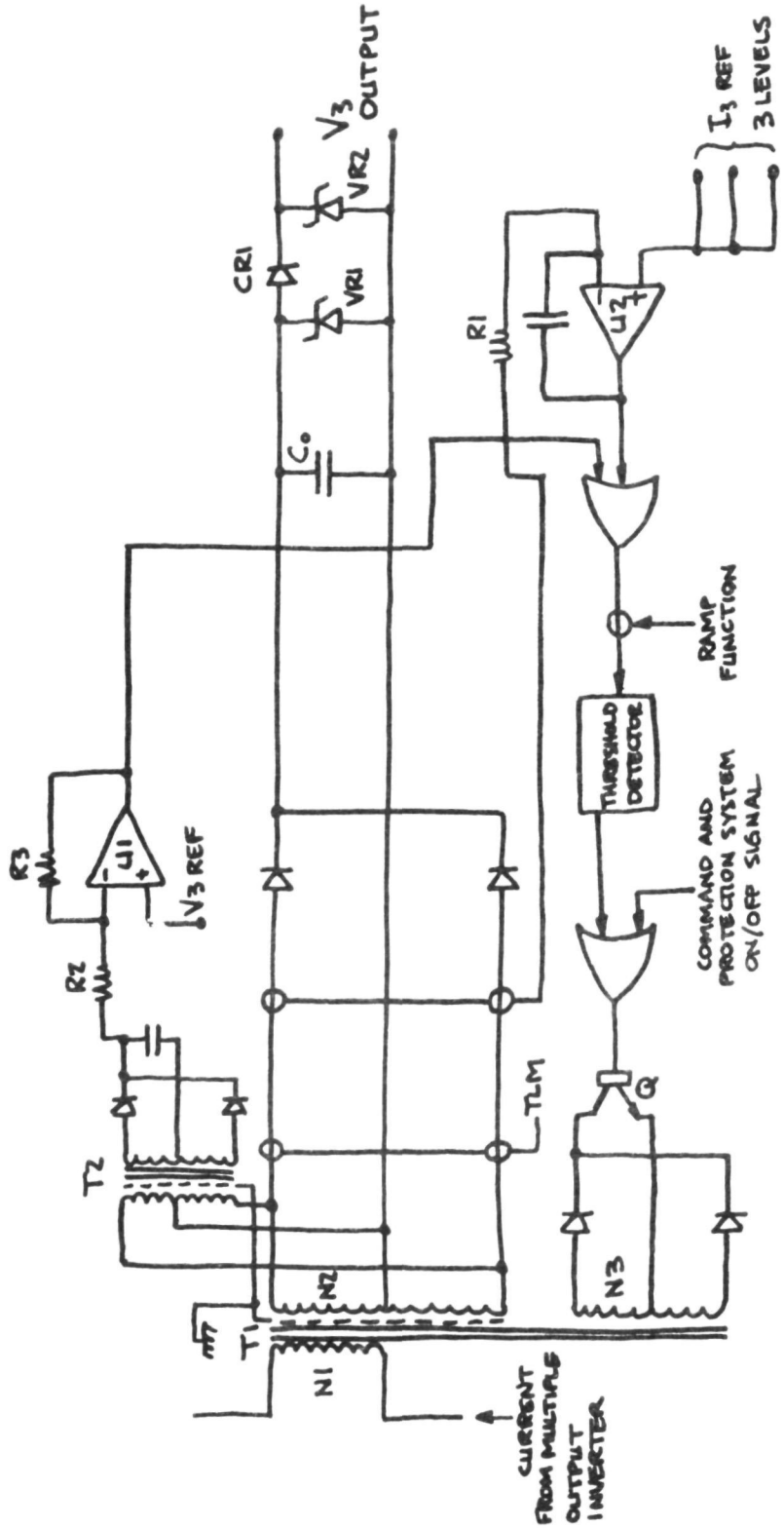


FIGURE B.4 V3, CATHODE HEATER SUPPLY BLOCK DIAGRAM

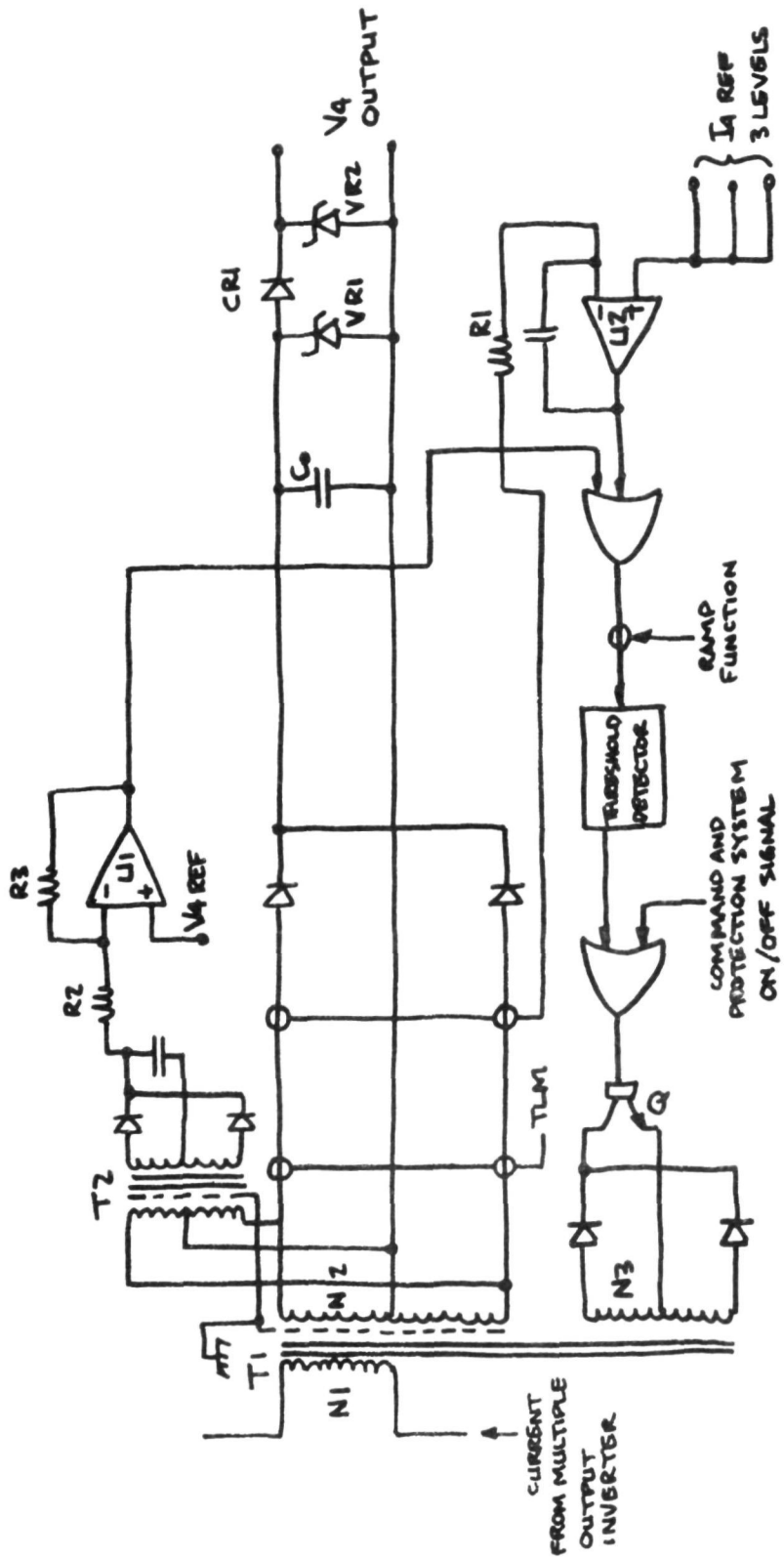


FIGURE B.5 V4, ISOLATOR SUPPLY BLOCK DIAGRAM

B.1.1.5 V5, Neutralizer Heater Supply

Figure B.6 is the block diagram for the V5 supply. Voltage and current limiting is provided with three externally adjustable current limit points. The output of the V5 supply is at neutralizer common which is clamped to spacecraft ground with a zener diode.

Output zener diode VR1 limits the maximum no load output voltage and CR1 protects the output circuitry from overstress during arc over.

B.1.1.6 V6, Neutralizer Vaporizer Supply

Figure B.7 is the block diagram for the V6 supply. The supply has three control loops.

- o V6 voltage limiting by means of T2 and operational amplifier U1
- o I6 current limiting by means of operational amplifier U2
- o V7 voltage control by means of operational amplifier U3.

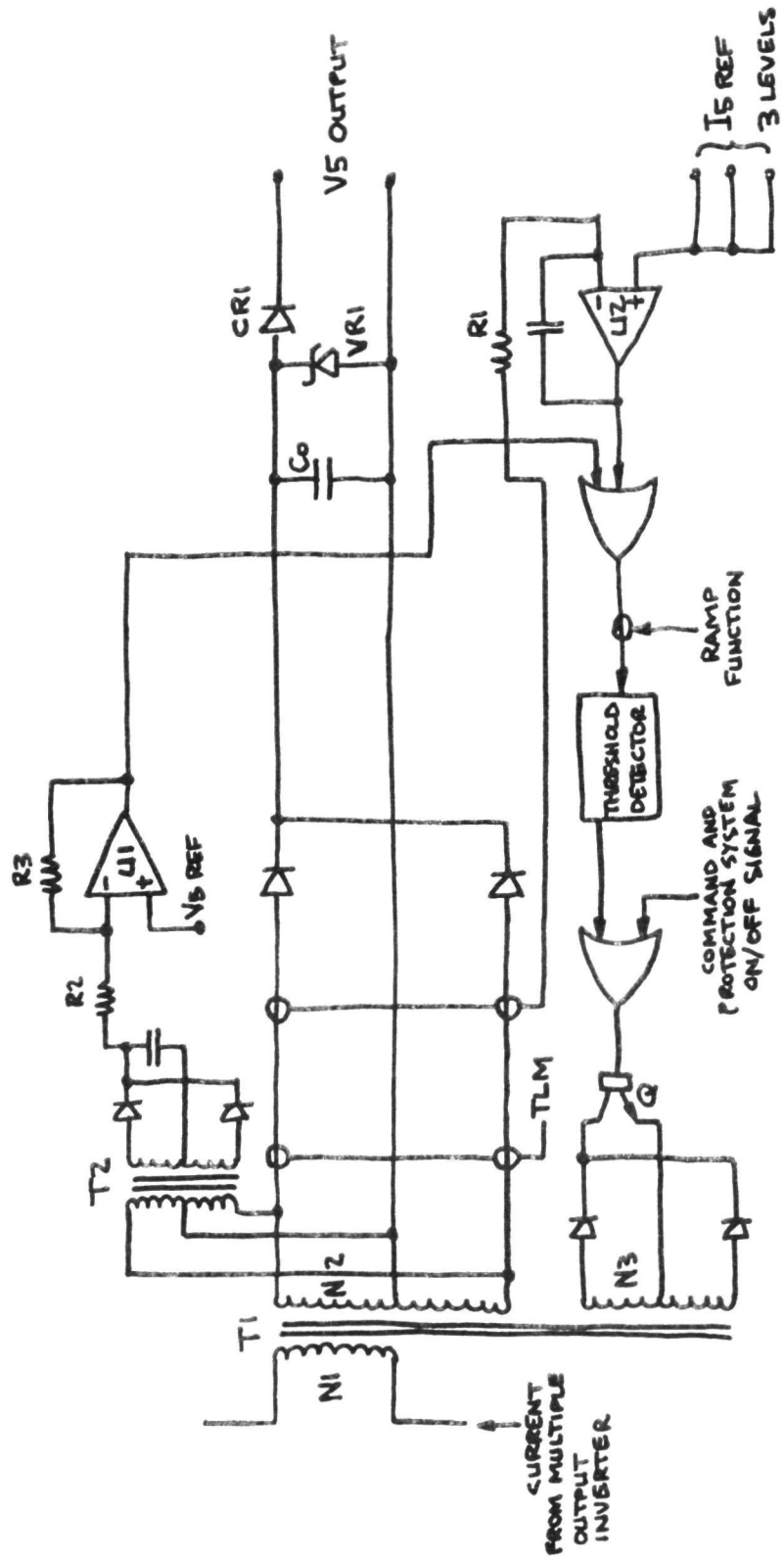
The first two loops control the maximum output voltage and output current. The current limit point is externally adjustable in three discrete steps. The third loop controls the V7 (neutralizer keeper) voltage to maintain stable neutralizer operation. Three external reference points allows variation of the neutralizer keeper voltage.

Output zener diode VR1 limits the maximum no load output voltage and CR1 protects the output circuitry from overstress during arc over of the beam supply.

B.1.1.7 V7, Neutralizer Keeper Supply

Figure B.8 is the block diagram for the neutralizer keeper supply. Constant ac current from the multiple output inverter power stage feeds the primary winding on T1, the main power transformer and T3, the 1000V booster transformer.

During startup, the keeper load impedance is very high and transformer T3 supplies 20mA average current to the output capacitor C1. The output voltage across C1 builds up until the clamp zener VR2 across winding N3 of T3 starts conducting and limits the output voltage at 1000Vdc. Diode CR1 isolates the high voltage from appearing on the 20V output capacitor Co. During turn-on of the keeper supply, the output voltage makes a smooth transfer from the high voltage (1000V) to the low voltage



FIBURE B.6 V5, NEUTRALIZER HEATER SUPPLY BLOCK DIAGRAM

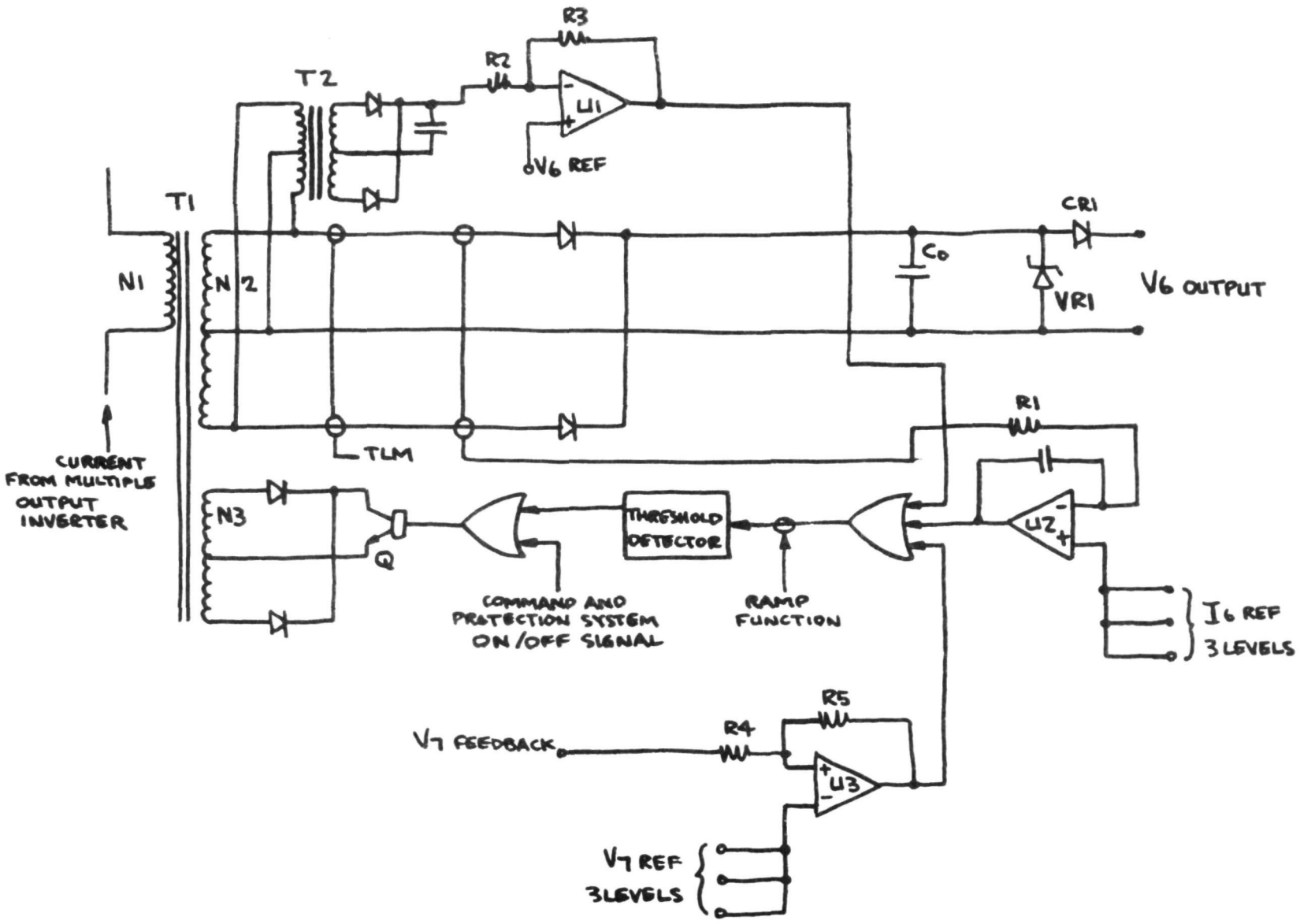


FIGURE B.7 V6, NEUTRALIZER VAPORIZER SUPPLY BLOCK DIAGRAM

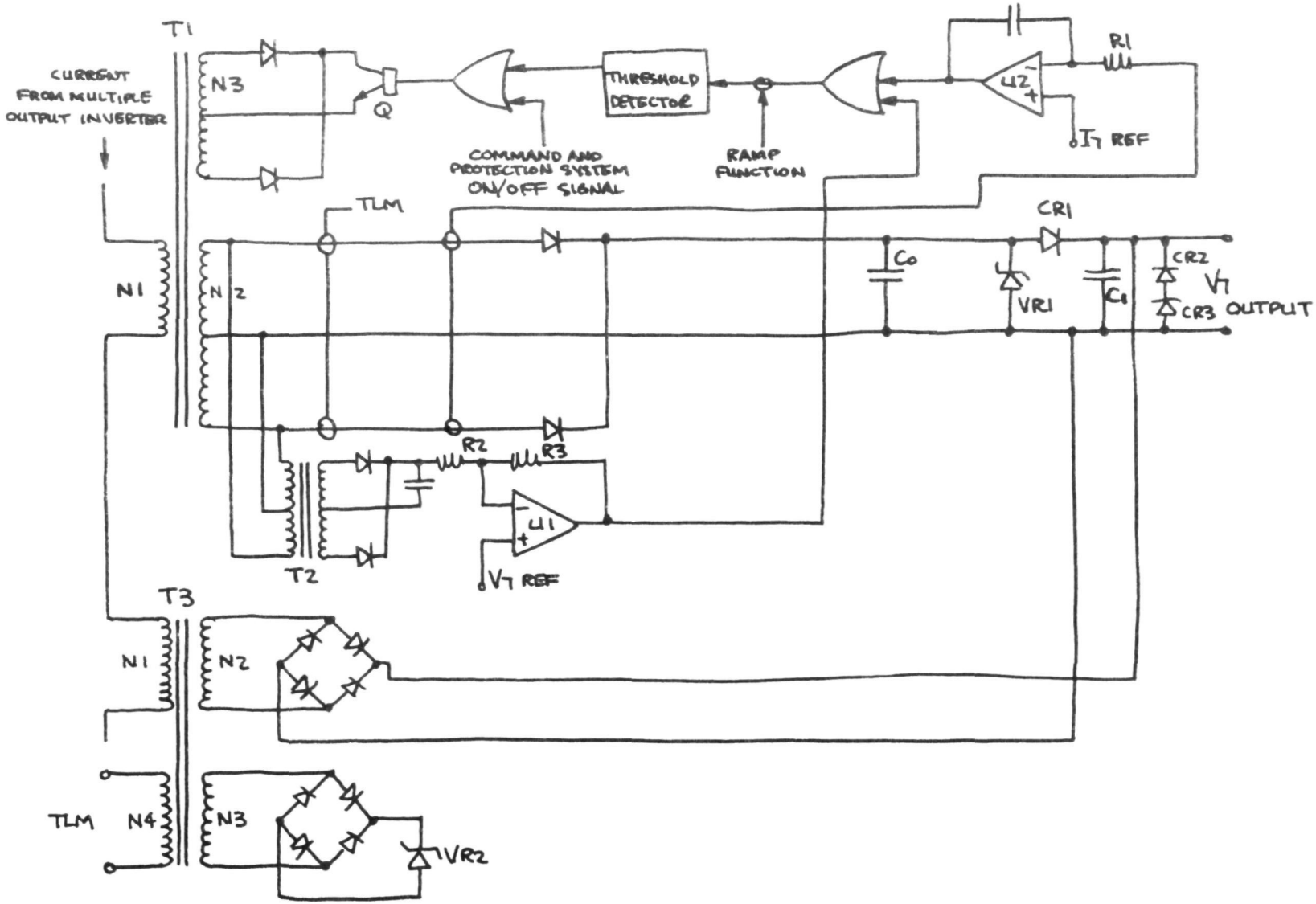


FIGURE B.8 V7, NEUTRALIZER KEEPER SUPPLY BLOCK DIAGRAM

high current (20V state. Diodes CR2 and CR3 are for arc protection.

The control system has two feedback loops:

- o Output current regulation by means of operational amplifier U2
- o Output voltage limiting by means of T2 and operational amplifier U1.

The output of the operational amplifier and ramp function controls the shorting transistor Q to provide the necessary output control.

B.1.1.8 V8, Cathode Keeper Supply

Figure B.9 is the block diagram for the cathode keeper supply. Its design is very similar to the neutralizer keeper supply V7 described in Section B.1.1.7, except that the V8 output must float at the +1.5KV screen potential.

All electronics are at ground potential since voltage isolation is provided by the magnetic voltage and current sensing.

Transformers T1, T2, and T3 have shields between the high voltage winding and the rest of the transformer for isolation purposes.

B.1.1.9 V9, Discharge Supply

Figure B.10 is the block diagram for the discharge supply. Constant ac current from the multiple output inverter power stage feeds the primary winding on T1, the main power transformer and T3, the 60V booster transformer. Output energy flows into winding N2 on transformer T1 and is rectified and filtered by the output filter capacitor Co. Power regulation achieved by the shorting SCR's across winding N2 on transformer T1.

During startup, the discharge load impedance is very high and transformer T3 supplies 20mA current to the output capacitor Co. The output voltage across Co builds up until the output zeners VR3 and VR4 starts conducting and limits the output voltage to 63Vdc. A smooth transfer is made from the high voltage to the low voltage high current state. Power zener diodes VR1 and VR2 limit the maximum no load voltage of transformer T1.

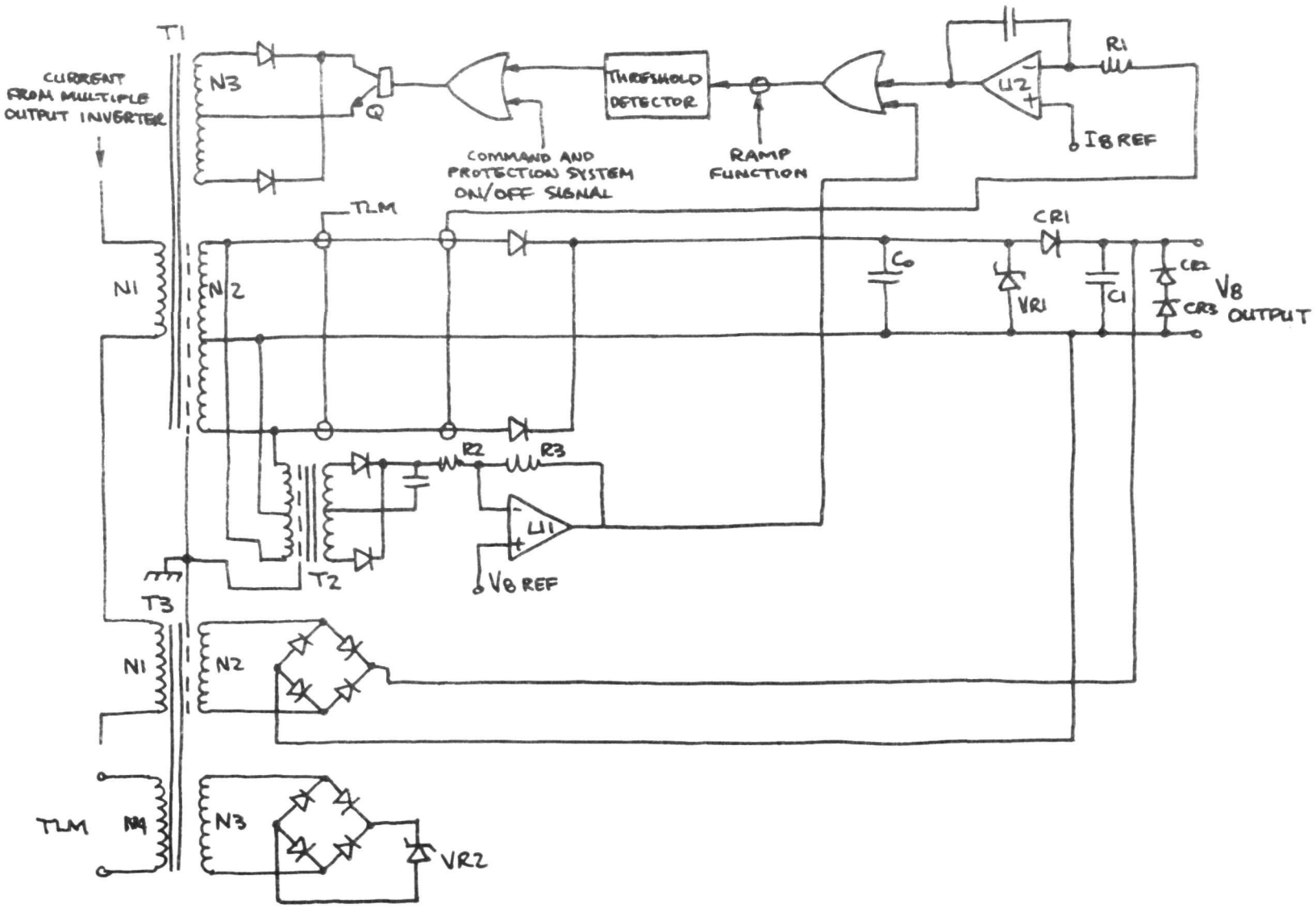


FIGURE B.9 V8, CATHODE KEEPER SUPPLY BLOCK DIAGRAM

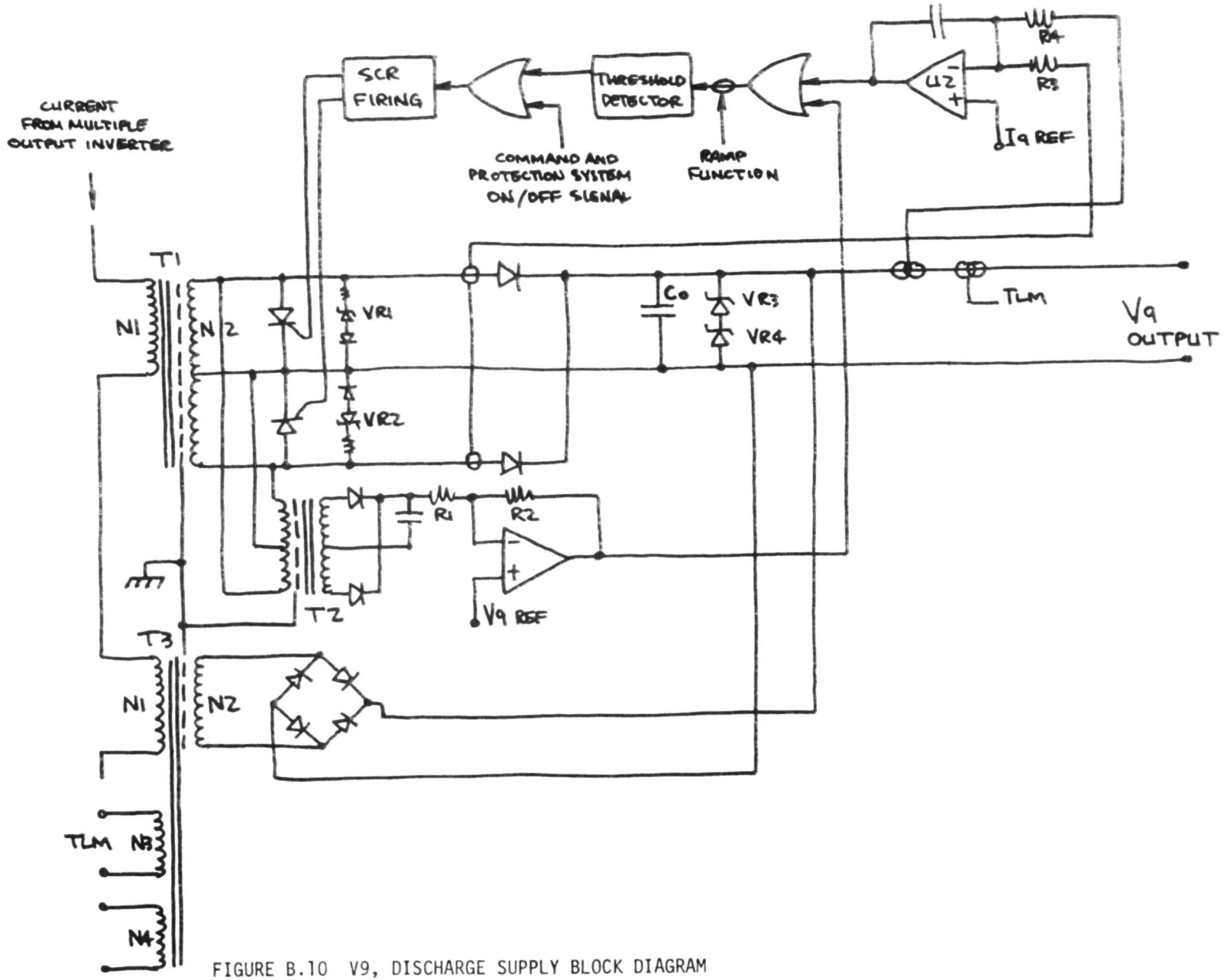


FIGURE B.10 V9, DISCHARGE SUPPLY BLOCK DIAGRAM

The V9 discharge supply has two feedback loops:

- o Output voltage limiting by means of operational amplifier U1.
- o Output current regulation by means of operational amplifier U2.

The first loop limits the maximum output voltage across transformer T1. The external command reference I9 controls the operating point of the discharge supply during steady-state operation. The current regulating loop incorporates the ASDTIC amplifiers for control where the secondary ac current signal is fed into operational amplifier U2, through gain adjusting resistor R3 and the dc output current signal from a two core series connected magnetic amplifier through gain adjusting resistor R4. The dc loop provides the high static accuracy and the ac loop provides regulator stability characteristic and eliminates the time constant in the magnetic current sensing amplifier.

The output of either operational amplifier operates the threshold detector depending on the mode of operation, i.e., voltage or current regulation. The ramp function is added to the output of the operational amplifier to obtain regulator stability when operating in a constant frequency system. The signal then goes to the SCR firing network which provides trigger power to the shorting SCR and also provides output/input isolation since the output of the discharge supply floats at the +1.5KV screen potential and the control electronics are at ground potential.

B.1.1.10 V12, Magnetic Baffle Supply

Figure B.11 is the block diagram for the magnetic baffle supply. Voltage and current limiting is provided with an external command reference I12 controlling the current limit level. The output of the V12 supply is floating at the +1.5KV screen potential. Transformers T1 and T2 have shields between the high voltage winding and the rest of the transformer.

Output zener diode VR1 limits the maximum no load output voltage and CR1 and VR2 protect the output circuitry from overstress during arc over.

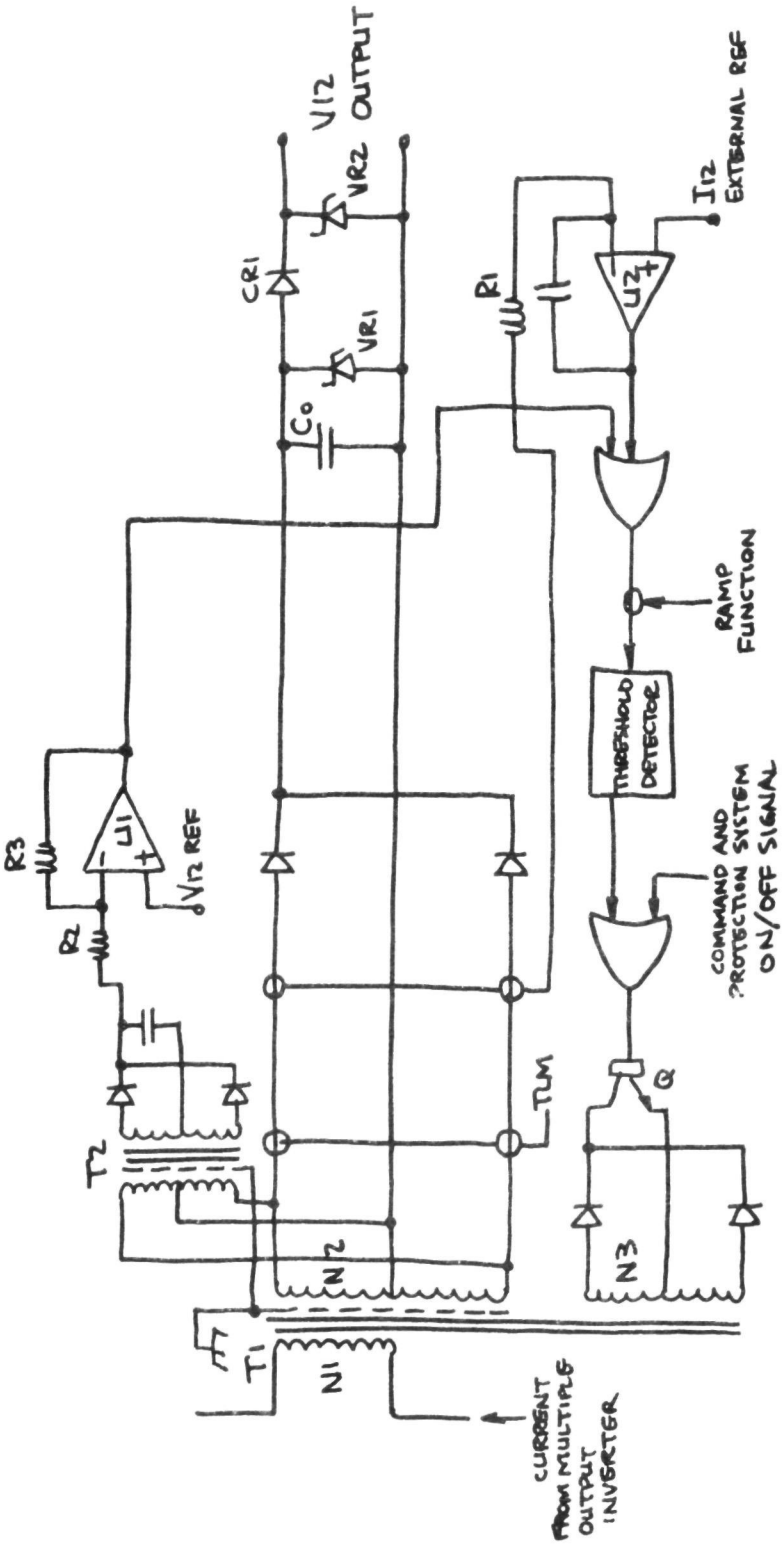


FIGURE B.11 V12, MAGNETIC BAFFLE SUPPLY BLOCK DIAGRAM

B.1.1.11 V_{AUX}, Auxiliary Supply

Figure B.12 is the block diagram for the internal auxiliary power supply. Constant current from the multiple output series inverter passes through the primary winding N1 and feeds all the secondary loads. The power transformer provides power at the different ground returns for the internal loads of the power processor.

The loads are:

1) +15V, -15V, +5V at input power return
2) +15V, -15V, +5V at command ground return
3) +15V, -15V, at output engine ground return.

Voltage regulation is achieved by sensing the +15V output and controlling shorting transistor Q across winding N2 by operational amplifier U1.

B.1.1.12 Ramp Generator

In a constant frequency system, it was found that an inherent instability was caused by an increase of the B/M ratio, where B is the average load current, and M is the peak current. It was found that, when the ratio reaches beyond a certain critical value, the regulated system becomes unstable. A means of modifying the system and improving the stability was accomplished by adding another ramp function to the existing integrator ramp during the on-time.

B.2 Screen Current-Main Vaporizor

In order to improve the accuracy of the ion engine thrust, the accuracy of both the screen voltage and screen current must be held to very tight tolerance.

The Analog-Signal-to-Discrete-Time-Interval-Converter (ASDTIC) control system has been adapted to the regulation of the beam output voltage.

Figure B.13 illustrates the mechanization of the ASDTIC control system to the screen current-main vaporizer control. In this configuration the screen current is the main feedback loop. The energy, being delivered to the main vaporizer, forms the high frequency ac loop. By utilizing the ASDTIC control principle, tight control of the screen current is possible.

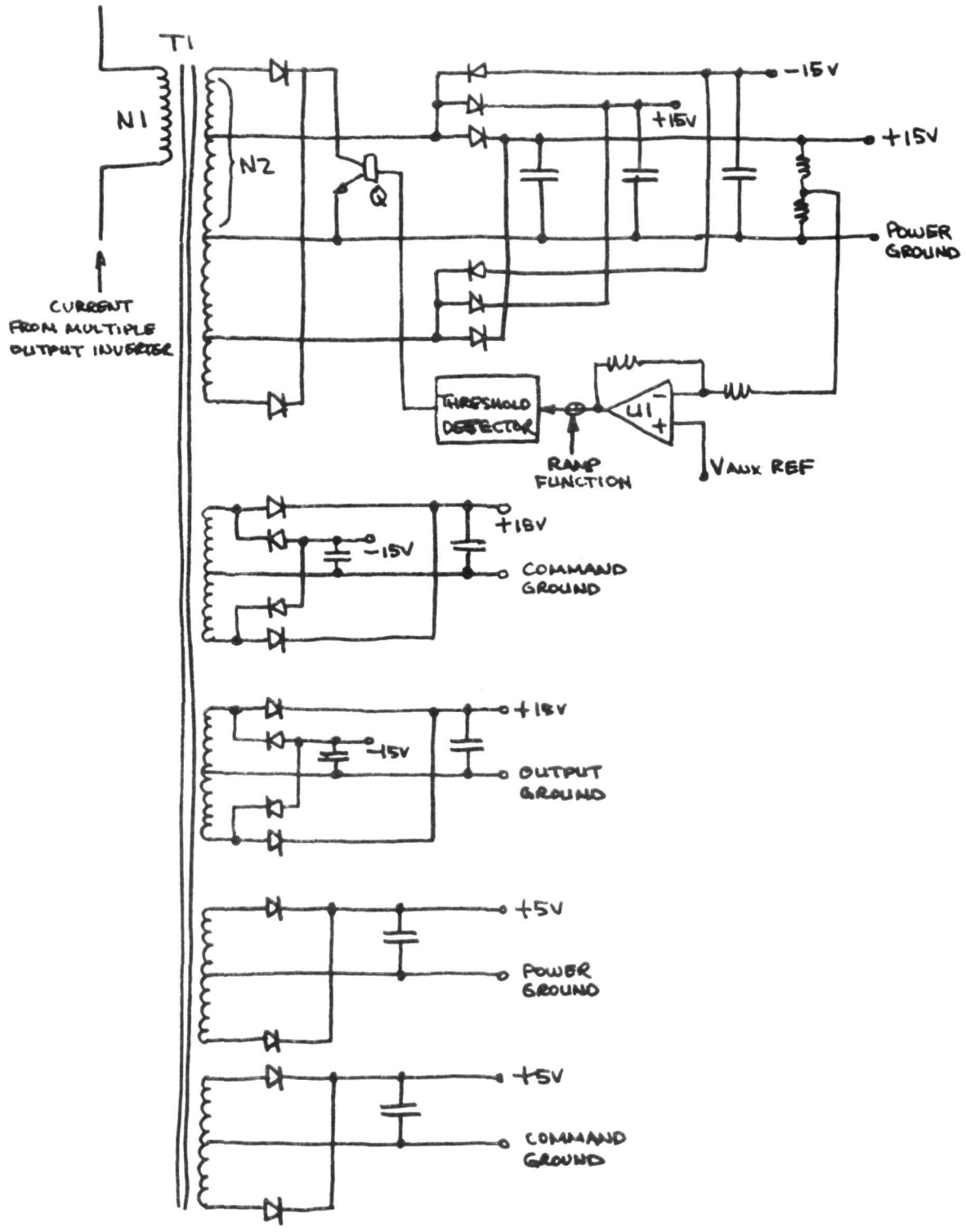


FIGURE B.12 VAUX SUPPLY BLOCK DIAGRAM

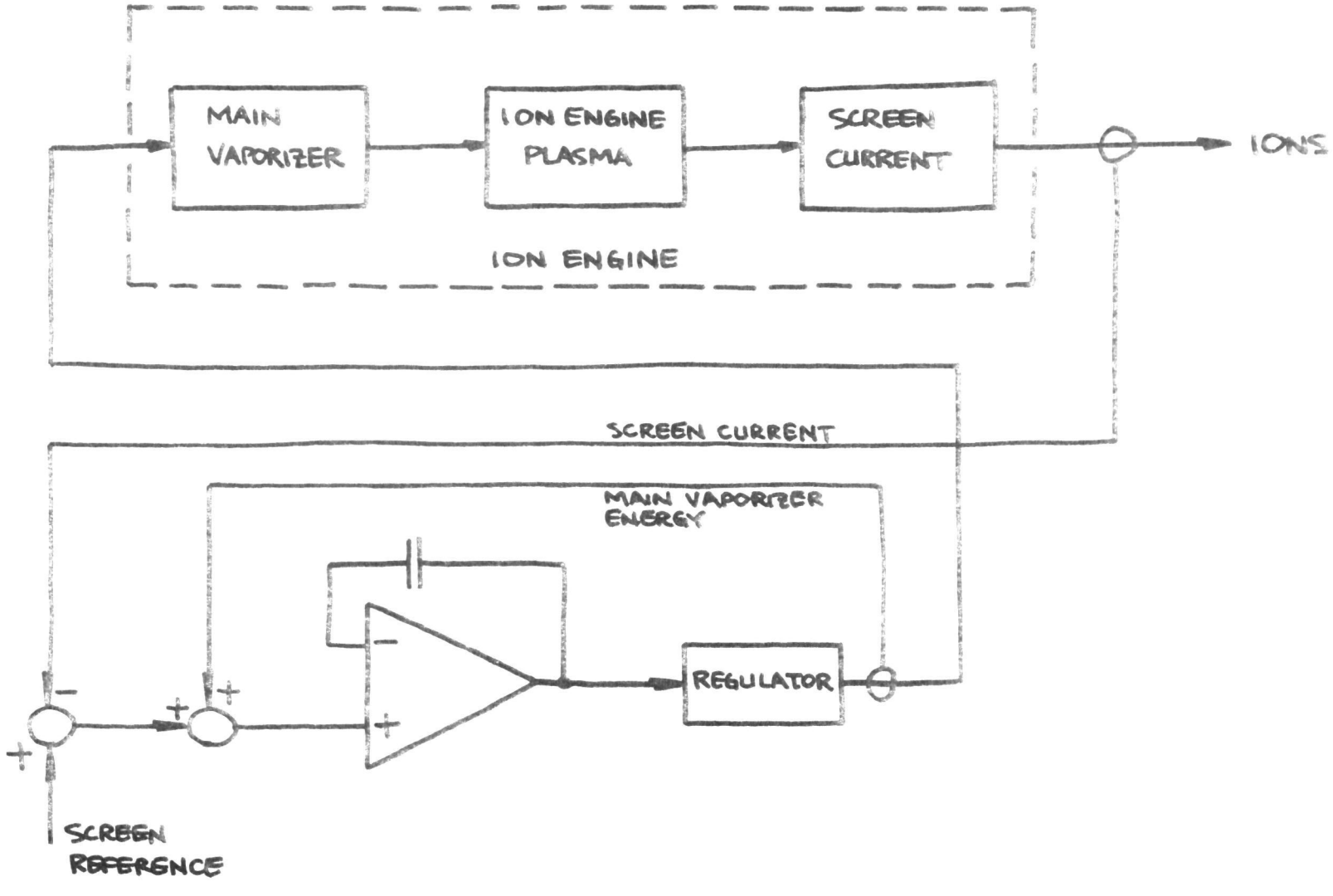


FIGURE B.13. SCREEN CURRENT-MAIN VAPORIZER CONTROL LOOP BLOCK DIAGRAM

B.3 Screen (V11) and Accelerator (V10) Supply

The screen and accelerator supply obtains its power from a SCR series resonant inverter. The configuration of the inverter is identical to the multiple output inverter with the exception of different L and C values.

Figure B.14 is the block diagram for the V10 and V11 power supplies. Both high voltage outputs are cimbined into a single power stage in order to reduce overall part count. The current flowing through transformer T1 when the SCR's are conducting develops a voltage which is rectified, filtered and delivered to the load. Regulation is achieved by sensing the V11 output and then controlling the repetition rate of the SCR's. Output current limiting resistors RL1 and RL2 control the peak current that can flow from the output filter capacitors C1, C2 and C3. The limiting resistors not only limit the peak discharge current but also control the transient voltage that can appear on the cabling to the engine and the separation of the output ground from the engine ground during transients.

The screen/accelerator supply has two regulating loops in addition to a series regulator for the accelerator output.

- o V11 output regulation by means of operational amplifier U1.
- o I_{10} overload control by means of operational amplifier U2.

The voltage regulating loop incorporates the ASDTIC control system to maintain output regulation accuracy and regulator stability. The dc loop senses the V11 output voltage and the ac loop senses the stored energy in the output capacitor C1 by means of a current transformer. The I_{10} overload control comes into action during shorts on the V10 output and protects the N3 winding from damage since N3 is designed to pass only 200mA instead of 2.2A which is the total capacity of the series resonant inverter. The output signals from the operational amplifiers control the threshold detector, the input/output ground isolation circuit,

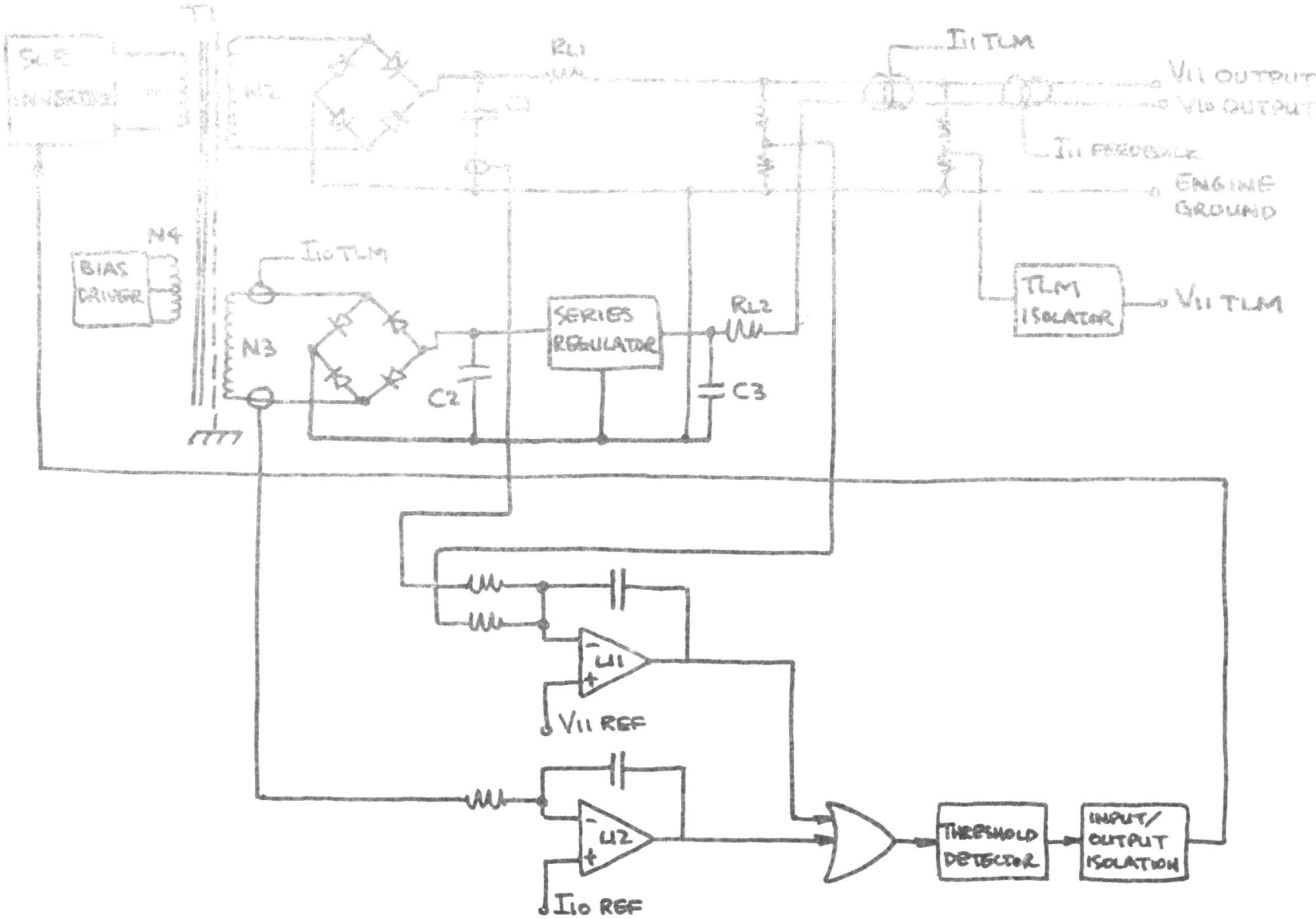


FIGURE B.14. V10, V11 ACCELERATOR AND SCREEN SUPPLY BLOCK DIAGRAM

and the control logic for the SCR series inverter. The input/output ground isolation separates the output ground return from the input power ground return for the SCR series inverter control logic.

Since the output voltage of V11 is variable from 1100Vdc to 1500Vdc, a series regulator was incorporated into the -1000Vdc supply. The series regulator is short circuit protected by the fact that it is driven from a current limited source.

B.4 Input Filter

The input filter design consists of a two-stage LC network for filtering the high ac current drawn by the inverters to 1% rms of the maximum input average dc current. A common input filter is used to reduce the total filter weight of the power processor. Minor cross coupling exists between the two inverters because of the common input filter, however, the regulator action of the two inverters will eliminate this modulation from appearing in the output loads and the input filter will attenuate the cross coupling signal to less then 1%. The input filter schematic is shown in Figure B.15.

B.5 Command and Protection

The command and protection circuitry of the power processing unit provides all the necessary commands for startup and shutdown of the processing unit. It also provides automatic recycling of the power processor in the event of any arcs that occur within the thruster or between the thruster and the facility ground. The block diagram of the command and protection system is shown in Figure B.16. The power processor is shutdown when an out of tolerance condition exists on the 200 to 400Vdc input bus or the internal +15V bus. The fault clearing system for the power processor comes into play when an overload on the beam or accelerator current is sensed and if the overload persists for a finite time, then the main vaporizer is turned off and the arc current reference is cut back. After a set delay, the outputs are recycled back on and the inverter is allowed to return to normal operation.

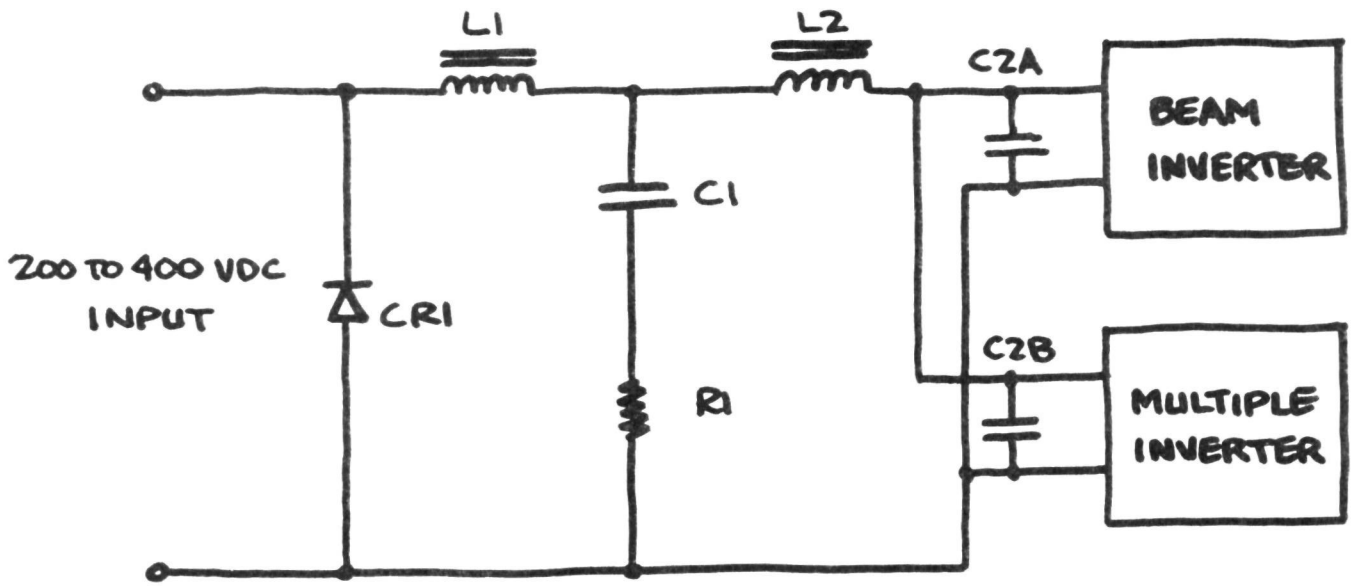


FIGURE B.15. INPUT FILTER BLOCK DIAGRAM

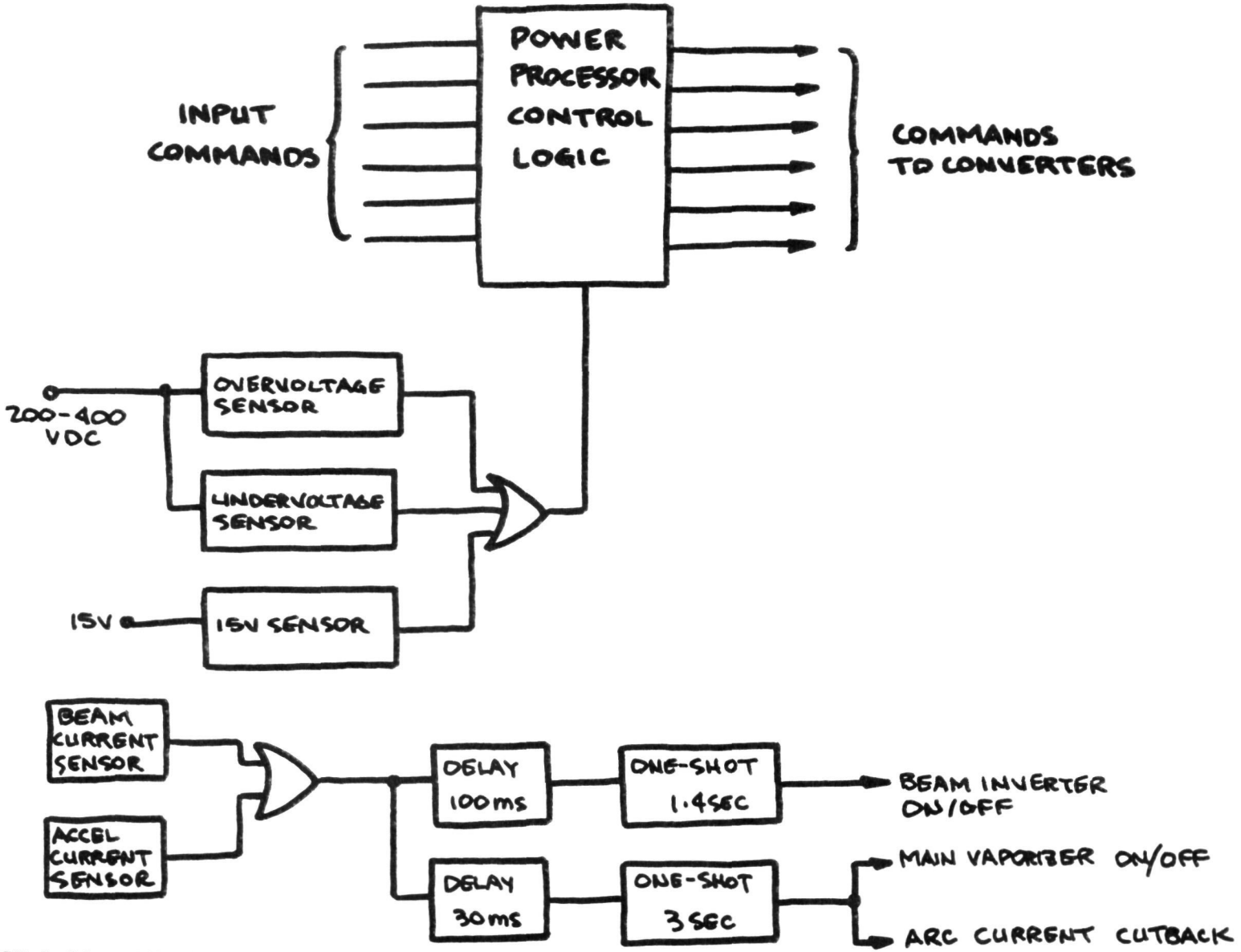


FIGURE B.16. COMMAND AND PROTECTION SYSTEM BLOCK DIAGRAM

B.6 Digital Interface Units

The digital interface unit is designed to transfer 16 bit digital words between a computer and the power processor. The input and output data from digitized command and telemetry unit will be in 16 bit serial or parallel format where the first 6 bits will be the address or identification and the last 10 bits will be data either input analog commands, on/off commands, or input data and analog data from the telemetry monitors. Figure B.17 shows the block diagram of the digital interface unit for the 30CM Ion Engine Power Processor. The digital interface unit is broken down into two major sections, the command unit and the telemetry unit. In the command unit, 16 bit words are shifted into a shift register and from there, they go to the address decoder, D-A converters and the command decoder. The address decoder decodes the first 6 bits and commands the locations for the remaining 10 bits. The command decoder decodes the power processor ON/OFF commands and the discrete reference signal commands. The D-A converters transform the 10 bit digital signals to analog voltage and current reference signals. The resolution of the analog reference is one part in 2^{10} or one part in 1024 or $\pm$ .098%.

The second section of the ditigal interface unit is the telemetry unit. A solid state analog switch is used to commutate the telemetry channels. The output of the analog switch goes to an A-D converter and then to the telemetry sequence unit where an address is assigned and then to the telemetry sequence unit where an address is assigned and then to the shift register which outputs the data to the computer. For high accuracy data, a 8 bit data word is assigned providing a resolution of one part in 256 or $\pm$ 0.39%. The low accuracy data is subcommutated which means that two additional bits would be used for the subcom address and six bits for data. The accuracy of the data is one part in 64 or $\pm$ 1.56%. The high accuracy data channels are I9 (discharge current), V9 (discharge voltage), I11 (screen current), V11 (screen voltage). All the other telemetry channels are low accuracy data channels.

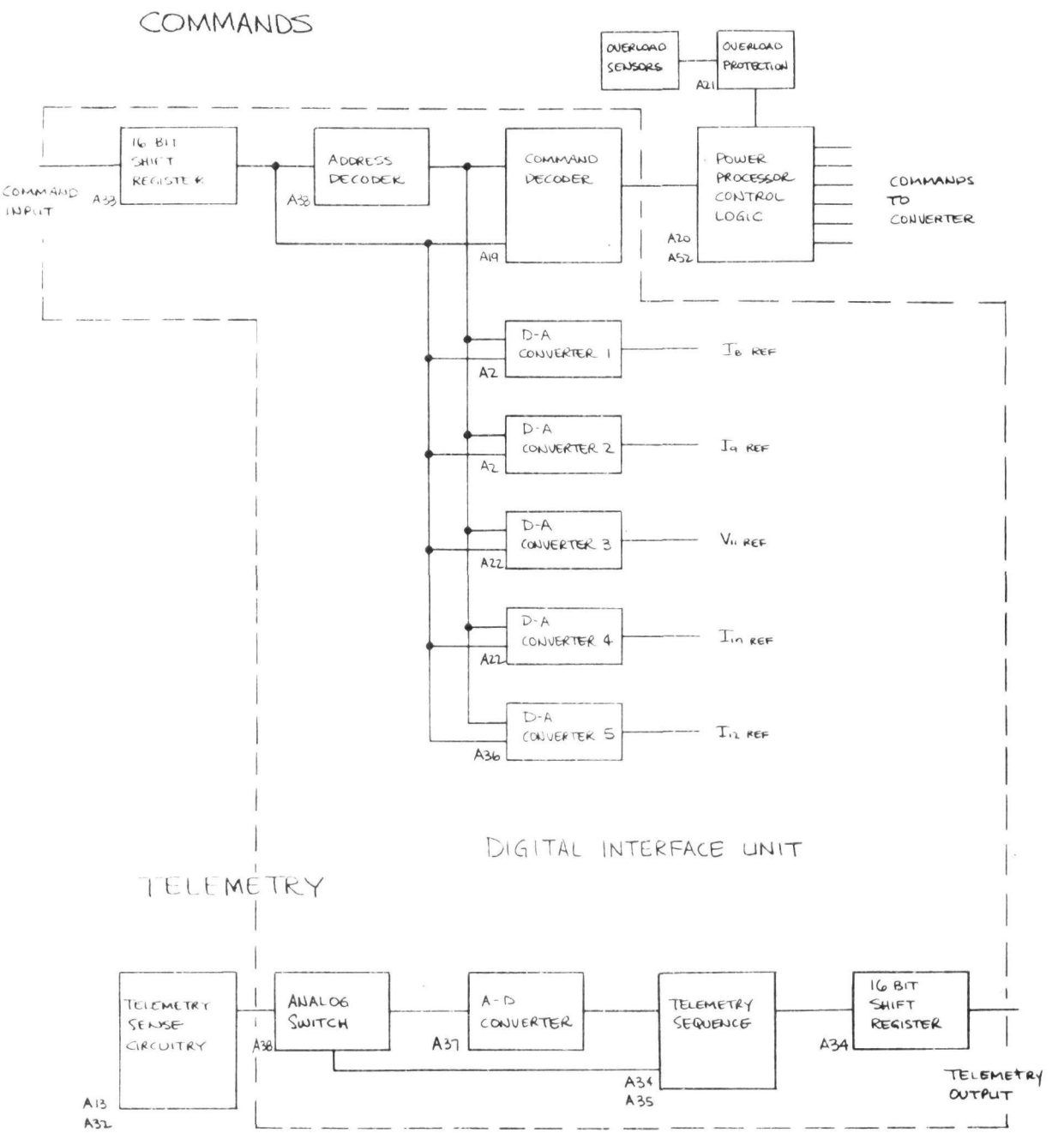


FIGURE B.17. DIGITAL INTERFACE UNIT BLOCK DIAGRAM

B.7 2.41kHz Auxiliary Supply

Figure B.18 is the block diagram for the 2.41kHz auxiliary housekeeping power supply. This supply is required to power the digital interface unit and the command and protection unit when the power processor inverters are not turned on. The power for this supply comes from a 2.41kHz, 50V rms squarewave voltage. A current limiting stage is incorporated before the power transformer to limit input current to 1A for protection of the 2.41kHz power bus.

The outputs of the 2.41kHz power supply are connected in parallel with the internal auxiliary power supply. When the internal auxiliary supply is on, no power is drawn from the 2.41kHz supply.

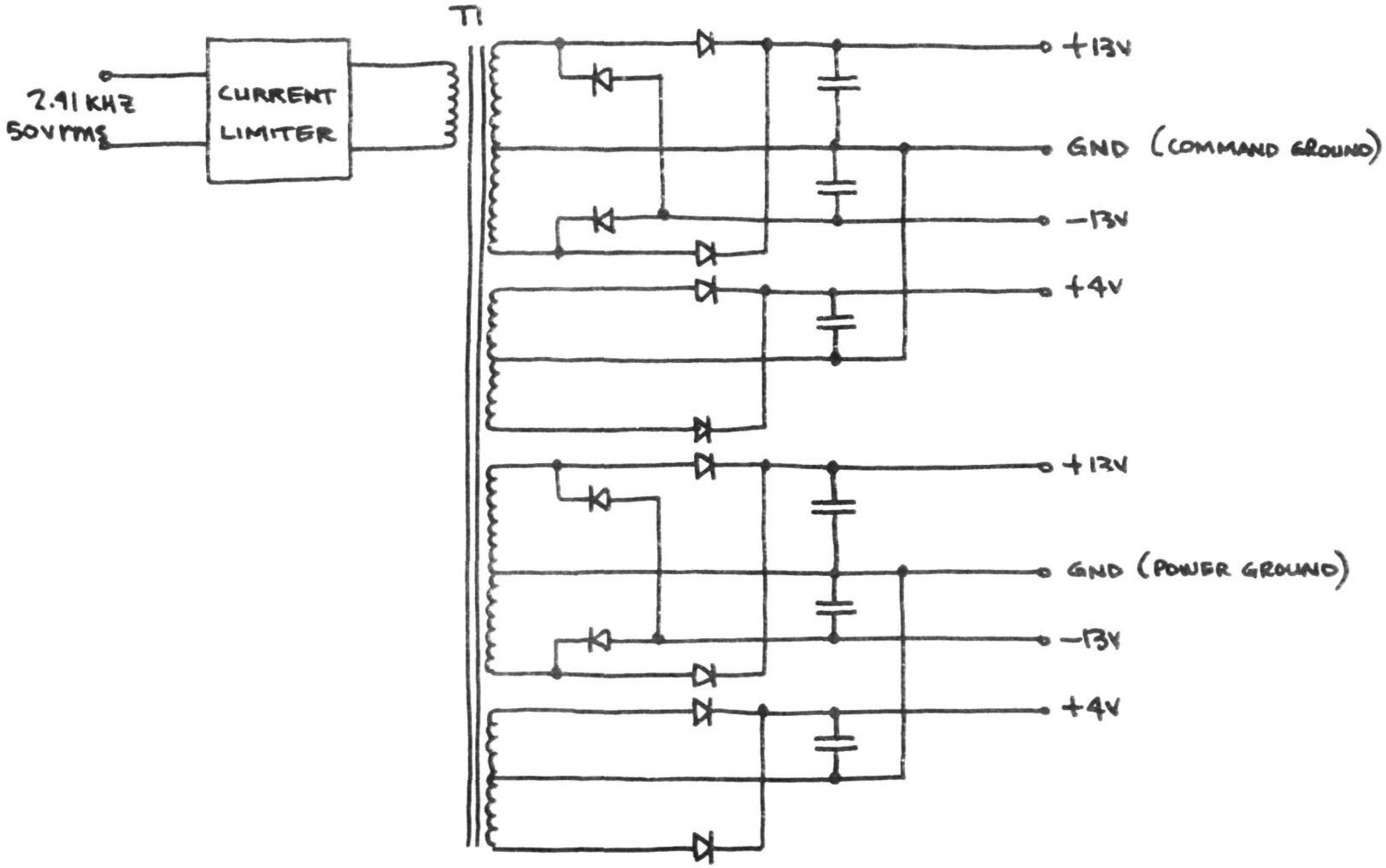


FIGURE B.18 2.41KHZ AUXILIARY POWER SUPPLY BLOCK DIAGRAM

APPENDIX C

C. Mechanical Design of 30CM Ion Thruster Power Processor

C.1 Thermal Vacuum Breadboard Mechanical Design

The 30cm ion engine power processor breadboard mechanical design includes the following features:

- Operation in a thermal vacuum environment
- Separation of control circuit, power circuits and high voltage circuits
- Grouping of control circuit components into removeable modules for maintainability and tests
- Layout of power components and component mounting procedure to minimize component temperature rise
- Separation of signal lines from power lines for noise isolation
- Easy removal of digital interface unit
- Separate input and output connectors providing isolation of functions
- Packaging technique to control electromagnetic conducted and radiated interference

The size of the baseplate has been selected to control the maximum baseplate temperature to 140°F. The minimum temperature is controlled by spacecraft louvers and no heater has been incorporated in the power processor design.

No attempt has been made in the mechanical design to demonstrate packaging weight penalties and to demonstrate meeting shock and vibration control.

C.2 Mechanical Layout

Figure C.2-1 shows the mechanical layout of the power processor. Its overall envelope dimensions are 145cm (57 in) x 66cm (26 in) x 13.6cm (5.38 in) high. The unit is designed to operate in a thermal vacuum environment.

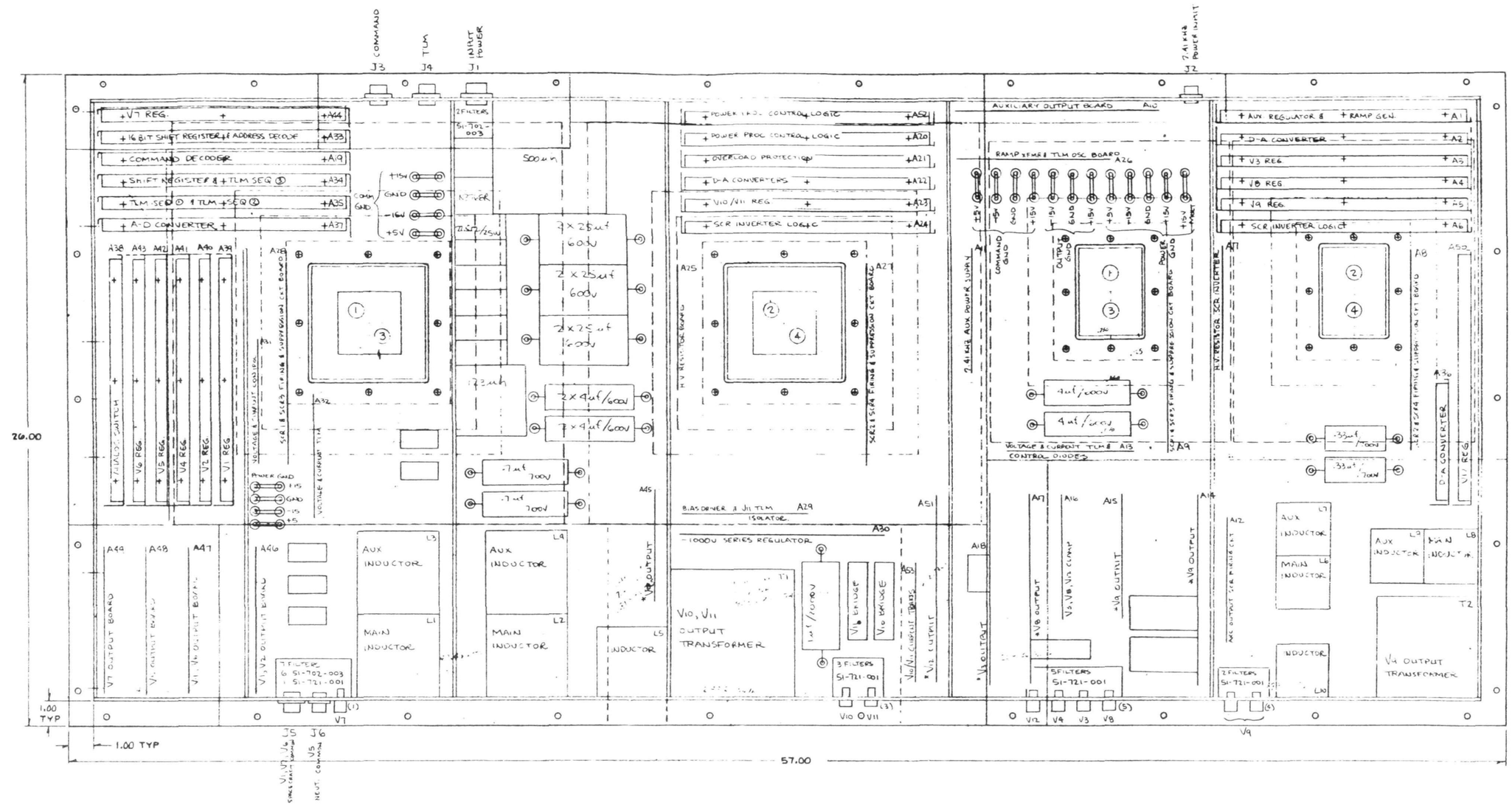
The breadboard was layed out in such a fashion so as to optimize the power flow from input to output, to separate the high voltage circuitry from the low voltage circuitry, to determine optimum grouping of components so that noise coupling from the high power circuitry to the control circuitry would be minimized and to determine the interwiring between functions.

The baseplate of the unit is a sheet of 60 mil aluminum 57 in long by 26 in wide. A rib one inch in from the edge is welded completely around bhe baseplate to give it structural rigidity. The outside rib is also used to mount the input and output connectors to the power processor. Five cross-ribs are welded onto the baseplate to give additional rigidity for the center of the baseplate.

The input power comes into the input filter area at the top of the baseplate through connector J1 and then into the beam supply inverter. The multiple output inverter is on the right side of the breadboard. All of the output circuitry is located near the bottom of the breadboard close to the output connectors. The high voltage outputs are on the right side and the low voltage outputs are on the left side of the power processor breadboard. The low level control cards are mounted near the top and left side of the breadboard away from the high power circuitry which is located near the center and bottom.

Figure C.2-2 shows a typical output board. This board is for an output referenced at engine ground. The aluminum plate acts as a heat sink to conduct the heat dissipated by the power components on the board to the baseplate where it is radiated.

Figure C.2-3 shows an output board where the output is referenced at the screen potential. The components mounted on the board are isolated with beryllium oxide washers for high voltage insulation. The output board itself is further isolated from the baseplate by the use of beryllium oxide insulators.



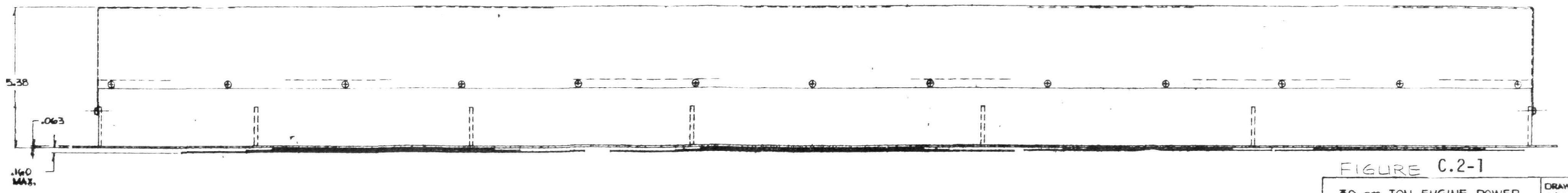


FIGURE C.2-1

30 cm ION ENGINE POWER PROCESSOR THERMAL VACUUM BREADBOARD LAYOUT

SCALE: 1/2

DRAWN: W. Kennedy

FIGURE C.2-2 OUTPUT BOARD (OUTPUT AT GROUND REFERENCE)

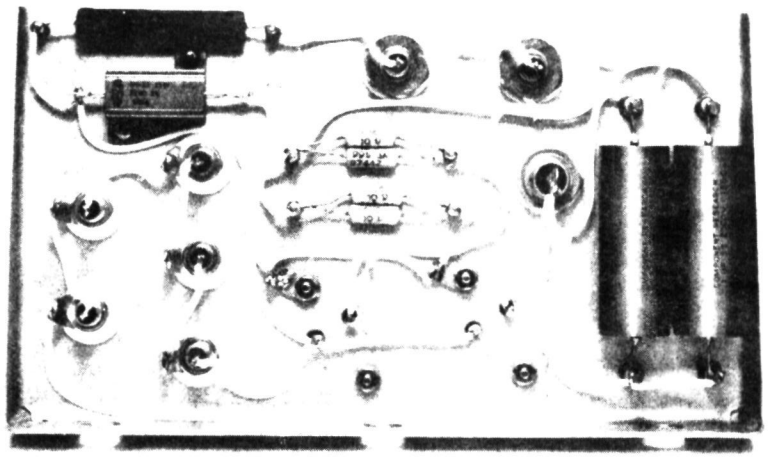


FIGURE C.2-3 OUTPUT BOARD (OUTPUT AT SCREEN POTENTIAL)

C.2 Mechanical Layout (Cont'd)

Figure C.2-4 shows a photograph of the power processor breadboard. Fabrication has not been completed but most of the control cards have been mounted. Also shown is the control signal cable elevated from the baseplate. The output connectors are mounted on the rear panel shown.

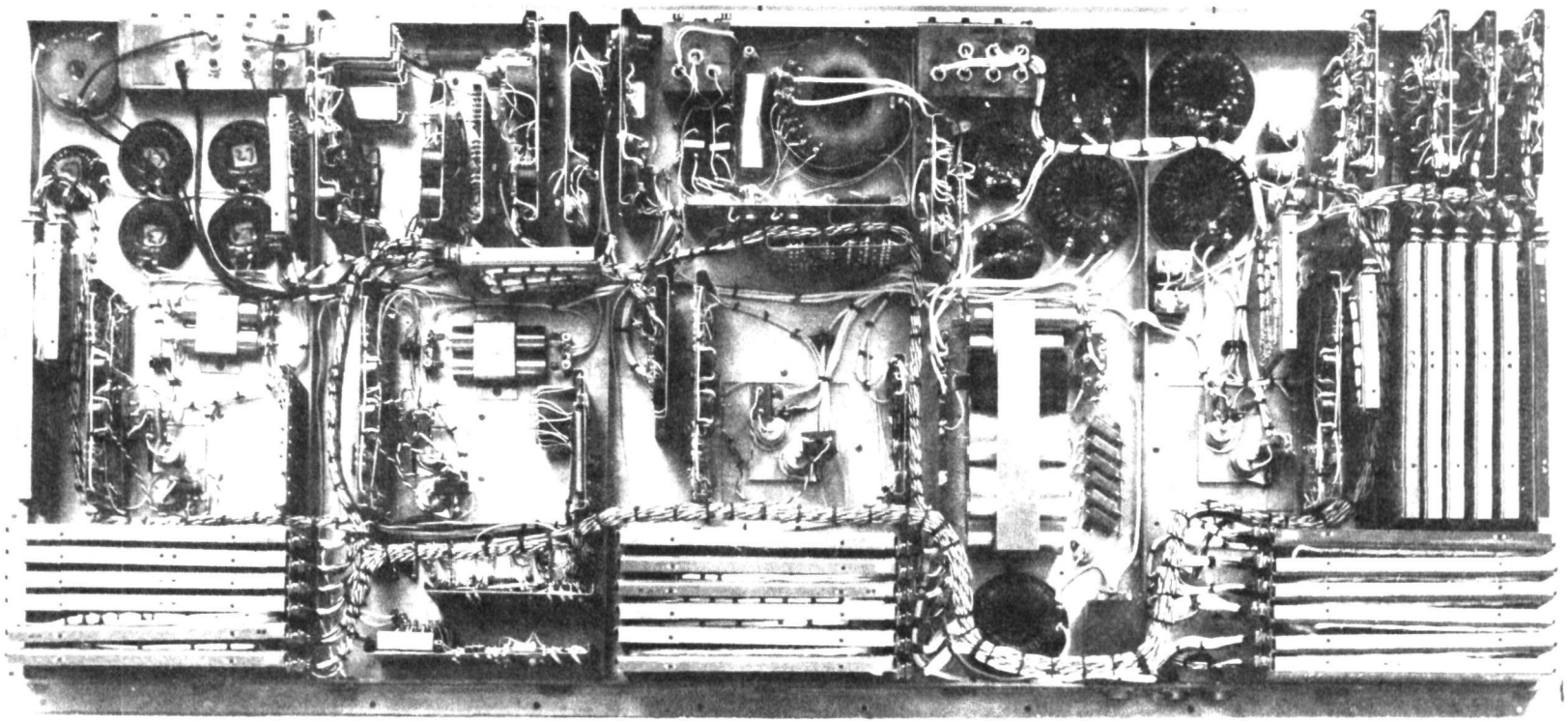


FIGURE C.2-4 30cm POWER PROCESSOR BREADBOARD

C.3 Control Electronic Cards

The control electronic cards are fabricated on 5 in x 10 in and 5 in x 5 in assemblies with Cannon D type connectors for easy removal. An aluminum frame around the card provides a means for mounting the assembly to the baseplate and also provides mounting for the Cannon connector. Two types of control cards were fabricated. Printed circuit cards were used where circuit commonality enabled several cards of one type to be used i.e., the inverter logic cards and all the output regulator cards. The output regulator cards were made for the worst case and parts deleted in the construction of the board for a particular regulator. Figure C.3-1 shows a typical printed circuit card, in this case an inverter logic card. Where there was no commonality, hard wiring was used to fabricate the cards. The control logic and digital interface cards were constructed in this manner. Figure C.3-2 and C.3-3 are typical hard wired cards.

On both the printed circuit cards and the hard wired cards, sockets were used for all integrated circuit chips for ease of replacement. In addition all of the transistors on the hard wired cards are mounted in sockets.

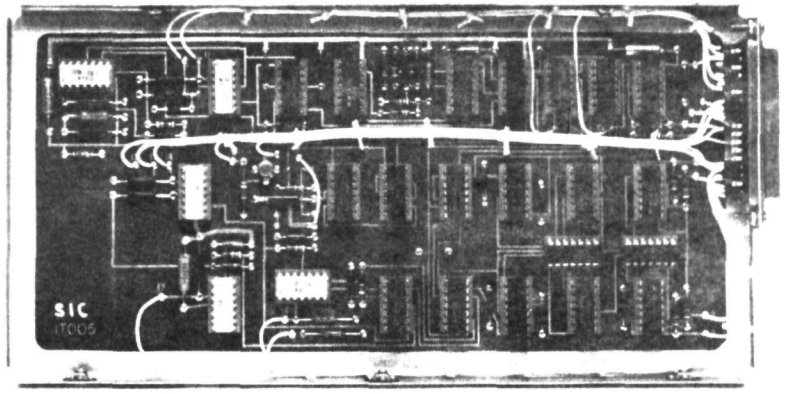


FIGURE C.3-1 PRINTED CIRCUIT CONTROL CARD

FIGURE C.3-2 HARD WIRED CONTROL CARD 5 in X 10 in

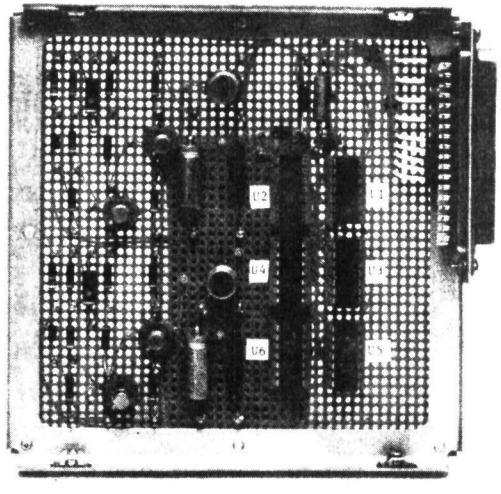


FIGURE C.3-3 HARD WIRED CONTROL CARD 5 in x 5 in

C.4 Thermal Control

The 30 cm Ion Engine Power Processor Electrical Breadboard has a power dissipation of 570 watts. Due to this high dissipation, a thermal control study had to be made to assure that the electronic components in the unit operated at a reasonable temperature. The unit was designed to operate in a thermal vacuum environment. The principle means of heat transfer is by means of thermal radiation to a simulated deep space environment (a cyrogenic Liquid Nitrogen tank). The baseplate was sized to have an adequate surface area to radiate away the 570 watts. The circuit cards and components are distributed so that the power dissipation is spread over the baseplate. The placement of components and cards was a trade-off between the electrical circuit requirements and the thermal dissipation requirements. Also certain critical components were looked at in detail.

All of the heat transfer was assumed to be out of the bottom of the Breadboard baseplate. The bottom surface of the baseplate is painted flat black to improve the aluminum surface emissivity. Fig C.4-1 is a plot of the surface area versus the average baseplate temperature. The baseplate has a surface area of 10.3 square feet, therefore, from Fig C.4-1 the average baseplate temperature is 140° F. This is a reasonable baseplate temperature because most spacecraft have platform temperatures of between 120 F and 160 F. Therefore, the baseplate size of 57" X 26 X .040 thick appears to be adequate to handle 570 watts of dissipation.

In order to minimize the temperature gradients in the baseplate, care was taken in locating circuit cards and critical high dissipating components. The baseplate was divided into areas allocated for various functions. The size of the area is a function of the power dissipation. The area allotted per watt was between 2.5 and 3.0 sq. in. per watt. The variation is due to that fact that some of the areas are shaded by the radiation fins for the SCR's. The power dissipation distribution is shown in Fig C.4-2

Certain critical components were analyzed in detail. These were the high dissipating SCR's and the magnetics. The SCR's are dissipating approximately 50 watts and 80 watts. The dissipations of the magnetics varied from 6 watts to 35 watts.

The eight critical SCR's are mounted in pairs. They are designed to operate at a 230° F (110° C) under the worst case. The Beam SCR's (2 pair) were designed for a worst case dissipation of 80 watts. The SCR's in one locale may be dissipating 40 watts each, or one may be dissipating 80 watts while the other is not operating. Although the total dissipation in one spot on the heatsink are the same, obviously, the worst case is when only one of the SCR's is on. This case will place the highest stress on one SCR. The junction to case temperature drop is 36 F. The mounting temperature drop with a BeO washer and a trucast interface is 27 F. Therefore, the radiating fin for the SCR pair had to be designed to have a 167 F temperature under the SCR's. A computer program was set up to obtain the required thickness of the heatsink. For analysis, the fin was assumed to be radial and tapered. The results of the analysis is shown in Fig C.4-3. A similar analysis was done for the multiplier inverter SCR's (2 pair) which were designed for 50 watt dissipations. The results are shown in Fig C.4-4. For manufacturing ease, the radial tapered fin was approximated by a rectangular plate with stepped thicknesses.The rectangular fin was attached to the bottom of the baseplate.

The other set of critical components that were analysed in detail were the magnetics. The thermal problem is magnified because of the high dissipations and the large number of layers of insulation that is required to prevent voltage breakdown. The operating voltages for the magnetics are 700 volts and 1500 volts. It was necessary to minimize the thickness of the potting material under the magnetics and to use trucast, relatively high thermal conducting epoxy, as an encapsulating material. A typical magnetic is shown in Fig C.4-5. Based on this configuration the internal temperatures of the magnetics were calculated. Fig C.4-6 summarizes the results of the thermal calculations. These temperatures are below the maximum allowable of 257 F (125 C).

.040 ALUMINUM PLATE

DISSIPATION = 570 WATTS = 1940 BTU's

ϵ = 0.85 (CATA-LAC BLACK)

RADIATES TO CRYOGENIC $L N_2$ TANK

$$\frac{1940}{\sigma \epsilon A} = T^4 = \frac{13320 \times 10^8}{A}$$

A (ft^2)	T(R)	T(F)
8.55	629	169
11.40	585	125
14.25	553	93
17.10	529	69
20.00	509	49

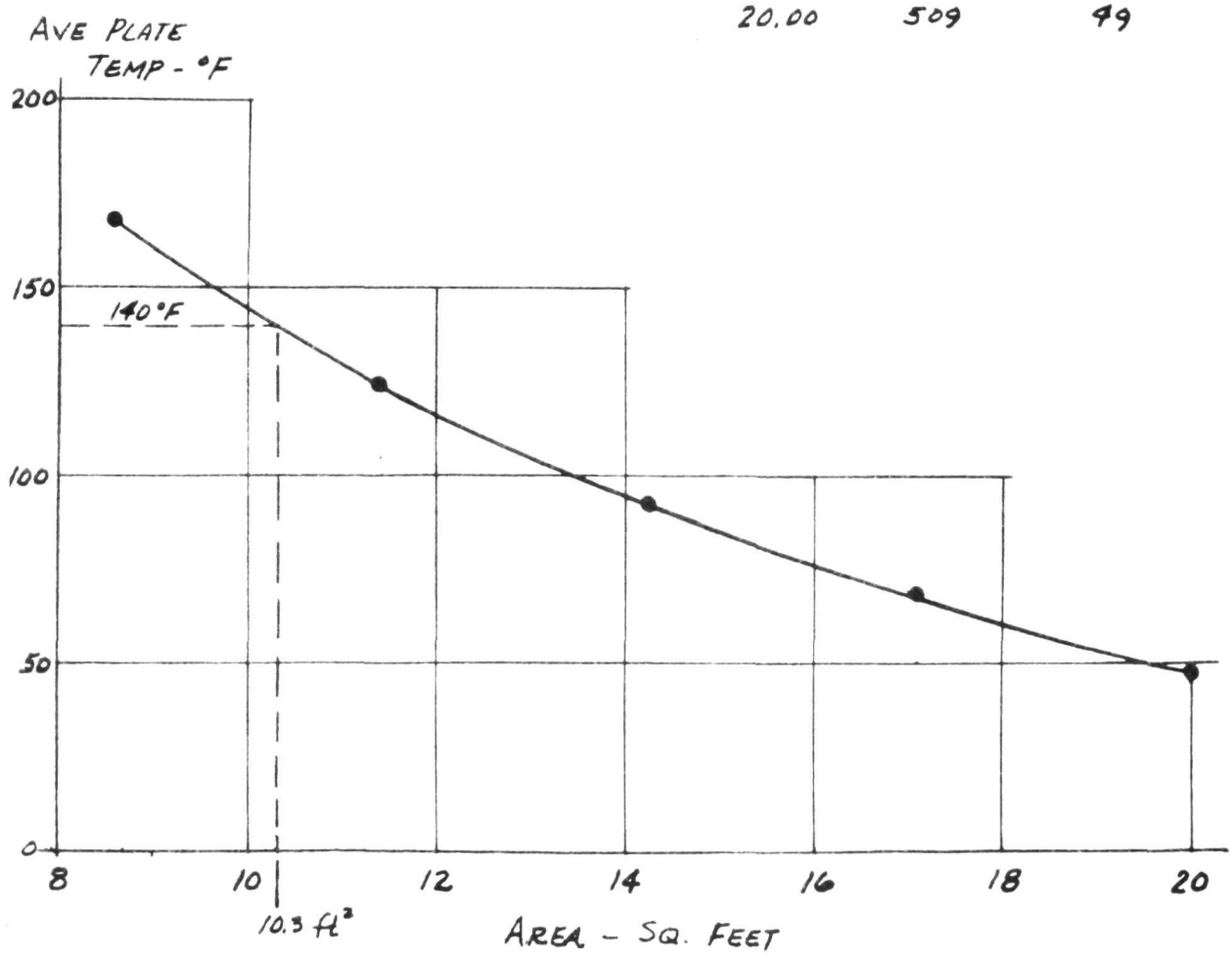


FIGURE C.4-1. SURFACE AREA VS. TEMPERATURE

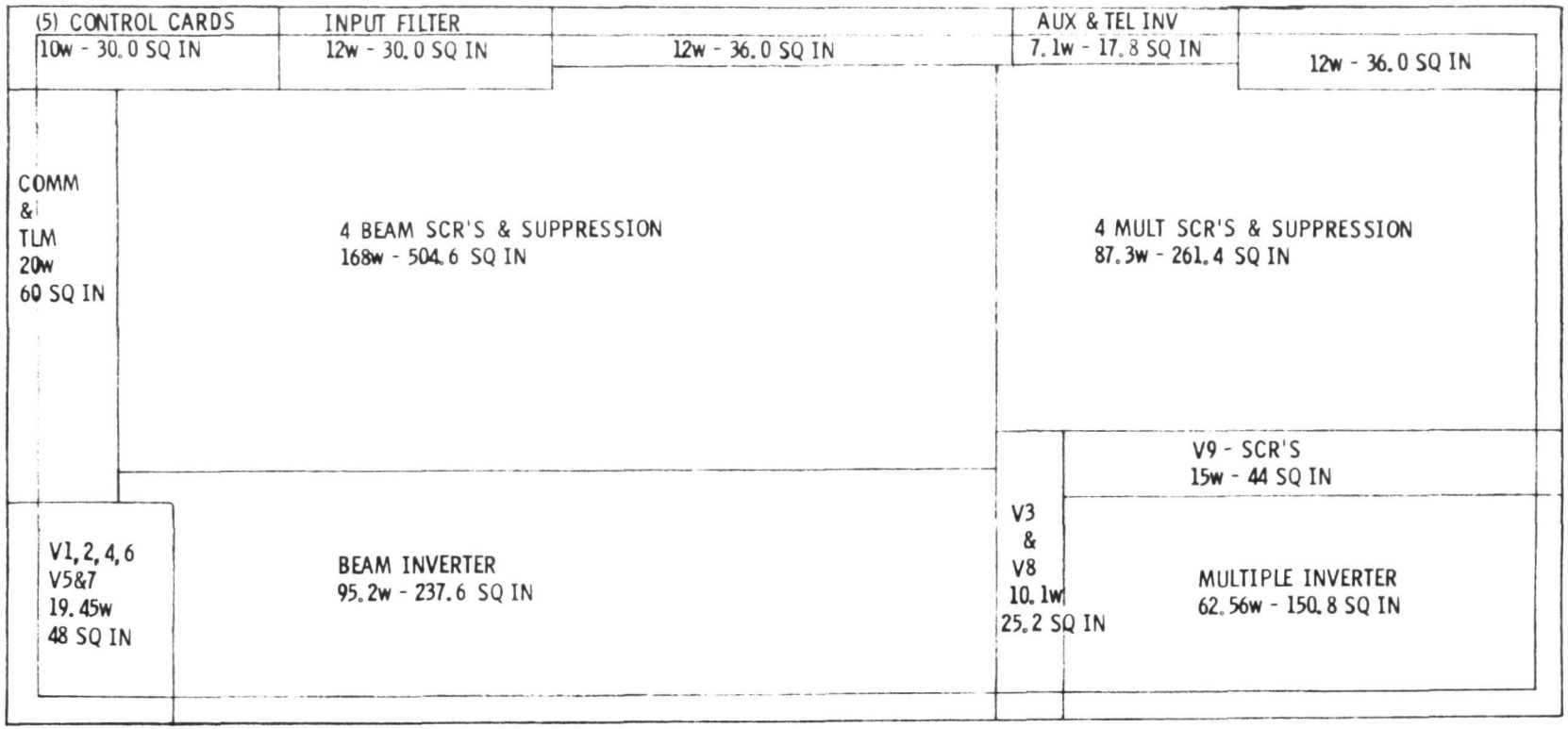


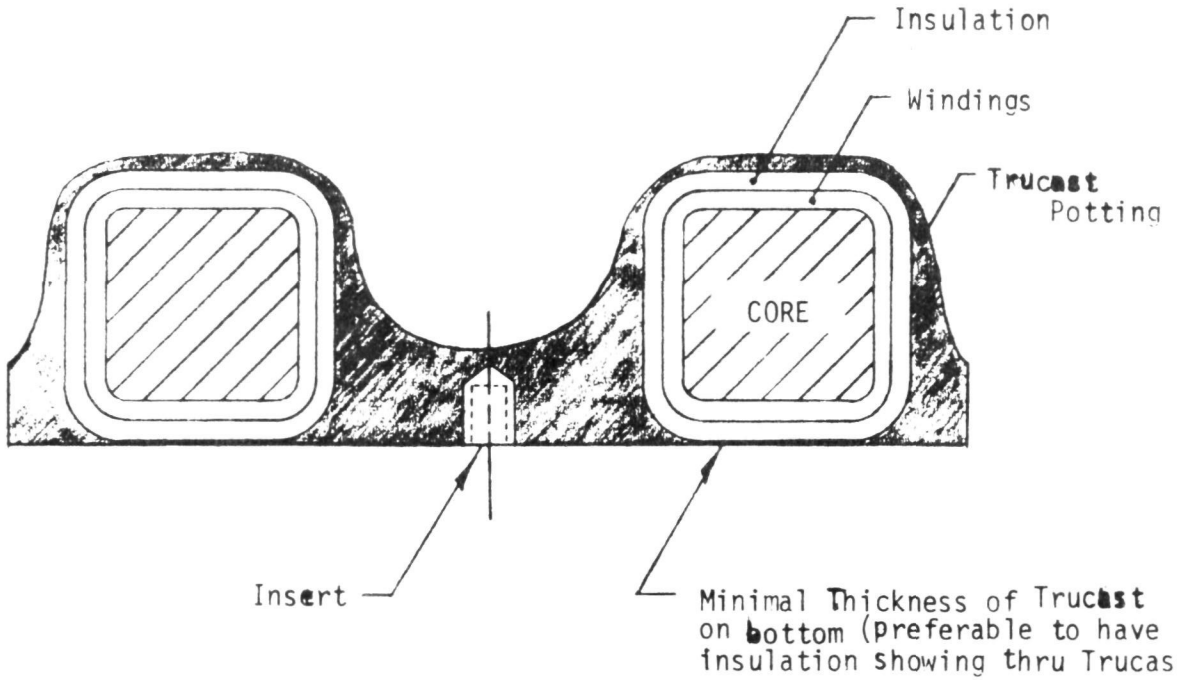
FIGURE C.4-2. POWER DISSIPATION DISTRIBUTION

RADIUS IN	THKNSS IN	TEMP F	HEAT W	HEAT W	WEIGHT LB	WEIGHT LB
0.70	0.505	167.00	.75	.75	0.078	0.078
1.20	0.505	163.88	1.42	2.16	0.151	0.228
1.70	0.246	157.63	2.08	4.24	0.112	0.340
2.20	0.222	151.38	2.68	6.93	0.136	0.476
2.70	0.140	145.13	3.24	10.17	0.108	0.584
3.20	0.130	138.88	3.74	13.91	0.121	0.705
3.70	0.091	132.63	4.19	18.10	0.099	0.803
4.20	0.084	126.38	4.60	22.70	0.104	0.907
4.70	0.061	120.13	4.97	27.67	0.086	0.993
5.20	0.060	114.15	5.30	32.97	0.093	1.087
5.70	0.060	109.23	5.64	38.61	0.103	1.189
6.20	0.060	105.28	5.99	44.60	0.112	1.301
6.70	0.060	102.18	6.35	50.94	0.122	1.423
7.20	0.060	99.83	6.73	57.67	0.131	1.554
7.70	0.060	98.14	7.13	64.80	0.140	1.694
8.20	0.060	97.07	7.54	72.34	0.150	1.844
8.70	0.060	96.56	7.99	80.33	0.159	2.004

FIGURE C.4-3. SCR'S DISSIPATING 80 WATTS

RADIUS IN	THKNSS IN	TEMP F	HEAT W	HEAT W	WEIGHT LB	WEIGHT LB
0.70	0.234	167.00	.75	.75	0.036	0.036
1.20	0.234	162.80	1.41	2.15	0.070	0.106
1.70	0.112	154.40	2.04	4.19	0.051	0.157
2.20	0.099	146.00	2.59	6.78	0.061	0.217
2.70	0.061	137.60	3.08	9.86	0.047	0.265
3.20	0.060	129.57	3.51	13.37	0.056	0.320
3.70	0.060	123.33	3.94	17.31	0.065	0.385
4.20	0.060	118.50	4.36	21.67	0.074	0.460
4.70	0.060	114.82	4.79	26.46	0.084	0.544
5.20	0.060	112.09	5.23	31.68	0.093	0.637
5.70	0.060	110.16	5.68	37.36	0.103	0.740
6.20	0.060	108.95	6.14	43.50	0.112	0.852
6.70	0.060	108.37	6.63	50.14	0.122	0.973

FIGURE C.4-4. SCR'S DISSIPATING 50 WATTS



Bond magnetics to chassis using Lefkoweld and screw down tight. To minimize Lefkoweld thickness.

FIGURE C.4-5. TYPICAL MAGNETIC CONFIGURATION

Ref. Designation	Operating Voltages (Volts)	Dissipations (Watts)	ΔT to Baseplate (° F)	Internal Temperature of Magnetic (° F)
L1 -L4	700	18	98.5	238.5
L5	700	12	86.5	226.5
L6-L9	700	10	91	231.0
L10	700	6	64	204.0
T1	1500	35	108	248.0
T2	1500	10	55	195.0

BASEPLATE TEMPERATURE = 140° F

FIGURE C.4-6. MAGNETICS TEMPERATURES

C.5 Cabling

The cabling of the power processor is accomplished so that the high power cables do not interfere with the low power control cables. The power cabling is put against the baseplate. The input power comes through the input power connector, the input filter and directly into the high power beam series resonant inverter and then the power lines lead to the lower power multiple output inverter. In this manner, the power cabling length and weight is minimized.

The low level control signal cable is elevated above the baseplate by about four inches. In this way, physical separation is obtained from the power cabling which is directly against the baseplate and coupling between the two is minimized. The routing of the control signal cable is shown in Figure C.5-1.

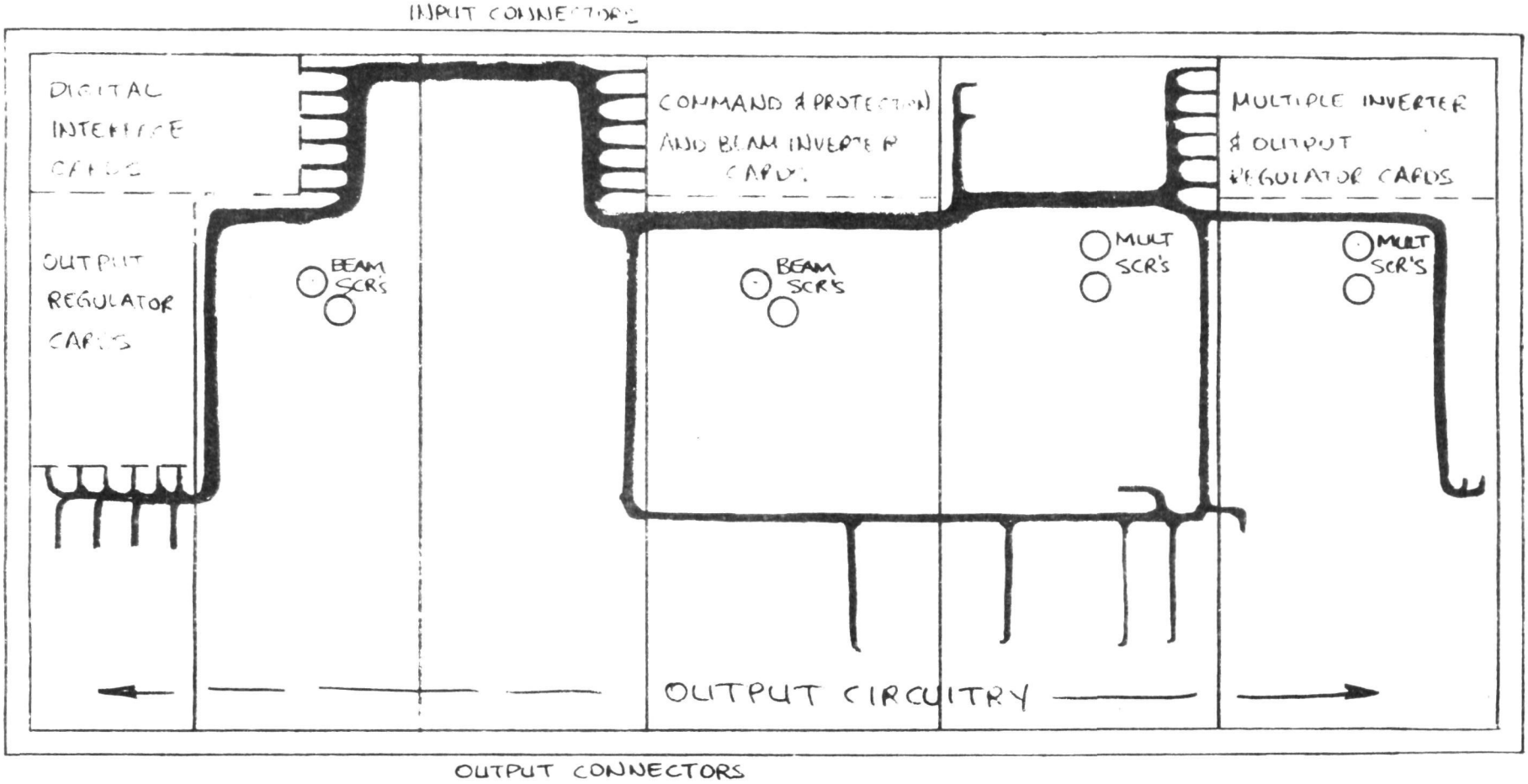


FIGURE C.5-1. CONTROL SIGNAL CABLING

C.6 Connectors & EMI Control

All input and output power lines have feedthrough filter assemblies to control the radiated and conducted interference level from the power processor. Figure C.2-1 shows the location of these filter assemblies near the power connectors and the location of all connectors.

The following is a list of connectors used for the power processor:

1) 200-400Vdc input power
2) 2.41kHz input power
3) Command lines to digital interface unit
4) Telemetry lines from digital interface unit
5) Low voltage outputs V1, V2, V6 & spacecraft return
6) Neutralizer low voltage outputs and return
7) Keeper output - (HV)
8) Screen (HV)
9) Accelerator (HV)
10) Screen return (HV)
11) V12 (HV)
12) V4 (HV)
13) V3 (HV)
14) V8 (HV)
15) High outputs return (HV)
16) V9 (+) (HV)
17) V9 (+) (HV)
18) V9 (-) (HV)
19) V9 (-) (HV)

High voltage connectors type Amp LGH-1/2 have been indicated.

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