General Disclaimer

One or more of the Following Statements may affect this Document

- This document has been reproduced from the best copy furnished by the organizational source. It is being released in the interest of making available as much information as possible.

- This document may contain data, which exceeds the sheet parameters. It was furnished in this condition by the organizational source and is the best copy available.

- This document may contain tone-on-tone or color graphs, charts and/or pictures, which have been reproduced in black and white.

- This document is paginated as submitted by the original source.

- Portions of this document are not fully legible due to the historical nature of some of the material. However, it is the best reproduction available from the original submission.

NASA TECHNICAL MEMORANDUM

NASA TM X-71735

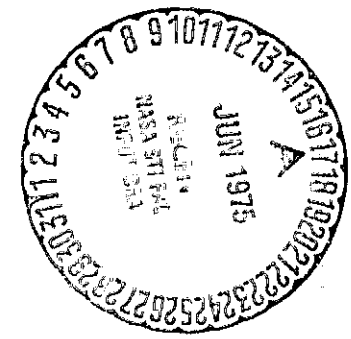
NASA TM X-71735

(NASA-TM-X-71735) EFFICIENCY AND WEIGHT OF VOLTAGE MULTIPLIER TYPE ULTRA LIGHTWEIGHT dc-dc CONVERTERS (NASA) 10 p HC $3.25 CSCL 10B

N75-23851

Unclas G3/33 22209

EFFICIENCY AND WEIGHT OF VOLTAGE MULTIPLIER TYPE ULTRA LIGHTWEIGHT D. C. -D. C. CONVERTERS



by W. T. Harrigill, Jr., and I. T. Myers
Lewis Research Center
Cleveland, Ohio 44135

TECHNICAL PAPER to be presented at
Power Electronics Specialists Conference sponsored by
the Institute of Electrical and Electronics Engineers
Culver City, California, June 9-11, 1975

EFFICIENCY AND WEIGHT OF VOLTAGE MULTIPLIER TYPE ULTRA LIGHTWEIGHT D.C.-D.C. CONVERTERS

W. T. Harrigill, Jr., and I. T. Myers

National Aeronautics and Space Administration
Lewis Research Center
Cleveland, Ohio 44135

SUMMARY

This paper presents an analytical and experimental study of a capacitor-diode voltage multiplier without a transformer which offers the possibility of high efficiency with light weight. D.c.-d.c. conversion efficiencies of about 94 percent were achieved at output powers of 150 watts at 1000 volts using 8× multiplication. A detailed identification of losses was made, including forward drop losses in component, switching losses, reverse junction capacitance charging losses, and charging losses in the main ladder capacitors.

INTRODUCTION

Power processing equipment used in space flight applications should be lightweight, and have the ability to deliver a wide range of output power while maintaining a high efficiency. Presently available equipment, which typically is a d.c.-d.c. converter including a transistor chopper with a transformer for voltage transformation, does not completely meet these requirements. Systems with high efficiency (90 to 95 percent) can be designed and built, but the total system weight is substantially higher than desired. The voltage multiplier concept, which uses capacitors and diodes for voltage transformation, appears attractive as an alternative.

This paper extends the concept of the transistor chopper driven capacitor diode voltage multiplier (CDVM) d.c.-d.c. converter (Refs. 1 to 4) to a wide range of weights, efficiencies, and output power by exploring the tradeoffs between the CDVM converter design parameters. This investigation indicates that it is possible to design either a very lightweight converter with somewhat reduced efficiency, a very high efficiency converter with a somewhat increased weight, or an in-between converter where the efficiency and weight can be tailored to a given application.

A 100-watt, 1000-volt experimental model with a chopping frequency of 70 kHz was used for all testing. Efficiencies as high as $94\frac{1}{2}$ percent were attained at 100 watts output with a component weight of about 2 kg/kW and a $92\frac{1}{2}$ percent efficiency at a component weight of 1 kg/kW. Thus the CDVM d.c.-d.c. converter offers a better combination of efficiency and weight, compared to conventional power processing, and also has the capability of a wide range of weight and efficiency to fit a given application.

EXPERIMENTAL MODEL

Figure 1 shows a circuit diagram of the experimental CDVM converter used to obtain the data in this report. The converter consists of a transistor chopper (driven at 70 kHz) connected directly into a voltage multiplier with $N = 8$. No transformer is required, which is a major advantage from a weight, cost, and efficiency standpoint. Two d.c. power supplies were used in the experimental setup for versatility and convenience. One supply could be used (with a voltage of $2\ V_1$) without affecting the converter performance. The nominal output voltage of the experimental model was 1000 volts with the input power supplies at +130 volts and -130 volts.

LOSSES AND EFFICIENCY

The tradeoff between efficiency, weight, and output power in the CDVM converter can be determined from a study of the losses involved in the system. These losses along with approximate expressions for their value, are listed in ten categories. They are:

(1) Capacitance charging losses (Ref. 5) in the voltage multiplier capacitors while the diodes are conducting. This includes series resistance losses in the leads, and in the equivalent series resistance of the capacitors. It is treated in detail in Ref. 5 and will not be derived here. Both losses in charging a capacitor from another capacitor, and in charging a capacitor from a power source are included as appropriate. Stray series inductance is ignored in this treatment. The expression for this loss (P_1) for a voltage multiplier with N diodes and N capacitors, a load current i_L and unit capacitors C_u operated at a frequency f is

$$P_1 = \frac{i_L^2 N\left(N^2 + \frac{1}{2}\right)}{12 f C_u} \qquad (1)$$

(2) Charging losses of the reverse biased

junction capacitance of the CDVM diodes during the time when the diodes are not conducting. This loss (P_2) is given by

$$P_2 = 4NC_{DR}V_i^2 f \qquad (2)$$

where C_{DR} is the junction capacitance of each diode in the voltage multiplier. As the diode junction begins to block where the input voltage swings from $+V_i$ to $-V_i$ or vice versa, the diode voltage changes from about a volt in the forward direction to $2V_i$ in the reverse. The charge taken from the capacitors C_u and the voltage sources to charge C_{DR} to $2V_i$ is then $2C_{DR}V_i$. Since the battery and/or capacitors supply the charge at a voltage $2V_i$, the amount of energy used in this junction capacitance charging is $4C_{DR}V_i^2$ per diode. The total energy loss for the N diodes is then $4C_{DR}NV_i^2$ for each charging cycle, which occurs f times per second. The power loss due to this cause is therefore $4C_{DR}NV_i^2 f$.

(3) Charging losses of the chopping transistor junction capacitance (output capacitance) during the transistor "off" period. This loss (P_3) is given by

$$P_3 = 8C_{TR}V_i^2 f \qquad (3)$$

It is similar to P_2. The junction capacitance C_{TR} of the individual transistor is charged to $2V_i$ each cycle, with a consequent energy loss of $4C_{TR}V_i^2$. Since there are two transistors operating at a frequency f, the total power loss is as given in Eq. (3).

(4) Forward conduction losses of the CDVM diodes. This loss is due to the forward voltage drop across the diodes during their "on" time. This power loss (P_4) is therefore

$$P_4 = NV_{DF}i_L \qquad (4)$$

since the average diode current must be equal (ignoring leakages) to the load current. V_{DF}, the forward drop of the conducting diode varies somewhat with load current, but was taken as a constant for this treatment. The factor N enters because there are N diodes, each of which must carry the load current i_L as an average current.

(5) Transistor forward conduction losses in the transistor chopper. As in the case of the diode, this is due to the saturation voltage across the transistors during the conduction cycle. This power loss (P_5) is given by

$$P_5 = 2V_{TF}Ni_L \qquad (5)$$

where V_{TF} is the forward conduction drop of the transistor. The number of diodes enter because the transistor current is Ni_L, neglecting second order effects, and the factor of 2 is needed because two transistors are used.

(6) Reverse bias d.c. leakage losses in the CDVM diodes caused by reversed current flow while the diodes are off. This power loss (P_6) is given by

$$P_6 = 2V_i i_{DR}N \qquad (6)$$

and is due to the use of N diodes, charged to a voltage $2V_i$, with a leakage current i_{DR}. For good diodes, the leakage current is in the microampere range, so that P_6 is usually negligible compared to other losses.

(7) D.c. leakage losses of the transistors in the "off" state. This loss is comparable to P_6 for the diodes. The expression for it is

$$P_7 = 2V_i i_{T,OFF} \qquad (7)$$

where $i_{T,OFF}$ is the residual current flowing through the transistor when it is off. This current is of the order of milliamperes so that P_7 cannot be ignored as P_6 was. Again, the factor of 2 is necessary because the chopper has two transistors.

(8) Transistor base drive losses. This is about 1 watt at 100 watts output. An approximate expression for this loss is

$$P_8 = \frac{i_L N V_d}{\beta} \qquad (8)$$

where V_d is in the transistor drive voltage. The average transistor collector current is Ni_L, so that the average base current is approximately $i_L N/\beta$ and the base drive power is as given in Eq. (8). Again, second order effects were ignored. It is believed that this loss can be decreased as the output power is reduced.

(9) Switching losses in the chopper transistors. This power loss P_9 is for turn on only, since the current goes to zero as capacitor charging is completed, and this occurs before the square wave voltage output from the chopper changes sign. The current drawn through the transistor is approximately a half sine wave (positive for one transistor, negative for the other) with a half period in each case of about 3.5 microseconds (τ_{IT} = 7 sec). The switching loss was calculated by assuming a linear switching decrease in voltage across the transistor from V_i to zero in the turn on time of the transistor τ_T. Integrating these two together over the transistor switching time τ_T, and multiplying by the chopping frequency f gives the power loss P_9.

$$P_9 = \frac{\pi^2 V_i i_L N}{3}\left(\frac{\tau_T}{\tau_{IT}}\right)^2 \qquad (9)$$

This switching loss is unusual in that it does not depend on the chopping frequency f. The reason for this is that peak value of the transistor current wave shape with period τ_{IT} is inversely proportional to f so that the factor drops out

in the final result.

(10) Switching losses in the CDVM diodes. The diode switching loss P_{10} is negligible, since the switching time for turn on is substantially less for good diodes than for transistors. The equation given for P_{10} in Table I is an upper limit for the case of zero rise time on the diode volts.

Table I lists these losses, the equation which characterizes each loss, and a calculated value for each loss (for an output power of 100 W) as a percentage of the output power. Transistor losses made up about 60 percent of the total. Second order effects have not been included, since the individual losses are small. The definition of symbols used in the equations are shown in Table II. The values of the parameters needed for the calculations were either determined from a direct laboratory measurement or obtained from the manufacturer's specification. The values used are given in Table III. The values shown are for commercially available components. Further selection or special development of components could bring further reduction of losses or weight. This is especially true of the capacitors, which make up the bulk of the weight of the converter.

With the above losses it is possible to write an overall efficiency equation as follows:

$$\eta = \frac{P_L}{P_L + P_1 + P_2 \cdots P_{10}}$$

If the experimental test model values are used in the above equation, a value of 94 percent is obtained for the overall efficiency at an output of 100 watts. The measured efficiency of the experimental model checks closely with this figure.

EXPERIMENTAL RESULTS

Because of the lower frequencies normally used in conventional d.c.-d.c. converters, the reverse junction capacitance charging losses (P_2, P_3 Table I) have little effect on conversion efficiency, and are not normally treated. Because the CDVM converter operates at a higher frequency (70 kHz) these losses do contribute to the total loss of the system. Therefore they were experimentally verified by adding extra capacitance across the diodes and/or transistors to simulate larger junction capacitance. The results of these measurements (Fig. 2) show that efficiency is reduced linearly with an increase in capacitance, which demonstrates the importance of designing with low junction capacitance transistors and diodes.

The effect of these losses is further illustrated in Fig. 3 where efficiency of the experimental model is shown as a function of output power for various combinations of junction capacitance and unit capacitance (C_u) values. The lowest efficiencies occur for high values of junction capacitance and low values of C_u. The maximum value of efficiency was obtained (about 95½ percent) with a C_u value of 4μF. C_u values varied during the tests from 1μF to 4μF with weights and efficiencies at 100 watts output varying from .8 kg/kW at 86 percent to about 2 kg/kW at 95½ percent, respectively. The transistor base drive circuit loss (P_8 Table I) is not included in this figure, but an estimate indicates that this loss will lower the efficiencies by about 1 percent. The experimental data also indicates that the overall efficiency remains relatively constant over a wide range of output power, since the efficiency varies only 2 percent between 25 and 150 watts (C_u = 4μF; top curve Fig. 3). Because the weight of the CDVM is strongly dependent on the value of C_u, and since the efficiency increases with larger values of C_u, it is possible to use these tradeoffs to optimize a system for a particular application.

For a value of C_u of 2 microfarads the capacitors C_1 to C_N make up about two thirds of the total weight, with the rest being due to transistors, diodes, and other components. For the case when C_u is equal to 4 microfarads, the capacitor weight is five sixths of the total. Reducing the capacitance value C_u reduces the weight, but increases the losses due to capacitor charging. Clearly, what is needed here is a higher energy density (lighter weight) capacitor, so that it would be possible to keep the efficiency high with large values of C_u, without paying a corresponding weight penalty.

SUMMARY OF RESULTS

An analytical and experimental investigation of a d.c.-d.c. converter using a capacitor-diode voltage multiplier was made with the following results.

1. Ten separate losses were identified in the CDVM converter.

2. Losses are a function of:

   (a) Chopping frequency

   (b) Capacitance size (C_u)

   (c) Transistor junction capacitance

   (d) Diode junction capacitance

   (e) Transistor forward voltage drop

   (f) Diode forward voltage drop

   (g) Transistor switching speed

   (h) Diode switching speed

   (i) The number of stages in the CDVM

   (j) Output voltage and output current

   (k) Chopper transistor base drive losses

3. [illegible]t (60 percent) of the losses were in the transistors.

4. The junction capacitance charging from varied linearly with the junction capacitance.

5. It is possible to use the tradeoffs to obtain an optimum system design for a given converter application.

6. A better combination of weight and efficiency are available with voltage multiplier d.c.-d.c. converters than with presently available converters.

7. Efficiency is relatively insensitive to output power.

8. Most of the weight of the converter is in the multiplier capacitors.

Difficult design problems are not anticipated when the CDVM converter is extended to a power processing system. The input filter design should be straightforward and have a low component weight due to the higher chopping frequency, and the output filtering should be minimal due to the filtering action of the CDVM.

REFERENCES

1. R. Rufer, "Battery Powered Converter Runs Multiplier Phototube," Electronics, vol. 33, p. 51, July 1960.

2. G. Olson, "D.c. to d.c. Converter Offers Positive or Negative Bias," Electronics, vol. 43, p. 45, May 1970.

3. K. N. Pal, "Transformerless Voltage Doubler Has Good Output Regulation," Electronic Design, vol. 26, p. 64, Dec. 1972.

4. C. B. Wheeler, "Power Supplies for Continuous Gas Lasers and Similar Discharges," J. Physics, Part E, Scientific Instru., vol. 4, pp. 159-164, Mar. 1971.

5. W. T. Harrigill and I. T. Myers, "High Performance D.C.-D.C. Conversion with Voltage Multipliers," in IEEE Power Electronics Specialist Conference, June 1974, pp. 91-96.

TABLE I. - LOSS SOURCES

Loss type	Formula for loss	Percent loss @ 100 W
1. CDVM capacitor charging loss	$P_1 = \frac{i_L^2 N\left(N^2 + \frac{1}{2}\right)}{12fC_u}$	1.5
2. Diode reverse junction charging loss	$P_2 = 4NC_{DR}V_i^2 f$	.3
3. Transistor reverse junction charging loss	$P_3 = 8C_{TR}V_i^2 f$	.7
4. Diode forward conduction losses	$P_4 = NV_{DF}i_L$	.8
5. Transistor forward conduction losses	$P_5 = 2V_{TF}Ni_L$	1.3
6. Diode reverse bias d.c. leakage losses	$P_6 = 2V_i i_{DR}N$	~0
7. Transistor "off" d.c. leakage losses	$P_7 = 2V_i i_{T,OFF}$	.3
8. Transistor base drive loss	$P_8 = \frac{i_L N V_d}{g}$	~1
9. Transistor switching losses	$P_9 = \frac{\pi^2 V_i i_L}{3} N\left(\frac{\tau_T}{\tau_{IT}}\right)^2$	.4
10. Diode switching losses	$P_{10} < \frac{\pi^2 V_i i_L N}{6}\left(\frac{\tau_D}{\tau_{ID}}\right)^2$	~0
Total losses		6.3%
Efficiency		94.3%

TABLE II. - DEFINITION OF SYMBOLS

C_{DR}	reverse junction capacitance of diode. Assumed to be the same for all diodes, F
C_{TR}	transistor "off" junction capacitance. Average value for the two transistors, F
C_u	unit CDVM capacitance (value for each capacitor for case where $C_1 = C_2 = \ldots, C_N$), F
$C_1, \ldots, C_N$	CDVM capacitors, F
f	frequency, Hz
i_{DR}	reverse leakage current of diodes at voltage $2V_i$
i_L	load current, A
$i_{T,OFF}$	transistor "off" d.c. leakage current, A
N	number of diodes (also voltage multiplication factor)
P_1	power loss due to CDVM capacitor charging loss
P_2	power loss due to reverse junction capacitance charging of diodes
P_3	power loss due to transistor "off" junction capacitance charging
P_4	power loss due to forward diode conduction drops
P_5	power loss due to forward transistor conduction drops
P_6	power loss due to reverse bias leakage of diodes
P_7	power loss due to transistor "off" d.c. leakage
P_8	transistor base drive power loss
P_9	transistor switching loss
P_{10}	diode switching loss
V_{DF}	diode conduction drop, V
V_d	transistor drive voltage, V
V_i	input voltage
V_{TF}	transistor average forward conduction drop, V
β	chopper transistor current gain
τ_D	diode switching time, sec
τ_{ID}	period of diode current, sec
τ_{IT}	period of transistor input current, sec
τ_T	transistor turn on time, sec

TABLE III. - PARAMETER VALUES

Parameter	Value
C_{DR}, diode reverse bias junction capacitance	7 pF
C_{TR}, transistor "off" junction capacitance	80 pF
V_{DF}, diode conduction drop	1.0 V
V_{TF}, transistor forward conduction drop	0.8 V
$i_{T,OFF}$, transistor "off" leakage current	1.0 mA
V_d, transistor drive voltage	10-15 V
β, chopper transistor current gain	10
τ_T, transistor turn on time	0.25 μsec
τ_D, diode switching time	<0.1 μsec
τ_{1D}, period of diode current	2 μsec
τ_{1T}, period of transistor input current	7 μsec
N, number of capacitors or diodes in CDVM	8
V_i, input voltage	130 V
f, operating frequency	70 kHz

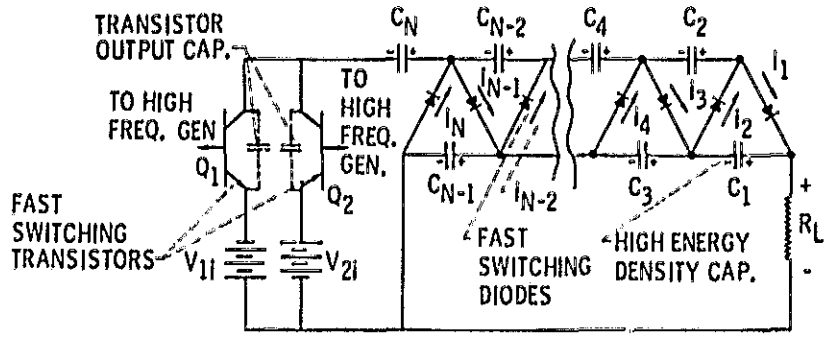


Figure 1. - Transformless capacitor diode voltage multiplier DC - DC converter. Either V_{1i} or V_{2i} can be zero or chosen arbitrarily within component ratings.

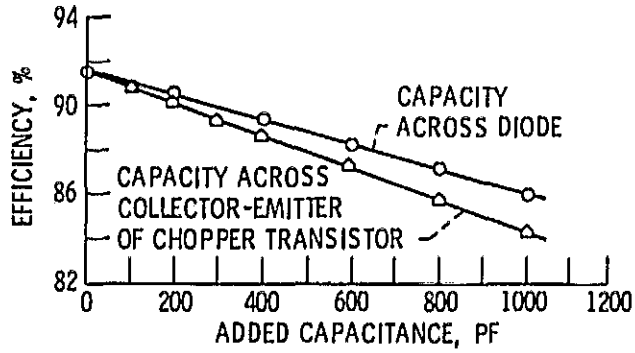


Figure 2. - Efficiency versus added capacity. Output power, 60 watts. Cu = 1 μF

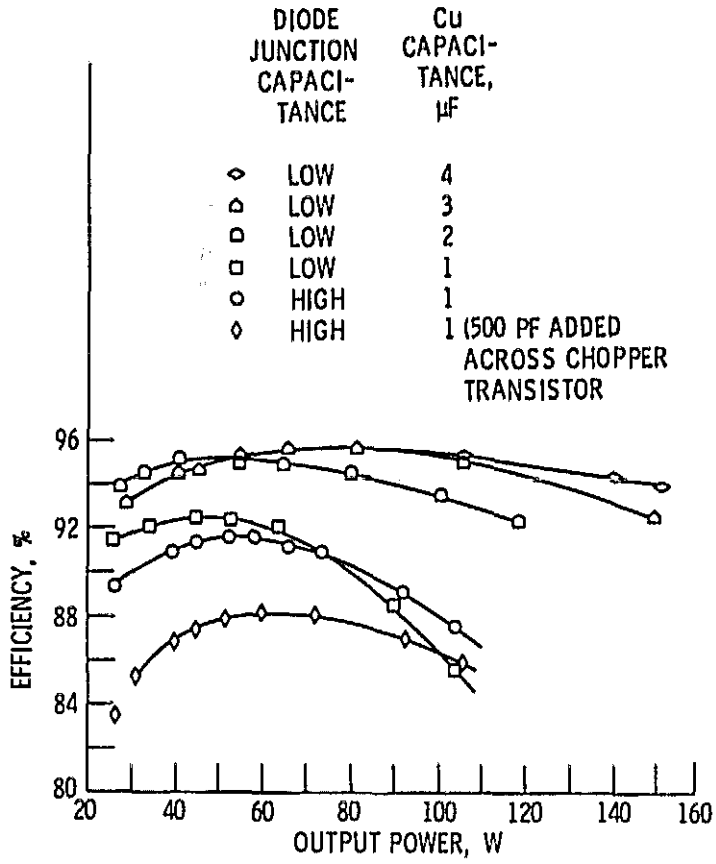


Figure 3. - Efficiency versus output power. High capacity diodes, 25 PF; low capacity diodes, 7 PF.