General Disclaimer

One or more of the Following Statements may affect this Document

- This document has been reproduced from the best copy furnished by the organizational source. It is being released in the interest of making available as much information as possible.

- This document may contain data, which exceeds the sheet parameters. It was furnished in this condition by the organizational source and is the best copy available.

- This document may contain tone-on-tone or color graphs, charts and/or pictures, which have been reproduced in black and white.

- This document is paginated as submitted by the original source.

- Portions of this document are not fully legible due to the historical nature of some of the material. However, it is the best reproduction available from the original submission.

DEVELOPMENT OF A BREADBOARD DESIGN OF A HIGH-PERFORMANCE, HIGH-RELIABILITY SWITCHING REGULATOR

2322-Final Report

April 1975

Contract No. 953691

APPROVED BY: K. Winsor

K. Winsor, Manager
Aerospace Systems Division

W. Croft

W. Croft, Manager
Power Systems Department

S. Lindena

Dr. S. J. Lindena
AUTHOR

Xerox Electro-Optical Systems

300 North Halstead Street
Pasadena, California 91107

Work Performed for Jet Propulsion Laboratory, California Institute of Technology, sponsored by National Aeronautics and Space Administration under Contract No. NAS 7-100.

ABSTRACT

The purpose of this contract was to develop a breadboard design of a high-performance, high-reliability switching regulator.

This report presents a comparison of two potential conversion methods, the series inverter and the inductive energy transfer (IET) conversion technique.

The investigations showed that a characteristic of the series inverter circuit (high equalizing current values in each half cycle) could not be accomplished with available components. Therefore, the investigations continued with the IET circuit only.

An IET circuit system was built with the use of computer-aided design in a 2, 4, and 8 stage configuration. These stages were staggered 180, 90, and 45 degrees, respectively. All stages were pulsewidth modulated (PWM) to regulate over an input voltage range from 200 to 400 volts dc at a regulated output voltage of 56 volts. The output power capability was 100 to 500 watts for the 2 and 8 stage configuration and 50 to 250 watts for the 4 stage configuration.

Equal control of up to eight 45 degree staggered stages was accomplished through the use of a digital-to-analog control circuit. This approach avoided the problem of generating equal control pulses for multiple stages over a wide temperature range and component drift characteristics.

Equal power sharing of all stages was achieved through a new technique using an inductively coupled balancing circuit. To maintain proper filtering, a specially designed L-C parallel circuit served as a buffer between the balancing circuit and the output filter section.

Through experimental and theoretical evaluation, the following conclusions were drawn:

The 8 stage, 45 degree staggered approach offers the following distinct advantages:

1. Uninterrupted input and output current flow.

2. Reduced input and output filtering requirements.

3. Parallel redundancy: a failure of 2 out of 8 stages does not diminish power output capability. Acceptable temperature rises are encountered in components of the remaining 6 stages.

4. Breadboard proved feasibility of a multistage approach.

The disadvantages of an 8 stage, 45 degrees staggered approach are:

1. Increased complexity.

2. More weight and less efficiency than the simple push-pull approach.

Multiple staggered (either 4 or 8) stages are recommended when parallel redundancy and lower input and output filtering are desired and when modular add-on power is required without increasing filter requirements.

CONTENTS

CONTENTS (Contd)

ILLUSTRATIONS

REV.

ILLUSTRATIONS (Contd)

TABLES

SECTION 1

INTRODUCTION

The power conversion units used in spacecraft applications have grown steadily from relative low power capabilities of a few watts to high power capabilities in the kilowatt range. Simultaneously, the duration of the usable life requirements of the power conversion units has grown from days to months and now may exceed several years.

These continuing trends have focussed the attention on both future power conversion design approaches and components to meet this challenge.

Clearly visible is a shift from the up-to-now standard input voltage of about 24 to 32 volts dc to input voltages of 200 to 400 volts dc. Supporting evidence of this shift are the production lines of the 'switch' (transistors and SCR's) manufacturers which show ever increasingly higher blocking voltages and faster switching speeds.

Another trend is also evident in the requirement for design approaches which allow increases of power by simply adding parallel modules, and thus avoiding the development of 'new models' which can meet the higher output power requirements.

The statement of work for this study reflects all of the above trends as follows:

> "The development is to be concerned only with an intermediate power handling capability with sufficient design flexibility to allow growth with minimum impact.
>
> "Study advantages and disadvantages of alternate approaches.
>
> "The input voltage shall range from 200 to 400 volts dc. Minimum efficiency at full load shall be 90 percent.

"Two approaches are to be investigated. These approaches are:

A. The Series Inverter

B. The Inductive Energy Transfer Circuit"

The investigation of the Series Inverter was discontinued after it became apparent that present-day components could not meet the functional requirements of this circuit. Even though the probability exists of designing around this component limitation it was decided, after a presentation of the advantages and disadvantages of both approaches, to continue with the Inductive Energy Transfer System only.

Investigations were conducted on conversion circuits with 2 stages, 180 degree staggered (push-pull), 4 stages, 90 degree staggered, and 8 stages, 45 degree staggered.

To cover all aspects of multistage staggered approaches, it was decided that the final configuration should be an 8 stage, 45 degree staggered circuit. It was felt that all data gathered from this approach would yield the most useful information and would advance the state-of-the-art in some areas even though the circuit performance might not meet the original objectives.

The information now available allows us not only to make the correct decisions regarding power requirements and circuit configuration, but also gives us the advanced technology of a multistage load balancing circuit and the performance characteristic and potential of a true digital control circuit which is capable of precisely controlling the pulsewidth modulation of the staggered multiple stages.

SECTION 2

TECHNICAL DISCUSSION

Of the many known conversion techniques, Xerox Electro-Optical Systems has investigated under this contract, two conversion circuits. These have been studied and sufficiently breadboard tested to select a preferred circuit.

The two circuits used during this selection period were:

a. The Pulsewidth-Modulated Series Inverter at a Fixed Frequency
b. The Inductive Energy Transfer Supply with Multiple Stages

For the proper understanding of these two approaches, a discussion of the theory of these two conversion techniques is presented in the following paragraphs.

2.1 THE PULSEWIDTH-MODULATED SERIES INVERTER AT FIXED FREQUENCY

2.1.1 THEORY OF OPERATION

From a great variety of possible circuit configurations, figure 2-1 shows a simplified circuit diagram of the Series Inverter.

To understand the operation of this circuit, assume that the capacitors are charged to equal but opposite voltages. Further assume that the battery terminals E are shorted and that resistor R is equal to O. Turning on SCR1 results in a discharging current from capacitor C1 through SCR1 and L. The discharge occurs in a resonant fashion and at the end of a half cycle; the voltage on capacitor C1 has changed to the opposite but equal voltage (assuming no losses).

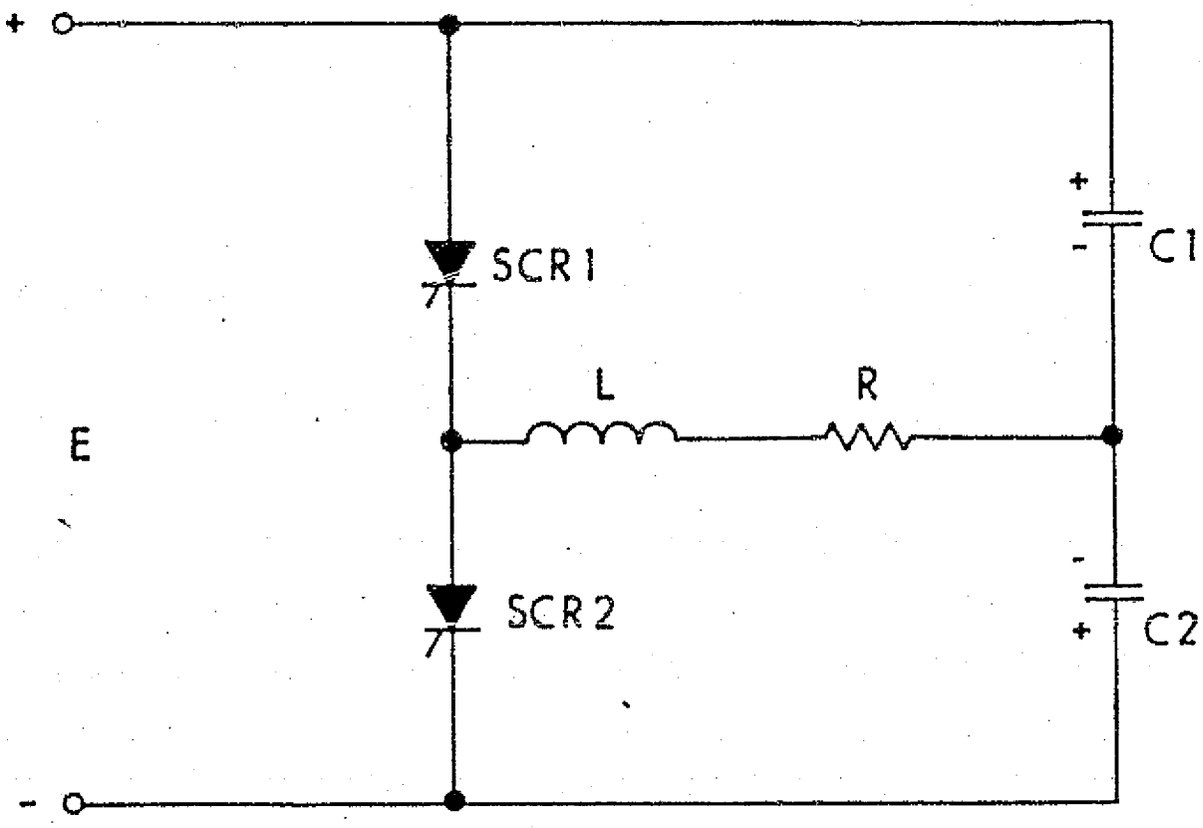


Figure 2-1. Series Inverter

At the same time, capacitor C2 discharges through the shorted battery terminals, SCR1 and L, and also reverses its polarity.

Firing of SCR2 repeats this cycle in the opposite direction. Because it has been assumed that the circuit is lossless, it will continue to operate with alternate firing of the SCRs. In the actual case, with losses, the battery must provide energy to restore these losses. If the battery voltage has a higher value than required to restore the losses, the voltages on the capacitors will build up until a balance between the input and output power is achieved.

If we now insert a load resistor R, it becomes apparent that a higher input voltage is required to keep the circuit operating in the resonant mode. The current waveshape through the load resistor R is shown in figure 2-2.

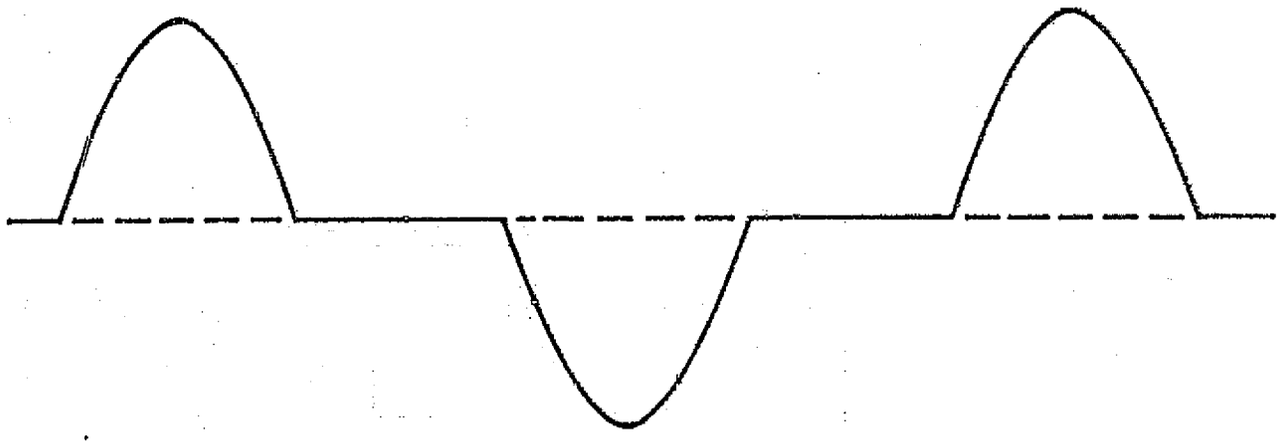


Figure 2-2. Current Pulses Through R

The repetition rate of the pulses is limited only by the recovery time of the SCRs and the resonant frequency of the LC network. The highest repetition rate is reached when the load current becomes a continuous sine wave.

For proper operation, the load resistor must not overdamp the circuit. It will be possible only in rare cases to connect the load as shown in figure 2-1. The difficulties are overcome by using the circuit diagram shown in figure 2-3. A transformer T1 has been added and the secondary of this transformer feeds the load which may be either an ac load or after rectification of the ac voltage, a dc load.

In this type of circuit, the most common approach is to couple the load to the series inverter through a transformer. The major disadvantage of this approach is that under light or no-load conditions, the magnetizing inductance of transformer T1 detunes the series resonant circuit of the series inverter and degrades operation. To overcome this problem, a new approach is used to connect the load. The simplified circuit diagram of this approach is presented in figure 2-4.

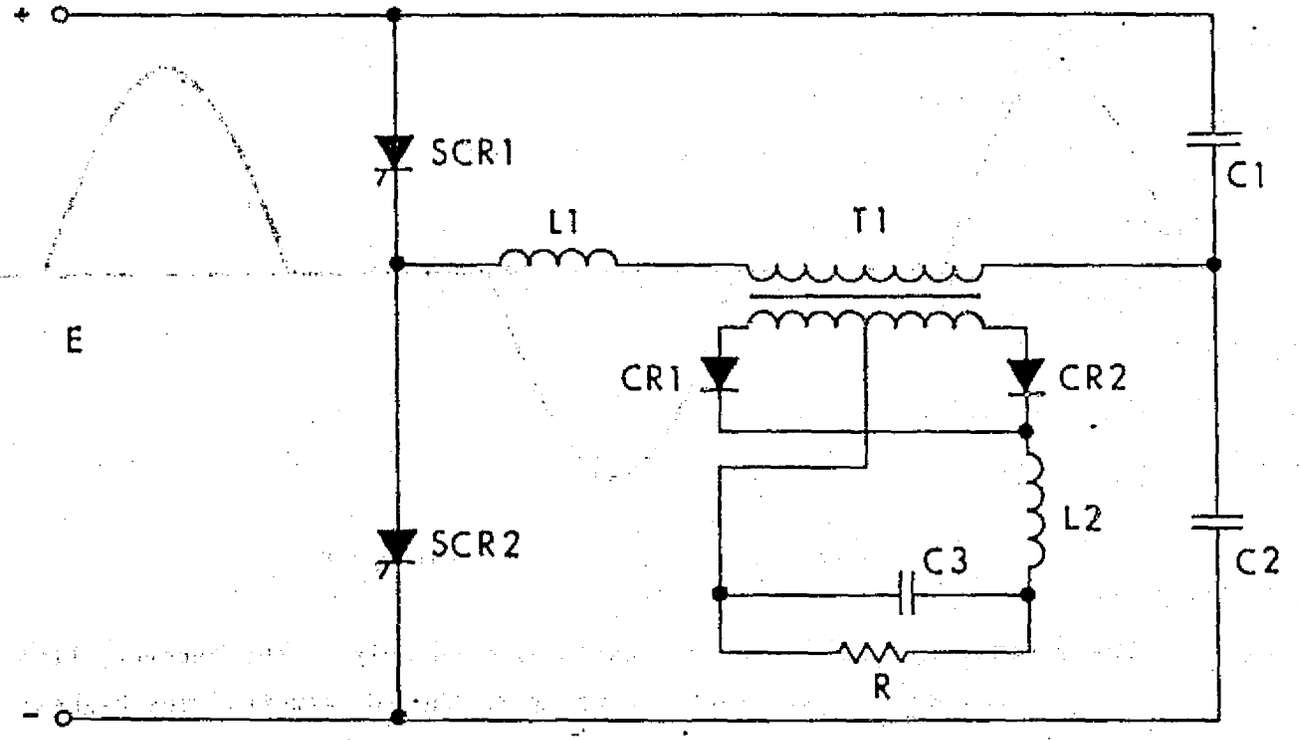


Figure 2-3. Series Inverter with Separate Transformer to Power Load

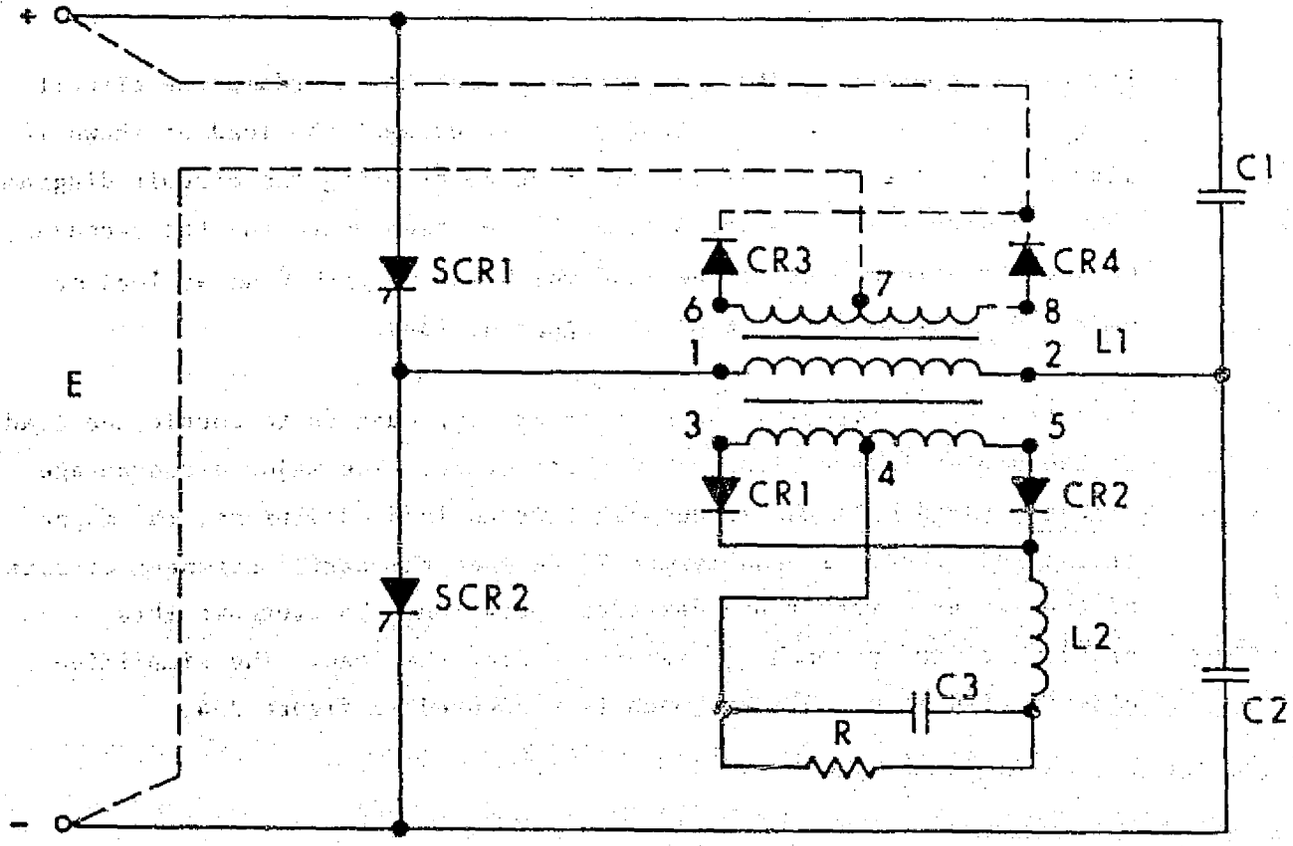


Figure 2-4. Series Inverter with Inductor Transformer L1 Power Load Coupling and No-Load Protection

The resonant-inductor L1 has been equipped with a secondary winding which powers an ac load connected directly across the secondary winding or powers a dc load through rectifiers as shown. This method of coupling the load to the series inverter is not only less complicated, but also avoids the no-load detuning problem previously mentioned in the description of figure 2-3.

2.1.2 MODES OF REGULATION

Two methods of regulation against input voltage variations and load changes were considered.

a. Variation of the Repetition Rate

The first approach is to vary the repetition rate of alternately firing switches SCR1 and SCR2 in figure 2-1. This method will produce the current pulse train as shown in figure 2-2. At very low repetition rates, the spacing between the individual current pulses becomes large and the energy delivered to the output becomes low.

At very high repetition rates, the spacing between the individual pulses becomes smaller and smaller until in the end-case, a continuous sinusoidal current waveshape is flowing through resistor R.

The major disadvantages of this approach are:

1. If dc is desired, filtering the output is difficult because the spacing between the constant energy pulses is large and therefore the filter capacitor must also be large to deliver energy between pulses.
2. If used in ac applications, the ac voltage generated across the load appears as shown in figure 2-2 with large dwell times between individual pulses.
3. At constant input voltage, the power delivered by the dc source is a train of constant amplitude sinusoidal half-wave current pulses with variable spacing.

The advantage of this approach, however, is simplicity and it also utilizes a very simple control circuit. Because of previously stated disadvantages, the following approach was also used in the investigation of the series inverter.

b. Pulsewidth Modulation of the Input Voltage

Figure 2-5 shows a simplified circuit diagram of a constant frequency series inverter with input voltage pulsewidth modulation. The closed-loop system to control the output voltage is also shown.

The two switches, SCR1 and SCR2, are driven at a fixed repetition rate such that the current flow through L1 is uninterrupted. The frequency of operation is therefore equal to the resonant frequency of L1 and C1 and C2 is parallel. SCR1 and SCR2 conduct alternately for 180 degrees each.

Transistor Q1 is controlled synchronously with the switch turn-on pulses which may be on for 180 degrees or less during each half cycle of operation. Controlling the "on-time" of transistor Q1 for 0 to 180 degrees in each half-cycle therefore allows continuous and smooth control of the output voltage; i.e., the voltage across resonant inductor-transformer L1. Switches SCR1 and SCR2 are "on" alternately for 180 degrees each; half cycle.

Conduction time of transistor Q1 is controlled by a closed loop which senses the output voltage.

A test of a series inverter of the type shown in figure 2-5 demonstrated the characteristic described above.

2.1.3 DESIGN ANALYSIS OF THE SERIES INVERTER WITHOUT PULSEWIDTH MODULATION

For simplicity in deriving the design equations for the series inverter, let us first assume that the load R is connected directly across the primary of L1, as shown in figure 2-6.

The dc input voltage E is connected directly to the series inverter. The ac voltage across L1 and load R is sinusoidal and its rms value is e. No losses are assumed in L1, C1, C2, SCR1 and SCR2. Capacitors C1 and C2 are charged and the polarities are as shown.

Upon firing of SCR2, the sinusoidal rms current i flows through the parallel combination of L1 and load R and at point A splits into two equal values of i/2. Each current reverses the polarity of the respective capacitors C1 and C2 in one-half cycle of oscillation. The

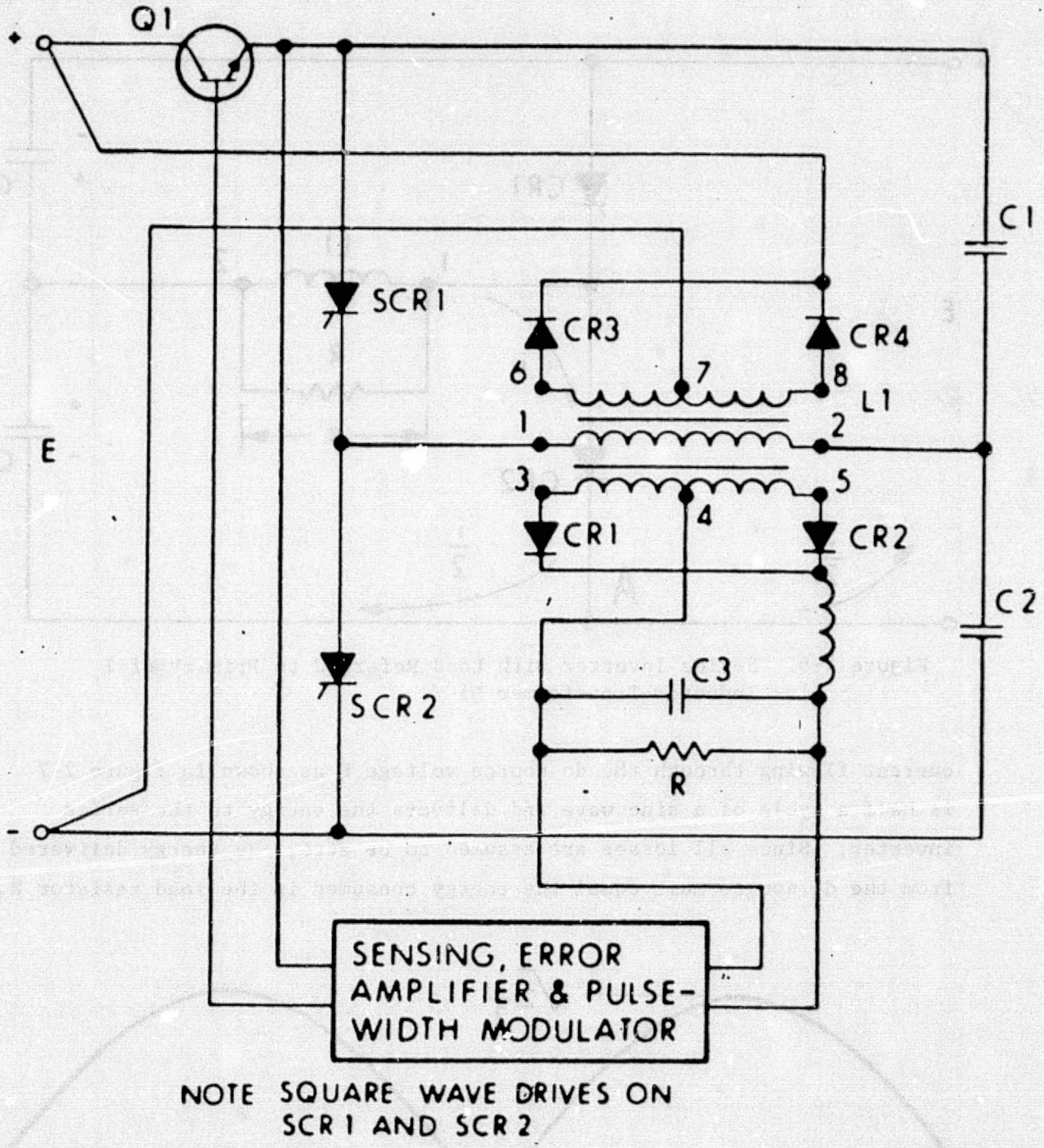


Figure 2-5. Regulated, Pulsewidth Modulated Series Inverter Supply with No-Load Protection

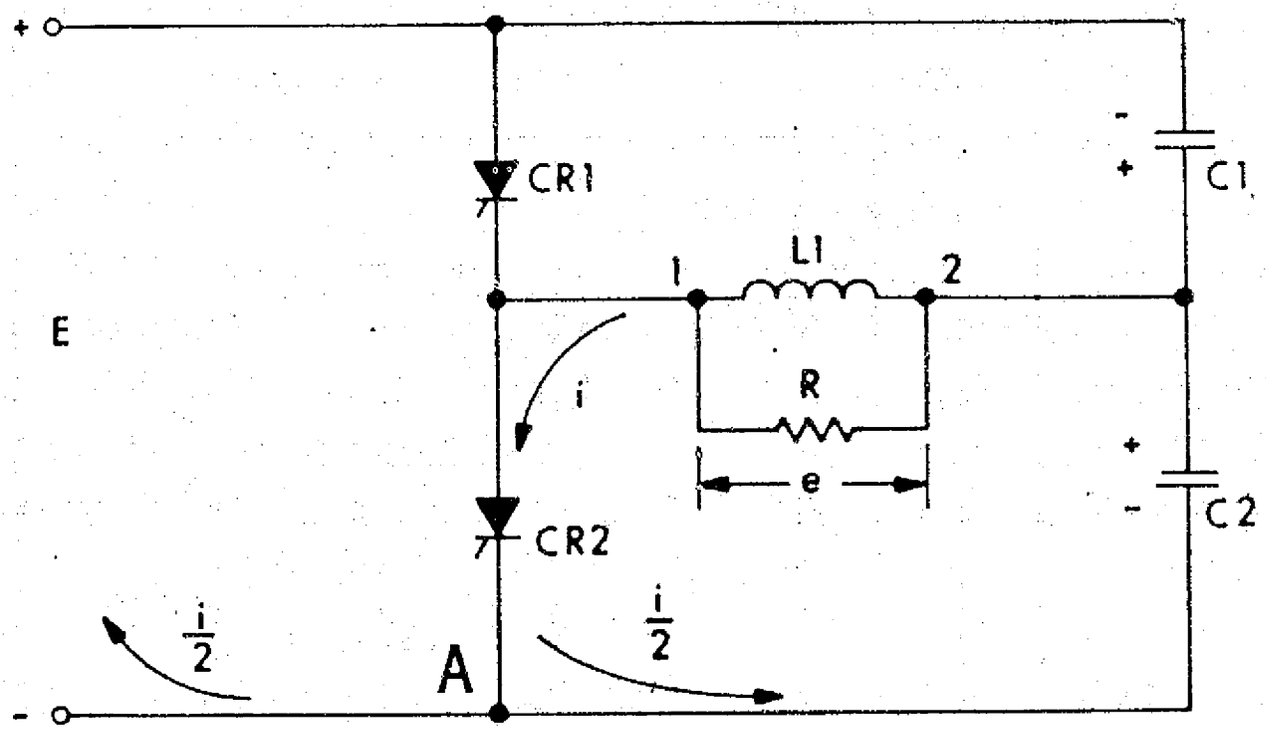


Figure 2-6. Series Inverter with Load Referred to Primary of I Inductor-Transformer L1

current flowing through the dc source voltage E as shown in figure 2-7 is half a cycle of a sine wave and delivers the energy to the series inverter. Since all losses are assumed to be zero, the energy delivered from the dc source must equal the energy consumed in the load resistor R.

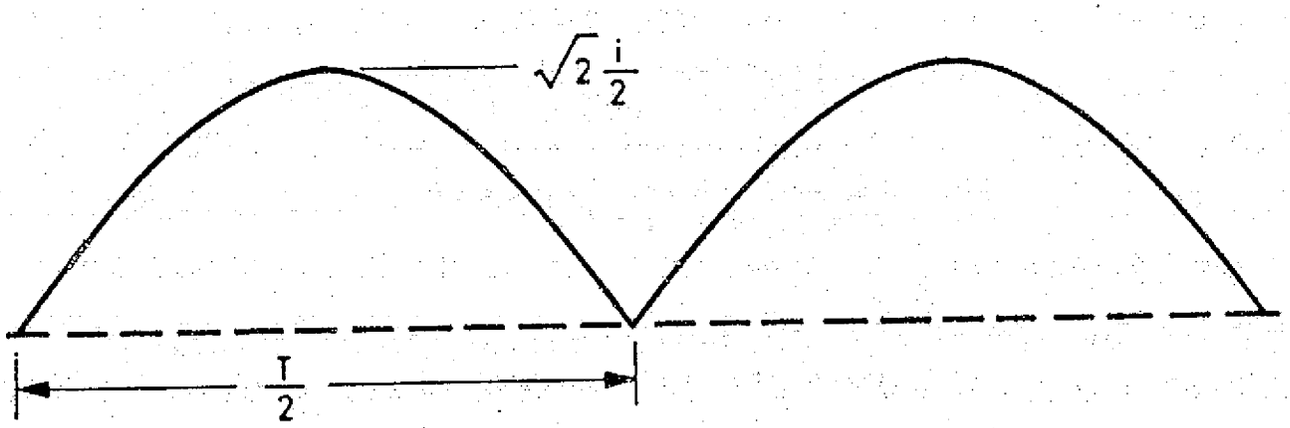


Figure 2-7. Current-Waveshape Through DC-Source E

The energy delivered by the dc source during one-half cycle is:

$$J_{in} = \int_0^{T/2} E\, i/2\, dt = E \int_0^{T/2} i/2\, dt \qquad (1)$$

Since i is sinusoidal, the solution of this integral is:

$$J_{in} = \frac{\sqrt{2}}{2\pi f} E\, i = \frac{E\, i}{4.44 \times f} \qquad (2)$$

where

E = dc input voltage
i = rms value of sinusoidal current
f = frequency (resonance)

The ac voltage e across and the current i through the parallel combination of L1 and R generate the real power

$$P = e\, i \cos \varphi \qquad (3)$$

where for this parallel combination:

$$\cos \varphi = \frac{1}{\sqrt{1 + \left(\frac{R}{\omega L}\right)^2}} \qquad (4)$$

In a half cycle of operation, the energy consumed in the load resistor R is then:

$$J_{out} = \frac{e\, i}{\sqrt{1 + \left(\frac{R}{\omega L}\right)^2}\ 2\, f} \qquad (5)$$

With no losses, J_{in} becomes equal to J_{out}. Combining Eqs. 2 and 5 yields the design equation:

$$e = \frac{\sqrt{2}}{\pi} E \sqrt{1 + \left(\frac{R}{\omega L}\right)^2} = 0.45\ E \sqrt{1 + \left(\frac{R}{\omega L}\right)^2} \qquad (6)$$

where

e = ac voltage across primary of inductor-transformer L1
R = load resistance referred to primary of inductor-transformer L1
ωL = primary impedance of inductor-transformer L1
E = dc input voltage

Assumptions:

1. No losses
2. Voltage waveshape across L1 remains sinusoidal

In most cases, the ratio of $\frac{R}{\omega L}$ is large compared to 1 and under this condition, Eq. 6 is simplified into

$$e \approx 0.45\ E \frac{R}{\omega L} \qquad (7)$$

$$R >> \omega L$$

These equations are, of course, valid only if the dc voltage E is applied continuously and is not subject to pulsewidth modulation.

2.1.4 DESIGN ANALYSIS OF THE SERIES INVERTER WITH PULSEWIDTH-MODULATION

For reasons of simplicity in deriving the design equation, let us assume that the load R is connected directly across the primary of inductor-transformer L1 as shown in figure 2-8.

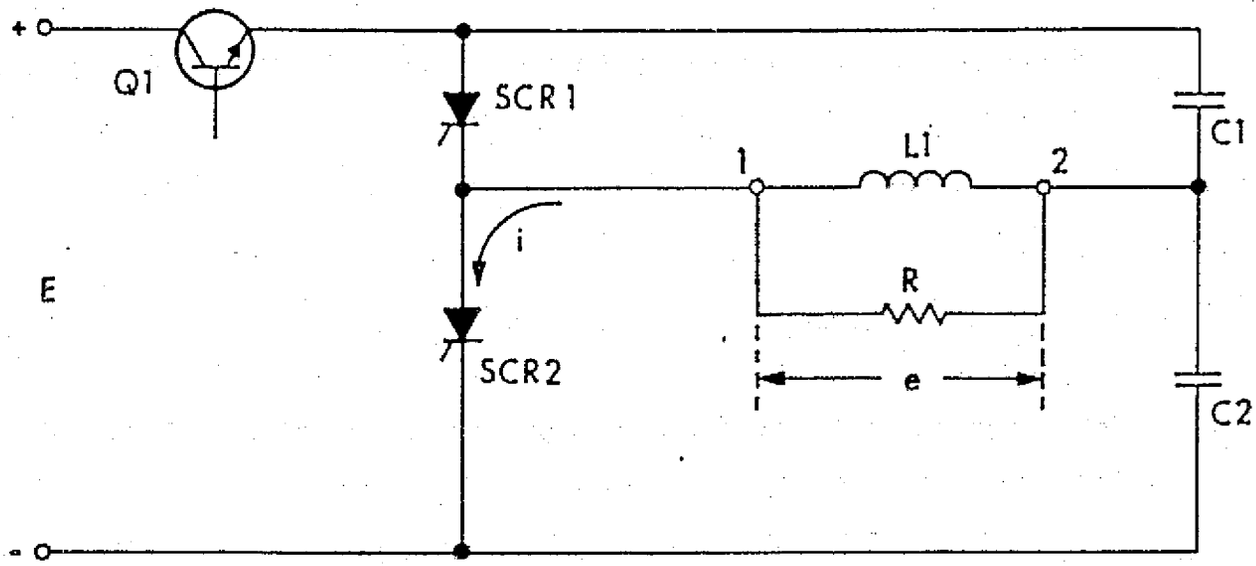


Figure 2-8. Series Inverter with Load Connected Across the Primary of Inductor-Transformer L1 and with Input-Voltage Pulsewidth Modulation

Under conditions of pulsewidth modulation, transistor Q1 controls the time during which the dc input source is connected to the series inverter during each half cycle of operation. The conduction or "on" time of transistor Q1 can vary between 0 and 180 degrees as shown in figure 2-9.

The current waveshape through the dc source during the "on-time" of transistor Q1 is shown in figure 2-9.

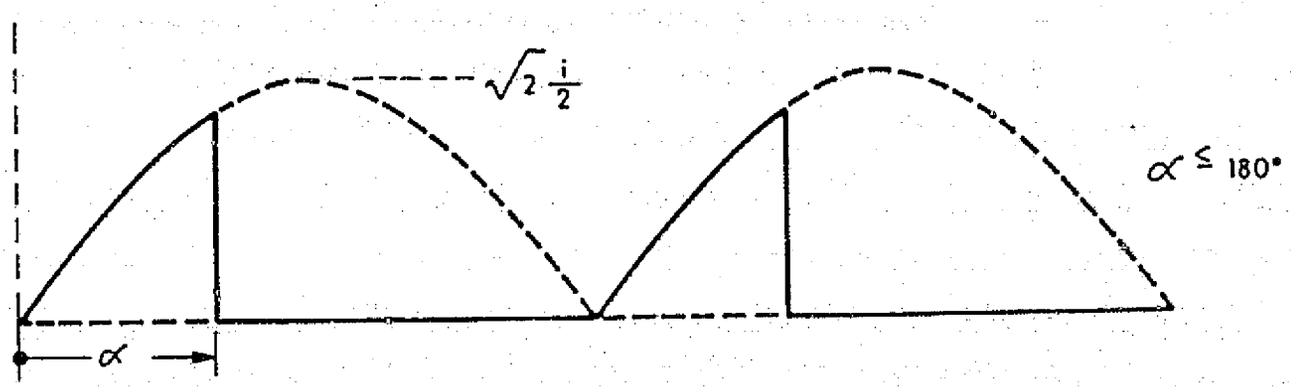


Figure 2-9. Current Waveshape Through DC-Source E

The energy delivered during one-half cycle of operation and during the conduction angle α of the transistor Q1 is

$$J_{in} = \frac{\sqrt{2}}{4\pi f} E\, i\, (1 - \cos \alpha)$$

$$J_{in} = \frac{E\, i}{4.44 \times 2f} (1 - \cos \alpha);\ 0 \leq \alpha \leq 180 \qquad (8)$$

The design equation for the ac voltage across the primary of the inductor-transformer L1 then becomes

$$\boxed{e = \frac{0.45}{2} E \sqrt{1 + \left(\frac{R}{\omega L}\right)^2} (1 - \cos \alpha)} \qquad (9)$$

In most cases where the ratio of $\frac{R}{\omega L}$ is large compared to 1, Eq. 9 can be simplified into

$$e = \frac{0.45}{2} E \frac{R}{\omega L} (1 - \cos \alpha) \qquad (10)$$

where

- e = ac voltage across primary of inductor-transformer L1
- E = dc input voltage
- R = load resistor referred to primary of inductor-transformer L1
- ωL = primary impedance of inductor-transformer L1
- α = conduction angle of transistor Q1; $\alpha \leq 180^{o}$

Assumptions:

1. No losses
2. Voltage waveshape across L1 remains sinusoidal
3. The load current waveshape remains sinusoidal.

The actual application requires rectification and output filters which shape the output current waveshape into the rectangular form. This change of the waveshape affects the above equations and would have required investigation if this circuit had been selected for further study.

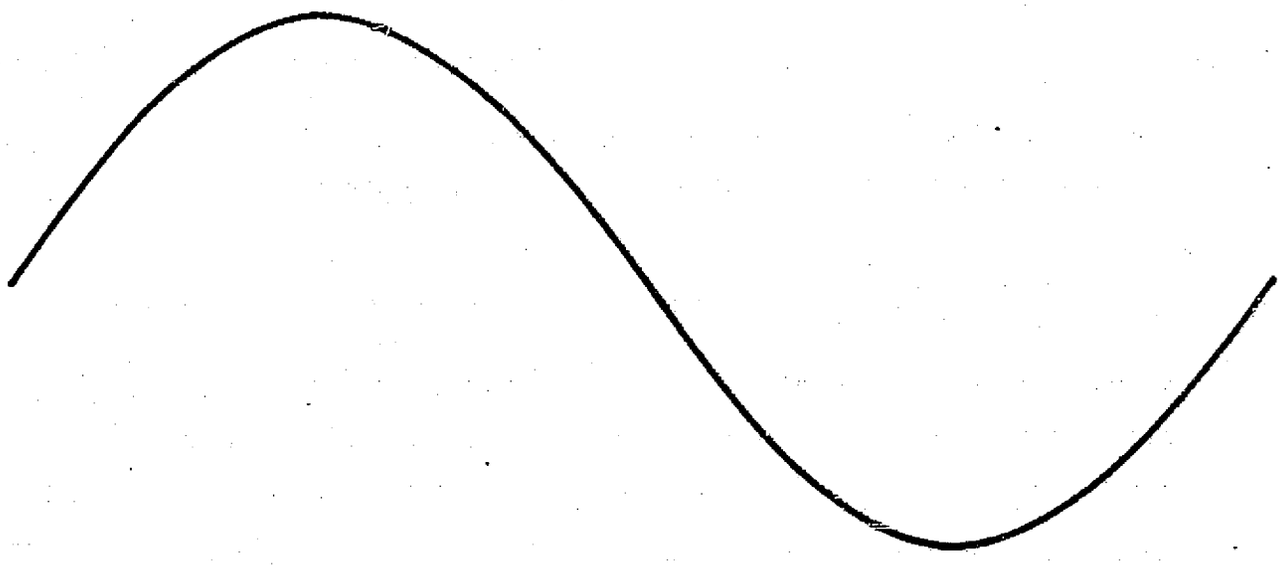
The voltage waveshapes occurring in the series inverter are best understood by remembering that only the current from one of the two capacitors C1 or C2 flows through the dc source during each half-cycle as shown in figure 2-6. As long as this current flow through the dc source is uninterrupted, during each half cycle the voltage waveshape across each capacitor will remain sinusoidal as shown in the upper trace of figure 2-10. With pulsewidth modulation of the input voltage, however, this current is interrupted and the associated capacitor ceases to carry current, and its voltage remains at a constant potential. This causes a flat-top to its voltage waveshape as shown in the lower trace of figure 2-10. Under varying pulsewidth modulation, the flat-top on one-half of the sinusoidal waveshape moves up and down. The same waveshape appears across the other capacitor except that it is shifted 180 degrees.

The voltage waveshapes, as shown, result when the series inverter is running slightly below the resonance frequency. If the inverter is driven at the no-load resonance frequency, the flat-top portion of the capacitor voltage waveshape shows part of the sine wave protruding above the lagging edge of the flat-top. Although this has no ill effects on the efficiency, cleaner voltage and current waveshapes result when the inverter is run slightly below the resonance frequency.

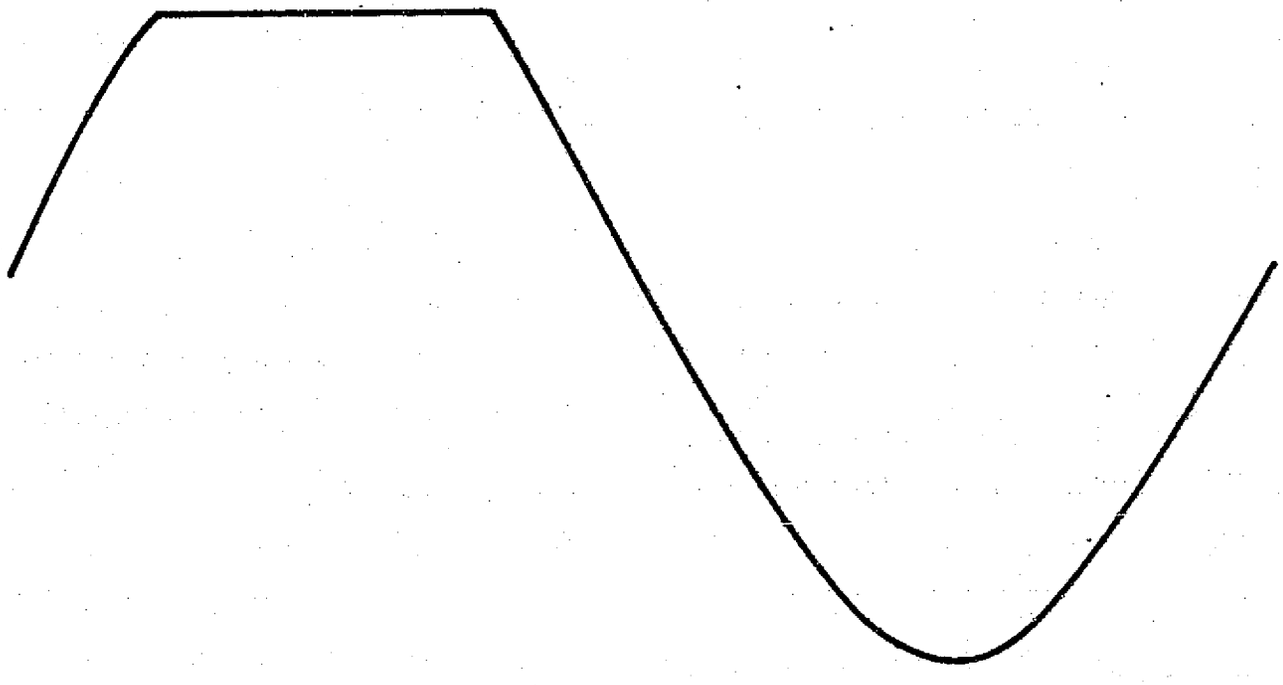
2.1.5 TEST RESULTS

A series inverter circuit as depicted in figure 2-5 was designed, built and tested with both ac and dc loads.

Inductor-transformer L1 was constructed with two stacked molybdenum permalloy powder cores (Magnetics Inc. 55110-A2). It had a primary



VOLTAGE WAVESHAPE ACROSS CAPACITOR C2 WITHOUT PULSEWIDTH MODULATION



VOLTAGE WAVESHAPE ACROSS CAPACITOR C2 WITH PULSEWIDTH MODULATION

Figure 2-10. Effects of Pulsewidth Modulation on Series Inverter

inductance of 1.06 mH operating at a flux density of 3.72 kG at 5 kHz. The two resonant capacitors were polycarbonate capacitors of 0.5 μF each. At a ratio of $R/\omega L = 2$, this power stage was capable of delivering maximum power in excess of 500 watts.

The power stage switches were either transistors or silicon controlled rectifiers (SCRs) which were driven by a 5 kHz squarewave source. The modulating switch was a transistor.

The test results without pulsewidth modulation are shown in figures 2-11 and 2-12 both for the transistor and the SCR power stages. These curves reflect efficiency, output power, output voltage, input power and input dc voltage, as a function of the ratio $R/\omega L$ and cover an output power range of 100 to 560 watts at a constant primary voltage of 200 Vac.

The test results were essentially the same whether the output stage switches were transistors or SCRs. Based upon these data, the Series Inverter presented a rather encouraging start with efficiency varying between 85 and 91 percent.

When pulsewidth modulation was initiated, a rather distinct characteristic of this circuit approach became apparent.

In the discussion of the theory of the series inverter, it was shown that one-half of the current through the inductor transformer flows through the dc-input source, whereas the other half flows through the power stage switch into the associated capacitor (see figure 2-6) and reverses its polarity. However, both capacitors carry equal currents. During pulsewidth-modulation, the current flow of one capacitor is interrupted and does not flow through the input source. This capacitor no longer changes its voltage and shows the characteristic flat-top voltage waveshape (see figure 2-10). During this time, however, the other capacitor maintains its uninterrupted current flow and as no energy is delivered during the off time of the pulsewidth modulating transistor, it delivers

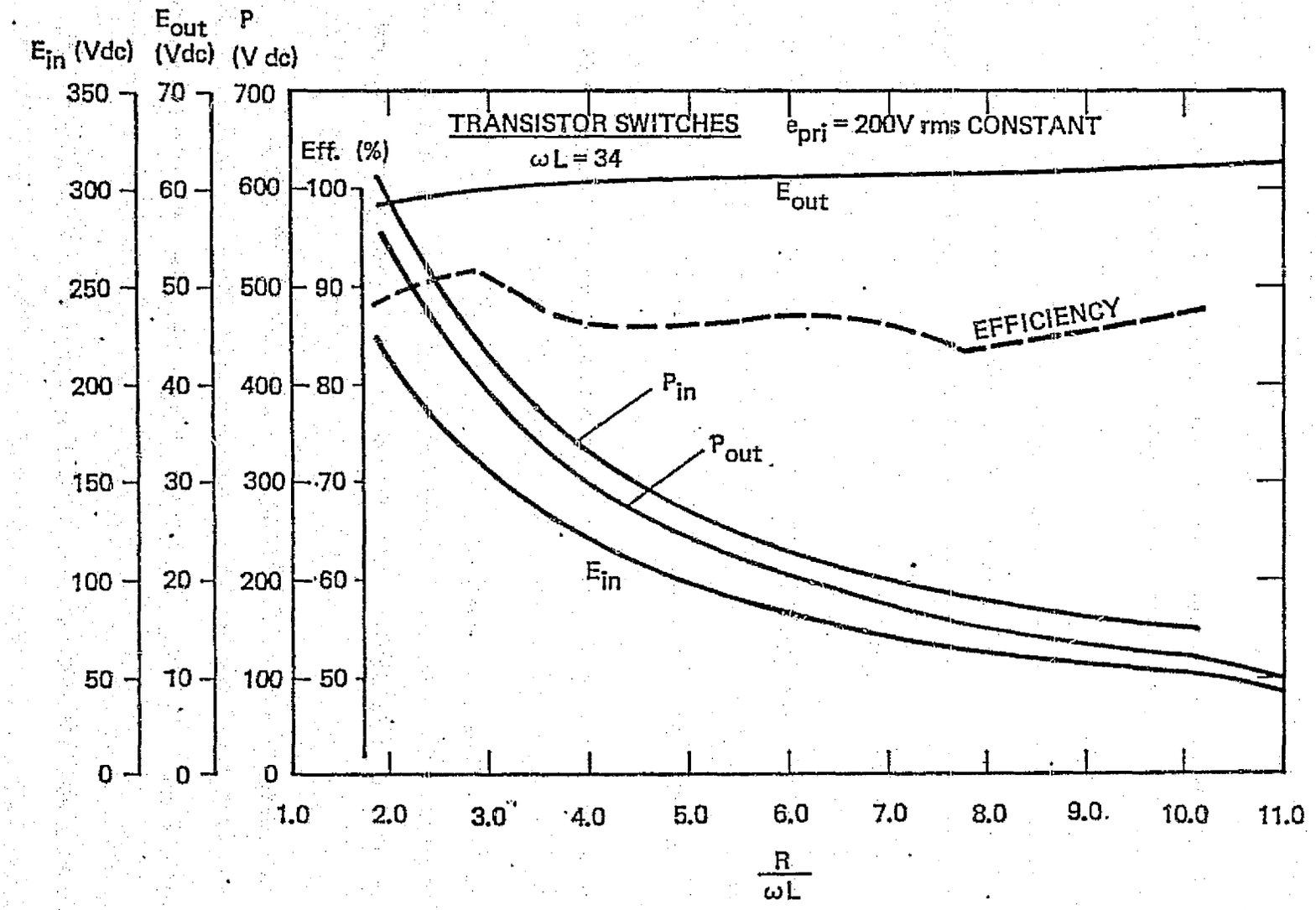


Figure 2-11. Test Results of the Series Inverter with Transistor Switches

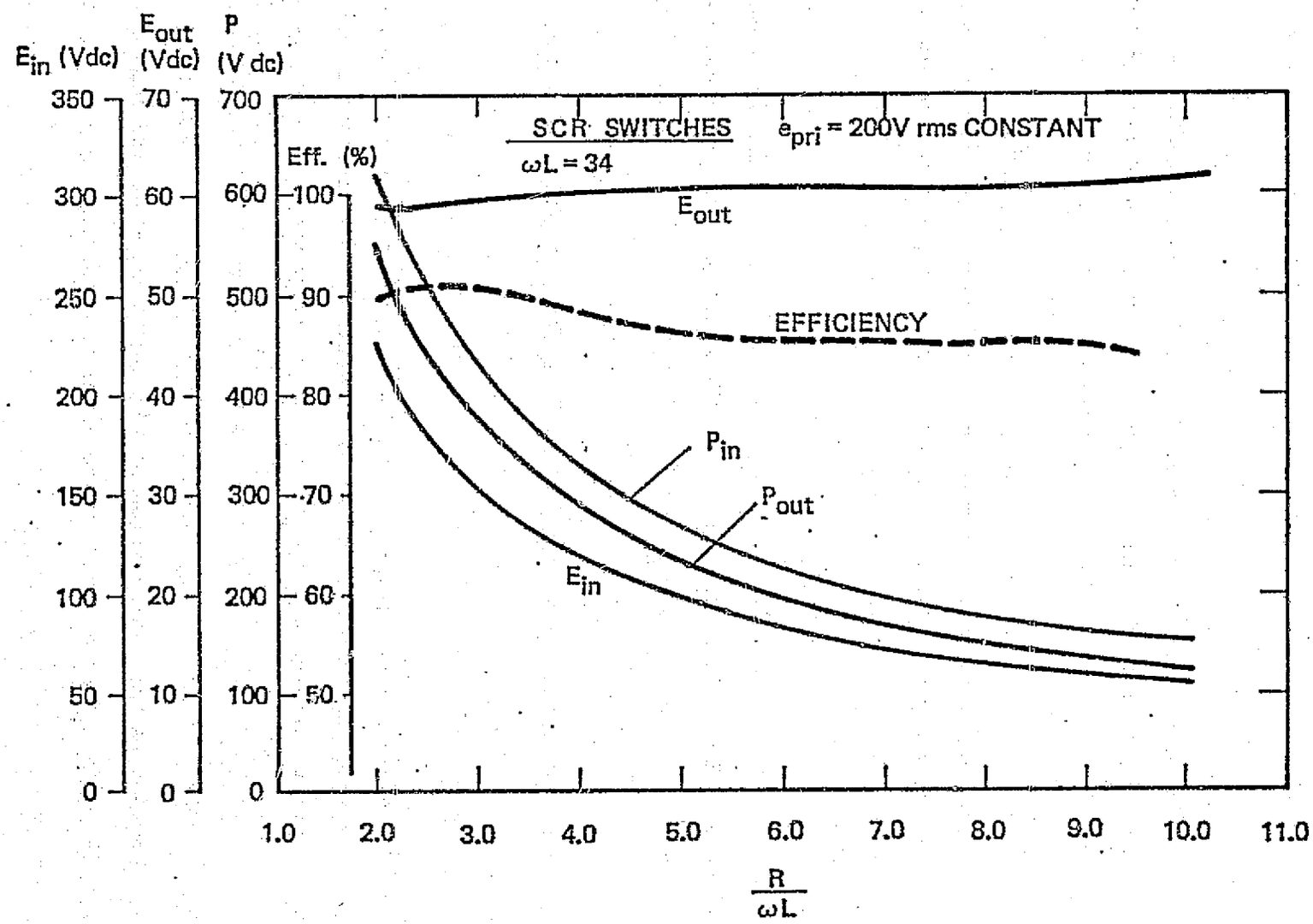


Figure 2-12. Test Results of the Series Inverter with SCR Switches

energy into the load. By doing so, it does lose part of its stored energy. It also does not recover to the full voltage which upsets the requirement that the sum of the voltages across both capacitors must be equal to the input voltage. Upon turn-on of the modulating transistor, the input voltage is applied not only to the power stage but also directly to the series connection of capacitors C1 and C2. As a consequence, a large in-rush current from the dc source through the modulating transistor is required to restore the voltage balance across capacitors C1 and C2. The magnitude of the in-rush current is limited only by the dc source impedance, the saturating characteristic of the modulating transistor, the wire connections, and the equivalent series resistance (ESR) of the two capacitors C1 and C2. As all of these impedances are small, the resulting in-rush current excees the capabilities of present day transistors.

This adverse characteristic of the series inverter was the principal reason for halting further efforts in this area and for continuing with the investigation of the inductive energy transfer (IET) system since no simple solution was available to overcome this problem.

2.2 THE INDUCTIVE ENERGY TRANSFER SUPPLY WITH MULTIPLE STAGES

2.2.1 THEORY OF OPERATION

The basic circuit diagram of an inductive energy transfer supply with two stages is shown in figure 2-13. A detailed description of the operation of an inductive energy transfer system is contained in the paper "Regulated Energy Transfer by Inductor Transformers for Single and Multiple Stages", (see Appendix D)

However, a brief discussion of the operation of an inductive energy transfer system is in order here.

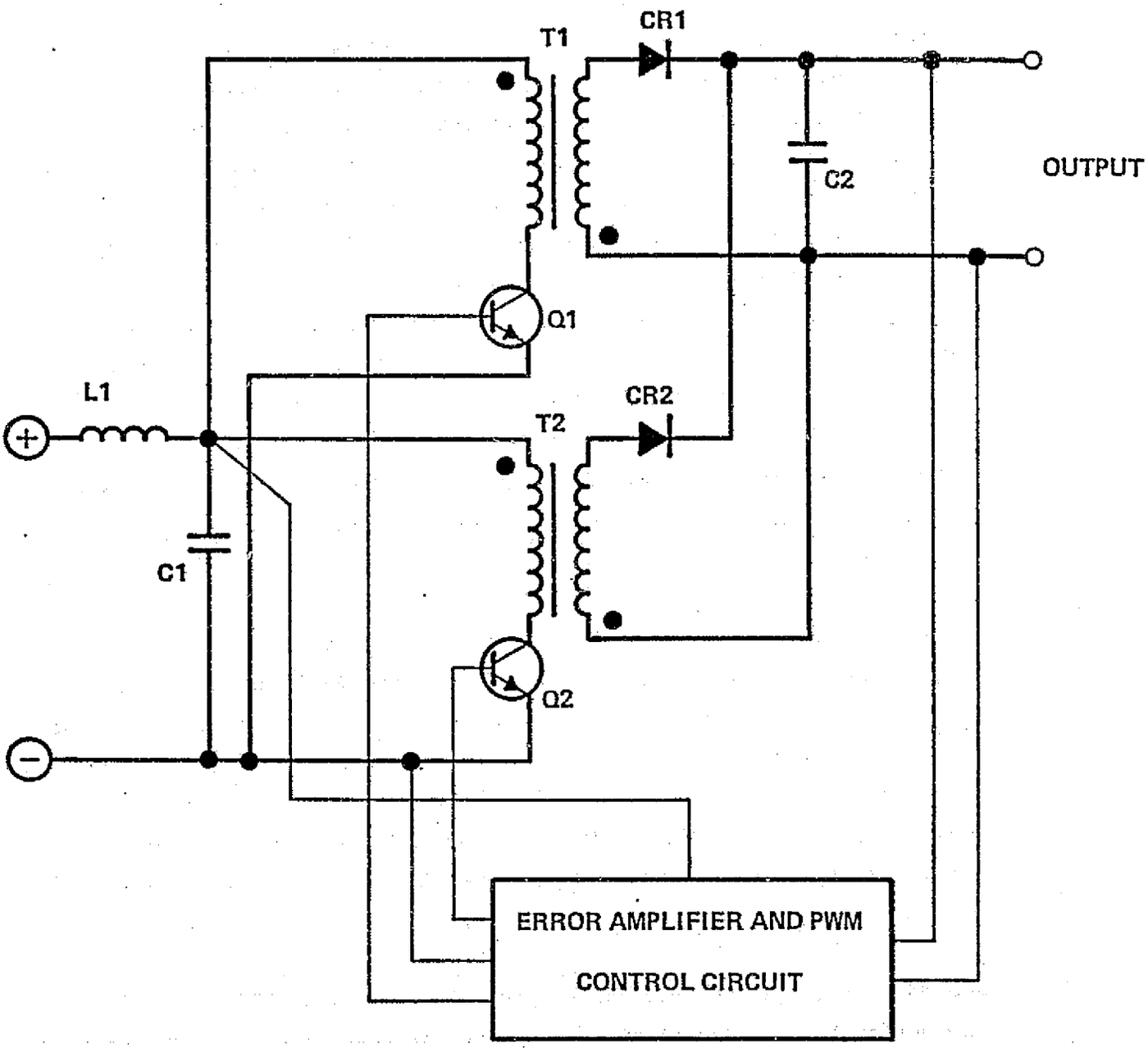


Figure 2-13. Inductive Energy Transfer Supply (2 Stages)

Consider the upper stage in figure 2-13 which consists of inductor-transformer T1, transistor switch Q1, diode CR1 and capacitor C2; assume that transistor Q1 is turned on from time zero to time t_1. During this period, the primary winding of inductor transformer T_1 is connected to the dc source and the current in the primary winding will increase linearly as long as the inductance of the inductor-transformer is constant. At the same time, the polarity of the secondary winding is such that diode CR1 is blocking current flow and thus isolates the secondary from the primary. At time t_1, transistor Q1 is turned off and since the ampere-turns on an inductor cannot change instantaneously, the secondary winding of the inductor-transformer T1 takes over with the same ampere-turns which were flowing at the moment of turn-off. The secondary now transfers energy into capacitor C2 and into the output load. As explained in Appendix D, the waveshape of the current through the primary and the secondary may be either triangular or trapezoidal. The dividing line between these two conditions is termed <u>critical resistance</u>. At any load resistance value below the critical value, there is no interrupted current flow on the inductor-transformer and the current waveshape becomes trapezoidal. It is the intent of this design to use only trapezoidal waveshapes and as such operate with load resistances below R_{crit}. To assure that operation is always below the critical resistance value, we must consider the minimum load requirement inasmuch as this determines the minimum value of inductance necessary to maintain an uninterrupted current flow. This minimum inductance which is calculated for the secondary side and always assures trapezoidal current waveshapes of the inductor-transformer is labeled $L_{min_{sec}}$.

The governing equation for the proper operation of an IET system is that the positive edt be equal to the negative or reset edt. We can therefore write:

$$\frac{E_{in}}{n_1} \times t_{on} = \frac{E_{out}}{n_2} t_{off} = \frac{E_{out}}{n_2} \left(T - t_{on}\right)$$

where

E_{in} = input voltage

E_{out} = output voltage

n_1 = primary number of turns

n_2 = secondary number of turns

t_{on} = conduction time of switching transistor

t_{off} = off time of switching transistor

T = $t_{on} + t_{off}$ = period of one cycle

k = $\frac{n_1}{n_2}$ = ratio of primary to secondary turns

$$t_{on} = \frac{T}{1 + \frac{E_{in}}{E_{out}} \times \frac{n_2}{n_1}} \tag{11}$$

and the duty cycle D is

$$D = \frac{t_{on}}{T} = \frac{1}{1 + \frac{E_{in}}{E_{out}} \times \frac{n_2}{n_1}} \tag{12}$$

To maintain a trapezoidal current waveshape under all conditions and hence an uninterrupted current flow in an IET stage, a minimum secondary inductance $L_{min_{sec}}$ is required. Its value is dependent on the frequency f, the minimum output power P_{min}, the output voltage E_{out}, and the duty cycle D or the ratio of on-time over period $\frac{t_{on}}{T}$. The equation for the required minimum secondary inductance is

$$L_{min_{sec}} = \frac{\left(E_{out}\right)^2}{2\,P_{min}\,f}\left(1 - \frac{t_{on}}{T}\right)^2 = \text{Minimum secondary inductance} \tag{13}$$

These three equations govern the behavior of this type of an Inductive Energy Transfer system.

Equation 11 shows that the on-time of the switching transistors is proportional to the period but is inversely proportional to the ratio of the input over output voltage and the ratio of primary turns to secondary turns.

Equation 12 gives the values for the duty cycle D and is independent of frequency. It shows that the turns ratio plays an important role in the value of the duty cycle.

Equation 13 shows the minimum required secondary inductance which guarantees an uninterrupted current flow.

A computer program was generated for a single stage inductive energy transfer system with an output power of 250 watts at a frequency of 5 kHz. The output voltage was kept constant at 56 volts dc. Table 2-1 shows an excerpt from this run. The parameters of maximum blocking voltage across the input switch E3, the duty cycle D, the peak end value of the input current I3, the peak start value of the output current A3, the rms input current I4, the rms output current A4, the rms input ripple current I6, the rms output ripple current A6, the minimum secondary inductance $L_{min_{sec}}$ required to maintain an uninterrupted current flow at a minimum power of 50 watts, and the required magnetic core power handling capability in cm^4 are tabulated as a function of the turns ratio K and the input voltage E_{in}. It should be noted that with the exception of cm^4 and $L_{min_{sec}}$, all values in table 2-1 are independent of frequency.

This tabulation shows some very interesting results. At a turns ratio of 2, the maximum blocking voltage is 512 volts. The duty cycle varies between 35.9 and 21.9 percent. The maximum peak current on the primary is 4.18 amperes and the maximum peak current on the secondary is 8.36 amperes. The maximum rms input current is 2.10 amperes and the

TABLE 2-1

COMPUTER CALCULATED VALUES FOR ONE STAGE OF 250 WATT CAPABILITY AS A FUNCTION OF DIFFERENT TURNS RATIOS AND VARYING INPUT VOLTAGES
(See Appendix A)

$K = \frac{N1}{N2}$	E_{in} [V]	E_3 [V]	D	I3 [A]	A3 [A]	rms I4 [A]	rms A4 [A]	rms Ripple Current I6 [A]	rms Ripple Current A6 [A]	L_{min} sec mH	cm^4 max
	200		0.218	6.86	6.86	2.69	5.08	2.38	2.43		40.458
1	300		0.157	6.36	6.36	2.11	4.89	1.94	2.01		
	400	456	0.123	6.11	6.11	1.79	4.80	1.68	1.76	4.83	
	200		0.359	4.18	8.36	2.10	5.61	1.69	3.40		42.039
2	300		0.272	3.68	7.36	1.61	5.27	1.38	2.79		
	400	512	0.219	3.43	6.86	1.34	5.08	1.19	2.43	3.83	
	200		0.456	3.285	9.85	1.86	6.09	1.38	4.15		42.289
3	300		0.359	2.78	8.36	1.40	5.61	1.125	3.40		
	400	568	0.296	2.53	7.61	1.16	5.35	0.97	2.96	3.11	
	200		0.528	2.84	11.36	1.73	6.54	1.20	4.78		42.289
4	300		0.427	2.34	9.36	1.28	5.94	0.97	3.92		
	400	624	0.359	2.09	8.36	1.05	5.61	0.84	3.40	2.58	
	200		0.583	2.57	12.86	1.65	6.96	1.07	5.34		42.164
5	300		0.483	2.07	10.36	1.21	6.25	0.87	4.37		
	400	680	0.412	1.82	9.11	0.98	5.86	0.75	3.79	2.17	
	200		0.627	2.39	14.36	1.59	7.36	0.98	5.85		42.039
6	300		0.528	1.89	11.36	1.15	6.54	0.80	4.78		
	400	736	0.456	1.64	9.86	0.93	6.09	0.69	4.15	1.85	
	200		0.662	2.26	15.86	1.55	7.73	0.91	6.31		41.623
7	300		0.566	1.76	12.36	1.11	6.82	0.74	5.16		
	400	792	0.494	1.51	10.61	0.29	6.32	0.64	4.48	1.60	
	200		0.691	2.17	17.36	1.51	8.09	0.85	6.74		41.498
8	300		0.599	1.67	13.36	1.08	7.10	0.69	5.51		
	400	843	0.528	1.42	11.36	0.86	6.54	0.60	4.78	1.395	
	200		0.716	2.09	18.86	1.49	8.43	0.80	7.15		41.290
9	300		0.627	1.59	14.36	1.06	7.36	0.65	5.84		
	400	904	0.557	1.34	12.11	0.84	6.75	0.56	5.07	1.28	
	200		0.737	2.03	20.36	1.46	8.76	0.76	7.53		41.040
10	300		0.651	1.536	15.36	1.04	7.61	0.62	6.16		
	400	960	0.583	1.286	12.86	0.82	6.90	0.54	5.34	1.09	

maximum rms output current is 5.61 amperes. The minimum secondary required inductance is 3.83 millihenry and the required cm^4 rating is 42.0 cm^4. Of specific interest is that, at these conditions, the minimum duty cycle is 21.9 percent. At a frequency of 10 kHz, this represents an on-time of only 21.9 microseconds.

The other extreme is seen when we select a turns ratio of $n_1/n_2 = 5$. In this case, the blocking voltage becomes 680 volts and the duty cycle will vary from 58.3 to 41.2 percent. The peak input current has become 2.57 amperes and the peak output current has become 12.86 amperes. The maximum rms input current has dropped to 1.65 amperes and the maximum rms output current has increased to 6.96 amperes. The minimum secondary inductance has dropped to 2.17 millihenry. The required power handling capability of the core remains about constant and is 42.1 cm^4.

This tabulation clearly shows that the trade-offs between turns ratio, blocking voltage, acceptable peak current, acceptable rms currents, and acceptable minimum inductances need to be made very carefully and require the use of a computer.

The computer values were based on a single IET stage with an output power of 250 watts at 5 kHz. In subsequent investigations, a minimum of 2 stages and a maximum of 8 stages was used because this reduced the ripple current and prevented an interrupted current flow in the primary and/or secondary. It is theoretically possible to increase the number of stages and have them staggered in such a way that almost no ripple current will be present either on the primary or on the secondary. This approach eventually leads to very complex circuitry.

For illustration, figures 2-14 and 2-15 show the waveshapes of a 4-stage inductive energy transfer system where the stages are staggered 90 degrees from each other. With an increasing number of stages, the ripple frequency increases and the amplitude of the ripple current

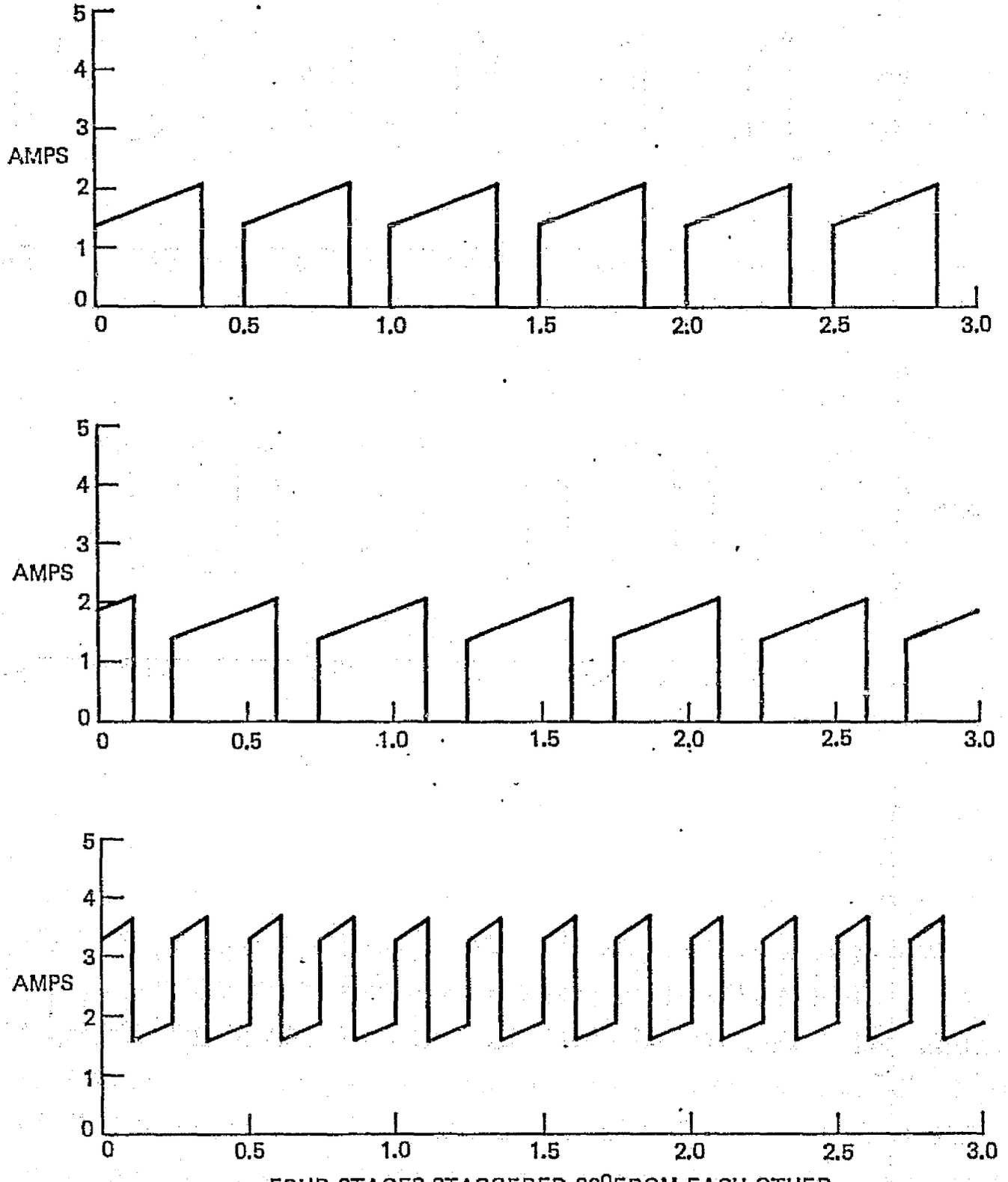
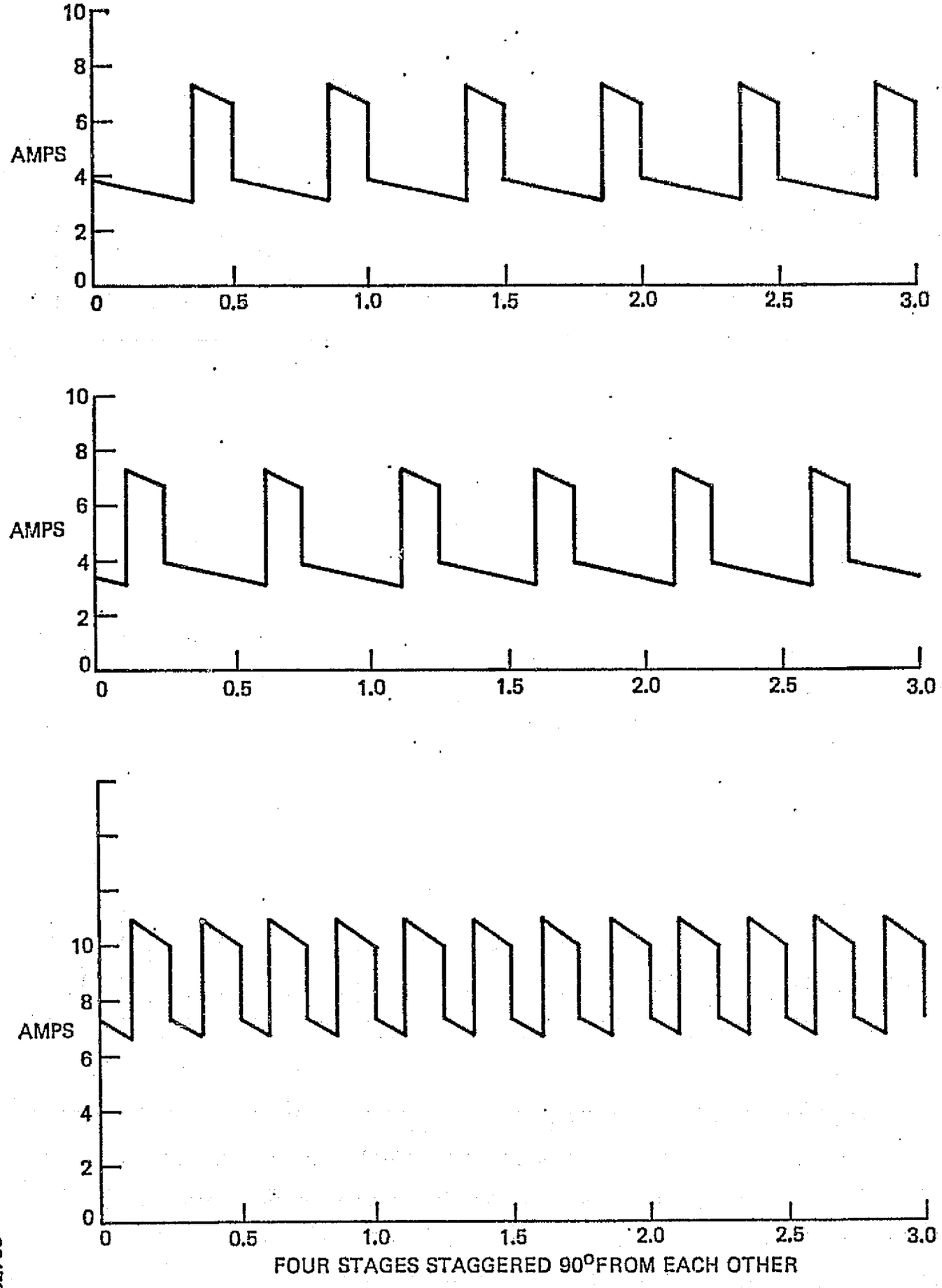


Figure 2-14. Primary Current Waveshapes for a 4-Stage Inductive Energy Transfer Circuit

52765



52766

Figure 2-15. Secondary Current Waveshapes for a 4-State Inductive Energy Transfer Circuit

decreases; the power-per-stage also decreases when the total power is kept constant. Based on figures 2-14 and 2-15, we can now understand that the filter capacitance will get smaller as more stages are employed in the power conversion unit.

The operation of the IET supply with trapezoidal current waveshapes is both desirable and beneficial. It does, however, also pose some characteristic problems during the parallel operation of multistage, staggered units. Therefore, a clear understanding of the generation of the trapezoidal current waveshapes is necessary.

2.2.1.1 Generation of Trapezoidal Current Waveshapes

For ease of understanding, let us consider operation with the following assumptions, namely:

E_{in} = constant

t_{on} = constant

t_{off} = constant

T = constant

From the previous statement, we know that with a load resistance of $R = R_{crit}$, operation occurs at an output voltage which is just sufficient to reset the core in the available time of t_{off}. This output voltage is:

$$E_{out} = \frac{E_{in} t_{on}}{t_{off}} \left(\frac{n_2}{n_1}\right); \text{ Valid for trapezoidal current waveshapes only} \qquad (14)$$

$$R \leq R_{crit} ,$$

If we continue to lower R and expect the core to reset properly when $E_{in}t_{on}$ = constant, then E_{out} must remain constant. Equation 14 is, therefore, not only valid when $R = R_{crit}$, but must also be valid when $R < R_{crit}$.

We can now complete the curve for the output voltage as a function of the load resistor in figure 2-16. It is constant at load resistor values below R_{crit}.

Let us now investigate the trapezoidal current waveshape in more detail and see how it comes into being. For this purpose, let us again assume that E_{in}, t_{on} and t_{off} are constant and that the load resistor is equal to R_{crit}. Therefore, the circuit is operating on the borderline between triangular and trapezoidal current waveshapes. Primary and secondary current waveshapes are as shown in figure 2-17 to the left of t_o. At a turns ratio of $n_1/n_2 = 1$, the change in current ΔI is equal in both primary and secondary. The output voltage has adjusted itself such that it takes the full time of t_{off} to reset the core and to bring the secondary winding current back to zero at the end of t_{off}. Now, at time t_o let us change R to a value less than R_{crit}. This will begin to lower the output voltage but does not yet affect the input current between the times t_o and t_1. At t_1, the secondary winding still takes over with the same peak current. The slope of the current, however, is now smaller as the output voltage has decreased and at t_2 the secondary current has only decreased by ΔI_1. Now at t_2, the primary is turned on again and, as no abrupt change in ampere-turns can occur, it must begin to conduct with the same ampere-turns represented by I_{low}. The constant input voltage E_{in} and the same t_{on} produce the same ΔI as before and at t_3, the input current has reached a new peak value $I_{low} + \Delta I$. Looking at the shape of the primary current between the times t_2 and t_3 clearly shows a considerable increase in current and, consequently, an increase in input power. The increased primary current is transferred into the secondary between the times t_3 and t_4. This increased current causes

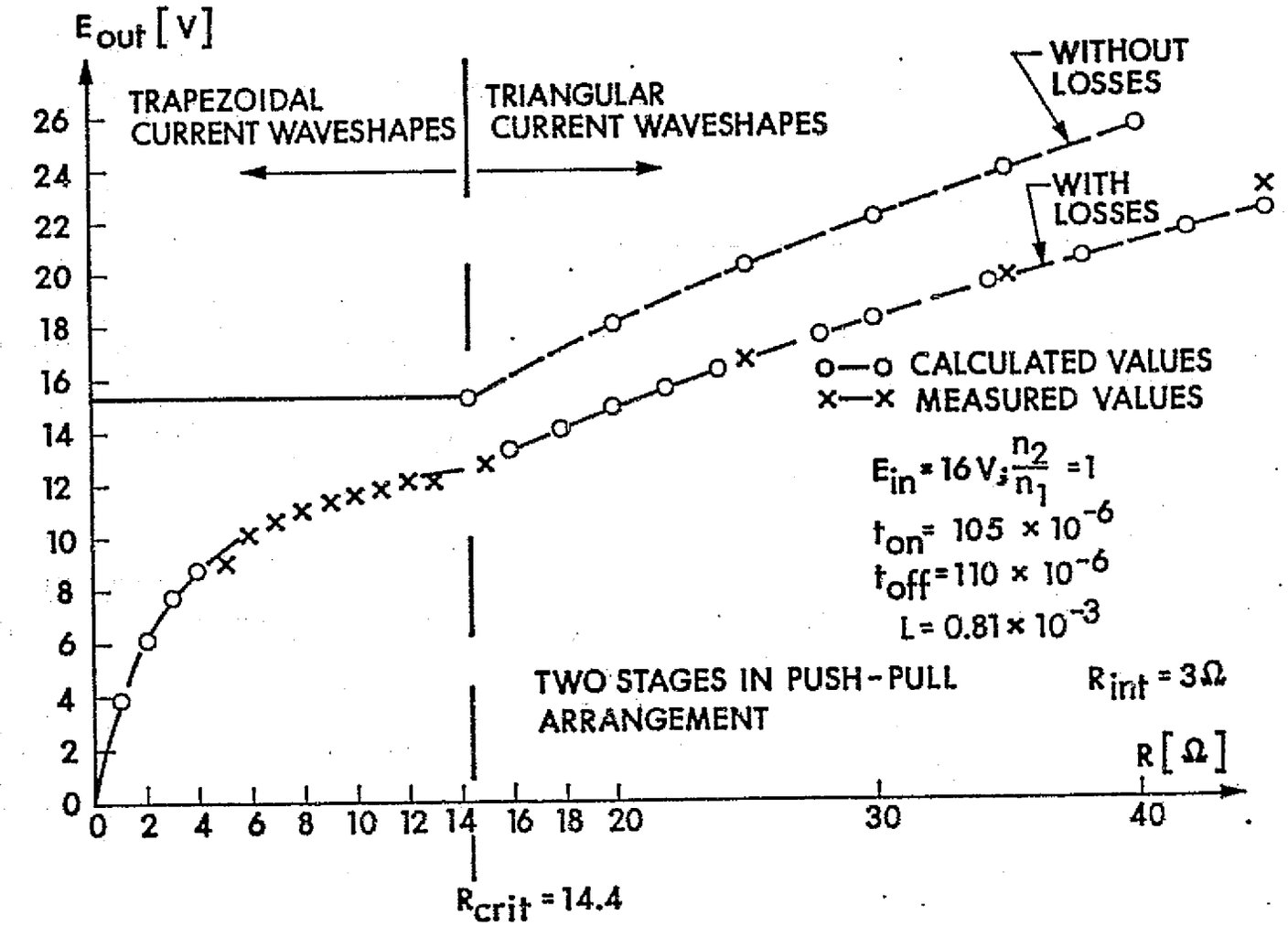


Figure 2-16. Output Voltage as Function of Load Resistance R Without and With Losses

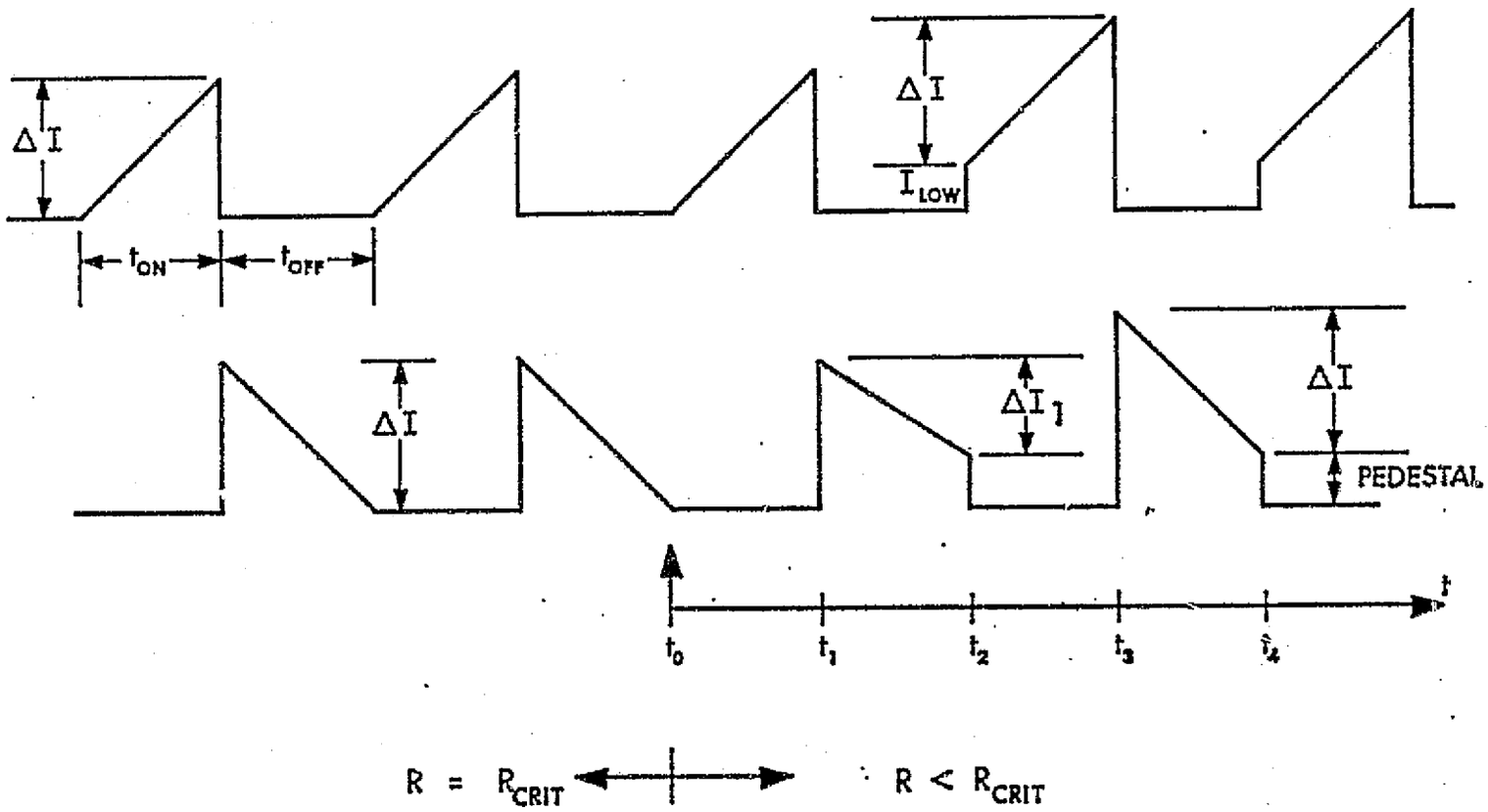


Figure 2-17. Transition from Triangular to Trapezoidal Current Waveshapes

the output voltage to climb until the same output voltage is restored as before. At this time, the old ΔI is also re-established as shown between t_3 and t_4. The circuit has reached a new stable operating condition, but now with trapezoidal current waveshapes and at a higher power output level.

It is important to note that the trapezoidal current waveshapes consist of a pedestal upon which rides ΔI caused by edt. Where ΔI is strictly subject to the condition that the positive edt is equal to the negative edt, one has to keep clearly in mind that the height of the pedestal is generated by an IET system only in order to generate the proper reset voltages. If somehow, as we shall see later, this voltage is delivered from other sources, the pedestal may become higher or lower than expected and thus becomes a very important aspect in equal power sharing for multiple, parallel operating stages.

2.2.1.2 Performance Characteristics With Losses

All equations derived so far are valid under the assumption that all losses are zero. Without going into a detailed analysis, let us simply assume as in figure 2-18, that all losses are concentrated in one resistor R_{int} which is in series with the load resistor and is inside the filtering effect of capacitor C. It is understood that this simplification is not in rigid agreement with the actual loss situation, but it gives us a simple insight into the output voltage characteristic as a function of R.

Figure 2-18 shows a two-stage push-pull arrangement and, consequently, Eq. 15 holds true.

$$E_{out} = \frac{E_{in} t_{on}}{t_{off}} \left(\frac{n_2}{n_1}\right) \; ; \quad R \leqq R_{crit} \text{ and results in trapezoidal current waveshapes} \qquad (15)$$

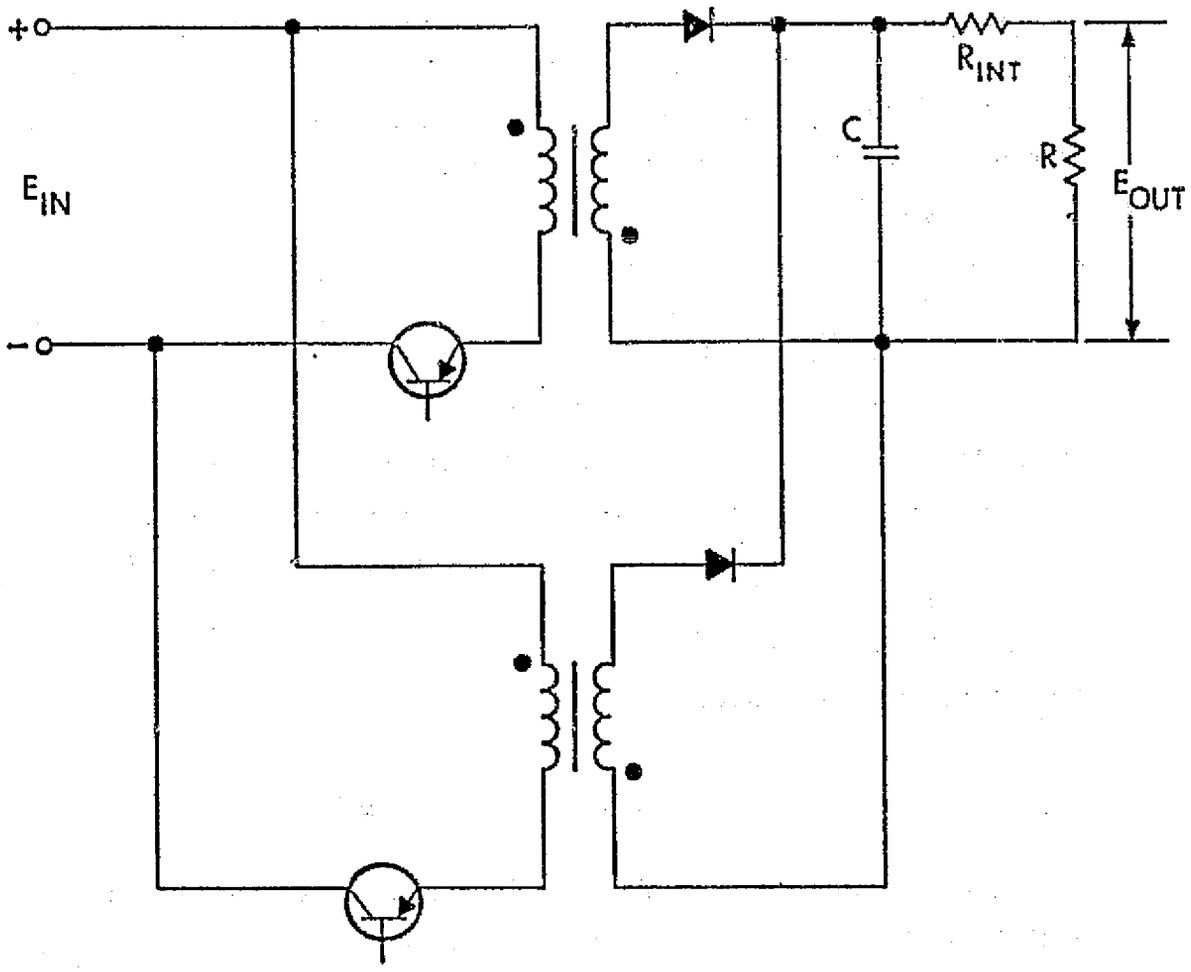


Figure 2-15. Two Stage Circuit with Lumped Losses

This output voltage, however, then appears across the series load combination of R_{int} and R. The actual output across R is then attenuated by $\frac{R}{R_{int} + R}$, and we write for the output voltage across R

$$E_{out} = \frac{\frac{E_{in} t_{on}}{t_{off}} \left(\frac{n_2}{n_1}\right)}{1 + \frac{R_{int}}{R}} \quad ; \qquad R \leqq R_{crit} \text{ and results in trapezoidal current waveshapes} \tag{16}$$

For values of R equal to or greater than R_{crit}, the output voltage increases proportional to the $\sqrt{R}$

$$E_{out} = \frac{\frac{E_{in} t_{on}}{t_{off}} \frac{n_2}{n_1}}{1 + \frac{R_{int}}{R_{crit}}} \sqrt{\frac{R}{R_{crit}}} \quad ; \quad R \geq R_{crit} \text{ and results in triangular current waveshapes} \qquad (17)$$

Figure 2-16 shows the theoretical (lossless) and the actual output characteristic of a two-stage (push-pull) IET circuit as a function of the load resistor. Input voltage, on-time, off-time, turns ratio, and inductance are constant.

2.3 THE INDUCTIVE ENERGY TRANSFER CIRCUIT APPROACH

2.3.1 THE BLOCK DIAGRAM

The block diagram, figure 2-19, shows the complete circuit configuration of the 8-stage, 45 degree staggered breadboard unit. The original 2-stage, 180 degree staggered unit was built along the same approach and consisted of a pre-regulator stage, a control circuit, and two push-pull stages. In the 8-stage version, this approach is repeated four times and thus consists of four push-pull stages which are staggered 45 degrees.

The pre-regulator was in all cases either a regulated power supply or a simple emitter-follower.

The control circuit employed used the well-known prirciple of superimposing a variable dc voltage on a triangular waveshape. The width of the triangular waveshape "peaking" above the dc voltage gives the desired pulsewidth. The superimposed dc voltage is controlled by an error amplifier which compares a portion of the output voltage with a fixed reference. The error amplifier thus governs the superimposed dc voltage and hence the required pulsewidth.

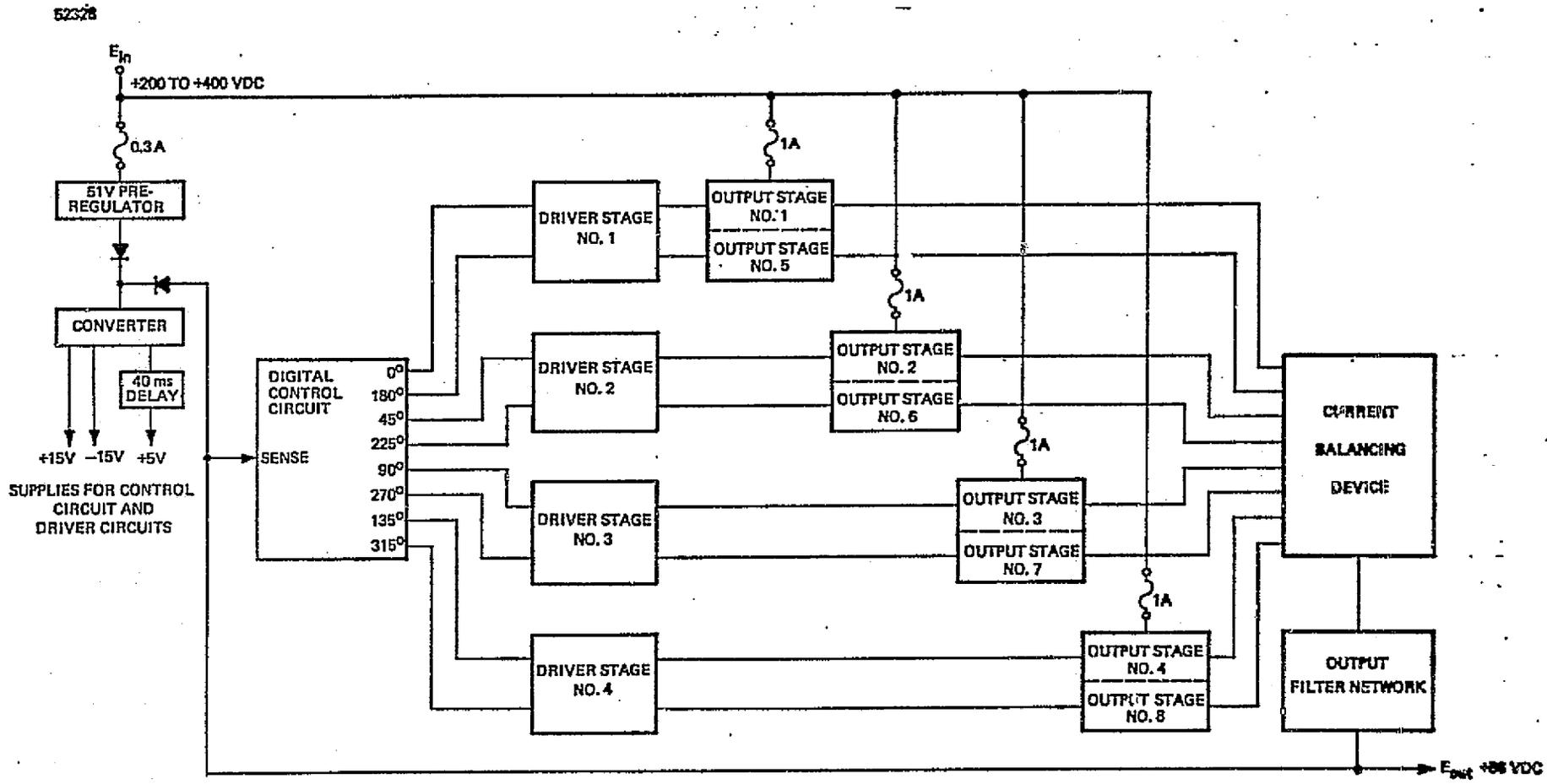


Figure 2-19. Inductive Energy Transfer Circuit Block Diagram

This principle is also employed in the digital control circuit, the only difference being that the triangular waveshape is a digital version of the analog triangular waveshape. A more detailed description is found under paragraph 2.3.2.

All power stages use the same configuration except that their control pulses are staggered according to the number of stages employed. A more detailed description is given in paragraph 2.3.3.

During the investigation, it was found that the power stages have a tendency to share the power unequally. To overcome this problem, a current balancing circuit was required and is described later.

2.3.2 CONTROL CIRCUIT

2.3.2.1 Control Circuit History

An analog control circuit approach was considered but due to circuit component variation over the temperature range, a 30 percent variation in pulsewidths could occur for an 8 stage IET circuit. Therefore, this approach was abandoned and it was decided to use a digital approach.

2.3.2.2 Control Circuit Components and Functions (See figure 2-20.)

1. (Z3) 2.56 MHZ clock.
2. (Z1 and Z2) 8-bit divide by 256 counter.
3. Four 8-bit up-down counters staggered 45 degree.
    a) (Z9 and Z10) staggered 0 degree.
    b) (Z16 and Z21) staggered 45 degrees.
    c) (Z23 and Z26) staggered 90 degrees.
    d) (Z29 and Z31) staggered 135 degrees.
4. Four 8-bit NAND gates used to reset the 45 degree staggered up-down counters.

a) (Z8) resets the 0 degree staggered up-down counter.

b) (Z28) resets the 45 degree staggered up-down counter.

c) (25) resets the 90 degree staggered up-down counter.

d) (Z18) resets the 135 degree staggered up-down counter.

5. Z2 signals 8, $\overline{8}$ controls and 0 degree staggered up-down counter.

6. Z37 dual flip-flop 8', $\overline{8}$' signals control the 45 degree staggered up-down counter.

7. Z2 signals 7, 8, $\overline{7}$, and $\overline{8}$ which are controlled by (Z12 and Z15) which control the 90 degree staggered up-down counter.

8. Z37 dual flip-flop signals 7', 8', $\overline{7}$' and $\overline{8}$' which are controlled by (Z38 and Z12) which control the 135 degrees staggered up-down counter.

9. Four 8-bit digital comparators which produce an output pulse when their corresponding up-down counter digital number is greater than the analog-to-digital control number.

   a) (Z33 and Z34) controlled by the 0 degree staggered up-down counter and produces an output pulse at 0 degree.

   b) (Z17 and Z22) controlled by the 45 degree staggered up-down counter and produces an output pulse at 45 degrees.

   c) (Z24 and Z37) controlled by the 90 degree staggered up-down counter and produces an output pulse at 90 degrees.

   d) (Z30 and Z32) controlled by the 135 degree staggered up-down counter and produces and output pulse at 135 degrees.

10. Four 8-bit digital comparators which produce an output pulse when the corresponding up-down counter digital number is smaller than the analog-to-digital control number.

    a) (Z40 and Z41) controlled by the 0 degree staggered up-down counter and produces ar output pulse at 180 degrees.

    b) (42 and Z43) controlled by the 45 degree staggered up-down counter and produces an output pulse at 225 deegrees.

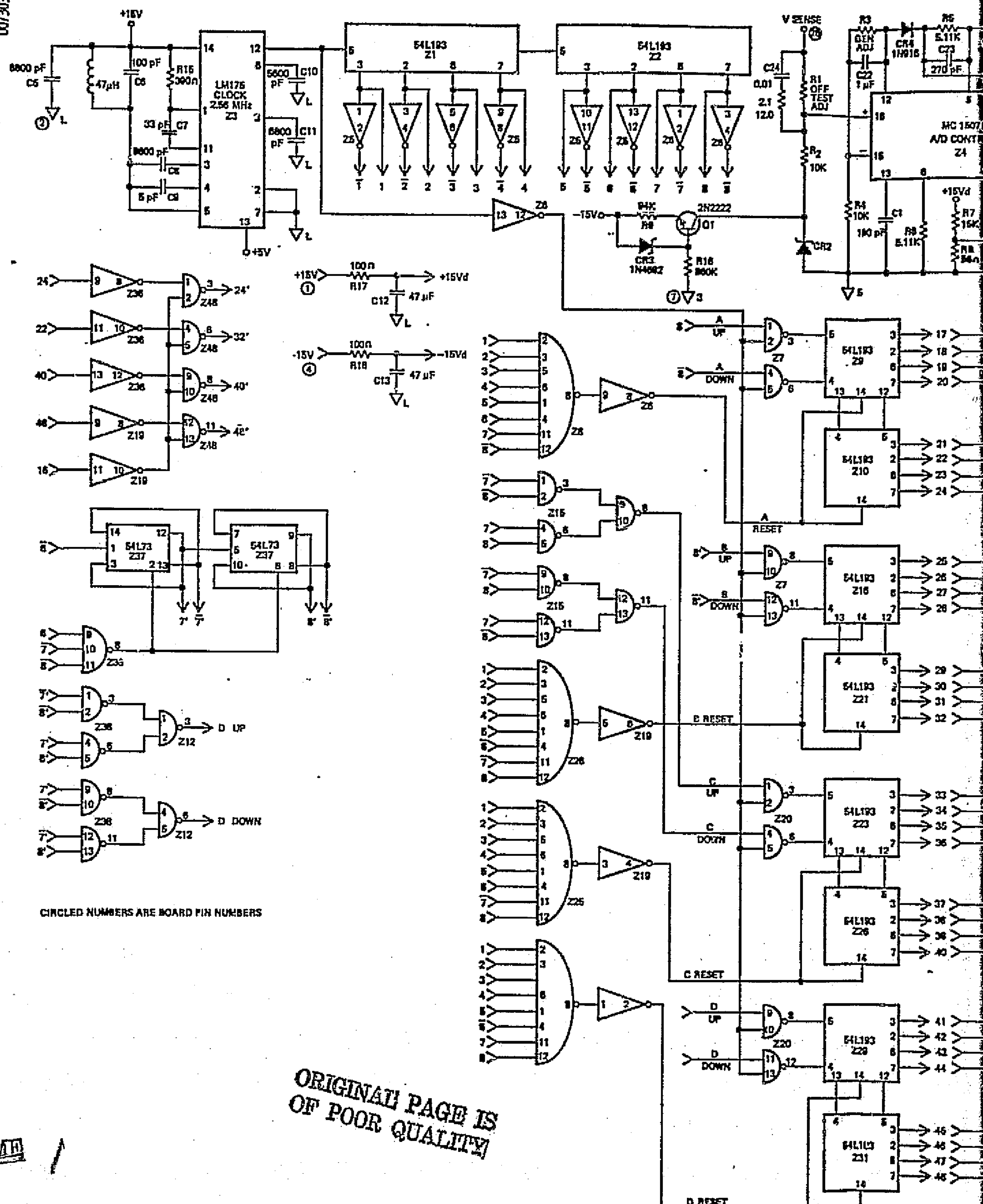
    c) (Z44 and Z45) controlled by the 90 degree staggered up-down counter and produces an output pulse at 270 degrees.

    d) (Z46 and Z47) controlled by the 135 staggered up-down counter and produces an output pulse at 315 degrees.

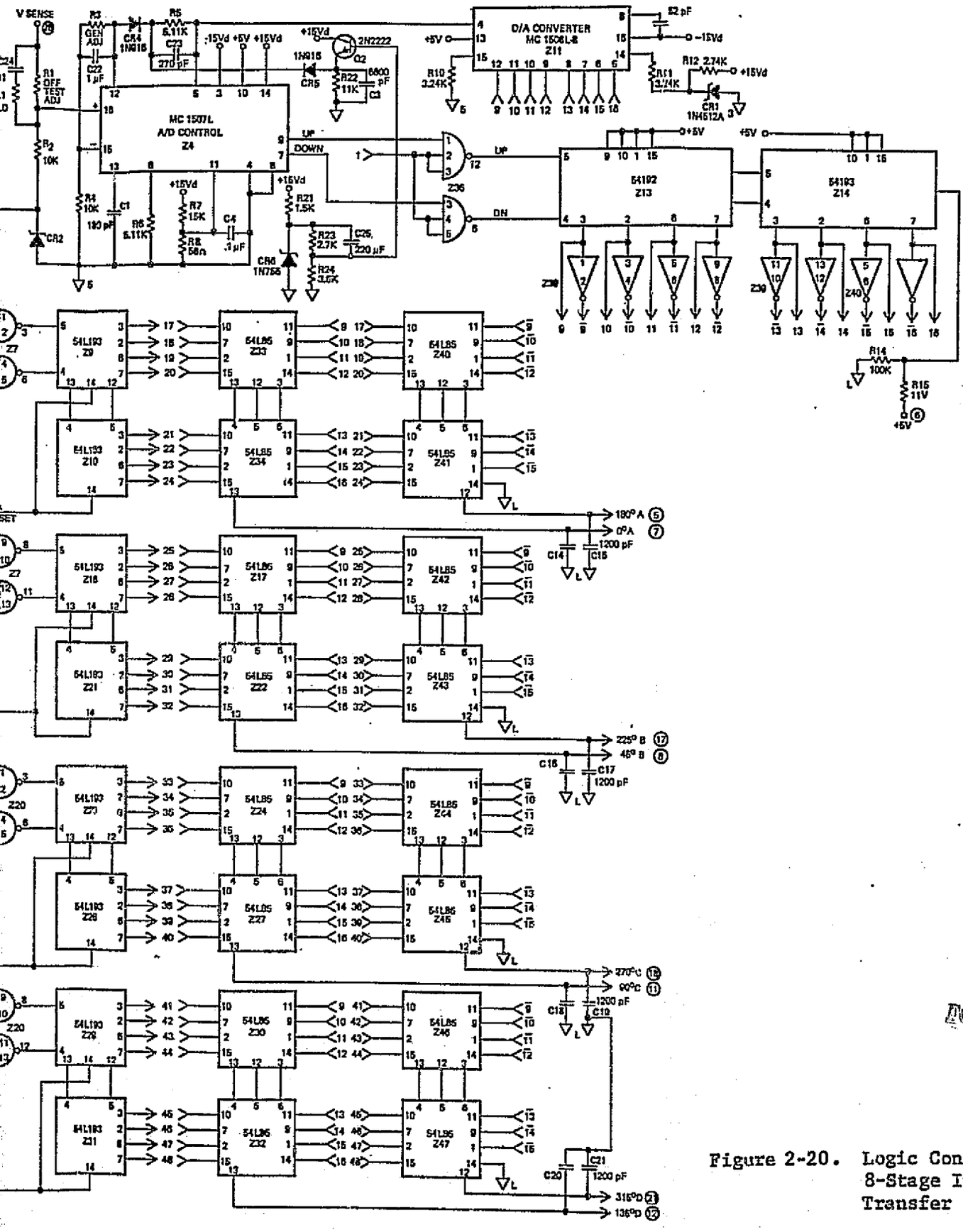
11. (Z4) A/D control, (Z11) D/A converter (Z35) triple three input NAND gate, and (Z13 and Z14) 8-bit up-down counter make up the analog-to-digital converter.

R62329

007303



CIRCLED NUMBERS ARE BOARD PIN NUMBERS



FOLDOUT FRAME 2

Figure 2-20. Logic Control Circuit for 8-Stage Inductive Energy Transfer System

12. Reference diodes

a) CR1 6.4V zener diode is the reference diode for Z11 D to A converter.

b) CR2 6.4V zener diode is the input amplifier offset reference diode.

c) CR3 6.4V zener diode is a constant current network for CR2.

d. CR6 7.5V zener diode is the reference diode for the 180 degree clamp circuit.

2.3.2.3 Operation of the Control Circuit

The heart of the control circuit consists of four up-down counters, eight digital comparators, and an analog-to-digital converter (see figure 2-20). The four up-down counters are controlled to reset, count up to 128, and then count back to 0. It takes 50 μsec (with a 2.56 MHz clock) to count up from 0 to 128 and 50 μsec to count down from 128 to 0. This is considered one cycle, or 360 degrees. The four up-down counters are displaced in time by 45 degrees (or 12.5 μsec).

Each up-down counter output digital number is fed into two digital comparators. The first digital comparator sets a digital number level which is proportional to the analog voltage feed into the digital-to-analog converter. If the up-down counters digital number is greater than the analog-to-digital converter digital number, a high power level is produced. This high output level remains until the up-down counter digital number falls to a magnitude which is less than the analog-to-digital converter digital number (see figure 2-21).

The second digital comparator sets the complement of the digital number level which is proportional to the analog voltage feed into the analog-to-digital converter. If the up-down counter digital number is smaller than the analog-to-digital converter digital number, a high output level is produced. This high output level remains until the up-down counter digital number rises to a magnitude which is greater than the analog-to-digital converter digital number. (See figure 2-22.)

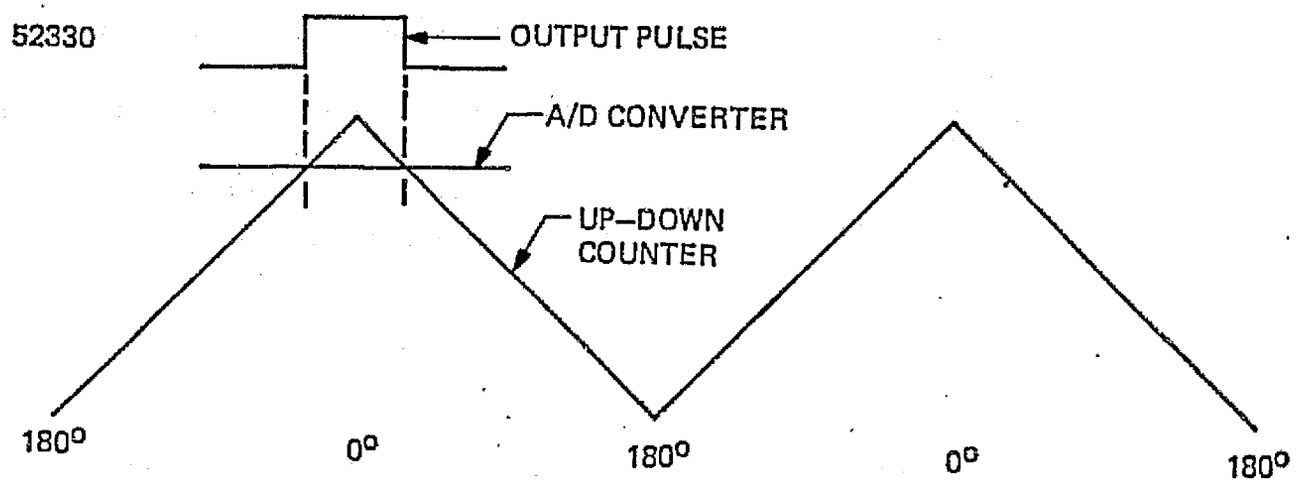


Figure 2-21. Output Pulsewidth Generation from the First Comparator

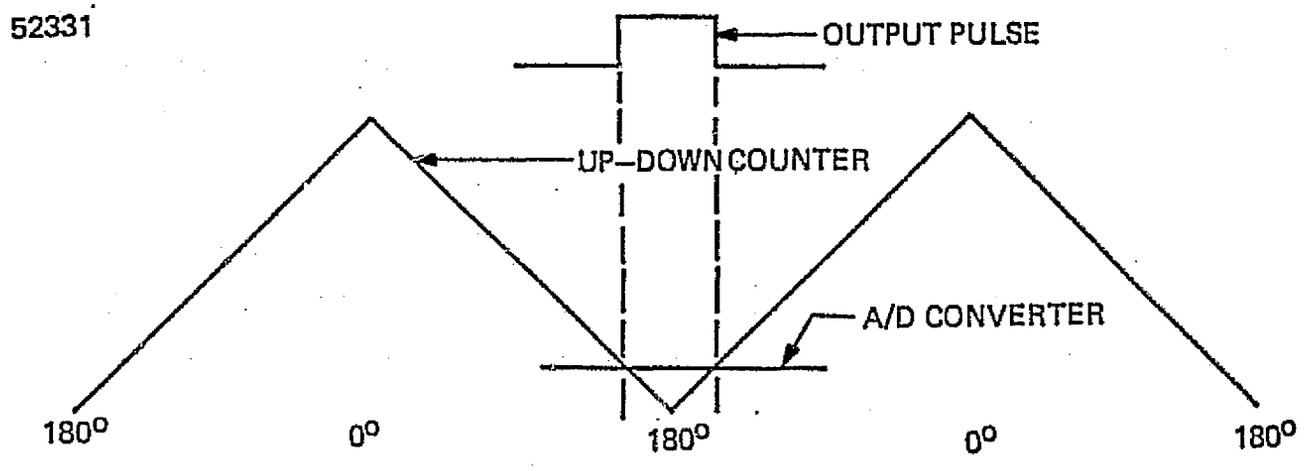


Figure 2-22. Output Pulsewidth Generation from the Second Comparator

The 0 degree up-down counter with its first comparator will produce an output pulse whose width is proportional to the analog input voltage and will by symmetrically centered around the 0 degree part of the cycle. The 0 degree up-down counter with its second comparator will produce an output pulse whose width is proportional to the analog input voltage and will be symmetrically centered around the 180 degree part of the cycle. The other three-up-down counters with their comparators will produce the following similar output pulses.

REV

1. 45 degree up-down counter and its first comparator will produce an output pulse at 45 degrees.
2. 45 degree up-down counter and its second comparator will produce an output pulse at 225 degrees.
3. 90 degree up-down counter and its first comparator will produce an output pulse at 90 degrees.
4. 90 degree up-down counter and its second counter and its second comparator will produce an output pulse at 270 degrees.
5. 135 degree up-down counter and its first comparator will produce an output pulse at 135 degrees.
6. 135 degree up-down counter and its second comparator will produce an output pulse at 315 degrees.

The analog-to-digital converter consists of an A/D control circuit, an 8-bit counter, a D/A converter, and a three input NAND gate. (See figure 2-23.)

52332

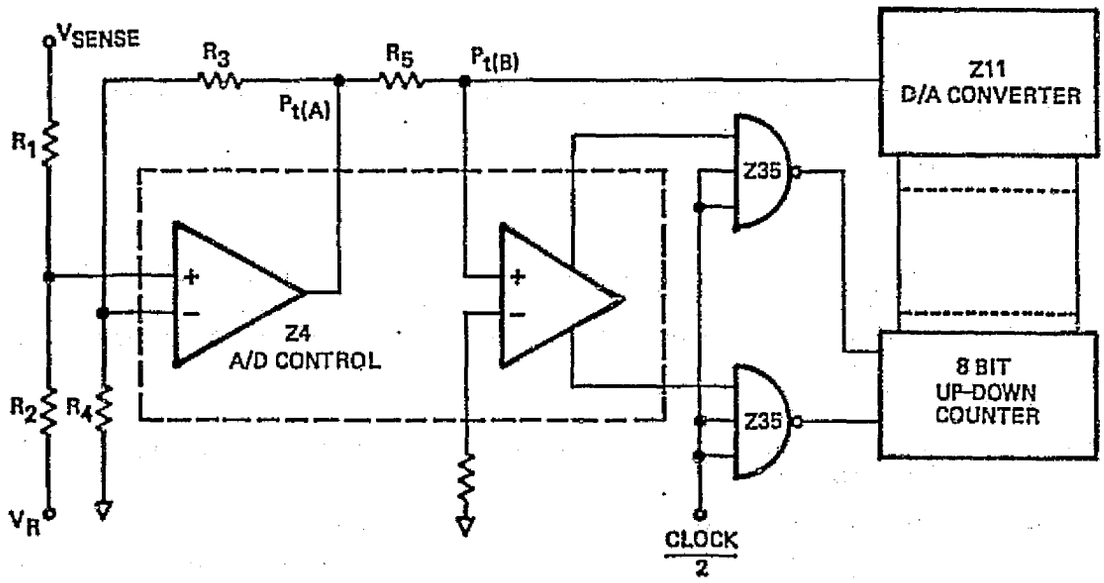


Figure 2-23. Analog-to-Digital Converter

Resistors R1, R2, R3, R4, and R5 set the gain of the analog-to-digital converter and also the voltage level of V sense. The circuit converts an analog voltage to a digital number as follows: Assume initially that

there is a voltage V at point (A) and the 8-bit counter is at 00000000, therefore there is no current being sunk by Z11 and no voltage drop across R5. The voltage at point (B) is therefore V. The comparator will make the up line high and the down line low. A clock will get through on the up line and cause the 8-bit counter to increase to 00000001.

This will produce a small current flow through R5 (7.8 μA) and cause a small voltage drop across R5 (39 mV). If voltage V is greater than this voltage drop, the comparator will hold the up line high and the down line low and allow a second clock to get through on the up line. This will cause the 8-bit counter to increase to 00000010 and produce a larger current flow through R5. This process will continue until the voltage drop across R5 equals the voltage V at point (A) and the 8-bit up-down counter will contain a digital number which will be proportional to the voltage V at point (A).

2.3.2.4 Advantages and Disadvantages of the Control Circuit

2.3.2.4.1 Advantages

1. All 8 output pulsewidth magnitude information comes from a common source (analog-to-digital converter) and since the pulsewidth magnitude is produced digitally, all 8 output pulsewidths are nearly identical within ±100 nsec.
2. All 8 output pulses are displaced nearly 45 degrees or 12.5μsec within ±100 nsec. This is easy to accomplish with the divide by 256 counter.
3. Phase shift is not a function of input voltage because the output pulses are always symmetric around their staggered point regardless of pulsewidth.
4. A change in clock frequency will not affect the IET circuit because the control circuit output pulsewidth to cycle period ratio is a constant.
5. An automatic turn-on circuit causes the output pulsewidth to start at 0 pulsewidth and slowly build up to 180 degree or to the desired pulsewidth over approximately a 1 second period.
6. Simplicity for adding more staggered stages.

2.3.2.4.2 Disadvantages

The disadvantages of the control circuit are:

1. Circuit complexity
2. Insufficient resolution

2.3.3 THE POWER AND DRIVER STAGES

The schematic, figure 2-24, shows two 180 degree staggered IET stages, their associated driver circuit and the output filter section. A single stage description is presented since all stages are identical.

Inductor-transformer T2-1 is built around a Super-Perm 49 Twin C-Core and carries two primary and one secondary windings. A Twin C-Core was selected because it allows the selection of the proper power handling capability (Window Area times Cross Section) and simultaneous selection of the proper ratio of Window Area over Cross Section. This selectivity in combination with the selection of the core material allows optimizing for low core losses, good coupling, low winding capacitance, low fringing flux and a high winding factor.

The secondary winding feeds power through the diode CR9-1, the current-balancing network, consisting of L1A/L1J, and the parallel combination of L2 and C9 into the output filter capacitors C10-C12 and the load. Diode CR9-1 allow operation of the secondary of the inductor-transformers only during the off-time of the primary switching transistors. This provides operation such that the input conditions are not directly reflected into the output.

The primary winding is split into two sections which are connected in series through Q1-1, one of the two switching transistors. In this winding configuration, the two halves of the primary winding serve as voltage

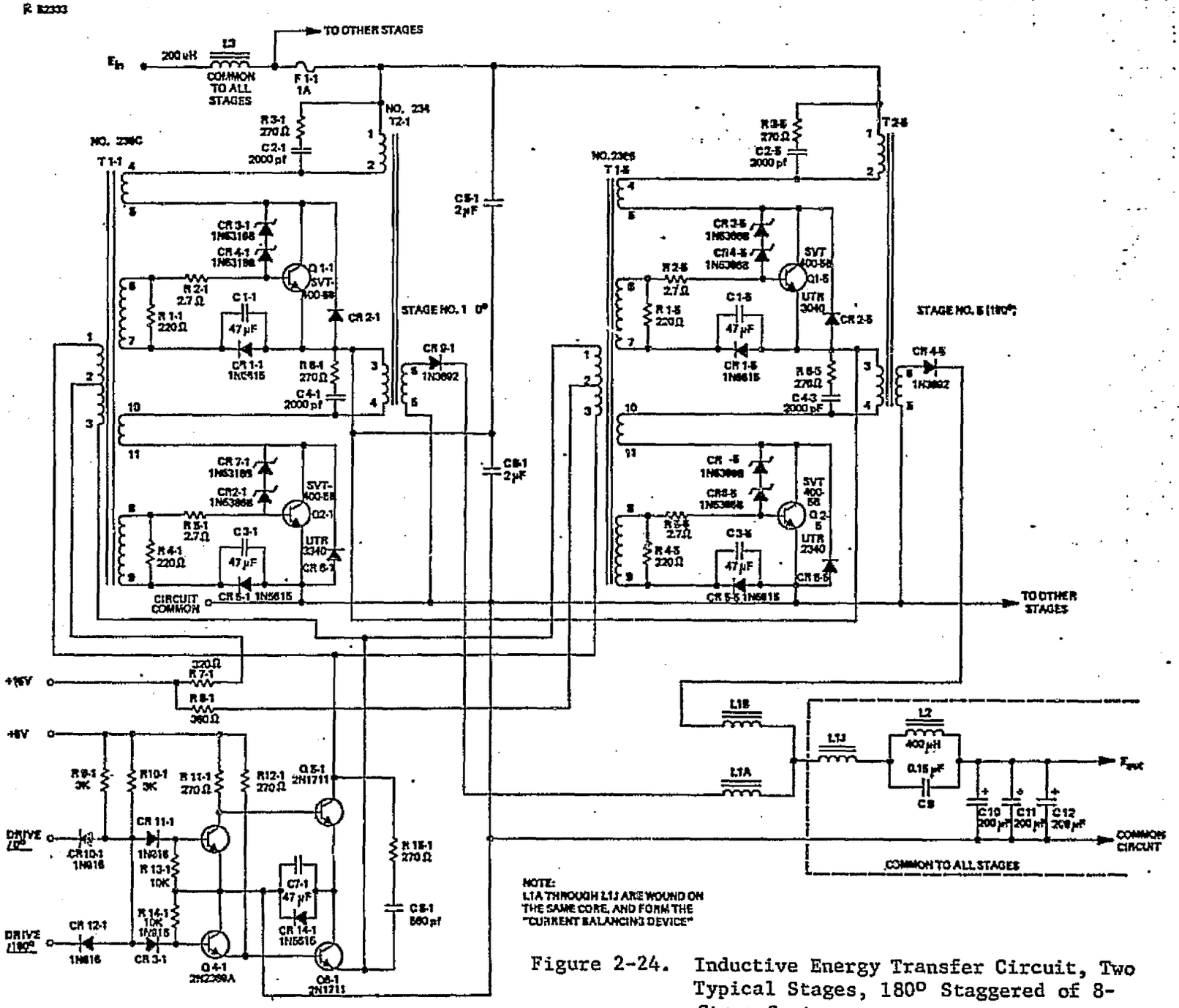


Figure 2-24. Inductive Energy Transfer Circuit, Two Typical Stages, 180° Staggered of 8-Stage System

dividers for the two switching transistors Q1-1 and Q2-1 and the two series connected input filter capacitors C5-1 and C6-1 which are common to two stages. The transistors used in this application are high speed, triple diffused planar transistors SVT400-5B and SVT400-3B which are packaged in a T061 package with an isolated collector. The voltage breakdown rating of both transistors is $V_{ceo_{sus}}$ = 400 volt. Their peak collector current rating is 10 ampere and 6 ampere respectively. During the study it became apparent that the SVT400-5B exhibited an exceptional high failure rate (44 out of 50). The lower rated SVT400-3B under identical conditions showed the opposite characteristic. The reasons for this unexpected behavior are under investigation by the manufacturer of the transistors.

In all stages, each switching transistor is protected against reverse voltage by a diode across the emitter-collector and against excessive voltage by a zener diode between collector and base. Further, all primary windings are paralleled with an R-C despiking network. During the dwell-time of the switching transistors, a parallel diode and capacitor in the base lead provides an off-bias voltage.

The driver stages use a current transformer (T1-1) with regenerative feedback. The feedback turns-ratio is 1 to 5 and assures a sufficient basedrive current proportional to the collector current.

The primary windings of two base drive transformers of two 180 degree staggered stages are always parallel connected with reverse polarity. In this connection, their primary sides can be controlled by one driver stage. In the absence of a control signal, both primaries of these current transformers are "short-circuited" by transistors Q5-1 and Q6-1 (both are conducting), which prevent them from generating any drive signal during the dwell time of the control signal from the logic circuit.

The output of the power stages is channeled through the output diode into a current balancing system which consists of a multifilar wound inductor connected in series with a parallel L-C circuit. Output filtering is accomplished by output capacitors (C10 through C12).

2.4 TECHNICAL ACCOMPLISHMENTS

2.4.1 COMPARISON OF THE TWO APPROACHES: SERIES INVERTER VERSUS INDUCTIVE ENERGY TRANSFER

At the beginning of the investigation, two circuit approaches were investigated. These two conversion circuits were the:

a. Series Inverter
b. Inductive Energy Transfer

Both circuits were designed for a power capability of 100 to 500 watts over an input voltage range of 200 to 400 volts dc and an output voltage of 56 volts dc.

The series inverter showed promising performance results but implementation of pulsewidth-modulation for regulation purposes was severely limited through the nonavailability of transistor switches capable of carrying the high current spikes required to equalize the capacitor voltages. This approach was therefore abandoned in favor of the inductive energy transfer approach.

For information purposes, a general comparison of one series inverter stage with a 2-stage inductive energy transfer supply is presented in table 2-2. The following tabulation is based on computer calculations and circuit component evaluations.

TABLE 2-2

COMPARISON OF THE TWO APPROACHES

Characteristic	Series Inverter	Inductive Energy Transfer, 2 Stage
Input L-C filter section	Required,	Required, smaller
Input ripple current, A_{rms}	1.37	1.19
Output ripple current, A_{rms}	4.71	2.4
Power stage	Fewer components	More components, 2 stages
Inherent no-load losses	No winding capacitance losses. Always high resonant current copper losses, full ac flux swing	Winding capacitor losses. Currents increase with load. Small ac-flux swing
Output filter	L-C larger; i_{ripple} larger	C filter only; i_{ripple} smaller
Frequency limitations	Limited by tank capacitor and core losses. B_{ac} large	Favorable as B_{ac} small and B_{dc} large
Weight at equal flux density	Lighter	Heavier
Weight at higher flux density	Heavier since no B increase is allowed	Lighter
Ripple current decrease possibilities	3 or multiphase	Staggered, smaller stages
Control circuit	About equal	
Ease of modular extension	Possible	Easier
Limiting characteristic	No present-day transistor can carry balancing current spikes	None inherent

2.4.2 THE TWO STAGE INDUCTIVE ENERGY TRANSFER APPROACH

The detailed circuit configuration of the 2 stage (push-pull) IET circuit is depicted in the following illustrations:

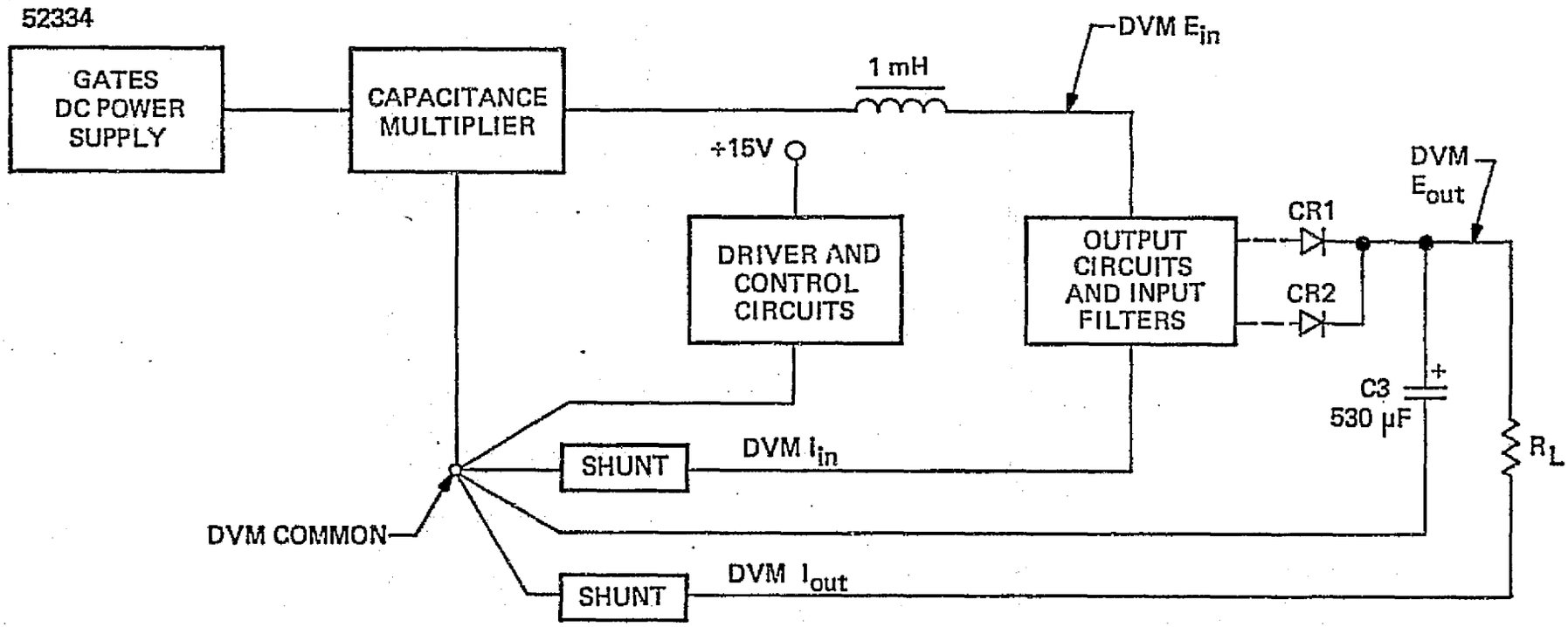
a. Figure 2-25, Block Diagram
b. Figure 2-26, IET System, 2 Output Stages
c. Figure 2-27, Driver Circuit for 2 Stages
d. Figure 2-28, Control Circuit for 2 Stages

The block diagram, figure 2-25, shows that the input power supply required a capacitance multiplier to make it a useful source in spite of its high output ripple voltage. It further shows that in order to assure correct test results a common "star" ground was established to which all metering was directly connected. This technique was adhered to in all circuit configurations. The block diagram also shows the driver and control circuit, the output stages with input filters, the two output diodes and the output filter. Power to the control circuit was delivered from a regulated +15 volts dc power supply.

Figure 2-26 shows the two output power stages with all associated components and the connection to the self-regenerative driver circuit.

The driver circuit is shown in detail in figure 2-27. Two current transformers T1 and T2 are controlled from one driver circuit and provide operation of two 180 degree staggered power stages in a "push-pull" arrangement.

The control circuit is shown in figure 2-28. This circuit generates a linear unijunction controlled ramp voltag which is amplified and fed into terminal 2 of the comparator LM111H where it is compared with a dc voltage fed into terminal 3. The dc level is generated by a differential



DVM: HP 2402A

Figure 2-25. Two Stage Inductive Energy Transfer Circuit Basic Test Set-up Block Diagram

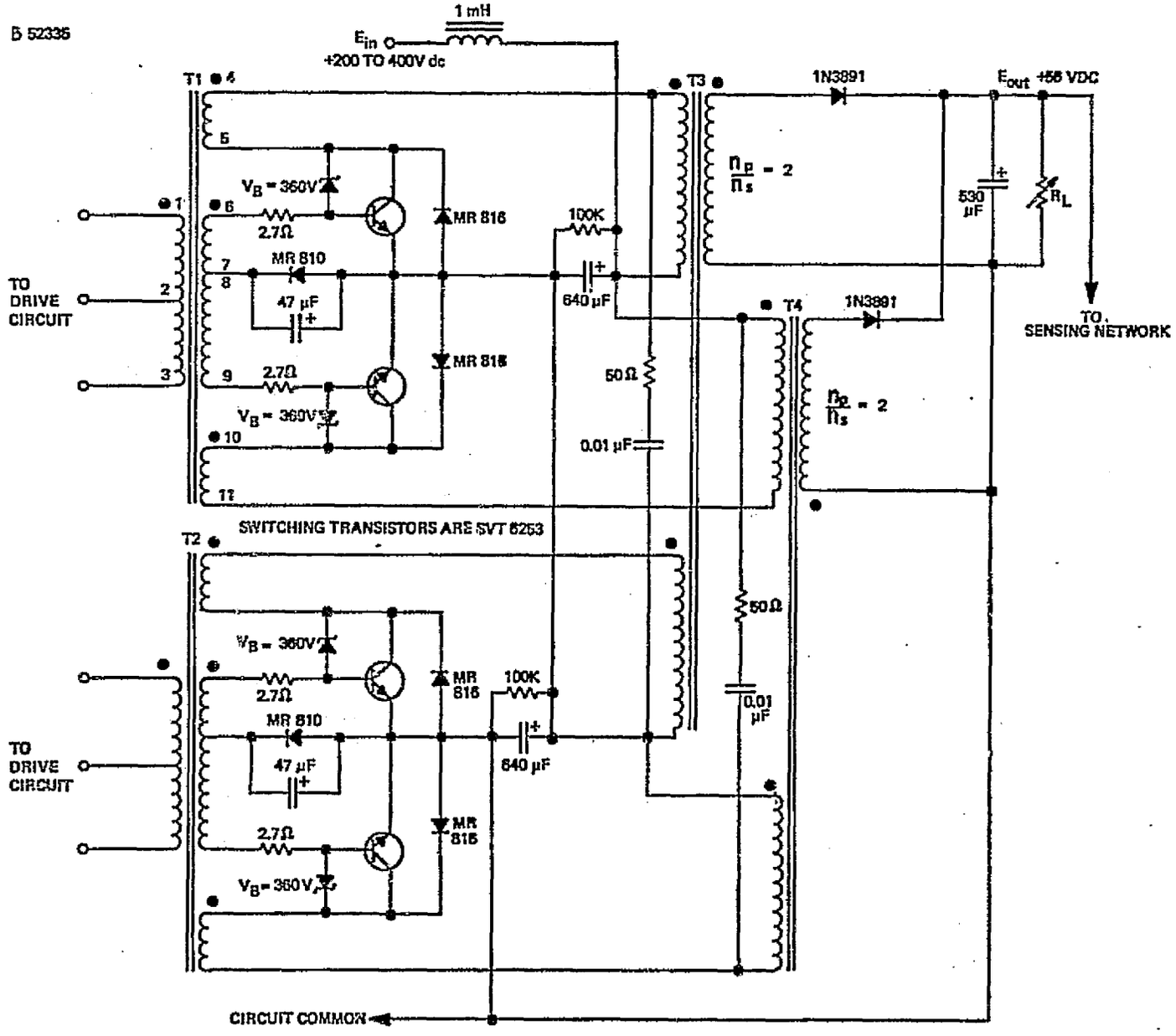


Figure 2-26. Two Stage Inductive Energy Transfer System Output Stages

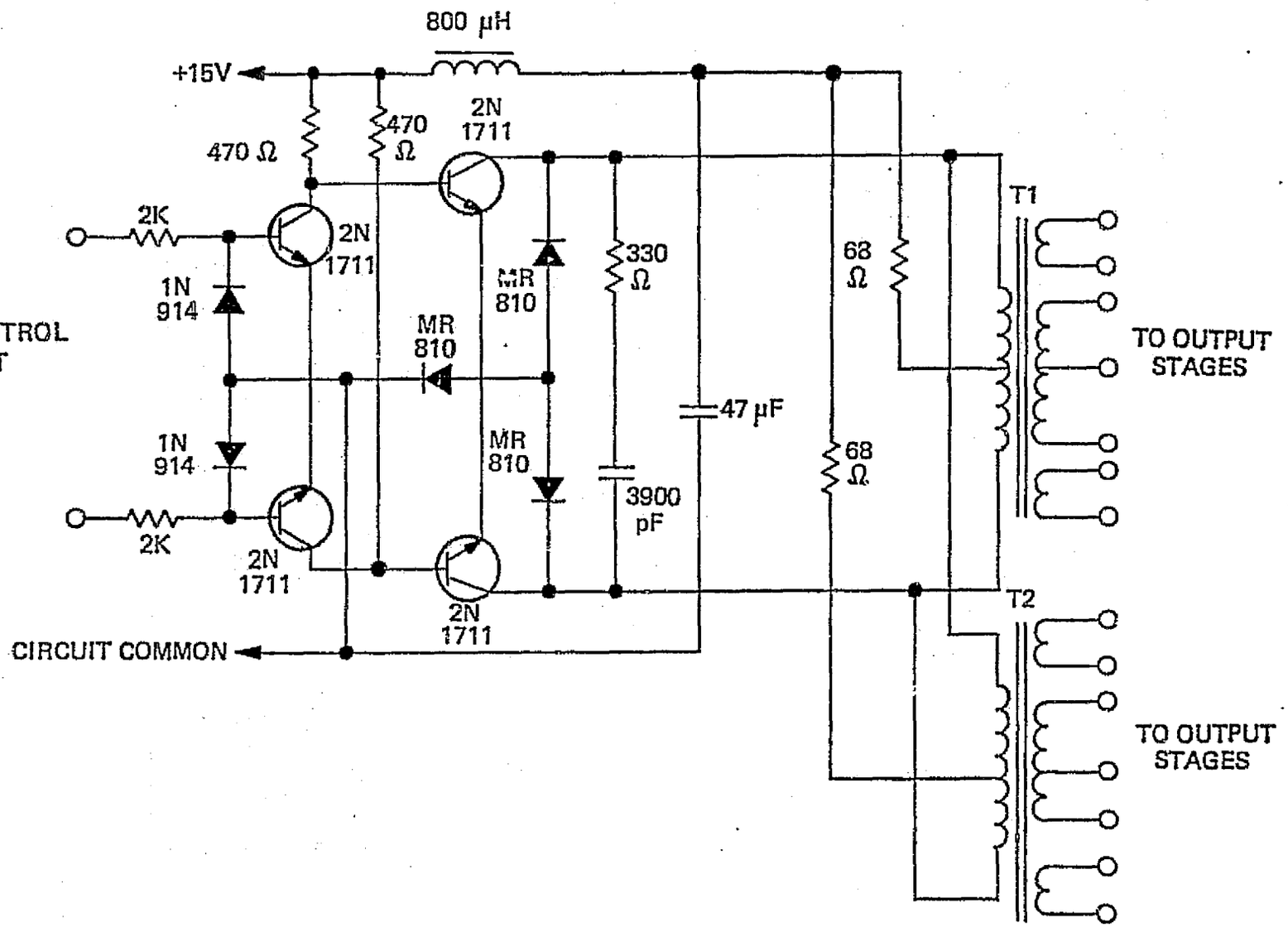


Figure 2-27. Inductive Energy Transfer System Driver Circuit

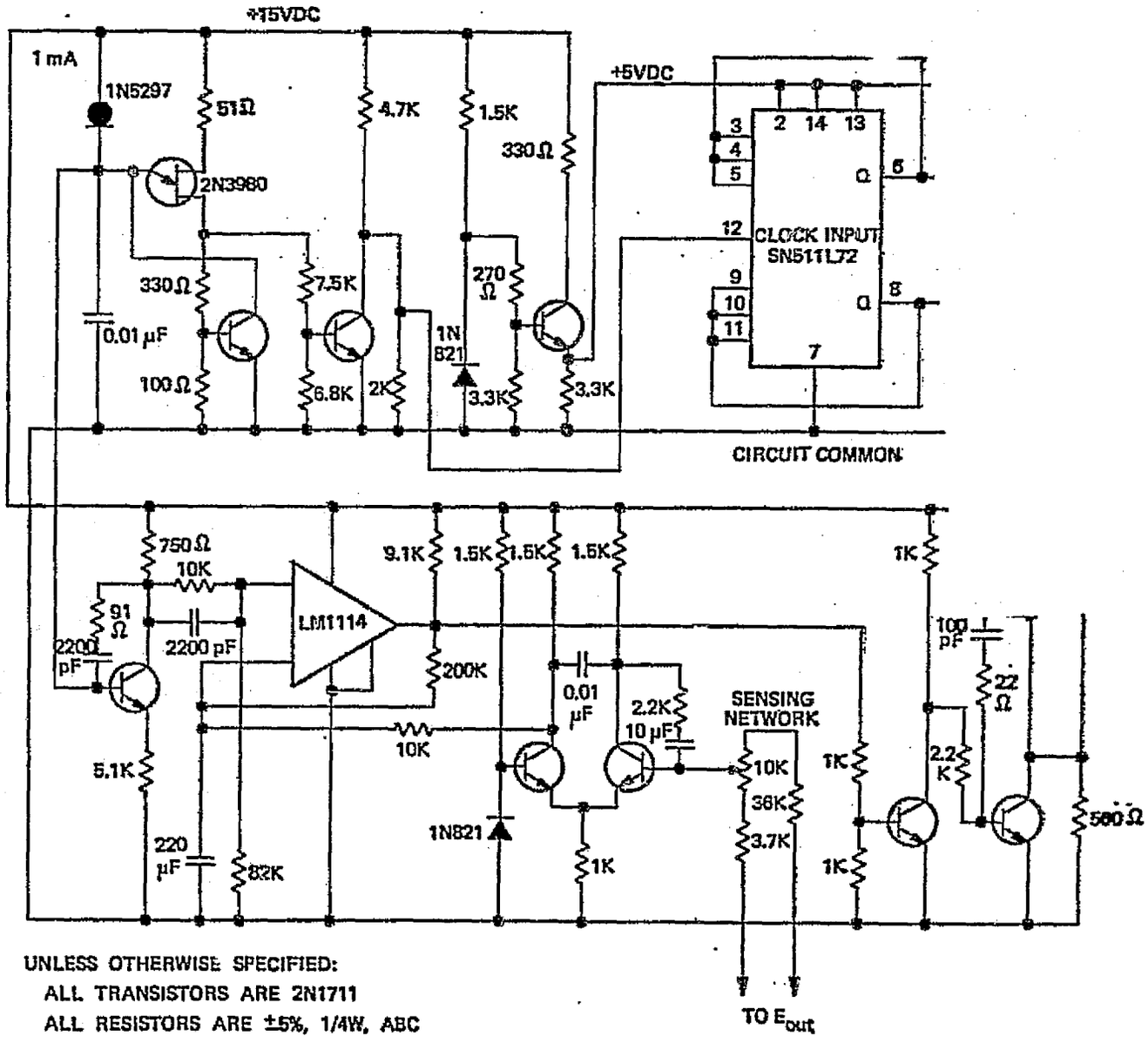


Figure 2-28. Inductive Energy Transfer System Control Circuit

amplifier which compares a portion of the output voltage of the power stages with a zener diode voltage and generates an error signal. This produces a pulsewidth-modulated output at terminal 7 of the comparator LM111H. These pulses are buffered, inverted and channeled through two "AND" gates into the drive circuit. The "AND" gates are synchronously controlled by the JK Flip-Flop.

2.4.3 THE PERFORMANCE CHARACTERISTICS OF THE 2 STAGE IET APPROACH

Table 2-3 and figure 2-29 show the measured performance data of the 2 stage IET circuit. Performance measurements were made for an input voltage range from 200 to 400 volt dc, for an output power range of about 100 to 500 watts and a regulated output voltage of 56 volts dc.

The efficiency was 90 ± 1.5 percent over the input voltage and output power range.

Since the overall circuit was not optimized and included the control losses, there is no doubt that the two stage approach would exhibit an overall efficiency better than 90 percent if optimized.

A relatively high ripple voltage at the input and output required the use of commercially available electrolytic capacitors and thus did not meet the specified requirements to use flight approvable components. Because large value 29F tantalum capacitors have delivery times in excess of a year and because add-on modular construction is desired, it was decided to pursue the 4 and 8 stage approaches, since these are capable of reducing the ripple current and providing modularity.

2.4.4 THE DIGITAL CONTROL CIRCUIT

Based on the decision to pursue a 4 and an 8 stage staggered unit, a decision had to be made as to whether or not an analog control circuit

TABLE 2-3

PERFORMANCE DATA OF THE 2-STAGE IET CIRCUIT

	R_L (Approx)	E_{in} (V dc)	I_{in} (A dc)	E_{out} (V dc)	I_{out} (A dc)	Input Ripple (mV rms)	Output Ripple (mV rms)	P_{in} (W)	P_{out} (W)	Efficiency (%)
R_{crit}	28 Ω	199.96	0.6323	56.119	2.050	205	115	126.44	115.04	90.99
	24.5 Ω	200.05	0.7274	56.084	2.364	220	122	145.52	132.58	91.11
	21.4 Ω	200.09	0.8715	56.074	2.838	235	132	174.38	159.14	91.26
	18.4 Ω	200.00	0.9575	56.066	3.128	265	138	191.90	175.37	91.39
$E_{in} \cong$	15.3 Ω	200.24	1.082	56.048	3.532	280	145	216.66	197.96	91.37
200V dc	12.2 Ω	200.07	1.415	56.007	4.613	325	157	283.10	258.36	91.26
	10.7 Ω	200.30	1.616	55.990	5.274	350	172	323.69	295.29	91.23
	9.2 Ω	200.31	1.879	55.961	6.119	380	175	376.38	342.43	90.98
	8.4 Ω	200.05	2.057	55.956	6.676	400	177	411.50	373.56	90.78
	7.7 Ω	200.25	2.287	55.922	7.368	420	180	457.97	412.03	89.97
	6.9 Ω	200.11	2.551	55.897	8.160	445	185	510.48	456.12	89.35
	6.2 Ω	200.05	2.861	55.864	9.070	470	182	572.34	506.69	88.53
R_{crit}	20Ω	300.01	0.5838	56.142	2.825	260	205	175.15	158.60	90.55
	18.4 Ω	299.91	0.6426	56.125	3.125	245	212	192.72	175.39	91.01
	15.3 Ω	300.05	0.7286	56.115	3.548	260	212	213.62	199.10	91.07
$E_{in} \cong$	12.2 Ω	300.03	0.9476	56.079	4.614	310	228	284.31	258.75	91.01
300V dc	10.7 Ω	300.15	1.081	56.056	5.261	325	218	324.46	294.91	90.89
	9.2 Ω	300.15	1.255	56.028	6.104	360	205	376.67	342.00	90.79
	8.4 Ω	300.00	1.370	56.018	6.662	375	198	411.00	373.20	90.80
	7.7 Ω	300.08	1.521	55.992	7.382	395	188	456.42	413.33	90.56
	6.9 Ω	300.05	1.694	55.963	8.175	420	188	508.29	457.50	90.00
	6.2 Ω	299.94	1.896	55.933	9.086	450	190	568.69	508.21	87.37
R_{crit}	15.3 Ω	399.96	0.5544	56.157	3.543	255	285	221.74	198.96	89.73
	12.2 Ω	399.95	0.7159	56.115	4.618	290	300	286.32	259.14	90.51
$E_{in} \cong$	10.7 Ω	400.28	0.8154	56.104	5.261	320	255	326.31	295.16	90.43
400V dc	9.2 Ω	400.21	0.9488	56.067	6.097	345	222	379.72	341.84	90.02
	8.4 Ω	400.09	1.033	56.064	6.646	360	205	413.29	372.60	90.16
	7.7 Ω	400.12	1.148	56.033	7.380	375	180	459.34	413.52	90.03
	6.9 Ω	400.33	1.274	56.003	8.175	400	175	510.02	457.83	89.77
	6.2 Ω	400.14	1.424	55.978	9.097	425	180	569.80	509.23	89.37

14 Dec 1973

IET Circuit

Closed loop with modified control circuit (Gated Drive)

Two inductor/transformers and four switching transistors SVT 6253

Input power does not include driver and control circuit power

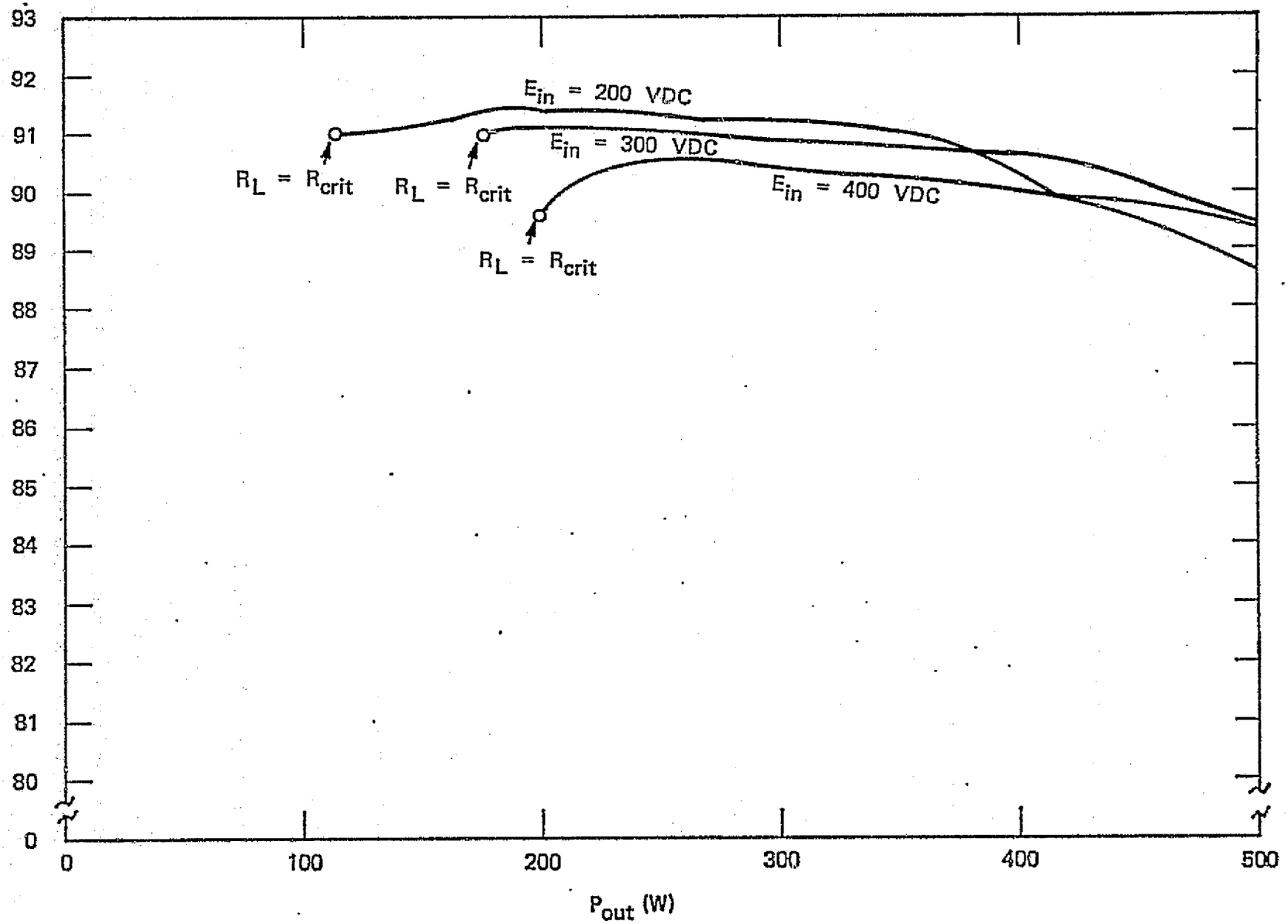


Figure 2-29. 2-Stage Inductive Energy Transfer Circuit Efficiency versus P_{out}

would be capable of delivering not only equal pulses but also equally spaced pulses over a temperature range of -20°C to +75°C. An 8 [illegible] 45 degree staggered unit would at least require four ramp gener. each of which would control two 180 degree staggered stages.

A previously developed IC-chip operated in a nearly identical ma as the control circuit used in the two stage IET unit. However, investigation of the effect of temperature changes on this circuit showed that the analog approach could not meet the requirements for a multistage time staggered unit (reference Appendix B). Therefore, the digital control circuit described in paragraph 2.2.3 was chosen because it precisely provided pulses of equal length and equal spacing.

The digital control circuit is best suited for precise multistage staggered control pulses because of its inherent insensitivity to temperature and its ease of stabilization. Currently the digital circuit lacks adequate resolution because of frequency limitations of components. A clock frequency and logic circuits capable of proper operation at ten times the speed of the present circuit would increase the resolution by a factor of 10. Commercial application components are approaching this speed. However, they have not been qualified for space flight hardware.

The analog sections of the control circuit are straightforward, but they are important since they influence the transfer characteristic of the control circuit.

2.4.5 THE OUTPUT-CURRENT BALANCING CIRCUIT

The individual inductor-transformer designed for and used in the IET had a minimum inductance such that under minimum load requirements, the current waveshapes remained trapezoidal. The design considerations for this requirement have been discussed in paragraph 2.2.1.

With trapezoidal current waveshapes on both primary and secondary sides of the individual inductor transformers, the individual current pulses can be likened to a "dc-pedestal" with a triangular current waveshape of amplitude ΔI superimposed on it.

The amplitude of ΔI is an ac condition to meet the ac requirement for positive edt to equal negative edt. It is expressed as

$$n_1 \Delta I_1 = n_2 \Delta I_2.$$

However, the dc pedestal is generated by each stage to provide the appropriate output voltage to properly reset the core. This is always the case if each stage operates by itself into its own load. If, however, an output voltage is already present across the load resistor and two stages or more operate in parallel with the same load, then the ac requirement must still be met to maintain proper operation and avoid saturation. But the dc pedestal, which generated the proper output and reset voltage in the single stage case, is no longer required. The output voltage is already present, either across the output filter capacitor or from another stage which is already delivering current to the common load, thus also producing voltage. As a consequence, two stages may well operate with the same ΔI's but one stage may deliver a dc pedestal current while the other stage does not. This results in a rather severe imbalance in output current and power even though the conduction times, the two inductor transformer characteristics, the switching transistor characteristics, and the output diode characteristics are identical in each stage. Unequal on and off times, different saturation voltages of the switching transistors, and different forward voltage drops of the output diodes, play a minor part in the unbalance in output power delivery. The two main reasons for the unbalance are the output filter capacitor and the simultaneous current conduction of the output windings of the inductor transformers into the common load.

It should be noted that the imbalance problem barely exists in two stages of low output power and hence high output impedance.

A circuit was developed which balances the output current for 2, 4, 6, or 8 stages. It consists of an inductor with multifilar windings individually connected to the outputs of the inductor transformers. The other ends of the windings are tied together and are connected in opposing polarity to the output winding on the balancing inductor. Under balanced conditions, all ampere turns on the balancing inductor cancel. Under unbalanced conditions, a corrective edt is generated and prevents full reset of output stages with lower currents. Thus, a dc pedestal current is introduced in the stages with too low output current and their output current is increased. This balancing inductor works well with a resistive load without filter capacitors across it.

The power supply specifications limit allowable output ripple and therefore output capacitors are necessary. To maintain balanced output current delivery, a parallel L-C combination was added between balancing inductor and output filter capacitors.

The combination of the balancing inductor in series with the parallel combination of an L-C circuit yielded balanced power delivery of all stages into the parallel combination of load resistor and output filter capacitor. However, it was observed that in the presence of a parallel combination of load resistor and output filter capacitors, the parallel L-C combination between balancing inductor and output filter capacitor and load resistor was practically sufficient to maintain balanced output current delivery from all stages.

This above new balancing concept has been developed, but more investigation is required to establish all pertinent factors which govern the operation of the balancing inductor and/or the parallel L-C combination in maintaining balanced power delivery from multiple stages.

2.4.6 THE PERFORMANCE OF THE 8-STAGE IET CIRCUIT

The room temperature performance of the 8-stage 45 degree staggered IET system is shown in table 2-4 and figures 2-30 through 2-32.

The tabulated data in table 2-4 shows the steady-state regulation against line and load variation, input and output ripple, and the efficiency at room temperature.

Figure 2-32 depicts the power losses as a function of output power and yields a most interesting insight into the performance of the 8-stage unit, and points out ways for improvement.

Extrapolating the power loss curves to the no-load condition yields the no-load losses of 32, 42 and 52 watts at input voltages of 200, 300, and 400 volts dc respectively.

An inspection of the loss curves yields the information that the no-load losses consist of a fixed loss (12 watts) plus a loss that is proportional to input voltage. The variable losses closely follow a quadratic relation to the output power or current.

A close approximation of all losses can be expressed in the following mathematical equation:

Total losses = (fixed losses) + (variable losses)

$$P_{loss} = \left(12 + \frac{E_{in}}{10}\right) + \left(2.68 \times 10^{-4} \times P_{out}^{2}\right) \qquad (18)$$

TABLE 2-4

ROOM TEMPERATURE PERFORMANCE DATA FOR THE 8-STAGE IET CIRCUIT

	R_L (Approx)	E_{in} (V dc)	I_{in} (A dc)	E_{out} (V dc)	I_{out} (A dc)	Input Ripple (mA p-p)	Output Ripple (mV p-p)	P_{in} (W)	P_{out} (W)	Efficiency (%)	18 July 1974
	41.4 Ω	200.25	0.680	55.97	1.795	150	200	136.17	100.47	73.78	8—Stage IET Circuit
	20.9 Ω	200.21	0.944	55.97	2.657	200	200	189.00	148.71	78.68	
	15.7 Ω	200.30	1.216	55.97	3.530	200	200	243.57	197.57	81.12	Efficiency vs P_{out} and
	12.5 Ω	200.03	1.530	55.97	4.518	250	150	306.05	252.87	82.62	E_{in}
$E_{in} \approx$	10.5 Ω	200.61	1.805	55.96	5.382	250	150	362.10	301.18	83.18	
200V dc	9.0 Ω	200.33	2.119	55.96	6.324	300	200	424.50	353.89	83.37	
	7.8 Ω	200.16	2.378	55.95	7.088	250	300	475.98	396.57	83.32	
	7.0 Ω	200.18	2.714	55.95	8.051	350	300	548.24	450.45	82.91	
	6.3 Ω	200.41	2.998	55.95	8.891	100	350	600.83	497.48	82.79	103
	31.4 Ω	300.25	0.488	56.24	1.804	150	150	146.52	101.46	69.24	
	20.9 Ω	300.00	0.662	56.19	2.665	50	200	198.60	149.75	75.40	
	15.7 Ω	300.70	0.842	56.19	3.542	200	100	253.19	199.03	78.61	
	12.5 Ω	300.54	1.050	56.19	4.534	300	100	315.57	254.77	80.73	
$E_{in} \approx$	10.5 Ω	300.35	1.236	56.19	5.401	300	150	371.23	303.48	81.75	
300V dc	9.0 Ω	300.25	1.440	56.18	6.346	350	150	432.36	356.52	82.46	
	7.8 Ω	300.07	1.609	56.18	7.115	350	150	482.81	399.72	82.79	
	7.0 Ω	300.16	1.831	56.18	8.092	350	200	549.59	454.61	82.72	
	6.3 Ω	300.01	2.020	56.18	8.940	400	200	606.02	502.25	82.88	104
	31.4 Ω	400.02	0.399	56.39	1.814	200	100	159.61	102.29	64.09	
	20.9 Ω	400.02	0.530	56.39	2.679	200	100	212.01	151.07	71.26	
	15.7 Ω	400.49	0.663	56.34	3.552	100	300	265.53	200.12	75.37	
	12.5 Ω	400.05	0.817	56.34	4.545	150	200	326.84	256.07	78.35	
$E_{in} \approx$	10.5 Ω	400.13	0.955	56.33	5.416	300	300	382.12	305.08	79.84	
400V dc	9.0 Ω	400.05	1.111	56.33	6.364	400	400	444.46	358.48	80.67	
	7.8 Ω	400.16	1.239	56.33	7.134	400	400	495.80	401.86	81.05	
	7.0 Ω	400.03	1.403	56.33	8.105	400	400	561.24	456.55	81.35	
	6.3 Ω	399.95	1.550	56.33	8.956	400	400	619.92	504.49	81.38	115

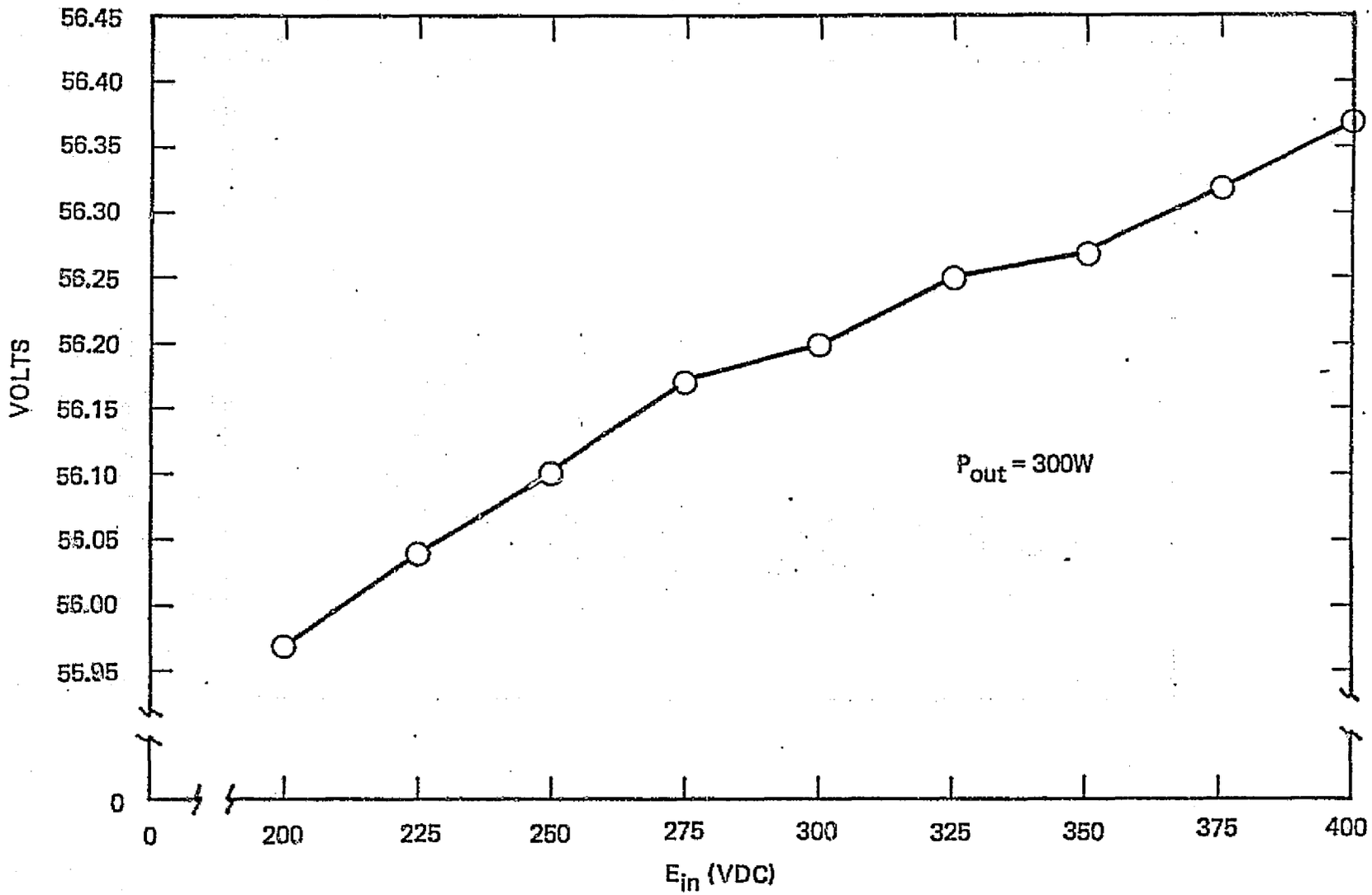


Figure 2-30. 8-Stage Inductive Energy Transfer Circuit Line Regulation

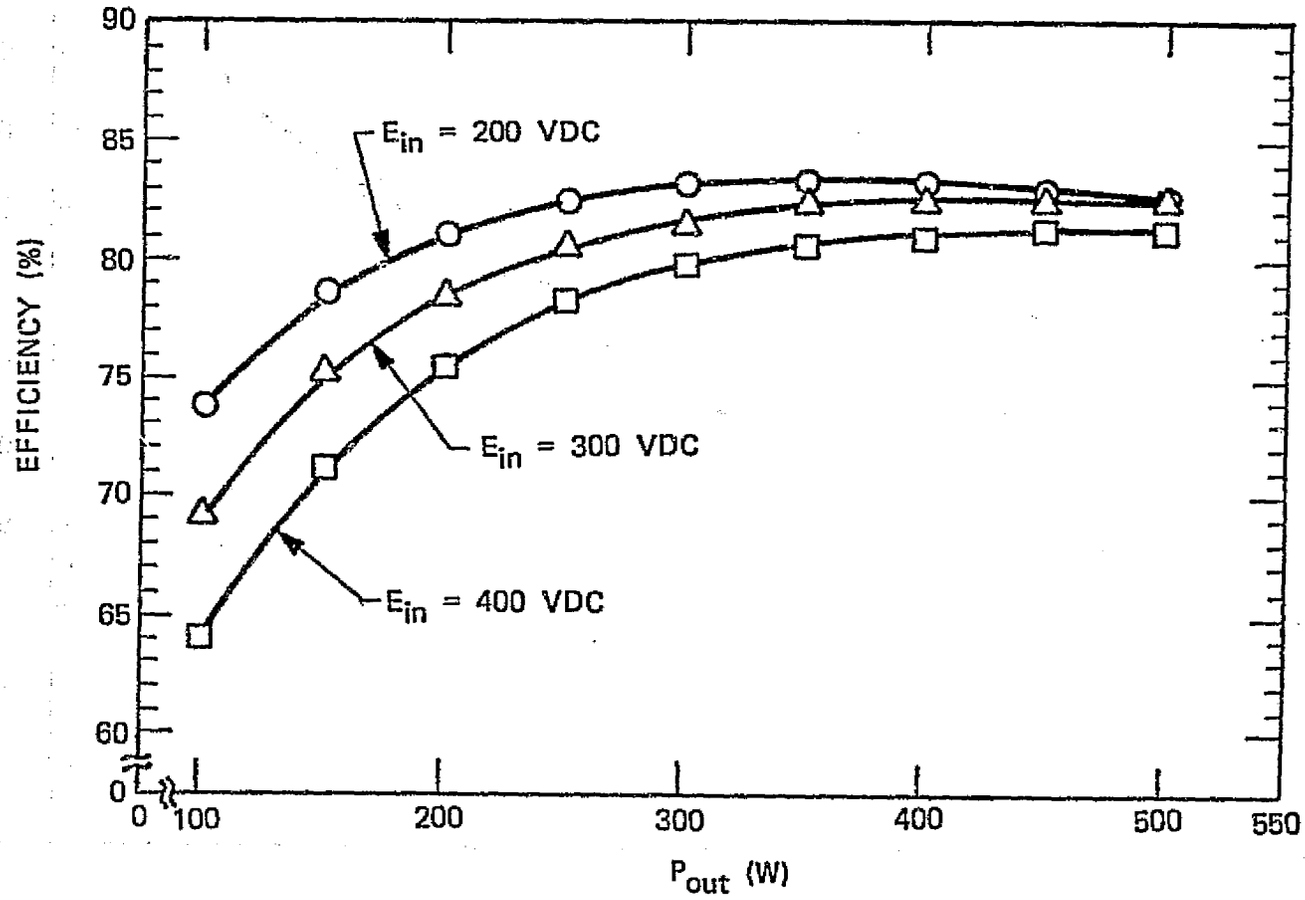


Figure 2-31. 8-Stage Inductive Energy Transfer Circuit Efficiency versus P_{out} and E_{in}

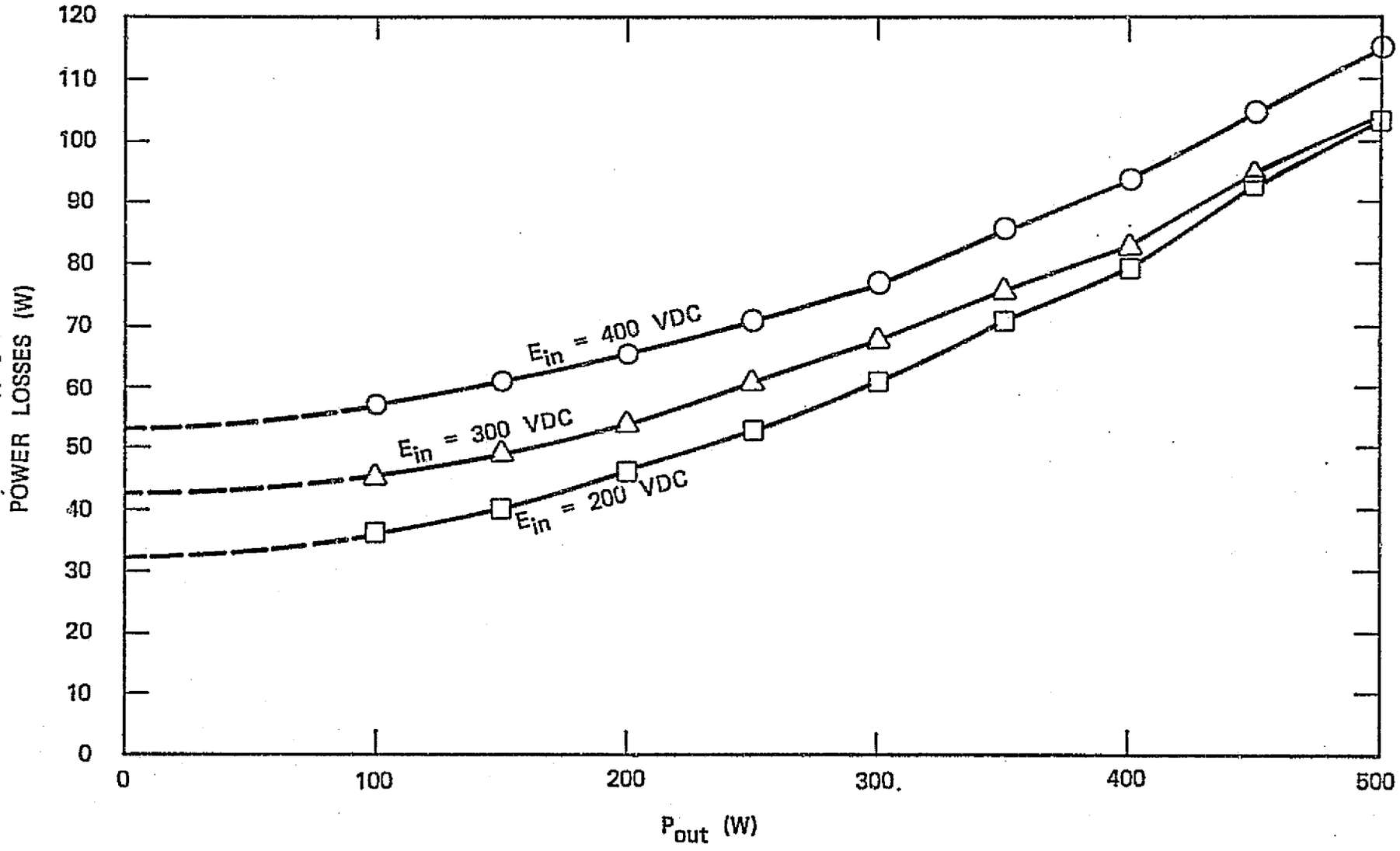


Figure 2-32. 8-Stage Inductive Energy Transfer Circuit Power Losses versus P_{out} and E_{in}

where

E_{in} = input voltage (volts)

P_{out} = output power (watts)

Differentiation of equation 18 at a fixed input voltage demonstrates that the highest point of efficiency occurs where fixed losses equal the quadratic losses. As the fixed losses increase with increasing input voltage, the highest point of efficiency will occur at higher power levels at higher input voltages. This effect can be seen in the efficiency curves where at higher input voltages, the highest point of efficiency moves to the right.

The equation also indicates clearly that an improvement in efficiency can best be accomplished in lowering the input voltage related losses. However, a large number of small stages cannot compete in efficiency with a low number of larger stages of equal total power. Whenever components are used where power capability increases faster than the heat or loss dissipating area, a low number of more powerful units will be more efficient than a high number of low power components. This is one of the reasons why the 8-stage unit does not meet the specified efficiency, even though improvements are possible.

Performance data of the unit as a function of temperature is shown on tables 2-5 through 2-7 and figures 2-33 through 2-39. Data was taken at -20^{o}, $+25^{o}C$ and $+75^{o}C$.

The 8-stage unit displays an output ripple which does not meet the ripple requirements. The main reason for non-compliance with the specification rests with the resolution of the digital control circuit. Due to a lack of flight approved logic components with high enough speed, the resolution is limited.

TABLE 2-5

PERFORMANCE DATA OF THE 8-STAGE IET CIRCUIT AT -20°C

t_{amb} = -20°C 26 January 1975

	R_L (Approx.)	E_{in} (V dc)	I_{in} (A dc)	E_{out} (V dc)	I_{out} (A dc)	Input Ripple (mA p-p)	Output Ripple (mV p-p)	P_{in} (W)	P_{out} (W)	Efficiency %
$E_{in} \approx$ 200V dc	31.4	203.73	0.65	56.05	1.78	40	100	132.43	99.77	75.3
	20.9	203.49	0.91	56.05	2.63	60	30	185.18	147.41	79.6
	15.7	203.27	1.17	56.03	3.49	75	100	237.83	195.55	82.2
	12.5	203.02	1.48	65.03	4.49	100	50	300.47	251.58	83.7
	10.5	202.85	1.75	56.02	5.32	120	100	354.99	298.03	84.0
	9.0	202.65	2.04	56.02	6.21	150	100	413.41	347.88	84.2
	7.8	202.51	2.31	56.01	7.03	150	200	467.80	393.75	84.2
	7.0	202.33	2.64	56.01	8.01	150	100	534.15	448.64	84.0
	6.3	202.22	2.91	56.00	8.83	200	100	588.46	494.48	84.0
$E_{in} \approx$ 300V dc	31.4	300.85	0.47	56.28	1.78	50	50	141.40	100.18	70.8
	20.9	300.68	0.65	56.27	2.65	60	40	195.44	149.12	76.3
	15.7	300.53	0.83	56.26	3.51	100	50	249.44	197.47	79.2
	12.5	300.35	1.03	56.26	4.51	150	300	309.36	253.73	82.0
	10.5	300.22	1.22	56.25	5.35	200	200	366.27	300.94	82.2
	9.0	300.09	1.41	56.25	6.25	200	200	423.13	351.00	83.0
	7.8	299.98	1.59	56.24	7.08	200	250	476.97	398.18	83.5
	7.0	299.86	1.80	56.24	8.05	200	150	539.75	452.73	83.9
	6.3	299.79	1.99	56.24	8.88	150	200	596.58	499.41	83.7
$E_{in} \approx$ 400V dc	31.4	399.64	0.38	56.43	1.79	60	50	151.86	101.01	66.5
	20.9	399.54	0.52	56.42	2.65	80	150	207.76	149.51	72.0
	15.7	399.46	0.65	56.41	3.53	100	75	259.65	199.13	76.7
	12.5	399.35	0.81	56.41	4.52	100	100	323.47	254.97	78.8
	10.5	399.28	0.95	56.40	5.37	150	100	379.32	302.87	79.8
	9.0	399.24	1.09	56.39	6.26	200	150	435.17	353.00	81.1
	7.8	399.20	1.24	56.39	7.11	200	100	495.01	400.93	81.0
	7.0	399.16	1.40	56.39	8.09	200	150	558.82	456.20	81.6
	6.3	399.17	1.54	56.39	8.91	200	200	614.72	502.44	81.7

TABLE 2-6

PERFORMANCE DATA OF THE 8-STAGE IET CIRCUIT AT +25°C

t_{amb} = +25°C 25 January 1975

	R_L (Approx.)	E_{in} (V dc)	I_{in} (A dc)	E_{out} (V dc)	I_{out} (A dc)	Input Ripple (mA p-p)	Output Ripple (mV p-p)	P_{in} (W)	P_{out} (W)	Efficiency %
$E_{in} \approx$ 200V dc	31.4	206.56	0.64	56.04	1.78	40	30	132.20	99.75	75.5
	20.9	206.32	0.90	56.03	2.63	50	150	185.69	147.36	-79.4
	15.7	206.10	1.16	56.02	3.50	100	50	239.08	196.07	82.0
	12.5	205.85	1.47	56.01	4.48	100	100	302.60	250.93	82.9
	10.5	205.66	1.73	56.01	5.32	100	100	355.79	297.97	83.7
	9.0	205.46	2.02	56.00	6.21	120	150	415.03	347.76	83.8
	7.8	205.31	2.29	56.00	7.03	150	200	470.16	393.68	83.7
	7.0	205.14	2.62	55.99	8.01	200	200	537.47	448.48	83.4
	6.3	205.04	2.90	55.99	8.82	200	200	594.62	493.83	83.1
$E_{in} \approx$ 300V dc	31.4	301.78	0.47	56.26	1.78	50	50	141.84	100.14	70.6
	20.9	301.61	0.64	56.26	2.64	50	75	193.03	148.53	76.9
	15.5	301.45	0.82	56.24	3.51	50	50	247.19	197.40	79.9
	12.5	301.28	1.02	56.24	4.51	60	50	307.31	253.64	82.5
	10.5	301.15	1.21	56.24	5.34	80	50	364.39	300.32	82.4
	9.0	301.02	1.40	56.23	6.23	100	50	421.43	350.31	83.1
	7.8	300.92	1.59	56.22	7.07	100	50	478.46	397.48	83.1
	7.0	300.81	1.80	56.20	8.05	250	500	541.46	452.41	83.6
	6.3	299.90	2.00	56.20	8.86	400	500	599.80	497.93	83.0
$E_{in} \approx$ 400V dc	31.4	400.42	0.38	56.42	1.79	60	150	152.16	100.99	66.4
	20.9	400.33	0.52	56.41	2.65	60	50	208.17	149.49	71.8
	15.7	400.25	0.65	56.40	3.53	70	150	260.16	199.09	76.5
	12.5	400.18	0.80	56.39	4.52	100	50	320.14	254.88	79.6
	10.5	400.12	0.95	56.38	5.36	100	50	380.11	302.02	79.5
	9.0	400.05	1.09	56.38	6.27	100	200	436.06	353.50	81.1
	7.8	400.02	1.23	56.38	7.12	100	150	492.03	401.43	81.6
	7.0	399.98	1.40	56.36	8.09	100	100	559.97	455.95	81.4
	6.3	399.97	1.54	56.36	8.93	100	100	615.95	503.30	81.7

TABLE 2-7

PERFORMANCE DATA OF THE 8-STAGE IET CIRCUIT AT +75°C

t_{amb} = +75°C 26 January 1975

	R_L (Approx.)	E_{in} (V dc)	I_{in} (A dc)	E_{out} (V dc)	I_{out} (A dc)	Input Ripple (mA p-p)	Output Ripple (mV p-p)	P_{in} (W)	P_{out} (W)	Efficiency %
$E_{in} \approx$ 200V dc	31.4	229.4	0.59	56.13	1.79	100	200	135.35	100.47	74.2
	20.9	229.1	0.83	56.11	2.65	200	400	190.15	148.69	78.2
	15.7	228.9	1.07	56.10	3.51	200	300	244.92	196.91	80.4
	12.5	228.7	1.35	56.09	4.49	200	500	308.74	251.84	81.6
	10.5	228.5	1.58	56.08	5.34	300	500	361.03	299.47	82.9
	9.0	228.4	1.85	56.08	6.22	300	500	422.54	348.82	82.6
	7.8	228.2	2.11	56.07	7.05	500	1000	481.50	395.29	82.1
	7.0	228.0	2.42	56.07	8.02	500	1000	551.76	449.68	81.5
	6.3	228.0	2.68	56.07	8.82	500	1000	611.04	494.54	80.9
$E_{in} \approx$ 300V dc	31.4	300.5	0.467	56.29	1.79	80	300	140.33	100.76	71.8
	20.9	300.3	0.645	56.26	2.65	100	50	193.69	149.09	77.0
	15.7	300.1	0.826	56.28	3.52	100	200	247.88	198.11	79.9
	12.5	299.9	1.04	56.25	4.51	100	200	311.90	253.69	81.3
	10.5	299.8	1.22	56.25	5.35	200	150	365.76	300.94	82.3
	9.0	299.7	1.43	56.23	6.25	200	200	428.57	351.44	82.0
	7.8	299.6	1.64	56.22	7.08	500	500	491.34	398.04	81.0
	7.0	299.5	1.88	56.20	8.05	600	600	563.06	452.41	80.3
	6.3	299.4	2.09	56.21	8.86	1000	1000	625.75	498.02	79.6

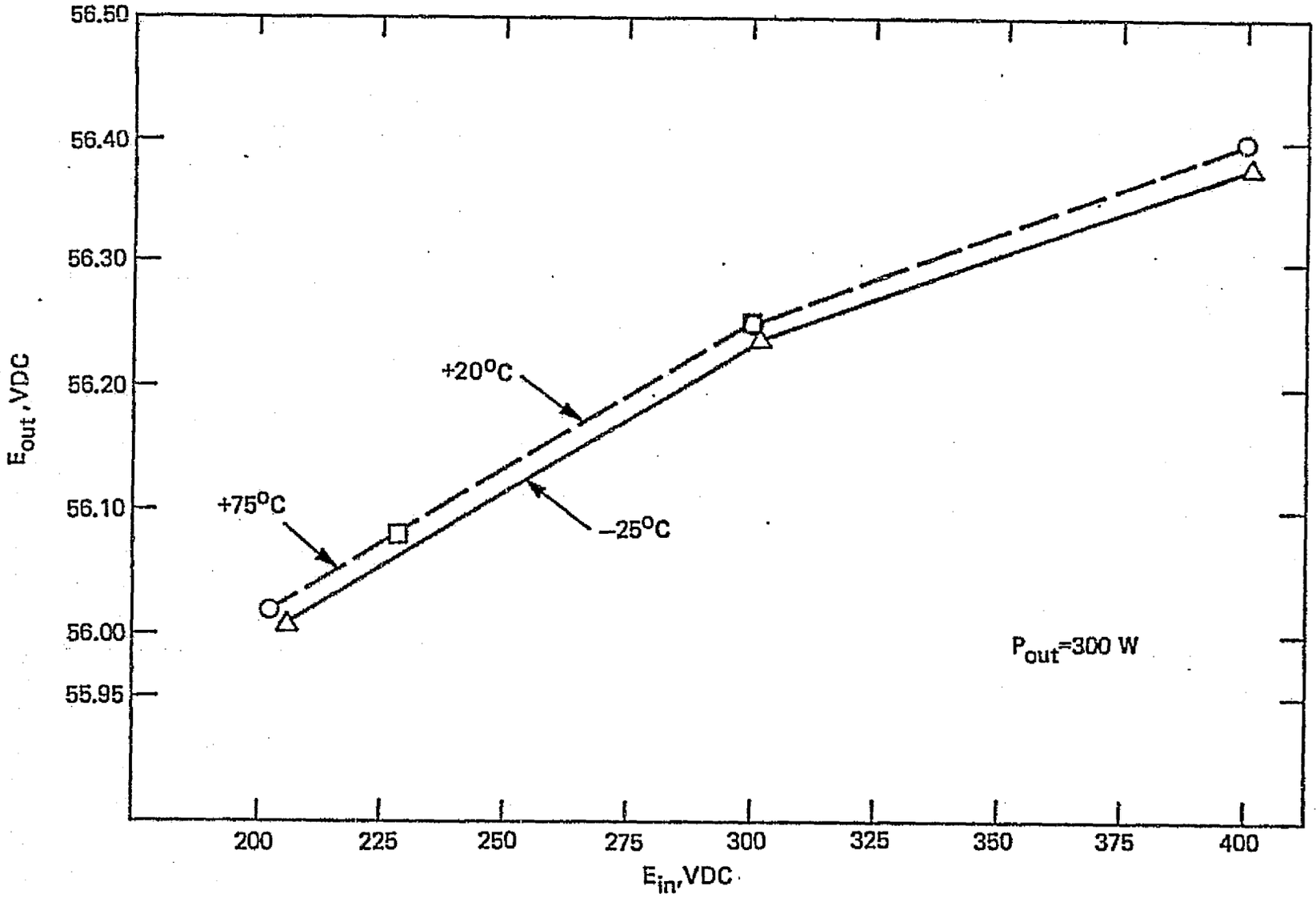


Figure 2-33. 8-Stage Inductive Energy Transfer Circuit Regulation as Function of Input Voltage and Temperature

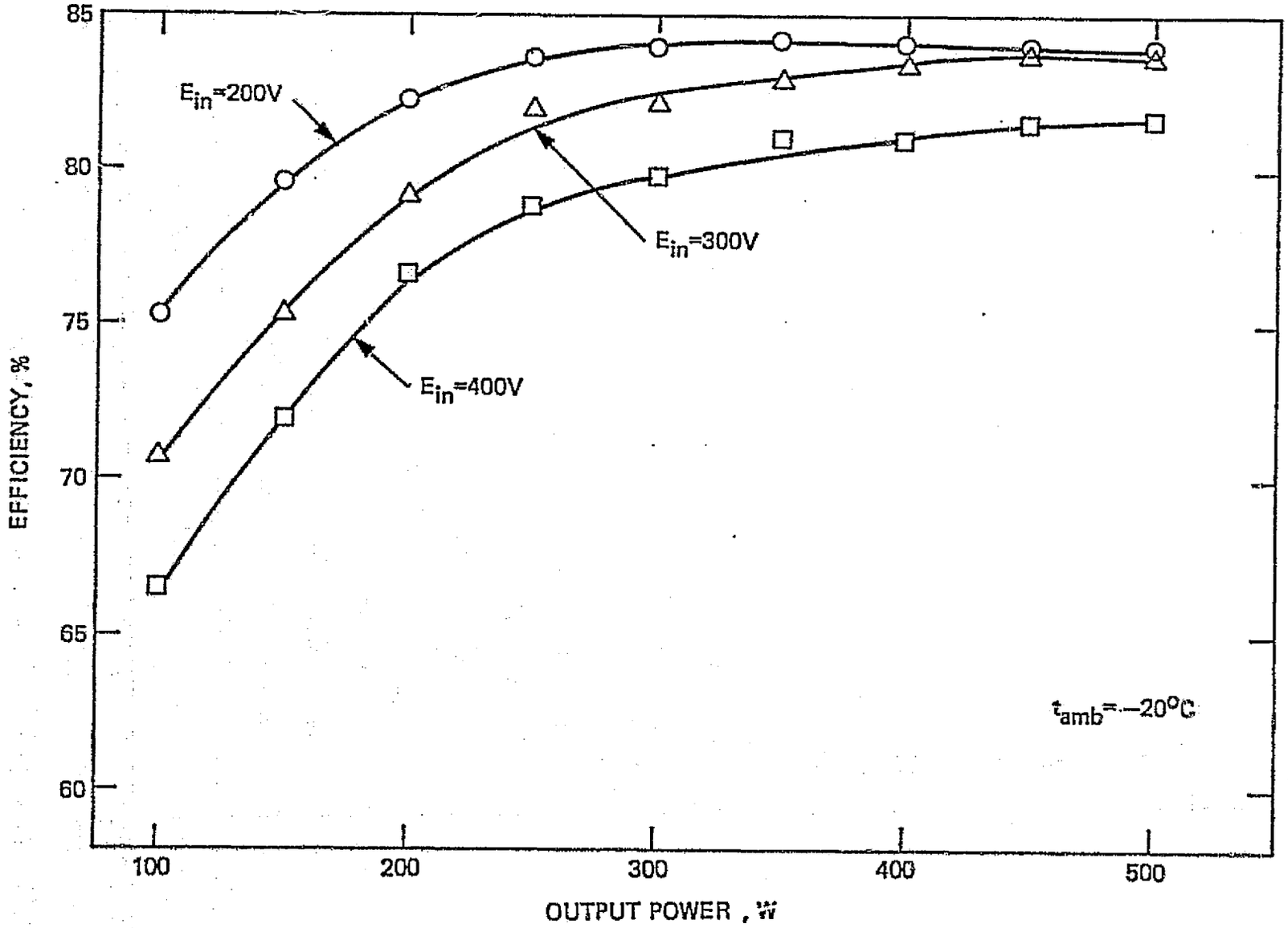


Figure 2-34. 8-Stage Inductive Energy Transfer Circuit Efficiency versus P_{out} and E_{in} at -20°C Temperature

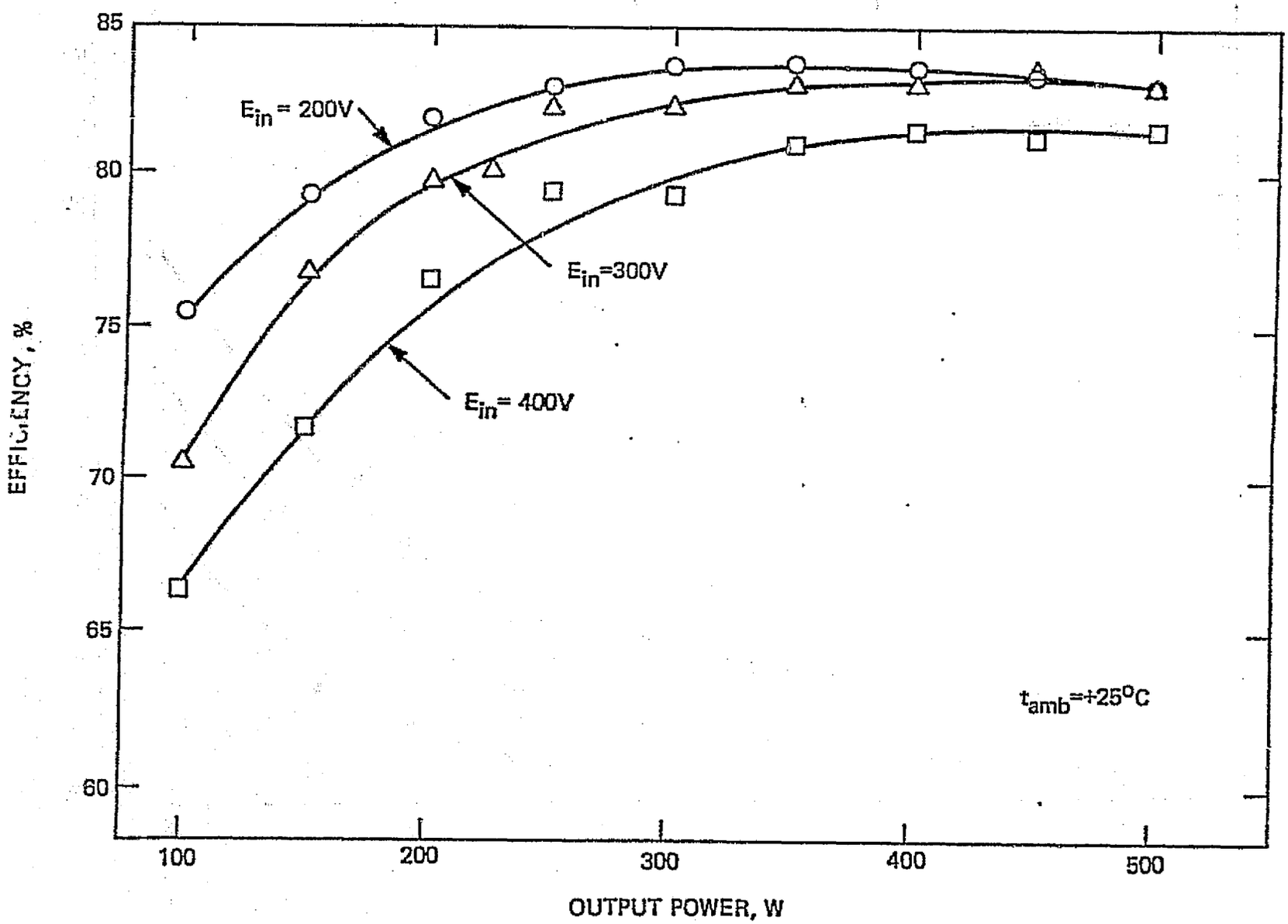


Figure 2-35. 8-State Inductive Energy Transfer Circuit Efficiency versus P_{out} and E_{in} at +25°C

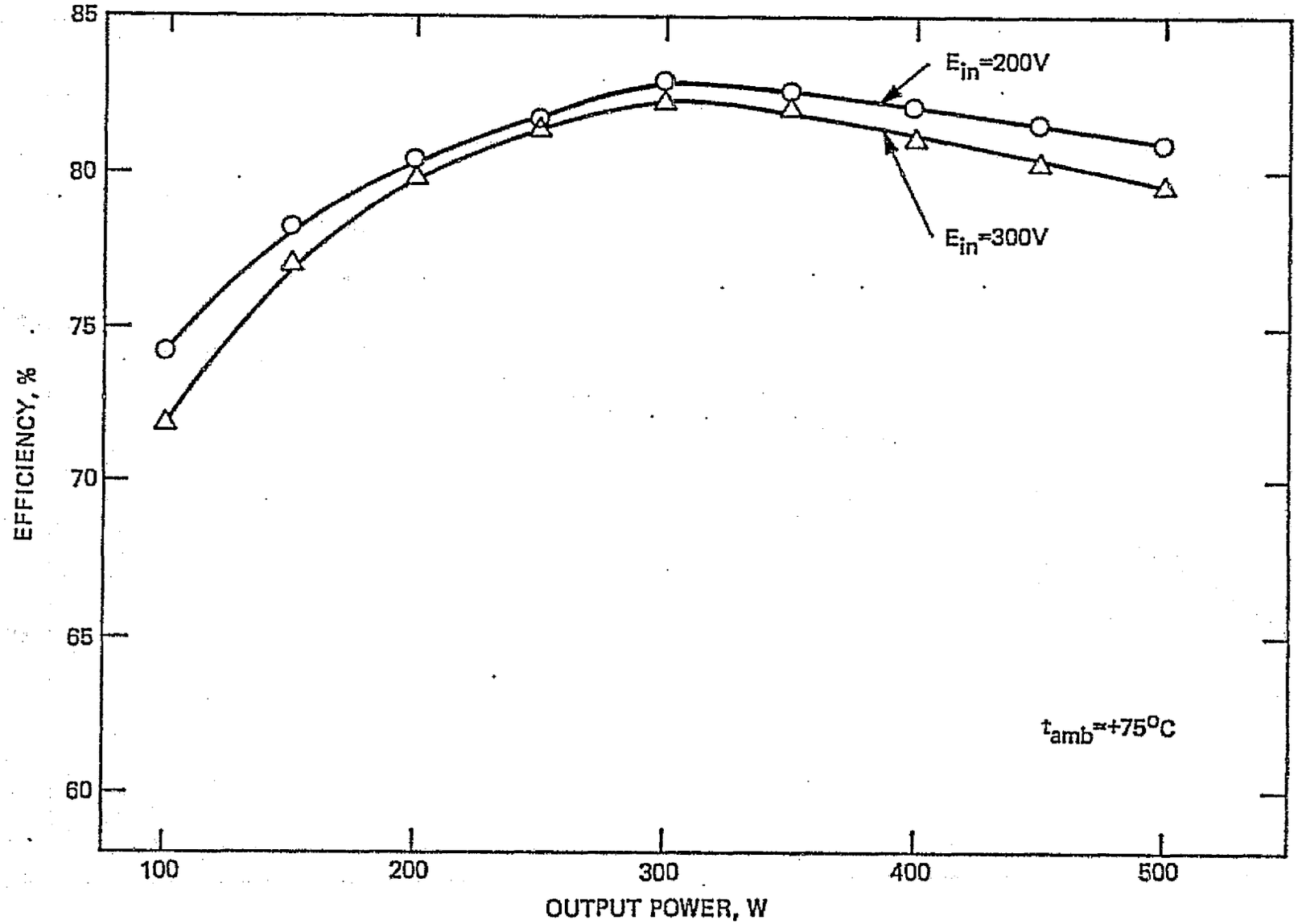


Figure 2-36. 8-Stage Inductive Energy Transfer Circuit Efficiency versus P_{out} and E_{in} at +75°C

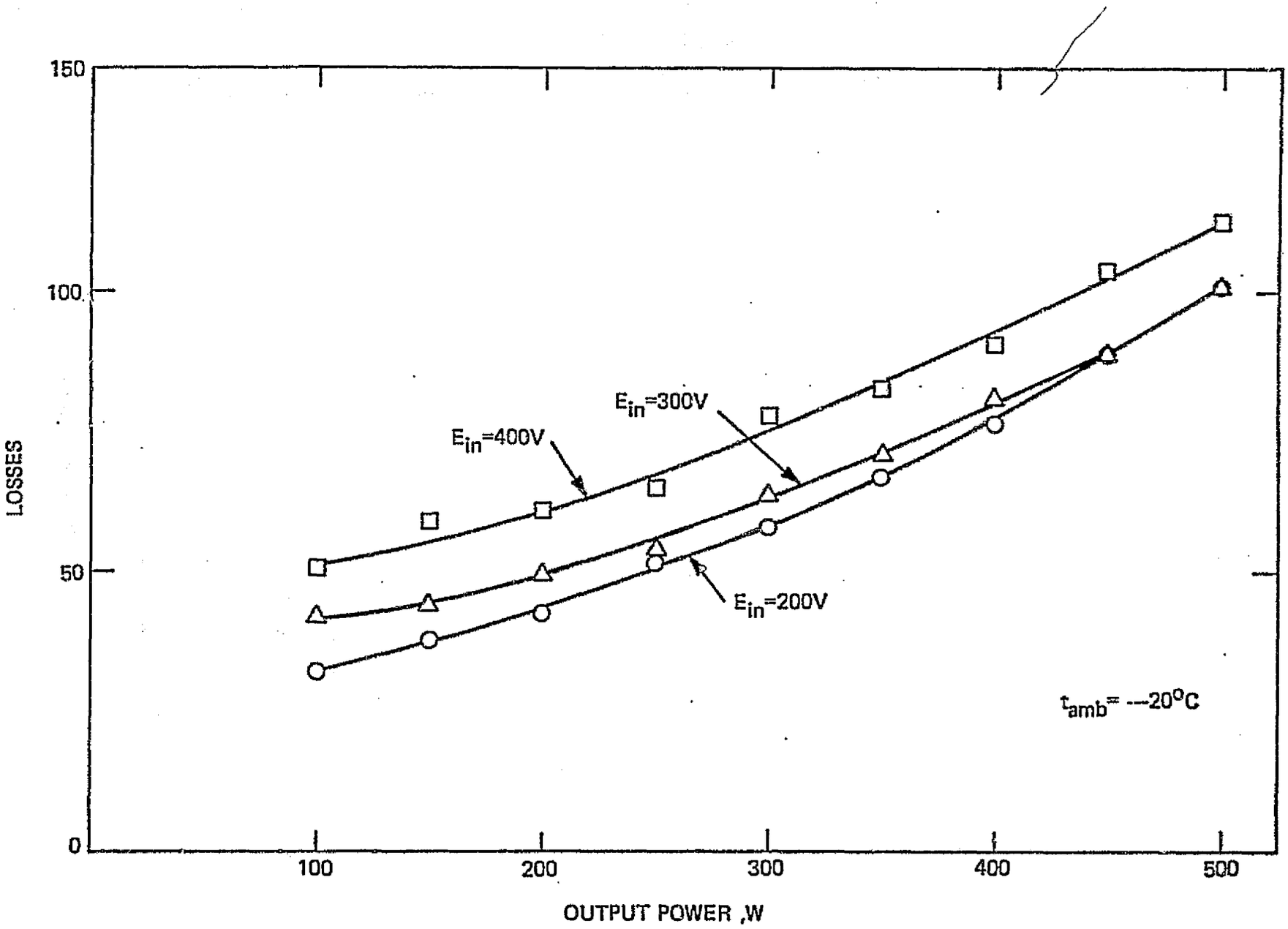


Figure 2-37. 8-Stage Inductive Energy Transfer System Losses versus P_{out} and E_{in} at -20°C

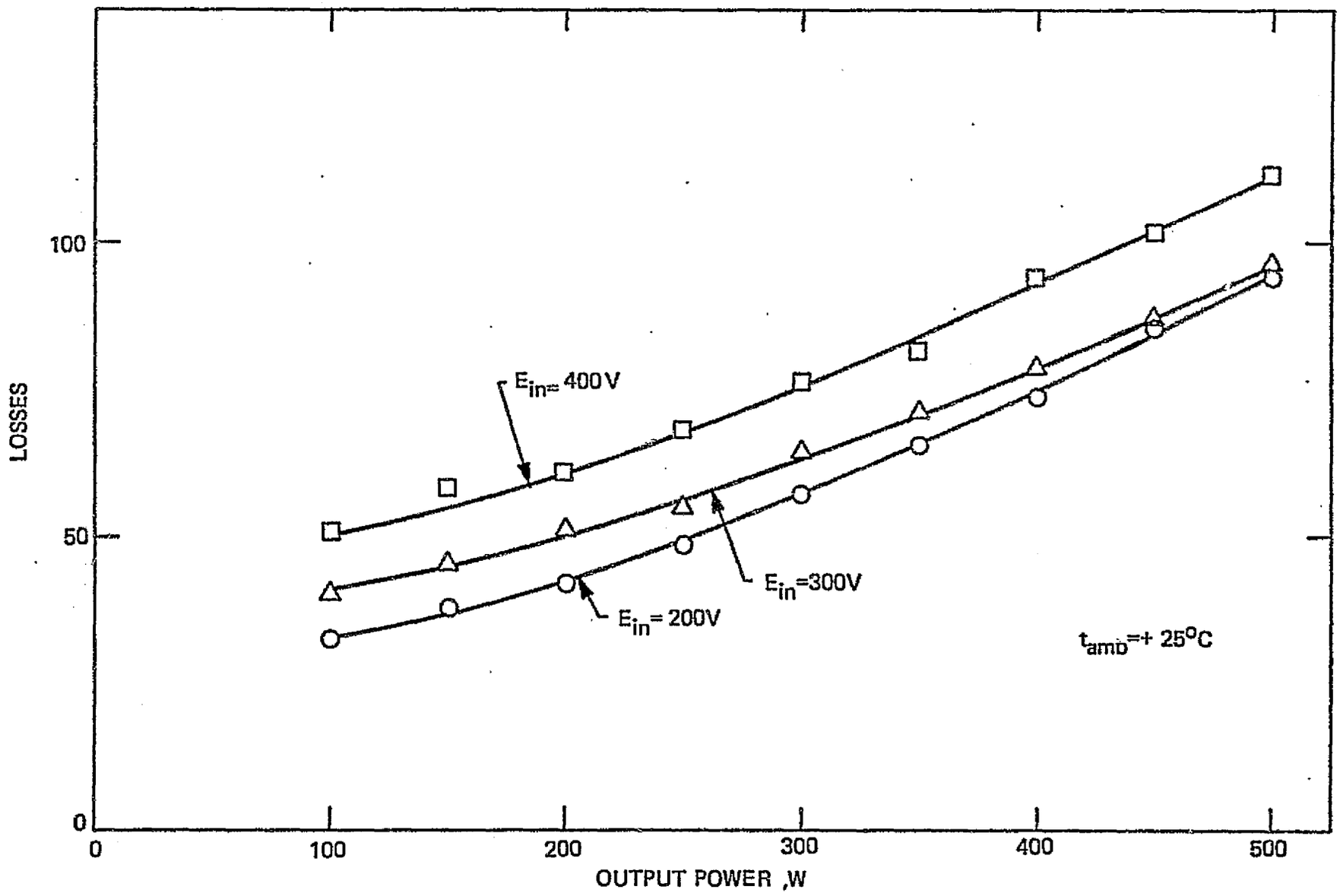


Figure 2-38. 8-Stage Inductive Energy Transfer System Losses versus P_{out} and E_{in} at +25°C

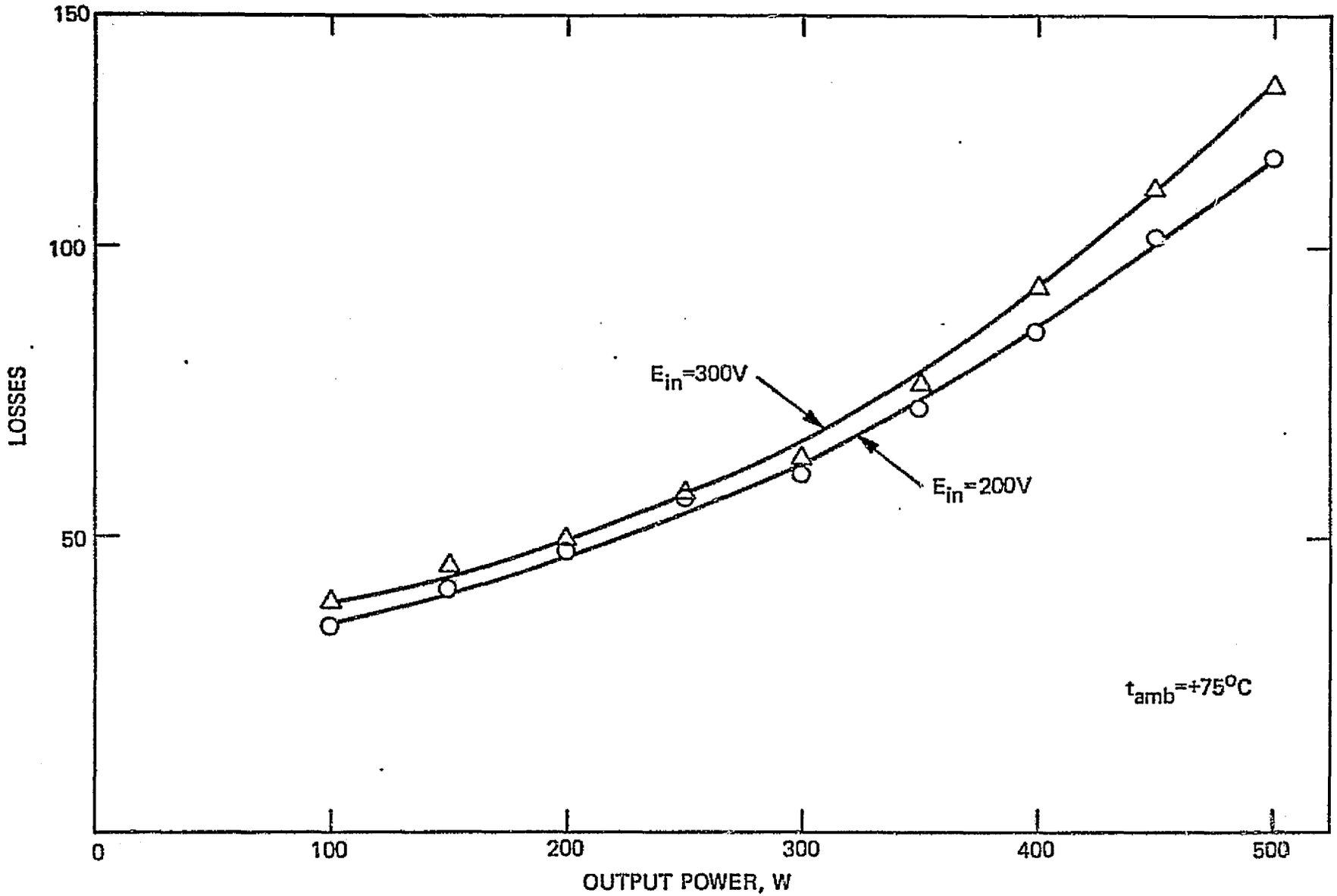


Figure 2-39. 8-Stage Inductive Energy Transfer System Losses versus P_{out} and E_{in} at +75°C

Whenever input voltage and load conditions allow the digital control circuit to operate on exactly one digit (and not between digits) only the 80 kHz ripple component is apparent and meets the ripple requirement. If, however, the sensing circuit forces the digital control to operate between digits (below resolution) the control will flutter between one or more digits. This results in the random appearing output ripple "spikes" which are superimposed on the inherent 80 kHz ripple. Higher clock frequency would require higher speed in the logic circuitry and would increase resolution and decrease "ripple". At present, flight-approved components meeting this requirement are not available.

Four analog control ramps could also have controlled 8 stages. Temperature drift calculations, however, indicated that uniformity in pulse-width and spacing would be very difficult to achieve. For this reason, as pointed out before, an analog control circuit was ruled out even though it would not have shown the problem associated with digital resolution.

The stability of the 8 stage 45 degree staggered unit is reflected in the Bode plots for minimum (20 percent) and maximum load, figures 2-40 and 2-41. The gain margins are -23 db and -22 db, respectively, and the phase margins are 72 degrees and 50 degrees. As a gain margin of 6 db and a phase margin of 45 degree is generally considered sufficient, the unit displays a high degree of stability.

The 8 stage 45 degree staggered unit allowed operation with only 6 of the 8 stages without upsetting performance to any unacceptable degree. Thus, parallel redundancy is a capability of the multistage, staggered approach. By the same token, the addition of other staggered stages can be accomplished with relative ease and without requiring additional filter circuits. An increase in number of stages raises the ripple frequency and would not place a greater stress on the filter capacitor at the same total output power levels.

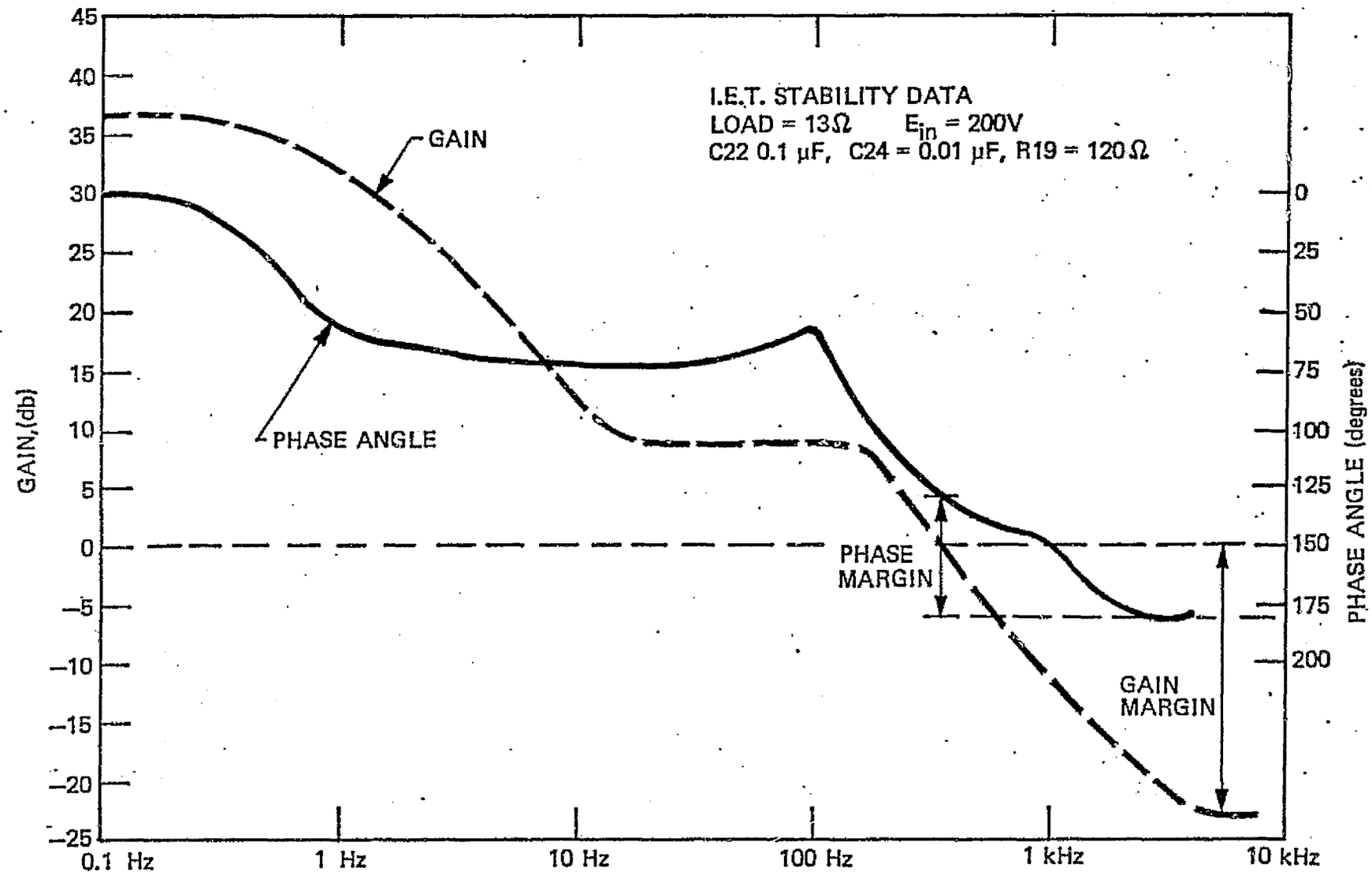


Figure 2-40. 8-Stage IET Stability at Minimum Load

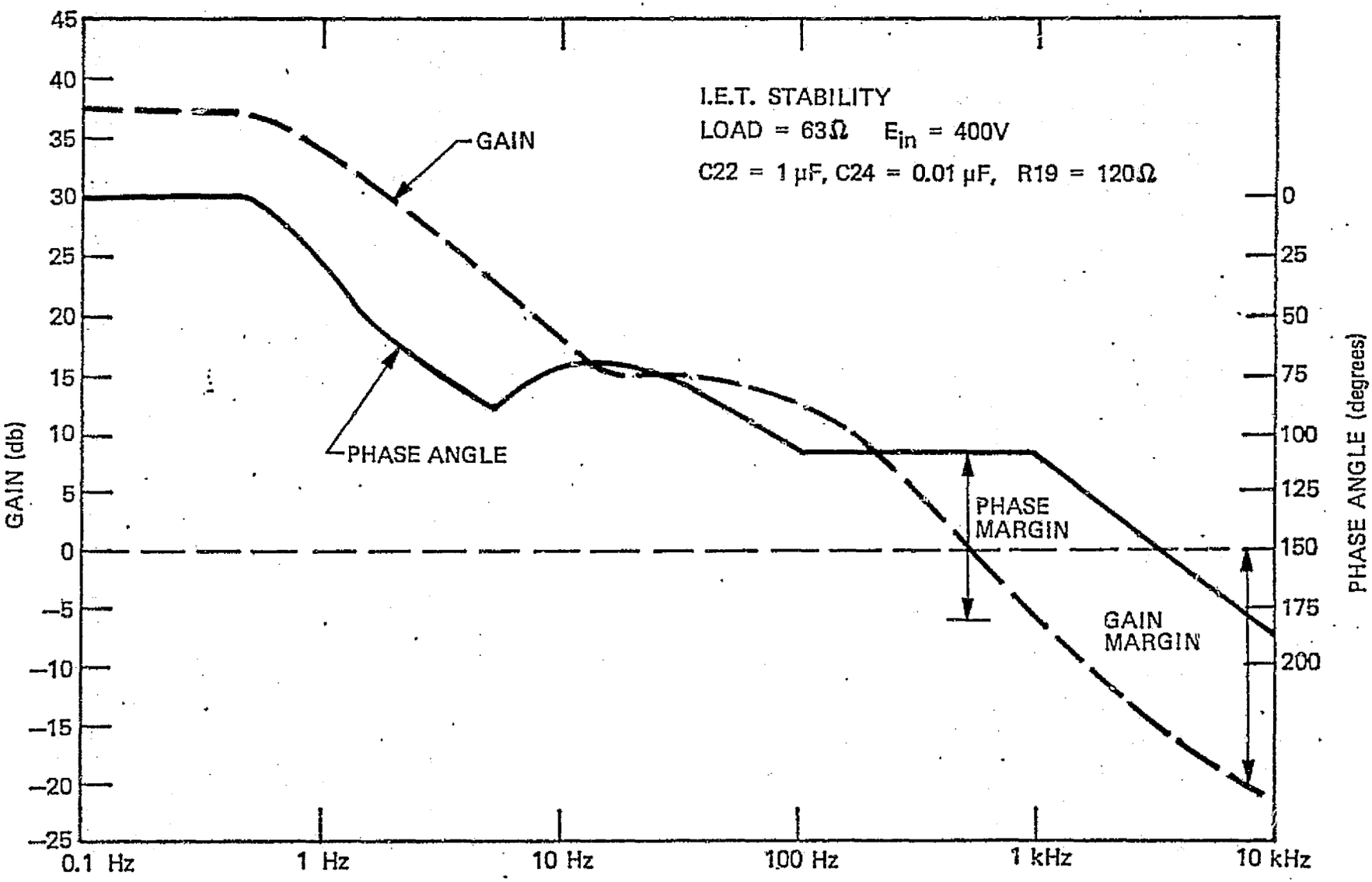


Figure 2-41. 8-Stable IET Stability Data at Maximum Load

2.4.7 APPRAISAL OF PROBLEM AREAS ENCOUNTERED

The firm requirement to use flight proven or flight approvable hardware caused deviations from the best approach and lowered the performance characteristics and increased complexity. Of particular impact were the requirements to use T061 packaged transistors. These transistors had a sustained breakdown voltage of 400 volts and made it necessary to operate with two capacitors in series on the primary side. Thus, each stage operated with two transistors in series and with two input filter capacitors in series. This resulted in double the number of driver circuits, transistors, transistor protective devices, input filter capacitors, etc. One transistor per stage with the appropriate voltage and current rating would have been the preferred choice and would have considerably improved efficiency and reliability and decreased complexity. Elimination of the driver transformer would also have been possible. It is expected that higher voltage components will be available in the near future.

The breadboard uses R-C despiking networks which cause losses between 20 and 25 watts. These losses can be reduced with energy recovery networks.

The total losses caused by using lower voltage components and despiking networks is more than 50 watts at full output power. Considerable improvement can be made by using higher voltage components. Commercial transistors that are available today can be used to demonstrate this feasibility. Demonstration with flight proven or flight approvable components can be appropriately left to later development.

The digital control circuit has the exceptional advantage of being capable of delivering pulses of equal length and equal spacing with almost no sensitivity to temperature changes. However, the logic circuit only operates properly within a well specified voltage range. Outside

this range, performance of the logic circuit becomes unpredictable and can cause failures of the power stages. This is the reason the 5 volt logic voltage is applied only after a delay and only after the other voltages were established. The input voltage sensitivity of the logic circuit is thus a factor which must be taken into account under all transient and steady state conditions. A separate logic voltage regulator would therefore be preferable.

The resolution of the digital control circuit causes a flutter when the sensing circuit is not compared with a specific number but rather flutters between one or several digits. The result is an apparent output ripple. Components capable of operating at higher frequency will eventually eliminate this problem below nominal ripple voltage values.

Output power balancing of all stages was a severe problem during the developmental phase. Even though a solution was found, further investigation is required to clarify the different performance characteristics of the circuit when operating into plair resistance load or into a resistive load with filter capacitors across it.

SECTION 3

RECOMMENDATIONS FOR IMPROVEMENT IN THE HARDWARE

For the 8 stage 45 degree staggered IET unit the following improvements in the hardware are recommended.

3.1 IMPROVEMENTS IN THE POWER STAGES

a. Use one transistor per stage and eliminate the series transistors.

b. Where possible, eliminate the driver transformers and use an all transistorized load current proportional drive circuit.

c. Avoid series connected input filter capacitors.

d. Eliminate despiking networks and employ energy recovery techniques.

e. Perform a detailed investigation of the operating characterstics of the balancing circuit, i.e., the characteristics of the balancing inductor, and of the parallel L-C combination. Investigate operation into plain resistive load and into resistive load with filter capacitors.

3.2 IMPROVEMENT IN THE DIGITAL CONTROL CIRCUIT

a. Achieve better resolution by using higher frequency components and eliminate or decrease "ripple voltage" caused by insufficient resolution.

b. Drive all logic circuits from a well defined and regulated voltage source such that operation in the "grey area" of unpredictability is eliminated.

3.3 IMPROVEMENT IN AUXILIARY SUPPLIES

Provide power supplies which meet all input requirements. Whenever input requirements are not met, this should at least assure proper operation of a logic circuit which disables the supply completely and protects against improper operation of the power stages.

SECTION 4

CONCLUSIONS

During the course of the contract, several areas of new technology were explored.

These areas included the use of an all digital control circuit. Its advantages, disadvantages, and future possibilities were explored. The circuit allowed precise generation of pulses of equal length, equal spacing and easy stabilization.

This program demonstrated that the 8-stage circuit has built-in redundancy and can continue to operate when one pair of stages is lost. It also showed that filter requirements are reduced and that the modular approach provides add-on power capability.

In the area of efficiency, the multiple stage unit cannot compete with the 2-stage 180 degree unit.

Depending on the requirements of the supply, the 2-stage and the multiple, staggered-stage approach both have advantages and disadvantages which must be carefully weighed before committing a system to one approach.

SECTION 5

NEW TECHNOLOGY

The application of a multi-winding balancing inductor, in a series with a parallel L-C circuit, accomplished uniform power sharing between all stages.

SECTION 6

RECOMMENDATIONS

Due to the different performance characteristics obtained when operating into a pure resistive or into a resistive load with a filter capacitor, it is recommended that an additonal investigation be conducted. The effort should consist of a complete theoretical analysis leading to a comprehensive design procedure.

APPENDIX A

COMPUTER PRINTOUT

APPENDIX A

```
 SAVE OVER ENTRANS1
>RUN
11:33   AUG 12  ENTRANS1...
THIS IS INDUCTIV ENERGY TRANSFER SYSTEM ENTRANS1.
 THE FOLLOWING VALUES FOR A SINGLE STAGE INDUCTIVE ENERGY TRANSFER
SYSTEM WITH PRIMARY AND SECONDARY WINDINGS ARE CALCULATED AT
MAXIMUM OUTPUT POWER P2= 250 WATT AS FUNCTION OF INPUT VOLTAGE E1
AND TURNS RATIO PRIMARY / SECONDARY= K= N1/N2:
 T1= ON-TIME OF PRIMARY WINDING, D= DUTY CYCLE OF PRIMARY WINDING,
E3= MAXIMUM BLOCKING VOLTAGE OF INPUT SWITCH, L2= MINIMUM
REQUIRED SECONDARY INDUCTANCE, L1= CORRESPONDING PRIMARY INDUCTANCE,
D1= TOTAL CHANGE IN INPUT CURRENT AS CAUSED BY E1*T1, D2= TOTAL
CHANGE IN OUTPUT CURRENT AS CAUSED BY E2*(T-T1), I1= AVERAGE
INPUT CURRENT DURING T1, I2= LOWEST INITIAL VALUE OF INPUT CURRENT,
I3= HIGHEST END VALUE OF INPUT CURRENT, I4= RMS VALUE OF INPUT
CURRENT, I5= AVERAGE VALUE OF INPUT CURRENT, I6= RMS RIPPLE
CURRENT ON AVERAGE INPUT CURRENT, A1 THROUGH A6 ARE THE CORRESPON
DING CURRENT VALUES IN THE SECONDARY WINDING, N4= REQUIRED INCH TO
THE FOURTH OF TOROIDAL INDUCTOR-TRANSFORMER.
   THE OUTPUT VOLTAGE IS CONSTANT AT E2= 56 VOLT DC. THE MAXIMUM
OUTPUT POWER IS P2= 250 WATT AND THE MINIMUM OUTPUT POWER IS
P3= 50 WATT. THE FREQUENCY IS F= 5000 HZ AND THE DURATION OF ONE
PERIOD IS T= 1/F. THE SELECTED PEAK FLUX DENSITY IS B= 6 KG. THE
SELECTED CIRC-MILS PER AMPERE ARE C= 500. THE SECONDARY MINIMUM
INDUCTANCE L2 IS CALCULATED SUCH THAT THE RESET TIME AT MINIMUM
OUTPUT POWER P3 IS EQUAL TO THE OFF-TIME. HENCE THERE IS NO
INTERRUPTION IN CURRENT FLOW IN THE INDUCTOR - TRANSFORMER
AND ALL CURRENT-WAVESHAPES ARE TRAPEZOIDAL. LOSSES ARE NEGLECTED.

K=   1        E1=    200    T1=    4.37500E-05        D=   .218750
E3=    256    L2=    3.82813E-03        L1=    3.82813E-03
D1=    2.28571          D2=    2.28571          I1=    5.71429
I2=    4.57143          I3=    6.85714          I4=    2.69037
I5=    1.25000          I6=    2.38235
A1=    5.71429          A2=    4.57143          A3=    6.85714
A4=    5.08432          A5=    4.46429          A6=    2.43321
N4=    .485918

K=   1        E1=    250    T1=    3.66013E-05        D=   .183007
E3=    306    L2=    4.18642E-03        L1=    4.18642E-03
D1=    2.18571          D2=    2.18571          I1=    5.46429
I2=    4.37143          I3=    6.55714          I4=    2.35311
I5=    1      I6=    2.13006
A1=    5.46429          A2=    4.37143          A3=    6.55714
A4=    4.97186          A5=    4.46429          A6=    2.18850
N4=    .478756

K=   1        E1=    300    T1=    3.14607E-05        D=   .157303
E3=    356    L2=    4.45398E-03        L1=    4.45398E-03
D1=    2.11905          D2=    2.11905          I1=    5.29762
I2=    4.23810          I3=    6.35714          I4=    2.11508
I5=    .833333          I6=    1.94399
A1=    5.29762          A2=    4.23810          A3=    6.35714
A4=    4.89545          A5=    4.46429          A6=    2.00887
N4=    .472620
```

K= 1 I E1= 350 T1= 2.75862E-05 D= .137931
E3= 406 L2= 4.66112E-03 L1= 4.66112E-03
D1= 2.07143 D2= 2.07143 I1= 5.17857
I2= 4.14286 I3= 6.21429 I4= 1.93605
I5= .714286 I6= 1.79947
A1= 5.17857 A2= 4.14286 A3= 6.21429
A4= 4.84013 A5= 4.46429 A6= 1.87003
N4= .467323

K= 1 E1= 400 T1= 2.45614E-05 D= .122807
E3= 456 L2= 4.82610E-03 L1= 4.82610E-03
D1= 2.03571 D2= 2.03571 I1= 5.08929
I2= 4.07143 I3= 6.10714 I4= 1.79533
I5= .625000 I6= 1.68303
A1= 5.08929 A2= 4.07143 A3= 6.10714
A4= 4.79822 A5= 4.46429 A6= 1.75872
N4= .462706

K= 2 E1= 200 T1= 7.17949E-05 D= .358974
E3= 312 L2= 2.57725E-03 L1= 1.03090E-02
D1= 1.39286 D2= 2.78571 I1= 3.48214
I2= 2.78571 I3= 4.17857 I4= 2.10017
I5= 1.25000 I6= 1.68767
A1= 6.96429 A2= 5.57143 A3= 8.35714
A4= 5.61294 A5= 4.46429 A6= 3.40224
N4= .503245

K= 2 E1= 250 T1= 6.18785E-05 D= .309392
E3= 362 L2= 2.99136E-03 L1= 1.19654E-02
D1= 1.29286 D2= 2.58571 I1= 3.23214
I2= 2.58571 I3= 3.87857 I4= 1.80976
I5= 1 I6= 1.50839
A1= 6N46429 A2= 5.17143 A3= 7.75714
A4= 5.40770 A5= 4.46429 A6= 3.05178
N4= .498742

K= 2 E1= 300 T1= 5.43689E-05 D= .271845
E3= 412 L2= 3.32548E-03 L1= 1.33019E-02
D1= 1.22619 D2= 2.45238 I1= 3.06548
I2= 2.45238 I3= 3.67857 I4= 1.60892
I5= .833333 I6= 1.37629
A1= 6.13095 A2= 4.90476 A3= 7.35714
A4= 5.26643 A5= 4.46429 A6= 2.79382
N4= .494229

K= 2 E1= 350 T1= 4.84848E-05 D= .242424
E3= 462 L2= 3.59963E-03 L1= 1.43985E-02
D1= 1.17857 D2= 2.35714 I1= 2.94643
I2= 2.35714 I3= 3.53571 I4= 1.46036
I5= .714286 I6= 1.27375
A1= 5.89286 A2= 4.71429 A3= 7.07143
A4= 5.16315 A5= 4.46429 A6= 2.59390
N4= .489932

K=	2	E1=	400	T1=	4.37500E-05	D=	.218750
E3=	512	L2=	3.82813E-03		L1=	1.53125E-02	
D1=	1.14286			D2=	2.28571	I1=	2.85714
I2=	2.28571			I3=	3.42857	I4=	1.34519
I5=	.625000			I6=	1.19118		
A1=	5.71429			A2=	4.57143	A3=	6.85714
A4=	5.08432			A5=	4.46429	A6=	2.43321
N4=	.485918						

K=	3	E1=	200	T1=	9.13043E-05	D=	.456522
E3=	368	L2=	1.85255E-03		L1=	1.66730E-02	
D1=	1.09524			D2=	3.28571	I1=	2.73810
I2=	2.19048			I3=	3.28571	I4=	1.86232
I5=	1.25000			I6=	1.38049		
A1=	8.21429			A2=	6.57143	A3=	9.85714
A4=	6.09589			A5=	4.46429	A6=	4.15091
N4=	.507951						

K=	3	E1=	250	T1=	8.03828E-05	D=	.401914
E3=	418	L2=	2.24354E-03		L1=	2.01918E-02	
D1=	.995238			D2=	2.98571	I1=	2.48810
I2=	1.99048			I3=	2.98571	I4=	1.58785
I5=	1	I6=	1.23340				
A1=	7.46429			A2=	5.97143	A3=	8.95714
A4=	5.81094			A5=	4.46429	A6=	3.71983
N4=	.505956						

K=	3	E1=	300	T1=	7.17949E-05	D=	.358974
E3=	468	L2=	2.57725E-03		L1=	2.31953E-02	
D1=	.928571			D2=	2.78571	I1=	2.32143
I2=	1.85714			I3=	2.78571	I4=	1.40011
I5=	.833333			I6=	1.12511		
A1=	6.96429			A2=	5.57143	A3=	8.35714
A4=	5.61294			A5=	4.46429	A6=	3.40224
N4=	.503245						

K=	3	E1=	350	T1=	6.48649E-05	D=	.324324
E3=	518	L2=	2.86340E-03		L1=	2.57706E-02	
D1=	.880952			D2=	2.64286	I1=	2.20238
I2=	1.76190			I3=	2.64286	I4=	1.26258
I5=	.714286			I6=	1.04111		
A1=	6.60714			A2=	5.28571	A3=	7.92857
A4=	5.46713			A5=	4.46429	A6=	3.15588
N4=	.500263						

K=	3	E1=	400	T1=	5.91549E-05	D=	.295775
E3=	568	L2=	3.11049E-03		L1=	2.79944E-02	
D1=	.845238			D2=	2.53571	I1=	2.11310
I2=	1.69048			I3=	2.53571	I4=	1.15685
I5=	.625000			I6=	.973483		
A1=	6.33929			A2=	5.07143	A3=	7.60714
A4=	5.35516			A5=	4.46429	A6=	2.95768
N4=	.497222						

C-2

K= 4 E1= 200 T1= 1.05660E-04 D= .528302
E3= 424 L2= 1.39551E-03 L1= 2.23282E-02
D1= .946429 D2= 3.78571 I1= 2.36607
I2= 1.89286 I3= 2.83929 I4= 1.73119
I5= 1.25000 I6= 1.19772
A1= 9.46429 A2= 7.57143 A3= 11.3571
A4= 6.54329 A5= 4.46429 A6= 4.78380
N4= .508228

K= 4 E1= 250 T1= 9.45148E-05 D= .472574
E3= 474 L2= 1.74473E-03 L1= 2.79158E-02
D1= .846429 D2= 3.38571 I1= 2.11607
I2= 1.69286 I3= 2.53929 I4= 1.46434
I5= 1 I6= 1.06971
A1= 8.46429 A2= 6.77143 A3= 10.1571
A4= 6.18796 A5= 4.46429 A6= 4.28497
N4= .508241

K= 4 E1= 300 T1= 8.54962E-05 D= .427481
E3= 524 L2= 2.05582E-03 L1= 3.28932E-02
D1= .779762 D2= 3.11905 I1= 1.94940
I2= 1.55952 I3= 2.33929 I4= 1.28303
I5= .833333 I6= .975561
A1= 7.79762 A2= 6.23810 A3= 9.35714
A4= 5.93927 A5= 4.46429 A6= 3.91728
N4= .507086

K= 4 E1= 350 T1= 7.80488E-05 D= .390244
E3= 574 L2= 2.33195E-03 L1= 3.73111E-02
D1= .732143 D2= 2.92857 I1= 1.83036
I2= 1.46429 I3= 2.19643 I4= 1.15101
I5= .714286 I6= .902566
A1= 7.32143 A2= 5.85714 A3= 8.78571
A4= 5.75506 A5= 4.46429 A6= 3.63193
N4= .505323

K= 4 E1= 400 T1= 7.17949E-05 D= .358974
E3= 624 L2= 2.57725E-03 L1= 4.12360E-02
D1= .696429 D2= 2.78571 I1= 1.74107
I2= 1.39286 I3= 2.08929 I4= 1.05009
I5= .625000 I6= .843833
A1= 6.96429 A2= 5.57143 A3= 8.35714
A4= 5.61294 A5= 4.46429 A6= 3.40224
N4= .503245

K= 5 E1= 200 T1= 1.16667E-04 D= .583333
E3= 480 L2= 1.08889E-03 L1= 2.72222E-02
D1= .857143 D2= 4.28571 I1= 2.14286
I2= 1.71429 I3= 2.57143 I4= 1.64751
I5= 1.25000 I6= 1.07321
A1= 10.7143 A2= 8.57143 A3= 12.8571
A4= 6.96200 A5= 4.46429 A6= 5.34224
N4= .506651

K=	5	I	E1=	250	T1=	1.05660E-04		D=	.528302
E3=	530		L2=	1.39551E-03		L1=	3.48879E-02		
D1=	.757143				D2=	3.78571		I1=	1.89286
I2=	1.51429				I3=	2.27143		I4=	1.38495
I5=	1		I6=	.958173					
A1=	9.46429				A2=	7.57143		A3=	11.3571
A4=	6.54329				A5=	4.46429		A6=	4.78380
N4=	.508228								

K=	5		E1=	300	T1=	9.65517E-05		D=	.482759
E3=	580		L2=	1.67800E-03		L1=	4.19501E-02		
D1=	.690476				D2=	3.45238		I1=	1.72619
I2=	1.38095				I3=	2.07143		I4=	1.20734
I5=	.833333				I6=	.873629			
A1=	8.63095				A2=	6.90476		A3=	10.3571
A4=	6.24858				A5=	4.46429		A6=	4.37206
N4=	.508357								

K=	5		E1=	350	T1=	8.88889E-05		D=	.444444
E3=	630		L2=	1.93580E-03		L1=	4.83951E-02		
D1=	.642857				D2=	3.21429		I1=	1.60714
I2=	1.28571				I3=	1.92857		I4=	1.07855
I5=	.714286				I6=	.808122			
A1=	8.03571				A2=	6.42857		A3=	9.64286
A4=	6.02927				A5=	4.46429		A6=	4.05243
N4=	.507645								

K=	5		E1=	400	T1=	8.23529E-05		D=	.411765
E3=	680		L2=	2.17024E-03		L1=	5.42561E-02		
D1=	.607143				D2=	3.03571		I1=	1.51786
I2=	1.21429				I3=	1.82143		I4=	.980464
I5=	.625000				I6=	.755437			
A1=	7.58929				A2=	6.07143		A3=	9.10714
A4=	5.85939				A5=	4.46429		A6=	3.79508
N4=	.506434								

K=	6		E1=	200	T1=	1.25373E-04		D=	.626866
E3=	536		L2=	8.73246E-04		L1=	3.14368E-02		
D1=	.797619				D2=	4.78571		I1=	1.99405
I2=	1.59524				I3=	2.39286		I4=	1.58927
I5=	1.25000				I6=	.981475			
A1=	11.9643				A2=	9.57143		A3=	14.3571
A4=	7.35691				A5=	4.46429		A6=	5.84759
N4=	.504255								

K=	6		E1=	250	T1=	1.14676E-04		D=	.573379
E3=	586		L2=	1.14154E-03		L1=	4.10954E-02		
D1=	.697619				D2=	4.18571		I1=	1.74405
I2=	1.39524				I3=	2.09286		I4=	1.32940
I5=	1		I6=	.875958					
A1=	10.4643				A2=	8.37143		A3=	12.5571
A4=	6.88029				A5=	4.46429		A6=	5.23532
N4=	.507054								

K= 6 E1= 300 T1= 1.05660E-04 D= .528302
E3= 636 L2= 1.39551E-03 L1= 5.02385E-02
D1= .630952 D2= 3.78571 I1= 1.57738
I2= 1.26190 I3= 1.89286 I4= 1.15413
I5= .833333 I6= .798477
A1= 9.46429 A2= 7.57143 A3= 11.3571
A4= 6.54329 A5= 4.46429 A6= 4.78380
N4= .508228

K= 6 E1= 350 T1= 9.79592E-05 D= .489796
E3= 686 L2= 1.63265E-03 L1= 5.87755E-02
D1= .583333 D2= 3.50000 I1= 1.45833
I2= 1.16667 I3= 1.75000 I4= 1.02740
I5= .714286 I6= .738479
A1= 8.75000 A2= 7.00000 A3= 10.5000
A4= 6.29153 A5= 4.46429 A6= 4.43323
N4= .508406

K= 6 E1= 400 T1= 9.13043E-05 D= .456522
E3= 736 L2= 1.85255E-03 L1= 6.66919E-02
D1= .547619 D2= 3.28571 I1= 1.36905
I2= 1.09524 I3= 1.64286 I4= .931162
I5= .625000 I6= .690245
A1= 8.21429 A2= 6.57143 A3= 9.85714
A4= 6.09589 A5= 4.46429 A6= 4.15091
N4= .507951

K= 7 E1= 200 T1= 1.32432E-04 D= .662162
E3= 592 L2= 7.15851E-04 L1= 3.50767E-02
D1= .755102 D2= 5.28571 I1= 1.88776
I2= 1.51020 I3= 2.26531 I4= 1.54634
I5= 1.25000 I6= .910306
A1= 13.2143 A2= 10.5714 A3= 15.8571
A4= 7.73168 A5= 4.46429 A6= 6.31261
N4= .501515

K= 7 E1= 250 T1= 1.22118E-04 D= .610592
E3= 642 L2= 9.51078E-04 L1= 4.66028E-02
D1= .655102 D2= 4.58571 I1= 1.63776
I2= 1.31020 I3= 1.96531 I4= 1.28825
I5= 1 I6= .812153
A1= 11.4643 A2= 9.17143 A3= 13.7571
A4= 7.20154 A5= 4.46429 A6= 5.65088
N4= .505274

K= 7 E1= 300 T1= 1.13295E-04 D= .566474
E3= 692 L2= 1.17879E-03 L1= 5.77607E-02
D1= .588435 D2= 4.11905 I1= 1.47109
I2= 1.17687 I3= 1.76531 I4= 1.11456
I5= .833333 I6= .740141
A1= 10.2976 A2= 8.23810 A3= 12.3571
A4= 6.82528 A5= 4.46429 A6= 5.16281
N4= .507303

K= 7 E1= 350 T1= 1.05660E-04 D= .528302
E3= 742 L2= 1.39551E-03 L1= 6.83802E-02
D1= .540816 D2= 3.78571 I1= 1.35204
I2= 1.08163 I3= 1.62245 I4= .989252
I5= .714286 I6= .684409
A1= 9.46429 A2= 7.57143 A3= 11.3571
A4= 6.54329 A5= 4.46429 A6= 4.78380
N4= .508228

K= 7 E1= 400 T1= 9.89899E-05 D= .494949
E3= 792 L2= 1.59984E-03 L1= 7.83920E-02
D1= .505102 D2= 3.53571 I1= 1.26276
I2= 1.01020 I3= 1.51531 I4= .894285
I5= .625000 I6= .639625
A1= 8.83929 A2= 7.07143 A3= 10.6071
A4= 6.32355 A5= 4.46429 A6= 4.47855
N4= .508426

K= 8 E1= 200 T1= 1.38272E-04 D= .691358
E3= 648 L2= 5.97470E-04 L1= 3.82381E-02
D1= .723214 D2= 5.78571 I1= 1.80804
I2= 1.44643 I3= 2.16964 I4= 1.51333
I5= 1.25000 I6= .853041
A1= 14.4643 A2= 11.5714 A3= 17.3571
A4= 8.08911 A5= 4.46429 A6= 6.74565
N4= .498661

K= 8 E1= 250 T1= 1.28367E-04 D= .641834
E3= 698 L2= 8.04591E-04 L1= 5.14938E-02
D1= .623214 D2= 4.98571 I1= 1.55804
I2= 1.24643 I3= 1.86964 I4= 1.25651
I5= 1 I6= .760795
A1= 12.4643 A2= 9.97143 A3= 14.9571
A4= 7.50906 A5= 4.46429 A6= 6.03790
N4= .503184

K= 8 E1= 300 T1= 1.19786E-04 D= .598930
E3= 748 L2= 1.00889E-03 L1= 6.45692E-02
D1= .556548 D2= 4.45238 I1= 1.39137
I2= 1.11310 I3= 1.66964 I4= 1.08394
I5= .833333 I6= .693173
A1= 11.1310 A2= 8.90476 A3= 13.3571
A4= 7.09608 A5= 4.46429 A6= 5.51584
N4= .505913

K= 8 E1= 350 T1= 1.12281E-04 D= .561404
E3= 798 L2= 1.20653E-03 L1= 7.72176E-02
D1= .508929 D2= 4.07143 I1= 1.27232
I2= 1.01786 I3= 1.52679 I4= .959645
I5= .714286 I6= .640870
A1= 10.1786 A2= 8.14286 A3= 12.2143
A4= 6.78571 A5= 4.46429 A6= 5.11039
N4= .507469

K=	8	E1=	400	T1=	1.05660E-04	D=	.528302		
E3=	848	L2=	1.39551E-03	L1=	8.93129E-02				
D1=	.473214			D2=	3.78571	I1=	1.18304		
I2=	.946429			I3=	1.41964	I4=	.865596		
I5=	.625000			I6=	.598858				
A1=	9.46429			A2=	7.57143	A3=	11.3571		
A4=	6.54329			A5=	4.46429	A6=	4.78380		
N4=	.508228								

K=	9	E1=	200	T1=	1.43182E-04	D=	.715909		
E3=	704	L2=	5.06198E-04	L1=	4.10021E-02				
D1=	.698413			D2=	6.28571	I1=	1.74603		
I2=	1.39683			I3=	2.09524	I4=	1.48716		
I5=	1.25000			I6=	.805692				
A1=	15.7143			A2=	12.5714	A3=	18.8571		
A4=	8.43140			A5=	4.46429	A6=	7.15252		
N4=	.495814								

K=	9	E1=	250	T1=	1.33687E-04	D=	.668435		
E3=	754	L2=	6.89514E-04	L1=	5.58507E-02				
D1=	.598413			D2=	5.38571	I1=	1.49603		
I2=	1.19683			I3=	1.79524	I4=	1.23125		
I5=	1	I6=	.718317						
A1=	13.4643			A2=	10.7714	A3=	16.1571		
A4=	7.80448			A5=	4.46429	A6=	6.40156		
N4=	.500948								

K=	9	E1=	300	T1=	1.25373E-04	D=	.626866		
E3=	804	L2=	8.73246E-04	L1=	7.07329E-02				
D1=	.531746			D2=	4.78571	I1=	1.32937		
I2=	1.06349			I3=	1.59524	I4=	1.05952		
I5=	.833333			I6=	.654317				
A1=	11.9643			A2=	9.57143	A3=	14.3571		
A4=	7.35691			A5=	4.46429	A6=	5.84759		
N4=	.504255								

K=	9	E1=	350	T1=	1.18033E-04	D=	.590164		
E3=	854	L2=	1.05348E-03	L1=	8.53319E-02				
D1=	.484127			D2=	4.35714	I1=	1.21032		
I2=	.968254			I3=	1.45238	I4=	.935970		
I5=	.714286			I6=	.604843				
A1=	10.8929			A2=	8.71429	A3=	13.0714		
A4=	7.01977			A5=	4.46429	A6=	5.41732		
N4=	.506344								

K=	9	E1=	400	T1=	1.11504E-04	D=	.557522		
E3=	904	L2=	1.22797E-03	L1=	9.94659E-02				
D1=	.448413			D2=	4.03571	I1=	1.12103		
I2=	.896825			I3=	1.34524	I4=	.842607		
I5=	.625000			I6=	.565121				
A1=	10.0893			A2=	8.07143	A3=	12.1071		
A4=	6.75589			A5=	4.46429	A6=	5.07072		
N4=	.507588								

```
K=   10        E1=   200     T1=   1.47368E-04        D=   .736842
E3=    760     L2=   4.34349E-04       L1=   4.34349E-02
D1=   .678571                D2=   6.78571          I1=   1.69643
I2=   1.35714                I3=   2.03571          I4=   1.46588
I5=   1.25000                I6=   .765709
A1=   16.9643                A2=   13.5714          A3=   20.3571
A4=   8.76032                A5=   4.46429          A6=   7.53746
N4=   .493034

K=   10        E1=   250     T1=   1.38272E-04        D=   .691358
E3=    810     L2=   5.97470E-04       L1=   5.97470E-02
D1=   .578571                D2=   5.78571          I1=   1.44643
I2=   1.15714                I3=   1.73571          I4=   1.21067
I5=   1        I6=   .682433
A1=   14.4643                A2=   11.5714          A3=   17.3571
A4=   8.08911                A5=   4.46429          A6=   6.74565
N4=   .498661

K=   10        E1=   300     T1=   1.30233E-04        D=   .651163
E3=    860     L2=   7.63223E-04       L1=   7.63223E-02
D1=   .511905                D2=   5.11905          I1=   1.27976
I2=   1.02381                I3=   1.53571          I4=   1.03956
I5=   .833333                I6=   .621485
A1=   12.7976                A2=   10.2381          A3=   15.3571
A4=   7.60881                A5=   4.46429          A6=   6.16151
N4=   .502449

K=   10        E1=   350     T1=   1.23077E-04        D=   .615385
E3=    910     L2=   9.27811E-04       L1=   9.27811E-02
D1=   .464286                D2=   4.64286          I1=   1.16071
I2=   .928571                I3=   1.39286          I4=   .916589
I5=   .714286                I6=   .574397
A1=   11.6071                A2=   9.28571          A3=   13.9286
A4=   7.24628                A5=   4.46429          A6=   5.70777
N4=   .504990

K=   10        E1=   400     T1=   1.16667E-04        D=   .583333
E3=    960     L2=   1.08889E-03       L1=   .108889
D1=   .428571                D2=   4.28571          I1=   1.07143
I2=   .857143                I3=   1.28571          I4=   .823754
I5=   .625000                I6=   .536606
A1=   10.7143                A2=   8.57143          A3=   12.8571
A4=   6.96200                A5=   4.46429          A6=   5.34224
N4=   .506651

106 HALT
>
```

APPENDIX B

TEMPERATURE CHARACTERISTIC CALCULATIONS FOR AN ANALOG CONTROL CIRCUIT

APPENDIX B

TEMPERATURE CHARACTERISTIC CALCULATIONS FOR AN ANALOG CONTROL CIRCUIT

1. Calculations of the power transistor on time period variation for the analog control circuit design.

$$t = C \frac{V_{high} - V_{comp}}{i}$$

$$V_{high} = 10V - V_{D1} - V_{CEQ1SAT}$$

$$V_{comp} = V_{REF} + V_{osz1} + \left[\frac{V_{REF} - K_{Vs}}{\frac{(R_1)(R_2 + R_3)}{(R_1 + R_2 + R_3)}} \right] R_4 + V_{osz2}$$

$$V_{comp} = V_{REF} + V_{osz1} + V_{osz2} + \frac{(V_{REF} - KV_s)(R_1 + R_2 + R_3) R_4}{(R_1)(R_2 + R_3)}$$

$$i = \frac{V_{D2} - V_{BEQ2}}{R_5} = 0.283MA$$

$$V_{REF} = \frac{V_{D3} R_7}{R_6 + R_7} = 2.2V$$

$$K = \frac{R_2 + R_3}{R_1 + R_2 + R_3} = 0.03828$$

Plug 6 into 3

$$\frac{\partial t}{\partial c_1} = R_5 A = 11{,}588$$

$$\frac{\partial t}{\partial 10V} = \frac{C_1 R_5}{V_{D2} - V_{BEQ2}} = 3.53 \times 10^{-5}$$

$$\frac{\partial t}{\partial V_{D1}} = \frac{- C_1 R_5}{V_{D2} - V_{BEQ2}} = 3.53 \times 10^{-5}$$

$$\frac{\partial t}{\partial V_{CEQ1SAT}} = \frac{C_1 R_5}{V_{D2} - V_{BEQ2}} = 3.53 \times 10^{-5}$$

$$\frac{\partial t}{\partial V_{D3}} = \frac{- C_1 R_5 R_7}{\left(V_{D2} - V_{BEQ2}\right)\left(R_6 + R_7\right)} \left[+ 1 + \frac{\left(R_1 + R_2 + R_3\right) R_4}{\left(R_1\right)\left(R_2 + R_3\right)}\right] = 4.265 \times 10^{-4}$$

$$\frac{\partial t}{\partial V_{osz1}} = \frac{C_1 R_5}{V_{D2} - V_{BEQ2}} = 3.53 \times 10^{-5}$$

$$\frac{\partial t}{\partial V_{osz2}} = \frac{C_1 R_5}{V_{D2} - V_{BEQ2}} = 3.53 \times 10^{-5}$$

$$\frac{\partial t}{\partial V_{D2}} = \frac{C_1 R_5 A \left(V_{D2} - V_{BEQ2}\right)}{\left(V_{D2} - V_{BEQ2}\right)^2} = 2.27 \times 10^{-5}$$

$$\frac{\partial t}{\partial V_{BEQ2}} = \frac{C_1 R_5 A \left(V_{D2} - V_{BEQ2}\right)}{\left(V_{D2} - V_{BEQ2}\right)^2} = 2.27 \times 10^{-5}$$

Take the total derivative

$$dt = \frac{\partial t}{\partial c_1} dc_1 + \frac{\partial t}{\partial .10V} d10V + \frac{\partial t}{\partial V_{D1}} + \frac{\partial t}{\partial V_{CEQ1SAT}} dV_{CEQ1SAT} + \frac{\partial t}{\partial V_{D3}} d_{VD3}$$

$$+ \frac{\partial t}{\partial V_{osz1}} d_{Vosz1} + \frac{\partial t}{\partial V_{osz2}} d_{Vosz2} + \frac{\partial t}{\partial V_{D2}} dVD2 + \frac{\partial t}{\partial V_{BEQ2}} dVBEQ2$$

$$dt = (11{,}588)\ (1 \times 10^{-9})\ dc_1 + 3.53 \times 10^{-5})\ (1)\ d10V + (3.53 \times 10^{-5})\ (0.24)\ dVD1$$

$$+ (3.53 \times 10^{-5})\ (0.025)\ dVCEQ1SAT + (4.265 \times 10^{-4})\ (0.352)\ dVD3 + (3.53 \times 10^{-5})\ (2.5 \times 10^{-4})\ dVosz1$$

$$+ (3.53 \times 10^{-5})\ (2.54 \times 10^{-4})\ dVosz2 + 2.27 \times 10^{-5})\ (0.56)\ dVD2 + (2.27 \times 10^{-5})\ (0.1)\ dVBEQ2$$

$$dt = (1.158 \times 10^{-5})\ dc_1 + (3.53 \times 10^{-5}\ d10V + (8.472 \times 10^{-6})\ dVD1 + (8.825 \times 10^{-7})\ dVCEQ1SAT$$

$$+ (1.50 \times 10^{-4})\ dVD3 + (8.9662 \times 10^{-9})\ dVosz1 + (8.9662 \times 10^{-9})\ dVosz2 + (1.2712 \times 10^{-5})\ dVD2$$

$$+ (2.27 \times 10^{-6})\ dVBEQ2$$

Do not vary d10V, dVD3, dVosz1 because they will be common to all multiple circuits.

$$dt = 3.5933 \times 10^{-5}$$

$$\frac{3.5933 \times 10^{-5}}{0.11588 \times 10^{-3}} = \frac{x}{100\%}$$

$$x = \pm 31\% \text{ error}$$

$$V_{comp} = V_{REF} + V_{osz1} + V_{osz2} + \frac{\left[V_{REF} - \frac{\left(R_2 + R_3\right) V_s}{\left(R_1 + R_2 + R_3\right)}\right]\left[R_1 + R_2 + R_3\right] R_4}{\left(R_1\right)\left(R_2 + R_3\right)}$$

$$V_{comp} = V_{REF} + V_{osz1} + V_{osz2} + \frac{V_{REF}\left(R_1 + R_2 + R_3\right) R_4}{\left(R_1\right)\left(R_2 + R_3\right)} - \frac{R_4 V_s}{R_1}$$

$$V_{comp} = V_{REF}\left[1 + \frac{\left(R_1 + R_2 + R_3\right)}{\left(R_1\right)\left(R_2 + R_3\right)} R_4\right] + V_{osz1} + V_{osz2} - \frac{R_4}{R_1} V_s$$

Plug 5 into 7

$$t = C_1 \left\{ \frac{10V - V_{D1} - V_{CEQ1SAT} - \frac{V_{D3} R_7}{R_6 + R_7}\left[1 + \frac{\left(R_1 + R_2 + R_3\right) R_4}{\left(R_1 \quad R_2 + R_3\right)}\right] - V_{osz1} - V_{osz2} + \frac{R_4}{R_1} V_s}{\frac{V_{D2} - V_{BEQ2}}{R_5}} \right\}$$

$$T = C_1 R_5 \left\{ \frac{\left(10V - V_{D1} - V_{CEQ1SAT}\right) - \frac{V_{D3} R_7}{R_6 + R_7}\left[1 + \frac{\left(R_1 + R_2 + R_3\right) R_4}{\left(R_1 \quad R_2 + R_3\right)}\right] - V_{osz1} - V_{osz2} + \frac{R_4}{R_1} V_s}{V_{D2} - V_{BEQ2}} \right\} = A$$

The above is the general transfer equation for the JPL analog control circuit. Let this general equation = A.

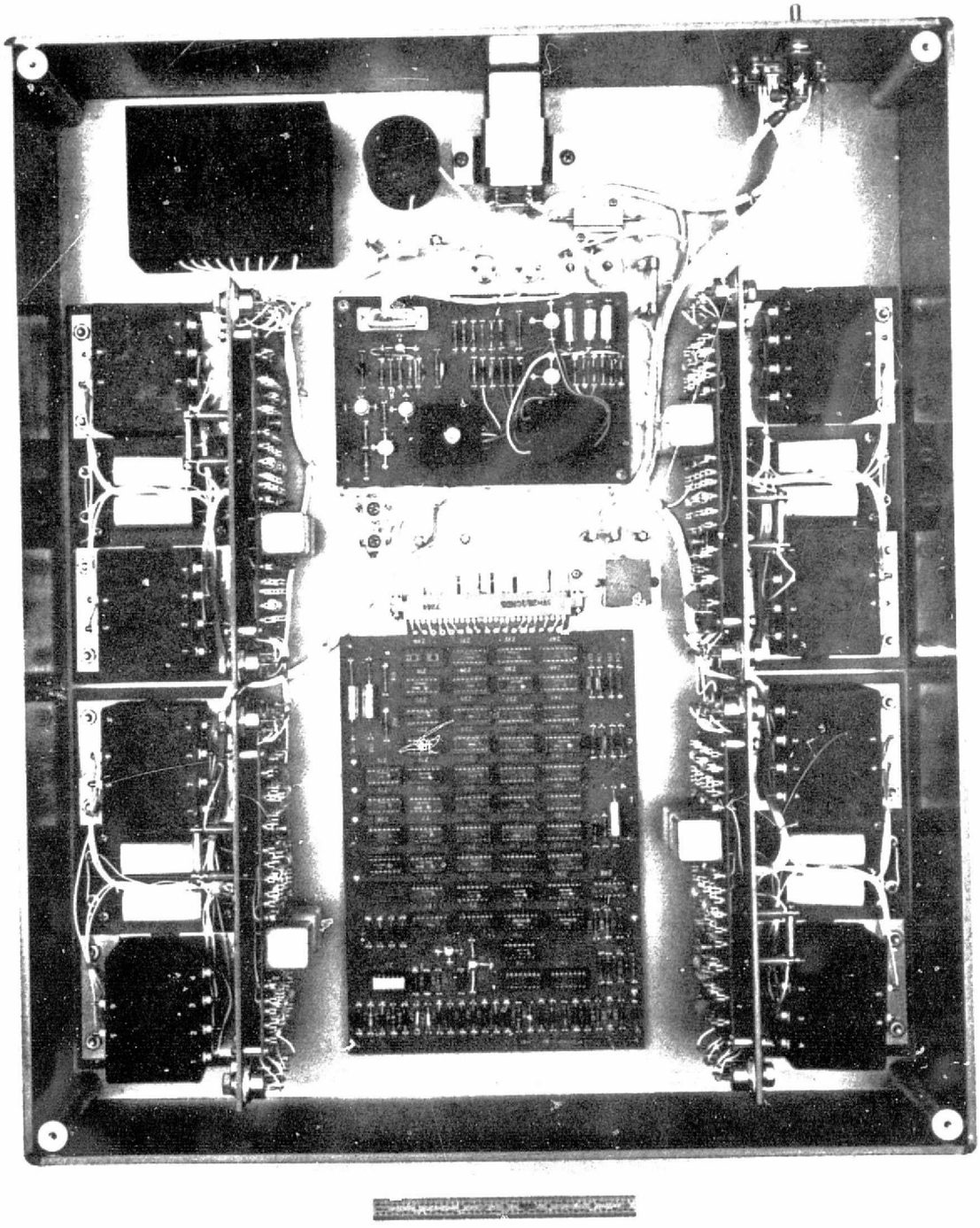
Find (assume resistors are perfect) $A = 0.64379$ $t_{nominal} = 0.11588$ MS

Over a $50^{\circ}C$ range

10V	=	10		d(10V)	=	1	
VD1	=	2.4	1N4370	d(DV1)	=	5% + 5%	= 0.24
VD2	=	5.6	1N752A	d(VD2)	=	5% + 5%	= 0.56
VD3	=	6.4	1N4570	d(VD2)	=	5% + 5%	= 0.352
VCEQ1SAT	=	0.2	2N2907	dVCEQ1SAT	=	0.5 mV/$^{\circ}C$	= 0.025
Vosz1	=	1 MV	1M108	dV(Osz1)	=	5 $\mu V/^{\circ}C$	= 2.54×10^{-4}
Vosz2	=	4MV	LM111	dV(osz2)	=	5 $\mu V/^{\circ}C$	= 2.54×10^{-4}
C_1	=	0.01 μf		dC_1	=	5% + 5%	= 1×10^{-9}
R_1	=	52K					
R_2	=	1.82K					
R_3	=	250Ω					
R_4	=	68K					
R_5	=	18K					
R_6	=	4.22K					
R_7	=	2.21K					
VBEQ2	=	0.5V	2N2222	dVBEQ2	=	2mV/$^{\circ}C$	= 0.1

APPENDIX C

PHOTOGRAPH OF UNIT



77463

8-Stage Inductive Energy Transfer Circuit Breadboard

APPENDIX D

REGULATED ENERGY TRANSFER BY INDUCTOR-TRANSFORMERS WITH SINGLE AND MULTIPLE STAGES

Reprinted from 24th ANNUAL PROCEEDINGS POWER SOURCES SYMPOSIUM — May 19, 20, 21, 1970

Session on Power Processing

REGULATED ENERGY TRANSFER BY INDUCTOR-TRANSFORMERS WITH SINGLE AND MULTIPLE STAGES

Dr. S. J. Lindena
Electro-Optical Systems

The application of energy-transfer and regulation techniques with inductor-transformer has been increasing in DC-to-DC conversion systems.

In most cases pulsewidth-modulation in combination with square-wave inverters have been used. In recent times, however, more and more use has been made of an inductive energy transfer system, which has some inherent advantages not present in other approaches.

Figure 1 shows the simplified circuit diagram. Transistor Q operates as a switch. Inductor-transformer T is an inductor with closely coupled primary and secondary windings and is connected with the polarities as shown by dots. The primary inductance L of transformer T is constant and capacitor C is large enough to make the ripple voltage across the load resistor negligible.

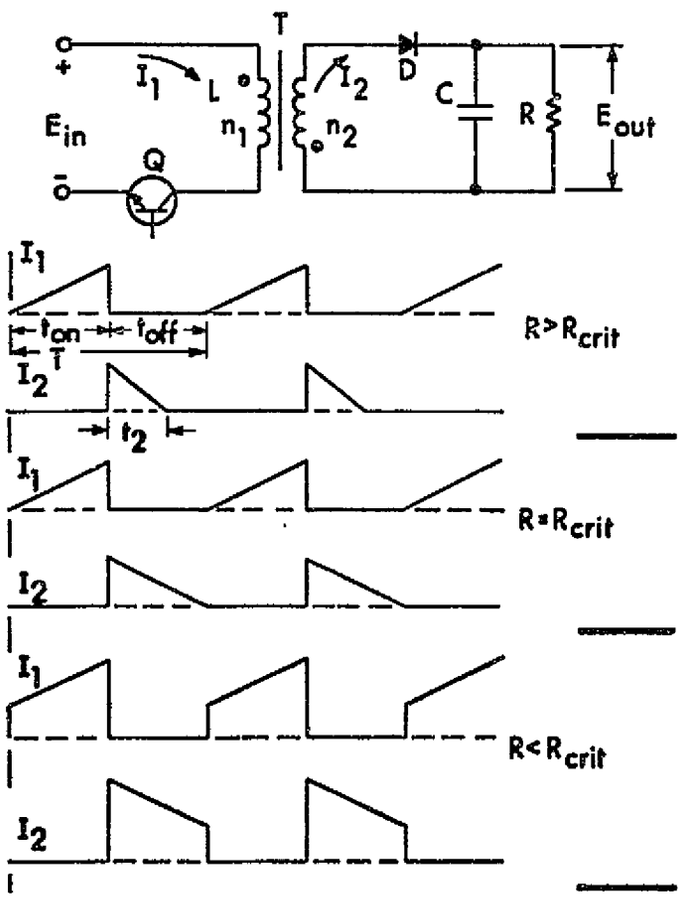


Figure 1. Different Current Waveshapes in One Stage

During the conduction time t_{on} of transistor Q, the current I, through the primary increases linearly to a peak value of I_p. During this time, diode D blocks conduction of the secondary winding and decouples it from the input voltage. At the end of t_{on}, the primary-current is turned off, and the secondary winding begins to conduct with the same ampere-turns. During the conduction time t_2 of the secondary, its current decreases linearly. The conduction time of the secondary winding t_2 can be less than or equal to t_{off}, the off time of the primary (see top two traces in Figure 1). Depending on the conduction time of the secondary, we can define two distinct operating modes which are sharply divided by a certain load resistor $R = R_{crit}$. The unit can either operate with triangular or with trapezoidal current-waveshapes. The following assumptions make it easier to understand these two operating modes:

E_{in} = constant
t_{on} = constant
t_{off} and hence T = constant

The Operating Modes with Triangular and Trapezoidal Current-Waveshapes.

The input power is constant when operating with triangular current-waveshapes and under the previous assumptions. The input energy is stored during the conduction time t_{on} and is:

$$J_1 = \frac{1}{2} \frac{(E_{in}\ t_{on})^2}{L} \qquad (1)$$

Under the assumption of no losses, the input energy is transferred during the conduction time of the secondary t_2 to the load resistor R. The output voltage E_{out} will adjust itself such that the stored energy J_1 is the same as the energy J_2 dissipated in load resistor R. The energy dissipated in R in one cycle is:

$$J_2 = \frac{(E_{out})^2}{R} T \qquad (2)$$

Combining these two equations yields the equation for the output voltage valid with triangular current waveshapes only.

$$E_{out} = E_{in}\ t_{on} \sqrt{\frac{R}{2LT}} \qquad (3)$$

A triangular current-waveshape is assured only when the energy transfer time t_2 (= conduction time of secondary winding) is less than the available time t_{off}. The conduction time of the secondary t_2 is governed by the requirement that the impressed volt-seconds into the core are equal to the resetting volt-seconds:

$$t_2 = \frac{E_{in}\, t_{on}}{E_{out}} \frac{n_2}{n_1} < t_{off} \qquad (4)$$

Valid for triangular current-waveshapes.

Equation (3) shows that the output voltage is a function of the load resistor R. Therefore, at a certain value of $R = R_{crit}$, the conduction time will become equal to t_{off}. This resistance value is:

$$R_{crit} = \frac{2LT}{t^2_{off}} \left(\frac{n_2}{n_1}\right)^2 \qquad (5)$$

This value of the load resistor R_{crit} establishes the dividing line between triangular and trapezoidal current-waveshapes. Traces 3 and 4 in Figure 1 show the associated current-waveshapes.

From the preceding information, we know that, at a load resistance value of less than R_{crit}, the conduction time t_2 of the secondary becomes equal to t_{off}. If the magnetic flux in the core is to reset properly, then the output voltage with trapezoidal current-waveshapes must be

$$E_{out} = \frac{E_{in}\, t_{on}}{t_{off}} \frac{n_2}{n_1} \qquad (6)$$

and becomes independent of R.

With a decreasing load resistor and constant input voltage E_{in} and constant t_{on}, the output voltage can be constant only if input and output currents increase. The resulting current-waveshape is trapezoidal as shown in traces 5 and 6 in Figure 1.

With the help of equations (3) and (6), we can now construct the theoretical curve of output voltage as a function of varying load resistor R as shown in the upper trace of Figure 2.

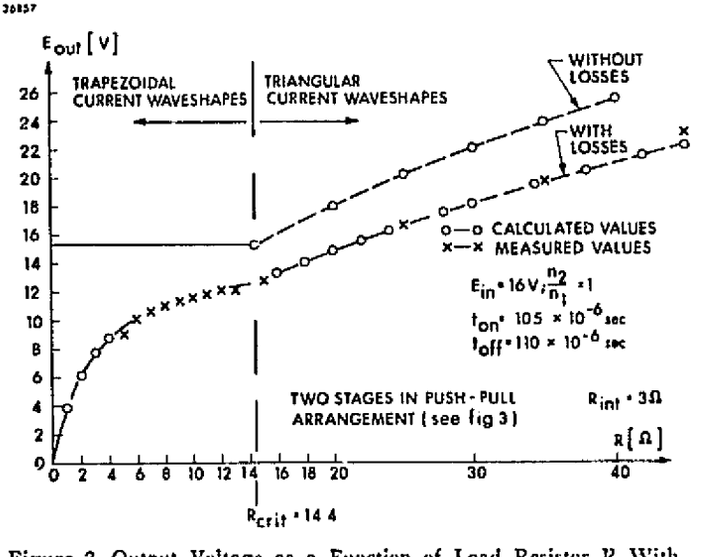


Figure 2. Output Voltage as a Function of Load Resistor R With and Without Losses

The bottom trace shows measured and calculated data. The circuit arrangement, built and tested as a model, used two stages operating alternately and thus reduced input current and output ripple considerably.

The difference in the two curves is caused by losses and is most pronounced toward the low end of load resistor R. The two main loss sources are primary and secondary winding resistance. In Figure 3 they are lumped under the combined loss resistor R_{int}, which is assumed to be inside the filtering effect of capacitor C. This loss resistor, which causes the main losses attenuates the theoretical output voltage by a factor of $\frac{R}{R + R_{int}}$. The theoretical output voltage for two stages operating alternately with triangular current-waveshapes is:

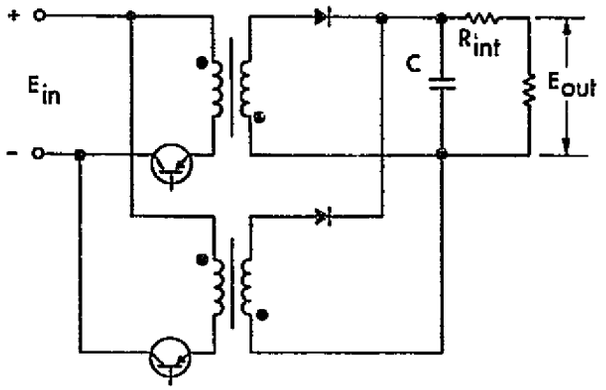


Figure 3. Two-Stage Circuit with Lumped Losses

$$E_{out} = E_{in}\, t_{on} \sqrt{\frac{R}{LT}} \quad ; \; R \geq R_{crit} \qquad (7)$$

For values of $R \geqq R_{crit}$ equation (6) remains valid, The critical resistance, however, becomes:

$$R_{crit} = \frac{LT}{t^2_{off}} \left(\frac{n_2}{n_1}\right)^2 \; ; \text{two stages} \qquad (8)$$

The calculated and measured values in Figure 3 show little difference, and verify the calculations.

Design Considerations

The use of trapezoidal current-waveshapes and two stages operating alternately allows us not only to considerably reduce the peak current and the RMS current as compared to the average current, it also allows us to generate an uninterrupted current flow into the load even when pulsewidth modulation is used for regulation purposes. Filter requirements are also reduced on both input and output.

Let us now consider the impact of the trapezoidal current-waveshape on the design of the inductor-transformer in one stage. The input voltage is constant and $t_{on} = t_{off}$ (see Figure 4).

With constant energy per pulse J, we can describe the input current-waveshape as:

$$I_{low} + \frac{\Delta I}{2} = \frac{J}{E_{in}\, t_{on}} \qquad (9)$$

The value of $I_{low} + \Delta I/2$ represents a medium current value I_m during the time of t_{on}. If I_{low} becomes equal to zero, we arrive at a triangular current-waveshape which dictates a minimum inductance L_{min} which is capable of

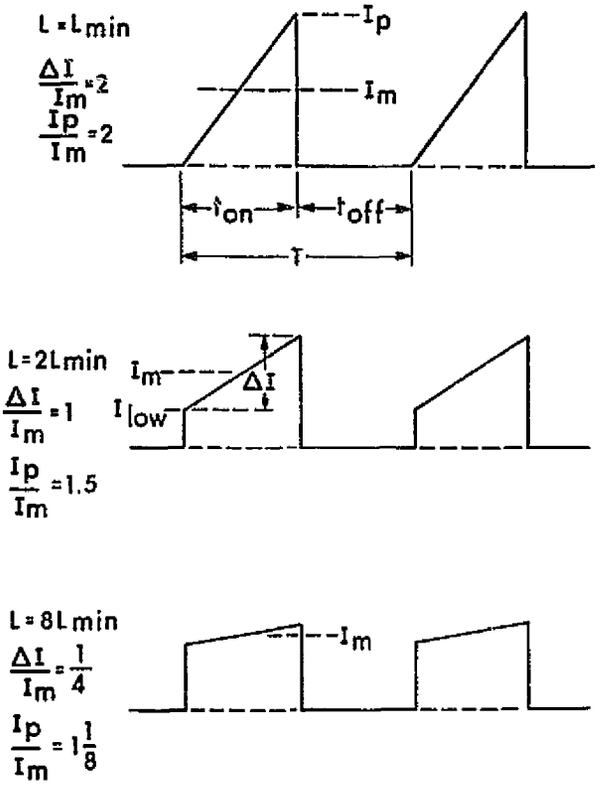


Figure 4. Different Input Current Waveshapes at Constant Input Voltage and Constant Power

transferring the same energy. One can also select ΔI small and I_{low} high and arrive at trapezoidal input and output Current waveshapes. Figure 4 shows a series of different input current-waveshapes at constant power level. Average current I_{av} and medium input pulse current I_m, therefore, are the same in all cases. Peak current I_p, RMS current i_{RMS} and L, however, are varying as functions of the waveshape.

The RMS value of the input current determines the wire size and can be computed as follows:

$$i_{RMS} = \sqrt{\frac{1}{T}\int_0^T i^2 dt} \qquad (10)$$

$$i_{RMS} = \sqrt{\frac{I_{low}^2 + I_{low}\Delta I + \frac{\Delta I^2}{3}}{2}}$$

Figure 5 shows the relations between flux densities and primary currents. It can be seen that a selected maximum value of flux density corresponds to I_p and ΔI corresponds

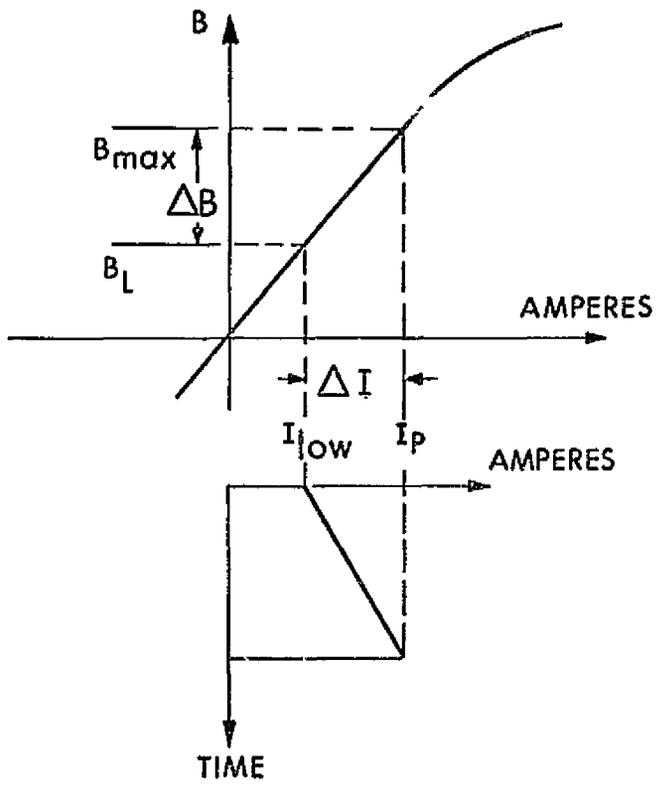


Figure 5. Relation Between Flux Densities and Primary Currents

to ΔB. If one now selects the value of edt equal to $E_{low} \times t_{on}$, then this corresponds to L ΔI and also to ΔB. Therefore, the total Vsec the core can absorb corresponds to LI_p and also to B_{max}. Therefore,

$$\int edt_{total} = k\, LI_p$$

The product of i_{RMS} times edt_{total} is, of course, the same as the more commonly known VA rating of a magnetic component as edt can also be written as e/2f, and the product of i_{RMS} edt converts into $i_{RMS}e/2f$.

The product of i_{RMS} times edt_{total} is directly proportional to the power handling capability of any magnetic component provided core configuration, max flux-density, circ-mils per ampere of wire size, winding factor and temperature rise are the same.

Listed as a relative value $\frac{\int edt_{total} \times i_{RMS}}{I_m^2 L_{min}}$ as a function of $\Delta I/I_m$ gives us an insight as to how the power handling capability or the VA rating of the inductor increases with decreasing $\Delta I/I_m$.

Table 1 lists the important parameters at a constant average pulse current I_m and hence constant power. (Consult Figure 4 for proper understanding of parameters.)

TABLE I
VA-RATING, RMS-CURRENT, INDUCTANCE AND PEAK SWITCHING CURRENT AS FUNCTION OF THE RATIO $\Delta I/I_m$

	CONSTANT AT I_m					
	CONSTANT AT I_{av}					
ΔI	$2I_m$	$1\frac{1}{2}I_m$	$1I_m$	$\frac{1}{2}I_m$	$\frac{1}{4}I_m$	$\frac{3}{16}I_m$
L	$1\,L_{min}$	$\frac{4}{3}L_{min}$	$2\,L_{min}$	$4\,L_{min}$	$8\,L_{min}$	$\frac{32}{3}L_{min}$
I_{low}	0	$\frac{1}{4}I_m$	$\frac{1}{2}I_m$	$\frac{3}{4}I_m$	$\frac{7}{8}I_m$	$\frac{15}{16}I_m$
I_p	$2I_m$	$1\frac{3}{4}I_m$	$1\frac{1}{2}I_m$	$1\frac{1}{4}I_m$	$1\frac{1}{8}I_m$	$1\frac{3}{32}I_m$
$\Delta I/I_m$	2	$1\frac{1}{2}$	1	$\frac{1}{2}$	$\frac{1}{4}$	$\frac{3}{16}$
I_p/I_m	2	$1\frac{3}{4}$	$1\frac{1}{2}$	$1\frac{1}{4}$	$1\frac{1}{8}$	$1\frac{3}{32}$
$L\,I_p\Delta\left/\int edt_{total}\right.$	$2L_{min}I_m$	$2\frac{1}{3}L_{min}I_m$	$2L_{min}I_m$	$2L_{min}I_m$	$2L_{min}I_m$	$2\frac{1}{3}L_{min}I_m$
i_{RMS}	$\sqrt{2/3}\,I_m$	$\sqrt{37/96}\,I_m$	$\sqrt{13/24}\,I_m$	$\sqrt{49/96}\,I_m$	$\sqrt{193/384}\,I_m$	$\sqrt{3081/6144}\,I_m$
i_{RMS}	$0.8165\,I_m$	$0.7708\,I_m$	$0.736\,I_m$	$0.7145\,I_m$	$0.7086\,I_m$	$0.7081\,I_m$
$(edt)_{total} \times i_{RMS}$	$1.633\,I_m^2 L_{min}$	$1.798\,I_m^2 L_{min}$	$2.208\,I_m^2 L_{min}$	$2.573\,I_m^2 L_{min}$	$2.837\,I_m^2 L_{min}$	$2.961\,I_m^2 L_{min}$

Figure 6 plots the relative values of required VA rating

$$\frac{(edt)_{total} \times i_{RMS}}{I_m^2 L_{min}},$$

$$\frac{10\, i_{RMS}}{I_m}, \frac{L}{L_{min}}, \text{ and } \frac{I_p}{I_m} \text{ as function of } \frac{\Delta I}{I_m}.$$

It can be shown that the product of i_{RMS} edt is related to window area W, core cross section A, flux swing ΔB and circ-mils/A of the inductor-transformer as shown:

$$i_{RMS}\,edt = \frac{WA\ k\ \Delta B}{\text{circ mils/A}} \qquad (11)$$

It is for this relation that the product of i_{RMS} edt also gives us an insight into size and volume of the inductor-transformer.

One can see in Figure 6 that at values below $\Delta I/I_m = \frac{1}{2}$, the VA rating and the ratio of L/L_{min} increase very rapidly whereas RMS current and peak current have almost reached their minimum values and allow for only little further improvement.

For economical reasons, one would, therefore, seldom design for values of $\Delta I/I_m$ below $\frac{1}{2}$.

There is one more reason for selecting this particular design value: with pulsewidth-modulation, t_{off} can approach the value of T as t_{on} becomes very small. If one now wants to maintain an uninterrupted current flow on the secondary and operate below the same R_{crit}, then L must become equal to 4 L_{min} as indicated by equation (8).

Single and Multiple Stage Operation

The power one stage can transfer is given by

$$P = \frac{1}{2} L \left(I_p^2 - I_{low}^2 \right) f \qquad (12)$$

It is limited by the switch capabilities (switching current and losses) and the inherent characteristic of an inductor with primary and secondary windings. In general, one will try to raise the frequency in order to reduce the size of the inductor-transformer. At a given maximum switching current, a frequency increase reduces the inductance L. If however, we keep the ratio of window area to core cross-section area to about constant, then the number of turns on the inductor decreases. Ultimately, we would have very few turns of heavy wire. The number of turns per unity of magnetic path length in combination with the permeability of the core, however, affects the coupling between primary and secondary windings.

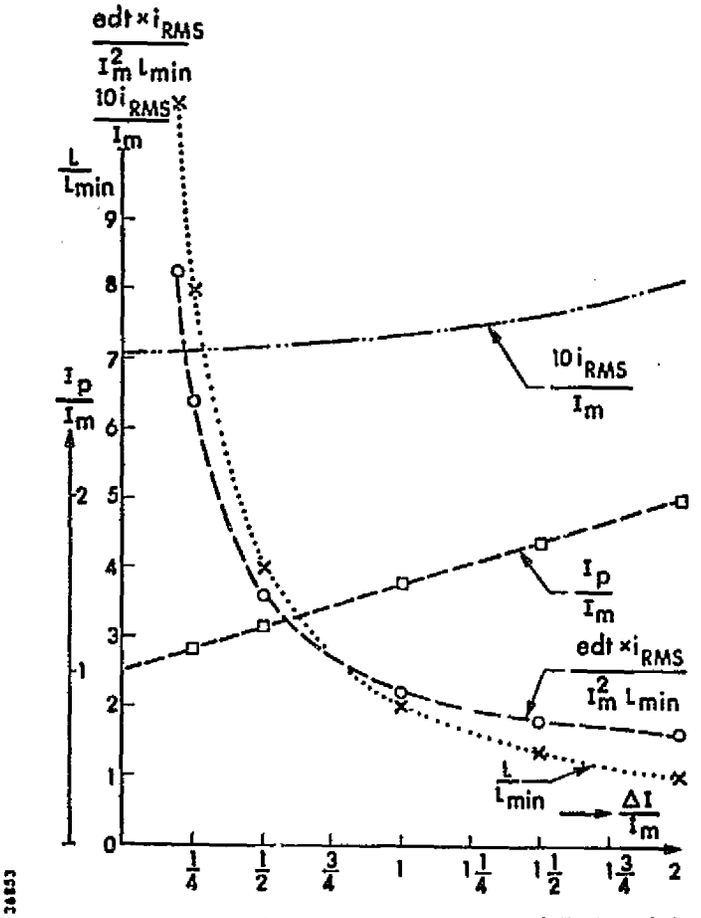


Figure 6. VA-Rating, RMS-Current, Inductance and Peak Switching Current as Function of the Ratio $\Delta I/I_m$

Good coupling and low leakage inductance is of extreme importance in the design of an inductor-transformer where the secondary has to abruptly take over the current from the primary. Experience has shown that with powder-core toroids and at high switching currents (50 amperes) it is difficult to obtain satisfactory coupling below

$$50 \frac{\text{turns}}{\text{cm}} \times \text{relative permeability.}$$

This then necessitates, at higher power levels and higher frequency, the use of multiple cores or stages connected to operate in parallel or in series whenever high power is required.

It is well known that one core of a given VA rating is smaller in size and weight than, for instance, 5 magnetic components with the same total sum of VA as before.

The triangular waveshape with its lower inductance, fewer turns and poorer coupling will force us into the use of multiple cores sooner than a unit designed for trapezoidal current-waveshapes with their higher inductance, more turns and better coupling.

We therefore will need less cores or stages in parallel when we operate with the trapezoidal current waveshape than when operating with the triangular current waveshape in order to achieve in both cases equally good coupling.

This fact then cancels the weight disadvantage of operating with the trapezoidal current-waveshapes which appeared in Figure 6.

A further advantage is of course that the trapezoidal current-waveshape requires less input and output filtering.

In a company sponsored R&D program we have built several small stages of 20 watts each and operated them successfully in series- and parallel-connections. All stages were controlled by one loop only and no extra circuitry was necessary to achieve equal power sharing.

This last characteristic of this type of circuit enhances the application of Self Test And Replace techniques and improves redundancy.

Conclusions

It can be stated that the inductive energy transfer system by means of inductor transformers and operating with trapezoidal current-waveshapes has the following advantages:

a. Higher efficiency.
b. Smaller input and output filters.
c. Ease of paralleling or seriesing several stages.
d. One loop can control all stages.
e. In higher power applications, where the use of more cores or stages is necessary, the use of the trapezoidal current waveshape will result in lower weight.