EFFECTS OF IONIZING RADIATION ON CCDs*

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The use of CCD sensors for satellite and deep space probes appears very attractive from the standpoints of size, weight, power, and reliability. One of the factors affecting CCD sensor reliability is the naturally occurring radiation levels encountered in such environments. This paper reports the preliminary results of tests of the effects of 1.2-MeV gamma radiation (Co^{60} source) and 20-MeV electrons (Linac source) on the operational characteristics of CCDs.

The effects of ionizing radiation on the charge transfer efficiency, dark current, and input/output circuitry are described. The improved radiation hardness of buried-channel CCDs is compared to surface-channel results. Both ion-implanted and epitaxial layer buried-channel device results are included. The advantages of using a single-thickness SiO_2 gate dielectric are described. The threshold voltage shifts and surface state density changes of dry, steam, and HCl doped oxides are discussed. Recent results on the recovery times and total dose effects of high-dose-rate pulses of 20-MeV electrons are reported.

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I. DESCRIPTION OF TEST DEVICES

All of the CCDs tested have been 4 ϕ double-level aluminum metal n-channel devices having SiO_2 gate oxide and anodized aluminum interlevel metal insulation. These devices have a coplanar overlapping gate structure and a single-thickness uniform gate oxide layer, which is desirable for radiation hardness because the effects of oxide charge buildup are the same under all gates. Although these devices were 4 ϕ type, they had the same gate metal and oxide structure as is being used in the 3 ϕ double-level anodized aluminum imagers developed at Texas Instruments (Ref. 1).

The test chip design used for the test samples contains the following devices: (1) two 150-bit 4 ϕ linear CCD shift registers, one having a precharged diffusion plus source follower output and one having a simple diode output, (2) a MOSFET test transistor with W/L = 10, (3) an MOS gate oxide capacitor, and (4) an MOS gated diode. All of these can be ion-implanted or fabricated on epitaxial material to form buried-channel type devices.

Two groups of test samples have been fabricated for the two series of tests made to date. The first of these included both surface and buried-channel devices, oxide process variations of 950° C steam, 1100° dry, and 1100° HCl-grown oxides. The metallization was e-beam evaporated. Buried-channel devices of both the ion-implanted and epitaxial layer type were included. The second group was mostly buried-channel type, with either 950° C steam or 1000° dry oxide. Diffused chrome doping of the oxide was done on some of the devices. Metallization variations were e-beam evaporated and thermally evaporated metal. PSG gate oxide passivation and a nitride overcoat were used on all devices tested.

II. DESCRIPTION OF RADIATION TESTS

Total dose gamma radiation tests were made using the Co^{60} radiation sources ($\approx$1.2-MeV photons) at Sandia Labs in Albuquerque and at the Nuclear Effects Laboratory, White Sands Missile Range. Dose levels ranged from 10^5 rad to 10^7 rad. In each of the two series of tests made, the test samples were connected in parallel and biased to simulate normal operating conditions in the CCD so that several samples could be irradiated at the same time. This was necessary because a large number of test samples was required due to the number of different process variations that were tested. All the CCD and test

device n-diffusions were reverse biased to +24 volts, and the gates were pulsed with a 50% duty cycle between 0 and +8, +12, or +15 volts.

The dose rate effects tests were made using the Linac source at the Nuclear Weapons Laboratory in the pulsed electron beam mode. The pulse width was 100 ns and electron energy was set at 20 MeV. The CCDs were tested for recovery time after pulses at dose rates of 10^8, 10^9, 10^{10} and 4×10^{10} rad/sec. To measure the recovery time, it was necessary to be able to operate the CCD with normal bias and clock levels and remotely monitor the output during irradiation in the source chamber. A special test set was made to permit driving the CCD clocks through more than 50 feet of cable and monitoring the output at clock rates of up to 10 MHz. This test equipment was also used for the Linac total dose test and was found to be very advantageous for total dose tests in that data can be easily obtained at several dose levels for the same device. This eliminates device-to-device variations when comparing effects at different dose levels.

III. EXPERIMENTAL RESULTS OF THE TOTAL DOSE GAMMA TESTS

Both surface- and buried-channel devices have been tested; the results obtained for the two types were very different. For surface-channel devices, the results can be summarized as follows:

(1) At levels of 10^5 rad or above, the charge transfer efficiency (CTE) was so degraded as to make the device useless.

(2) Relatively low dc threshold shifts occurred in the MOSFETs.

(3) Large increases in CCD leakage current occurred.

(4) The CV curves of the MOS capacitors exhibited large negative shifts at high frequency.

The surface-channel CCDs had pre-irradiation charge transfer efficiencies of 0.9991 to 0.9995 which decreased so much as to become unmeasurable after irradiation. The 1.0-MHz CV curve shift for the test capacitors ranged from 11 volts to over 60 volts after 10^6 rad, depending on the oxide growth process. The CV shifts were very frequency-dependent, as shown in Figure 1. GV measurements indicated surface state trap densities of over 10^{12} per eV-cm^2. This explains the large CTE degradation seen in these devices. However, as shown in Figure 2, there was little shift in the MOSFET dc threshold voltage (except

for the HCℓ-grown oxide), implying very little increase in the fixed surface charge. The HCℓ-grown oxides were much worse than either the steam or dry oxides in regard to surface state and fixed charge buildup. CCD leakage current was initially 100-200 nA/cm^2 and typically increased by a factor of 50 after irradiation. Leakage in the sub-threshold region for the MOSFETs also increased appreciably.

The test results for buried-channel CCDs can be summarized as follows:

(1) While considerable variation has been seen, changes in charge transfer inefficiency (CTI) of $<5 \times 10^{-5}$ have been found in several samples after exposures of 10^6 rad. The variation of CTI frequency is not measurably changed after irradiation.

(2) The full-well capacity is not significantly changed.

(3) Large increases in both fixed charge and surface state trapping effects after irradiation have been seen for devices heavily ion-implanted through the gate oxide.

(4) The surface charge buildup causes input and output threshold voltage shifts.

(5) The surface trapping states have little effect on operation of the buried-channel CCD but may cause significant G_m loss in the MOSFETs in the output circuit.

A plot of the increase in CTI versus dose (Figure 3) shows wide variations, but some samples had increases of 5×10^{-5} or less even after 10^6 rad. Both pre- and post-irradiation measurements were made without externally introduced fat zero. The cause of the CTI increase has not been determined. However, the large fixed charge buildup at the interface may have moved the channel nearer the surface so that the surface state traps affected the charge transfer.

In some devices, breakdown between the channel and the p+ channel stop diffusion occurs after irradiation and results in a large increase in dark current. This breakdown is attributed to the increased channel potential resulting from the fixed charge buildup and can be eliminated by increasing the substrate bias which reduces the potential between the channel and channel stop.

The increase in fixed oxide charge and interface trapping states was determined by pulsed turn-off measurements made on the buried-channel MOSFETs. If the gates of these depletion mode MOSFETs are pulsed from near 0 volts with a negative pulse V_T (pulse) just large enough to overcome the potential due to the fixed charge layer, the source-drain current will be momentarily cut off but will then again start to flow if there were a significant number of filled trapping states which can empty electrons into the channel. This effect is seen in the current waveforms of Figure 4. The size of the negative gate pulse must be increased by an amount $\Delta V_T(ss)$ in order to keep the channel turned off after the traps empty and the total number of surface state traps involved is equal to $\Delta V_T(ss) \cdot C_{ox}/q$, where ΔV_T (pulse) is the change in pulsed threshold after exposure. From these measurements, the increase in fixed charge after 10^6 rad for the ion-implanted BC MOSFETs was found to be 3 to 4 $\times 10^{12}/cm^2$ for both wet and dry grown oxide. The total number of surface state traps ranged from about 1 to 5 $\times 10^{12}/cm^2$.

No correlation was found between the different types of oxide and the increase in fixed charge or surface states for the implanted buried-channel devices tested. Of course, the resulting threshold voltage shift is inversely proportional to the oxide capacitance, and therefore a strong correlation is seen between threshold shifts and oxide thickness. The reason for the much larger buildup of fixed charge in the implanted buried-channel devices has not been fully determined but may be due to the ion implant through the gate oxide. Much smaller fixed charge increases were seen in the epitaxial buried-layer devices, but this may be due to other factors. The input threshold voltage changes seen on buried-channel CCDs is less than the threshold voltage changes of the MOSFETs even though both were biased the same during irradiation.

Noise measurements were made before and after irradiation using a low-noise input technique (Ref. 2) and a correlated double-sampling scheme (Ref. 3) to reduce the noise on the output node. Before irradiation, the noise ranged from 100-300 electrons, and the dominant source was the output source follower. After exposure, the noise increased by an amount equivalent to the shot noise on the increased leakage current.

IV. RESULTS OF THE PULSE RECOVERY TESTS

Waveforms of the CCD output during and after a 100-ns wide, 10^{10}-rad/sec pulse of 20-MeV electrons are shown in Figure 5. Recovery to normal operating levels at the CCD output occurred in from 240 to 310 μs for dose rates of from 10^8 to 4×10^{10} rad/sec and a clock rate of 1 MHz. This recovery time can be divided into two parts. During the first, which starts with the radiation pulse and lasts 50 to 100 μs, the CCD output diode is discharged to near substrate potential due to the large amount of radiation-generated charge present. After this charge is removed by the output drain diffusions of the reset and source follower MOSFETs, normal output circuit levels are reestablished and the excess charge remaining in the CCD channel is clocked out in a period of about 200 μs. For the 4×10^{10} rad/sec level pulses, an increased output leakage was seen, which decayed with a time constant of approximately 1.0 ms. This is thought to be due to the thermal time constant for removal of heat generated by the large photocurrents which flow in the output circuit.

V. LINAC TOTAL DOSE TESTS

Total dose effects tests were made using 100-ns wide, 20-MeV electron pulses of about 80 rad per pulse and 10 pulses per second. The source was turned off and data taken at levels of 0, 5×10^4, 10^5, 3×10^5, and 10^6 rad. The CCD input threshold was found to shift by 3 to 6 volts at 10^6 rad, depending on oxide thickness. Typically, one half of this shift had occurred at a dose of 10^5 rad, and little shift was seen after 5×10^5 rad. The CTI increase was more than that seen in the better devices in the Co^{60} gamma tests. The devices typically had a large increase in leakage current at about 3×10^5 rad, which made CTI measurements difficult. It was later found that this leakage current can be greatly reduced by increasing the substrate bias, as in the case of some of the Co^{60} irradiated devices.

One very different result for these tests was that the source follower gain was degraded much less than was the case for the Co^{60} tests. This is probably due to the fact that for a high dose rate source, the CCD output node is discharged to nearly substrate voltage by the large photocurrent during the radiation. Therefore, the gate bias on the source follower is nearly zero during irradiation compared to a gate bias of about +24 volts for buried-channel devices in the low-dose-rate Co^{60} tests.

VI. CONCLUSIONS

It seems unlikely that total dose hardness to the 10^6-rad range can be achieved with surface-channel CCDs due to large CTE degradation caused by surface state trapping. However, even though several problems remain with the buried-channel devices tested to date, it appears that buried-channel devices can be made using the structure described here that will give good performance after exposure to doses of up to 10^6 rad. The major problems identified are input and output level shifts, increased dark current and associated noise, and output MOSFET gain loss.

REFERENCES

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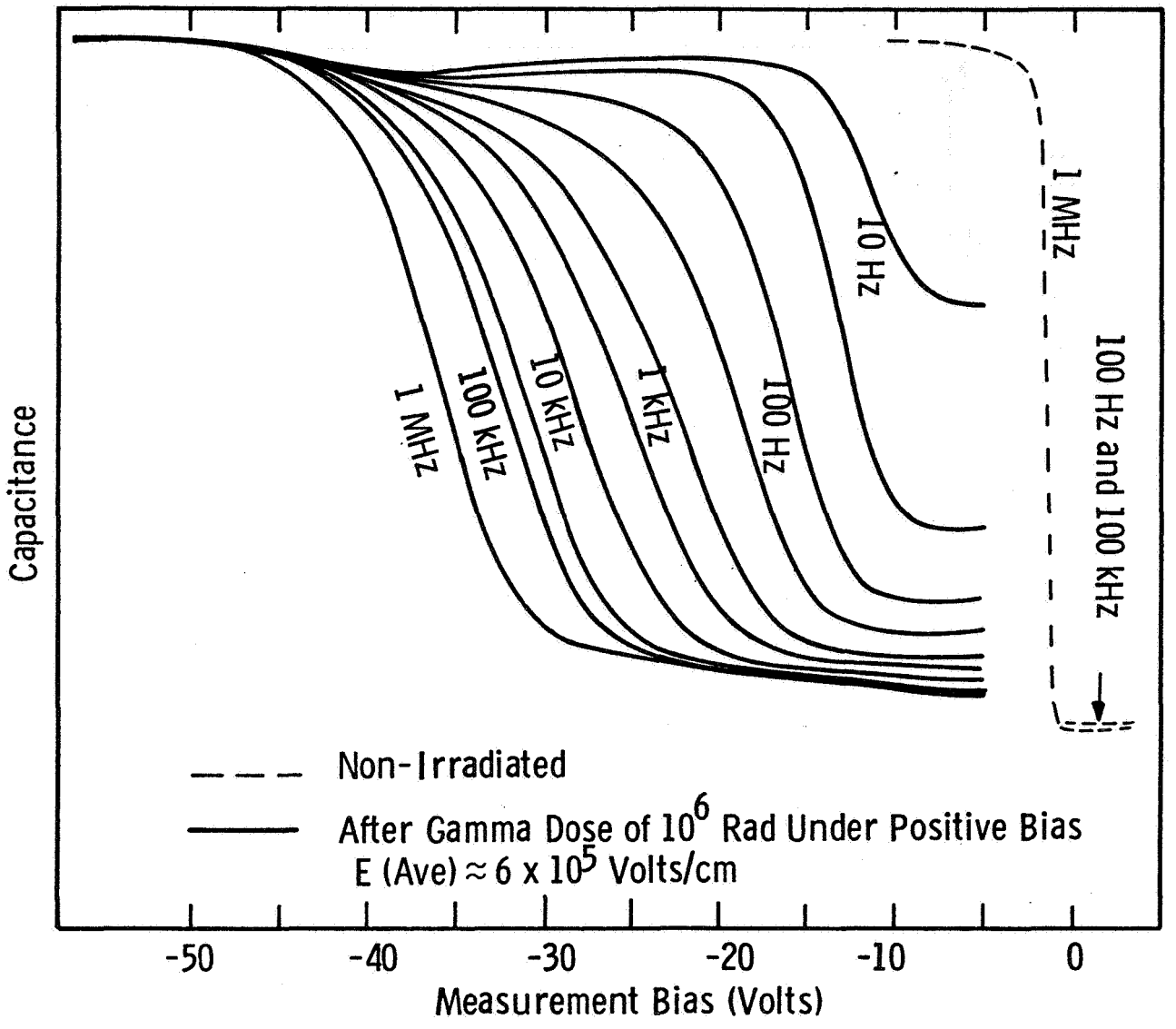


Figure 1. Curves showing CV shift with frequency for surface-channel MOS capacitors with HCℓ oxide

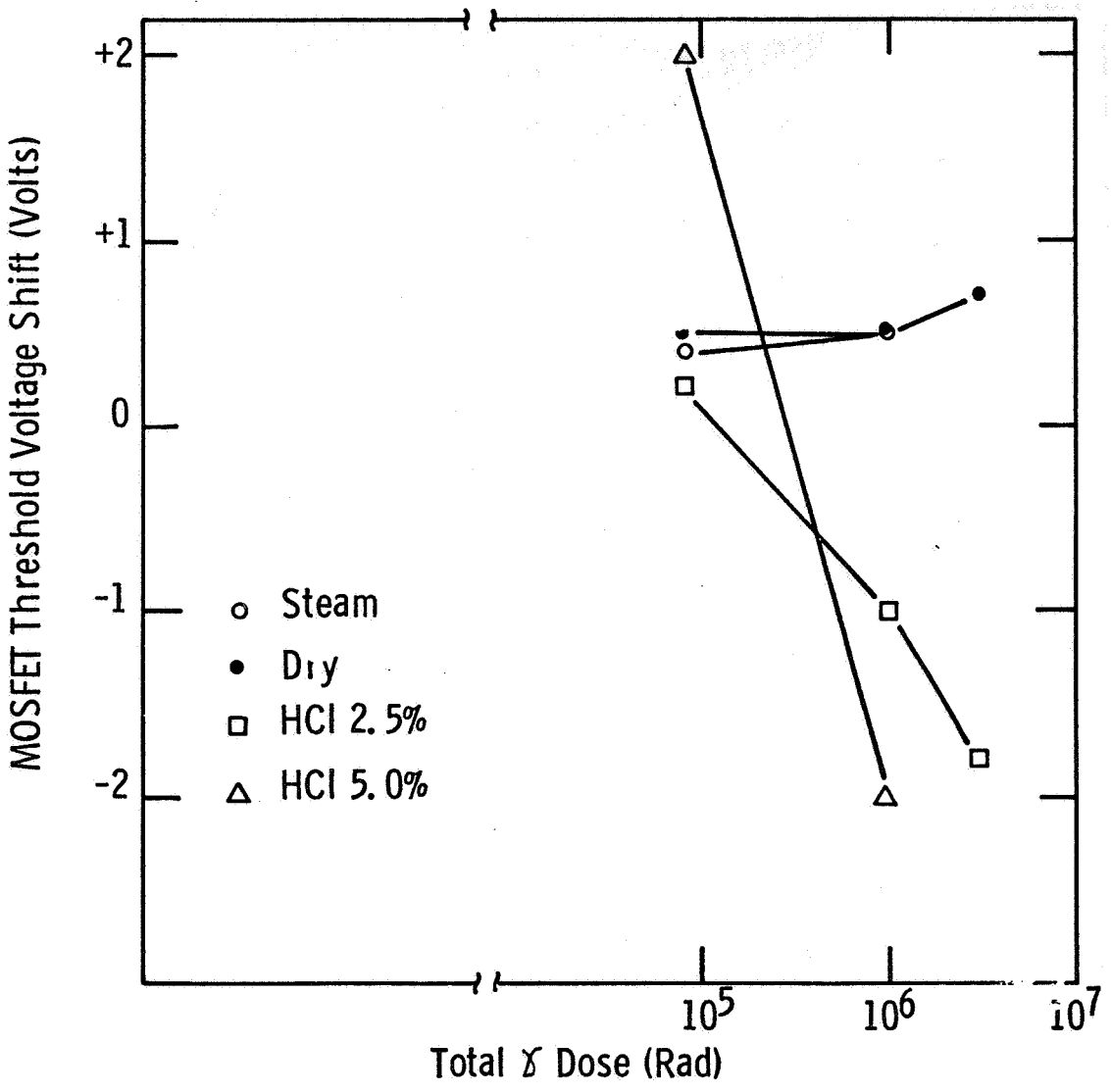


Figure 2. MOSFET threshold variation with gamma dose for surface-channel devices

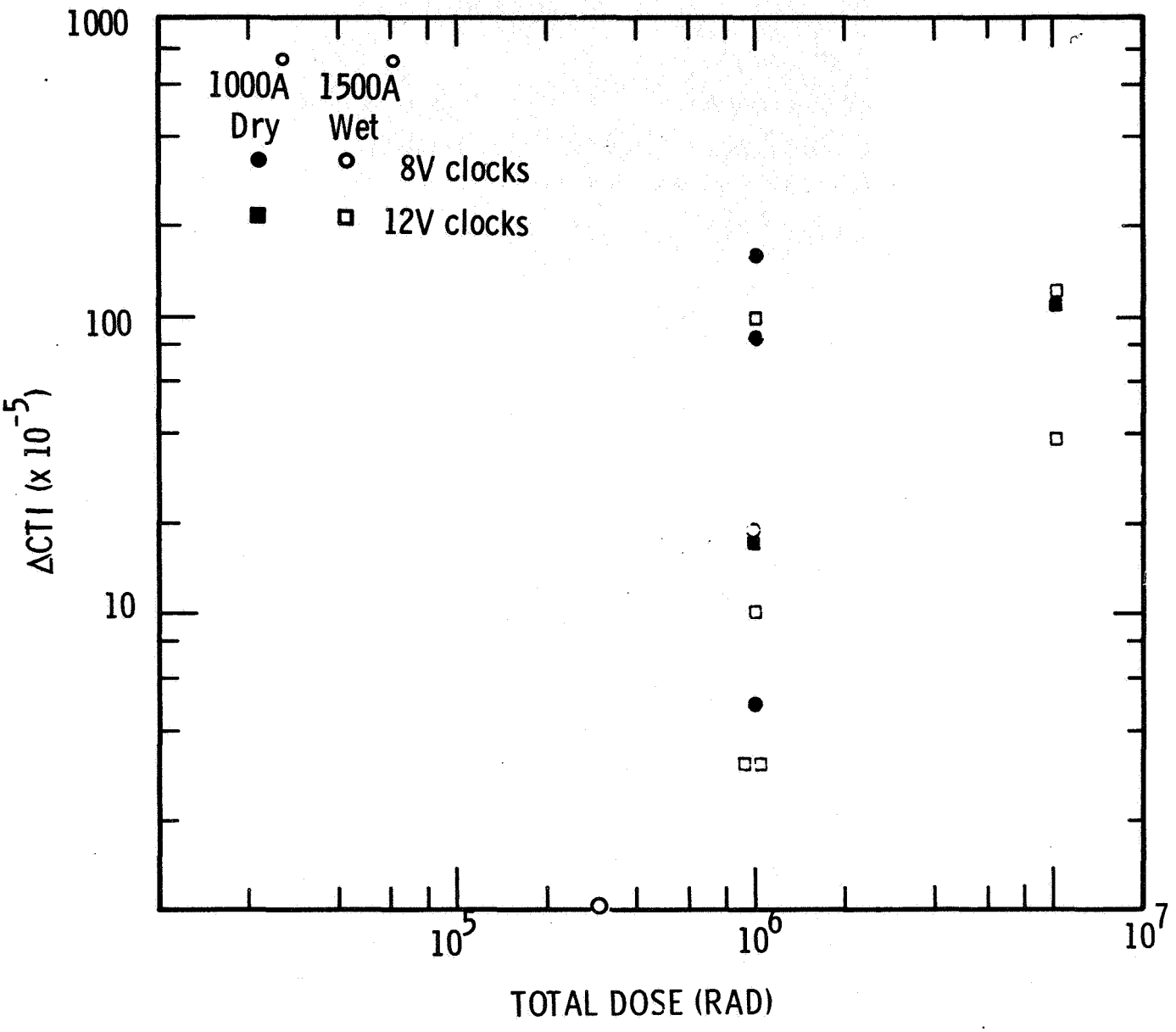
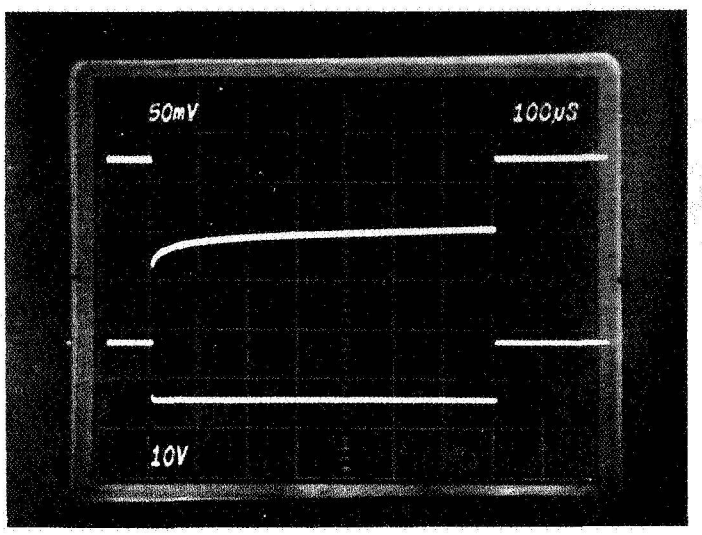
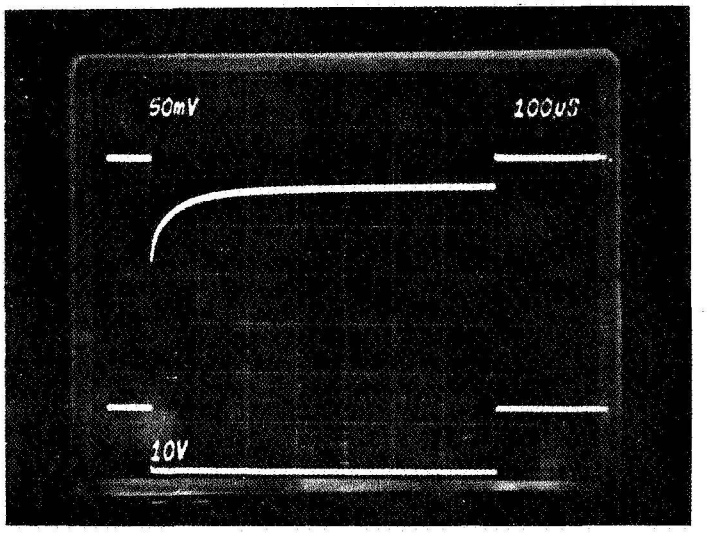


Figure 3. Change in charge transfer inefficiency with gamma dose for buried-channel CCDs

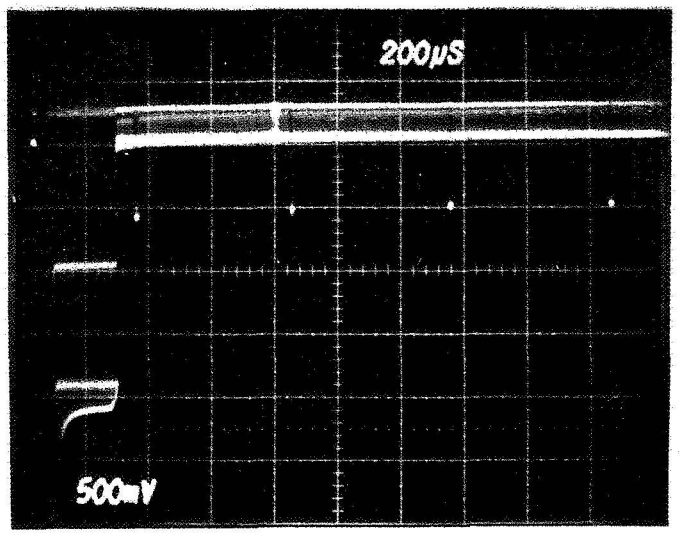


Sample 68-6-66

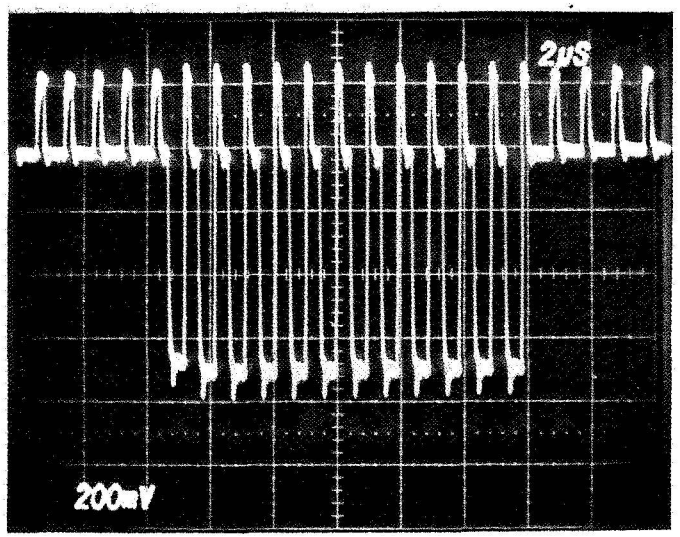


Sample 68-4-157

Figure 4. Variation of MOSFET drain current with time due to emptying of surface state traps [Top trace – 1_D (2 ma/div), lower trace – V_G. (10 V/div).]



Output waveforms of buried channel CCD showing operation during and after exposure to a 100ns wide pulse of 20 Mev electrons from Linac dose rate is 10^{10} Rad/sec.



Expanded scale waveform of CCD signal pulse demonstrating good CTE after recovery from saturation caused by photocurrent from radiation pulse.

Figure 5. Waveforms of CCD output showing recovery from 10^{10} rad/sec radiation pulse