EFFECTS OF IONIZING RADIATION ON CHARGE-COUPLED IMAGERS

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The effects of ionizing radiation on three different charge-coupled imagers have been investigated. Device performance was evaluated as a function of total gamma ray dose. The principal failure mechanisms have been identified for each particular device structure. The clock and bias voltages required for high total dose operation of the devices are presented.

I. INTRODUCTION

The recently developed charge-coupled devices (CCDs) are expected to have low cost, small size, low power consumption, and high reliability. Such characteristics make CCDs especially attractive for space flight missions if the devices can be made to operate in a radiation environment. Since no standard CCD design has yet emerged, we have been engaged in a program to evaluate the effects of ionizing radiation on several of the CCD structures currently in use. Our objectives have been to identify the radiation-induced failure mechanisms and to determine whether the clock and bias voltages can be modified to permit higher total dose operation.

The CCD imagers that we have evaluated include: (1) a 256-bit, two-phase linear imager with overlapping polysilicon gates; (2) a 60-bit, three-phase linear imager with planar doped polysilicon electrodes and high-resistivity polysilicon interelectrode isolation; and (3) a 100 X 100 bit area imager with associated two-phase transfer registers. All three types of

imagers were buried-channel devices. No effort was made to process harden any of the devices to radiation.*

II. REVIEW OF CCD OPERATION

Space considerations do not permit an explanation of the manner in which CCD imagers operate. Instead, the reader is directed to a number of tutorial papers (Refs. 1, 2, 3). Those aspects of CCD operation which are important to the treatment of radiation effects were briefly presented by Killiany et al. (Ref. 4). The state-of-the-art in CCD imagers has recently been reviewed by Barbe (Ref. 5).

III. EXPERIMENTAL DETAILS AND RESULTS

A. 256 X 1 Linear Imager

The test device is a 256-bit linear imager employing the double-register parallel transfer readout organization shown in Figure 1a (Ref. 6). The 256 photosites are separated by diffused channel stops and covered by a polysilicon photogate 23 μm wide. The center-to-center spacing of the photosites is 13 μm. The two-phase parallel shift registers have overlapping polysilicon gates and self-aligned ion implanted barriers. The right-left register outputs are interlaced at the output gate and fed into the gated charge integrator. The shift registers are designed to operate at 5 MHz with a resulting 10 MHz output data rate. The on-chip compensation amplifier can be used to suppress the reset clock noise by use of a differential amplifier in the external video circuitry.

A cross-section of the shift register is shown in Figure 1b. The gate insulator is a combination of an oxide and a nitride (Si_3N_4) layer. The self-aligned barrier is formed by means of a boron implant. The shift registers are covered with aluminum to prevent the incident light from going through the polysilicon gates and smearing the image.

The devices were characterized in both the integration mode and the continuous mode of operation. For the integration mode, the photogates are

*The devices were fabricated by Fairchild Semiconductor, R&D Laboratory, Palo Alto, California, and are commercially available. Fairchild's 500-stage linear imager has the same structure as the 60 X 1 test imager.

held at +5 V, and the 1-MHz shift register clocks swing from 0 to +7 V with a 50% duty cycle. Charge is transferred from the photosites to the shift registers by holding the shift register clocks at their high value and pulsing the transfer gate from 0 to +7 V. In the devices available for testing, one of the shift registers was inoperable. Hence, all photosites had to empty into one register. This necessitated the use of a modified timing diagram. The reset pulse frequency was 1 MHz instead of the 2-MHz rate required to interlace the outputs of the parallel registers.

The input diode (ϕ_{SB}) and input gate (GB) were respectively biased to +12 V and 0 V to prevent charge from being introduced into the shift registers electrically. The output gate (OG) was held at +3 V, while both the reset drain and output diode voltage was +15 V.

For continuous mode operation, both the photogate and transfer gates were held at 0 V.

Two devices were irradiated, with Cobalt 60 gamma rays, the first to 4.5×10^4 rads (Si) and the second to 1.88×10^5 rads (Si). The devices were irradiated while being operated as line imagers with normal bias and clock voltages applied. The integration time was 12.8 ms. An unirradiated control device was also recharacterized after each dose increment as a check to the proper operation of the electronics. For total doses less than 5×10^4 rads, a dose rate of 8.2×10^2 rads (Si)/min was employed. The highest dose rate employed was 4.6×10^3 rads (Si)/min. The flat-band voltage shift was determined from 1-MHz C-V curves taken from an on-chip buried-channel capacitor whose gate was biased with the ϕ-1 clock and which had +15 V applied to the buried channel.

The radiation-induced flat-band voltage shift (ΔV_{FB}), shown in Figure 2a, limited device operation with the pre-irradiation clocks and bias to 4.5×10^4 rads (Si). The failure mechanisms resulting from ΔV_{FB} were: (1) buried channel driven out of depletion, (2) reset transistor biased in the conducting state for the entire clock period, and (3) input gate turned on. These three effects will be discussed separately in the following paragraphs.

The first requirement for successful operation of a buried-channel CCD is that, for zero signal, the implanted layer should be entirely depleted of majority carriers. The depletion is accomplished by applying a sufficiently large positive voltage to the output diode at the end of the CCD channel. The effect of the positive charge buildup in the oxide during irradiation is to increase the reverse bias required for total depletion. The minimum reset voltage required to deplete the buried channel is shown in Figure 2b as a function of radiation dose. The maximum reverse bias that can be applied across the output diode of this device is 18 V. Hence, for doses greater than 5×10^4 rads, with the pre-irradiation gate clock and bias voltages previously specified, the reset drain voltage required to deplete the buried channel is greater than the maximum reverse bias which can be applied to the output diode.

The pre-irradiation threshold voltage of the reset drain transistor was +5 V. For doses greater than 4×10^4 rads, the flat-band voltage shift is of sufficient magnitude to cause the reset transistor to be biased into the conducting state for the entire clock period. This has the effect of severely distorting the output signal. Proper reset drain transistor operation can be restored by applying a negative dc offset to the reset gate clock of sufficient magnitude to turn off the transistor between pulses.

The input gate threshold voltage as a function of dose is shown in Figure 2b. For a pre-irradiation input gate voltage of 0 V, the input would be turned on at 4.5×10^4 rads, filling the shift register wells. Saturation of the imager shift register can be avoided by simply increasing the reverse bias on the input diode while biasing the input gate to a negative voltage. In order to apply an analog signal to the shift register, a more sophisticated input scheme which minimizes the effect of the flat-band voltage shift must be employed since the input gate voltage swing between threshold and full-well is only about 0.5 V (Ref. 7).

At doses greater than 2×10^4 rads, the gain of the on-chip FET amplifier began to degrade. After 4×10^4 rads, the voltage output for a full-well signal was reduced to ~70% of its pre-irradiation value. The decrease in the amplifier gain was probably due to a shift in the operating point of the amplifier to large current values with a corresponding smaller transconductance.

The pre-irradiation full-well signal voltage could be restored by increasing the output drain voltage from +15 to +18 V.

The transfer inefficiency as a function of dose for electrically introduced full-well and half-well signals is shown in Figure 3a. The larger increase in the inefficiency for the full-well signal can probably be attributed to increased interface trapping. The interface state density as measured by a G-V technique was $1.3 \times 10^{10}/(cm^2 eV)$ at 0 rads and increased to a value of $6 \times 10^{10}/(cm^2 eV)$ at 4.5×10^4 rads. At 4×10^4 rads, a measurement of inefficiency vs. signal amplitude showed a sharp increase in loss for signals greater than 50% full-well. The inefficiency for 25% full-well was approximately the same as the 50% full-well value. A larger inefficiency for signals greater than 50% full-well is expected since the buried-channel device is operating in the surface-channel mode with increased interface state trapping (Ref. 8).

The increase in the thermally generated charge (dark current) density as a function of dose is shown for both devices in Figure 3b. The 27-fold increase at 4×10^4 rads would restrict operation to short integration times (i.e., the wells are filled with the dark charge in approximately 17 ms) or require cooled operation.

The full-well capacity of both the photosite and shift register wells remained at the pre-irradiation value of 3×10^5 electrons at 4×10^4 rads.

In principle, the minimum reset drain voltage required to totally deplete the buried channel could be reduced to the pre-irradiation value by applying a negative dc offset voltage to all clock and bias gates to compensate for the change in surface potential produced by the trapping of positive charge in the oxide during irradiation. This was confirmed experimentally for device No. 9 at 2×10^4 and 3×10^4 rads by applying offset voltages of -3.5 V and -5 V, respectively.

Device No. 9 was operated for doses greater than 4.5×10^4 rads, with a reset drain bias of 17.5 V, by applying a negative 5-V offset to all gate clocks and bias except the reset transistor gate whose clock had a negative 3-V offset. The input diode voltage was held at the pre-irradiation value, while the output transistor drain bias was increased to 18 V. Device No. 9 was irradiated with these offset voltages for doses greater than 5×10^4 rads and functioned up to

a dose of 9×10^4 rads. Operation at 10^5 rads was restored with the application of a negative 9-V offset to the gate clock and bias voltages. The transfer inefficiency, full-well capacity, and signal amplitude at 7.5×10^4 rads were approximately the same as those measured at 4×10^4 rads. However, the dark current density increased to 2000 nA/cm^2. At 1.25×10^5 rads, the transfer inefficiency for a half full-well signal had increased to 3×10^{-3}.

Unless a capability exists for changing the voltages on the gate clocks and the bias of a device after it has been irradiated, the unirradiated devices must be capable of being operated with those negative offset voltages which are compatible with operation at large doses. Two unirradiated devices were operated as imagers with a -5 V offset on all gate clocks and bias except the reset transistor clock, which has a -3 V offset.

In summary, these devices were operated with the pre-irradiation clock and bias up to 4.5×10^4 rads. The application of negative dc offset voltages to the gates extended the operational range to 1.25×10^5 rads.

B. 60 X 1 Linear Imager

This device, with a structure as illustrated in Figure 4, is a three-phase buried-channel CCD with planar, doped polysilicon electrodes and high-resistivity polysilicon interelectrode isolation. The substrate is 60-95 ohm-cm p-type silicon with <100> orientation. The channel oxide is thermally grown by a dry oxide technique and is 1800 Å thick. Ion implantation of phosphorus through the oxide is used to form a buried-channel 3000 Å thick with an average doping of 3×10^{16} cm^{-3}. A layer of high-resistivity polysilicon about 5000 Å thick is deposited over the channel oxide. The electrode pattern is formed by selective phosphorus diffusion into the polysilicon sheet. A vapor-deposited oxide is used to protect the device from damage.

During operation, the buried channel was kept completely depleted by a reverse bias of nominally 13 V between the channel drain contact and the substrate. (All voltages are referenced to the grounded substrate.) The phase voltage clock swing was between -2 V and +5 V. The imaging gate was held at +5 V during the integration time and was pulsed to -2 V when charge was to be transferred to the vertical registers. The transfer gate was held at -2 V during integration and was pulsed to +5 V when charge was to be

transferred to the vertical registers. The nominal integration time was 1 ms. The aluminum light shield was connected to the substrate.

The flat-band voltage shift under the imaging gate was -5.5 V at 3×10^4 rads. The failure mechanisms resulting from ΔV_{FB} were: (1) buried channel driven out of depletion, (2) channel induced in the undoped polysilicon interelectrode isolation regions. These two effects will be discussed separately in the following paragraphs.

The minimum reset drain voltage (V_{DR}) required to deplete the buried channel was +10 V for an unirradiated device. At a dose slightly greater than 1×10^4 rads, the nominal +13 V reset drain bias was no longer sufficient to totally deplete the channel. Experimentally, after 3×10^4 rads, a reset drain voltage of +15 V was required to operate the CCD.

The resistivity of the undoped polysilicon isolation between the gate electrodes was reduced by a factor of approximately 20 after a total dose of 3×10^4 rads. This drop in the resistance was due to field-induced channeling in the undoped polysilicon as a result of trapped positive charge in the oxide. The lower isolation resistance allowed the various clock and bias voltages to mix together. The principal result of the mixing was that the transfer and imaging gate waveforms were altered such that almost no barrier existed between the photosensitive elements and the vertical transport registers. A cross-section of the device with calculated pre- and post-irradiation potential profiles is shown in Figures 4c through 4e. The barrier reduction allowed almost all of the photo-generated charge under the imaging gate to continuously spill into the vertical registers instead of being collected for an integration time prior to being transferred. As a result, the effective output signal was reduced to approximately 3% of the pre-irradiation full-well capacity. This observed reduction agrees well with that expected from the profile of Figure 4e. Consequently, these devices became inoperative at a total dose of 3×10^4 rads, and operation could not be recovered by adjusting the bias and clock voltages.

Additional details concerning the effects of radiation on these devices have been published (Ref. 9).

C. 100 X 100 Area Imager

The device consists of 10^4 photosensitive sites arranged in 100 columns, each containing 100 sites (see Figure 5a). Adjacent to each column of photosensitive sites is a vertical transfer register. The horizontal shift register is employed to multiplex the signals from the vertical registers. A differential FET amplifier on the chip provides the video output.

During irradiation, the buried channel was kept depleted by applying a reverse bias of nominally 16 V between the channel drain and substrate. The horizontal clock rate was 2 MHz with a voltage swing between +3 V and -7 V. The vertical clock pulses were 10 μs wide with a period of 63 μs. For one of the vertical phases, the pulse swing was from +1.5 V to -7 V and back; for the other, the pulse swing was from -7 V to +1.5 V and back. During integration, the photosensitive sites were held at +4.5 V to collect photoelectrons and then were briefly pulsed to +1.5 V to transfer the charge into the vertical transfer registers. The integration time was about 8 ms.

The device has the structure shown in Figure 5b. It is a two-phase, buried-channel CCD with ion-implanted barriers. The electrodes are doped polysilicon and the interelectrode isolation is high-resistivity polysilicon. The CCD substrate is 60-90 ohm-cm p-type silicon with <100> orientation. The channel oxide is 1200 Å thick and is grown by a dry oxide technique. Ion implantation of arsenic through the oxide is used to form an n-type buried channel with a thickness of about 3000 Å and an average doping of 1×10^{16} cm^{-3}. The barriers necessary for two-phase operation are formed by implanting boron into the channel. A layer of high-resistivity polysilicon is deposited over the channel oxide. The electrode pattern is formed by selective diffusion into the undoped polysilicon sheet. A thick vapor-deposited oxide covers the device. Aluminum light shields are used to cover all of the active region except for the photosensitive areas.

These CCDs were used as the imaging device in a TV operating at a frame rate of 120 frames/second (4 times the conventional TV rate), with a line time of 65 μs. The geometrically calculated limiting resolution for these devices is approximately 16 lp/mm in the vertical direction and 12 lp/mm in the horizontal direction. The experimental values determined with a

resolution target range from 14 to 16 lp/mm vertically and from 11 to 12 lp/mm horizontally. A typical pre-irradiation image is shown in Figure 5c.

For a total dose of 1×10^4 rads, no change in the imaging quality of the devices was observable. At 3×10^4 rads, the image did deteriorate significantly. A qualitative demonstration of this is shown in Figure 5d. The limiting resolution at this total dose decreased to between 6 and 10 lp/mm vertically and between 5 and 6 lp/mm horizontally. At a total dose of 1×10^5 rads, no image at all was obtained with the original clock and bias voltages. After substantial adjustments of the operating conditions, a rather poor image could be recovered.

Measurements on interelectrode resistances indicate that channeling in the polysilicon isolation regions is very likely responsible for the CCD deterioration at higher doses. The dc interelectrode resistance for both the vertical and horizontal clocks was observed to drop to approximately 20% of its pre-irradiation value at 3×10^4 rads and to less than 10% at 1×10^5 rads. The reduced interelectrode resistance allows a mixing of the clocking waveforms with a resulting disturbance in the potential well and barrier shapes. The effect appears to be the same as that seen on the 60 X 1 imagers described in the preceding section.

Additional details concerning the effects of radiation on these devices have been published (Ref. 4).

IV. CONCLUSION

The operating range of a CCD imager in a radiation environment can be extended by carefully choosing the pre-irradiation bias voltages. For the devices tested, the most important consideration was to bias the reset drain so that the buried channel remained depleted after irradiation.

REFERENCES

1. D.F. Barbe, "The Charge-Coupled Concept," Reports of NRL Progress, March 1972, p. 1.

2. M.F. Tompsett, "Charge Transfer Devices," J. Vac. Sci. Tech., 9, 1166 (1972).

REFERENCES (continued)

3. J.E. Carnes and W.F. Kosonocky, "Charge-Coupled Devices and Applications," Solid State Tech., 17, 67 (1974).

4. J.M. Killiany, W.D. Baker, N.S. Saks, and D.F. Barbe, "Effects of Ionizing Radiation on Charge-Coupled Device Structures," IEEE Trans. Nuc. Sci., NS-21, 193 (1974).

5. D.F. Barbe, "Imaging Devices Using the Charge-Coupled Concept," Proc. IEEE, 63, 38 (1975).

6. C.K. Kim, "Two-Phase Charge Coupled Linear Imaging Devices with Self-Aligned Implanted Barrier," Proceedings of the International Electron Device Meeting, Washington, D.C., Dec. 1974, p. 55.

7. S.P. Emmons and D.D. Buss, "Techniques for Introducing a Low Noise Fat Zero in CCD's," Device Research Conference, Boulder, Colorado, June 1973.

8. C.K. Kim, "Design and Operation of Buried Channel Charge-Coupled Devices," Proceedings of the CCD Applications Conference, San Diego, California, Sept. 1973, p. 7.

9. J.M. Killiany, N.S. Saks, W.D. Baker, and D.F. Barbe, "Effects of Radiation on Buried-Channel CCD's with Doped Polysilicon Gates and Undoped Polysilicon Interelectrode Isolation," Appl. Phys. Lett., 24, 506 (1974).

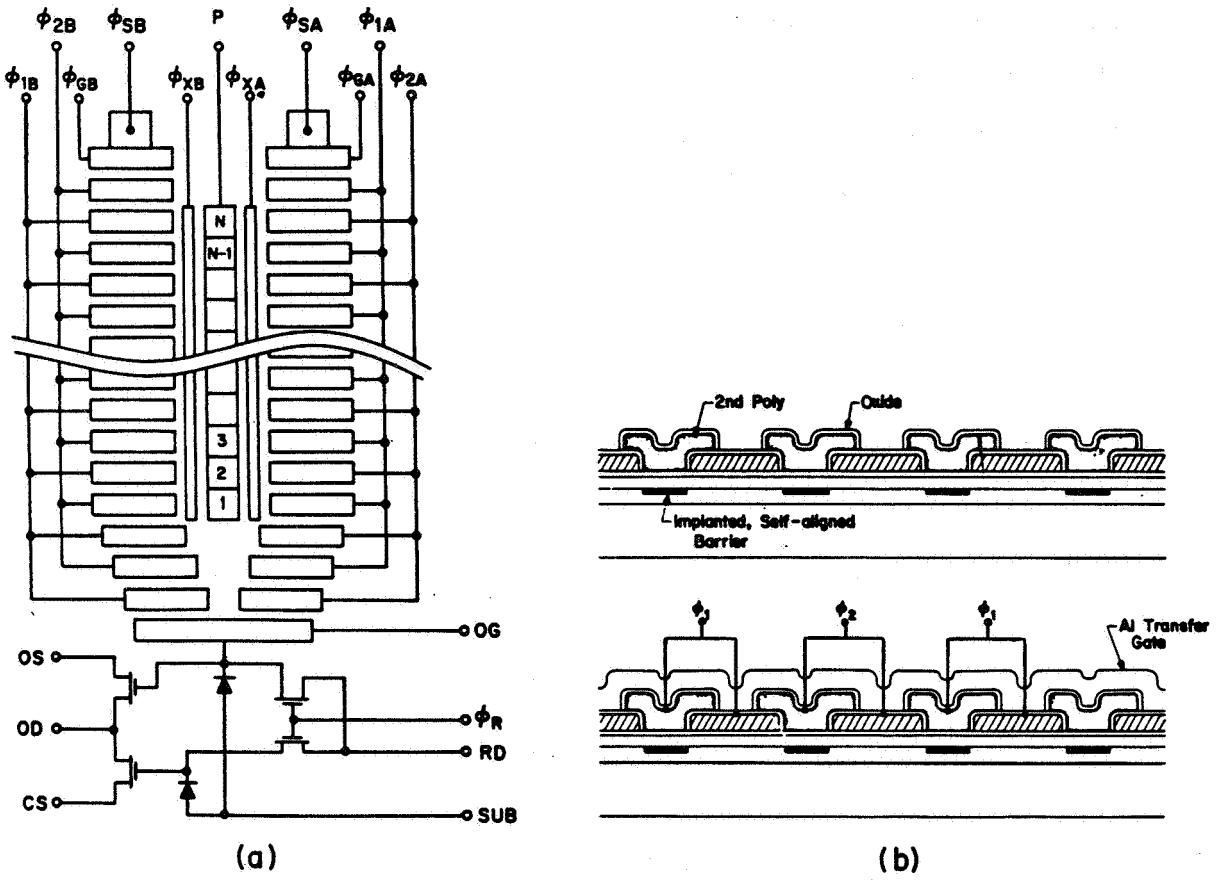

Figure 1. 256 X 1 CCD structure: (a) top view of the device; (b) cross-sectional view along the shift register

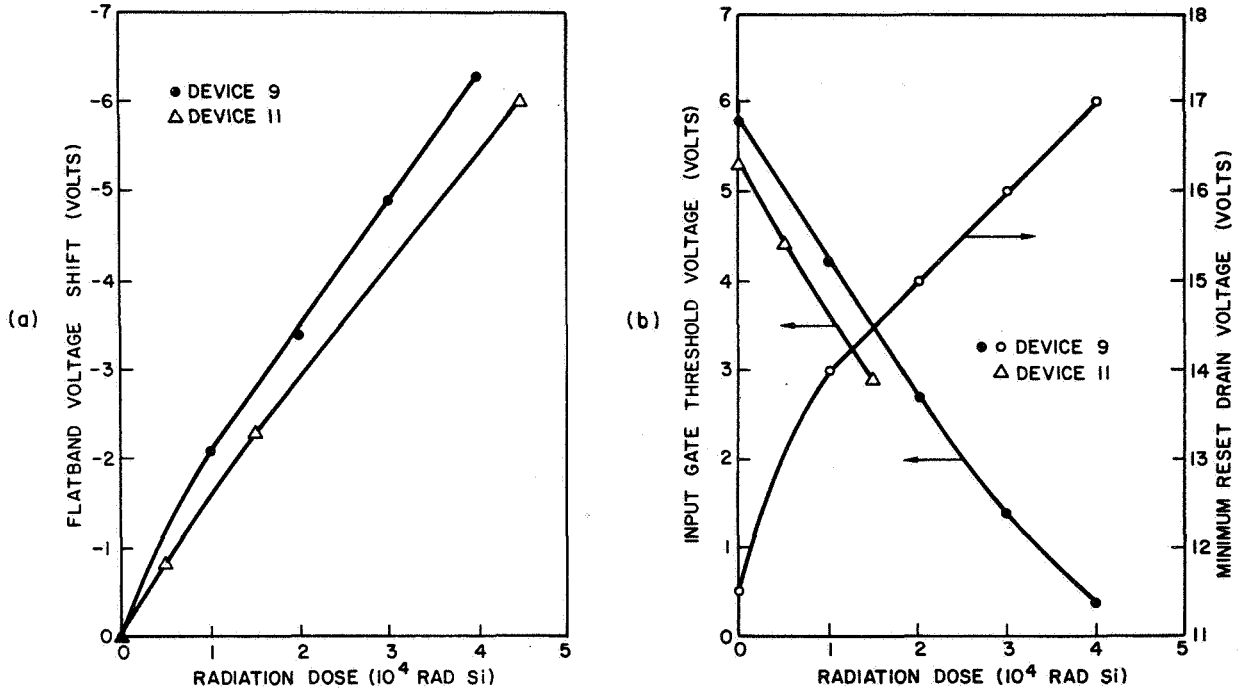

Figure 2. (a) Flat-band voltage shift vs. total dose for 256 X 1; (b) input gate threshold voltage and minimum reset drain voltage vs. total dose for 256 X 1

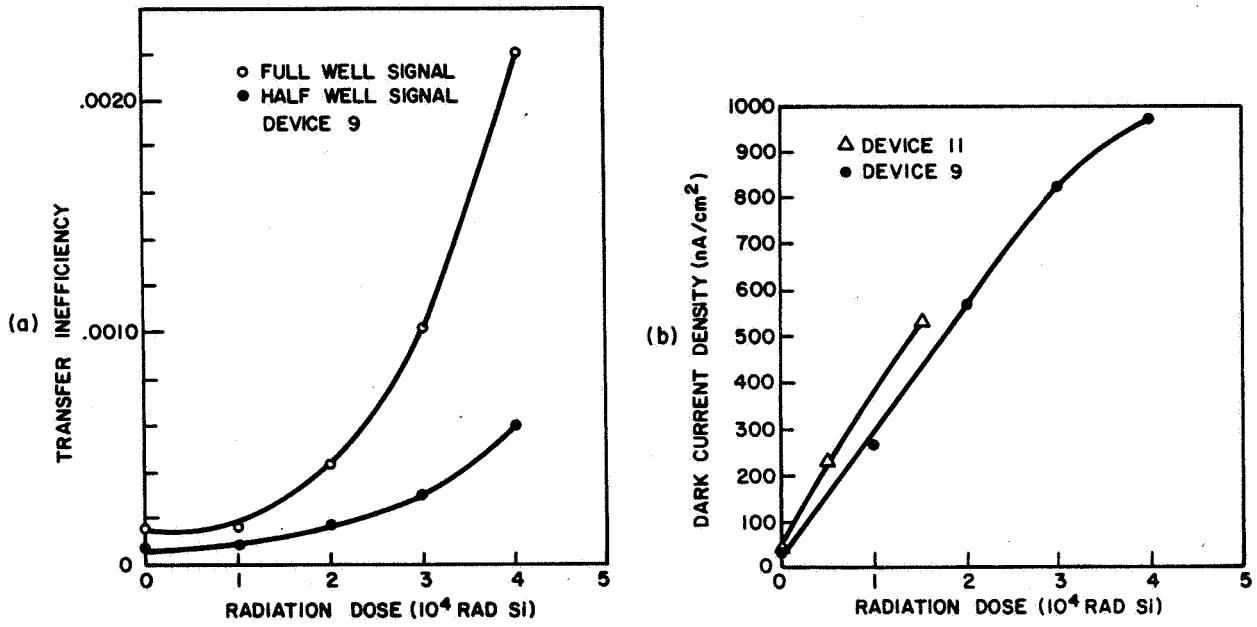

Figure 3. (a) Transfer inefficiency vs. total dose for 256 X 1; (b) dark current density vs. total dose for 256 X 1

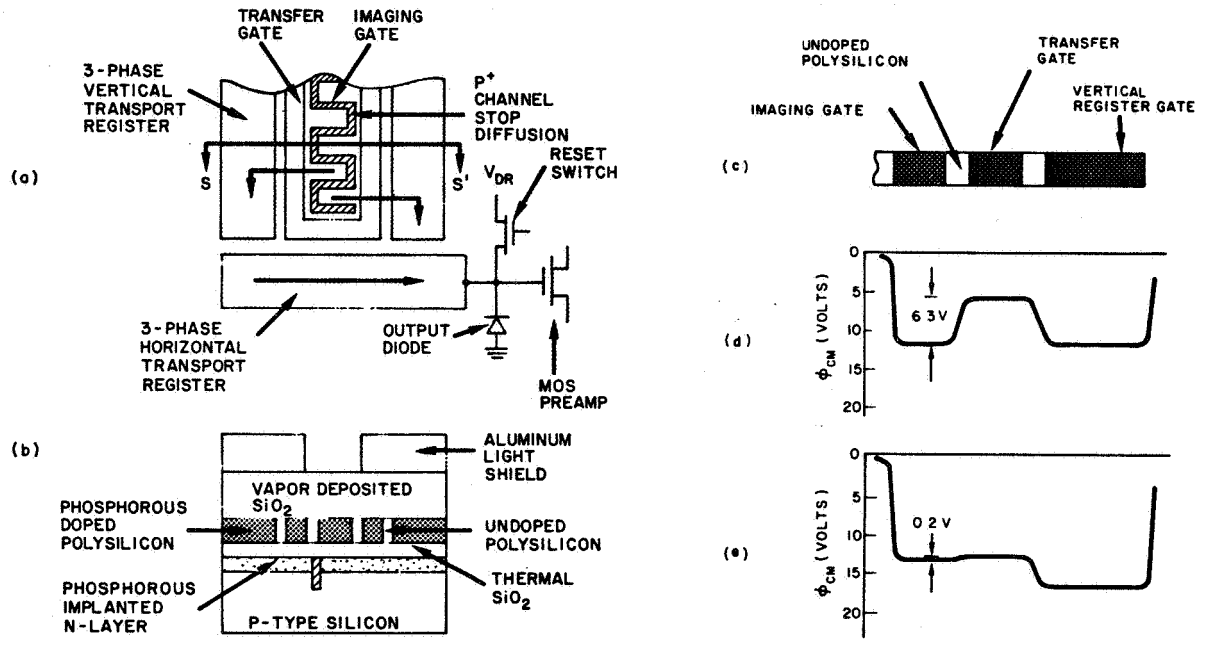

Figure 4. 60 X 1 CCD structure and potential profiles: (a) top view; (b) cross-sectional view; (c) cross-section of the gate structure; (d) pre-irradiation profile of the maximum channel potential; (e) profile of the maximum channel potential after 3×10^4 rads

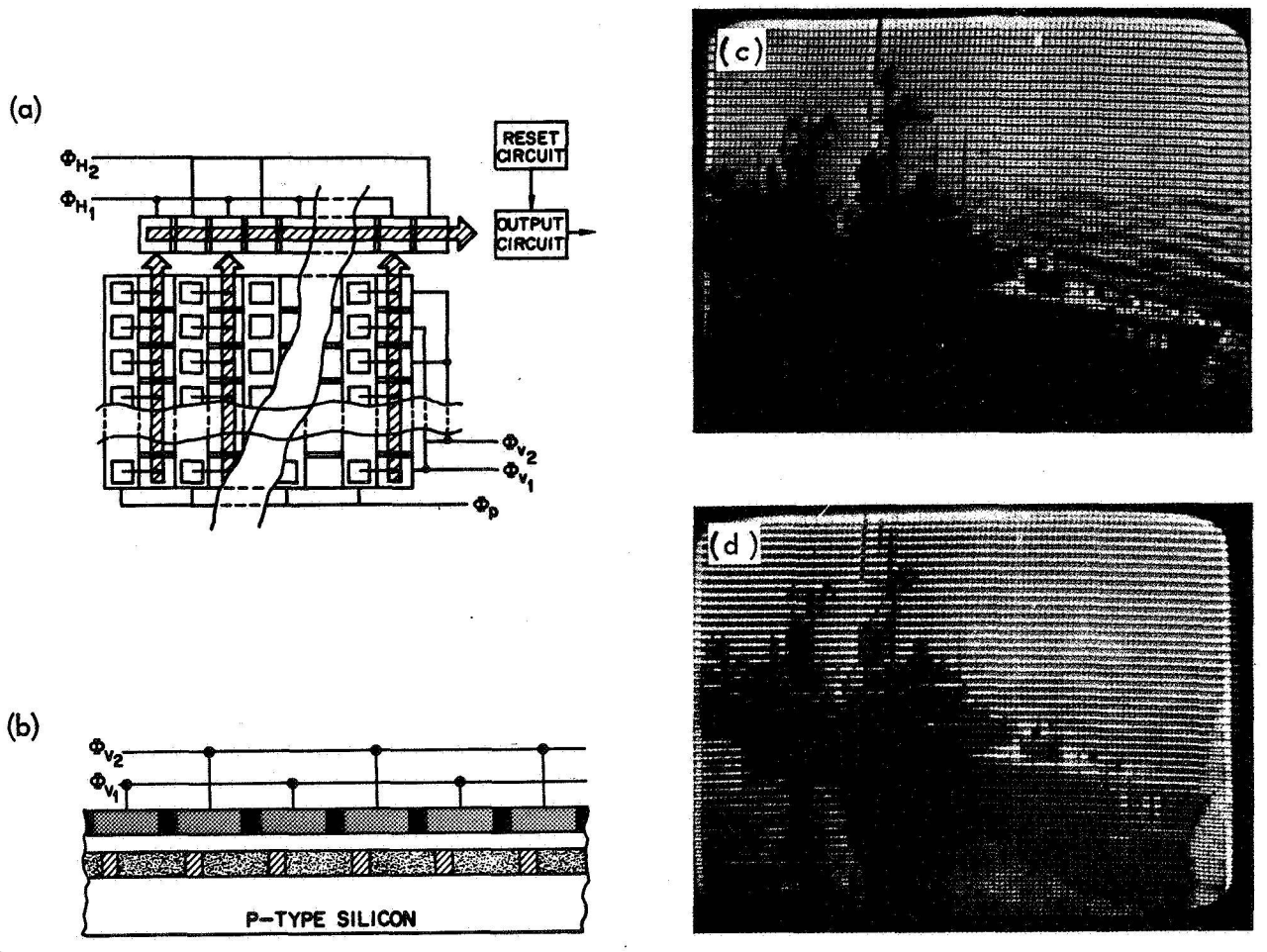

Figure 5. 100 X 100 CCD structure and image quality: (a) top view of the device; (b) cross-sectional view along a vertical transfer register; (c) pre-irradiation image; (d) image after 3×10^4 rads