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BATTERY PEAK CHARGE VOLTAGE MONITOR FOR

DUAL AIR DENSITY SATELLITE

By Thomas A. Shull

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16. Abstract

A battery peak charge voltage monitor has been developed for use on the Dual Air Density Satellite (DADS). This device retains a reading of the maximum voltage reached by the spacecraft battery during periods of charging and makes it available during periods of data transmission. The monitor is connected across the battery and operates solely from the battery. It is powered continuously with quiescent input current of only 3 milliamperes. Standard integrated circuits and a thin-film resistor network are utilized. The monitor occupies approximately 40 square centimeters of a printed-circuit board within a larger electronic package.

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BATTERY PEAK CHARGE VOLTAGE MONITOR

FOR DUAL AIR DENSITY SATELLITE

By Thomas A. Shull

SUMMARY

A battery peak charge voltage monitor has been developed for use on
the Dual Air Density Satellite (DADS). This device retains a reading of the
maximum voltage reached by the spacecraft battery during periods of charging
and makes it available during periods of data transmission. The monitor is
connected across the battery and operates solely from the battery. It is
powered continuously with quiescent input current of only 3 milliamperes.
Standard integrated circuits and a thin-film resistor network are utilized.
The monitor occupies approximately 40 square centimeters of a printed-circuit
board within a larger electronic package.

INTRODUCTION

The life and performance of a satellite depends heavily on its
battery. To prolong battery life through efficient use, many measurements
are made concerning its parameters. There is one measurement, however, that
cannot be made during periods of data transmission. This is the maximum
voltage reached by the battery while being charged. This is because battery
charging only occurs between interrogations, due to the power required by
the data system. In order to obtain charge information, a device was needed
that could monitor the battery between interrogations, measure the peak
charge voltage, and hold the measurement for subsequent transmission. For
interrogations in darkness, this could mean holding 30 to 40 minutes,

requiring more than simply a holding capacitor. This paper describes the operation, design, and testing of a battery peak charge voltage monitor developed for the Dual Air Density Satellite (DADS).

SYSTEM OPERATION

Figure 1 is a functional block diagram of the peak charge voltage battery monitor. It is a parallel feedback analog-to-digital converter with an up counter in the feedback loop. The unit is connected directly across the battery which is both the input and power source. The monitor output reading is available as eight parallel logic lines. The only other connections are reset and ground.

The peak charge measurement is made by maintaining an internal voltage that is equivalent to the maximum input voltage. The input battery voltage, V_B, is first divided in half. $V_B/2$ is then compared to the output from the R-2R ladder, V_L. V_L is directly proportional to the binary count at the ladder inputs. The comparator then adjusts V_L by controlling the binary count. When V_B is applied, the count is increased until V_L differs from $V_B/2$ by no more than half the measurement resolution. For any further increase in V_B, the count increases until V_L once again approximates $V_B/2$. If V_B decreases, the count does not change. Therefore, the binary count at the ladder inputs represents the maximum voltage attained by the input.

To obtain a new reading, the count is reset and the process is repeated. On the DAD satellites, the battery monitor is reset at the end of each interrogation by the main bus off command. There is also a reset pulse generated by a system timer after approximately 4 minutes of data

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transmission. This provides a calibration check between the monitor and the spacecraft data system encoder.

The eight logic lines brought out are actually the least significant eight bits of a nine-bit measurement. Under normal conditions, the input voltage is within the range of 11 to 16 volts. Taking advantage of this fact, the most significant or half-scale bit can be held to a "1." This allows a measurement with nine-bit resolution to be introduced into an eight-bit data system. Accuracy is improved by using a 10-bit ladder. The tenth bit is set to a "1" to give V_L the proper offset.

SYSTEM DESCRIPTION

Figure 2 is a complete schematic of the battery monitor.

Ladder Network

The ladder is a thin-film resistor network composed of a standard 10-bit R-2R ladder with two additional 2R resistors. The value of R is 50 kilohms. This value keeps the expected variation of the ladder switch impedance negligible and minimizes power dissipation. The two additional resistors are used to divide V_B in half. They have the value 2R to make the impedance seen at the comparator inputs equal. Each switch leg of the ladder is 2R-500 ohms to allow for the switch impedance. All the resistors are ratic matched, and being in the same package, track well under temperature variations. The ladder accuracy is $\pm$ 1/2 least significant bit out of 1C.

Comparator

The comparator includes a 108A operational amplifier, two complementary MOS or CMOS logic NAND gates, two resistors, and a zener diode. The 108A is a general-purpose, low-power amplifier. It is connected open loop providing a gain in excess of 40 volts/millivolt. This is followed by the two NAND gates, G3 and G4, which effectively add more gain to the comparator. The output of the comparator is a logic "1" or "0," depending on whether $V_B/2$ is larger or smaller than V_L. The output changes states for input differences of less than 0.1 millivolt. The NAND gates are biased by V_R and, therefore, should not see an input greater than V_R. The 108A's output voltage, however, can change from near ground to near V_B. The discrete components, R_2, R_3, and D1, provide signal level shifting to interface the operational amplifier to the NAND gates.

Control Logic

The control logic is made up of a CMOS seven-stage binary counter, two CMOS J-K flip-flops, and several discrete parts. CMOS logic is a low-power logic family whose output characteristics are similar to that of a switch. The output is tied to either the logic supply or ground through approximately 500 ohms internal impedance. Therefore, with the reference voltage used as the logic supply, the counter outputs serve as ladder switches. The counter outputs are also connected through series resistors to the inputs of a logic register within the data system. These resistors are required to prevent loading of the ladder when the data system is off. If the register was included within the monitor, these

resistors would not be required. The seven-stage counter and flip-flop 2 make up the eight-bit counter. The flip-flop is the least significant bit. Its "J" and "K" inputs are connected to the output of the comparator to control the counting. Ladder legs 1 and 10 are connected to V_R and ground through the remaining flip-flop. The role of the ladder termination resistor and leg 10 are reversed by connecting the termination resistor to V_R. The discrete parts, R_8, R_9, D2, and D3, provide level shifting and input protection for the reset lines.

Oscillator

The oscillator is a CMOS circuit that is available from manufacturers application literature. The oscillator frequency of 50 Hz was chosen to allow ample settling time between each count, minimize power consumption, and permit the monitor to track changes in the battery voltage. To minimize noise on the battery line, the input to the monitor is low-pass filtered with a filter cutoff of approximately 30 Hz.

Voltage Regulator

The reference voltage of 8.192 volts is developed from the battery voltage by a circuit using an LM105 regulator. The reference voltage covers the measurement voltage range 8.192 to 16.352 and gives an even binary count value. It provides 16 millivolts per count at the ladder output or 32 millivolts per count at the monitor input. If the input falls below 11 volts, the regulator operation is impaired. However, the battery is not expected to fall below this value. A sensistor is included in the regulator circuit to improve stability over the expected

temperature range. The reference was found to hold within 3 millivolts under the range + 60 to - 30°C.

TESTING

Testing of the battery monitor was performed in two stages. Preliminary functional tests for the selection of adjustment resistors were performed at the printed-circuit board level. System tests were incorporated into the testing of the larger electronic system in which it was located. The battery monitor has undergone complete pre-flight qualification and flight level testing. The basic test procedure is to supply a known input voltage, reset the device, and read the binary output number after counting ceases. Tests were conducted at temperatures of - 30°C, 25°C, and 60°C and for input voltages in the range of 11 to 16 volts. The quiescent current was 3 milliamperes and the worst-case, during counting, 4 milliamperes. Six units were built and all performed satisfactorily under tests and during DADS integration and environmental checkout.

CONCLUSIONS

A low-power, battery peak charge voltage monitor has been designed, built, and tested for satellite application. It is self-contained and derives its internal power from the input source. It uses standard integrated circuit components, a thin-film resistor network, and several passive components. The device retains the peak voltage reached by the spacecraft battery between interrogations and makes it available to the data system during data transmission. The input voltage is 11 to 16 volts,

with a resolution and accuracy of 32 millivolts. The device has a quiescent current of 3 milliamperes and a worst-case current during counting of 4 milliamperes. The device has performed satisfactorily through subsystem, spacecraft qualification, and pre-flight tests. The device is readily adaptable for use in other systems.
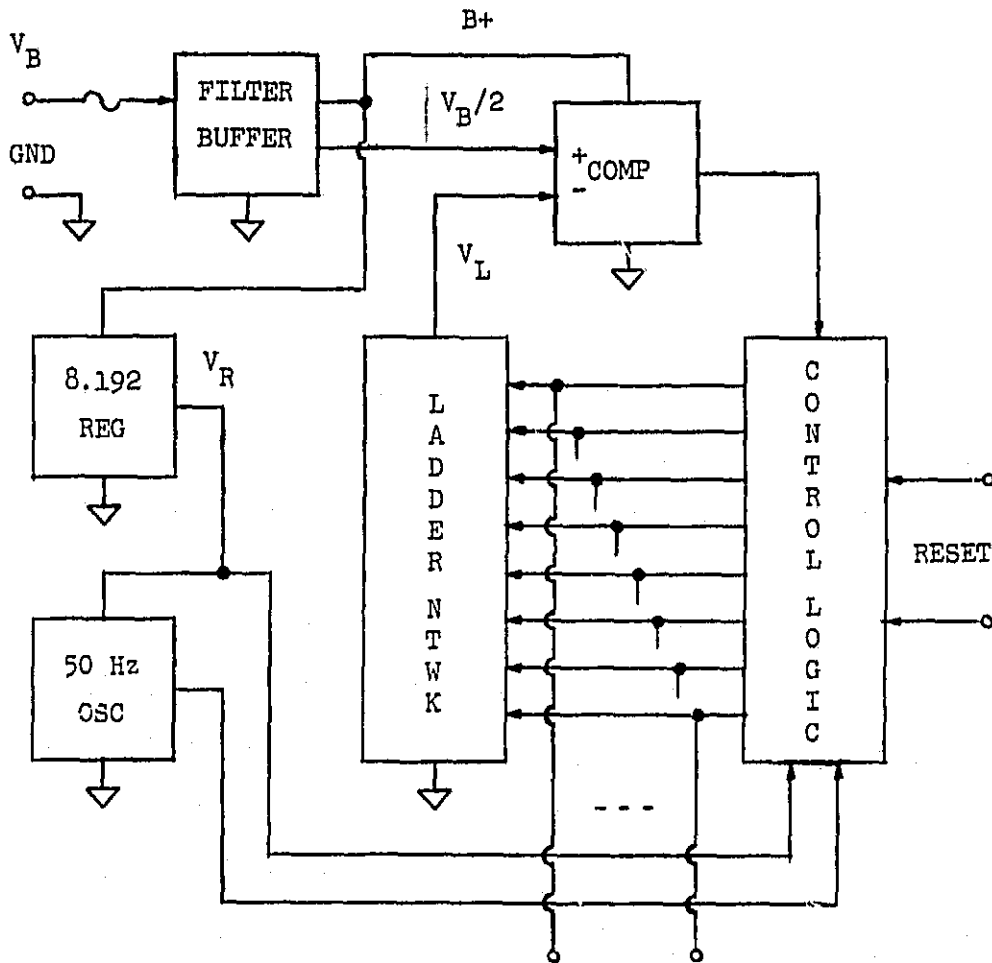
VB

B+

FILTER
BUFFER

VB/2

+
COMP
−

GND

VL

8.192
REG

VR

L
A
D
D
E
R

N
T
W
K

C
O
N
T
R
O
L

L
O
G
I
C

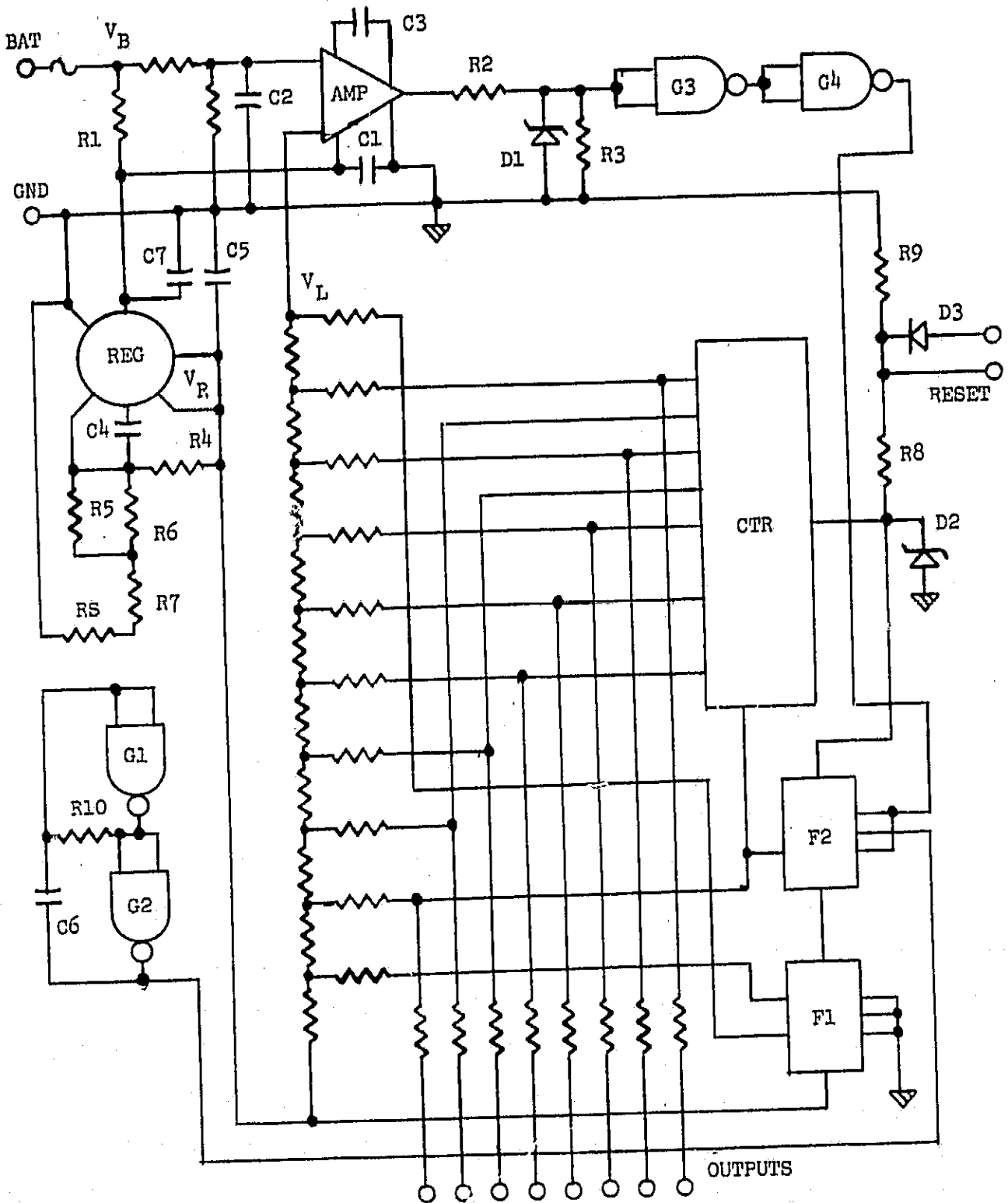RESET

50 Hz
OSC

- - -

Figure 1. − Battery peak charge voltage monitor block diagram.

Figure 2. - Battery peak charge voltage monitor.