https://ntrs.nasa.gov/search.jsp?R=19750025097 2020-03-22T18:45:16+00:00Z

General Disclaimer

One or more of the Following Statements may affect this Document

- This document has been reproduced from the best copy furnished by the organizational source. It is being released in the interest of making available as much information as possible.

- This document may contain data, which exceeds the sheet parameters. It was furnished in this condition by the organizational source and is the best copy available.

- This document may contain tone-on-tone or color graphs, charts and/or pictures, which have been reproduced in black and white.

- This document is paginated as submitted by the original source.

- Portions of this document are not fully legible due to the historical nature of some of the material. However, it is the best reproduction available from the original submission.

Produced by the NASA Center for Aerospace Information (CASI)

NASA CR- 144678

PLATED WIRE RANDOM ACCESS MEMORIES

Lee D. Gouldin
Motorola, Inc.
Government Electronics Division
8201 E. McDowell Road
Scottsdale, Arizona 85252

June 1975
FINAL REPORT FOR PERIOD
June 1974 - June 1975

Prepared for
GODDARD SPACE FLIGHT CENTER
Greenbelt, Maryland 20771

(NASA-CR-144678) PLATED WIRE RANDOM ACCESS MEMORIES Final Report, Jun. 1974 - Jun. 1975 (Motorola, Inc.) 262 p HC $6.25 CSCL 09B

N75-33170

Unclas
G3/19 42710

OCT 1975
RECEIVED
NASA STI FACILITY
INPUT BRANCH

FINAL REPORT

PLATED WIRE RANDOM ACCESS MEMORIES

June 1975
for period
June 1974 - June 1975

Contract No. NAS 5-20576
for
GODDARD SPACE FLIGHT CENTER
Greenbelt, Maryland 20771

Contracting Officer: Hattie Swihart
Technical Officer: William Stewart

Approved by: James Thomas

James Thomas, Manager
Aerospace Data Section

Howard E Parks

Howard Parks, Program Manager

MOTOROLA *Government Electronics Division*
8201 E. McDOWELL ROAD, SCOTTSDALE, ARIZ. 85252

REPORT NO. 4601-400 JOB NO. 75-4619

TOTAL PAGES 218

EFFECTIVE PAGES:

i thru iii
1 thru 34

ATTACHMENTS: PREFACE: Prior to Table of Contents
ATTACHMENT I: ACCEPTANCE TEST PROCEDURE (35 Pages)
ATTACHMENT II: ACCEPTANCE TEST DATA SHEETS S/N 103 (35 Pages)
ATTACHMENT III: ACCEPTANCE TEST DATA SHEETS S/N 104 (35 Pages)
ATTACHMENT IV: ACCEPTANCE TEST DATA SHEETS S/N 105 (35 Pages)
ATTACHMENT V: ACCEPTANCE TEST DATA SHEETS S/N 106 (35 Pages)

REV.	BY	APPROVED	DATE	DESCRIPTION
NC	SLT	See Title Page	6/25/75	Initial Issue

PREFACE

This Final Report documents the work done under NASA Contract NAS-5-20576 by Motorola, Inc., Government Electronics Division for the Goddard Space Flight Center, Greenbelt, Maryland. The work performed under the subject contract entailed the construction and testing of a 4096-words by 18-bits Random Access, NDRO-Plated Wire Memory. Four memory units were delivered to Goddard. This report gives the performance requirements, construction, and test history of the units along with a complete technical and functional description. The report covers the period from June 1974 through June 1975.

TABLE OF CONTENTS

Paragraph	Title	Page
	SECTION 1 INTRODUCTION AND OVERALL PROGRAM SUMMARY	
1.	INTRODUCTION	1
1.1	Program Summary	1
1.2	Results Attained	1
	SECTION 2 HISTORICAL PROGRAM SUMMARY	
2.	PROGRAM HISTORY	4
2.1	Serial Number 103	4
2.2	Serial Number 104	4
2.3	Serial Number 105	5
2.4	Serial Number 106	6
	SECTION 3 TECHNICAL DESCRIPTION	
3.	DESCRIPTION	8
3.1	System Configuration	8
3.2	Electrical Interface	8
3.2.1	Power Source Requirements	13
3.2.2	Thermistor Characteristics	13
3.3	Functional Description	15
3.3.1	Memory Organization	15
3.3.2	Word-Line Selection and Drive	19
3.3.3	Control and Sequencing	19
3.3.4	Write Operation	21
3.3.5	Read Operation	22
3.4	Electrical Parts	22
3.4.1	Logic Circuits	23
3.4.2	Discrete Parts	23
3.4.3	Transformer	24
3.4.4	Sense Amplifier	24
3.4.5	Hybrid Circuits	24
3.5	Mechanical Design	26
3.5.1	Stack Design	26
3.5.2	System Packaging	32
3.5.3	Materials	33

TABLE OF CONTENTS (CONTD)

Paragraph	Title	Page
	SECTION 4 TESTING	
4.	GENERAL	34
4.1	System Level Testing	34
4.2	Memory Stack Testing	34
4.3	Hybrid Circuit Screening	34

ATTACHMENT I: ACCEPTANCE TEST PROCEDURES (35 Pages)

ATTACHMENT II: ACCEPTANCE TEST DATA SHEETS, S/N 103 (35 Pages)

ATTACHMENT III: ACCEPTANCE TEST DATA SHEET, S/N 104 (35 Pages)

ATTACHMENT IV: ACCEPTANCE TEST DATA SHEET, S/N 105 (35 Pages)

ATTACHMENT V: ACCEPTANCE TEST DATA SHEET, S/N 106 (35 Pages)

LIST OF ILLUSTRATIONS

Figure	Title	Page
1	4K x 18 Bit Plated Wire Memory System	7
2	4K x 18 Bit Plated Wire Integral Assembly	7
3	Memory System Electrical Interface	9
4	Overall Functional Block Diagram	16
5	Simplified Memory Drive and Sense Diagram	17
6	Word-Line Selection Matrix	18
7	Sequencer, Logic Diagram	20
8	System Timing, Write Operation	21
9	System Timing, Read Operation	23
10	Four-Channel Sense Amplifier, Functional Diagram	25
11	Delay Circuit, Functional Diagram	26
12	Custom Package and Layout	27
13	Word-Line Selection Matrix, Functional Diagram	28
14	Digit Driver, Functional Diagram	29
15	Power Switch +5V/-6V	30
16	Power Switch +5V/+5V	30
17	Tunnel Structure Construction	32
18	Memory Plane Construction	32

SECTION 1

INTRODUCTION AND OVERALL PROGRAM SUMMARY

1. INTRODUCTION

This Final Engineering Report documents the overall activity and history of the work performed by Motorola Inc., Government Electronics Division, Scottsdale, Arizona for the Goddard Space Flight Center, Greenbelt, Maryland, under NASA Contract No. NAS 5-20576. The report is submitted in accordance with the requirements of Specifications 73-15079 modified June 1974 and the addendum dated May 1974, and covers the period from June 1974 through June 1975.

1.1 PROGRAM SUMMARY

The work performed under the subject contract entailed the construction and testing of a 4096-word by 18-bit Random Access, NDRO-Plated Wire Memory.

The primary design parameters, in order of importance, were:

- High reliability
- Low power
- Volume
- Weight

Four memory units, serial no. 103, 104, 105, and 106 were delivered.

1.2 RESULTS ATTAINED

The memory units were subjected to comprehensive functional and environmental testing at the end-item level to verify comformance with the specified requirements.

A comparison of the memory unit's most significant physical and performance characteristics versus the specified requirements is shown in Table 1.

Table 1. Memory Performance Versus Specified Requirements

Characteristic	Contract Reference	Specified	Measured
Volume	73-15079	160 in^3	158.5 in^3
Weight	73-15079 Mod 6/20/74	5.8 Pounds	5.640 pounds (SN103) 5.562 pounds (SN104) 5.594 pounds (SN105) 5.580 pounds (SN106)
Power Operate	73-15079 Mod 6/20/74	7 watts	5.963 watts max (SN103) 5.914 watts max (SN104) 5.324 watts max (SN105) 5.687 watts max (SN106)
Power Standby	73-15079	170 milliwatts	149 milliwatts max (SN103) 147-milliwatts max (SN104) 139 milliwatts max (SN105) 147 milliwatts max (SN106)
Voltage Tolerance	73-15079	±5% on all	±5% on all
Operating Rate	73-15079	500 kHz	600 kHz
Access Time	73-15079	500 nanoseconds	<500 nanoseconds
Operating Temp.	73-15079	-40°C to +85°C	Tested from -40°C to +85°C
Operating Vacuum	73-15079 Mod 6/20/74	One atm. to 10^{-5} mm Hg modified for test purposes.	Tested from one atm. to 10^{-5} mm Hg.

Table 1. Memory Performance Versus Specified Requirements (Contd)

Characteristic	Contract Reference	Specified	Measured
Operating Vibration	73-15079 Mod 6/20/74	Sinusoidal 5.25 Hz-.33 in da 25-110 Hz-10g Peak 110-2000 Hz-5g Peak Two octaves/ minute Random 15 Hz, .0004 g^2/Hz 15-70 Hz, Linear Increase 70-100 Hz, 0.138 g^2/Hz 100-400 Hz Linear Decrease 400-2000 Hz, 0.0089 g^2/Hz Two min/axis	Tested at specified levels
Operating Shock	73-15079	Two shock pulses of 30g for 6 and 12 milliseconds in three axis	Tested at specified levels

SECTION 2

HISTORICAL PROGRAM SUMMARY

2. PROGRAM HISTORY

The design modification, construction, and test history, as related to the hardware requirements of this contract, is summarized in this section.

Four low-power random access spacecraft memories were constructed, tested, and delivered under this contract. The memories were constructed using the same basic design as units SN101 and SN102, previously delivered under contract no. NAS5-23163, with slight modifications. The word current generator was changed from a hybrid circuit to a discrete circuit which required a new layout of the timing and control board. The housing material was changed from aluminum to magnesium and the mu-metal magnetic shielding was removed to reduce the overall weight of each unit.

The initial contract was for three memory units with an option for two follow-on units. On 9/23/74 the contract was modified to exercise the option on the fourth memory unit and revise delivery schedule due to repair of a memory unit previously delivered under contract no. NAS 5-23163 which had been subjected to over temperature at GSFC.

The summarization is in chronological order from date of contract award to date of final delivery of the memory units.

2.1 SERIAL NUMBER 103

Assembly was completed and system testing began in January 1975. On 2/6/75 GSFC reported they had found a wire bond problem while performing construction analysis on the single digit driver hybrid circuits. Construction analysis at Motorola confirmed the problem and traced the cause to contamination of the gold plating on the single digit driver package. New packages were procured, tested for gold purity, and new single digit driver hybrids were constructed. The new single digit driver hybrids were installed in March 1975 and system test resumed.

Several minor design modifications were recommended to GSFC in April 1975 to improve waveform timing tolerances due to capacitance differences with the new Timing and Control board layout and to reduce power consumption. These modifications were approved by GSFC and incorporated in all units.

The unit was acceptance tested and shipped to GSFC on May 13, 1975.

2.2 SERIAL NUMBER 104

Assembly was completed and system testing began in April 1975. Due to bit errors during stack test and system test Serial Number 105 advanced ahead of SN104. Acceptance testing was completed on June 9, 1975 and shipped to GSFC.

2.3 SERIAL NUMBER 105

Assembly was completed and system testing began in May 1975. During acceptance test three failures occurred. GSFC Malfunction Reports were written and submitted to GSFC.

The first failure was a marginal level bit error which occurred during worst case pattern testing at -40°C and was corrected by replacing a wire pair. Reference GSFC MRF No. D07898.

The second failure was again a marginal level bit error which occurred during worst case pattern testing. This error occurred during the intermediate temperature test after the -40°C testing had been completed. The error was corrected by replacing a wire pair. Reference GSFC MRF No. D07899.

The third failure also occurred at cold temperature. This time a complete digit pair was bad due to a film of flux on one of the connector pins. Reference GSFC MRF No. D078900. The connector pins were cleaned and the unit confidence tested at cold temperature. Temperature testing per the acceptance test procedure was repeated and the unit shipped to GSFC on May 30, 1975.

2.4 SERIAL NUMBER 106

Assembly was completed and system testing began in May 1975. The unit failed cold temperature test due to an unsoldered pin on I/C U5 on the Timing and Control Board. GSFC Malfunction Report No. D09085 was written and submitted to GSFC. Acceptance testing was completed and the unit was shipped to GSFC on June 26, 1975.

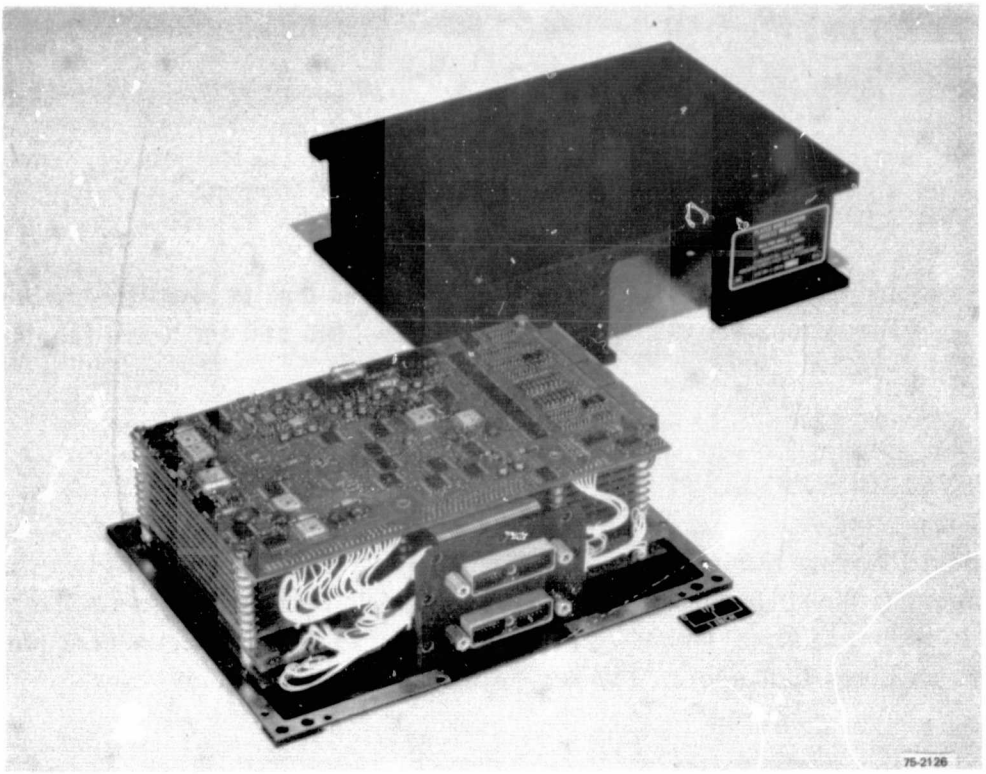


Figure 1. 4K x 18 Bit Plated Wire Memory System

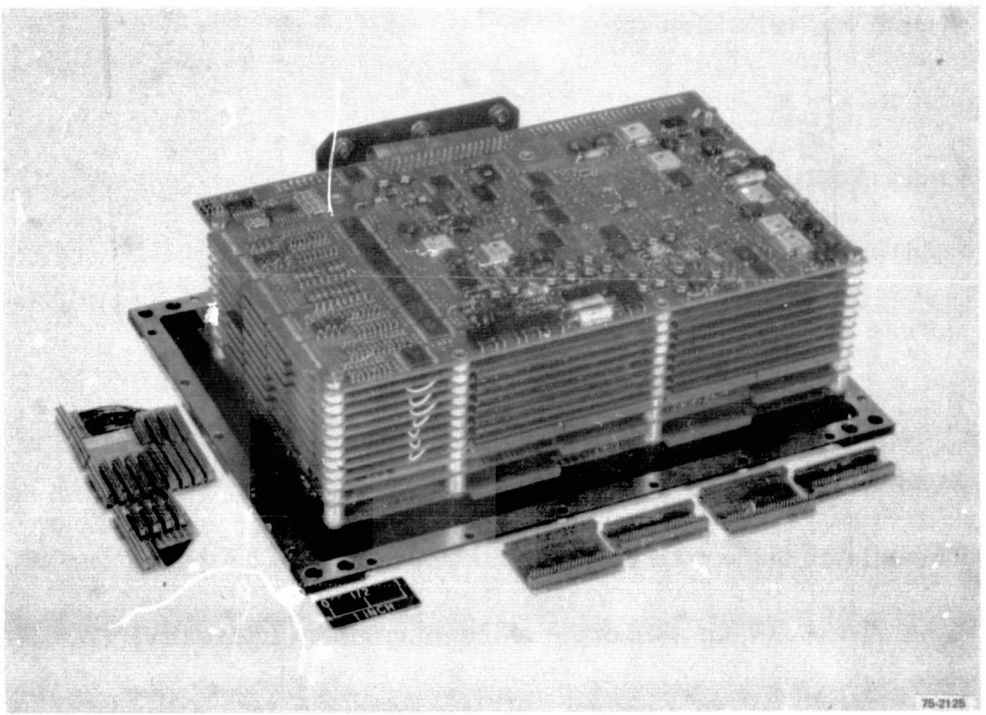


Figure 2. 4K x 18 Bit Plated Wire Integral Assembly

SECTION 3

TECHNICAL DESCRIPTION

3. DESCRIPTION

The memory unit is shown in Figures 1 and 2. The unit is identified as Motorola Part Number 01-P13701D002. Serial Numbers 103, 104, 105 and 106 were fabricated, tested & delivered.

3.1 SYSTEM CONFIGURATION

Motorola Drawing Numbers 01-P13701D, 15-P13745D, and 15-13746D (included in the engineering drawing package submitted to GSFC) completely define the end-item package in terms of size, mounting pattern, etc. The external connector pin assignments are as given in Table 2. The weight of each delivered unit was <5.8 pounds.

3.2 ELECTRICAL INTERFACE

Connectors J1 and J2 are Deutsch, Type 75020-442P, as modified and supplied by GSFC. The total memory interface is comprised of the following (Refer to Figure 3 Memory System Electrical Interface):

- 18 Input Data Lines (to memory)
- 16 Input Address Lines (to memory)
- 18 Output Data Lines (from memory)
- 1 Initiate Line (to memory)
- 1 Read/Write Select Line (to memory)
- 1 Read Complete Line (from memory)
- 2 Thermistor Sensor Lines (from memory)
- 7 Lines for -6.1V (to memory - all lines common internally)
- 5 Lines for +5.0V (to memory - all lines common internally)
- 12 Lines for Power and Signal Return (all lines common internally)

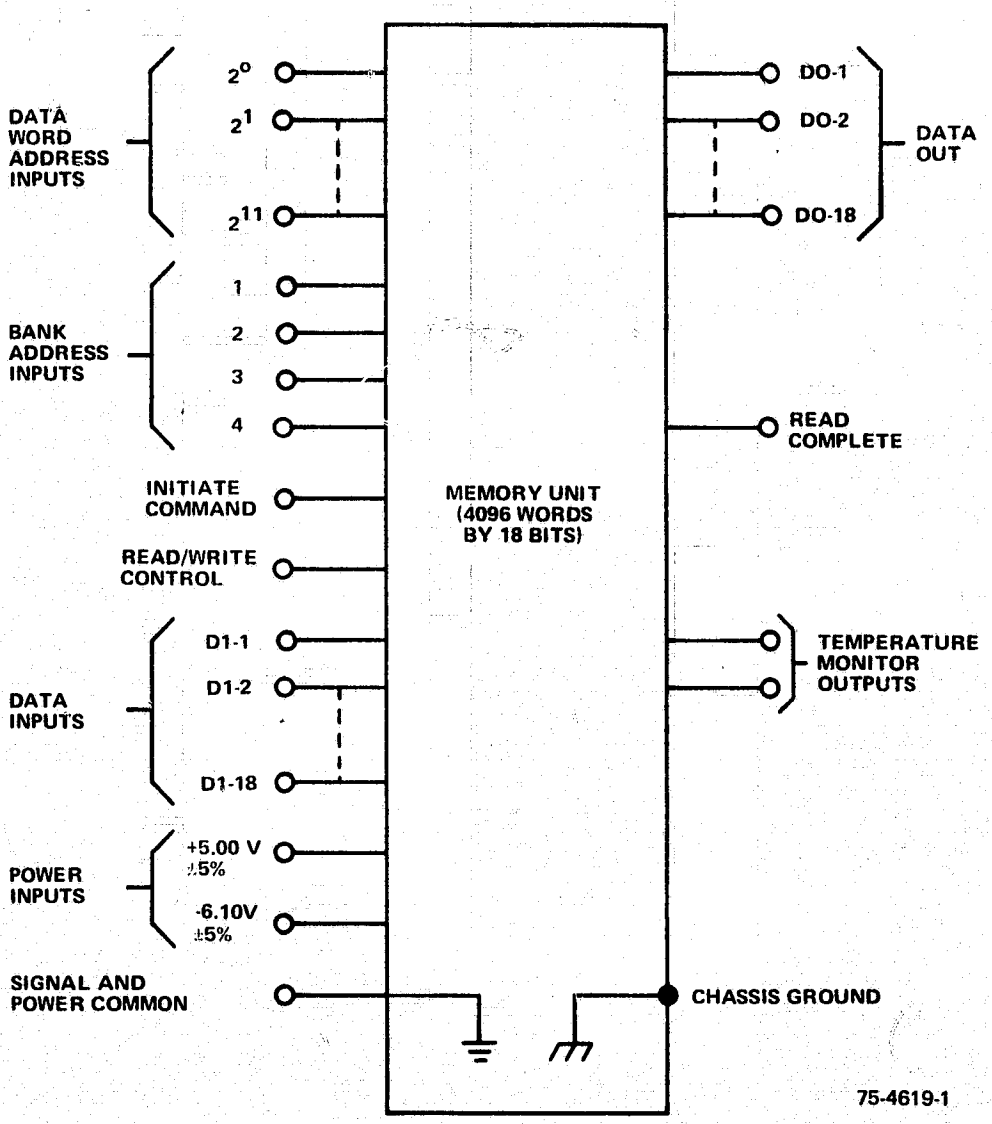


Figure 3. Memory System Electrical Interface

All signal inputs and outputs are to, or from, TTL Series 54 Standard logic devices. All inputs present one unit load. There is no internal loading on any of the output signal lines. The 18 data output lines and the read complete line are driven from open collector logic elements whose output transistor is normally in the OFF state.

The electrical interface characteristics of the delivered unit are as follows. On all signal inputs, a logic ONE is defined as the most positive voltage level, with respect to the return. On all signal outputs, a logic ONE is defined as the high impedance state. All time relationships are defined from the 50 percent points of the respective signals. Transition times (where applicable) are as specified for TTL Series 54 Standard logic with loading as applied. Stability is defined as being above the minimum logic ONE level or below the maximum logic ZERO level.

Memory Capacity: 4096 words of 18 bits each (73,728 bits total).

Access: Random by word via 12-bit input address. Also provides for addressing by memory unit via four-bit bank address. All bank address bits must be at a logic ONE for access.

Access Time: 500 nanoseconds, maximum, from leading edge of Initiate signal.

Read Cycle Time: 1.20 microseconds, maximum, from leading edge of Initiate signal.

Write Cycle Time: 1.00 microseconds, maximum, from leading edge of Initiate signal.

Operate Rate: 0 to 600k operations per second, minimum, with any read/write ratio.

Initiate Signal: Active level = logic ONE. Minimum pulse width = 50 nanoseconds. Maximum pulse width = 450 nanoseconds.

Read/Write Select: Read = logic ONE. Write = logic ZERO. Must be stable from leading edge of Initiate signal to end of read or write cycle.

Bank Address Lines: Must be stable from leading edge of Initiate pulse to end of Read or Write cycle.

Word Address Lines: Must be stable from leading edge of Initiate to end of cycle time.

Table 2. External Connector Pin Assignments

Pin No.	Function	Pin No.	Function
J1-1A	Address Bit 2^0	J2-1A	Data Input Bit 2^0
-1B	Address Bit 2^1	-1B	Data Input Bit 2^1
-1C	Address Bit 2^2	-1C	Data Input Bit 2^2
-1D	Address Bit 2^3	-1D	Data Input Bit 2^3
-1E	Address Bit 2^4	-1E	Data Input Bit 2^4
-1F	Address Bit 2^5	-1F	Data Input Bit 2^5
-1G	Address Bit 2^6	-1G	Data Input Bit 2^6
-1H	Return	-1H	Data Input Bit 2^7
-1J	Read/Write Control	-1J	Data Input Bit 2^8
-1K	Return	-1K	Data Input Bit 2^9
-1L	Return	-1L	Data Input Bit 2^{10}
-1M	Return	-1M	Data Input Bit 2^{11}
-1N	Initiate Command	-1N	Data Input Bit 2^{12}
-1P	Not Assigned	-1P	Data Input Bit 2^{13}
-2A	Address Bit 2^7	-2A	Data Input Bit 2^{14}
-2B	Address Bit 2^8	-2B	Data Input Bit 2^{15}
-2C	Address Bit 2^9	-2C	Data Input Bit 2^{16}
-2D	Address Bit 2^{10}	-2D	Data Input Bit 2^{17}
-2E	Address Bit 2^{11}	-2E	Data Output Bit 2^0
-2F	Bank Address Bit 0	-2F	Data Output Bit 2^1
-2G	Bank Address Bit 1	-2G	Data Output Bit 2^2
-2H	-6.1V	-2H	Data Output Bit 2^3
-2J	-6.1V	-2J	Data Output Bit 2^4
-2K	-6.1V	-2K	Data Output Bit 2^5
-2L	-6.1V	-2L	Data Output Bit 2^6
-2M	-6.1V	-2M	Data Output Bit 2^7
-2N	-6.1V	-2N	Data Output Bit 2^8

Table 2 External Connector Pin Assignments (Contd)

Pin No.	Function	Pin No.	Function
J1-2P	-6.1V	J2-2P	Data Output Bit 2^9
-3A	Bank Address Bit 2	-3A	Data Output Bit 2^{10}
-3B	Bank Address Bit 3	-3B	Data Output Bit 2^{11}
-3C	+5.0V	-3C	Data Output Bit 2^{12}
-3D	+5.0V	-3D	Data Output Bit 2^{13}
-3E	+5.0V	-3E	Data Output Bit 2^{14}
-3F	+5.0V	-3F	Data Output Bit 2^{15}
-3G	+5.0V	-3G	Data Output Bit 2^{16}
-3H	Thermistor	-3H	Data Output Bit 2^{17}
-3J	Thermistor	-3J	Return
-3K	Read Complete	-3K	Return
-3L	Return	-3L	Return
-3M	Return	-3M	Return
-3N	Not Assigned	-3N	Return
-3P	Not Assigned	-3P	Return

Input Date Lines: For write operations, must be stable from leading edge of Initiate to end of cycle time. For read operations, may be any level within TTL logic limits.

Read Complete Line: Presents high impedance (20k minimum) in quiescent state. Goes active (i.e. low impedance) at end of access time (maximum of 500 nanoseconds following leading edge of Initiate signal). Remains at active level for minimum of 250 nanoseconds and maximum of 450 nanoseconds. Will sink minimum of 10 mA at 0.3V in active state.

Data Output Lines: Presents high impedance state (20k minimum) in quiescent state. Goes active (i.e. low impedance) prior to or in coincidence with the leading edge of Read Complete signal and remains active for minimum of 150 nanoseconds following trailing edge of Read Complete signal and maximum of 750 nanoseconds. Will sink minimum of 10 mA at 0.3 V in active state.

3.2.1 Power Source Requirements

The memory unit operates from power sources of +5.0V and -6.1V. Requirements imposed on these power sources by the memory are as follow (all measurements made at connector terminals):

+5.0V:

Regulation: ±5%

Average Standby Current: 12.2 mA, worst-case.

Average Operate Current: 795 mA, worst-case at operate rate of 500k operations per second and read/write ratio of one.

Standby Power: 64.1 milliwatts maximum at +5.25V.

Operate Power: 4.171 watts, maximum, at +5.25V and at operate rate of 500 kHz with a read/write ratio of one.

-6.1V:

Regulation: ±5%

Average Standby Current: 14.5 mA, worst-case.

Average Operate Current: 280 mA, worst-case at operate rate of 500k operations per second and read/write ratio of one.

Standby Power: 92.8 milliwatts, maximum, at -6.40 volts.

Operate Power: 1.792 watts, maximum, at -6.40 volts and at operate rate of 500 kHz with read/write ratio of one.

3.2.2 Thermistor Characteristics

The thermistor is mounted at the approximate center of the unit. It is a YSI Type 44006 precision element with a nominal impedance of 10k ohms at +25°C. The resistance versus temperature characteristic is given in Table 3.

Table 3. Thermistor Resistance Versus Temperature

RESISTANCE VERSUS TEMPERATURE −80°C to +150°C																							
TEMP°C	RES	TEMP°C	RES	TEMP°C	RES	TEMP°C	RES	TEMP°C	RES	TEMP°C	RES	TEMP°C	RES	TEMP°C	RES
−80	3558K	−50	441.3K	−20	78.91K	+10	18.79K	+40	5592	+70	1990	+100	816.8	+130	376.4
79	3296K	49	414.5K	19	74.91K	11	17.98K	41	5389	71	1928	101	794.6	131	367.4
78	3055K	48	389.4K	18	71.13K	12	17.22K	42	5193	72	1868	102	773.1	132	358.7
77	2833K	47	366.0K	17	67.57K	13	16.49K	43	5006	73	1810	103	752.3	133	350.3
76	2629K	46	344.1K	16	64.20K	14	15.79K	44	4827	74	1754	104	732.1	134	342.0
75	2440K	45	323.7K	15	61.02K	15	15.13K	45	4655	75	1700	105	712.6	135	334.0
74	2266K	44	304.6K	14	58.01K	16	14.50K	46	4489	76	1648	106	693.6	136	326.3
73	2106K	43	286.7K	13	55.17K	17	13.90K	47	4331	77	1598	107	675.3	137	318.7
72	1957K	42	270.0K	12	52.48K	18	13.33K	48	4179	78	1549	108	657.5	138	311.3
71	1821K	41	254.4K	11	49.94K	19	12.79K	49	4033	79	1503	109	640.3	139	304.2
−70	1694K	−40	239.8K	−10	47.54K	+20	12.26K	+50	3893	+80	1458	+110	623.5	+140	297.2
69	1577K	39	226.0K	9	45.27K	21	11.77K	51	3758	81	1414	111	607.3	141	290.4
68	1469K	38	213.2K	8	43.11K	22	11.29K	52	3629	82	1372	112	591.6	142	283.8
67	1369K	37	201.1K	7	41.07K	23	10.84K	53	3504	83	1332	113	576.4	143	277.4
66	1276K	36	189.8K	6	39.14K	24	10.41K	54	3385	84	1293	114	561.6	144	271.2
65	1190K	35	179.2K	5	37.31K	25	10.00K	55	3270	85	1255	115	547.3	145	265.1
64	1111K	34	169.3K	4	35.57K	26	9605	56	3160	86	1218	116	533.4	146	259.2
63	1037K	33	160.0K	3	33.93K	27	9227	57	3054	87	1183	117	519.9	147	253.4
62	968.4K	32	151.2K	2	32.37K	28	8867	58	2952	88	1149	118	506.8	148	247.8
61	904.9K	31	143.0K	−1	30.89K	29	8523	59	2854	89	1116	119	494.1	149	242.3
−60	845.9K	−30	135.2K	0	29.49K	+30	8194	+60	2760	+90	1084	+120	481.8	+150	237.0
59	791.1K	29	127.9K	+1	28.15K	31	7880	61	2669	91	1053	121	469.8		
58	740.2K	28	121.1K	2	26.89K	32	7579	62	2582	92	1023	122	458.2		
57	692.8K	27	114.6K	3	25.69K	33	7291	63	2497	93	994.2	123	446.9		
56	648.8K	26	108.6K	4	24.55K	34	7016	64	2417	94	966.3	124	435.9		
55	607.8K	25	102.9K	5	23.46K	35	6752	65	2339	95	939.3	125	425.3		
54	569.6K	24	97.49K	6	22.43K	36	6500	66	2264	96	913.2	126	414.9		
53	534.1K	23	92.43K	7	21.45K	37	6258	67	2191	97	887.9	127	404.9		
52	501.0K	22	87.66K	8	20.52K	38	6026	68	2122	98	863.4	128	395.1		
51	470.1K	21	83.16K	9	19.63K	+39	5805	69	2055	99	839.7	129	385.6		

29-6

ORIGINAL PAGE ■
OF POOR QUALITY

3.3 FUNCTIONAL DESCRIPTION

3.3.1 Memory Organization

The memory is organized into 1024 memory words of 72 bits each (expandable to 96 bits). Each memory word therefore comprises four 18-bit external data words. Figure 4 is a block diagram of the memory organization. The memory stack itself is packaged on eight identical printed wiring, glass-epoxy substrates, with 128 two-turn word lines on each board, for a total of 1024.

Each word-line wraps twice around 144 plated wires, with the corresponding wires in each of the eight boards connected in series. At the far end, each pair of adjacent wires is shorted together, forming seventy-two pairs, with each pair traversing between all 1024 word-lines. The opposite ends of each pair terminate at the input of a differential sense amplifier. The outputs of a bi-directional digit driver current source is also connected to each pair of wires at the same end as the sense terminations. A specific bit storage location is formed at the crossover points of a particular word line and a pair of plated wires.

Using two wires for each bit storage (i.e., two crossovers) allows a differential implementation for information sensing, virtually eliminating common-mode noise problems and increasing the signal outputs at any given word current level, thus permitting operation at lower word currents than would have been required with a single crossover-per-bit implementation.

A memory word consists of the 72 bits under a single word line on a particular memory stack board. A particular data word address uniquely locates an 18-bit data word by identifying a word line and a group of 18 sense amplifier channels or 18 digit driver current sources.

The only electronics packaged as part of the memory stack is associated with word line selection. The rest of the electronics is packaged on three similar board assemblies.

3.3.2 Word-Line Selection and Drive

Figures 5 and 6 show the word current selection and drive method. Word-line addressing is accomplished through a two-level tree of transistor switches. The first level steers the word current to one of 64 unique areas of the stack. The second level steers the word current into one of 16 word lines in the particular word group addressed through the first level. Both levels are packaged on the memory stack boards.

ORIGINAL PAGE IS
OF POOR QUALITY

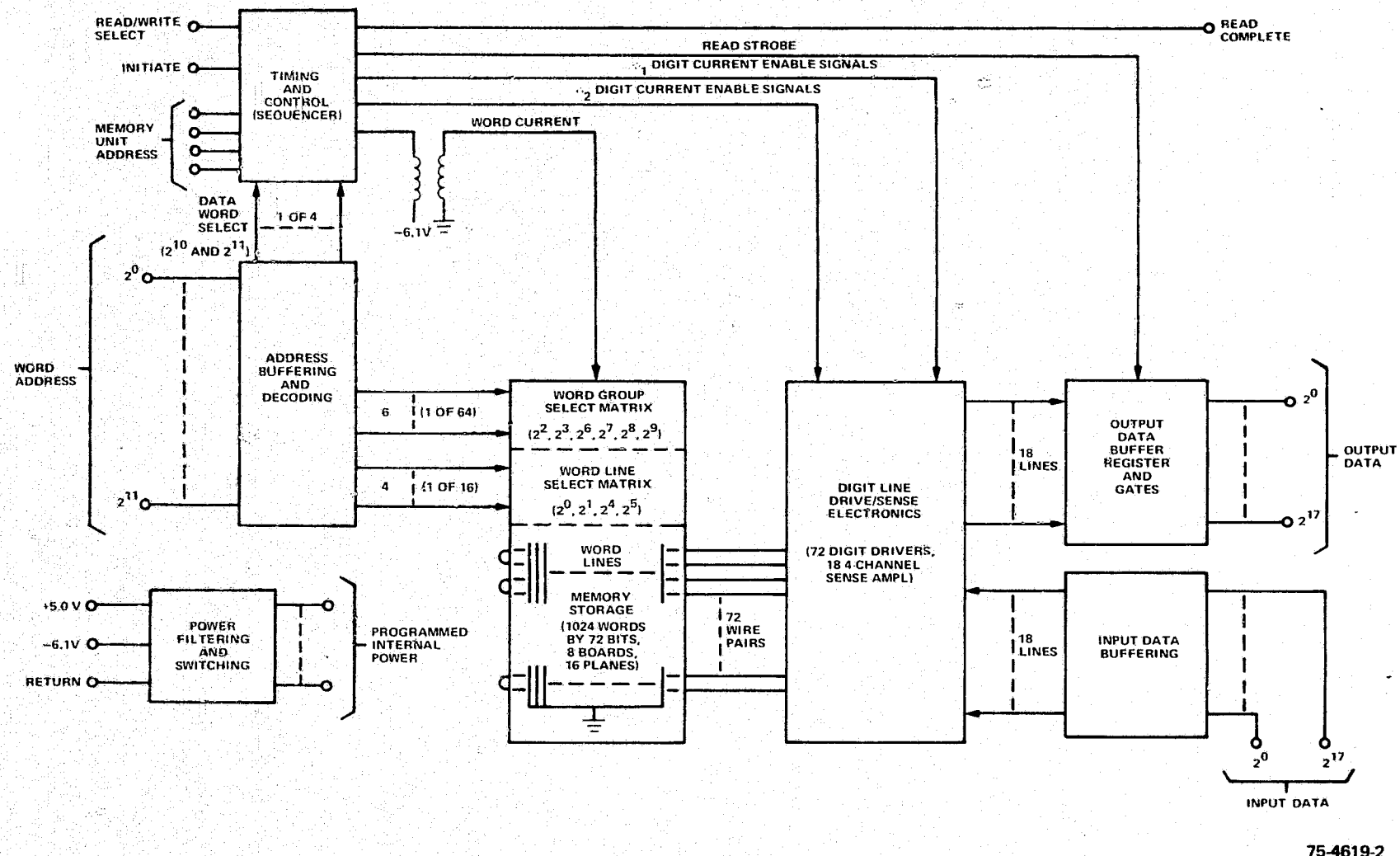


Figure 4. Overall Functional Block Diagram

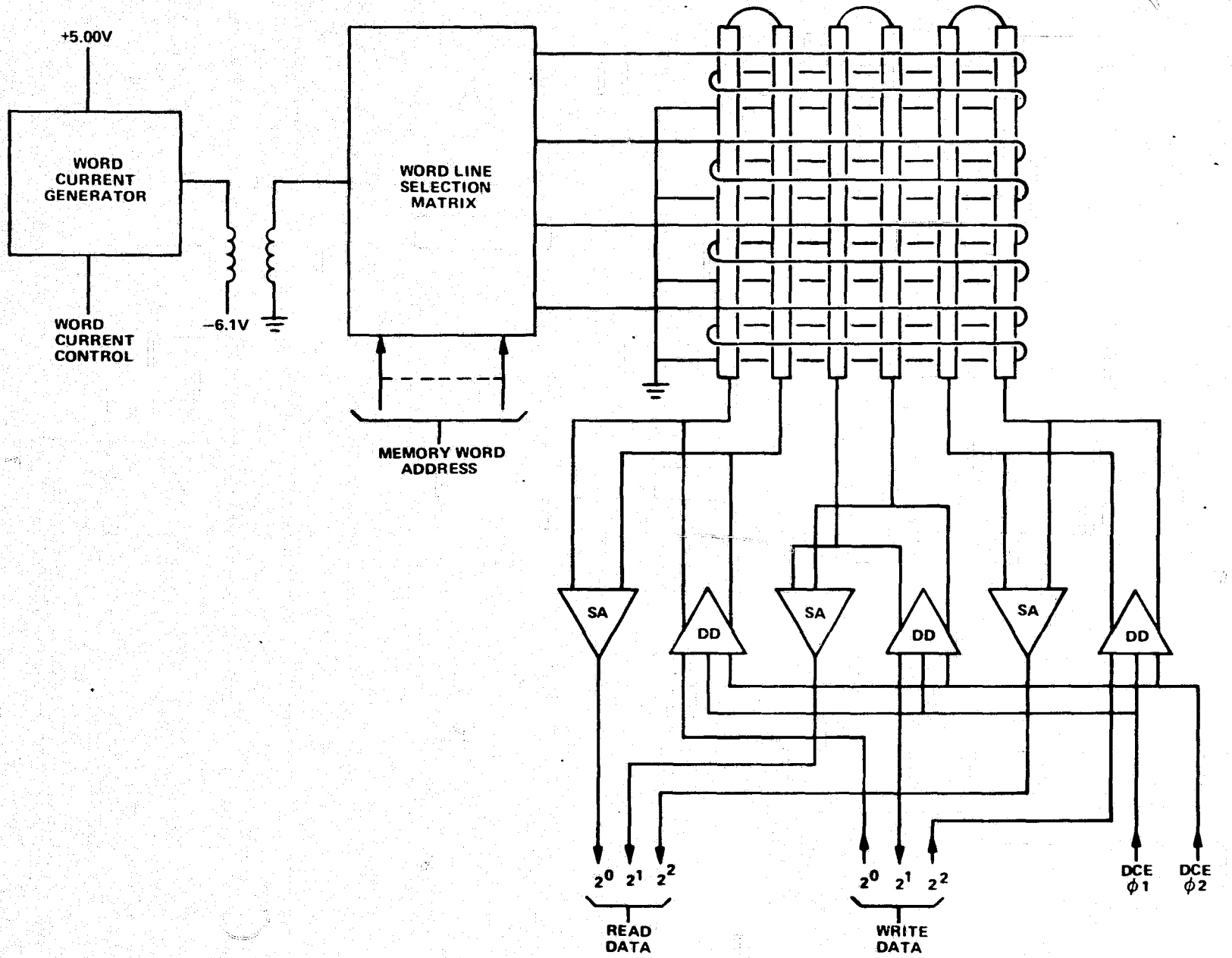


Figure 5. Simplified Memory Drive and Sense Diagram

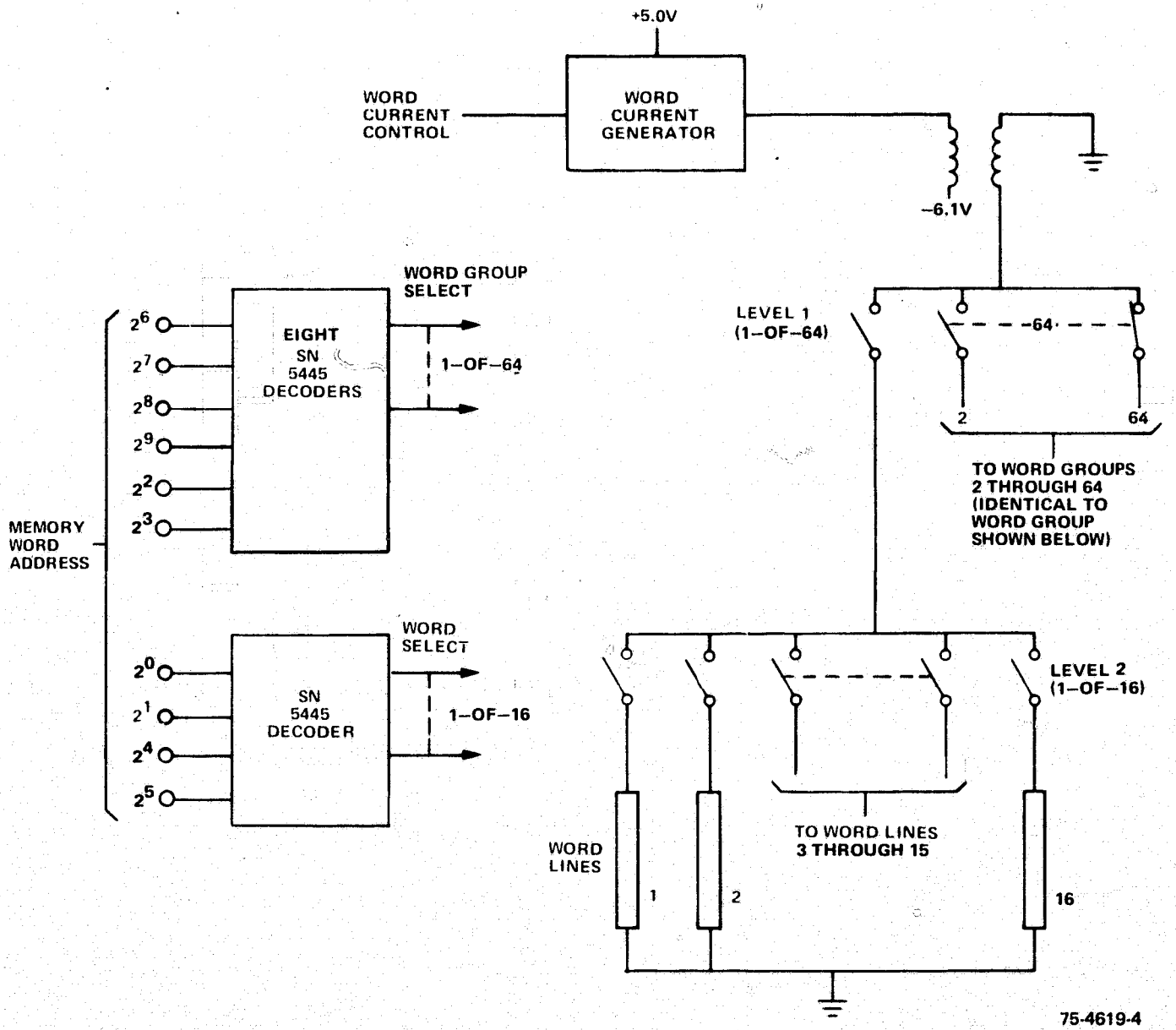


Figure 6. Word-Line Selection Matrix

The data word address is decoded in the sequencer, using SNC 5445 Binary-to-Decimal Decoders. Address bits 2^2, 2^3 and 2^6 through 2^9 are decoded into 1-of-64 and identify the word group. Bits 2^0, 2^1, 2^4 and 2^5 are decoded into 1-of-16 and identify the word line within a group. Bits 2^{10} and 2^{11} identify a particular data word location (1-of-4) along the addressed word line. The apparent anomaly in sequence of the bits allocated for identification of word group and word line is a result of test considerations. With the switching matrix implementation used in the system, the address bit allocation defined above will identify adjacent word lines across a plane when the address sequences in a straight binary code.

Since only one end of each word-line is actively switched (with the opposite end returned to ground) only the addressed word-line has any voltage applied to it (with reference to the quiescent level). Thus, current flow in the stack resulting from charge transfer to/from stray capacitance is minimized and stack charge "restoration" is not necessary. The resulting design is significantly less complex, faster and more noise-free.

A transformer is used for coupling between the word current generator and the word line selection matrix to negate the need for a third, high-voltage power input. The transformer also provides some additional measure of noise reduction.

3.3.3 Control and Sequencing .

The memory design does not use a discrete internal clock. Instead, memory sequences are generated from a series of programmable delays. A diagram of the sequencer logic is shown in Figure 7. Each delay is programmable, independent of any other delay. (The actual programming is accomplished by selection of discrete component values). Thus, timing sequences can be optimized for performance and power consumption.

Power to all but a minimum of control logic is switched off between memory cycles. The delay circuit is designed to come up in a normalized state when power is applied.

When an Initiate signal occurs, the power switch is turned on. If the signal is of longer duration than delay τ_A (approximately 35 nanoseconds), then the Initiate Override signal is actuated, locking the memory in the operate mode until the read or write cycle is completed.

Power to the digit drivers, sense amplifiers, and associated logic is also controlled through the sequencer. The corresponding power switches are physically located on the digit electronics board assemblies.

Delays τ_B through τ_E are activated for a write cycle. Delays τ_B and τ_D set the width of the two phases of digit current and τ_C sets the separation between the two phases. Delay τ_E controls the duration of the word current. The ϕ_1 and ϕ_2 digit current control for one of the four possible data words are activated, depending on the states of address bits 2^{10} and 2^{11}.

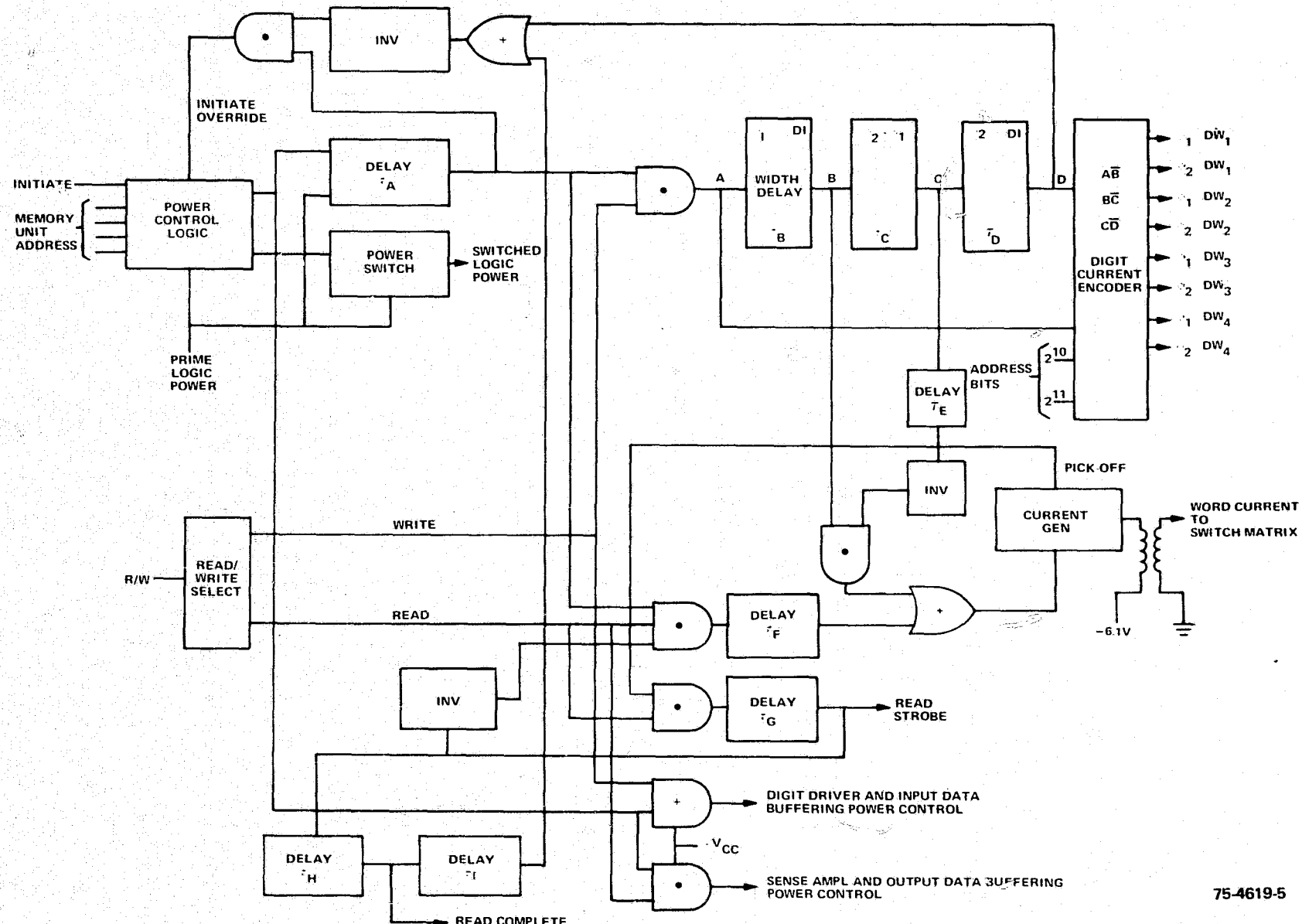


Figure 7. Sequencer, Logic Diagram

Delays τ_F through τ_I are activated during a read cycle. Delay τ_F starts the word current after power start-up transients have had an opportunity to dissipate. A pick-off from the word current level is delayed by τ_G and used as the read strobe, which clocks the sense amplifier outputs into the output data buffer register. Delays τ_H and τ_I set the duration of the read complete and the post-read data hold periods, respectively.

3.3.4 Write Operation

The memory timing for a write cycle is shown in Figure 8. For proper operation, the address, data and read/write control signals must be stable prior to the leading edge of the initiate command and must remain stable until the write cycle has been completed.

When an initiate command pulse occurs in the presence of a low (or ground) level on the read/write control line, power to the sequencer and to the write electronics is turned on. A low impedance path is connected from the word current generator to a particular word line (through the word line selection matrix) as identified by address bits 2^0 through 2^9. A group of 18 digit driver current sources is then energized for ϕ_1 current. The particular current sources are identified by address bits 2^{10} and 2^{11}. The polarity of current (i.e. direction along the plated wire element) from any current source is controlled by the logic level of the data input to that current source. The ϕ_1 digit current is then terminated and ϕ_2 current enabled. The two phases are of equal amplitude and duration. This balanced current implementation precludes any hysteresis build-up due to an unequal history of data "one" and "zero" writes.

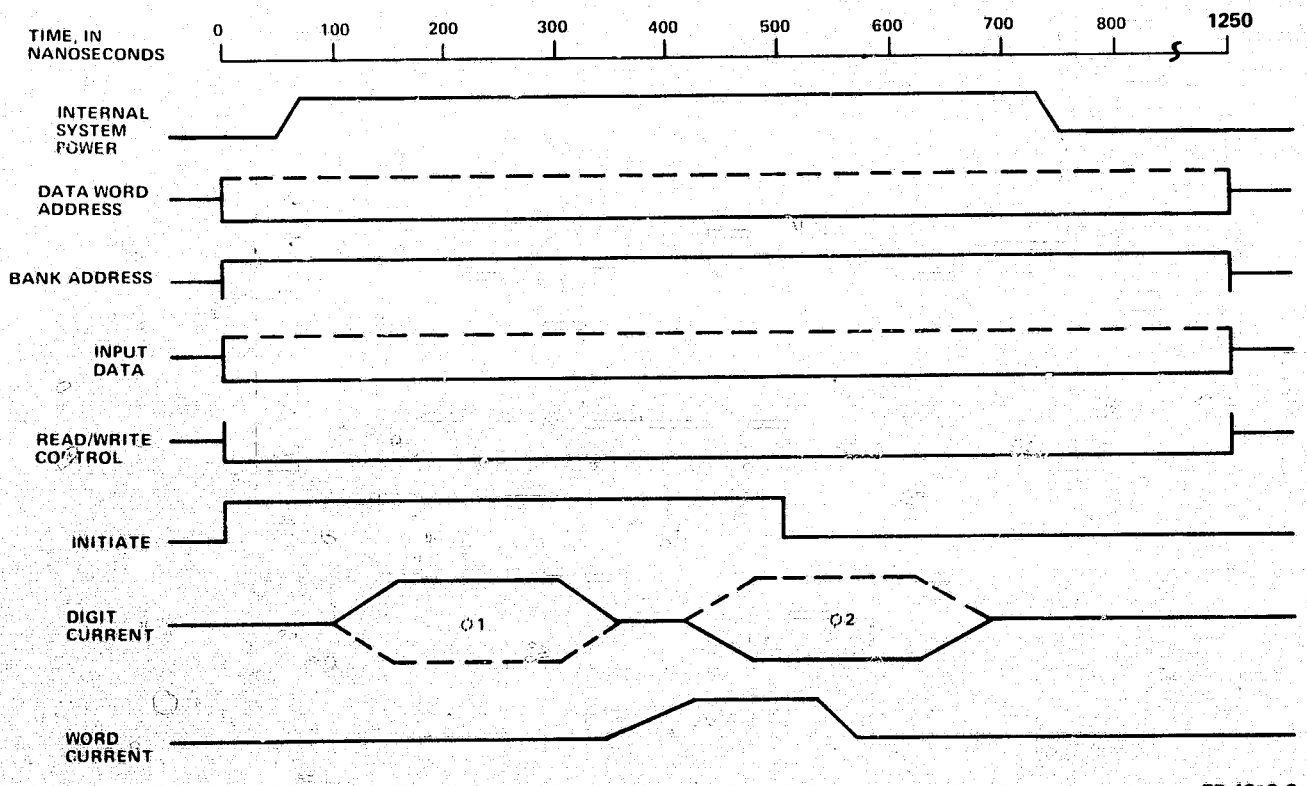


Figure 8. System Timing, Write Operation

The word current generator is energized early enough that the terminating transition of the word current can be made to occur during the time when ϕ_2 digit current is at full amplitude. Data is "written into" the wire when the word current terminates in the presence of digit current.

At the end of the ϕ_2 digit current, the write cycle is complete and internal system power is turned off. A write cycle, from the leading edge of the initiate command to turn-off of system power, requires approximately 750 nanoseconds.

3.3.5 Read Operation

The memory timing for a read cycle is shown in **Figure 9.** For proper operation, the address and read/write control lines must be stable prior to the leading edge of the initiate command and must remain stable until completion of the read cycle.

When the initiate command pulse occurs in coincidence with a high level on the read/write control line, power to the sequencer and the read electronics is turned on. A low impedance path is again connected to the addressed word line through the word line selection matrix. A group of 18 sense amplifier channels are selected, as identified by address bits 2^{10} and 2^{11}.

After any transients generated in the sense amplifiers have had a chance to settle out, the word current generator is energized. Signals are induced in the plated wires during the word current transients and are amplified by the sense amplifiers. The leading edge transient of the word current is controlled to effect the widest useable "window" in the sense amplifier output. The amplifier outputs are used as steering inputs to buffer storage registers. The polarity depends on the state of the information previously "written into" the plated wire.

The information "read out" during the turn-on transient of the word current is clocked into the the buffer register by the strobe. The strobe is generated by a level detector in the current generator. This minimizes possible uncertainties in strobe position.

The read-complete signal is initiated when the data is clocked into the buffer register. It is maintained for a minimum of 250 nanoseconds and a maximum of 450 nanoseconds. Output data is maintained in the buffer register for at least 150 nanoseconds after termination of the read complete signal. At the end of this time the read cycle is complete and internal power is switched off.

The data and read complete sources are Series 54 open collector logic elements. A low impedance (i.e. output transistor on) denotes the active level for the read complete line and a logic zero on the data lines. The only time the low impedance condition will exist on a data line is during the actual read-out of a bit 0.

3.4 ELECTRICAL PARTS

High-Rel, screened parts were used in construction of the memory. Six pieces of each electronic device were submitted to GSFC for evaluation.

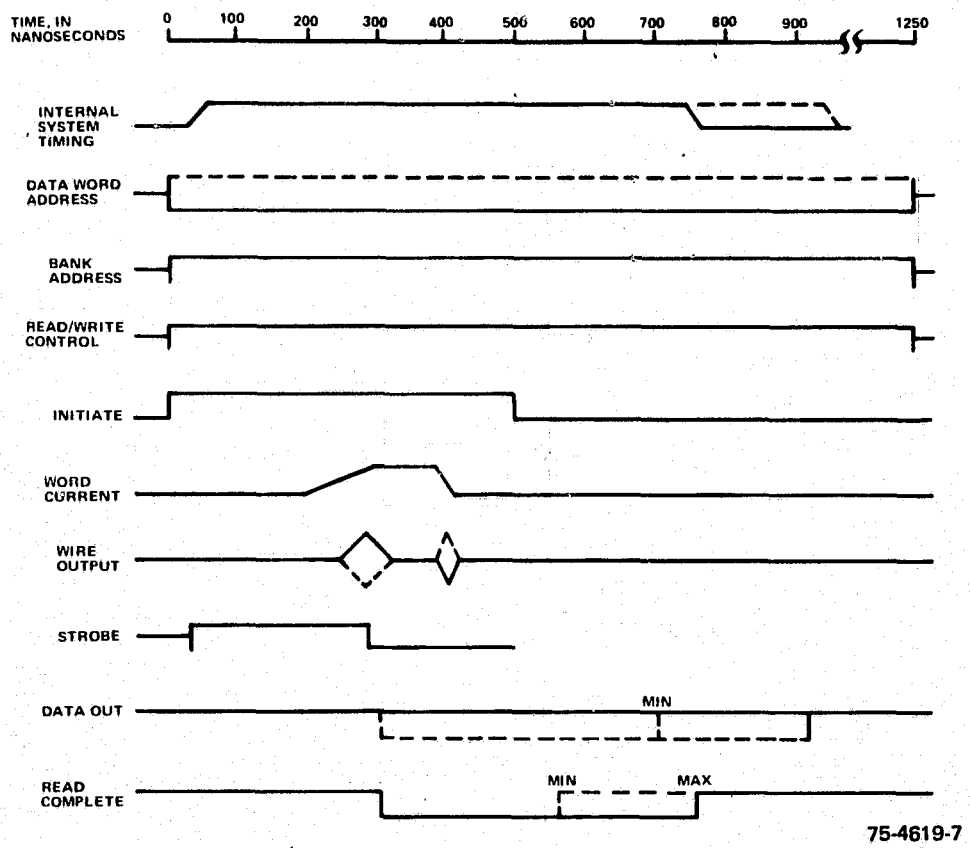


Figure 9. System Timing, Read Operation

3.4.1 Logic Circuits

Series 54 TTL integrated circuit logic elements were used throughout the memory. These were procured per vendor High-Rel specification SNC which is MIL-STD-883, Class B.

3.4.2 Discrete Parts

Two types of established reliability resistors were used in the memory; the RCRXXG Composition and the RNR55C metal film. The RCRXXG were procured to S failure-rate levels and the RNR55C were procured to R failure-rate levels.

Three types of capacitors were used; the CSR 13 style established reliability tantalum with failure rate of R or lower, the CKRO6 style, established reliability ceramic with failure rate of R or lower, and the CM series cap per MIL-C-5/18 with additional screening. Transistors and diodes were either purchased as JAN TX parts or screened to JAN TX equivalent per the documents indicated in the parts control list.

3.4.3 Transformer

A single rf transformer was used in the memory for coupling the word current from the generator to the memory stack. The transformer was fabricated in-house to the requirements of MIL-C-15305, Type LT6K, with temperature cycling per MIL-STD-202, Method 102, Condition C, except 10 cycles at -55°C.

3.4.4 Sense Amplifier

The four-channel sense amplifier (SC 12200 FB2) is shown in Figure 10. The input terminating resistors are external to the package.

3.4.5 Hybrid Circuits

Six different hybrids are used in the memory. These are custom circuits manufactured in-house and screened to meet the requirements of this program. Each of these circuits is described briefly in the following paragraphs.

3.4.5.1 Delay Circuit

The delay circuit is shown, functionally, in Figure 11. Only the high-to-low transition at the input is delayed at the output, with both the true and complement outputs available. The delay is adjustable from a minimum of approximately 25 nanoseconds to a maximum of several microseconds.

3.4.5.2 Word-Line Selection Circuits

The word-line selection circuits are shown in Figures 12 and 13. A particular switch is closed by grounding the corresponding selection input. The first and second level switches are packaged together. A particular package contains one first level switch and two banks of four second level switches each. Each of four second level selection inputs controls one switch in each bank. A single selection input controls the first level switch. The pin-outs are configured so that a first level switch can be connected to a second level bank in a different package, as well as to a bank in its own package.

3.4.5.3 Digit Driver

The digit driver is shown in Figure 14. Basically, it consists of two current sources with steering such that, depending on the logic inputs, one of the sources may be enabled to conduct current through the load in a particular direction. The T1 and T2 inputs denote successive time periods for the two opposite phases of digit current. The D and $\overline{D}$ inputs denote the true and complement levels of an input data bit. If D is true, then current will flow in the direction indicated during T1 and in the opposite direction during T2. The current flow would be opposite if $\overline{D}$ were true.

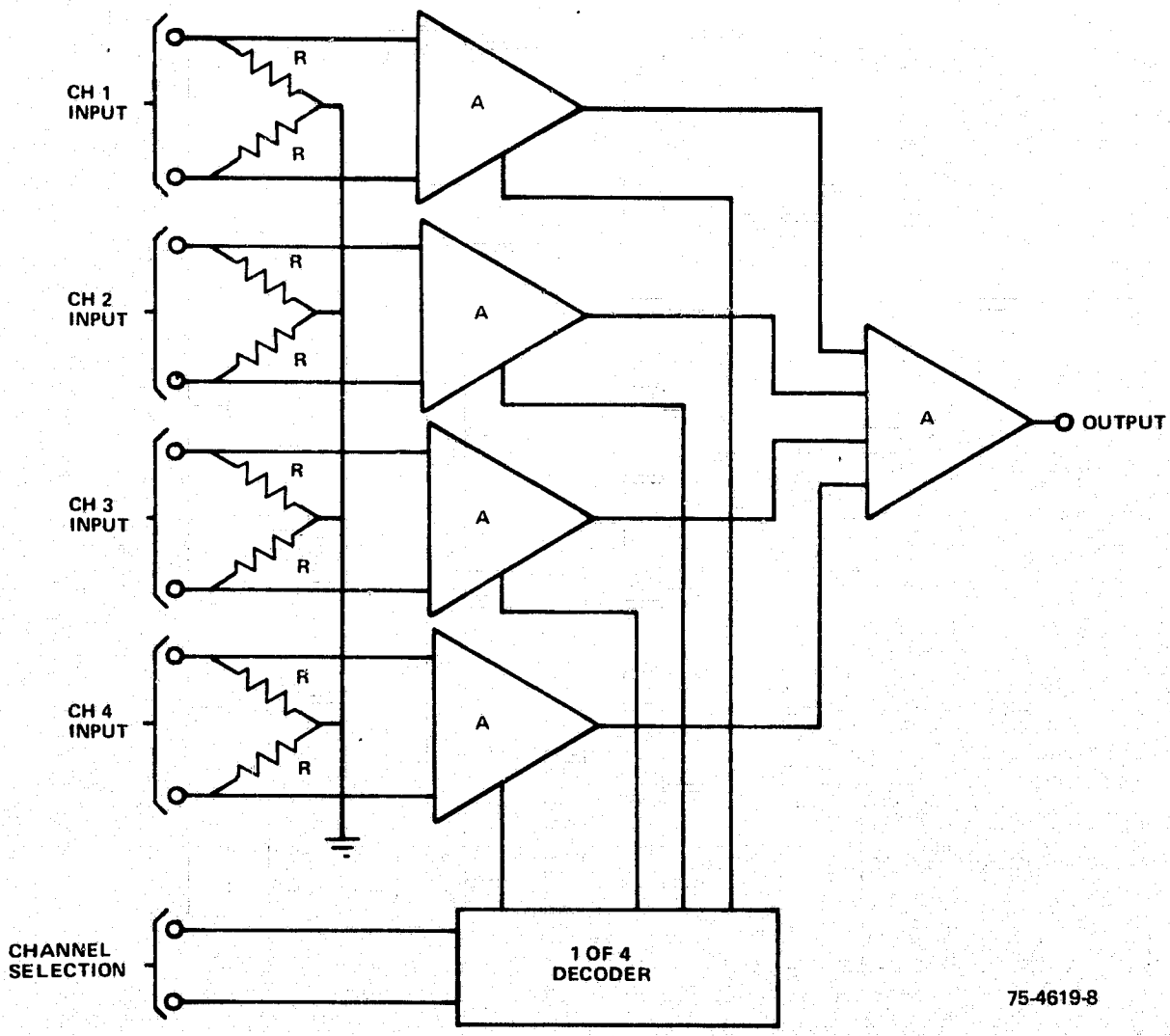


Figure 10. Four-Channel Sense Amplifier, Functional Diagram

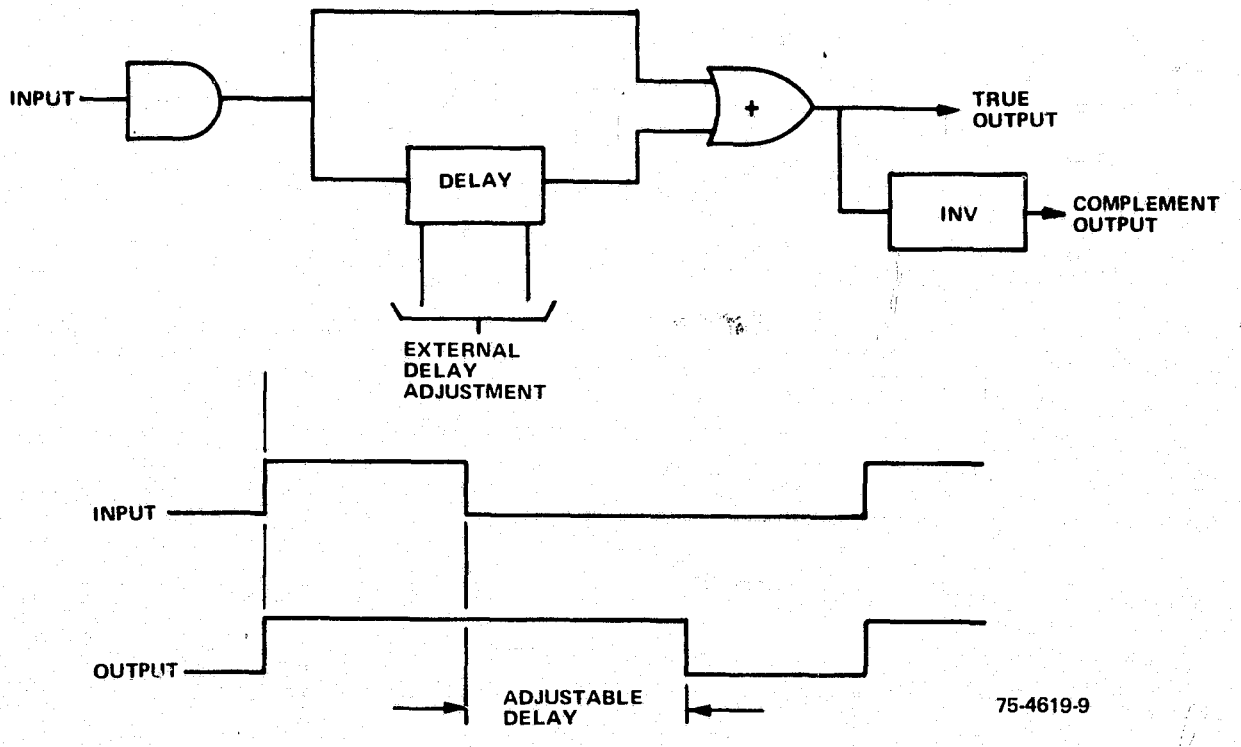


Figure 11. Delay Circuit, Functional Diagram

3.4.5.4 Power Switches

Two types of power switches are used in the memory. One type provides two independently controlled logic level (i.e., +5.0 V) outputs from the primary +5 V input. The other type provides two sets of +5.0 V and -6.1 V outputs from the corresponding inputs. Each set is controlled independently. The switches themselves consume no power when in the OFF state. The switches perform no regulation. They are shown functionally in Figures 15 and 16.

3.5 MECHANICAL DESIGN

3.5.1 Stack Design

The plated wire memory stack used in the LP RASM used a standard Motorola plane design for spaceborne memories developed to high reliability, quality assurance, and workmanship standards. The primary design goal of the stack was simplicity of fabrication combined with high reliability. The number of solder joints and plated through holes are minimized to accomplish this end. The stack consists of eight planes arranged and interconnected to meet the specific requirements of the LP RASM. Specific details of stack construction are described below.

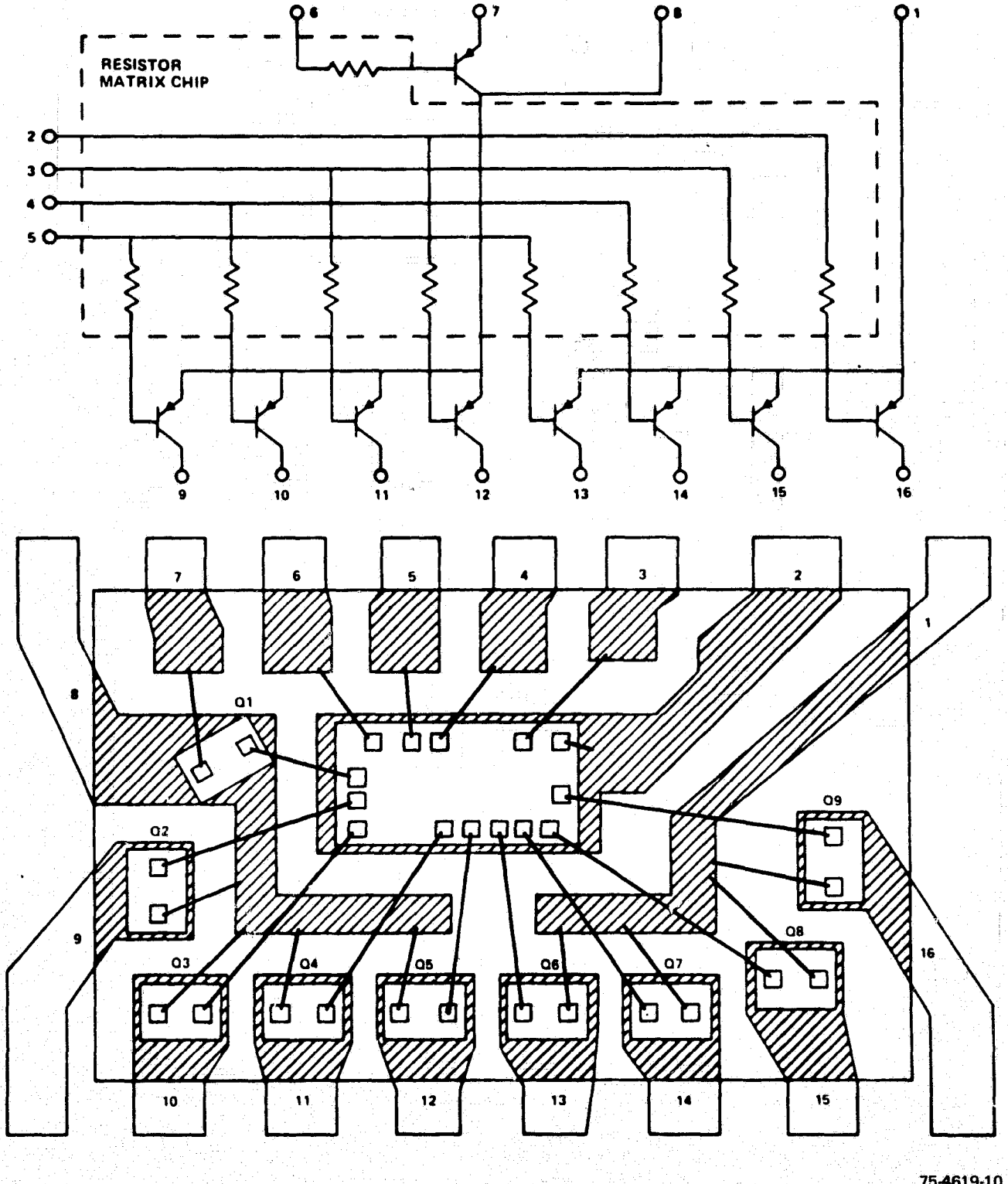


Figure 12. Custom Package and Layout

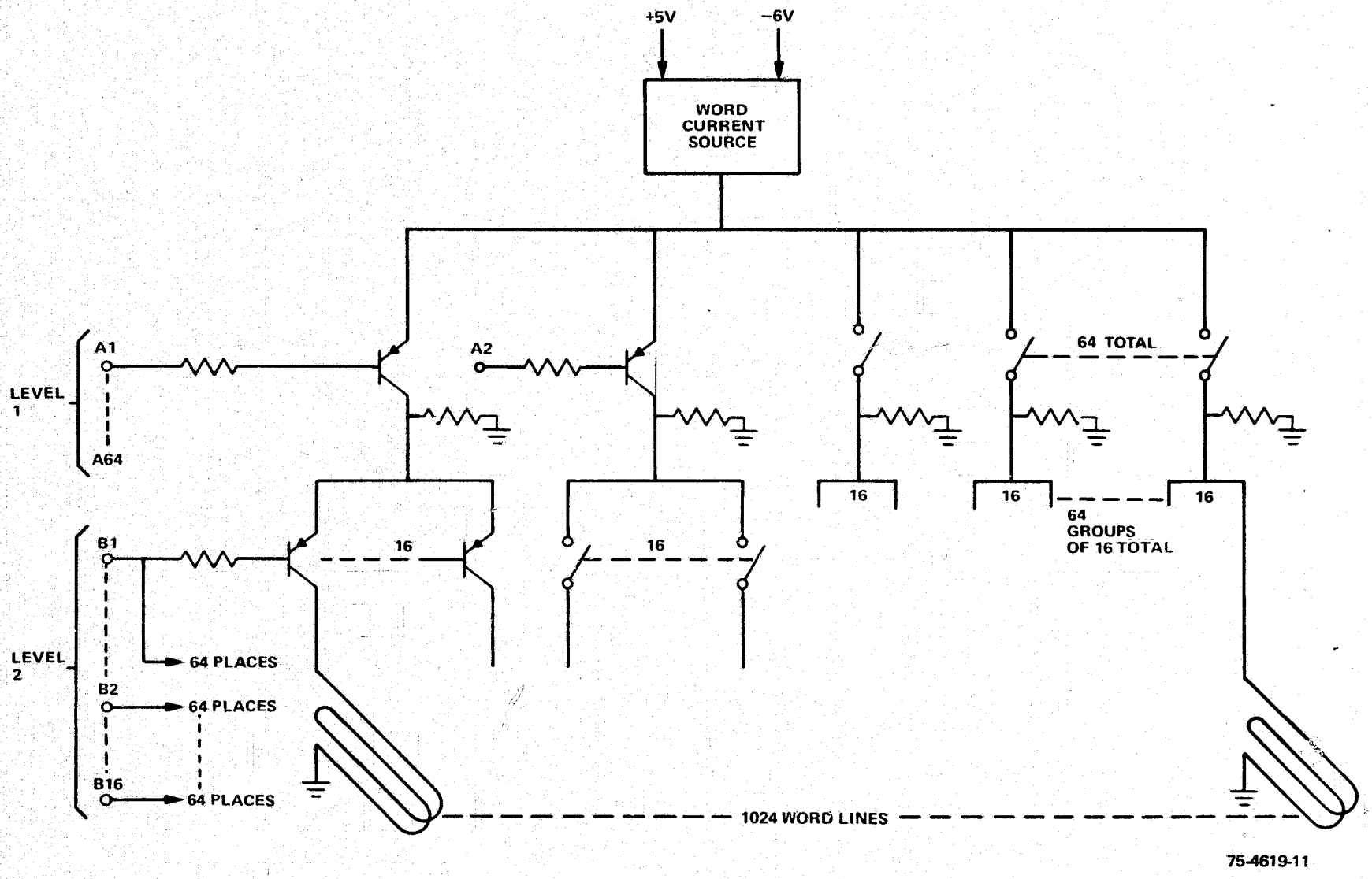


Figure 13. Word-Line Selection Matrix, Functional Diagram

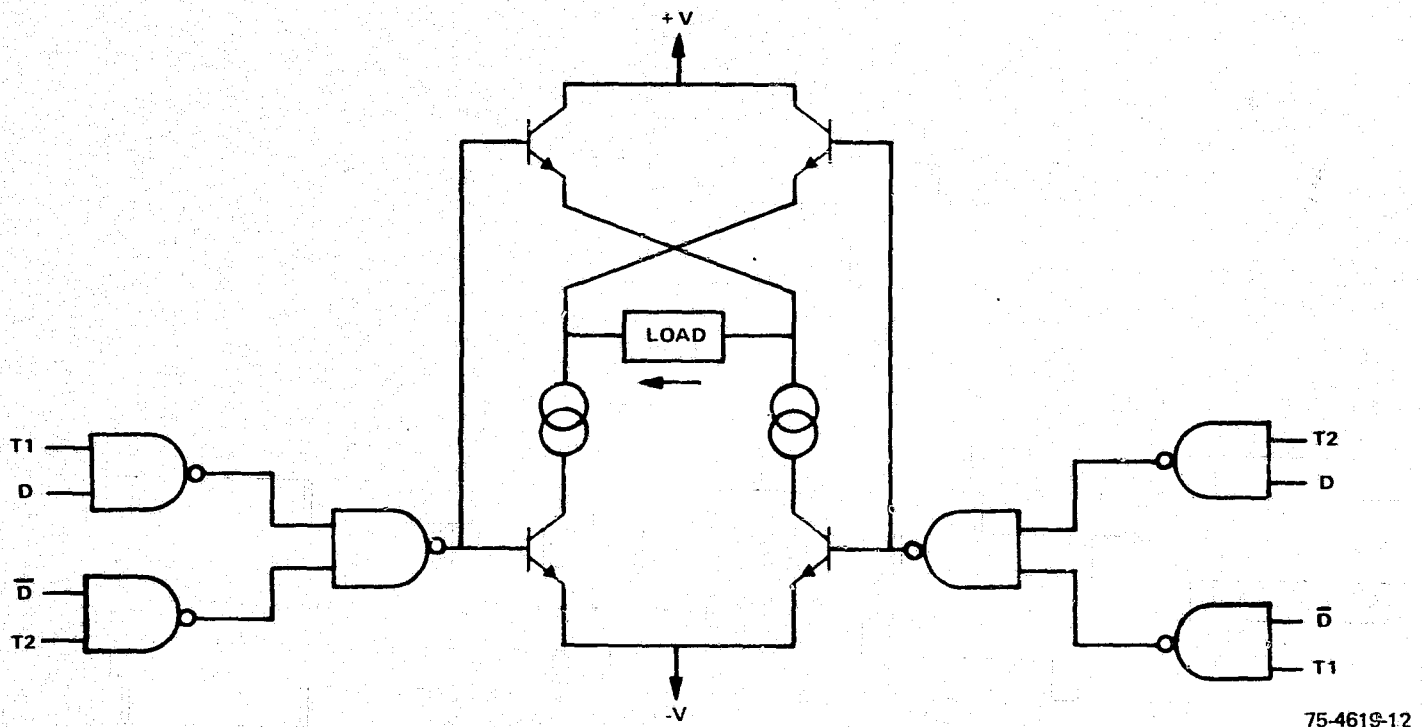


Figure 14. Digit Driver, Functional Diagram

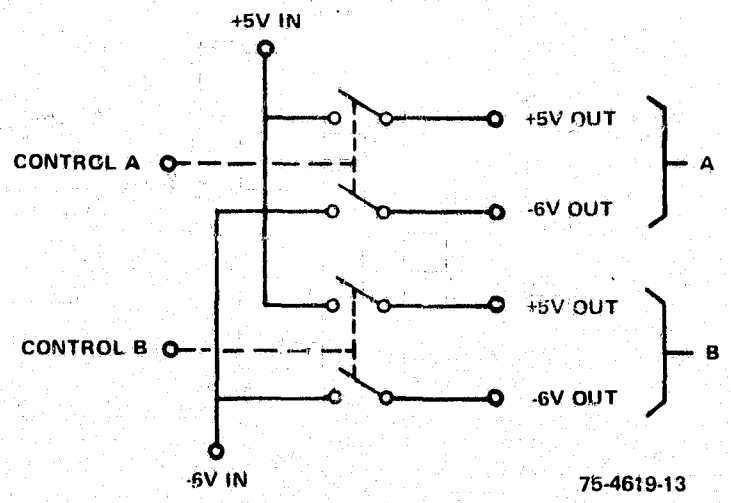


Figure 15. Power Switch +5V/-6V

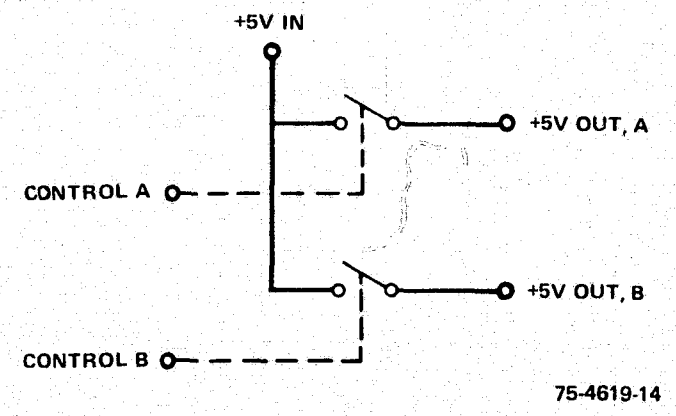


Figure 16. Power Switch +5V/+5V

The tunnel structure, the heart of the memory plane, contains the word lines and the plated wire which stores the bits of data. The plated wires are installed in 0.007 diameter tunnels on 0.025 centers in a polymide-FEP tunnel matt. The tunnel matt is constructed by forming the FEP (between the polyimide film) around dummy wires at controlled temperature, pressure and wire tension. After complete assembly processing the dummy wires are removed and the plated wire is installed in the tunnel.

Word lines of etched copper on glass epoxy board are laminated to each side of the tunnel matt so that they are perpendicular to the tunnels (plated wire). The word lines are double turn (twice around the wires per line). Their mechanical configuration is 0.010 wide conductor, an intervening 0.005 space and another 0.010 conductor, all on repetitive 0.050 centers. Plated-thru holes at each end of the tunnel matt creates the double turn word lines.

Each carrier structure contains 64 word lines and 100 bit lines (Plated wire tunnel pairs). To provide the desired storage capacity for the LP RASM only 72 tunnel pairs are populated (plated wire installed).

Keepers, of high magnetic permeability and processed with extreme care, are bonded to the outer surface of the glass epoxy board which support the word lines to contain the word line field and shield against external magnetic fields. The tunnel matt and word lines are carefully fabricated and then laminated into a subassembly using multilayer printed wiring board techniques. The keepers are then laminated using similar techniques. A cross section of the tunnel structure is shown in Figure 17.

The memory plane is fabricated by laminating two tunnel structures to each side of a motherboard. The motherboard is a two-sided printed wiring board which has a ground plane laminated in the center. The input and return for the matrix is tracked to the edge of the board where pc board interconnect is used to interface with the plane. Two tunnel structures per plane provide 128 word x 72 bit capacity. Installation of the 8 word-drive flat packs per side, by lap soldering, completes the memory plane subassembly. Memory plane construction is shown in Figure 18.

The memory stack consists of eight memory planes electrically and mechanically integrated into one unit to provide 1024 words x 72 bits of storage. The digit lines of each plane are interconnected with flat flexible circuitry bonded to the motherboard which permits the stack to be opened as necessary during assembly and rework. The plated wire is formed like a "hairpin" and installed into the top and bottom carrier structure (similar to a trombone slide). The two ends of the plated wire are lap soldered directly to the conductor of the interconnecting flex cable. This approach for installing the plated wire minimizes the number of solder joints required while providing the required stress relief.

PC board interconnect with miniature connectors (see Figure 2) is used to interconnect common word drive signals from plane to plane and carry all digit and word signals to the electronics. The use of printed circuitry interconnect provides controlled impedance and line characteristics. The connectors allow the stack to be connected/disconnected from the electronics with minimum effort.

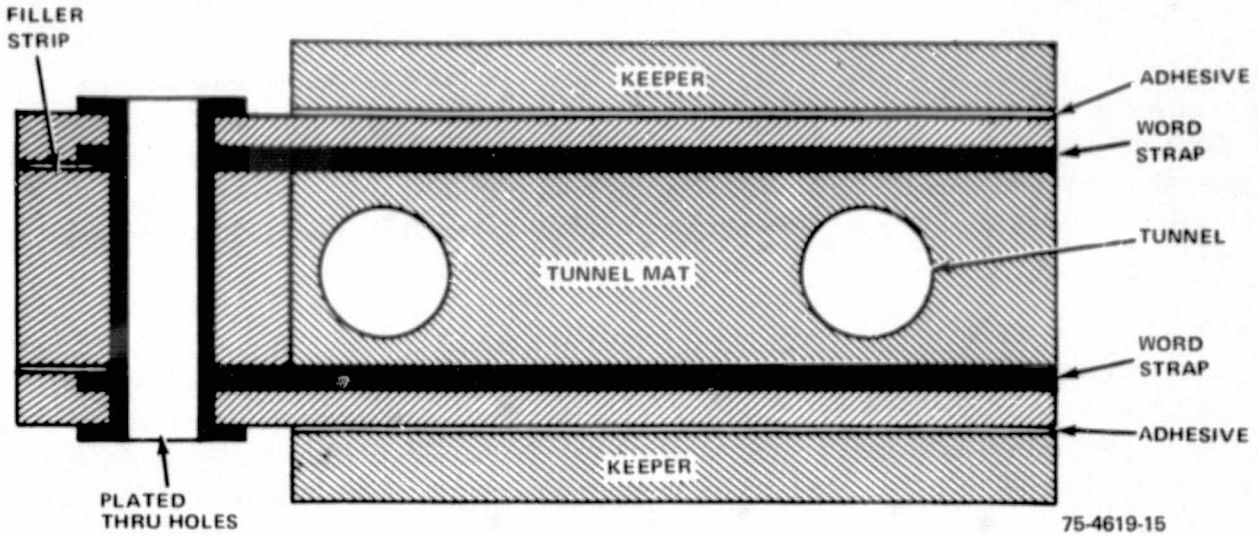


Figure 17. Tunnel Structure Construction

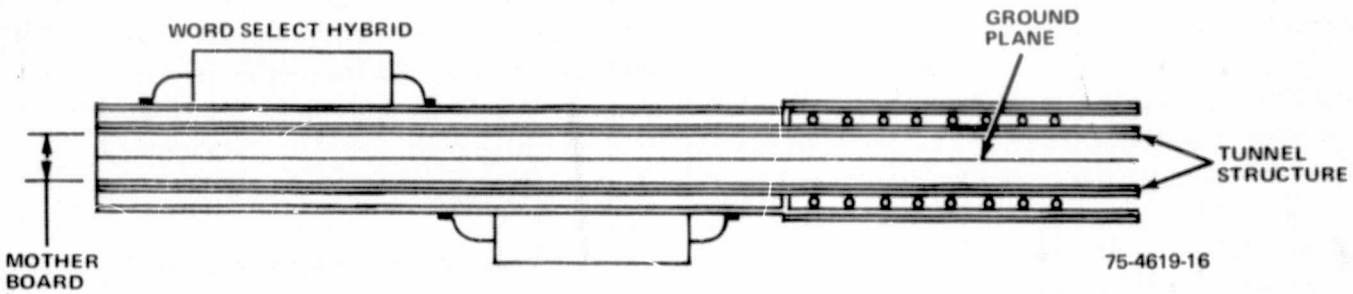


Figure 18. Memory Plane Construction

During assembly, spacers are installed at each tie-down location on the planes to precisely position the planes relative to each other in the stack. The tie-downs are located to provide maximum stability under dynamic conditions.

3.5.2 System Packaging

The 4k x 18 bit Low Power Random Access Spacecraft Memory developed by Motorola consisted of a 1k by 72 plated wire stack, two digit drive/sense electronics boards and a timing/control/word drive board, all contained in an aluminum or magnesium housing.

The concept of stacking the electronics boards in the same manner as the planes was used in the complete memory package. The timing/control/word drive board is located on top of the plated wire stack while the two digit drive/sense boards are located below the plated wire stack. This arrangement eliminates interference between signals as the digit line interconnects leave the plated wire stack in one direction while the word lines go the other direction.

The size of the memory plane (i.e., number of word lines, digit lines, required structural mounting and word drive matrix area) determine the "plan view" size of the system package. The basic plane size is 8.05" long x 4.38" wide and contains 8 tie-down screws. The electronics boards have the same mounting tie-down locations and length as the plane but are 5.0" wide.

Mechanically, each of the electronic boards are essentially identical. Each consists of a printed wiring board to which flat pack integrated circuits (Motorola plated wire hybrids or conventional logic) are lap soldered and a few discrete components are mounted. The digit boards contain the digit drivers, sense amplifiers, data input buffers and data output registers. The third board contains the timing and control logic and the transistor word drive select electronics.

After the boards are assembled, a thin conformal coating is applied to the board assembly. This coating provides protection in a high humidity environment, protection against shorting across components and a vibration damping effect on the boards. This provides an encapsulated assembly that is easily disassembled for servicing or repair.

Flat flexible cable is used for interconnecting between board assemblies. The flex interconnect is arranged so the plated wire stack and printed wiring boards can be assembled in the system stack (described previously) or opened out to provide access for testing or troubleshooting of the boards, the stack or the system. The connection to the external connector is a conventional hard wire harness.

The plated wire stack and electronics boards are assembled by stacking them into a single unit and installing them in a housing. Spacers are provided between the boards and the stack at the tie down locations to position them with respect to each other. Eight special high-strength screws pass through the spacers and secure the system in the housing.

The system assembly is contained in a single protective housing which was machined from AZ 31B magnesium material and shipped to GSFC for gold plating. The memory housing is 8.6" long x 6.3" wide x 2.9" high (exclusive of mounting flanges and connectors) establishing a volume of 157 cubic inches. The system has a total weight of 5.80 pounds.

3.5.3 Materials

Motorola's basic memory system design uses materials that meet the requirements of high reliability spaceborne hardware, particularly in the area of environment, outgassing and compatibility with other materials in the spacecraft. Materials are used that were approved on the Mariner '71 subsystems which Motorola designed and fabricated and have since been proven by the success of the mission. These materials were also used on the two memories previously delivered to GSFC under contract No. NAS 5-23163 with the exception of an adhesive used in the fabrication of the memory planes which was changed to facilitate manufacturing. This adhesive has been tested and approved for use by GSFC.

SECTION 4

TESTING

4. GENERAL

Comprehensive testing was performed on the memory and its subassemblies at each level of assembly.

4.1 SYSTEM LEVEL TESTING

Acceptance tests were conducted at the system level. Acceptance testing included complete functional tests at temperature extremes of $+85^{\circ}C$ and $-40^{\circ}C$. The acceptance test procedure and test data records are included as an Appendix. Acceptance ambient temperature functional tests were repeated after environmental testing.

Environmental testing consisted of both sine and random vibration, shock, and vacuum (to 10^{-5} mm Hg). The memory unit was continuously exercised with a worst case pattern during all environmental testing.

4.2 MEMORY STACK TESTING

A 100 percent on-line test was performed on the plated-wire during manufacture under relatively severe test patterns and word/digit current variations.

In addition to the on-line wire test, the memory stack was subjected to comprehensive worst case test patterns at the stack level using an EH 8500 computer controlled stack tester. Tests performed include adverse history being hard written in 1000 times and then the opposite polarity being written one time and immediately read out. Also adjacent bits are written into 10,000 times at the opposite polarity of the bit under test and then the bit under test is read out to test the effects of adjacent bit disturbs.

Any wire which did not meet the minimum output level requirements was replaced and the unit retested.

4.3 HYBRID CIRCUIT SCREENING

All hybrid microcircuits used in the memory were subjected to extensive, 100-percent screening to criteria based on MIL-STD-883 criteria. In addition to comprehensive electrical tests at temperature extremes, these tests included pre-cap visual inspection, centrifuge, operational vibration, stabilization bake, thermal cycling, power aging, and leak testing.

ATTACHMENT I

ACCEPTANCE TEST PROCEDURES

LOW POWER RANDOM ACCESS

SPACECRAFT MEMORY

PART NO. 01-P13701D

(35 PAGES)

PRECEDING PAGE BLANK NOT FILMED

APPLICATION	
ASSEMBLY	USED ON

ASTERISK INDICATES DATA WHICH IS NONMANDATORY FOR INFORMATION ONLY.

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
X1	Initial Release	1-2-73	H. Tweed
X2	Incorporated changes prior to first usage.	3-16-73	H. Tweed
X3	Change -6.9V to -6.1V	6-18-73	H. Tweed
X4	Change 10^{-6} mmHg to 10^{-5} mmHg. Change sine sweep levels, page 28. Change random vibration levels, page 29.	7-24-73	H. Tweed
X5	Revised per MCO S7836	2-10-75	
X6	Revised Per MCO S7844	4-28-75	

REV	X1	X1	X6	X1	X1	X3																								
SHEET	27	28	29	30	31	32	33	34	35																					
REV STATUS OF SHEETS	REV			X6	X1	X1	X1	X3	X1	X6	X6	X6	X1	X1	X6	X5	X6	X6	X1	X1	X6	X6	X6	X6	X6	X6	X6	X6	X6	X3
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26			

FOR ASSOCIATED LISTS SEE

INTERPRET DRAWING IN ACCORDANCE WITH STANDARDS PRESCRIBED BY

UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES AND END USE. FOR TOLERANCES SEE NOTE

MATERIAL:

DR BY H. Tweed

CHK BY

MFG

PROJ NO. 4339 4601

CONTR NO. NAS5-23163 NAS5-20576

RELEASE NOTICE

APPROVED H. Tweed DATE 1-2-73

APPROVED DATE

MOTOROLA INC.
Government Electronics Division
8201 EAST McDOWELL ROAD
SCOTTSDALE, ARIZONA 85252

ACCEPTANCE TEST PROCEDURE, LOW POWER RANDOM ACCESS SPACECRAFT MEMORY, PART NO. 01-P13701D *

SIZE	CODE IDENT NO.	DWG. NO.
A	94990	12-P13722D

SCALE

SHEET 1 OF 35

TABLE OF CONTENTS

SECTION	TITLE	PAGE
1.	SCOPE	3
2.	REFERENCE INFORMATION	3
3.	TEST EQUIPMENT AND ENVIRONMENTAL REQUIREMENTS	4
4.	TEST SCHEDULE	6
5.	TEST RECORDS	7
6.	PHYSICAL CHARACTERISTICS	7
7.	INITIAL FUNCTIONAL TESTS	7
8.	TEMPERATURE TEST	20
9.	VACUUM TEST	24
10.	VIBRATION TEST	27
11.	SHOCK TEST	29
12.	FINAL FUNCTIONAL TESTS	30

1. SCOPE

This procedure and the test data sheet (12-P11216B) define the unit acceptance requirements for the Low Power Random Access Spacecraft Memory, Motorola Part No. 01-P13701D, manufactured under Contract No. NAS 5-23163.

2. REFERENCE INFORMATION

2.1 SPECIFICATIONS APPLICABLE

S-562-P-24	Low Power Random Access Spacecraft Memory.
12-P13721D	Test Data Record
12-P11173B	Motorola Plated Wire Memory Tester Operating Manual.

2.2 DEFINITIONS

1	UP position on DATA and ADDRESS switches. DATA and ADDRESS lamps ON
0	DOWN position on DATA and ADDRESS switches. DATA and ADDRESS lamps OFF
Tester	Motorola Plated Wire Memory Tester
MSB	Most Significant Bit
LSB	Least Significant Bit
Error Lamps	Lamp ON indicates ERROR present.

3. TEST EQUIPMENT AND ENVIRONMENTAL REQUIREMENTS

3.1 TEST EQUIPMENT

The calibrated test equipment listed below, or its equivalent, will be required to perform this test procedure. Any equipment used as an equivalent to that listed below shall be recorded in the data sheet.

STANDARD TEST EQUIPMENT

ITEM	MANUFACTURER	MANUFACTURER'S MODEL OR TYPE	RANGE & ACCURACY
DC Milliammeter	Hewlett Packard	428B	0-10 Amp.
Oscilloscope	Tektronix	585	50ns/cm
Scope Plug-In	Tektronix	82	Tr 1.5ns
Digital Voltmeter	Hewlett-Packard	3440A	Accuracy ± .05% of reading
Counter	CMC	727BN	0.1% ± 1/2 LSB
DC Multifunction Unit	Hewlett-Packard	3444A	0-999.9 ma. 0-9.999 megohms
Oven	Wyle	CO-106-1800	-100°F to +500°F
Power Supplies	Precision Design Inc	5015-A	0-50V, 1.5 Amp.
Power Supplies	Precision Design Inc	5015-S	0-50V, 1.5 Amp.
Pulse Generator	EH	139B	10Hz to 50MHz

NON-STANDARD TEST EQUIPMENT

(NO CALIBRATION REQUIRED)

Motorola Plated Wire Memory Tester 01-P11170B001

NOTE: The Motorola Plated Wire Memory Tester supplies inputs to the memory under test from SN5400 series logic and presents a single unit load of SN5400 logic on the memory output lines.

Motorola Tester Interface Box T-5909

NOTE: The Interface Box puts a 51 ohm resistor in series with all of the signals going to the memory and provides a 1K pull up resistor to signals coming back from the memory.

ENVIRONMENTAL TEST EQUIPMENT

ITEM	MANUFACTURER	MODEL NO.
Vibration Tester	LING	275
Vacuum Chamber	NRC	2707
Shock Tester	MRL	2424
Vibration Test Fixture	MOT	—

3.2 TEST CONDITIONS

Unless otherwise specified all tests shall be performed under the following conditions.

3.2.1 Power Supply Voltage

The unit specified to be tested shall operate from the following DC source voltages:

+5.0V ± 5%
-6.1V ± 5%

3.2.2 Ambient Temperature

The unit shall be tested in a laboratory area having a temperature of $+25 \pm 10^{\circ}C$ ($77 \pm 18^{\circ}F$).

3.2.3 Ambient Humidity

Normal laboratory ambient, not to exceed 90%.

3.2.4 Ambient Atmospheric Pressure

Normal laboratory ambient.

3.2.5 Stabilization Period

The test equipment shall not be used to conduct tests until after a minimum warm-up period of 15 minutes.

4. TEST SCHEDULE

The testing to be performed on each memory unit is as follows:

1. Physical Characteristics (Weight and Dimensions)
2. Comprehensive Initial Functional Tests.
3. Operational Tests at Temperature Extremes.
4. Operational Vacuum Tests
5. Operational Vibration Tests
6. Operational Shock Tests
7. Final Functional Tests

Tests 3 through 6 may be performed in any sequence.

5. TEST RECORDS

5.1 TEST LOG

The Test Log shall be used to record the history of the memory, starting from the first system test. The log shall reference all testing, rework and idle time for the particular memory unit.

5.2 DATA RECORD

All test results shall be recorded in the Test Data Record, Motorola Document No. 12-P13721D.

6. PHYSICAL CHARACTERISTICS

6.1 WEIGHT

Place the LP RASM on the scale and read and record, in the data sheet, the weight of the memory, in pounds.

6.2 DIMENSIONS

Measure and record, in the data sheet, the outside dimensions as shown in Figure 1. Compute and record, in the data sheet, the memory volume by multiplying dimension W by dimension H by dimension D. (V = W X H X D).

7. INITIAL FUNCTIONAL TESTS

7.1 INTERCONNECTION

Record connector mate/demate history according to IUE connector log requirements.

At the Interface Box, set memory power to OFF. Connect the unit under test as shown in Figure 2, except that the Interface Box will not be connected to the Plated Wire Memory Tester. The

connections are all labeled on the Interface Box.

Turn the coarse voltage controls fully counterclockwise and turn on power to all electrical test equipment.

Using the scope, adjust the Pulse Generator for +3 ± 0.1V positive pulses of 450 ± 10 nanosecond duration (at the 50 percent points) at a 500 ± 1.0 KHz rep rate. (Use the counter to adjust the rep rate). The pulse generator output must be terminated in 50 ohms and connected to the tester when making these adjustments.

Normal precaution shall be taken to ensure that the equipment is not dropped or damaged in any way while it is being handled, or while the connectors are being engaged.

7.2 PRELIMINARY CONTROL SETTINGS

Set the Tester and Interface Box controls as follows and maintain these control settings unless otherwise directed in the individual tests.

CONTROL	SETTING
TESTER	
BD1-BD4(24 Switches)	Up
Tape Reader Power	Light Off
Run-Off-Rewind Switch	OFF
Tester Power	Light On
Address Switches	Down

CONTROL	SETTING
TESTER (Cont.)	
Data Switches	UP
READ/WRITE	WRITE
Word Length	24
READ 1/ READ 7 Switch	READ 1
Address Pattern	SEQ.
Data Pattern	MAN
Frequency	EXT.
INTERFACE BOX	
Memory Select Switches	All 2.4V
Input Current Switch	GND
Output Pullup Resistor	GND
WC Switch	OFF
Initiate Pulse Switch	GND
WC2 Switch	OFF
Memory Power	OFF

7.3 INITIAL POWER SUPPLY CONDITIONS

Using the DVM, adjust the three supplies as follows:

+5V to Interface Box: +5.0V $\pm$ 0.1V

+5V to Memory: +5.0 $\pm$ 0.1V

-6.1V to Memory: -6.1 $\pm$ 0.1V

Set the meter selection switches to measure current and leave them in this position. Disconnect the output side of all three power supplies from the Interface Box.

All subsequent mention of +5V in the procedure refers to memory power unless otherwise specified.

7.4 CHASSIS ISOLATION

Using the digital ohmmeter verify that the impedance between the memory chassis and ground test point on the interface box is $\geq$ 9 megohoms. Record the results in the Data Sheet.

7.5 INPUT SIGNAL LOADING

7.5.1 Connect the two +5V supplies to the Interface Box. (If the Interface Box supply overloads, reset it by turning its power off and back on).

7.5.2 Remove the jumper wire from the INT PULSE test point. Connect the digital ammeter between the INT PULSE and INT PULSE SW test points. Momentarily turn the MEMORY POWER switch to ON and measure and record the current. Set the INT PULSE switch to the +2.4V position. Momentarily set the memory power switch to ON and again measure and record the current. Disconnect the ammeter and connect the jumper wire between the INT PULSE and INT PULSE SW test points.

7.5.3 Replace the jumper from the MEMORY SELECT 1 test point to the MEMORY SELECT 1 SWITCH test point with the digital ammeter. Momentarily set MEMORY POWER to ON and measure and record the current. Set the MEMORY SELECT 1 SWITCH to the GND position.

Momentarily set MEMORY POWER to ON and measure and record the current.

Disconnect the ammeter and replace the jumper wire. Set the MEMORY SELECT 1 SWITCH back to the +2.4V position.

7.5.4 Repeat paragraph 7.5.3 for MEMORY SELECT 2, MEMORY SELECT 3, and MEMORY SELECT 4.

7.5.5 Connect the ammeter from the READ/WRITE test point to the INPUT CURRENT SWITCH test point. Set the Initiate Pulse Switch to 2.4V. Momentarily set the memory power switch to ON. Measure and record the current. Move the INPUT CURRENT SWITCH to the +2.4V position. Momentarily set the MEMORY POWER switch to ON and measure and record the current. Return the INPUT CURRENT SWITCH to the GND position.

7.5.6 Connect the ammeter between the ADDRESS BIT 2^{0} and the INPUT CURRENT test points. Momentarily set the MEMORY POWER switch to the ON position and measure and record the current.

Set the INPUT CURRENT SWITCH to the +2.4V position. Momentarily set the MEMORY POWER switch to the ON position and measure and record the current. Set the INPUT CURRENT SWITCH back to the GND position.

Repeat the above two measurements at each of the 12 address bit test points. Connect a jumper between the R/W and GND test points. Repeat the above two measurements at each of the 18 DI test points (i.e. with the ammeter conn. between a DI test point and the INPUT CURRENT test point).

Verify that the MEMORY POWER switch is OFF. Remove the jumper from the R/W test point and install the jumper from the INT PULSE test point back in its original position.

7.6 VERIFICATION OF OPEN COLLECTOR ON OUTPUT SIGNALS.

7.6.1 Connect the Interface Box to the tester. Connect the -6.1V power supply to the Interface Box. At the tester, depress the STOP and RESET pushbuttons. Set the initiate pulse SW to pulse position.

7.6.2 Turn the MEMORY POWER switch ON and push the START button on the tester. The tester will write a "1" in all data bits in all 4096 addresses one time and stop.

7.6.3 Set the READ/WRITE switch on the tester to the READ position. Push the tester START button. Using the Dual Trace of the oscilloscope, measure and record in the data sheet the voltage at the READ COMPLETE test point 150 ns after the leading edge of the pulse at the INITIATE PULSE test point. The voltage shall be $\leq$100 mv. Disregard errors.
(The read complete output for this test and the data outputs for the next test are terminated with a 1K resistor to GND).

7.6.4 Measure and record in the data sheet the voltage at each of the 18 data output lines that occurs 500 ns after the leading edge of the Initiate Pulse. The voltage shall be $\leq$100 mv. Push the tester stop button. Set the OUTPUT PULLUP RESISTOR switch to the +5V position.

7.7 POWER CONSUMPTION

7.7.1 Using the DVM, adjust the +5V and -6.1V memory power supplies to +5.0 ± 0.1V and -6.1 ± 0.1V, respectively. Record the voltages.

Using the 428B milliammeter, measure and record the current from the +5V memory supply. Compute and record the +5V power.

7.7.2 Using the milliammeter, measure and record the current to the -6.1V supply. Compute and record the -6.1V power.

7.7.3 Compute and record the total Memory Idle Power.

7.7.4 Set the DATA PATTERN switch to SEQ. and momentarily depress the RESET and START buttons. The tester should be cycling through memory addresses.

7.7.5 Repeat 7.7.1.

7.7.6 Repeat 7.7.2.

7.7.7 Compute and Record the Total Active Power. Momentarily depress the tester stop pushbutton.

7.8 READ COMPLETE TIMING

7.8.1 Connect the oscilloscope as follows; trigger input jack to the INITIATE PULSE test point, channel A voltage probe to the INITIATE PULSE test point and the channel B voltage probe to the READ COMPLETE test point.

7.8.2 Set the DATA PATTERN switch to MAN, READ/WRITE switch to READ, and tester BD1 switch 0 to the up position.

7.8.3 Depress and release the RESET button, then the START button.

7.8.4 Synchronize the oscilloscope on the leading edge of the initiate pulse.

7.8.5 The read complete pulse shall be a negative pulse and shall be generated 500 nanoseconds maximum after the leading edge of the initiate pulse and the duration shall be 250 ns minimum and 450 ns maximum. (All timing relationships shall be measured at the 50% points). Record the pulse delay and duration in the data sheet.

7.8.6 Momentarily depress the STOP button and set the READ/WRITE switch to WRITE. Set all data switches to the down position. Depress and release the RESET button, then the START button. Set the READ/WRITE switch to READ and momentarily depress the START switch.

7.8.7 Connect the scope channel A voltage probe to the first data output line test point (DO-0). The high-to-low transition on the data output line shall occur prior to (or in coincidence with) the leading edge of the read complete pulse. The low-to-high transition of the data output line shall occur no earlier than 150 nanoseconds following the trailing edge of the read complete pulse. (All timing relationships shall be measured at the 50 percent points). Record the results.

7.8.8 Repeat the measurements of 7.8.7 at each of the remaining 17 data output line test points. Record the results. Depress and release the stop button.

7.9 SYSTEM FUNCTIONAL TESTS

7.9.1 Depress and release the RESET button. Set the ADDRESS PATTERN switch to SEQ. Adjust the pulse generator frequency to 600 $\pm$ 1.0 KHz.

Set the DATA PATTERN switch to SEQ.

7.9.2 Depress and release the START button. The tester will then begin cycling through all memory locations. It steps to the first address, writes a "0", reads a "0", writes a "1" and reads a "1" in all bits in that address word, then steps to the next address, etc. The tester continues this cycle unless an error occurs.

Test for 2 minutes and record any errors. Depress the STOP button.

7.9.3 Set the READ 1/READ 7 Switch to the READ 7 position. The READ 7 mode causes the tester to write a "0", read a "0" seven times, write a "1", and read a "1" seven times in each memory location.

7.9.4 Depress and release the START button. The Tester will continue to cycle unless an error occurs.

Test for 2 minutes and record any errors.

7.9.5 Depress and release the STOP button. Set the DATA PATTERN switch to MAN and the READ/WRITE switch to WRITE. Set all DATA switches to the DOWN position.

7.9.6 Depress and release the RESET button and then the START button.

7.9.7 Set all DATA switches to the UP position.

7.9.8 Depress and release the RESET button and then the START button.

7.9.9 Set the READ/WRITE switch to READ. Depress and release the RESET button.

7.9.10 Depress and release the START button. Test for one minute. Record any errors.

7.9.11 Depress and release the STOP button.

7.9.12 Set the READ/WRITE switch to WRITE.

7.9.13 Set all DATA switches to the DOWN position. Depress and release the RESET button.

7.9.14 Depress and release the START button. The memory will cycle thru all 4096 addresses one time and stop.

7.9.15 Set the READ/WRITE switch to READ. Depress and release the RESET button.

7.9.16 Depress and release the START button. Run for one minute. Record any errors.

7.9.17 Depress and release the STOP button.

7.10 RANDOM ACCESS CAPABILITY

7.10.1 Set the READ/WRITE switch to WRITE and the ADDRESS PATTERN switch to MAN.

7.10.2 Select an address at random with the ADDRESS switches.

7.10.3 Set the DATA switches in a random pattern. Depress and release the RESET button.

7.10.4 Depress and release the START button. The selected data will be written into the selected address.

7.10.5 Depress and release the Stop button. Set the READ/WRITE switch to READ.

7.10.6 Depress and release the START button. The data in this address location will be read out. If an error occurs, note this in the data sheet.

7.10.7 The operator should select 3 other addresses at random, repeating steps 7.10.2 through 7.10.6 to verify the random access capability.

7.11 NON-VOLATILITY TEST

7.11.1 Set the ADDRESS PATTERN switch to SEQ and the DATA PATTERN switch to MAN.

7.11.2 Set the DATA switches to a random pattern. Depress and release the RESET button. Set the READ/WRITE switch to WRITE.

7.11.3 Depress and release the START button. The tester will run through all 4096 addresses one time and then stop. Set the READ/WRITE switch to READ.

7.11.4 Turn memory power to OFF.

7.11.5 Depress and release the RESET button.

7.11.6 Turn memory power to ON.

7.11.7 Depress and release the START button. If any errors occur, record them on the data sheet. If no errors occur, no words were disturbed when the power was interrupted.

7.11.8 Depress and release the STOP button.

7.11.9 Repeat 7.11.4 through 7.11.8 four times. Record any errors.

7.12 MEMORY SELECT TEST

7.12.1 Set the ADDRESS PATTERN switch to SEQ and the DATA PATTERN switch to SEQ. Set the No. 0 switch on BD1 to the down position.

7.12.2 Set the MEMORY SELECT switches to 0000.

7.12.3 Depress and release the RESET button, then the START button. The tester should indicate an error at the first address. Record this address on the data sheet.

7.12.4 Repeat 7.12.3 with the memory select switches set to 0001, 0010, 0011, 0100, 0101, 0110, 0111, 1000, 1001, 1010, 1011, 1100, 1101, and 1110.

7.12.5 Set the MEMORY SELECT switches to 1111.

7.12.6 Set the No. 0 switch on BD1 to the UP position. Depress and release the RESET button, then the START button. Allow the tester to run for 2 minutes. Record any errors. Depress and release the STOP button.

7.13 WORST CASE PATTERN TEST

7.13.1 Set the DATA PATTERN switch and the ADDRESS PATTERN switch to WC1. Turn the WC switch ON. Depress and release the STOP and RESET buttons.

7.13.2 Depress and release the START button. The tester will execute the following sequence:

A. Write a "1" in every bit of every word 2^{10} times.

B. Write a "0" once in every bit of every word under an even numbered word line in the stack.

C. Write a "1" in every bit of every word under an odd numbered word line and read the previously written "0" in every bit of every word under an even numbered word line until the operator sequences to the next group or until an error is detected. The READ light is lit during this cycle.

NOTE: If any error lights are ON when cycle C starts, disregard them and depress RESET one time prior to starting the one minute count. This applies to all worst-case pattern tests.

Run in cycle C for two minutes. Record any errors on the data sheet.

7.13.3 Press and release the WC1 SEQ button. The tester will execute the preceeding sequence, except "even" and "odd" are interchanged. The $WC2^0$ and $WC2^1$ lights will indicate the second WC1 group is under test. Record any errors.

7.13.4 Repeat 7.13.3 for WC1 groups 3 and 4 in which "1" and "0" are interchanged. Record any errors on the data sheet. Depress and release the STOP button. Turn the MEMORY POWER to OFF.

8. TEMPERATURE TEST

The temperature tests shall be conducted under normal laboratory conditions, with the exception of temperature.

8.1 TEST SETUP

Place the unit in the temperature chamber and establish the test setup as shown in Figure 3.

8.2 LOW TEMPERATURE

Place the memory unit in a plastic bag and seal the chamber.

8.2.1 Decrease the chamber ambient temperature to $-40^{\circ} \pm 3^{\circ}C$. When the chamber has reached this temperature, note the time.

8.2.2 Beginning 150 minutes after the chamber temperature has reached $-40^{\circ}C$, measure and record the thermistor resistance at 10 minute intervals. At each measurement, except the first one, calculate the percent change from the previous reading. When the change is less than 5 percent turn off the chamber and proceed to paragraph 8.2.3.

8.2.3 Depress the START button. The memory shall run without error for 2 minutes. Depress the STOP button and record the results.

8.2.4 Turn on the chamber and set the +5V supply to 5.25V ± 0.2V and the -6.1V supply to -6.40 ± .02V. Measure and record the power supply volt and the standby power (paragraphs 7.7.1 through 7.7.3, except do not readjust the voltages). Set the READ 1/READ 7 Switch to READ 1.

8.2.5 Adjust the pulse generator frequency to 500 ± 1.0 KHz. Set the DATA PATTERN and ADDRESS PATTERN switches to SEQ. Push the START pushbutton. Measure and record, in the data sheet, the operating power (paragraphs 7.7.5 through 7.7.7, except adjust the voltages to +5.25 ± 0.02V and -6.40 ± 0.02V).

8.2.6 Adjust the pulse generator frequency to 600 ± 1.0 KHz. Set the READ 1/READ 7 Switch to READ 7. Set the +5V supply to +4.75 ± .02V and the -6.1V supply to -5.80 ± .02V. Turn off the chamber and push the RESET pushbutton. The memory shall run without error for two minutes. Depress the STOP button. Record the results in the data sheet. Set the READ 1/READ 7 Switch to READ 1. Push the START button and readjust the voltages to 4.75 and -5.8. Push STOP.

8.2.7 Turn on the chamber and allow it to cool for 5 minutes. Then turn off the chamber and proceed to paragraph 8.2.8.

8.2.8 Repeat paragraph 7.13.1 through 7.13.4.

8.2.9 Set the MEMORY POWER switch to ON. Depress and release the START button. Using the DVM, adjust the memory power supplies to +5.25 ± 0.02V and -6.40 ± 0.02V. Depress the STOP button.

8.2.10 Turn on the chamber and allow it to cool for 5 minutes. Then turn off the chamber and proceed to paragraph 8.2.11.

8.2.11 Repeat paragraphs 7.13.1 through 7.13.4.

8.3 INTERMEDIATE TEMPERATURE TEST

Set the chamber HEAT SELECTOR to the 375W position and the temperature to +85°C. Record the time.

8.3.1 Push the Reset and START buttons. Using the DVM, adjust the memory power supplies to +5.0 ± 0.2V and -6.1V ±.02V. Depress the STOP button.

8.3.2 At 10 minute intervals record the thermistor resistance and repeat paragraphs 7.13.1 thru 7.13.4 except that each test will be run for 1 minute.

NOTE: When the thermistor indicates the internal temperature of the MEMORY is between 0°C and 15°C open the chamber and remove the plastic bag from the memory. Reseal the chamber.

Testing may be discontinued when the THERMISTOR indicates +75°C.

8.3.3 When the chamber temperature reaches +85° ± 3°C record the time on the data sheet.

8.4 HIGH TEMPERATURE

Beginning 50 minutes after the temperature chamber has reached 85°C measure and record the thermistor resistance at 10 minute intervals.

8.4 (cont.)

At each measurement except the first one calculate the percentage change from the previous reading. When the change is less than 5 percent, proceed to paragraph 8.4.1.

8.4.1 Set the ADDRESS PATTERN and DATA PATTERN switches to SEQ. Turn the MEMORY POWER to ON. Using the DVM, adjust the memory power supplies to +5.25 ± 0.01V and -6.40 ± 0.02V. Measure and record the power supply voltage, current and standby (idle) power (paragraphs 7.7.1 through 7.7.3, except do not readjust the voltages). Set the READ 1/READ 7 Switch to READ 7.

8.4.2 Depress the START button. The memory shall run without error for 2 minutes. Record the results. Set the READ 1/READ 7 Switch to READ 1.

8.4.3 Adjust the pulse generator frequency to 500 ± 1.0 KHz. Measure and record the operating power (paragraphs 7.7.5 through 7.7.7, except adjust the voltages to +5.25 ± 0.02V and -6.40 ± 0.02V). Depress the STOP button. Adjust the pulse generator frequency to 600 ± 1.0 KHz.

8.4.4 Repeat paragraphs 7.13.1 through 7.13.4.

8.4.5 Set the MEMORY POWER switch to ON. Depress and release the START button. Using the DVM, adjust the memory power supplies to +4.75 ± 0.02V and -5.80 ± 0.02V. Depress the STOP button.

8.4.6 Repeat paragraphs 7.13.1 through 7.13.4.

8.4.7 Set the MEMORY POWER switch to ON.
Set the +5V supply to 5.0V ± .02 and the -6.1V and to -6.1 ± .02V. Set the DATA PATTERN switch to MAN and the ADDRESS PATTERN switch to SEQ. Set the READ/WRITE switch to WRITE. Select a random pattern and push the START pushbutton. The tester will write the data once in each of the 4096 addresses and stop. Set the READ/WRITE switch to READ and push the START pushbutton. The memory shall run without error. After 2 minutes, push the STOP button. Record the results. Set MEMORY POWER to OFF.

9. VACUUM TEST

9.1 SETUP

9.1.1 Verify that the MEMORY POWER switch on the Interface Box is in the OFF position. Turn the voltage controls fully counter-clockwise on all three power supplies.
Connect the equipment as shown in Figure 3.
Turn on power to all memory associated test equipment.

9.1.2 Set the Tester and Interface Box controls as follows and maintain these control settings unless otherwise directed in the individual tests.

CONTROL	SETTING
TESTER	
BD1-BD4 (24 Switches)	UP
Tape Reader Power	Light Off
Run-OFF-Rewind Switch	OFF
Tester Power	Light ON
ADDRESS Switches	DOWN
DATA Switches	DOWN
READ/WRITE	READ
WORD LENGTH	24
READ 1/READ 7 Switch	READ 7
ADDRESS PATTERN	SEQ
DATA PATTERN	SEQ
FREQUENCY	EXT
INTERFACE BOX	
MEMORY SELECT SWITCHES	All 2.4V
INPUT CURRENT SWITCH	GND
OUTPUT PULLUP RESISTOR	+5V
INITIATE PULSE SWITCH	PULSE
WC2 SWITCH	OFF
WC SWITCH	OFF
MEMORY POWER	OFF

9.1.3 Push the STOP button. Turn on all three power supplies. Using the DVM, adjust the Interface Box supply to +5.0 ± 0.1V. Set the memory supplies to approximately +5V and -6V. Set the MEMORY POWER switch to ON. Using the DVM, adjust the memory supplies to +5.0 ± 0.1V and -6.1 ± 0.1V. Set the memory power switch to OFF.

9.1.4 Using the scope, adjust the Pulse Generator for +3.0 ± 0.1V positive pulses of 450 ± 10 nanoseconds duration (measured at the 50% points). Using the counter, adjust the rep rate to 600 ± 1.0 KHz. The pulse generator must be terminated in 50 ohms and connected to the tester when making these adjustments. Just prior to starting the environmental test, proceed to the next applicable paragraph.

9.2 TEST

Push the tester STOP and RESET pushbuttons. Turn the MEMORY POWER ON and push the START pushbutton on the tester. The tester will write a "0", read a "0" seven times in all data bits, write a "1", read a "1" seven times in all bits, step to the next address and repeat the same sequence. The tester will keep cycling until an error occurs. Record any bit errors. Proceed immediately to paragraph 9.2.1.

9.2.1 While monitoring the tester for errors, start the vacuum chamber pump and pump the air out of the vacuum chamber at a rate such that the pressure inside the chamber drops to 7 mmHg in less than five minutes. Record any errors.

9.2.2 Continue pumping the chamber until the pressure 10^{-5} mmHg. In order to reach this pressure, the test may last several hours. Therefore, one hour after the test has started, the memory and tester may be turned off by pushing the STOP pushbutton on the tester, turning the MEMORY POWER OFF and turning the TESTER POWER OFF. After the chamber has reached 10^{-5} mmHg, test the memory as outlined in paragraph 7.13. Record any errors. Push the memory STOP pushbutton, turn the MEMORY POWER OFF, turn the TESTER POWER OFF and return the memory to one atmosphere pressure.

10. VIBRATION TEST

The following vibration tests are to be performed in three mutually perpendicular axes. The tests include sine sweep and random vibration, and the levels to be used are described below in the individual tests. These levels are inputs to the base or mounting bracket of the unit under test. The unit shall be functionally tested during the vibration testing to insure correct operation. Prior to performing the random vibration a spectral analysis of the tester input shall be performed to insure that the random vibration input is within the specified limits. The analysis

shall be plotted and the data sheet kept as part of the test data. For information only, an accelerometer shall be mounted on the top surface of the housing while testing the X and Z axes. Plot the output from this accelerometer and file as part of the test data.

10.1 SINE SWEEP TEST

10.1.1 Verify that the MEMORY POWER switch is in the OFF position. Turn the coarse voltage controls fully counterclockwise on all three power supplies.

Connect the equipment as shown in Figure 3 and turn on power to all memory associated test equipment.

Perform paragraphs 9.1.2, 9.1.3, and 9.1.4.

Mount the memory unit on the shake table so as to be vibrated in the vertical (Y) axis as shown in Figure 4. (The axis order may be varied for convenience).

10.1.2 Push the STOP and RESET buttons. Turn the MEMORY POWER ON. Perform a sine sweep over the fequency range of 5-2000 Hz at the levels listed below:

FREQUENCY RANGE	TEST LEVEL
5-25 Hz	0.33 in DA
24-110 Hz	10G PEAK
110-2000 Hz	5g PEAK

The sweep rate is to be 2 octaves per minute. During the sweep, repeatedly perform the tests of paragraph 7.13. Record any bit errors in the Qual Test Data Sheet. Push the STOP button.

10.2 RANDOM VIBRATION

10.2.1 Perform the spectral analysis specified in paragraph 10. While applying the following random vibration input, repeatedly perform the tests of paragraph 7.13.

FREQUENCY RANGE	TEST LEVEL	TOLERANCE
15 Hz	.0044 g^2/Hz	± 3db
15-70 Hz	LINEAR INCREASE	Log-Log Plot
70-100 Hz	.138 g^2/Hz	± 3db
100-400 Hz	LINEAR DECREASE	Log-Log Plot
400-2000 Hz	.0089 g^2/Hz	± 3db

The test time is to be 2 minutes per axis.

Record any errors in the Data Record.

10.22 Repeat paragraph 10.1.2 and 10.2, in the two other mutually perpendicular axes as shown in Figure 4. Push the STOP button. Turn the MEMORY POWER OFF and then turn the TESTER POWER OFF.

11. SHOCK TEST

Two shocks in each direction shall be applied along the three mutually perpendicular axes of the LP RASM (total of 6 shocks).

11.1 SETUP

Verify that the MEMORY POWER switch is in the OFF position. Turn the coarse voltage controls fully counterclockwise on all three power supplies. Connect the equipment as shown in Figure 3 and apply power to all memory associated test equipment. Set the controls as shown in para. 9.1.2 and perform para. 9.1.3 and 9.1.4. Mount the LP RASM on the shock table so as to apply

the shock in the vertical (Y) axis as shown in Figure 5. (The axes order may be varied for convenience).

11.2 TEST

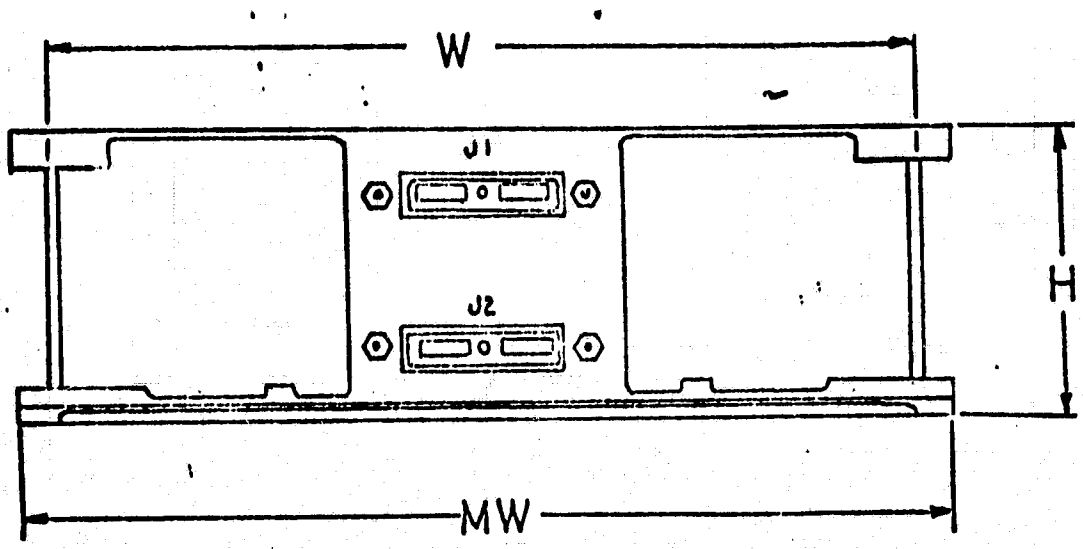
11.2.1 Push the STOP and RESET buttons. Turn the MEMORY POWER ON and push the START button. The tester is now testing the LP RASM for bit errors. Apply a half sine shock pulse of 30 g's for a duration of 6 milliseconds. Record any bit errors. Push the STOP button.

11.2.2 Push the RESET and START buttons. Apply a half sine shock pulse of 30 g's for a duration of 12 milliseconds. Record any bit errors.

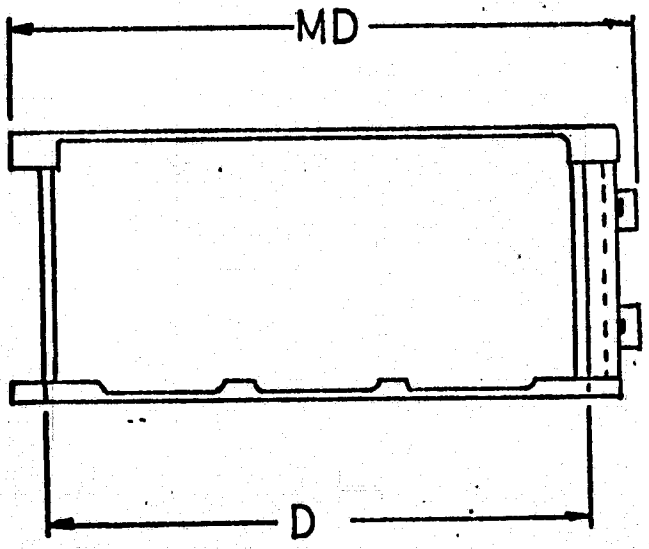
11.2.3 Repeat para. 11.2.1 and 11.2.2 for each of the other two directions as shown in Figure 5. Push the STOP button. Turn the MEMORY POWER OFF and then turn the TESTER POWER OFF.

12. FINAL FUNCTIONAL TESTS

To insure that the memory is still operating properly, perform all the tests of paragraph 7. Record the data.



FRONT



SIDE

FIGURE 1. LP RASM OUTLINE DIMENSIONS

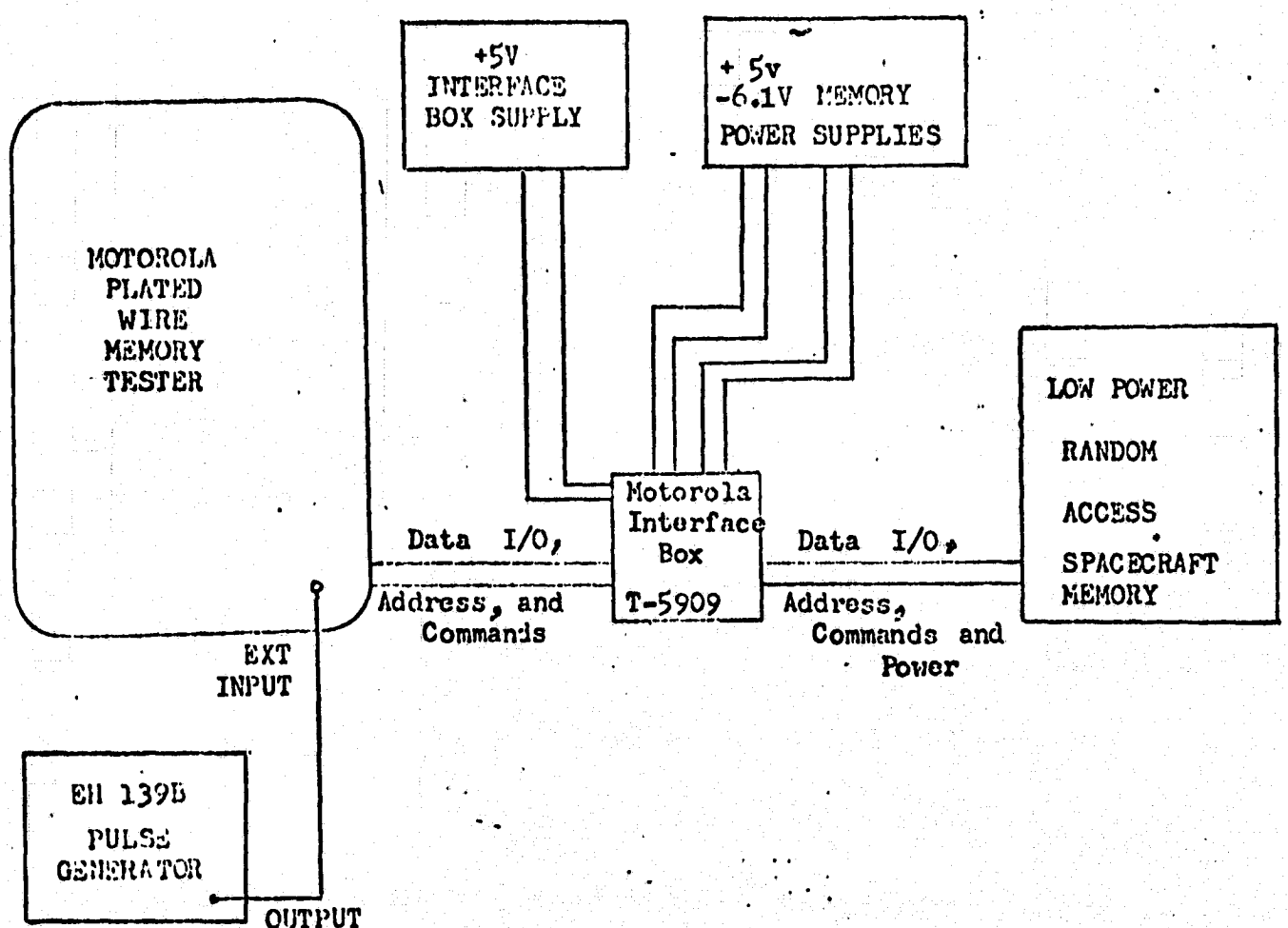


FIGURE 2. TEST SET UP

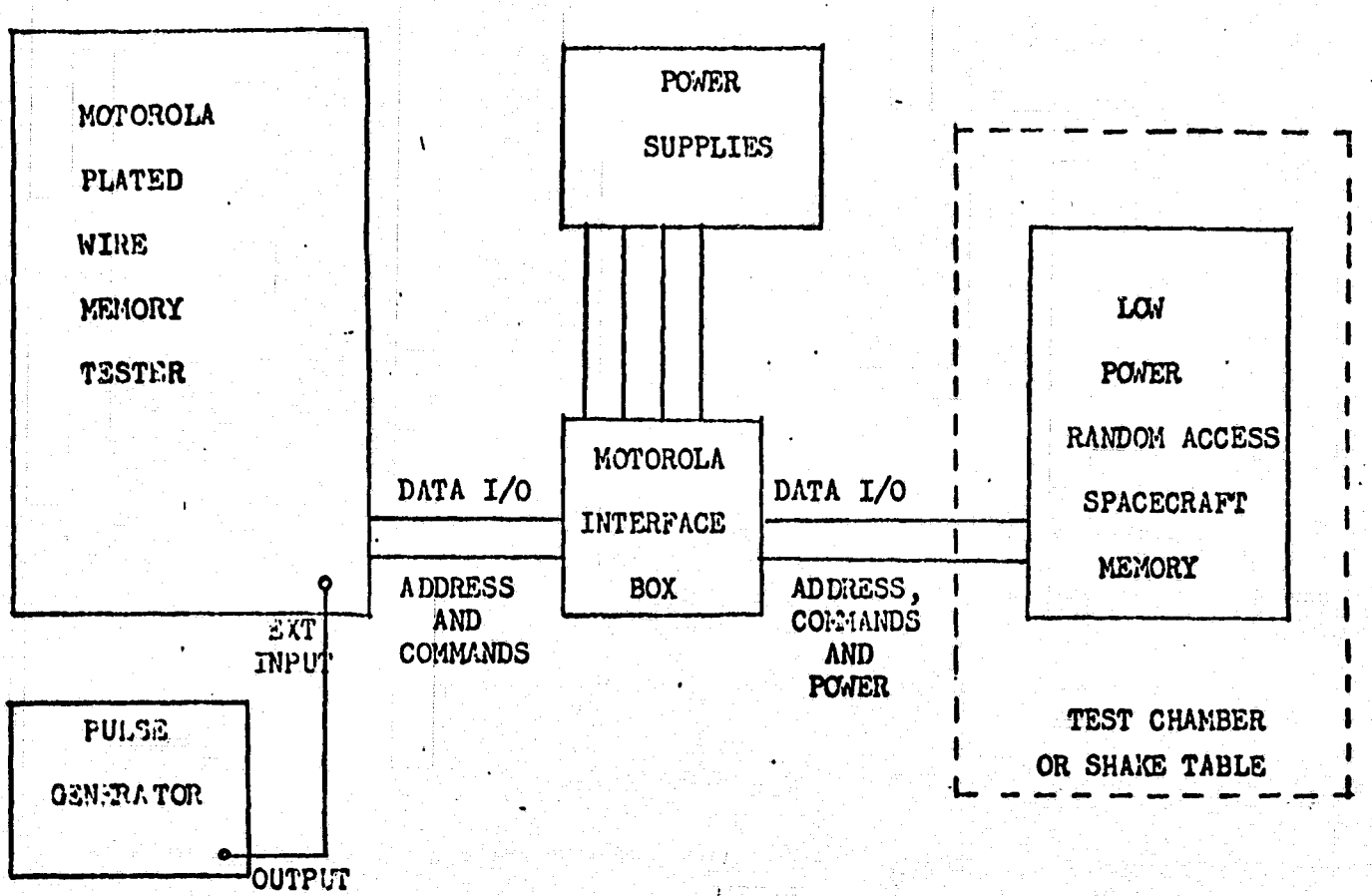


FIGURE 3. TEST SET UP

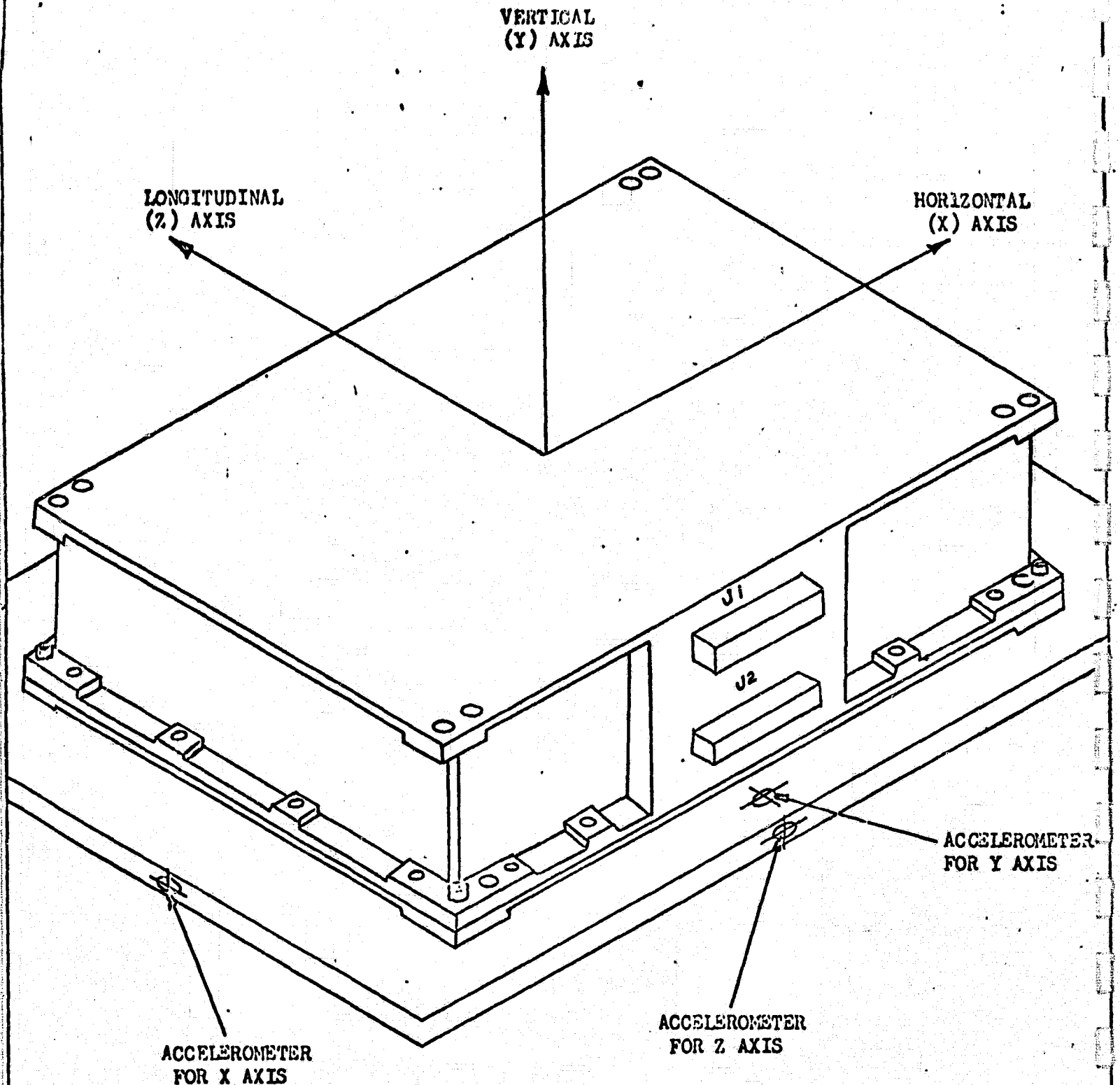
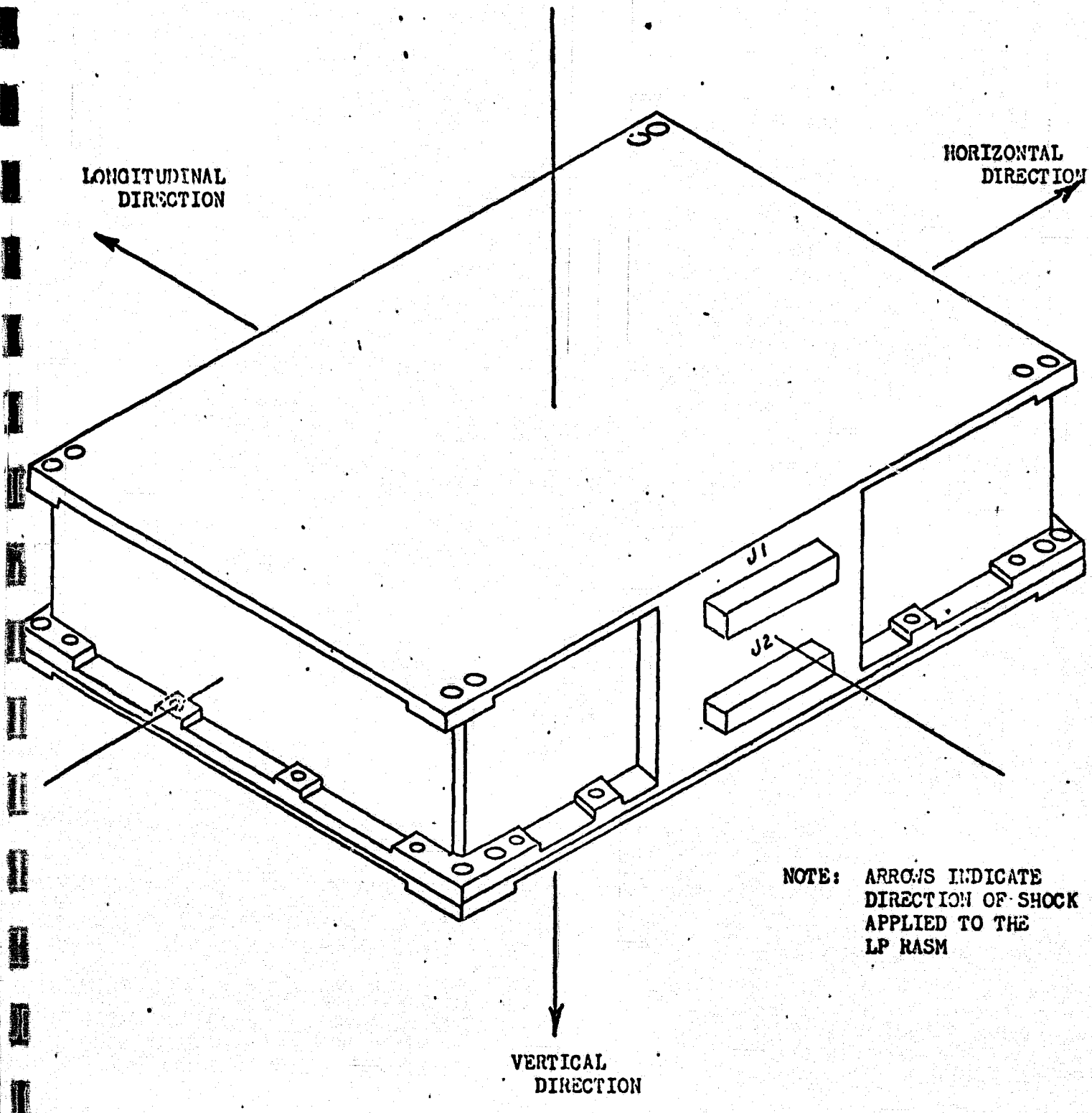


FIGURE 4. VIBRATION AXES



NOTE: ARROWS INDICATE DIRECTION OF SHOCK APPLIED TO THE LP RASM

FIGURE 5. SHOCK DIRECTIONS

MOTOROLA INC. Government Electronics Division 8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252	SIZE A	CODE IDENT NO. 94990	DWG NO. 12-P13722D
	SCALE NONE	REVISION	SHEET 35

ATTACHMENT II

ACCEPTANCE TEST DATA SHEET

LOW POWER RANDOM ACCESS

SPACECRAFT MEMORY

PART NO. 01-P13701D

SERIAL NUMBER 103

(35 PAGES)

PRECEDING PAGE BLANK NOT FILMED

*APPLICATION	
NEXT ASSEMBLY	USED ON

ASTERISK INDICATES DATA WHICH IS NONMANDATORY FOR INFORMATION ONLY.

4601

S/N 103

· REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
X1	Initial Release	—	—
X2	Incorporated changes prior to First Usage	3-16-73	H. Tweed
X3	Change -6.9V to -6.1V	6-18-73	H. Tweed
X4	Change 6000mw to 7000mw, pages 10, 17, 19, 30. Change weight from 6.0 to 6.5 pounds, page 2.	7-24-73	H. Tweed
X5	Add weight 5.8 pounds for magnesium chassis MCO S7835.	2-10-75	
X6	Revised per MCO S7845	4-28-75	

REV	X1	X4	X1	X3	X1	X1	X1	X1	X1																					
SHEET	27	28	29	30	31	32	33	34	35																					
REV STATUS OF SHEETS	REV	X5	X5	X1	X1	X1	X1	X1	X1	X1	X1	X4	X1	X1	X1	X1	X1	X6	X6	X6	X6	X6	X1	X1	X1	X1	X1	X1		
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26			

FOR ASSOCIATED LISTS SEE

INTERPRET DRAWING IN ACCORDANCE WITH STANDARDS PRESCRIBED BY

UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES AND END USE. FOR TOLERANCES SEE NOTE

MATERIAL:

DR BY H. Tweed

CHK BY

MFG

PROJ NO. 4339 4601

CONTR NO. NAS5-23163 NAS5-20576

RELEASE NOTICE

APPROVED DATE 1-2-73 H. Tweed

APPROVED DATE

MOTOROLA INC. Government Electronics Division / 8201 EAST McDOWELL ROAD SCOTTSDALE, ARIZONA 85252

ACCEPTANCE TEST DATA SHEET, LOW POWER RANDOM ACCESS SPACECRAFT MEMORY, PART NO. 01-P13701D

SIZE	CODE IDENT NO.	DWG. NO.
A	94990	12-P13721D

SCALE

SHEET 1 OF 35

V-1-C-19911-100A-7/70 DWG FORMAT

1. **SCOPE**

This test data sheet is to be used to record data as required by the Acceptance Test Procedure for the Low Power Random Access Spacecraft Memory.

2. **REFERENCE INFORMATION**

2.1 **SPECIFICATIONS APPLICABLE**

S-562-P-24	Low Power Random Access Spacecraft Memory
12-P13722D	Acceptance Test Procedure, Low Power Random Access Spacecraft Memory

3. **TEST DATA**

Unit S/N 103 Start Date of Tests 4/28/75

Tested by B. [illegible]

ATP PARA. NO.

3.1 EQUIVALENT TEST EQUIPMENT

DC MILLIAMMETER	H/P	428A
OSCILLOSCOPE	TEK	585A
DIGITAL VOLTMETER	FLUKE	8120A
COUNTER	H/P	5745L
POWER SUPPLY	POWER DESIGN	6050A

4. **PHYSICAL CHARACTERISTICS** **Limit**

6.1 **WEIGHT**

Weight of LP-RASM = 5.640 Pounds 6.5 pounds (aluminum)
5.8 pounds (magnesium)

MSFC

MOTOROLA INC. Government Electronics Division	SIZE	CODE IDENT NO.	DWG NO.
8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252	A	94990	12-P13721D
	SCALE	REVISION	SHEET 2

S/N 103

Date of Test 4/28/75

Tested By B-Lott

6.2 DIMENSIONS

Limit

H - 2.896 inches

M W - 8.960 inches

W - 8.630 inches

D - 6.322 inches

MD - 6.929 inches

V = H X W X D = 158.0 inches^3 ≤ 160 inches^3

MJ.
ESFP

MOTOROLA INC. Government Electronics Division 8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252	SIZE A	CODE IDENT NO. 94990	DWG NO. 12-P13721D
	SCALE	REVISION	SHEET 3

S/N 103 Date of Test 4/29/75

Tested By B. Fort

			Limit
7.4	CHASSIS ISOLATION		
	Impedance	≥ 11,999 MEGOHMS	≥ 9 megohms
7.5	INPUT SIGNAL LOADING		
7.5.2	Current from INITIATE PULSE to Gnd	1.15 ma	≤ 2 ma
	Current from 2.4V to INITIATE PULSE	3.43 μa	≤ 20 μa
7.5.3	Current from MEM SEL 1 to Gnd	1.14 ma	≤ 2 ma
	Current from 2.4V to MEM SEL 1	2.49 μa	≤ 20 μa
7.5.4	Current from MEM SEL 2 to Gnd	1.14 ma	≤ 2 ma
	Current from 2.4V to MEM SEL 2	3.46 μa	≤ 20 μa
	Current from MEM SEL 3 to Gnd	1.14 ma	≤ 2 ma
	Current from 2.4V to MEL SEL 3	3.42 μa	≤ 20 μa
	Current from MEM SEL 4 to Gnd	1.14 ma	≤ 2 ma
	Current from 2.4V to MEM SEL 4	2.49 μa	≤ 20 μa
7.5.5	Current from READ/WRITE to Gnd	.856 ma	≤ 2 ma
	Current from 2.4V to READ/WRITE	~~.856~~ 4.9 μa	≤ 20 μa
7.5.6	Current from ADDRESS 2^0 to Gnd	.87 ma	≤ 2 ma
	Current from 2.4V to ADDRESS 2^0	5.28 μa	≤ 20 μa

MMS 6SEC

MOTOROLA INC. Government Electronics Division	SIZE	CODE IDENT NO.	DWG NO.
8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252	A	94990	12-P13721D
	SCALE	REVISION	SHEET 4

S/N 103

Date of Test B. 104

Tested By 4/28/74

		Limits
Current from ADDRESS 2^1 to Gnd	.875 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^1	5.06 μa	≤ 20 μa
Current from ADDRESS 2^2 to Gnd	.945 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^2	5.68 μa	≤ 20 μa
Current from ADDRESS 2^3 to Gnd	.882 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^3	5.36 μa	≤ 20 μa
Current from ADDRESS 2^4 to Gnd	.934 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^4	6.1 μa	≤ 20 μa

MRS
ESEC

S/N 103

Date of Test 4/28/75

Tested By B. Fort

		Limits
Current from ADDRESS 2^5 to Gnd	.884 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^5	4.73 μa	≤ 20μa
Current from ADDRESS 2^6 to Gnd	.870 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^5	5.00 μa	≤ 20μa
Current from ADDRESS 2^7 to Gnd	.962 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^7	5.62 μa	≤ 20μa
Current from ADDRESS 2^8 to Gnd	.993 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^8	.99 μa	≤ 20μa
Current from ADDRESS 2^9 to Gnd	.967 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^9	1.09 μa	≤ 20μa
Current from ADDRESS 2^{10} to Gnd	.852 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^{10}	5.46 μa	≤ 20μa
Current from ADDRESS 2^{11} to Gnd	.855 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^{11}	5.42 μa	≤ 20μa
Current from DATA IN BIT 0 to Gnd	1.056 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 0	7.96 μa	≤ 20μa

MMS
GSFC

S/N 103

Date of Test 4/28/75

Tested By B. Fry

		Limits
Current from DATA IN BIT 1 to Gnd	1.04 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 1	8.12 μa	≤ 20 μa
Current from DATA IN BIT 2 to Gnd	1.06 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 2	7.45 μa	≤ 20 μa
Current from DATA IN BIT 3 to Gnd	.996 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 3	8.7 μa	≤ 20 μa
Current from DATA IN BIT 4 to Gnd	1.00 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 4	8.62 μa	≤ 20 μa
Current from DATA IN BIT 5 to Gnd	1.024 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 5	8.72 μa	≤ 20 μa
Current from DATA IN BIT 6 to Gnd	1.05 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 6	7.0 μa	≤ 20 μa
Current from DATA IN BIT 7 to Gnd	1.04 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 7	7.53 μa	≤ 20 μa
Current from DATA IN BIT 8 to Gnd	1.04 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 8	7.54 μa	≤ 20 μa
Current from DATA IN BIT 9 to Gnd	.965 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 9	3.06 μa	≤ 20 μa

MSFC

S/N 103

Date of Test 4/28/75

Tested By B. Ford

		Limits
Current from DATA IN BIT 10 to Gnd	.969 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 10	3.11 μa	≤ 20μa
Current from DATA IN BIT 11 to Gnd	.972 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 11	2.92 μa	≤ 20μa
Current from DATA IN BIT 12 to Gnd	.806 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 12	7.23 μa	≤ 20μa
Current from DATA IN BIT 13 to Gnd	.815 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 14	7.47 μa	≤ 20μa
Current from DATA IN BIT 14 to Gnd	.840 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 14	8.02 μa	≤ 20μa
Current from DATA IN BIT 15 to Gnd	.950 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 15	4.97 μa	≤ 20μa
Current from DATA IN BIT 16 to Gnd	.922 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 17	5.03 μa	≤ 20μa
Current from DATA IN BIT 17 to Gnd	.929 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 17	5.13 μa	≤ 20μa

MRS
GSFC

S/N 103

Date of Test 4/28/75

Tested By B Fox

			Limit
7.6	VERIFICATION OF OPEN COLLECTOR ON OUTPUT SIGNALS		
7.6.3	READ COMPLETE voltage	70 mv	≤ 100 mv
7.6.4	DATA OUT BIT 0 voltage	10 mv	≤ 100 mv
	DATA OUT BIT 1 voltage	10 mv	≤ 100 mv
	DATA OUT BIT 2 voltage	0 mv	≤ 100 mv
	DATA OUT BIT 3 voltage	-10 mv	≤ 100 mv
	DATA OUT BIT 4 voltage	-10 mv	≤ 100 mv
	DATA OUT BIT 5 voltage	-10 mv	≤ 100 mv
	DATA OUT BIT 6 voltage	-10 mv	≤ 100 mv
	DATA OUT BIT 7 voltage	-20 mv	≤ 100 mv
	DATA OUT BIT 8 voltage	-20 mv	≤ 100 mv
	DATA OUT BIT 9 voltage	-10 mv	≤ 100 mv
	DATA OUT BIT 10 voltage	-10 mv	≤ 100 mv
	DATA OUT BIT 11 voltage	-10 mv	≤ 100 mv
	DATA OUT BIT 12 voltage	-10 mv	≤ 100 mv
	DATA OUT BIT 13 voltage	0 mv	≤ 100 mv
	DATA OUT BIT 14 voltage	20 mv	≤ 100 mv
	DATA OUT BIT 15 voltage	-10 mv	≤ 100 mv
	DATA OUT BIT 16 voltage	-20 mv	≤ 100 mv
	DATA OUT BIT 17 voltage	-10 mv	≤ 100 mv

MMS
GSFC

S/N 103

Date of Test 4/28/75

Tested By B Tot

				Limits
7.7	POWER CONSUMPTION (25°C)			
7.7.1	Memory +5V Voltage	4.993	Volts	
	Memory -6.1V voltage	6.102	Volts	
	+5V Current	10.3	ma	
	+5V Power	51.5	mw	
7.7.2	Memory -6.1V Current	4.7	ma	
	Memory -6.1V Power	28.7	mw	
7.7.3	Total Memory Idle Power	~~33.4~~ 80.2	mw	170 mw max
7.7.5	Memory +5V Voltage	5.006	Volts	
	Memory -6.1V Voltage	6.101	Volts	
	+5V Current	695	ma	
	+5V Power	3475	mw	
7.7.6	Memory -6.1V Current	240	ma	
	Memory -6.1V Power	1464	mw	
7.7.7	Total Active Power	~~4939~~ ~~7204~~	mw	7000 mw max.
7.8	READ COMPLETE TIMING			
7.8.5	Delay	410	ns	500 ns max.
	Duration	330	ns	250 ns min 450 ns max.

6.1
4.7
427
244
28.67

4
695
5
3475

240
6.1
240
1440
1464.0

WMS
ESF-C

MOTOROLA INC. Government Electronics Division	SIZE	CODE IDENT NO.	DWG NO.
8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252	A	94990	12-P13721D
	SCALE	REVISION	SHEET 10

AV-2-U-160M-100A-3/69 DWG FORMAT

S/N 103

Date of Test 4/28/75

Tested by B. Scott

LIMITS

7.8.7 & 7.8.8 READ COMPLETE/DATA OUTPUT TIMING

DO-0	OK ✓	REJECT	
DO-1	OK ✓	REJECT	
DO-2	OK ✓	REJECT	
DO-3	OK ✓	REJECT	
DO-4	OK ✓	REJECT	
DO-5	OK ✓	REJECT	
DO-6	OK ✓	REJECT	
DO-7	OK ✓	REJECT	REFER TO TEST PROC.
DO-8	OK ✓	REJECT	
DO-9	OK ✓	REJECT	
DO-10	OK ✓	REJECT	
DO-11	OK ✓	REJECT	
DO-12	OK ✓	REJECT	
DO-13	OK ✓	REJECT	
DO-14	OK ✓	REJECT	
DO-15	OK ✓	REJECT	
DO-16	OK ✓	REJECT	
DO-17	OK ✓	REJECT	

WMS
65FC

S/N 103

Date of Test 4/29/73
Tested By [illegible]

		Limits
7.9	SYSTEM FUNCTIONAL TEST	
7.9.2	Did an error occur?	
	No ✓	
	Yes ____ Address ____ Bits ____	0 errors
7.9.4	Did an error occur?	
	No ✓	
	Yes ____ Address ____ Bits ____	0 errors
7.9.10	Did an error occur?	
	No ✓	
	Yes ____ Address ____ Bits ____	0 errors
7.9.16	Did an error occur?	
	No ✓	
	Yes ____ Address ____ Bits ____	0 errors
7.10	RANDOM ACCESS CAPABILITY	
7.10.6	Did an error occur?	
	No ✓	
	Yes ____ Address ____ Bits ____	0 errors
7.10.7	Did an error occur?	
	a) No ✓	
	Yes ____ Address ____ Bits ____	0 errors

WNS
GSFC

S/N 103

Date of Test 4/28/75
Tested By [illegible]

		Limits
b)	No ✓	
	Yes ____ Address ____ Bits ____	0 errors
c)	No ✓	
	Yes ____ Address ____ Bits ____	0 errors
7.11	NON-VOLATILITY TEST	
7.11.7 & 7.11.9	Did an error occur?	
	No ✓	
	Yes ____ Address ____ Bits ____	0 errors
7.12	MEMORY SELECT TEST	
7.12.3	Address 0000 (Octal)	0000
7.12.4	Address 0001 0000 (Octal)	0000
	0010 0000 (Octal)	0000
	0011 0000 (Octal)	0000
	0100 0000 (Octal)	0000
	0101 0000 (Octal)	0000
	0110 0000 (Octal)	0000
	0111 0000 (Octal)	0000
	1000 0000 (Octal)	0000
	1001 0000 (Octal)	0000
	1010 0000 (Octal)	0000

MMS
GSFC

S/N 103

Date of Test 4/28/75

Tested By B. Foo

		Limits
Address 1011	0000 (Octal)	0000
1100	0000 (Octal)	0000
1101	0000 (Octal)	0000
1110	0000 (Octal)	0000

7.12.6 Did an error occur?

No ✓

Yes ____ Address ____ Bits ____ 0 errors

7.13 WORST CASE PATTERN TEST

7.13.2 Did an error occur?

No ✓

Yes ____ Address ____ Bits ____ 0 errors

7.13.3 Did an error occur?

No ✓

Yes ____ Address ____ Bits ____ 0 errors

WMS
GSFC

S/N 103

Date of Test 4/28/75

Tested By B. Fox

Limits

7.13.4 a) Did an error occur?

No ✓

Yes ____ Address ____ Bit ____ 0 errors

b) Did an error occur?

No ✓

Yes ____ Address ____ Bit ____ 0 errors

MMS
GSFC

MOTOROLA INC. Government Electronics Division	SIZE	CODE IDENT NO.	DWG NO.
8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252	A	94990	12-P13721D
	SCALE	REVISION	SHEET 15

S/N 103

DATE OF TEST 4/2-9/75
TESTED BY B. Zw

8. TEMPERATURE TEST — LIMITS

8.2.1 TIME 5:57

8.2.2 LOW TEMPERATURE

THERMISTOR RESISTANCE

150 MINUTES 222.3 K OHMS

160 MINUTES 222.7 K OHMS % CHANGE .2%

170 MINUTES _____ K OHMS % CHANGE _____

180 MINUTES _____ K OHMS % CHANGE _____

190 MINUTES _____ K OHMS % CHANGE _____

8.2.3 DID AN ERROR OCCUR?

NO ✓

YES _____ ADDRESS _____ BITS _____ 0 ERRORS

8.2.4

-6.1 V VOLTAGE	6.400 VOLTS	+5 V VOLTAGE	5.254 VOLTS
-6.1 V CURRENT	14.3 ma	+5 V CURRENT	10.9 ma
-6.1 V POWER	91.52 mw	+5 V POWER	57.26 mw

TOTAL MEMORY IDLE POWER 148.78 mw — 170 mw MAX

8.2.5

-6.1 V VOLTAGE	6.402 VOLTS	+5 V VOLTAGE	5.25 VOLTS
-6.1 V CURRENT	263 ma	+5 V CURRENT	700 ma
-6.1 V POWER	1,683 mw	+5 V POWER	3,675 mw

TOTAL MEMORY OPERATING POWER 5358 mw — 7000 mw MAX

WTB ESFC

MOTOROLA INC. Government Electronics Division	SIZE	CODE IDENT NO.	DWG NO.
8201 EAST McDOWELL ROAD SCOTTSDALE, ARIZONA 85257	A	94990	12-P13721D
	SCALE	REVISION	SHEET 16

S/N 103

DATE OF TEST 4/29/75

TESTED BY B Fort

LIMITS

8.2.6 DID AN ERROR OCCUR?

NO ✓

YES ____ ADDRESS _____ BIT _____ 0 ERRORS

8.2.8 WC a) DID AN ERROR OCCUR?

NO ✓

YES ____ ADDRESS _____ BIT _____ 0 ERRORS

WC b) DID AN ERROR OCCUR?

NO ✓

YES ____ ADDRESS _____ BIT _____ 0 ERRORS

WC c) DID AN ERROR OCCUR?

NO ✓

YES ____ ADDRESS _____ BIT _____ 0 ERRORS

WC d) DID AN ERROR OCCUR?

NO ✓

YES ____ ADDRESS _____ BIT _____ 0 ERRORS

8.2.8 II WC a) DID AN ERROR OCCUR?

NO ✓

YES ____ ADDRESS _____ BIT _____ 0 ERRORS

WMS GSFC

S/N 103

DATE OF TEST 4/29/75

TESTED BY B. Hunt

LIMITS

8.2.9 (Cont.)

WC b) DID AN ERROR OCCUR?

NO ✓

YES ____ ADDRESS ____ BIT ____ 0 ERRORS

WC c) DID AN ERROR OCCUR?

NO ✓

YES ____ ADDRESS ____ BIT ____ 0 ERRORS

WC d) DID AN ERROR OCCUR?

NO ✓

YES ____ ADDRESS ____ BIT ____ 0 ERRORS

8.3 INTERMEDIATE TEMPERATURE TEST

TIME 9:43

8.3.2 TIME	THERMISTOR READING.		DID ANY ERROR OCCUR?			
9:45	126.8	K OHMS	NO ✓	YES ____		0 ERRORS
9:55	98.6	K OHMS	NO ✓	YES ____		0 ERRORS
10:05	52.00	K OHMS	NO ✓	YES ____		0 ERRORS
10:15	24.0	K OHMS	NO ✓	YES ____		0 ERRORS
10:25	16.25	K OHMS	NO ✓	YES ____		0 ERRORS
10:35	9.36	K OHMS	NO ✓	YES ____		0 ERRORS
10:45	5.77	K OHMS	NO ✓	YES ____		0 ERRORS
10:55	3.30	K OHMS	NO ✓	YES ____		0 ERRORS
11:05	2.73	K OHMS	NO ✓	YES ____		0 ERRORS
11:15	2.10	K OHMS	NO ✓	YES ____		0 ERRORS
____	____	K OHMS	NO ____	YES ____		0 ERRORS
____	____	K OHMS	NO ____	YES ____		0 ERRORS

MSEC

S/N 103

DATE OF TEST 4/29/75

TESTED BY B. [illegible]

LIMITS

8.3.3 TIME 10:54

8.4 160 ~~50~~ MINUTES 1.408 K OHMS

170 ~~60~~ MINUTES 1.408 K OHMS % CHANGE 0

~~70~~ MINUTES _____ K OHMS % CHANGE

80 MINUTES _____ K OHMS % CHANGE

90 MINUTES _____ K OHMS % CHANGE

8.4.1 -6.1 V VOLTAGE 6.403 VOLTS +5 V VOLTAGE 5.252 VOLTS

-6.1 V CURRENT 6.3 ma +5 V CURRENT 12.2 ma

-6.1 V POWER 40.3 mw +5 V POWER 64.1 mw

TOTAL MEMORY IDLE POWER 104.4 mw 170 mw MAX

8.4.2 DID AN ERROR OCCUR?

NO ✓

YES ____ ADDRESS _____ BIT _____ 0 ERRORS

8.4.3 -6.1 V VOLTAGE 6.400 VOLTS +5 V VOLTAGE 5.247 VOLTS

-6.1 V CURRENT 280 ma +5 V VOLTAGE 795 ma

-6.1 V POWER 1792 mw +5 V POWER 4171 mw

TOTAL MEMORY OPERATING POWER 5963 mw 7000 mw MAX

8.4.4 WC a) DID AN ERROR OCCUR?

NO ✓

YES ____ ADDRESS _____ BIT _____ 0 ERRORS

MTJ GSFC

MOTOROLA INC. Government Electronics Division	SIZE	CODE IDENT NO.	DWG NO.
8201 EAST McDOWELL ROAD SCOTTSDALE, ARIZONA 85257	A	94990	12-P13721D
	SCALE	REVISION	SHEET 19

S/N 103 DATE OF TEST 4/29/75

TESTED BY B. Fort

LIMITS

8.4.4 (Cont.)

WC b) DID AN ERROR OCCUR?

NO ✓

YES ____ ADDRESS ____ BIT ____ O ERRORS

WC c) DID AN ERROR OCCUR?

NO ✓

YES ~~✓~~ GR ADDRESS ____ BIT ____ O ERRORS

WC d) DID AN ERROR OCCUR ?

NO ✓

YES ____ ADDRESS ____ BIT ____ O ERRORS

8.4.6 WC a) DID AN ERROR OCCUR?

NO ✓

YES ____ ADDRESS ____ BIT ____ O ERRORS

WC b) DID AN ERROR OCCUR?

NO ✓

YES ____ ADDRESS ____ BIT ____ O ERRORS

WC c) DID AN ERROR OCCUR?

NO ✓

YES ____ ADDRESS ____ BIT ____ O ERRORS

WC d) DID AN ERROR OCCUR?

NO ✓

YES ____ ADDRESS ____ BIT ____ O ERRORS

8.4.7 DID AN ERROR OCCUR?

NO ✓

YES ____ ADDRESS ____ BIT ____ O ERRORS

C-2

MS GSFC

MOTOROLA INC.
Government Electronics Division
8201 EAST McDOWELL ROAD
SCOTTSDALE, ARIZONA 85257

SIZE	CODE IDENT NO.	DWG NO.
A	94990	12-P13721D

SCALE | REVISION | SHEET 20

AV-2-B-199H-100A-2 74 DWG FORMAT

S/N 103 Date of Test 5/5/75

Tested by B. Hart

Limits

9. VACUUM TEST

9.2 Did Any Bit Errors Occur?

No ✓

Yes _____ Address _____ Bits _____ 0 Errors

9.2.1 Fast Decompression

Date 5/5/75 Tested by B. Hart

Did Any Bit Errors Occur?

No ✓

Yes _____ Address _____ Bits _____ 0 Errors

9.2.2 Hard Vacuum

Date 5/5/75 Tested by B. Hart

Did Any Bit Errors Occur?

No ✓

Yes _____ Address _____ Bits _____ 0 Errors

10. VIBRATION TEST

Date 5/6/75 Tested by [signature]

SINE SWEEP

Axis X - Did Any Bit Errors Occur?

No ✓

Yes _____ Freq _____ Address _____ Bits ____ 0 Errors

MOTOROLA INC. Government Electronics Division	SIZE	CODE IDENT NO.	DWG NO.
8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252	A	94990	12-P13721D
	SCALE	REVISION	SHEET 21

S/N 103

Date of Test 5/6/75

Tested by [illegible]

Axis Y - Did Any Bit Error Occur?

Limits

No ✓

Yes ____ Freq ____ Address ____ Bits ____ 0 Errors

Axis Z - Did Any Bit Errors Occur?

No ✓

Yes ____ Freq ____ Address ____ Bits ____ 0 Errors

RANDOM VIBRATION

Axis X - Did Any Bit Errors Occur?

No ✓

Yes ____ Freq ____ Address ____ Bits ____ 0 Errors

Axis Y - Did Any Bit Errors Occur?

No ✓

Yes ____ Freq ____ Address ____ Bits ____ 0 Errors

Axis Z - Did Any Bit Errors Occur?

No ✓

Yes ____ Freq ____ Address ____ Bits ____ 0 Errors

Good Test No plot

RERAN FOR PLOT

11. SHOCK TEST

Date 5/8/75 Tested By ____

6 MILLISECOND DURATION SHOCK

Y Direction - Did Any Bit Errors Occur?
(VERTICAL)

No ✓

Yes ____ Address ____ Bits ____ 0 Errors

MOTOROLA INC. Government Electronics Division	SIZE	CODE IDENT NO.	DWG NO.
8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252	A	94990	12-P13721D
	SCALE	REVISION	SHEET 22

S/N 103

Date of Test 5-7-75

Tested by

Limits

Z Direction - Did Any Bit Errors Occur?

No ✓

Yes _____ Address _____ Bits _____ 0 Errors

X Direction - Did Any Bit Errors Occur?

No ✓

Yes _____ Address _____ Bits _____ 0 Errors

12 MILLISECOND DURATION SHOCK

Y Direction - Did Any Bit Errors Occur?

No ✓

Yes _____ Address _____ Bits _____ 0 Errors

Z Direction - Did Any Bit Errors Occur?

No ✓

Yes _____ Address _____ Bits _____ 0 Errors

X Direction - Did Any Bit Errors Occur?

No ✓

Yes _____ Address _____ Bits _____ 0 Errors

MAY 8-1975

S/N 103 Date of Test 5-9-75.

Tested By E.E.C.

		Limit
7.4	CHASSIS ISOLATION	
	Impedance >10	≥ 9 megohms
7.5	INPUT SIGNAL LOADING	
7.5.2	Current from INITIATE PULSE to Gnd 1.164 ma	≤ 2 ma
	Current from 2.4V to INITIATE PULSE 3.57 μa	≤ 20 μa
7.5.3	Current from MEM SEL 1 to Gnd 1.167 ma	≤ 2 ma
	Current from 2.4V to MEM SEL 1 2.52 μa	≤ 20 μa
7.5.4	Current from MEM SEL 2 to Gnd 1.166 ma	≤ 2 ma
	Current from 2.4V to MEM SEL 2 3.59 μa	≤ 20 μa
	Current from MEM SEL 3 to Gnd 1.165 ma	≤ 2 ma
	Current from 2.4V to MEL SEL 3 3.54 μa	≤ 20 μa
	Current from MEM SEL 4 to Gnd 1.163 ma	≤ 2 ma
	Current from 2.4V to MEM SEL 4 2.56 μa	≤ 20 μa
7.5.5	Current from READ/WRITE to Gnd 0.877 ma	≤ 2 ma
	Current from 2.4V to READ/WRITE 5.13 μa	≤ 20 μa
7.5.6	Current from ADDRESS 2^0 to Gnd .843 ma	≤ 2 ma
	Current from 2.4V to ADDRESS 2^0 5.47 μa	≤ 20 μa

W.W. Hoffmeier 5-9-75

S/N 103

Date of Test 5-9-75

Tested By [signature]

		Limits
Current from ADDRESS 2^1 to Gnd	.876 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^1	5.22 μa	≤ 20 μa
Current from ADDRESS 2^2 to Gnd	.967 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^2	5.87 μa	≤ 20 μa
Current from ADDRESS 2^3 to Gnd	.904 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^3	5.57 μa	≤ 20 μa
Current from ADDRESS 2^4 to Gnd	.958 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^4	6.33 μa	≤ 20 μa

H.W. Heffernan
5-9-75

S/N 103

Date of Test 5-9-75

Tested By [signature]

		Limits
Current from ADDRESS 2^5 to Gnd	.905 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^5	4.92 μa	≤ 20μa
Current from ADDRESS 2^6 to Gnd	.891 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^5	5.19 μa	≤ 20μa
Current from ADDRESS 2^7 to Gnd	.986 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^7	5.85 μa	≤ 20μa
Current from ADDRESS 2^8 to Gnd	1.016 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^8	1.02 μa	≤ 20μa
Current from ADDRESS 2^9 to Gnd	.991 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^9	1.11 μa	≤ 20μa
Current from ADDRESS 2^{10} to Gnd	.873 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^{10}	5.60 μa	≤ 20μa
Current from ADDRESS 2^{11} to Gnd	.876 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^{11}	5.57 μa	≤ 20μa
Current from DATA IN BIT 0 to Gnd	1.08 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 0	8.21 μa	≤ 20μa

T.W. Heffernan
5-9-75

S/N 103

Date of Test 5-9-75

Tested By [signature]

		Limits
Current from DATA IN BIT 1 to Gnd	1.06 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 1	8.37 μa	≤ 20 μa
Current from DATA IN BIT 2 to Gnd	1.08 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 2	7.66 μa	≤ 20 μa
Current from DATA IN BIT 3 to Gnd	1.02 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 3	8.97 μa	≤ 20 μa
Current from DATA IN BIT 4 to Gnd	1.02 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 4	8.90 μa	≤ 20 μa
Current from DATA IN BIT 5 to Gnd	1.05 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 5	8.96 μa	≤ 20 μa
Current from DATA IN BIT 6 to Gnd	1.08 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 6	7.78 μa	≤ 20 μa
Current from DATA IN BIT 7 to Gnd	1.07 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 7	7.80 μa	≤ 20 μa
Current from DATA IN BIT 8 to Gnd	1.06 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 8	7.77 μa	≤ 20 μa
Current from DATA IN BIT 9 to Gnd	.988 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 9	3.16 μa	≤ 20 μa

[signature] 5-9-75

MOTOROLA INC.
Government Electronics Division
8201 E. McDOWELL ROAD

SIZE	CODE IDENT NO.	DWG NO.
A	94990	12-P13721D

SCALE	REVISION	SHEET 27

S/N 103

Date of Test 5-9-75

Tested By [signature]

		Limits
Current from DATA IN BIT 10 to Gnd	.991 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 10	3.21 μa	≤ 20μa
Current from DATA IN BIT 11 to Gnd	.995 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 11	2.99 μa	≤ 20μa
Current from DATA IN BIT 12 to Gnd	.826 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 12	7.44 μa	≤ 20μa
Current from DATA IN BIT 13 to Gnd	.835 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 14	7.67 μa	≤ 20μa
Current from DATA IN BIT 14 to Gnd	.860 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 14	8.21 μa	≤ 20μa
Current from DATA IN BIT 15 to Gnd	.974 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 15	5.10 μa	≤ 20μa
Current from DATA IN BIT 16 to Gnd	.945 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 17	5.20 μa	≤ 20μa
Current from DATA IN BIT 17 to Gnd	.950 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 17	5.32 μa	≤ 20μa

S/N 103

Date of Test 5-9-75

Tested By [signature]

				Limit
7.6	VERIFICATION OF OPEN COLLECTOR ON OUTPUT SIGNALS			
7.6.3	READ COMPLETE voltage	20	mv	≤ 100 mv
7.6.4	DATA OUT BIT 0 voltage	25	mv	≤ 100 mv
	DATA OUT BIT 1 voltage	20	mv	≤ 100 mv
	DATA OUT BIT 2 voltage	20	mv	≤ 100 mv
	DATA OUT BIT 3 voltage	10	mv	≤ 100 mv
	DATA OUT BIT 4 voltage	10	mv	≤ 100 mv
	DATA OUT BIT 5 voltage	10	mv	≤ 100 mv
	DATA OUT BIT 6 voltage	0	mv	≤ 100 mv
	DATA OUT BIT 7 voltage	0	mv	≤ 100 mv
	DATA OUT BIT 8 voltage	0	mv	≤ 100 mv
	DATA OUT BIT 9 voltage	10	mv	≤ 100 mv
	DATA OUT BIT 10 voltage	25	mv	≤ 100 mv
	DATA OUT BIT 11 voltage	30	mv	≤ 100 mv
	DATA OUT BIT 12 voltage	25	mv	≤ 100 mv
	DATA OUT BIT 13 voltage	30	mv	≤ 100 mv
	DATA OUT BIT 14 voltage	30	mv	≤ 100 mv
	DATA OUT BIT 15 voltage	40	mv	≤ 100 mv
	DATA OUT BIT 16 voltage	25	mv	≤ 100 mv
	DATA OUT BIT 17 voltage	30	mv	≤ 100 mv

S/N 103

Date of Test 5-9-75

Tested By [signature]

			Limits
7.7	POWER CONSUMPTION (25°C)		
7.7.1	Memory +5V Voltage	5.011 Volts	
	Memory -6.1V voltage	6.103 Volts	
	+5V Current	10.5 ma	
	+5V Power	52.615 mw	
7.7.2	Memory -6.1V Current	4.9 ma	
	Memory -6.1V Power	29.904 mw	
7.7.3	Total Memory Idle Power	82.519 mw	170 mw max
7.7.5	Memory +5V Voltage	5.002 Volts	
	Memory -6.1V Voltage	6.100 Volts	
	+5V Current	690 ma	
	+5V Power	3,451.0 mw	
7.7.6	Memory -6.1V Current	238 ma	
	Memory -6.1V Power	1,451.8 mw	
7.7.7	Total Active Power	4,902.8 mw	7000 mw max.
7.8	READ COMPLETE TIMING		
7.8.5	Delay	410 ns	500 ns max.
	Duration	340 ns	250 ns min 450 ns max.

S/N 103 Date of Test 5-9-75

Tested by [signature]

		LIMITS
7.8.7 & 7.8.8	READ COMPLETE/DATA OUTPUT TIMING	
DO-0	OK ✓ REJECT	
DO-1	OK ✓ REJECT	
DO-2	OK ✓ REJECT	
DO-3	OK ✓ REJECT	
DO-4	OK ✓ REJECT	
DO-5	OK ✓ REJECT	
DO-6	OK ✓ REJECT	
DO-7	OK ✓ REJECT	REFER TO TEST PROC.
DO-8	OK ✓ REJECT	
DO-9	OK ✓ REJECT	
DO-10	OK ✓ REJECT	
DO-11	OK ✓ REJECT	
DO-12	OK ✓ REJECT	
DO-13	OK ✓ REJECT	
DO-14	OK ✓ REJECT	
DO-15	OK ✓ REJECT	
DO-16	OK ✓ REJECT	
DO-17	OK ✓ REJECT	

S/N 103

Date of Test 5-9-75
Tested By [signature]

		Limits
7.9	SYSTEM FUNCTIONAL TEST	
7.9.2	Did an error occur?	
	No ✓	
	Yes ____ Address ____ Bits ____	0 errors
7.9.4	Did an error occur?	
	No ✓	
	Yes ____ Address ____ Bits ____	0 errors
7.9.10	Did an error occur?	
	No ✓	
	Yes ____ Address ____ Bits ____	0 errors
7.9.16	Did an error occur?	
	No ✓	
	Yes ____ Address ____ Bits ____	0 errors
7.10	RANDOM ACCESS CAPABILITY	
7.10.6	Did an error occur?	
	No ✓	
	Yes ____ Address ____ Bits ____	0 errors
7.10.7	Did an error occur?	
	a) No ✓	
	Yes ____ Address ____ Bits ____	0 errors

S/N 103

Date of Test 5-9-75
Tested By [signature]

Limits

b) No ✓

Yes ____ Address ____ Bits ____ 0 errors

c) No ✓

Yes ____ Address ____ Bits ____ 0 errors

7.11 NON-VOLATILITY TEST

7.11.7 & 7.11.9 Did an error occur?

No ✓

Yes ____ Address ____ Bits ____ 0 errors

7.12 MEMORY SELECT TEST

7.12.3 Address 0000 (Octal) 0000

7.12.4 Address 0001 0000 (Octal) 0000

0010 0000 (Octal) 0000

0011 0000 (Octal) 0000

0100 0000 (Octal) 0000

0101 0000 (Octal) 0000

0110 0000 (Octal) 0000

0111 0000 (Octal) 0000

1000 0000 (Octal) 0000

1001 0000 (Octal) 0000

1010 0000 (Octal) 0000

S/N 103

Date of Test 5-9-75

Tested By [signature]

		Limits
Address 1011	6000 (Octal)	0000
1100	0000 (Octal)	0000
1101	0000 (Octal)	0000
1110	0000 (Octal)	0000

7.12.6 Did an error occur?

No ✓

Yes _____ Address _____ Bits _____ 0 errors

7.13 WORST CASE PATTERN TEST

7.13.2 Did an error occur?

No ✓

Yes _____ Address _____ Bits _____ 0 errors

7.13.3 Did an error occur?

No ✓

Yes _____ Address _____ Bits _____ 0 errors

S/N 103

Date of Test 5-9-75

Tested By [signature]

			Limits
7.13.4	a)	Did an error occur?	
		No ✓	
		Yes ____ Address ____ Bit ____	0 errors
	b)	Did an error occur?	
		No ✓	
		Yes ____ Address ____ Bit ____	0 errors

CONTROL 41

W.O. 3039

HIGH VACUUM TEST

Unit: PLATED WIRE MEMORY	Project: 4601-400	Date: 5-5-75
Model: N/A	Specification: 12-P13701 D	
Serial: 103	Operator: JOE MOLLERE	
Vacuum System No.: 3	Observer: BOB LOTT (3328)	

TIME	PRESSURE (mm Hg A)	REMARKS
1021	ATM	START TO H. VAC
1030	1.4×10^{-4}	
1100	3.1×10^{-5}	
1130	2×10^{-5}	
1200	1.3×10^{-5}	
1230	1×10^{-5}	
1300	1.7×10^{-6}	
1330	9.8×10^{-6}	
1340	8.6×10^{-6}	VENT TO AMB.
		OPEN BELL JAR-END TEST

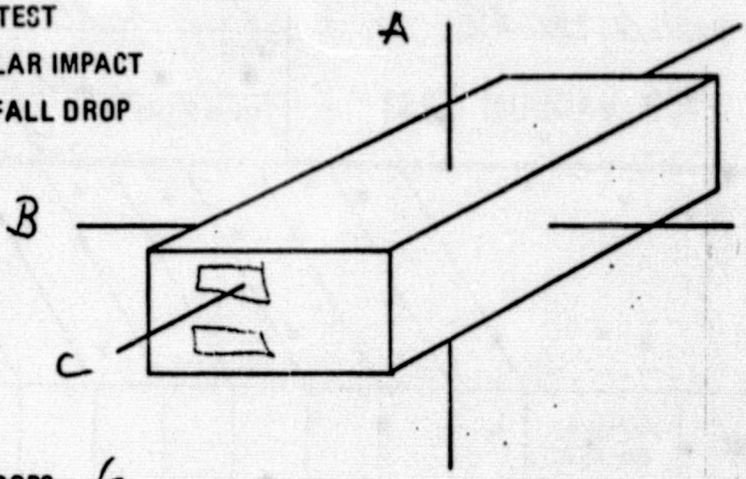
PRECEDING PAGE BLANK NOT FILMED

MOTOROLA INC.
Government Electronics Division

SHOCK TEST (DROP)

PROJECT 4601-400
DATE 5-8-75
SHEET 1 OF 1
W.O. NO. 3040
CONTROL NO. 11
UNIT PWM
SERIAL NO. 103
OPERATOR [illegible]
OBSERVER [illegible]
VIBRATION MOUNTS
NO. OF DROPS PER ~~FACE~~ AXIS ~~[illegible]~~ below TOTAL NO. OF DROPS 6
ACCELERATION 30 G'S
PULSE DURATION 6 & 12 MS
SPEC DETAILS 12-P137220

TYPE OF TEST
☒ MODULAR IMPACT
☐ FREE FALL DROP



DROP HEIGHT 1 3/4 & 4 3/4 IN.
PROGRAMMER PRESSURE NA P.S.I.
TYPE OF WAVESHAPE 1/2 sine
BANDPASS FILTER .2 LOW FR. Hz
4300 HIGH FR. Hz
REMARKS 3 drops at 6 ms & 3 drops at 12 ms

Pads for 12 ms: 8x8x1/4 Plastic
2 - 8x8x1/4" rubber
3 - 8x8x1/16 rubber
3 - 1" blue closed
1 - 1" blue open

PAD AND PLATE CONFIGURATION		
ITEM NO.	PART NO.	α DESCRIPTION
1	MRL 2359	alum plate (B)
2	MOT 2796	1" red open (B)
3	MOT 2358	alum plate (T)
4		
5		
6		
7		
8		
9		

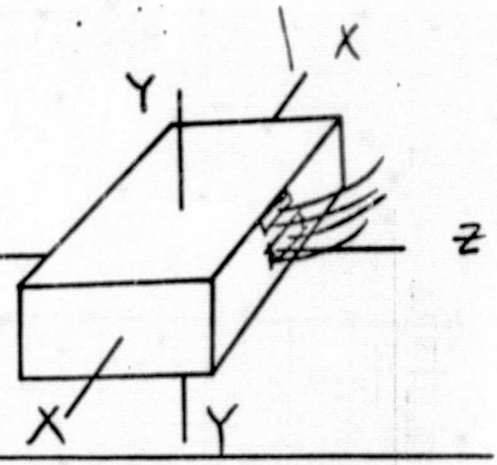
AXIS	FACE	1 (6 ms)	2	3	4 (12 ms)	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	1	/			/																
	2																				
B	1	/			/																
	2																				
C	1	/			/																
	2																				

Test complete

MOTOROLA INC.
Government Electronics Division

VIBRATION TEST

SHEET 1 OF 1 DATE 5-6-75
PROJECT 4601-400 UNIT PLATED WIRE MEMORY
CONTROL NO. 01-02 W.O. NO. 3041
OPERATOR O SMITH
OBSERVER L. GOULDIN
CYCLE TIME 2 MIN/AXIS FREQ. 15 TO 2K Hz SHAPED RANDOM
SPEC DETAILS 12-P13722 D



AXIS / RUN NO	TIME START	TIME STOP	~~ACCUM.~~ ULATED VIB. TIME	UNIT SER. NO.	DISPLACEMENT INCHES D.A.	ACCELERATION RMS PK G'S / MV (RMS)	REMARKS
Z 1	1757	1759	2 MIN	103	NA	5.61 / 56.1	SHAPED RANDOM NOISE
Z 2	1901	20 1901	20SEC	103	NA	5.61 / 56.1	" " "
Z 3	1938	20 1938	20SEC	103	NA	5.61 / 56.1	" " "
Z 4	1954	21 1958	4 21	103	.33"	10-5 / ~~20.7-35.3~~	5-2K HZ
X 5	2111	2113	2 MIN	103	NA	5.61 / 56.1	SHAPED RANDOM NOISE
X 6	2119	21 2123	4 21	103	.33"	10-5 / ~~20.7-35.3~~	5-2KHZ
Z 7	2148	20 2148	20SEC	103	NA	5.61 / 56.1	SHAPED RANDOM NOISE
Y 8	2248	21 2252	4 21	103	.33"	10-5 / ~~20.7-35.3~~	5-2KHZ
Y 9	2257	2259	2 MIN	103	NA	5.61 / 56.1	SHAPED RANDOM NOISE
					←		END TEST

Plated

PROJECT 4601-100 UNIT Wire Memory SER. NO. 103

X AXIS SAMPLE (LOOP) TIME 10 SECONDS

FILTER B.W. 1. 5 HZ SCAN RATE 1.125 HZ AVG. TIME 10 SECONDS
2. 10 HZ SCAN RATE 2.25 HZ AVG. TIME 10 SECONDS
3. 20 HZ SCAN RATE 3.5 HZ AVG. TIME 10 SECONDS
4. 50 HZ SCAN RATE 14.25 HZ AVG. TIME 10 SECONDS

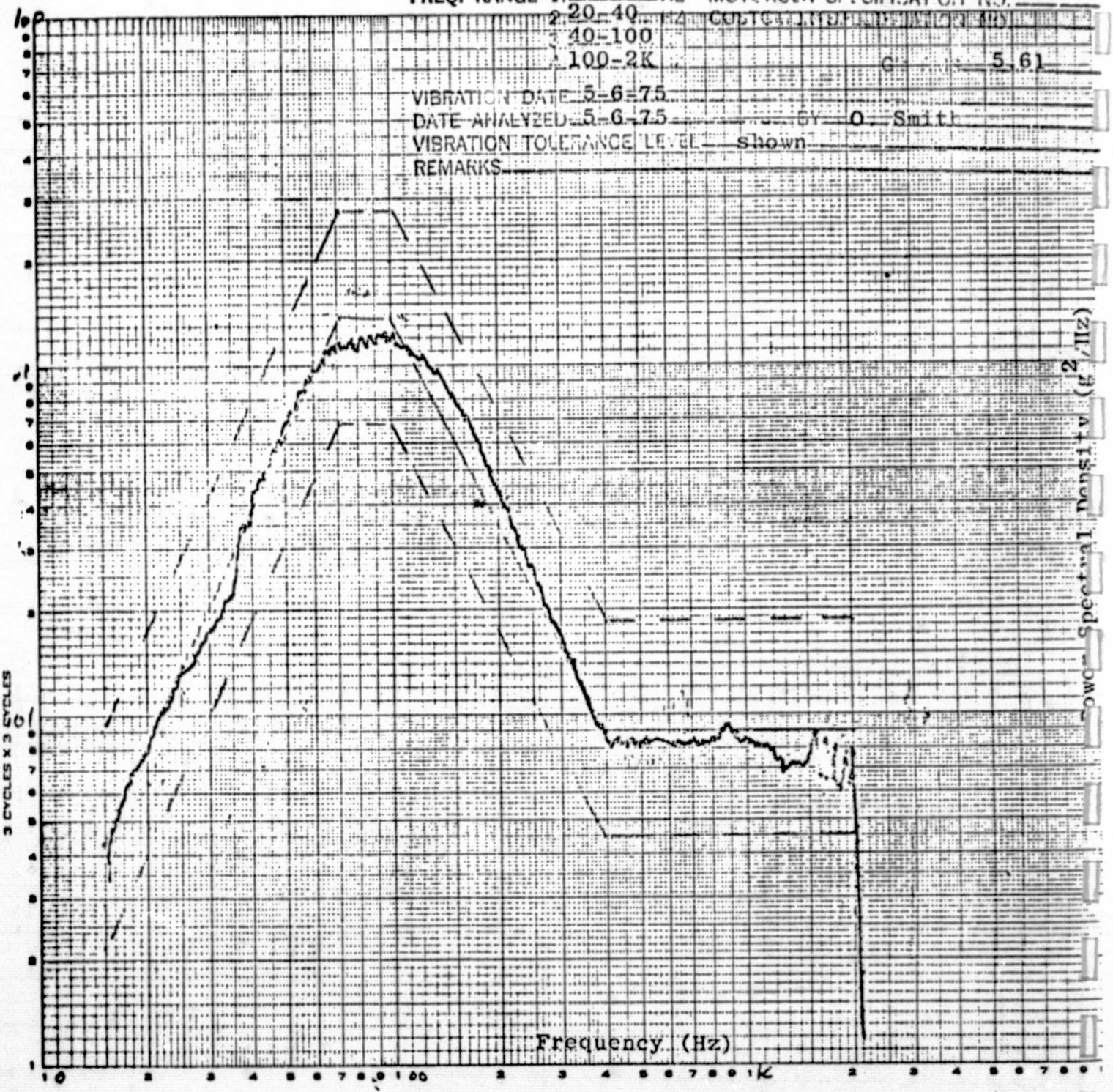
FREQ. RANGE 1. 15-20 HZ MOTOROLA SPECIFICATION NO.
2. 20-40 HZ CUSTOMER SPECIFICATION NO.
3. 40-100
4. 100-2K G 5.61

VIBRATION DATE 5-6-75

DATE ANALYZED 5-6-75 BY O. Smith

VIBRATION TOLERANCE LEVEL shown

REMARKS



G²/Hz Power Spectral Density

EUGENE DIETZGEN CO. MADE IN U.S.A.

NO. 340-L33 DIETZGEN GRAPH PAPER LOGARITHMIC 3 CYCLES X 3 CYCLES

ORIGINAL PAGE IS
OF POOR QUALITY

Plated

PROJECT 1601-100 UNIT Wire Memory SER. NO. 103

X AXIS SAMPLE (LOOP) TIME 10 SECONDS

FILTER B.W. 1. 5 HZ SCAN RATE 1125 HZ AVG. TIME 1. 10 SECONDS
2 10 HZ SCAN RATE 225 HZ AVG. TIME 2. 10 SECONDS
3 20 HZ SCAN RATE 35 HZ AVG. TIME 3. 10 SECONDS
4 50 HZ SCAN RATE 1425 HZ AVG. TIME 4. 10 SECONDS

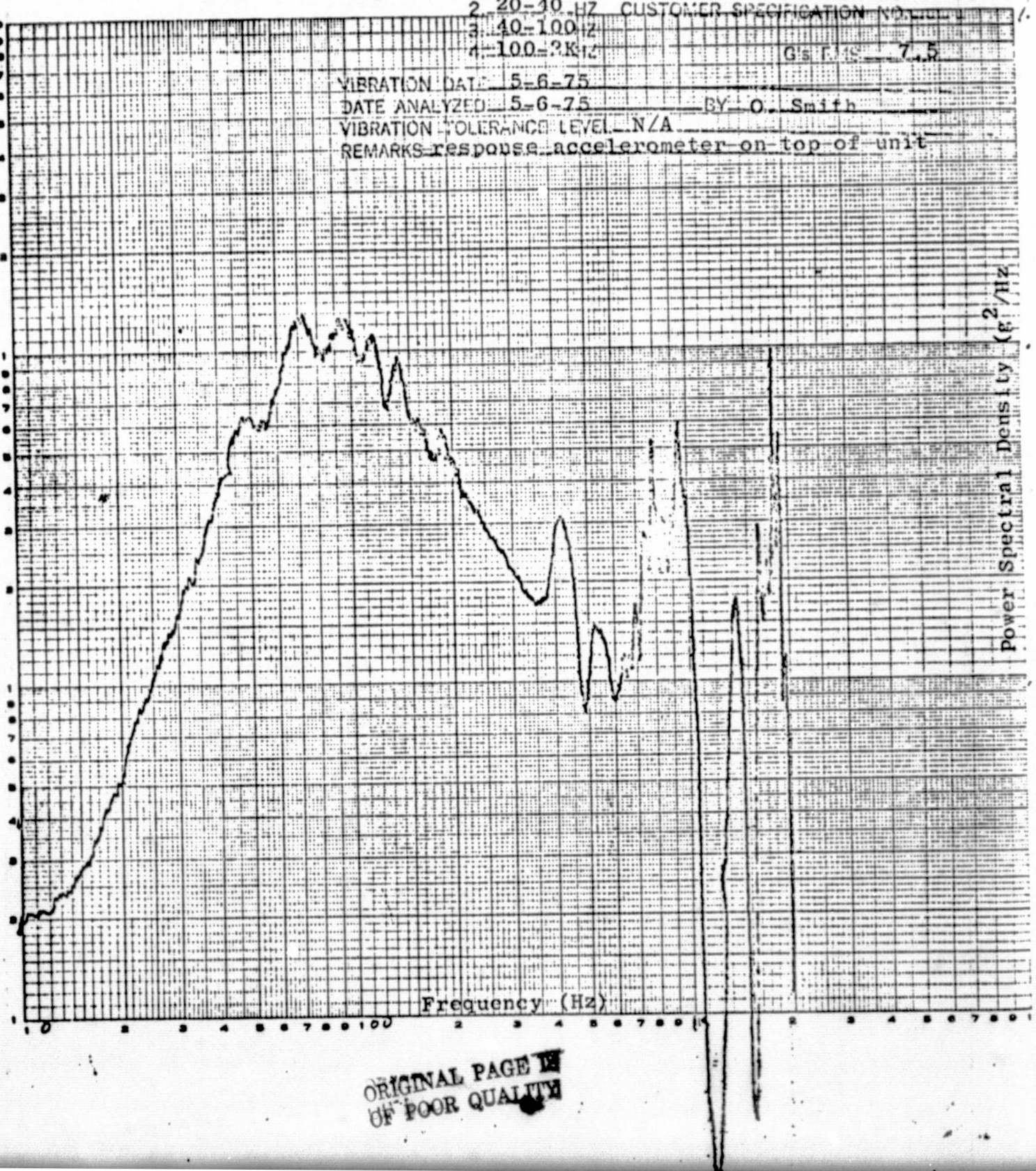
FREQ. RANGE 1. 15-20 HZ MOTOROLA SPECIFICATION NO. ____
2. 20-40 HZ CUSTOMER SPECIFICATION NO. ____
3. 40-100 HZ
4. 100-2K HZ G's RMS 7.5

VIBRATION DATA 5-6-75

DATE ANALYZED 5-6-75 BY O. Smith

VIBRATION TOLERANCE LEVEL N/A

REMARKS response accelerometer on top of unit



EUGENE DIETZGEN CO. MADE IN U.S.A.

NO. 340-L33 DIETZGEN GRAPH PAPER 21TH 3 CYCLES X 3 CYCLES

ORIGINAL PAGE IS
OF POOR QUALITY

PROJECT [illegible] UNIT Wire Memory SER. NO. 103

Y AXIS SAMPLE (LOOP) TIME 10 SECONDS

FILTER B.W. 1. 5HZ SCAN RATE 1.125 AVG. TIME 1.10 SECONDS
2. 10HZ SCAN RATE 2.25HZ AVG. TIME 2.10 SECONDS
3. 20HZ SCAN RATE 3.5 HZ AVG. TIME 3.10 SECONDS
4. 50HZ SCAN RATE 11.25HZ AVG. TIME 4.10 SECONDS

FREQ. RANGE 1 15-20 HZ MOTOROLA SPECIFICATION NO.
2 20-40 HZ CUSTOMER SPECIFICATION NO.
3 40-100 HZ
4 100-2K HZ 5.61

VIBRATION DATE 5-6-75
DATE ANALYZED 5-6-75 O. Smith
VIBRATION TOLERANCE LEVEL shown
REMARKS

Power Spectral Density (g^2/Hz)

Frequency (Hz)

10 2 3 4 5 6 7 8 9 100 2 3 4 5 6 7 8 9 1K 2 3 4 5 6 7 8 9

EUGENE DIETZGEN CO. MADE IN U. S. A.

NO. 340-L33 DIETZGEN GRAPH PAPER LOGARITHMIC 3 CYCLES X 3 CYCLES

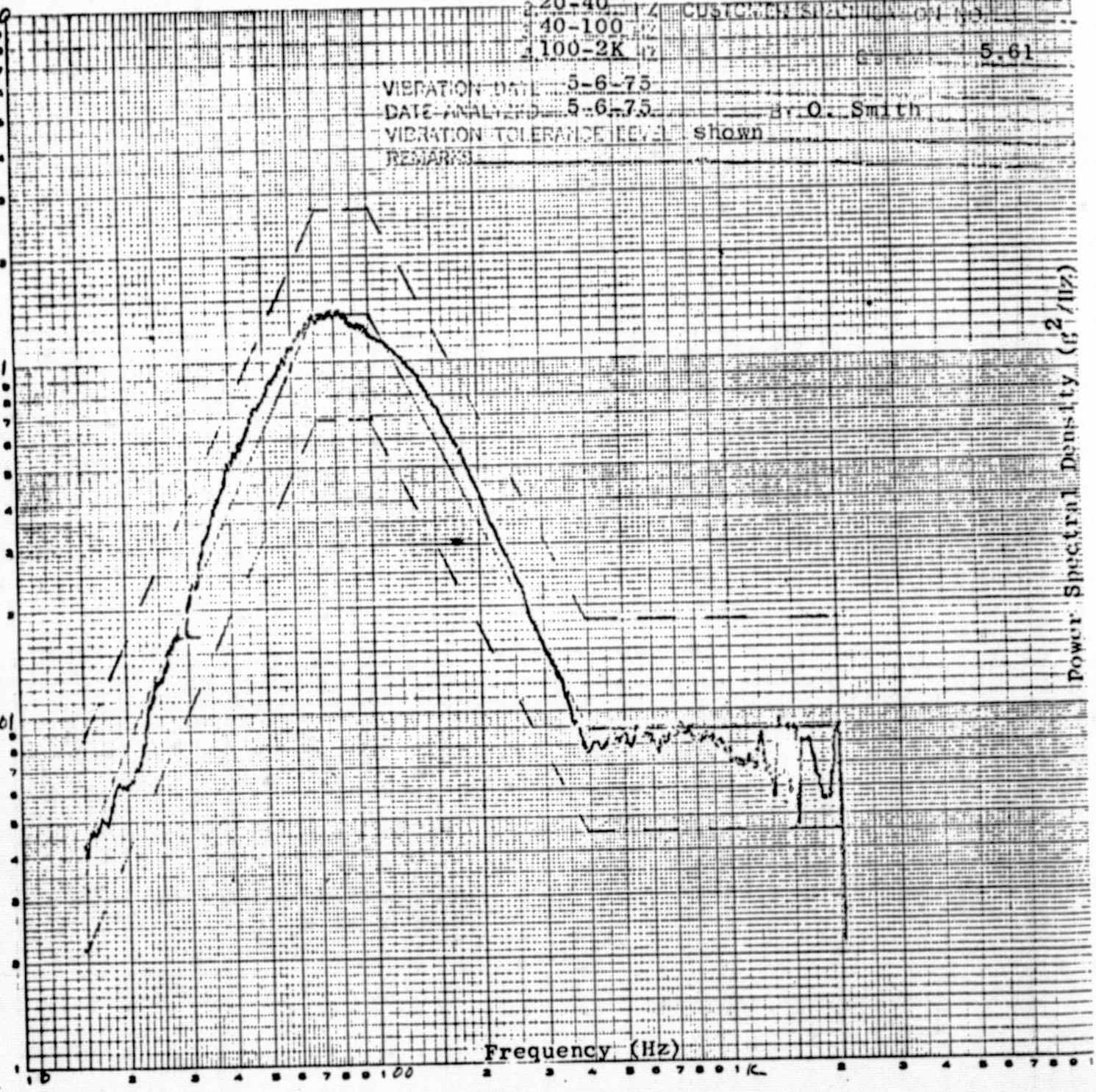
PROJECT 4601-400 UNIT Wire Memory SER. NO. 103

Z AXIS SAMPLE (LOOP) TIME 10 SECONDS

FILTER B.W., 1. 5 HZ SCAN RATE 1.125 HZ AVG. TIME 1 10 SECONDS
2. 10 HZ SCAN RATE 2.25 HZ AVG. TIME 2 10 SECONDS
3. 20 HZ SCAN RATE 4.5 HZ AVG. TIME 3 10 SECONDS
4. 50 HZ SCAN RATE 14.25 HZ AVG. TIME 4 10 SECONDS

FREQ. RANGE 1. 15-20 HZ MOTOROLA SPECIFICATION NO.
2. 20-40 HZ CUSTOMER SPECIFICATION (IF ANY)
3. 40-100 HZ
4. 100-2K HZ Gs 5.61

VIBRATION DATE 5-6-75
DATE ANALYZED 5-6-75 BY O. Smith
VIBRATION TOLERANCE LEVEL shown
REMARKS



EUGENE DIETZGEN CO. MADE IN U.S.A.

NO. 340-L33 DIETZGEN GRAPH PAPER CAR C 3 CYCLES X 3 CYCLES

ORIGINAL PAGE IS
OF POOR QUALITY

Plated

PROJECT 1601-400 UNIT Wire Memory SER. NO. 103

Z AXIS SAMPLE (LOOP) TIME 10 SECONDS

FILTER B.W. 1. 5 HZ SCAN RATE 1.125 HZ A.C. TIME 10 SECONDS

2 10 HZ SCAN RATE 2.25 A.C. TIME 10

20 HZ SCAN RATE 4.5 10

50 HZ SCAN RATE 11.25 10

FREQ. RANGE 1 15-20 HZ MANUAL

20-40 HZ CUSTOM

40-100

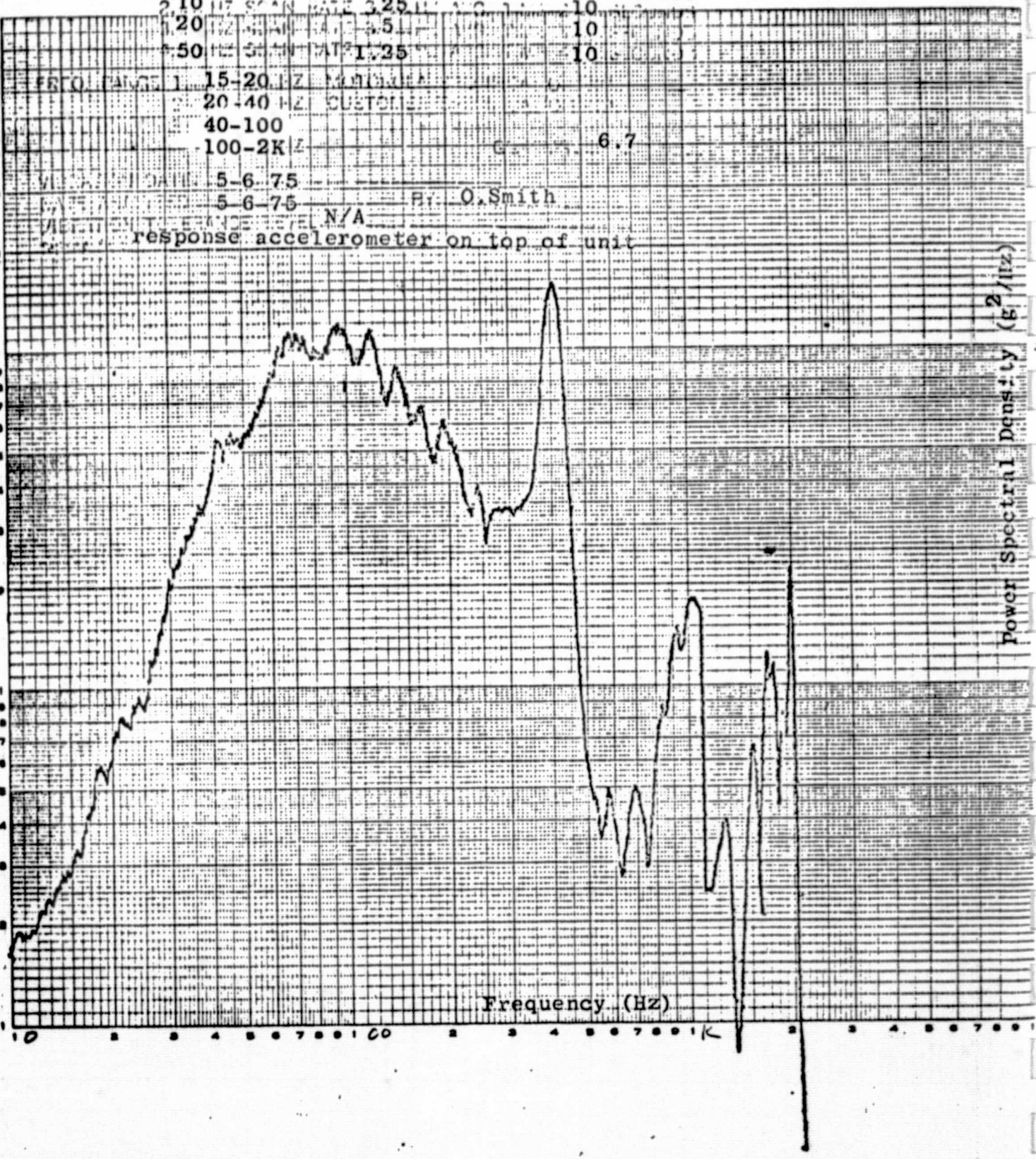
100-2K HZ G 6.7

5-6-75

5-6-75 BY O.Smith

N/A

response accelerometer on top of unit



EUGENE DIETZGEN CO. MADE IN U.S.A.

NO. 340-L33 DIETZGEN GRAPH PAPER LOGARITHMIC 3 CYCLES X 3 CYCLES

K&E AUDIO FREQUENCY
KEUFFEL & ESSER CO. MADE IN U.S.A.

46 6882

X

PLATED WIRE

PROJECT 46A-402 UNIT MEMORY SER. NO 103

X AXIS FREQ. RANGE 5-2KHZ

PLOTTER CAL FREQ X Y 10 DB/in

ACCELERATION 10-5 PKGS. DISPLACEMENT .33" DA

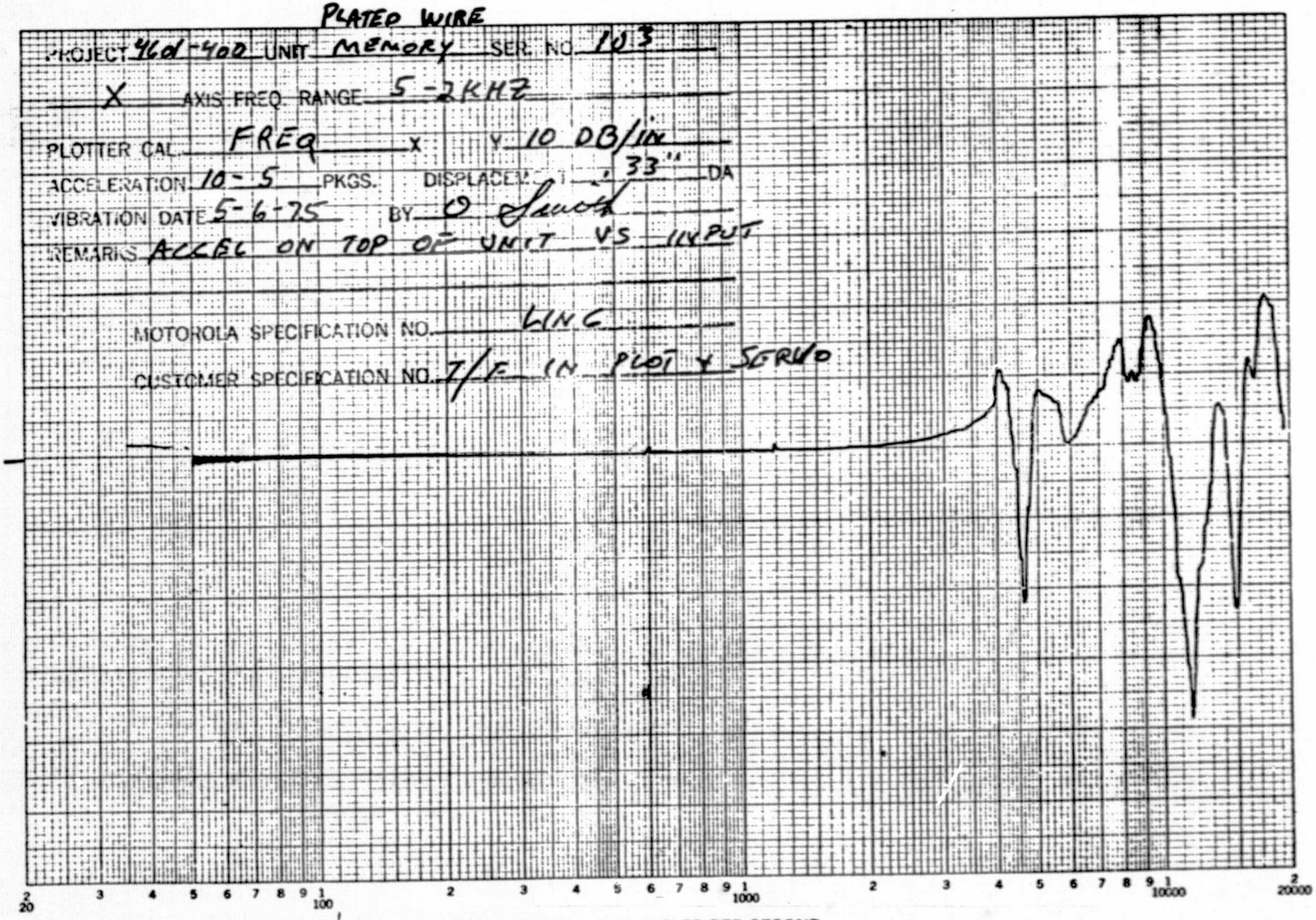
VIBRATION DATE 5-6-75 BY D Smith

REMARKS ACCEL ON TOP OF UNIT VS INPUT

MOTOROLA SPECIFICATION NO. LINC

CUSTOMER SPECIFICATION NO. T/E IN PLOT Y SERVO

T=1



FREQUENCY IN CYCLES PER SECOND

K·E AUDIO FREQUENCY KEUFFEL & ESSER CO. MADE IN U.S.A.

46 6882

Z

PLATED WIRE

PROJECT Hlor-400 UNIT MEMORY SER. NO. 103

Z AXIS FREQ. RANGE 5 - 2KHZ

PLOTTER CAL FREQ X Y 10 DB/IN

ACCELERATION 10 - 5 PKGS. DISPLACEMENT .33" DA

VIBRATION DATE 5-6-75 BY O SMITH

REMARKS ACCEL ON TOP OF UNIT VS INPUT

MOTOROLA SPECIFICATION NO. LINK

CUSTOMER SPECIFICATION NO. T/F IN PLOT & SERVO

T=1 -

2 3 4 5 6 7 8 9 1 2 3 4 5 6 7 8 9 1 2 3 4 5 6 7 8 9 1 2
20 100 1000 10000 20000

FREQUENCY IN CYCLES PER SECOND

ATTACHMENT III

ACCEPTANCE TEST DATA SHEET,

LOW POWER RANDOM ACCESS SP

SPACECRAFT MEMORY

PART NO. 12-P13721D

DRAWING NO. 12-P13721D

SERIAL NUMBER 104

(35 PAGES)

* APPLICATION	
NEXT ASSEMBLY	USED ON

*ASTERISK INDICATES DATA WHICH IS NONMANDATORY OR FOR INFORMATION ONLY.

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
X1	Initial Release	—	—
X2	Incorporated changes prior to First Usage	3-16-73	H. Tweed
X3	Change -6.9V to -6.1V	6-18-73	H. Tweed
X4	Change 6000mw to 7000mw, pages 10, 17, 19, 30. Change weight from 6.0 to 6.5 pounds, page 2.	7-24-73	H. Tweed
X5	Add weight 5.8 pounds for magnesium chassis MCO S7835.	2-10-75	
X6	Revised per MCO S7845	4-28-75	

S.N 109

REV		X1	X4	X1	X3	X1	X1	X1	X1	X1																				
SHEET		27	28	29	30	31	32	33	34	35																				
REV STATUS	REV		X5	X5	X1	X1	X1	X1	X1	X1	X1	X1	X4	X1	X1	X1	X1	X1	X6	X6	X6	X6	X6	X1	X1	X1	X1	X1	X1	
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26			

FOR ASSOCIATED LISTS SEE

INTERPRET DRAWING IN ACCORDANCE WITH STANDARDS PRESCRIBED BY

UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES AND END USE. FOR TOLERANCES SEE NOTE

MATERIAL:

DR BY H. Tweed

CHK BY

MFG

PROJ NO. 4339 4601

CONTR NO. NAS5-23163 NAS5-20576

RELEASE NOTICE

APPROVED DATE 1-2-73 H. Tweed

APPROVED DATE

MOTOROLA INC. Government Electronics Division / 8201 EAST McDOWELL ROAD SCOTTSDALE, ARIZONA 85252

ACCEPTANCE TEST DATA SHEET, LOW POWER RANDOM ACCESS SPACE-CRAFT MEMORY, PART NO. 01-P13701D

SIZE	CODE IDENT NO.	DWG. NO.
A	94990	12-P13721D

SCALE

SHEET 1 OF 35

1. SCOPE

This test data sheet is to be used to record data as required by the Acceptance Test Procedure for the Low Power Random Access Spacecraft Memory.

2. REFERENCE INFORMATION

2.1 SPECIFICATIONS APPLICABLE

S-562-P-26	Low Power Random Access Spacecraft Memory
12-P13722D	Acceptance Test Procedure, Low Power Random Access Spacecraft Memory

3. TEST DATA

Unit S/N 104 Start Date of Tests 5/28/75

Tested by [signature]

ATP PARA. NO.

3.1 EQUIVALENT TEST EQUIPMENT

DC Millimeter H.P 428A 0-1A
Digital Voltmeter Fluke 8120A (Multimeter)
Counter HP5245L

4. PHYSICAL CHARACTERISTICS Limit

6.1 WEIGHT

Weight of LP-RASM = 5.562 Pounds 6.5 pounds (aluminum)
5.8 pounds (magnesium)

MOTOROLA INC. Government Electronics Division 8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252	SIZE A	CODE IDENT NO. 94990	DWG NO. 12-P13721D
	SCALE	REVISION	SHEET 2

S/N 109 Date of Test 5/28/75

Tested By

6.2 DIMENSIONS

		Limit
H =	2.895 inches	
W =	5.630 inches	
MW =	0.955 inches	
D =	1.322 inches	
MD =	~~1.670~~ 1.676 inches	
V = H X W X D =	157.66 inches^3	≤ 160 inches^3

MOTOROLA INC. Government Electronics Division 8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252	SIZE A	CODE IDENT NO. 94990	DWG NO. 12-P13721D
	SCALE	REVISION	SHEET 3

S/N 104

Date of Test 5/28/75

Tested By [signature]

			Limit
7.4	CHASSIS ISOLATION		
	Impedance	> 9 meg Ω	≥ 9 megohms
7.5	INPUT SIGNAL LOADING		
7.5.2	Current from INITIATE PULSE to Gnd	1.405 ma	≤ 2 ma
	Current from 2.4V to INITIATE PULSE	1.40 μa	≤ 20 μa
7.5.3	Current from MEM SEL 1 to Gnd	1.403 ma	≤ 2 ma
	Current from 2.4V to MEM SEL 1	1.04 μa	≤ 20 μa
7.5.4	Current from MEM SEL 2 to Gnd	1.407 ma	≤ 2 ma
	Current from 2.4V to MEM SEL 2	1.41 μa	≤ 20 μa
	Current from MEM SEL 3 to Gnd	1.408 ma	≤ 2 ma
	Current from 2.4V to MEL SEL 3	1.42 μa	≤ 20 μa
	Current from MEM SEL 4 to Gnd	1.401 ma	≤ 2 ma
	Current from 2.4V to MEM SEL 4	1.02 μa	≤ 20 μa
7.5.5	Current from READ/WRITE to Gnd	1.008 ma	≤ 2 ma
	Current from 2.4V to READ/WRITE	1.30 μa	≤ 20 μa
7.5.6	Current from ADDRESS 2^0 to Gnd	.912 ma	≤ 2 ma
	Current from 2.4V to ADDRESS 2^0	5.62 μa	≤ 20 μa

S/N 104

Date of Test 5/28/75

Tested By [signature]

		Limits
Current from ADDRESS 2^1 to Gnd	.918 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^1	6.17 μa	≤ 20 μa
Current from ADDRESS 2^2 to Gnd	.985 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^2	7.06 μa	≤ 20 μa
Current from ADDRESS 2^3 to Gnd	.916 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^3	7.80 μa	≤ 20 μa
Current from ADDRESS 2^4 to Gnd	.965 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^4	8.22 μa	≤ 20 μa

S/N 104

Date of Test 5/28/75

Tested By [signature]

		Limits
Current from ADDRESS 2^5 to Gnd	.906 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^5	5.69 μa	≤ 20μa
Current from ADDRESS 2^6 to Gnd	.901 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^5	5.79 μa	≤ 20μa
Current from ADDRESS 2^7 to Gnd	.973 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^7	6.62 μa	≤ 20μa
Current from ADDRESS 2^8 to Gnd	.946 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^8	1.44 μa	≤ 20μa
Current from ADDRESS 2^9 to Gnd	.935 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^9	1.14 μa	≤ 20μa
Current from ADDRESS 2^{10} to Gnd	1.006 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^{10}	1.32 μa	≤ 20μa
Current from ADDRESS 2^{11} to Gnd	1.008 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^{11}	1.36 μa	≤ 20μa
Current from DATA IN BIT 0 to Gnd	1.061 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 0	7.59 μa	≤ 20μa

S/N 104

Date of Test 5/28/75

Tested By [signature]

		Limits
Current from DATA IN BIT 1 to Gnd	1.072 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 1	7.70 μa	≤ 20 μa
Current from DATA IN BIT 2 to Gnd	1.081 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 2	7.00 μa	≤ 20 μa
Current from DATA IN BIT 3 to Gnd	1.045 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 3	9.68 μa	≤ 20 μa
Current from DATA IN BIT 4 to Gnd	1.037 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 4	9.62 μa	≤ 20 μa
Current from DATA IN BIT 5 to Gnd	1.052 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 5	9.36 μa	≤ 20 μa
Current from DATA IN BIT 6 to Gnd	1.073 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 6	7.88 μa	≤ 20 μa
Current from DATA IN BIT 7 to Gnd	1.057 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 7	7.67 μa	≤ 20 μa
Current from DATA IN BIT 8 to Gnd	1.051 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 8	8.11 μa	≤ 20 μa
Current from DATA IN BIT 9 to Gnd	.991 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 9	8.46 μa	≤ 20 μa

S/N 104

Date of Test 5/28/75

Tested By [signature]

		Limits
Current from DATA IN BIT 10 to Gnd	.999 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 10	9.31 μa	≤ 20μa
Current from DATA IN BIT 11 to Gnd	1.003 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 11	8.41 μa	≤ 20μa
Current from DATA IN BIT 12 to Gnd	1.053 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 12	9.86 μa	≤ 20μa
Current from DATA IN BIT 13 to Gnd	1.056 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 14	9.53 μa	≤ 20μa
Current from DATA IN BIT 14 to Gnd	1.070 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 14	9.27 μa	≤ 20μa
Current from DATA IN BIT 15 to Gnd	1.056 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 15	6.31 μa	≤ 20μa
Current from DATA IN BIT 16 to Gnd	1.040 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 17	6.43 μa	≤ 20μa
Current from DATA IN BIT 17 to Gnd	1.062 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 17	7.57 μa	≤ 20μa

S/N 104

Date of Test 5/28/75

Tested By [signature]

				Limit
7.6	VERIFICATION OF OPEN COLLECTOR ON OUTPUT SIGNALS			
7.6.3	READ COMPLETE voltage	50	mv	≤ 100 mv
7.6.4	DATA OUT BIT 0 voltage	20	mv	≤ 100 mv
	DATA OUT BIT 1 voltage	20	mv	≤ 100 mv
	DATA OUT BIT 2 voltage	10	mv	≤ 100 mv
	DATA OUT BIT 3 voltage	20	mv	≤ 100 mv
	DATA OUT BIT 4 voltage	10	mv	≤ 100 mv
	DATA OUT BIT 5 voltage	0	mv	≤ 100 mv
	DATA OUT BIT 6 voltage	10	mv	≤ 100 mv
	DATA OUT BIT 7 voltage	0	mv	≤ 100 mv
	DATA OUT BIT 8 voltage	0	mv	≤ 100 mv
	DATA OUT BIT 9 voltage	20	mv	≤ 100 mv
	DATA OUT BIT 10 voltage	20	mv	≤ 100 mv
	DATA OUT BIT 11 voltage	20	mv	≤ 100 mv
	DATA OUT BIT 12 voltage	20	mv	≤ 100 mv
	DATA OUT BIT 13 voltage	25	mv	≤ 100 mv
	DATA OUT BIT 14 voltage	40	mv	≤ 100 mv
	DATA OUT BIT 15 voltage	10	mv	≤ 100 mv
	DATA OUT BIT 16 voltage	10	mv	≤ 100 mv
	DATA OUT BIT 17 voltage	10	mv	≤ 100 mv

S/N 104

Date of Test 5/28/75

Tested By [signature]

			Limits
7.7	POWER CONSUMPTION (25°C)		
7.7.1	Memory +5V Voltage	5.005 Volts	
	Memory -6.1V voltage	6.103 Volts	
	+5V Current	10.1 ma	
	+5V Power	50.5505 mw	
7.7.2	Memory -6.1V Current	3.15 ma	
	Memory -6.1V Power	19.22445 mw	
7.7.3	Total Memory Idle Power	69.77495 mw	170 mw max
7.7.5	Memory +5V Voltage	5.001 Volts	
	Memory -6.1V Voltage	6.105 Volts	
	+5V Current	665 ma	
	+5V Power	3325.665 mw	
7.7.6	Memory -6.1V Current	225 ma	
	Memory -6.1V Power	1373.625 mw	
7.7.7	Total Active Power	4699.290 mw	7000 mw max.
7.8	READ COMPLETE TIMING		
7.8.5	Delay	395 ns	500 ns max.
	Duration	320 ns	250 ns min 450 ns max.

S/N 104

Date of Test 5/28/75

Tested by [signature]

7.8.7 & 7.8.8 READ COMPLETE/DATA OUTPUT TIMING

		LIMITS
DO-0	OK ✓ REJECT	
DO-1	OK ✓ REJECT	
DO-2	OK ✓ REJECT	
DO-3	OK ✓ REJECT	
DO-4	OK ✓ REJECT	
DO-5	OK ✓ REJECT	
DO-6	OK ✓ REJECT	
DO-7	OK ✓ REJECT	REFER TO TEST PROC.
DO-8	OK ✓ REJECT	
DO-9	OK ✓ REJECT	
DO-10	OK ✓ REJECT	
DO-11	OK ✓ REJECT	
DO-12	OK ✓ REJECT	
DO-13	OK ✓ REJECT	
DO-14	OK ✓ REJECT	
DO-15	OK ✓ REJECT	
DO-16	OK ✓ REJECT	
DO-17	OK ✓ REJECT	

S/N 104

Date of Test 5/28/75
Tested By [illegible]

		Limits
7.9	SYSTEM FUNCTIONAL TEST	
7.9.2	Did an error occur?	
	No X	
	Yes ____ Address ____ Bits ____	0 errors
7.9.4	Did an error occur?	
	No X	
	Yes ____ Address ____ Bits ____	0 errors
7.9.10	Did an error occur?	
	No X	
	Yes ____ Address ____ Bits ____	0 errors
7.9.16	Did an error occur?	
	No X	
	Yes ____ Address ____ Bits ____	0 errors
7.10	RANDOM ACCESS CAPABILITY	
7.10.6	Did an error occur?	
	No X	
	Yes ____ Address ____ Bits ____	0 errors
7.10.7	Did an error occur?	
	a) No X	
	Yes ____ Address ____ Bits ____	0 errors

S/N 104

Date of Test 5/28/75
Tested By [signature]

			Limits
	b) No X		
	Yes ____ Address ____ Bits ____		0 errors
	c) No X		
	Yes ____ Address ____ Bits ____		0 errors
7.11	NON-VOLATILITY TEST		
7.11.7 & 7.11.9	Did an error occur? No X		
	Yes ____ Address ____ Bits ____		0 errors
7.12	MEMORY SELECT TEST		
7.12.3	Address 0000 (Octal)		0000
7.12.4	Address 0001 0000 (Octal)		0000
	0010 0000 (Octal)		0000
	0011 0000 (Octal)		0000
	0100 0000 (Octal)		0000
	0101 0000 (Octal)		0000
	0110 0000 (Octal)		0000
	0111 0000 (Octal)		0000
	1000 0000 (Octal)		0000
	1001 0000 (Octal)		0000
	1010 0000 (Octal)		0000

S/N 104

Date of Test 5/28/75

Tested By [illegible]

		Limits
Address 1011	0000 (Octal)	0000
1100	0000 (Octal)	0000
1101	0000 (Octal)	0000
1110	0000 (Octal)	0000

7.12.6 Did an error occur?

No X

Yes _____ Address _____ Bits _____ 0 errors

7.13 WORST CASE PATTERN TEST

7.13.2 Did an error occur?

No X

Yes _____ Address _____ Bits _____ 0 errors

7.13.3 Did an error occur?

No X

Yes _____ Address _____ Bits _____ 0 errors

S/N 104

Date of Test 5/28/75

Tested By [signature]

			Limits
7.13.4	a)	Did an error occur?	
		No X	
		Yes ____ Address ____ Bit ____	0 errors
	b)	Did an error occur?	
		No X	
		Yes ____ Address ____ Bit ____	0 errors

S/N 104

DATE OF TEST 5/29/73

TESTED BY [signature]

8.	TEMPERATURE TEST	LIMITS
8.2.1	TIME 7:00	
8.2.2	LOW TEMPERATURE	
	THERMISTOR RESISTANCE	
	150 MINUTES 200 K OHMS	
	160 MINUTES 204 K OHMS % CHANGE 2%	
	170 MINUTES _____ K OHMS % CHANGE _____	
	180 MINUTES _____ K OHMS % CHANGE _____	
	190 MINUTES _____ K OHMS % CHANGE _____	
8.2.3	DID AN ERROR OCCUR?	
	NO X	
	YES _____ ADDRESS _____ BITS _____	0 ERRORS
8.2.4	-6.1 V VOLTAGE 6.404 VOLTS	+5 V VOLTAGE 5.247 VOLTS
	-6.1 V CURRENT 14.0 ma	+5 V CURRENT 10.8 ma
	-6.1 V POWER 89.656 mw	+5 V POWER 56.6892 mw
	TOTAL MEMORY IDLE POWER 146.3452 mw	170 mw MAX
8.2.5	-6.1 V VOLTAGE 6.401 VOLTS	+5 V VOLTAGE 5.249 VOLTS
	-6.1 V CURRENT 254 ma	+5 V CURRENT 685 ma
	-6.1 V POWER 1625.854 mw	+5 V POWER 3595.565 mw
	TOTAL MEMORY OPERATING POWER 5221.49 mw	7000 mw MAX

(M 1189)

S/N 104

DATE OF TEST 5/28/75

TESTED BY [signature]

		LIMITS
8.2.6	DID AN ERROR OCCUR?	
	NO X	
	YES ____ ADDRESS ____ BIT ____	0 ERRORS
8.2.8	WC a) DID AN ERROR OCCUR?	
	NO X	
	YES ____ ADDRESS ____ BIT ____	0 ERRORS
	WC b) DID AN ERROR OCCUR?	
	NO X	
	YES ____ ADDRESS ____ BIT ____	0 ERRORS
	WC c) DID AN ERROR OCCUR?	
	NO X	
	YES ____ ADDRESS ____ BIT ____	0 ERRORS
	WC d) DID AN ERROR OCCUR?	
	NO X	
	YES ____ ADDRESS ____ BIT ____	0 ERRORS
8.2.11	WC a) DID AN ERROR OCCUR?	
	NO X	
	YES ____ ADDRESS ____ BIT ____	0 ERRORS

S/N 104

DATE OF TEST 5/29/76

TESTED BY [signature]

LIMITS

8.2.11 (Cont.)

WC b) DID AN ERROR OCCUR?

NO X

YES ___ ADDRESS ___ BIT ___ 0 ERRORS

WC c) DID AN ERROR OCCUR?

NO X

YES ___ ADDRESS ___ BIT ___ 0 ERRORS

WC d) DID AN ERROR OCCUR?

NO X

YES ___ ADDRESS ___ BIT ___ 0 ERRORS

8.3 INTERMEDIATE TEMPERATURE TEST

TIME 10:16

8.3.2

TIME	THERMISTOR READING.		DID ANY ERROR OCCUR?		
10:26	136K	K OHMS	NO X	YES ___	0 ERRORS
10:36	72.6	K OHMS	NO X	YES ___	0 ERRORS
10:46	34.9	K OHMS	NO X	YES ___	0 ERRORS
10:56	19.7	K OHMS	NO X	YES ___	0 ERRORS
11:06	11.6	K OHMS	NO X	YES ___	0 ERRORS
11:16	7.12	K OHMS	NO X	YES ___	0 ERRORS
11:26	4.64	K OHMS	NO X	YES ___	0 ERRORS
11:36	3.41	K OHMS	NO X	YES ___	0 ERRORS
11:46	2.57	K OHMS	NO X	YES ___	0 ERRORS
11:56	2.09	K OHMS	NO X	YES ___	0 ERRORS
12:06	1.71	K OHMS	NO X	YES ___	0 ERRORS
___	___	K OHMS	NO ___	YES ___	0 ERRORS

S/N 104

DATE OF TEST 5/29/75

TESTED BY [signature]

LIMITS

8.3.3 TIME 11:30

8.4 50 MINUTES — K OHMS

60 MINUTES — K OHMS % CHANGE

70 MINUTES — K OHMS % CHANGE

80 MINUTES 1.51 K OHMS % CHANGE

90 MINUTES 1.61 K OHMS % CHANGE .000%

8.4.1 -6.1 V VOLTAGE 6.403 VOLTS +5 V VOLTAGE 5.256 VOLTS

-6.1 V CURRENT 7.1 ma +5 V CURRENT 12.0 ma

-6.1 V POWER 45.4613 mw +5 V POWER 63.072 mw

TOTAL MEMORY IDLE POWER 108.5333 mw 170 mw MAX

8.4.2 DID AN ERROR OCCUR?

NO X

YES ___ ADDRESS ___ BIT ___ 0 ERRORS

8.4.3 -6.1 V VOLTAGE 6.400 VOLTS +5 V VOLTAGE 5.253 VOLTS

-6.1 V CURRENT 275 ma +5 V VOLTAGE 790 ma

-6.1 V POWER ~~1760~~ mw 1760 +5 V POWER ~~4053.62~~ mw 4153.82

TOTAL MEMORY OPERATING POWER ~~6003.72~~ 5914 mw 7000 mw MAX

8.4.4 WC a) DID AN ERROR OCCUR?

NO X

YES ___ ADDRESS ___ BIT ___ 0 ERRORS

(M 489)

MOTOROLA INC. Government Electronics Division	SIZE	CODE IDENT NO.	DWG NO.
8201 EAST McDOWELL ROAD SCOTTSDALE, ARIZONA 85257	A	94990	12-P13721D
	SCALE	REVISION	SHEET 19

S/N 104 DATE OF TEST 5/29/75

TESTED BY

LIMITS

8.4.4 (Cont.)

WC b) DID AN ERROR OCCUR?

NO X

YES ____ ADDRESS _____ BIT _____ 0 ERRORS

WC c) DID AN ERROR OCCUR?

NO X

YES ____ ADDRESS _____ BIT _____ 0 ERRORS

WC d) DID AN ERROR OCCUR ?

NO X

YES ____ ADDRESS _____ BIT _____ 0 ERRORS

8.4.6 WC a) DID AN ERROR OCCUR?

NO X

YES ____ ADDRESS _____ BIT _____ 0 ERRORS

WC b) DID AN ERROR OCCUR?

NO X

YES ____ ADDRESS _____ BIT _____ 0 ERRORS

WC c) DID AN ERROR OCCUR?

NO X

YES ____ ADDRESS _____ BIT _____ 0 ERRORS

WC d) DID AN ERROR OCCUR?

NO X

YES ____ ADDRESS _____ BIT _____ 0 ERRORS

8.4.7 DID AN ERROR OCCUR?

NO X

YES ____ ADDRESS _____ BIT _____ 0 ERRORS

S/N 109 Date of Test 6-3-75

Tested by

Limits

9. VACUUM TEST

9.2 Did Any Bit Errors Occur?

JUN - 3 1975

No ✓

Yes _____ Address _____ Bits _____ 0 Errors

9.2.1 Fast Decompression

Date 6-3-75 Tested by

Did Any Bit Errors Occur?

No ✓

Yes _____ Address _____ Bits _____ 0 Errors

9.2.2 Hard Vacuum

Date 6-3-75 Tested by

Did Any Bit Errors Occur?

No ✓

Yes _____ Address _____ Bits _____ 0 Errors

JUN 3 1975

10. VIBRATION TEST

Date 6-5-75 Tested by

JUN - 5 1975

SINE SWEEP

Axis X - Did Any Bit Errors Occur?

No ✓

Yes _____ Freq _____ Address _____ Bits ____ 0 Errors

S/N 104 Date of Test 6-5-75

Tested by [signature]

Axis Y - Did Any Bit Error Occur? Limits JUN. - 51

No ✓

Yes ____ Freq _____ Address _____ Bits _____ 0 Errors

Axis Z - Did Any Bit Errors Occur?

No ✓

Yes ____ Freq _____ Address _____ Bits _____ 0 Errors

RANDOM VIBRATION

Axis X - Did Any Bit Errors Occur?

No ✓

Yes ____ Freq _____ Address _____ Bits _____ 0 Errors

Axis Y - Did Any Bit Errors Occur?

No ✓

Yes ____ Freq _____ Address _____ Bits _____ 0 Errors

Axis Z - Did Any Bit Errors Occur?

No ✓

Yes ____ Freq _____ Address _____ Bits _____ 0 Errors JUN. - 51

11. SHOCK TEST

Date 5-30-75 Tested By [signature]

6 MILLISECOND DURATION SHOCK

Y Direction - Did Any Bit Errors Occur?

No ✓

MAY 30 1975

Yes _____ Address _____ Bits _____ 0 Errors

MOTOROLA INC. Government Electronics Division 8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252	SIZE A	CODE IDENT NO. 94990	DWG NO. 12-P13721D
	SCALE	REVISION	SHEET 22

AV-2-R-1991-100A-3-69 DWG FORMAT

S/N 109 Date of Test 5-30-75

Tested by

Limits

MAY 30 1975

Z Direction - Did Any Bit Errors Occur?

No ✓

Yes _____ Address _____ Bits _____ 0 Errors

X Direction - Did Any Bit Errors Occur?

No ✓

Yes _____ Address _____ Bits _____ 0 Errors

12 MILLISECOND DURATION SHOCK

Y Direction - Did Any Bit Errors Occur?

No ✓

Yes _____ Address _____ Bits _____ 0 Errors

Z Direction - Did Any Bit Errors Occur?

No ✓

Yes _____ Address _____ Bits _____ 0 Errors

X Direction - Did Any Bit Errors Occur?

No ✓

Yes _____ Address _____ Bits _____ 0 Errors

MAY 30 1975

S/N 104 Date of Test 6/6/75.

Tested By [signature]

			Limit
7.4	CHASSIS ISOLATION		
	Impedance	≥ 9	≥ 9 megohms
7.5	INPUT SIGNAL LOADING		
7.5.2	Current from INITIATE PULSE to Gnd	1.38 ma	≤ 2 ma
	Current from 2.4V to INITIATE PULSE	1.31 μa	≤ 20 μa
7.5.3	Current from MEM SEL 1 to Gnd	1.38 ma	≤ 2 ma
	Current from 2.4V to MEM SEL 1	.97 μa	≤ 20 μa
7.5.4	Current from MEM SEL 2 to Gnd	1.39 ma	≤ 2 ma
	Current from 2.4V to MEM SEL 2	1.38 μa	≤ 20 μa
	Current from MEM SEL 3 to Gnd	1.38 ma	≤ 2 ma
	Current from 2.4V to MEL SEL 3	1.34 μa	≤ 20 μa
	Current from MEM SEL 4 to Gnd	1.38 ma	≤ 2 ma
	Current from 2.4V to MEM SEL 4	.96 μa	≤ 20 μa
7.5.5	Current from READ/WRITE to Gnd	1.002 ma	≤ 2 ma
	Current from 2.4V to READ/WRITE	1.26 μa	≤ 20 μa
7.5.6	Current from ADDRESS 2^0 to Gnd	.99 ma	≤ 2 ma
	Current from 2.4V to ADDRESS 2^0	6.34 μa	≤ 20 μa

S/N 104

Date of Test 6/6/75

Tested By [signature]

		Limits
Current from ADDRESS 2^1 to Gnd	.90 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^1	5.93 μa	≤ 20 μa
Current from ADDRESS 2^2 to Gnd	.97 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^2	6.76 μa	≤ 20 μa
Current from ADDRESS 2^3 to Gnd	.90 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^3	7.40 μa	≤ 20 μa
Current from ADDRESS 2^4 to Gnd	.95 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^4	7.83 μa	≤ 20 μa

S/N 104

Date of Test 6/6/75

Tested By [signature]

		Limits
Current from ADDRESS 2^5 to Gnd	.89 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^5	5.42 μa	≤ 20μa
Current from ADDRESS 2^6 to Gnd	.89 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^5	5.52 μa	≤ 20μa
Current from ADDRESS 2^7 to Gnd	.96 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^7	6.53 μa	≤ 20μa
Current from ADDRESS 2^8 to Gnd	.93 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^8	1.10 μa	≤ 20μa
Current from ADDRESS 2^9 to Gnd	.92 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^9	1.09 μa	≤ 20μa
Current from ADDRESS 2^{10} to Gnd	.99 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^{10}	1.27 μa	≤ 20μa
Current from ADDRESS 2^{11} to Gnd	.99 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^{11}	1.30 μa	≤ 20μa
Current from DATA IN BIT 0 to Gnd	1.04 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 0	~~1.06~~ 7.20 μa	≤ 20μa

S/N 104

Date of Test 6/6/75

Tested By [signature]

		Limits
Current from DATA IN BIT 1 to Gnd	1.06 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 1	7.32 μa	≤ 20μa
Current from DATA IN BIT 2 to Gnd	1.06 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 2	6.71 μa	≤ 20μa
Current from DATA IN BIT 3 to Gnd	1.03 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 3	9.22 μa	≤ 20μa
Current from DATA IN BIT 4 to Gnd	1.02 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 4	9.16 μa	≤ 20μa
Current from DATA IN BIT 5 to Gnd	1.04 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 5	8.97 μa	≤ 20μa
Current from DATA IN BIT 6 to Gnd	1.06 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 6	7.65 μa	≤ 20μa
Current from DATA IN BIT 7 to Gnd	1.04 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 7	7.31 μa	≤ 20μa
Current from DATA IN BIT 8 to Gnd	1.03 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 8	7.73 μa	≤ 20μa
Current from DATA IN BIT 9 to Gnd	.97 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 9	8.09 μa	≤ 20μa

S/N 104

Date of Test 6/6/75

Tested By

		Limits
Current from DATA IN BIT 10 to Gnd	.98 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 10	8.89 μa	≤ 20μa
Current from DATA IN BIT 11 to Gnd	.99 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 11	8.09 μa	≤ 20μa
Current from DATA IN BIT 12 to Gnd	1.04 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 12	9.43 μa	≤ 20μa
Current from DATA IN BIT 13 to Gnd	1.04 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 14	9.12 μa	≤ 20μa
Current from DATA IN BIT 14 to Gnd	1.05 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 14	8.93 μa	≤ 20μa
Current from DATA IN BIT 15 to Gnd	1.06 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 15	6.09 μa	≤ 20μa
Current from DATA IN BIT 16 to Gnd	1.03 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 17	6.16 μa	≤ 20μa
Current from DATA IN BIT 17 to Gnd	1.05 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 17	7.24 μa	≤ 20μa

S/N 104

Date of Test 6/6/75

Tested By [signature]

			Limit
7.6	VERIFICATION OF OPEN COLLECTOR ON OUTPUT SIGNALS		
7.6.3	READ COMPLETE voltage	68 mv	≤ 100 mv
7.6.4	DATA OUT BIT 0 voltage	40 mv	≤ 100 mv
	DATA OUT BIT 1 voltage	40 mv	≤ 100 mv
	DATA OUT BIT 2 voltage	30 mv	≤ 100 mv
	DATA OUT BIT 3 voltage	30 mv	≤ 100 mv
	DATA OUT BIT 4 voltage	25 mv	≤ 100 mv
	DATA OUT BIT 5 voltage	20 mv	≤ 100 mv
	DATA OUT BIT 6 voltage	20 mv	≤ 100 mv
	DATA OUT BIT 7 voltage	0 mv	≤ 100 mv
	DATA OUT BIT 8 voltage	0 mv	≤ 100 mv
	DATA OUT BIT 9 voltage	20 mv	≤ 100 mv
	DATA OUT BIT 10 voltage	20 mv	≤ 100 mv
	DATA OUT BIT 11 voltage	25 mv	≤ 100 mv
	DATA OUT BIT 12 voltage	20 mv	≤ 100 mv
	DATA OUT BIT 13 voltage	25 mv	≤ 100 mv
	DATA OUT BIT 14 voltage	25 mv	≤ 100 mv
	DATA OUT BIT 15 voltage	20 mv	≤ 100 mv
	DATA OUT BIT 16 voltage	16 mv	≤ 100 mv
	DATA OUT BIT 17 voltage	15 mv	≤ 100 mv

S/N 104

Date of Test 6/6/75

Tested By

			Limits
7.7	POWER CONSUMPTION (25°C)		HP 412A
7.7.1	Memory +5V Voltage	5.008 Volts	
	Memory -6.1V voltage	-6.016 Volts	
	+5V Current	10.1 ma	
	+5V Power	50.6 mw	
7.7.2	Memory -6.1V Current	3.1 ma	
	Memory -6.1V Power	18.7 mw	
7.7.3	Total Memory Idle Power	69.3 mw	170 mw max
7.7.5	Memory +5V Voltage	5.009 Volts	
	Memory -6.1V Voltage	-6.109 Volts	
	+5V Current	650 ma	
	+5V Power	3255.9 mw	
7.7.6	Memory -6.1V Current	220 ma	
	Memory -6.1V Power	1394.0 mw	
7.7.7	Total Active Power	4599.9 mw	7000 mw max.
7.8	READ COMPLETE TIMING		
7.8.5	Delay	390 ns	500 ns max.
	Duration	320 ns	250 ns min 450 ns max.

M 610

S/N 104

Date of Test 6/6/75

Tested by [signature]

7.8.7 & 7.8.8 READ COMPLETE/DATA OUTPUT TIMING			LIMITS
DO-0	OK ✓	REJECT	
DO-1	OK ✓	REJECT	
DO-2	OK ✓	REJECT	
DO-3	OK ✓	REJECT	
DO-4	OK ✓	REJECT	
DO-5	OK ✓	REJECT	
DO-6	OK ✓	REJECT	
DO-7	OK ✓	REJECT	REFER TO TEST PROC.
DO-8	OK ✓	REJECT	
DO-9	OK ✓	REJECT	
DO-10	OK ✓	REJECT	
DO-11	OK ✓	REJECT	
DO-12	OK ✓	REJECT	
DO-13	OK ✓	REJECT	
DO-14	OK ✓	REJECT	
DO-15	OK ✓	REJECT	
DO-16	OK ✓	REJECT	
DO-17	OK ✓	REJECT	

S/N 104

Date of Test 6/6/75
Tested By

		Limits
7.9	SYSTEM FUNCTIONAL TEST	
7.9.2	Did an error occur?	
	No X	
	Yes ____ Address ____ Bits ____	0 errors
7.9.4	Did an error occur?	
	No X	
	Yes ____ Address ____ Bits ____	0 errors
7.9.10	Did an error occur?	
	No X	
	Yes ____ Address ____ Bits ____	0 errors
7.9.16	Did an error occur?	
	No X	
	Yes ____ Address ____ Bits ____	0 errors
7.10	RANDOM ACCESS CAPABILITY	
7.10.6	Did an error occur?	
	No X	
	Yes ____ Address ____ Bits ____	0 errors
7.10.7	Did an error occur?	
	a) No X	
	Yes ____ Address ____ Bits ____	0 errors

S/N 104

Date of Test 6/6/75
Tested By [signature]

					Limits
	b) No X				
	Yes ____	Address ____	Bits ____		0 errors
	c) No X				
	Yes ____	Address ____	Bits ____		0 errors
7.11	NON-VOLATILITY TEST				
7.11.7 & 7.11.9	Did an error occur?				
	No X				
	Yes ____	Address ____	Bits ____		0 errors
7.12	MEMORY SELECT TEST				
7.12.3	Address 0000 (Octal)				0000
7.12.4	Address 0001	0000	(Octal)		0000
	0010	0000	(Octal)		0000
	0011	0000	(Octal)		0000
	0100	0000	(Octal)		0000
	0101	0000	(Octal)		0000
	0110	0000	(Octal)		0000
	0111	0000	(Octal)		0000
	1000	0000	(Octal)		0000
	1001	0000	(Octal)		0000
	1010	0000	(Octal)		0000

S/N 104

Date of Test 6/6/75

Tested By

		Limits
Address 1011	0000 (Octal)	0000
1100	0000 (Octal)	0000
1101	0000 (Octal)	0000
1110	0000 (Octal)	0000

7.12.6 Did an error occur?

No X

Yes _____ Address _____ Bits _____ 0 errors

7.13 WORST CASE PATTERN TEST

7.13.2 Did an error occur?

No X

Yes _____ Address _____ Bits _____ 0 errors

7.13.3 Did an error occur?

No X

Yes _____ Address _____ Bits _____ 0 errors

S/N 104

Date of Test 6/6/75

Tested By

		Limits
7.13.4	a) Did an error occur?	
	No X	
	Yes ____ Address ____ Bit ____	0 errors
	b) Did an error occur?	
	No X	
	Yes ____ Address ____ Bit ____	0 errors

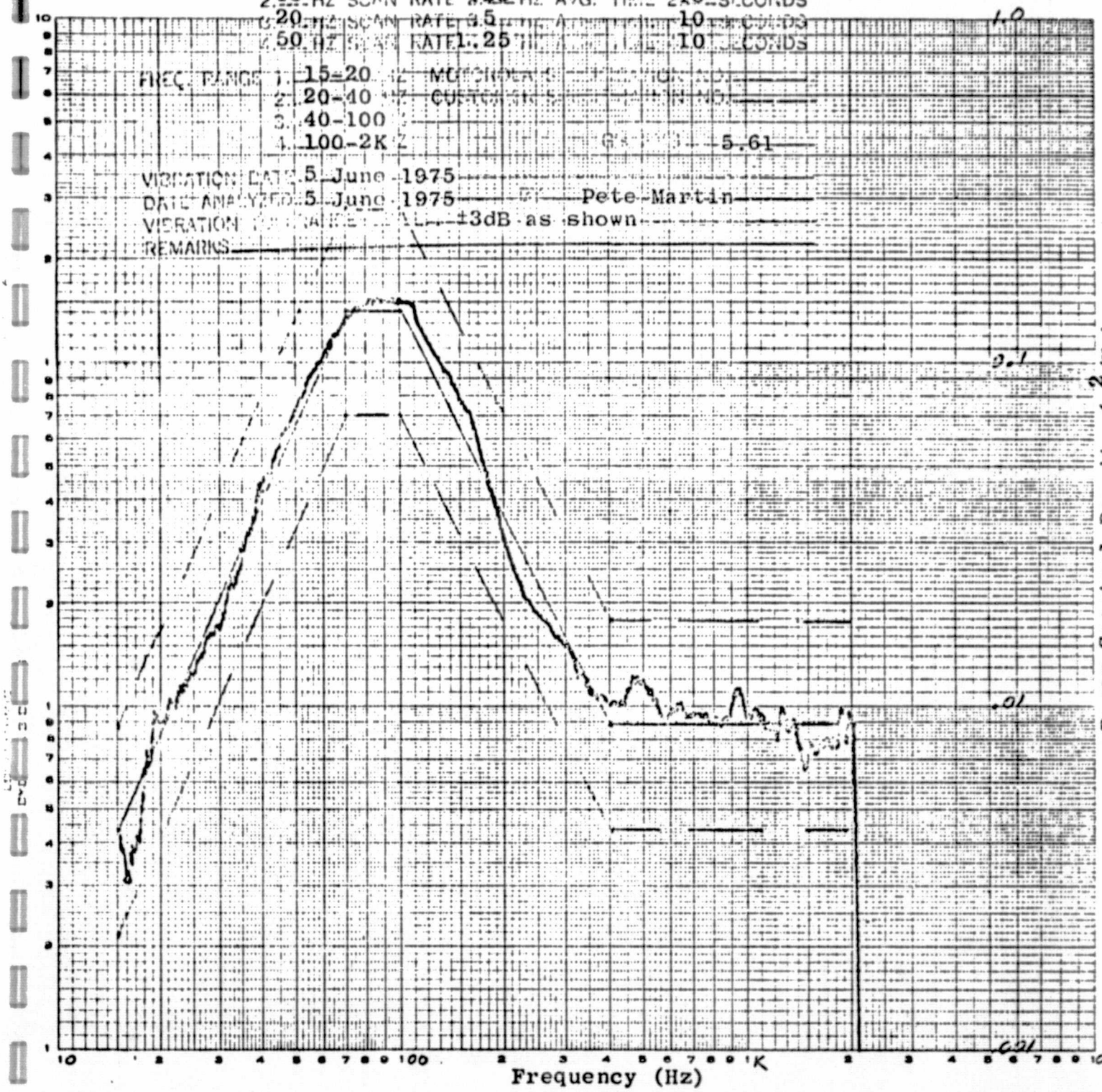
PROJECT 4601-400 UNIT P-W Memory SER. NO. 104

X&Z AXIS SAMPLE (LOOP) TIME 10 SECONDS

FILTER B.W. 1. 5 HZ SCAN RATE .125 HZ AVG. TIME 10 SECONDS
2. 10 HZ SCAN RATE .25 HZ AVG. TIME 10 SECONDS
3. 20 HZ SCAN RATE .5 HZ AVG. TIME 10 SECONDS
4. 50 HZ SCAN RATE 1.25 HZ AVG. TIME 10 SECONDS

FREQ. RANGE 1. 15-20 HZ MODIFICATION NO.
2. 20-40 HZ CUSTOMER'S ITEM NO.
3. 40-100
4. 100-2K G's RMS 5.61

VIBRATION DATE 5 June 1975
DATE ANALYZED 5 June 1975 BY Pete Martin
VIBRATION TOLERANCE LEVEL ±3dB as shown
REMARKS



PRECEDING PAGE BLANK NOT FILMED

ORIGINAL PAGE IS OF POOR QUALITY

PROJECT 4601-400 UNIT P-W Memory SER. NO. 104

X AXIS SAMPLE (LOOP) TIME 10 SECONDS

FILTER B.W. 1. 5 HZ SCAN RATE 125 HZ AVG. TIME 1.10 SECONDS
210 HZ SCAN RATE 225 HZ AVG. TIME 2.10 SECONDS
320 HZ SCAN RATE 325 HZ AVG. TIME 3.10 SECONDS
450 HZ SCAN RATE 1025 HZ AVG. TIME 10 SECONDS

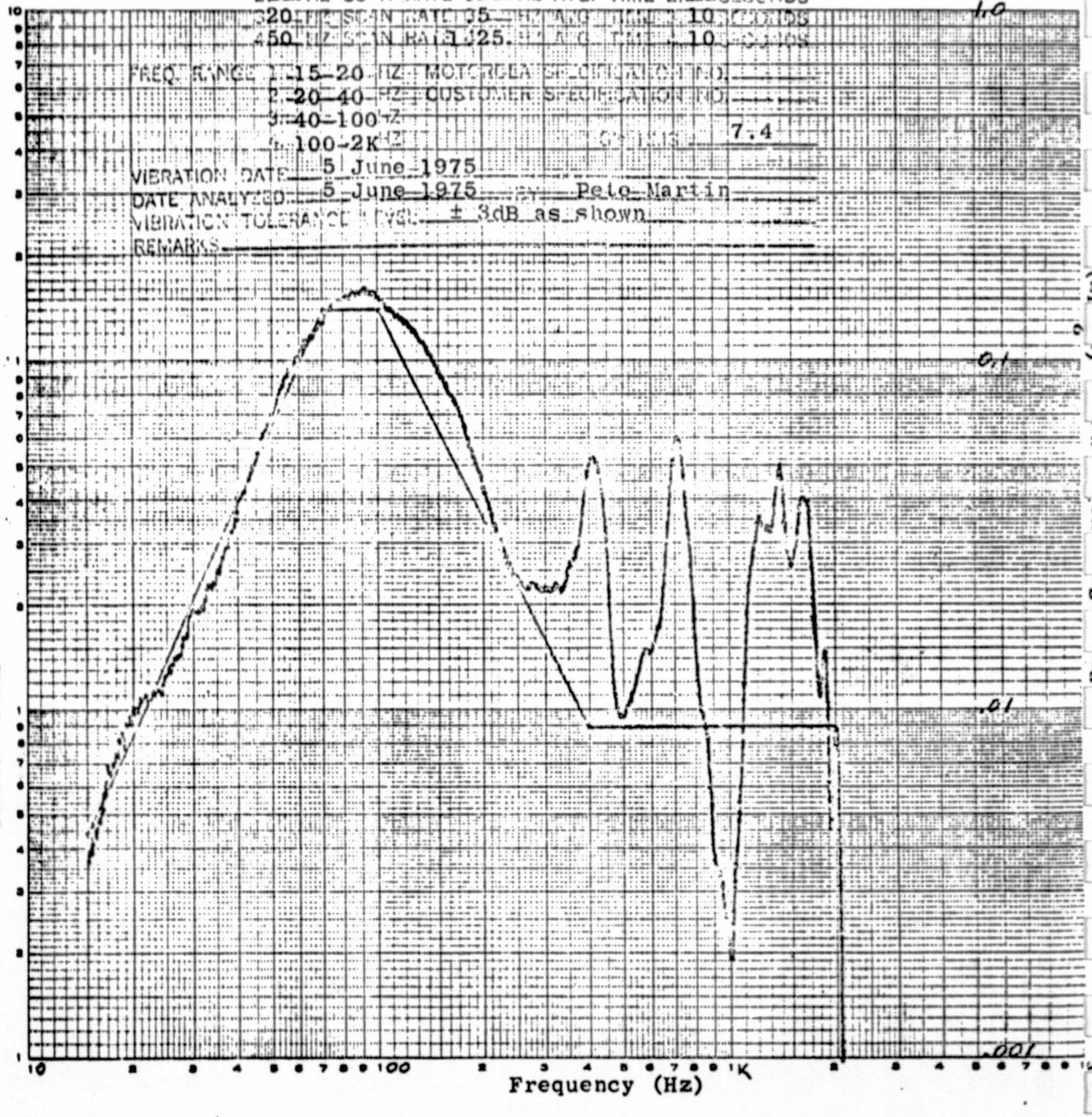
FREQ. RANGE 1. 15-20 HZ MOTOROLA SPECIFICATION NO.
2. 20-40 HZ CUSTOMER SPECIFICATION NO.
3. 40-100 HZ
4. 100-2K HZ G'S RMS 7.4

VIBRATION DATE 5 June 1975

DATE ANALYZED 5 June 1975 BY Peto-Martin

VIBRATION TOLERANCE ENVEL. ± 3dB as shown

REMARKS



LOGARITHMIC
3 CYCLES X 3 CYCLES

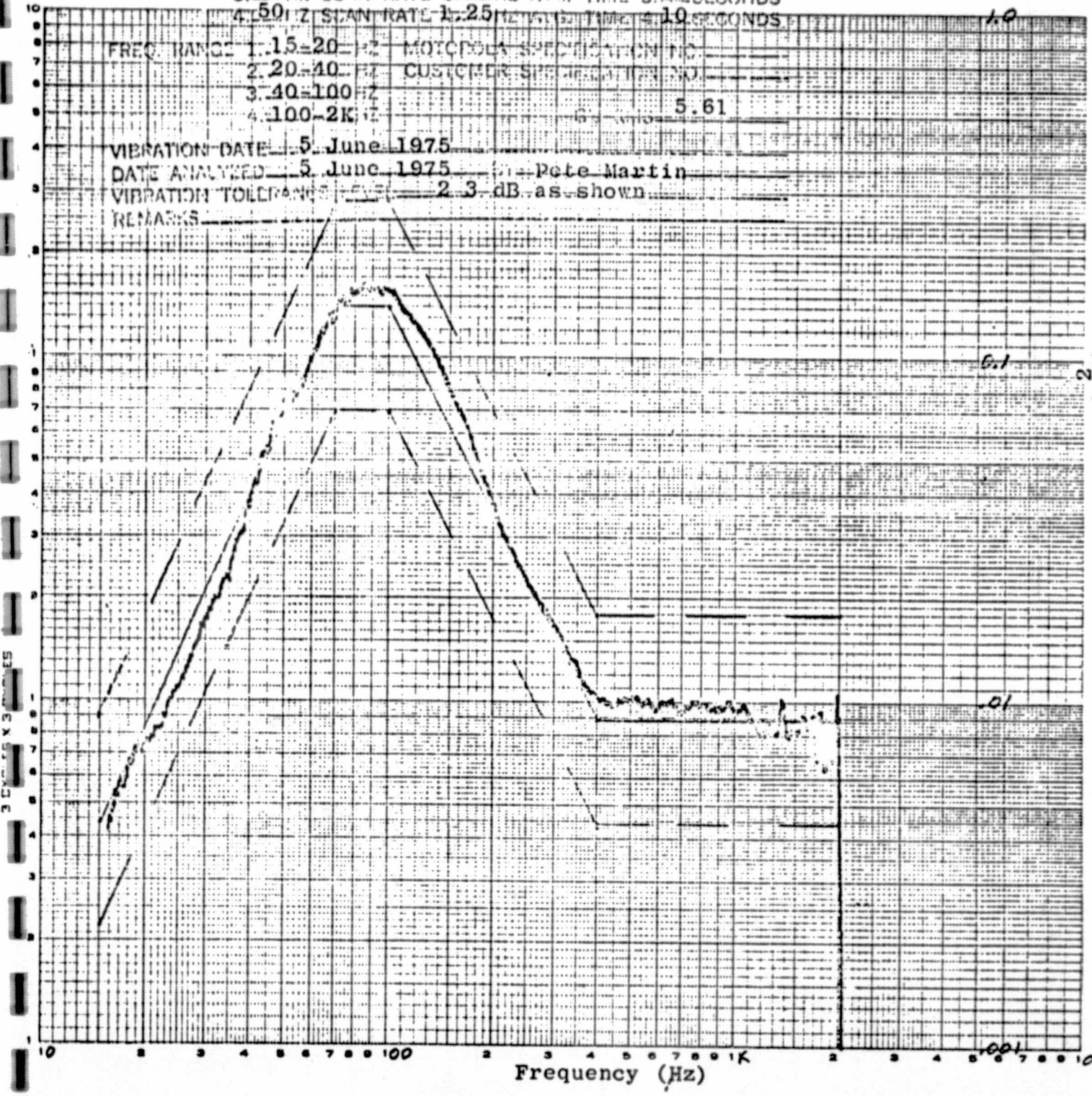
PROJECT 4601-400 UNIT P-W Memory SER. NO. 104

Y AXIS SAMPLE (LOOP) TIME 10 SECONDS

FILTER B.W. 1. 5 HZ SCAN RATE 1. 125 HZ AVG. TIME 1. 10 SECONDS
2. 10 HZ SCAN RATE 2. 25 HZ AVG. TIME 2. 10 SECONDS
3. 20 HZ SCAN RATE 3. 5 HZ AVG. TIME 3. 10 SECONDS
4. 50 HZ SCAN RATE 4. 25 HZ AVG. TIME 4. 10 SECONDS

FREQ. RANGE 1. 15-20 HZ MOTOROLA SPECIFICATION NO.
2. 20-40 HZ CUSTOMER SPECIFICATION NO.
3. 40-100 HZ
4. 100-2K HZ 5.61

VIBRATION DATE 5 June 1975
DATE ANALYZED 5 June 1975 Pete Martin
VIBRATION TOLERANCE 2 3 dB as shown
REMARKS



ORIGINAL PAGE IS
OF POOR QUALITY

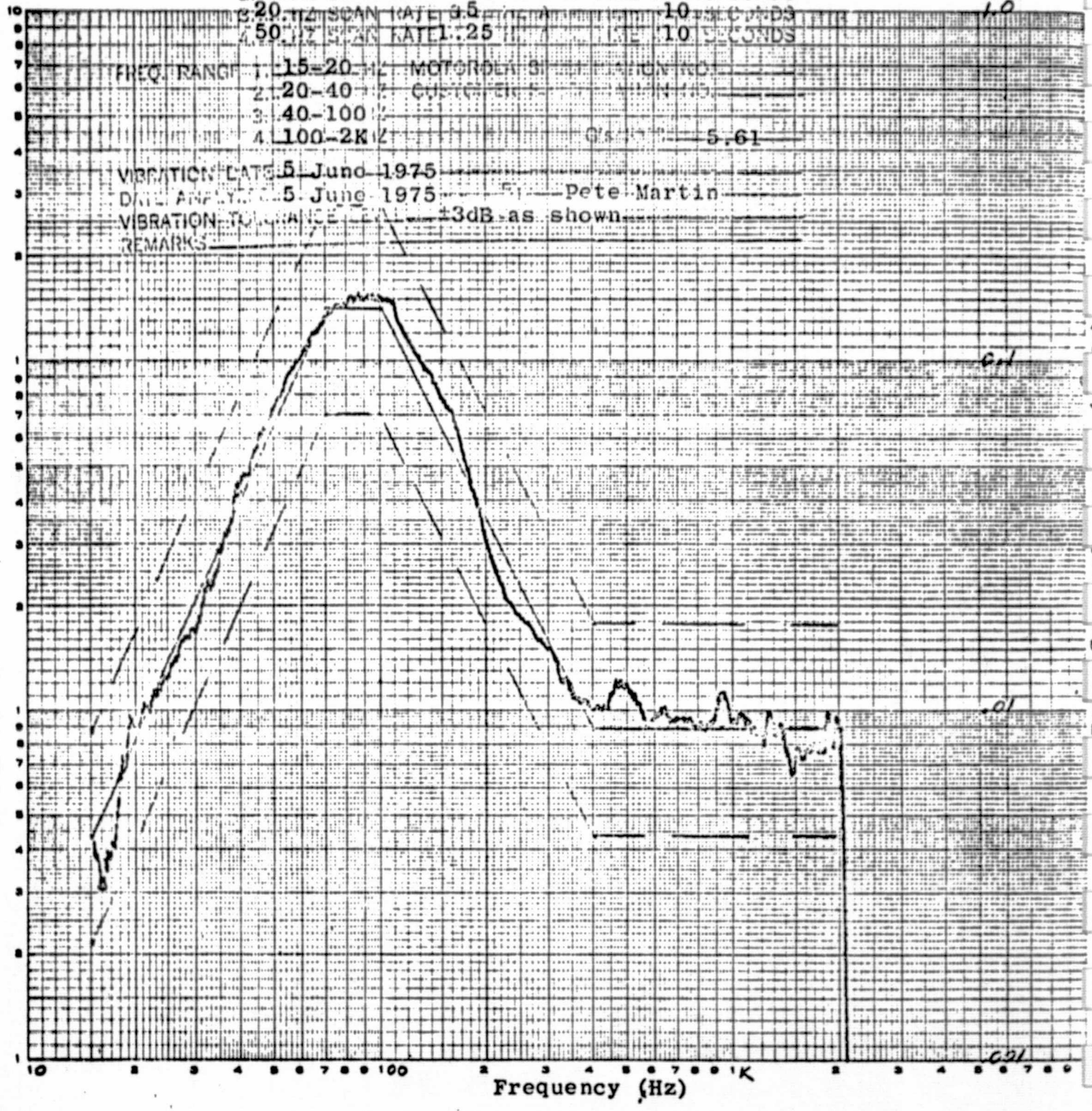
PROJECT 4601-400 UNIT P-W Memory SER. NO. 104

X&Z AXIS SAMPLE (LOOP) TIME 10 SECONDS

FILTER B.W. 1. 5 HZ SCAN RATE 1.125 HZ AVG. TIME 1 10 SECONDS
2. 10 HZ SCAN RATE 2.25 HZ AVG. TIME 2 10 SECONDS
3. 20 HZ SCAN RATE 4.5 HZ AVG. TIME 3 10 SECONDS
4. 50 HZ SCAN RATE 11.25 HZ AVG. TIME 4 10 SECONDS

FREQ. RANGE 1. 15-20 HZ MOTOROLA STATION NO. _____
2. 20-40 HZ CURTISS-WRIGHT STATION NO. _____
3. 40-100 HZ
4. 100-2K HZ G's (RMS) 5.61

VIBRATION DATE 5 June 1975
DATA ANALYZED 5 June 1975 BY Pete Martin
VIBRATION TOLERANCE ±3dB as shown
REMARKS _____



KEUFFEL & ESSER CO. MADE IN U.S.A.

NO. 340-1313 DIETZGEN GRAPH PAPER
LOGARITHMIC
3 CYCLES X 3 CYCLES

PROJECT 4601-400 UNIT P-W Memory SER. NO. 104

Z AXIS SAMPLE (LOOP) TIME 10 SECONDS

FILTER B.W. 1. 5 HZ SCAN RATE 1. 12½ AVG. TIME 1 10 SECONDS
2. 10 HZ SCAN RATE 2. 25 HZ AVG. TIME 2 10 SECONDS
3. 20 HZ SCAN RATE 3. 5 HZ AVG. TIME 3 10 SECONDS
4. 50 HZ SCAN RATE 4. 25 HZ AVG. TIME 4 10 SECONDS

FREQ. RANGE 1. 15-20 Z MOTOROLA SPECIFICATION NO.
2. 20-40 CUSTOMER SPECIFICATION NO.
3. 40-100
4. 100-2K G's 8.6

VIBRATION DATE 5 June 1975
DATE ANALYZED 5 June 1975 Pete Martin
VIBRATION TOLERANCE LEVEL NA
REMARKS Response of top cover

Power Spectral Density (g^2/Hz)

Frequency (Hz)

ORIGINAL PAGE IS
OF POOR QUALITY

MOTOROLA INC.
Government Electronics Division

VIBRATION TEST

SHEET 1 OF _____ DATE 5 June 75

PROJECT 4601-400 UNIT Plated Wire Memory

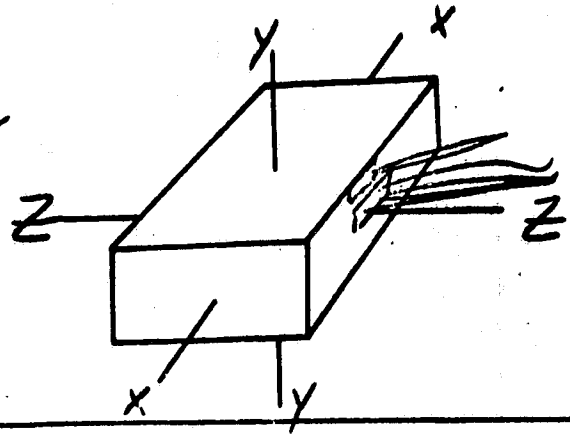
CONTROL NO. 01 & 02 W.O. NO. 3041

OPERATOR Pete Martin

OBSERVER Lee Moulden

CYCLE TIME 4.3 MIN FREQ. 5 TO 2000 Hz

SPEC DETAILS _____



AXIS / RUN NO.	TIME START	TIME STOP	~~ACCUM.~~ RATED VIB. TIME	UNIT SER. NO.	DISPLACEMENT INCHES D.A.	ACCELERATION X RMS X PK / G'S MV (RMS)	REMARKS
Z	13:44	13:46	2 MIN	104	NA	5.6 GRMS / 56	shaped random
Z	13:49	13:54	4.3 MIN	104	.33	10 & 5 / 70 & 35	sine sweep 5-110-2KHZ
X	13:20	13:25	4.3 MIN	104	.33	10 & 5 / 70 & 35	sine sweep 5-110-2KHZ
X	13:27	13:29	2 MIN	104	NA	5.6 GRMS / 56	shaped random
Y	14:45	14:47	2 MIN	104	NA	5.6 GRMS / 56	shaped random
Y	14:48	14:53	4.3 MIN	104	.33	10 & 5 / 70 & 35	sine sweep 5-110-2KHZ

W.O. 3039
CONTROL 4.1

HIGH VACUUM TEST

Unit: PLATED WIRE MEMORY	Project: 2661 - 4.00	Date: 6-3-75	
Model: N/A	Specification: 12-P1372 D		
Serial: 104	Operator: JOE MOLLERE		
Vacuum System No.: 3	Observer: LEE GOULDIN		

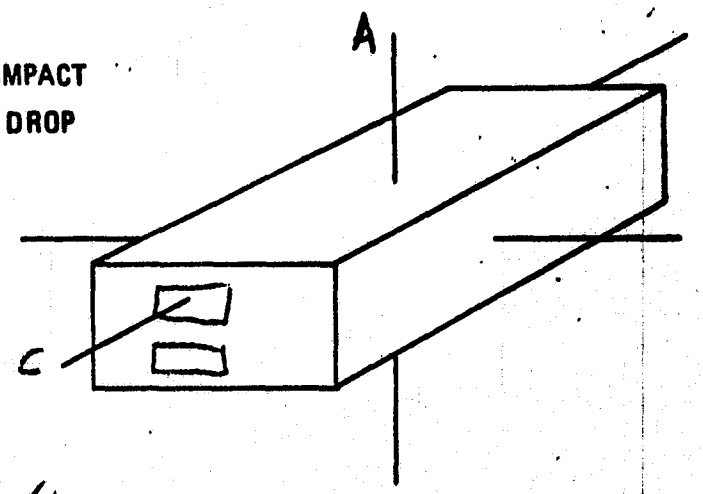
TIME	PRESSURE (mm Hg A)											REMARKS
0950	ATM											START TO HI VAC
0953	7 MM											
0910	6.3×10^{-5}											
0930	3×10^{-5}											
1000	2×10^{-5}											
1030	1.4×10^{-5}											
1100	1.1×10^{-5}											
1115	4.9×10^{-6}											
1130	9.9×10^{-6}											END TEST

MOTOROLA INC.
Government Electronics Division

SHOCK TEST
(DROP)

PROJECT 4601-400
DATE 5-30-75
SHEET 1 OF 1
W.O. NO. 3040
CONTROL NO. 11
UNIT P W. M.
SERIAL NO. 104
OPERATOR Lec M
OBSERVER Lec Gordon
VIBRATION MOUNTS none
NO. OF DROPS PER ~~FACE~~ AXIS 2 TOTAL NO. OF DROPS 6
ACCELERATION 30 G'S
PULSE DURATION 6 & 12 MS
SPEC DETAILS 12-P13722D

TYPE OF TEST
☒ MODULAR IMPACT
☐ FREE FALL DROP



DROP HEIGHT 1 3/4 & 4 3/4 IN.
PROGRAMMER PRESSURE NA P.S.I.
TYPE OF WAVESHAPE half sine
BANDPASS FILTER .2 LOW FR. Hz
3700 HIGH FR. Hz
REMARKS 3 drops at 6 ms & 3 drops at 12 ms

Pads for 12 ms; 1-8x8x¼ plastic
2-8x8x½ nylon
3-8x8x½ nylon
3-1" thick closed
1-1" thick open

PAD AND PLATE CONFIGURATION		
ITEM NO.	PART NO.	DESCRIPTION
1	MRL 2359	alum plate (B)
2	MT 2756	1" pad open (B)
3	MT 2356	alum plate (T)
4		
5		
6		
7		
8		
9		

6 ms 12 ms

AXIS	FACE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	1	/										/									
	2																				
B	1	/										/									
	2	/																			
C	1	/										/									
	2																				

test complete.

ATTACHMENT IV

ACCEPTANCE TEST DATA SHEET

LOW POWER RANDOM ACCESS

SPACECRAFT MEMORY

PART NO. 12-P13721D

SERIAL NUMBER 105

(35 PAGES)

*APPLICATION	
NXT ASSEMBLY	USED ON

*ASTERISK INDICATES DATA WHICH IS NONMANDATORY - FOR INFORMATION ONLY.

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
X1	Initial Release	—	—
X2	Incorporated changes prior to First Usage.	3-16-73	H. Tweed
X3	Change -6.9V to -6.1V	6-18-73	H. Tweed
X4	Change 6000mw to 7000mw, pages 10, 17, 19, 30. Change weight from 6.0 to 6.5 pounds, page 2.	7-24-73	H. Tweed
X5	Add weight 5.8 pounds for magnesium chassis MCO S7835.	2-10-75	
X6	Revised per MCO S7845	4-28-75	

4601

SN 105

REV	X1	X4	X1	X3	X1	X1	X1	X1	X1																				
SHEET	27	28	29	30	31	32	33	34	35																				
REV STATUS OF SHEETS	REV	X 5	X5	X1	X1	X1	X1	X1	X1	X1	X1	X4	X1	X1	X1	X1	X1	X6	X6	X6	X6	X6	X1	X1	X1	X1	X1	X1	
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26		

FOR ASSOCIATED LISTS SEE

INTERPRET DRAWING IN ACCORDANCE WITH STANDARDS PRESCRIBED BY

UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES AND END USE. FOR TOLERANCES SEE NOTE

DR BY H. Tweed

CHK BY

MFG

PROJ NO 4339 4601

CONTR NO NAS5-23163 NAS5-20576

RELEASE NOTICE

APPROVED DATE 1-2-73 H. Tweed

APPROVED DATE

MATERIAL:

MOTOROLA INC. Government Electronics Division / 8201 EAST McDOWELL ROAD SCOTTSDALE, ARIZONA 85252

ACCEPTANCE TEST DATA SHEET, LOW POWER RANDOM ACCESS SPACE-CRAFT MEMORY, PART NO. 01-P13701D

SIZE	CODE IDENT NO.	DWG. NO.
A	94990	12-P13721D

SCALE

SHEET 1 OF 35

1. SCOPE

This test data sheet is to be used to record data as required by the Acceptance Test Procedure for the Low Power Random Access Spacecraft Memory.

2. REFERENCE INFORMATION

2.1 SPECIFICATIONS APPLICABLE

S-562-P-24	Low Power Random Access Spacecraft Memory
12-P13722D	Acceptance Test Procedure, Low Power Random Access Spacecraft Memory

3. TEST DATA

Unit S/N 105 Start Date of Tests 5/15/75

Tested by [signature]

ATP PARA. NO.

3.1 EQUIVALENT TEST EQUIPMENT

DC Williameter H.P 428 A 0-1A
DIGITAL VOLTMETER FLUKE 8120A (MULTIMETER)
COUNTER HP 5245L

4. PHYSICAL CHARACTERISTICS — Limit

6.1 WEIGHT

Weight of LP-RASM - 5.594 Pounds — 6.5 pounds (aluminum) 5.8 pounds (magnesium)

S/N 105

Date of Test 5/15/75

Tested By [signature]

6.2 DIMENSIONS

Limit

H = 2.905 inches

mW ~~W~~ = 6.927 inches

W ~~MW~~ = 6.322 inches

mD ~~D~~ = 8.960 inches

D ~~MD~~ = 8.630 inches

V = H X W X D = 158.5 inches^3 ≤ 160 inches^3

MOTOROLA INC. Government Electronics Division	SIZE	CODE IDENT NO.	DWG NO.
8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252	A	94990	12-P13721D
	SCALE	REVISION	SHEET 3

AV-2-B-100H-100A 2/60 DWG FORMAT

S/N 105 Date of Test 5/15/75

Tested By [signature]

		Limit
7.4	CHASSIS ISOLATION	
	Impedance >9meg	≥ 9 megohms
7.5	INPUT SIGNAL LOADING	
7.5.2	Current from INITIATE PULSE to Gnd 1.109 ma	≤ 2 ma
	Current from 2.4V to INITIATE PULSE .88 μa	≤ 20 μa
7.5.3	Current from MEM SEL 1 to Gnd 1.105 ma	≤ 2 ma
	Current from 2.4V to MEM SEL 1 .61 μa	≤ 20 μa
7.5.4	Current from MEM SEL 2 to Gnd 1.109 ma	≤ 2 ma
	Current from 2.4V to MEM SEL 2 .82 μa	≤ 20 μa
	Current from MEM SEL 3 to Gnd 1.109 ma	≤ 2 ma
	Current from 2.4V to MEL SEL 3 .82 μa	≤ 20 μa
	Current from MEM SEL 4 to Gnd 1.105 ma	≤ 2 ma
	Current from 2.4V to MEM SEL 4 .60 μa	≤ 20 μa
7.5.5	Current from READ/WRITE to Gnd .914 ma	≤ 2 ma
	Current from 2.4V to READ/WRITE 1.54 μa	≤ 20 μa
7.5.6	Current from ADDRESS 2^0 to Gnd .939 ma	≤ 2 ma
	Current from 2.4V to ADDRESS 2^0 5.78 μa	≤ 20 μa

S/N 105

Date of Test 5/15/75

Tested By

		Limits
Current from ADDRESS 2^1 to Gnd	.942 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^1	5.33 μa	≤ 20 μa
Current from ADDRESS 2^2 to Gnd	1.017 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^2	6.35 μa	≤ 20 μa
Current from ADDRESS 2^3 to Gnd	.940 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^3	6.74 μa	≤ 20 μa
Current from ADDRESS 2^4 to Gnd	.994 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^4	7.51 μa	≤ 20 μa

S/N 105

Date of Test 5/15/75

Tested By

		Limits
Current from ADDRESS 2^5 to Gnd	.943 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^5	6.02 μa	≤ 20μa
Current from ADDRESS 2^6 to Gnd	.921 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^5	5.71 μa	≤ 20μa
Current from ADDRESS 2^7 to Gnd	1.005 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^7	6.68 μa	≤ 20μa
Current from ADDRESS 2^8 to Gnd	1.039 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^8	1.56 μa	≤ 20μa
Current from ADDRESS 2^9 to Gnd	1.016 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^9	1.67 μa	≤ 20μa
Current from ADDRESS 2^{10} to Gnd	.910 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^{10}	1.59 μa	≤ 20μa
Current from ADDRESS 2^{11} to Gnd	.905 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^{11}	1.60 μa	≤ 20μa
Current from DATA IN BIT 0 to Gnd	1.045 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 0	2.46 μa	≤ 20μa

S/N 105

Date of Test 5/15/75

Tested By [illegible]

		Limits
Current from DATA IN BIT 1 to Gnd	1.037 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 1	6.85 μa	≤ 20 μa
Current from DATA IN BIT 2 to Gnd	1.052 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 2	7.09 μa	≤ 20 μa
Current from DATA IN BIT 3 to Gnd	1.029 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 3	8.20 μa	≤ 20 μa
Current from DATA IN BIT 4 to Gnd	1.011 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 4	7.20 μa	≤ 20 μa
Current from DATA IN BIT 5 to Gnd	1.048 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 5	7.45 μa	≤ 20 μa
Current from DATA IN BIT 6 to Gnd	1.016 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 6	5.48 μa	≤ 20 μa
Current from DATA IN BIT 7 to Gnd	0.992 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 7	5.51 μa	≤ 20 μa
Current from DATA IN BIT 8 to Gnd	0.996 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 8	5.83 μa	≤ 20 μa
Current from DATA IN BIT 9 to Gnd	0.970 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 9	6.02 μa	≤ 20 μa

S/N 105

Date of Test 5/15/75

Tested By

		Limits
Current from DATA IN BIT 10 to Gnd	0.971 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 10	6.01 μa	≤ 20μa
Current from DATA IN BIT 11 to Gnd	0.980 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 11	6.04 μa	≤ 20μa
Current from DATA IN BIT 12 to Gnd	0.990 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 12	5.60 μa	≤ 20μa
Current from DATA IN BIT 13 to Gnd	0.991 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 14	5.64 μa	≤ 20μa
Current from DATA IN BIT 14 to Gnd	0.995 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 14	5.36 μa	≤ 20μa
Current from DATA IN BIT 15 to Gnd	0.884 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 15	4.17 μa	≤ 20μa
Current from DATA IN BIT 16 to Gnd	0.874 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 17	4.66 μa	≤ 20μa
Current from DATA IN BIT 17 to Gnd	0.879 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 17	4.77 μa	≤ 20μa

S/N 105

Date of Test 5/15/75

Tested By

			Limit
7.6	VERIFICATION OF OPEN COLLECTOR ON OUTPUT SIGNALS		
7.6.3	READ COMPLETE voltage	20.0 mv	≤ 100 mv
7.6.4	DATA OUT BIT 0 voltage	10.0 mv	≤ 100 mv
	DATA OUT BIT 1 voltage	10.0 mv	≤ 100 mv
	DATA OUT BIT 2 voltage	5.0 mv	≤ 100 mv
	DATA OUT BIT 3 voltage	10.0 mv	≤ 100 mv
	DATA OUT BIT 4 voltage	5.0 mv	≤ 100 mv
	DATA OUT BIT 5 voltage	0.0 mv	≤ 100 mv
	DATA OUT BIT 6 voltage	0.0 mv	≤ 100 mv
	DATA OUT BIT 7 voltage	0.0 mv	≤ 100 mv
	DATA OUT BIT 8 voltage	10.0 mv	≤ 100 mv
	DATA OUT BIT 9 voltage	20.0 mv	≤ 100 mv
	DATA OUT BIT 10 voltage	15.0 mv	≤ 100 mv
	DATA OUT BIT 11 voltage	20.0 mv	≤ 100 mv
	DATA OUT BIT 12 voltage	20.0 mv	≤ 100 mv
	DATA OUT BIT 13 voltage	20.0 mv	≤ 100 mv
	DATA OUT BIT 14 voltage	20.5 mv	≤ 100 mv
	DATA OUT BIT 15 voltage	15.0 mv	≤ 100 mv
	DATA OUT BIT 16 voltage	25.0 mv	≤ 100 mv
	DATA OUT BIT 17 voltage	25.0 mv	≤ 100 mv

S/N 105

Date of Test 5/15/75

Tested By [signature]

				Limits
7.7	POWER CONSUMPTION (25°C)			
7.7.1	Memory +5V Voltage	+5.001	Volts	
	Memory -6.1V voltage	-6.103	Volts	
	+5V Current	10.5	ma	
	+5V Power	52.5	mw	
7.7.2	Memory -6.1V Current	3.3	ma	
	Memory -6.1V Power	20.2	mw	
7.7.3	Total Memory Idle Power	72.7	mw	170 mw max
7.7.5	Memory +5V Voltage	+5.006	Volts	
	Memory -6.1V Voltage	-6.105	Volts	
	+5V Current	680	ma	
	+5V Power	3404	mw	
7.7.6	Memory -6.1V Current	220	ma	
	Memory -6.1V Power	1343	mw	
7.7.7	Total Active Power	4747	mw	7000 mw max.
7.8	READ COMPLETE TIMING			
7.8.5	Delay	380	ns	500 ns max.
	Duration	330	ns	250 ns min 450 ns max.

S/N 105

Date of Test 5/15/75.

Tested by [signature]

7.8.7 & 7.8.8 READ COMPLETE/DATA OUTPUT TIMING

			LIMITS
DO-0	OK ✓	REJECT	
DO-1	OK ✓	REJECT	
DO-2	OK ✓	REJECT	
DO-3	OK ✓	REJECT	
DO-4	OK ✓	REJECT	
DO-5	OK ✓	REJECT	
DO-6	OK ✓	REJECT	
DO-7	OK ✓	REJECT	REFER TO TEST PROC.
DO-8	OK ✓	REJECT	
DO-9	OK ✓	REJECT	
DO-10	OK ✓	REJECT	
DO-11	OK ✓	REJECT	
DO-12	OK ✓	REJECT	
DO-13	OK ✓	REJECT	
DO-14	OK ✓	REJECT	
DO-15	OK ✓	REJECT	
DO-16	OK ✓	REJECT	
DO-17	OK ✓	REJECT	

S/N 105

Date of Test 5/15/75
Tested By [signature]

		Limits
7.9	SYSTEM FUNCTIONAL TEST	
7.9.2	Did an error occur?	
	No ✓	
	Yes ____ Address ____ Bits ____	0 errors
7.9.4	Did an error occur?	
	No ✓	
	Yes ____ Address ____ Bits ____	0 errors
7.9.10	Did an error occur?	
	No ✓	
	Yes ____ Address ____ Bits ____	0 errors
7.9.16	Did an error occur?	
	No ✓	
	Yes ____ Address ____ Bits ____	0 errors
7.10	RANDOM ACCESS CAPABILITY	
7.10.6	Did an error occur?	
	No ✓	
	Yes ____ Address ____ Bits ____	0 errors
7.10.7	Did an error occur?	
	a) No ✓	
	Yes ____ Address ____ Bits ____	0 errors

S/N 105

Date of Test 5/15/75
Tested By [signature]

			Limits
b)	No ✓		
	Yes ____ Address ____ Bits ____		0 errors
c)	No ✓		
	Yes ____ Address ____ Bits ____		0 errors
7.11	NON-VOLATILITY TEST		
7.11.7 & 7.11.9	Did an error occur? No ✓		
	Yes ____ Address ____ Bits ____		0 errors
7.12	MEMORY SELECT TEST		
7.12.3	Address 0000 (Octal)		0000
7.12.4	Address 0001 0001 (Octal)		0000
	0010 (Octal)		0000
	0011 (Octal)		0000
	0100 (Octal)		0000
	0101 (Octal)		0000
	0110 (Octal)		0000
	0111 (Octal)		0000
	1000 (Octal)		0000
	1001 (Octal)		0000
	1010 (Octal)		0000

S/N 105

Date of Test 5/15/75

Tested By [signature]

		Limits
Address 1011 0000 (Octal)		0000
1100 0000 (Octal)		0000
1101 0000 (Octal)		0000
1110 0000 (Octal)		0000

7.12.6 Did an error occur?

No ✓

Yes _____ Address _____ Bits _____ 0 errors

7.13 WORST CASE PATTERN TEST

7.13.2 Did an error occur?

No ✓

Yes _____ Address _____ Bits _____ 0 errors

7.13.3 Did an error occur?

No ✓

Yes _____ Address _____ Bits _____ 0 errors

S/N 105

Date of Test 5/15/75

Tested By

		Limits
7.13.4 a)	Did an error occur?	
	No ✓	
	Yes ____ Address ____ Bit ____	0 errors
b)	Did an error occur?	
	No ✓	
	Yes ____ Address ____ Bit ____	0 errors

S/N 105

DATE OF TEST 5/20/75
TESTED BY [signature]

8. TEMPERATURE TEST — LIMITS

8.2.1 TIME 6:30

8.2.2 LOW TEMPERATURE

THERMISTOR RESISTANCE

150 MINUTES 221.2 K OHMS

160 MINUTES 221.5 K OHMS % CHANGE _____

170 MINUTES _____ K OHMS % CHANGE _____

180 MINUTES _____ K OHMS % CHANGE _____

190 MINUTES _____ K OHMS % CHANGE _____

8.2.3 DID AN ERROR OCCUR?

NO X

YES _____ ADDRESS _____ BITS _____ 0 ERRORS

8.2.4 -6.1 V VOLTAGE -6.405 VOLTS +5 V VOLTAGE 5.255 VOLTS

-6.1 V CURRENT -12.8 ma +5 V CURRENT 10.3 ma

-6.1 V POWER 81.99 mw +5 V POWER 54.13 mw

TOTAL MEMORY IDLE POWER 136.12 mw 170 mw MAX

8.2.5 -6.1 V VOLTAGE -6.401 VOLTS +5 V VOLTAGE 5.250 VOLTS

-6.1 V CURRENT ~~77~~ ma 240 +5 V CURRENT ~~660~~ ma 670

-6.1 V POWER 1537 mw +5 V POWER 3518 mw

TOTAL MEMORY OPERATING POWER 5055 mw 7000 mw MAX

S/N 105

DATE OF TEST 5/20/75

TESTED BY [signature]

				LIMITS
8.2.6	DID AN ERROR OCCUR?			
	NO X			
	YES ___	ADDRESS ___	BIT ___	0 ERRORS
8.2.8	WC a) DID AN ERROR OCCUR?			
	NO X			
	YES ___	ADDRESS ___	BIT ___	0 ERRORS
	WC b) DID AN ERROR OCCUR?			
	NO X			
	YES ___	ADDRESS ___	BIT ___	0 ERRORS
	WC c) DID AN ERROR OCCUR?			
	NO X			
	YES ___	ADDRESS ___	BIT ___	0 ERRORS
	WC d) DID AN ERROR OCCUR?			
	NO X			
	YES ___	ADDRESS ___	BIT ___	0 ERRORS
8.2.11	WC a) DID AN ERROR OCCUR?			
	NO X			
	YES ___	ADDRESS ___	BIT ___	0 ERRORS

S/N 105 DATE OF TEST 5/20/75

TESTED BY [signature]

LIMITS

8.2.11 (Cont.)

WC b) DID AN ERROR OCCUR?

NO X

YES ___ ADDRESS _____ BIT _____ 0 ERRORS

WC c) DID AN ERROR OCCUR?

NO X

YES ___ ADDRESS _____ BIT _____ 0 ERRORS

WC d) DID AN ERROR OCCUR?

NO

YES X ADDRESS 3001 BIT 13 0 ERRORS

8.3 INTERMEDIATE TEMPERATURE TEST

TIME 10:45

8.3.2 TIME	THERMISTOR READING.		DID ANY ERROR OCCUR?		
10:55	128	K OHMS	NO X	YES ___	0 ERRORS
___	___	K OHMS	NO ___	YES ___	0 ERRORS
___	___	K OHMS	NO ___	YES ___	0 ERRORS
___	___	K OHMS	NO ___	YES ___	0 ERRORS
___	___	K OHMS	NO ___	YES ___	0 ERRORS
___	___	K OHMS	NO ___	YES ___	0 ERRORS
___	___	K OHMS	NO ___	YES ___	0 ERRORS
___	___	K OHMS	NO ___	YES ___	0 ERRORS
___	___	K OHMS	NO ___	YES ___	0 ERRORS
___	___	K OHMS	NO ___	YES ___	0 ERRORS
___	___	K OHMS	NO ___	YES ___	0 ERRORS
___	___	K OHMS	NO ___	YES ___	0 ERRORS

S/N 105

DATE OF TEST 5/24/75

TESTED BY [signature]

LIMITS

8.3.3 TIME 11:30

8.4 50 MINUTES ——— K OHMS

60 MINUTES 1.506 K OHMS % CHANGE

70 MINUTES 1.472 K OHMS % CHANGE

80 MINUTES 1.443 K OHMS % CHANGE

90 MINUTES _____ K OHMS % CHANGE

8.4.1 -6.1 V VOLTAGE -6.402 VOLTS +5 V VOLTAGE 5.250 VOLTS

-6.1 V CURRENT 6.4 ma +5 V CURRENT 11.8 ma

-6.1 V POWER 40.9728 mw +5 V POWER 61.95 mw

TOTAL MEMORY IDLE POWER 102.9228 mw 170 mw MAX

8.4.2 DID AN ERROR OCCUR?

NO X

YES ___ ADDRESS _____ BIT _____ 0 ERRORS

8.4.3 -6.1 V VOLTAGE 6.406 VOLTS +5 V VOLTAGE 5.25 VOLTS

-6.1 V CURRENT 255 ma +5 V VOLTAGE 760 ma

-6.1 V POWER 1633.53 mw +5 V POWER 3990.6 mw

TOTAL MEMORY OPERATING POWER 5323.53 mw 7000 mw MAX

8.4.4 WC a) DID AN ERROR OCCUR?

NO X

YES ___ ADDRESS _____ BIT _____ 0 ERRORS

MOTOROLA INC. Government Electronics Division	SIZE	CODE IDENT NO.	DWG NO.
8201 EAST McDOWELL ROAD SCOTTSDALE, ARIZONA 85257	A	94990	12-P13721D
	SCALE	REVISION	SHEET 19

S/N 105

DATE OF TEST 5/27/75

TESTED BY

LIMITS

8.4.4 (Cont.)

WC b) DID AN ERROR OCCUR?

NO X

YES ____ ADDRESS _____ BIT _____ 0 ERRORS

WC c) DID AN ERROR OCCUR?

NO X

YES ____ ADDRESS _____ BIT _____ 0 ERRORS

WC d) DID AN ERROR OCCUR ?

NO X

YES ____ ADDRESS _____ BIT _____ 0 ERRORS

8.4.6 WC a) DID AN ERROR OCCUR?

NO X

YES ____ ADDRESS _____ BIT _____ 0 ERRORS

WC b) DID AN ERROR OCCUR?

NO X

YES ____ ADDRESS _____ BIT _____ 0 ERRORS

WC c) DID AN ERROR OCCUR?

NO X

YES ____ ADDRESS _____ BIT _____ 0 ERRORS

WC d) DID AN ERROR OCCUR?

NO X

YES ____ ADDRESS _____ BIT _____ 0 ERRORS

8.4.7 DID AN ERROR OCCUR?

NO X

YES ____ ADDRESS _____ BIT _____ 0 ERRORS

S/N 105 Date of Test 5/19/75

Tested by [signature]

Limits

9. VACUUM TEST

9.2 Did Any Bit Errors Occur?

No ✓

Yes _____ Address _____ Bits _____ 0 Errors

9.2.1 Fast Decompression

Date 5/19/75 Tested by [signature]

Did Any Bit Errors Occur?

No ✓

Yes _____ Address _____ Bits _____ 0 Errors

9.2.2 Hard Vacuum

Date 5/19/75 Tested by [signature] MAY 19 1974

Did Any Bit Errors Occur?

No ✓

Yes _____ Address _____ Bits _____ 0 Errors

10. VIBRATION TEST

Date 5-21-75 Tested by [signature] MAY 19 1974 MAY 21 1974

SINE SWEEP

Axis X - Did Any Bit Errors Occur?

No ✓

Yes _____ Freq _____ Address _____ Bits _____ 0 Errors

S/N 105 Date of Test 5-21-75

Tested by [signature]

Axis Y - Did Any Bit Error Occur? **Limits**

No ✓

Yes ____ Freq _____ Address _____ Bits _____ 0 Errors

Axis Z - Did Any Bit Errors Occur?

No ✓

Yes ____ Freq _____ Address _____ Bits _____ 0 Errors

RANDOM VIBRATION

Axis X - Did Any Bit Errors Occur?

No ✓

Yes ____ Freq _____ Address _____ Bits _____ 0 Errors

Axis Y - Did Any Bit Errors Occur?

No ✓

Yes ____ Freq _____ Address _____ Bits _____ 0 Errors

Axis Z - Did Any Bit Errors Occur?

No ✓

Yes ____ Freq _____ Address _____ Bits _____ 0 Errors

MAY 21 1974

11. SHOCK TEST

Date 5/16/75 Tested By [signature]

MAY 16 1975

6 MILLISECOND DURATION SHOCK

Y Direction - Did Any Bit Errors Occur?

No ✓

Yes _____ Address _____ Bits _____ 0 Errors

S/N 105 Date of Test 5/16/75

Tested by

Limits MAY 16 1975

Z Direction - Did Any Bit Errors Occur?

No ✓

Yes ____ Address ____ Bits ____ 0 Errors

X Direction - Did Any Bit Errors Occur?

No ✓

Yes ____ Address ____ Bits ____ 0 Errors

12 MILLISECOND DURATION SHOCK

Y Direction - Did Any Bit Errors Occur?

No ✓

Yes ____ Address ____ Bits ____ 0 Errors

Z Direction - Did Any Bit Errors Occur?

No ✓

Yes ____ Address ____ Bits ____ 0 Errors

X Direction - Did Any Bit Errors Occur?

No ✓

Yes ____ Address ____ Bits ____ 0 Errors

MAY 16 1975

S/N 105 Date of Test 5/27/75

Tested By [signature]

			Limit
7.4	CHASSIS ISOLATION		
	Impedance	≥ 9 meg Ω	≥ 9 megohms
7.5	INPUT SIGNAL LOADING		
7.5.2	Current from INITIATE PULSE to Gnd	1.104 ma	≤ 2 ma
	Current from 2.4V to INITIATE PULSE	.90 μa	≤ 20 μa
7.5.3	Current from MEM SEL 1 to Gnd	1.102 ma	≤ 2 ma
	Current from 2.4V to MEM SEL 1	.61 μa	≤ 20 μa
7.5.4	Current from MEM SEL 2 to Gnd	1.105 ma	≤ 2 ma
	Current from 2.4V to MEM SEL 2	.83 μa	≤ 20 μa
	Current from MEM SEL 3 to Gnd	1.105 ma	≤ 2 ma
	Current from 2.4V to MEL SEL 3	.83 μa	≤ 20 μa
	Current from MEM SEL 4 to Gnd	1.102 ma	≤ 2 ma
	Current from 2.4V to MEM SEL 4	.61 μa	≤ 20 μa
7.5.5	Current from READ/WRITE to Gnd	.905 ma	≤ 2 ma
	Current from 2.4V to READ/WRITE	1.59 μa	≤ 20 μa
7.5.6	Current from ADDRESS 2^0 to Gnd	.931 ma	≤ 2 ma
	Current from 2.4V to ADDRESS 2^0	5.85 μa	≤ 20 μa

S/N 105

Date of Test 5/27/75

Tested By

		Limits
Current from ADDRESS 2^1 to Gnd	.932 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^1	5.42 μa	≤ 20 μa
Current from ADDRESS 2^2 to Gnd	1.009 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^2	6.44 μa	≤ 20 μa
Current from ADDRESS 2^3 to Gnd	.932 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^3	6.82 μa	≤ 20 μa
Current from ADDRESS 2^4 to Gnd	.986 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^4	7.61 μa	≤ 20 μa

S/N 105

Date of Test 5/27/75

Tested By

		Limits
Current from ADDRESS 2^5 to Gnd	.935 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^5	6.12 μa	≤ 20μa
Current from ADDRESS 2^6 to Gnd	.914 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^5	5.81 μa	≤ 20μa
Current from ADDRESS 2^7 to Gnd	.997 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^7	6.79 μa	≤ 20μa
Current from ADDRESS 2^8 to Gnd	1.030 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^8	1.63 μa	≤ 20μa
Current from ADDRESS 2^9 to Gnd	1.007 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^9	1.74 μa	≤ 20μa
Current from ADDRESS 2^{10} to Gnd	.902 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^{10}	1.64 μa	≤ 20μa
Current from ADDRESS 2^{11} to Gnd	.898 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^{11}	1.66 μa	≤ 20μa
Current from DATA IN BIT 0 to Gnd	1.037 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 0	7.56 μa	≤ 20 μa

S/N 105

Date of Test 5/27/75

Tested By [signature]

		Limits
Current from DATA IN BIT 1 to Gnd	1.030 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 1	6.97 μa	≤ 20 μa
Current from DATA IN BIT 2 to Gnd	1.044 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 2	7.21 μa	≤ 20 μa
Current from DATA IN BIT 3 to Gnd	1.020 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 3	8.30 μa	≤ 20 μa
Current from DATA IN BIT 4 to Gnd	1.003 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 4	7.30 μa	≤ 20 μa
Current from DATA IN BIT 5 to Gnd	1.040 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 5	7.57 μa	≤ 20 μa
Current from DATA IN BIT 6 to Gnd	1.007 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 6	5.57 μa	≤ 20 μa
Current from DATA IN BIT 7 to Gnd	.985 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 7	5.60 μa	≤ 20 μa
Current from DATA IN BIT 8 to Gnd	.988 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 8	5.92 μa	≤ 20 μa
Current from DATA IN BIT 9 to Gnd	.963 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 9	6.05 μa	≤ 20 μa

C-3

S/N 105

Date of Test 5/27/75

Tested By

		Limits
Current from DATA IN BIT 10 to Gnd	.962 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 10	6.03 μa	≤ 20μa
Current from DATA IN BIT 11 to Gnd	.972 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 11	6.07 μa	≤ 20μa
Current from DATA IN BIT 12 to Gnd	.983 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 12	5.65 μa	≤ 20μa
Current from DATA IN BIT 13 to Gnd	.984 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 14	5.69 μa	≤ 20μa
Current from DATA IN BIT 14 to Gnd	.989 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 14	5.41 μa	≤ 20μa
Current from DATA IN BIT 15 to Gnd	.877 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 15	4.22 μa	≤ 20μa
Current from DATA IN BIT 16 to Gnd	.868 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 17	4.70 μa	≤ 20μa
Current from DATA IN BIT 17 to Gnd	.873 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 17	4.80 μa	≤ 20μa

S/N 105

Date of Test 5/27/76

Tested By

			Limit
7.6	VERIFICATION OF OPEN COLLECTOR ON OUTPUT SIGNALS		
7.6.3	READ COMPLETE voltage 50	mv	≤ 100 mv
7.6.4	DATA OUT BIT 0 voltage 20	mv	≤ 100 mv
	DATA OUT BIT 1 voltage 0	mv	≤ 100 mv
	DATA OUT BIT 2 voltage 0	mv	≤ 100 mv
	DATA OUT BIT 3 voltage 0	mv	≤ 100 mv
	DATA OUT BIT 4 voltage 10	mv	≤ 100 mv
	DATA OUT BIT 5 voltage 10	mv	≤ 100 mv
	DATA OUT BIT 6 voltage 5	mv	≤ 100 mv
	DATA OUT BIT 7 voltage 0	mv	≤ 100 mv
	DATA OUT BIT 8 voltage 0	mv	≤ 100 mv
	DATA OUT BIT 9 voltage 15	mv	≤ 100 mv
	DATA OUT BIT 10 voltage 10	mv	≤ 100 mv
	DATA OUT BIT 11 voltage 15	mv	≤ 100 mv
	DATA OUT BIT 12 voltage 15	mv	≤ 100 mv
	DATA OUT BIT 13 voltage 15	mv	≤ 100 mv
	DATA OUT BIT 14 voltage 15	mv	≤ 100 mv
	DATA OUT BIT 15 voltage 10	mv	≤ 100 mv
	DATA OUT BIT 16 voltage 5	mv	≤ 100 mv
	DATA OUT BIT 17 voltage 10	mv	≤ 100 mv

S/N 105

Date of Test 5-27-75

Tested By [signature]

				Limits
7.7	POWER CONSUMPTION (25°C)			
7.7.1	Memory +5V Voltage	5.000	Volts	
	Memory -6.1V voltage	~~10.1~~ 6.102	Volts	6.102V cls
	+5V Current	10.1	ma	
	+5V Power	50.5	mw	
7.7.2	Memory -6.1V Current	~~6.102~~ 3.2	ma	3,2 cls
	Memory -6.1V Power	19.5264	mw	
7.7.3	Total Memory Idle Power	70.02	mw	170 mw max
7.7.5	Memory +5V Voltage	5.001	Volts	
	Memory -6.1V Voltage	6.107	Volts	
	+5V Current	670	ma	
	+5V Power	5350.67	mw	
7.7.6	Memory -6.1V Current	215	ma	
	Memory -6.1V Power	1313.005	mw	
7.7.7	Total Active Power	6663.675	mw	7000 mw max.
7.8	READ COMPLETE TIMING			
7.8.5	Delay	405	ns	500 ns max.
	Duration	330	ns	250 ns min 450 ns max.

S/N 105

Date of Test 5/27/75

Tested by

7.8.7 & 7.8.8 READ COMPLETE/DATA OUTPUT TIMING			LIMITS
DO-0	OK ✓	REJECT	
DO-1	OK ✓	REJECT	
DO-2	OK ✓	REJECT	
DO-3	OK ✓	REJECT	
DO-4	OK ✓	REJECT	
DO-5	OK ✓	REJECT	
DO-6	OK ✓	REJECT	
DO-7	OK ✓	REJECT	REFER TO TEST PROC.
DO-8	OK ✓	REJECT	
DO-9	OK ✓	REJECT	
DO-10	OK ✓	REJECT	
DO-11	OK ✓	REJECT	
DO-12	OK ✓	REJECT	
DO-13	OK ✓	REJECT	
DO-14	OK ✓	REJECT	
DO-15	OK ✓	REJECT	
DO-16	OK ✓	REJECT	
DO-17	OK ✓	REJECT	

S/N 105

Date of Test 5/27/75
Tested By

		Limits
7.9	SYSTEM FUNCTIONAL TEST	
7.9.2	Did an error occur?	
	No X	
	Yes ___ Address ___ Bits ___	0 errors
7.9.4	Did an error occur?	
	No X	
	Yes ___ Address ___ Bits ___	0 errors
7.9.10	Did an error occur?	
	No X	
	Yes ___ Address ___ Bits ___	0 errors
7.9.16	Did an error occur?	
	No X	
	Yes ___ Address ___ Bits ___	0 errors
7.10	RANDOM ACCESS CAPABILITY	
7.10.6	Did an error occur?	
	No ___	
	Yes ___ Address ___ Bits ___	0 errors
7.10.7	Did an error occur?	
	a) No X	
	Yes ___ Address ___ Bits ___	0 errors

S/N 105

Date of Test 5/22/75
Tested By

Limits

b) No X
Yes ____ Address ____ Bits ____ 0 errors

c) No X
Yes ____ Address ____ Bits ____ 0 errors

7.11 NON-VOLATILITY TEST

7.11.7 & 7.11.9 Did an error occur?
No X
Yes ____ Address ____ Bits ____ 0 errors

7.12 MEMORY SELECT TEST

7.12.3 Address 0000 (Octal) 0000

7.12.4 Address
0001 0000 (Octal) 0000
0010 0000 (Octal) 0000
0011 0000 (Octal) 0000
0100 0000 (Octal) 0000
0101 0000 (Octal) 0000
0110 0000 (Octal) 0000
0111 0000 (Octal) 0000
1000 0000 (Octal) 0000
1001 0000 (Octal) 0000
1010 0000 (Octal) 0000

S/N 105

Date of Test 5/27/75

Tested By [signature]

		Limits
Address 1011	000 (Octal)	0000
1100	0000 (Octal)	0000
1101	0000 (Octal)	0000
1110	0000 (Octal)	0000

7.12.6 Did an error occur?

No X

Yes _____ Address _____ Bits _____ 0 errors

7.13 WORST CASE PATTERN TEST

7.13.2 Did an error occur?

No X

Yes _____ Address _____ Bits _____ 0 errors

7.13.3 Did an error occur?

No X

Yes _____ Address _____ Bits _____ 0 errors

S/N 105

Date of Test 5/27/75

Tested By

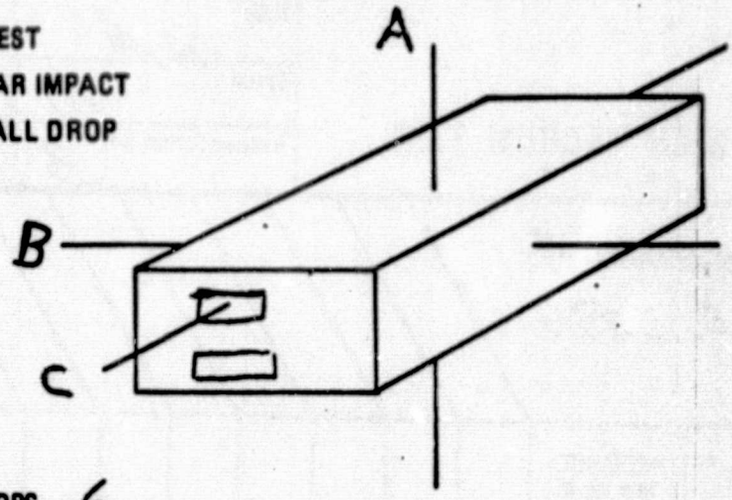
			Limits
7.13.4	a)	Did an error occur?	
		No X	
		Yes ____ Address ____ Bit ____	0 errors
	b)	Did an error occur?	
		No X	
		Yes ____ Address ____ Bit ____	0 errors

MOTOROLA INC.
Government Electronics Division

SHOCK TEST (DROP)

PROJECT 4601-400
DATE 5-16-75
SHEET 1 OF 1
W.O. NO. 30410
CONTROL NO. 11
UNIT Plated Wire Memory
SERIAL NO. 105
OPERATOR Sec 11
OBSERVER L. S. Gaulden
VIBRATION MOUNTS None
NO. OF DROPS PER ~~FACE~~ See below TOTAL NO. OF DROPS 6
ACCELERATION 30 G'S
PULSE DURATION 6 & 12 MS
SPEC DETAILS 13-P13722D

TYPE OF TEST
☒ MODULAR IMPACT
☐ FREE FALL DROP



DROP HEIGHT 1 3/16 & 4 3/4 IN.
PROGRAMMER PRESSURE N/A P.S.I.
TYPE OF WAVESHAPE ½ sine
BANDPASS FILTER .2 LOW FR. Hz
4300 HIGH FR. Hz
REMARKS 3 drops at 6 ms & 3 drops at 12 ms
Pads for 12 ms are 1 - 8x8x½ plaster
2 - 8x8x¼ rubber
3 - 8x8x 1/16 rubber
3 - 1" blue closed
1 - 1" blue open

PAD AND PLATE CONFIGURATION

ITEM NO.	PART NO.	DESCRIPTION	1
1	MRL 2357	alum plate	(B)
2	MOT 2776	1" pad open	(B)
3	MOT 2358	alum plate	(T)
4			
5			
6			
7			
8			
9			

6 MS 12 MS

AXIS	FACE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	1	/			/																
	2																				
B	1	/			/																
	2																				
C	1	/			/																
	2																				

PRECEDING PAGE BLANK NOT FILMED Test complete

83332 4/74 CTL 734

HIGH VACUUM TEST

Unit: PLATED WIRE MEMORY	Project: 4601-400
Model: N/A	Specification: 12-P-B701D
Serial: 105	Operator: JOE MOLLERE
Vacuum System No.: 3	Observer: LEE GOULDEN

CONTROL #1
W.O. 3039

TIME	PRESSURE (mm Hg A)	REMARKS
0945	ATM	START PUMPING
0949	5 MM	
0955	4×10^{-4}	
0930	3×10^{-5}	
1000	1.5×10^{-5}	
1030	1.2×10^{-5}	
1100	1×10^{-5}	
1110	2.9×10^{-6}	HEAT TO ATM

MOTOROLA INC.
Government Electronics Division

VIBRATION TEST

SHEET 1 OF _____ DATE 21 May 75

PROJECT 4401-400 UNIT Plated Wire Memory

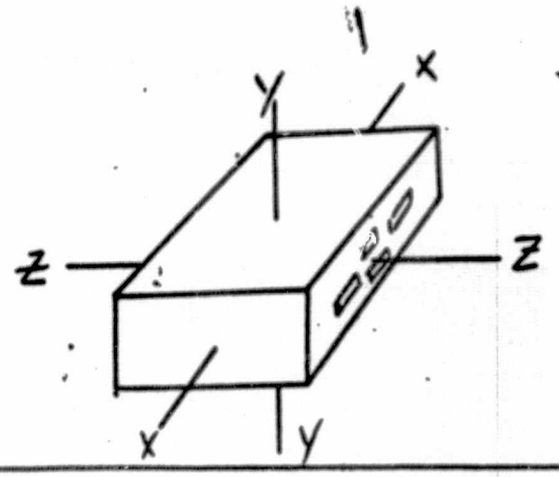
CONTROL NO. 01 & 02 W.O. NO. 3041

OPERATOR Pete Martin

OBSERVER Lee Gouldin

CYCLE TIME 4.3 min FREQ. 5 TO 2000 Hz

SPEC DETAILS _____



AXIS / RUN NO.	TIME START	TIME STOP	~~ACCUM~~ VIB. TIME	UNIT SER. NO.	DISPLACEMENT INCHES D.A.	ACCELERATION G's RMS / PK / MV (RMS)	REMARKS
Y	10:03	10:05	2 MIN	105	NA	5.61 / 56.1	shaped random
Y	10:10	10:14	4.3 MIN	105	.33	10g pk ± 2g pk / 70 ± 35	sine sweep 5-110-2000 Hz
Z	11:19	11:21	2 MIN	105	NA	5.61 / 56.1	shaped random
Z	11:23	11:27	4.3 MIN	105	.33	10g pk ± 2g pk / 70 ± 35	sine sweep 5-110-2000 Hz
X	12:41	12:43	2 MIN	105	NA	5.61 / 56.1	shaped random
X	12:45	12:49	4.3 MIN	105	.33	10g pk ± 2g pk / 70 ± 35	sine sweep 5-110-2000 Hz

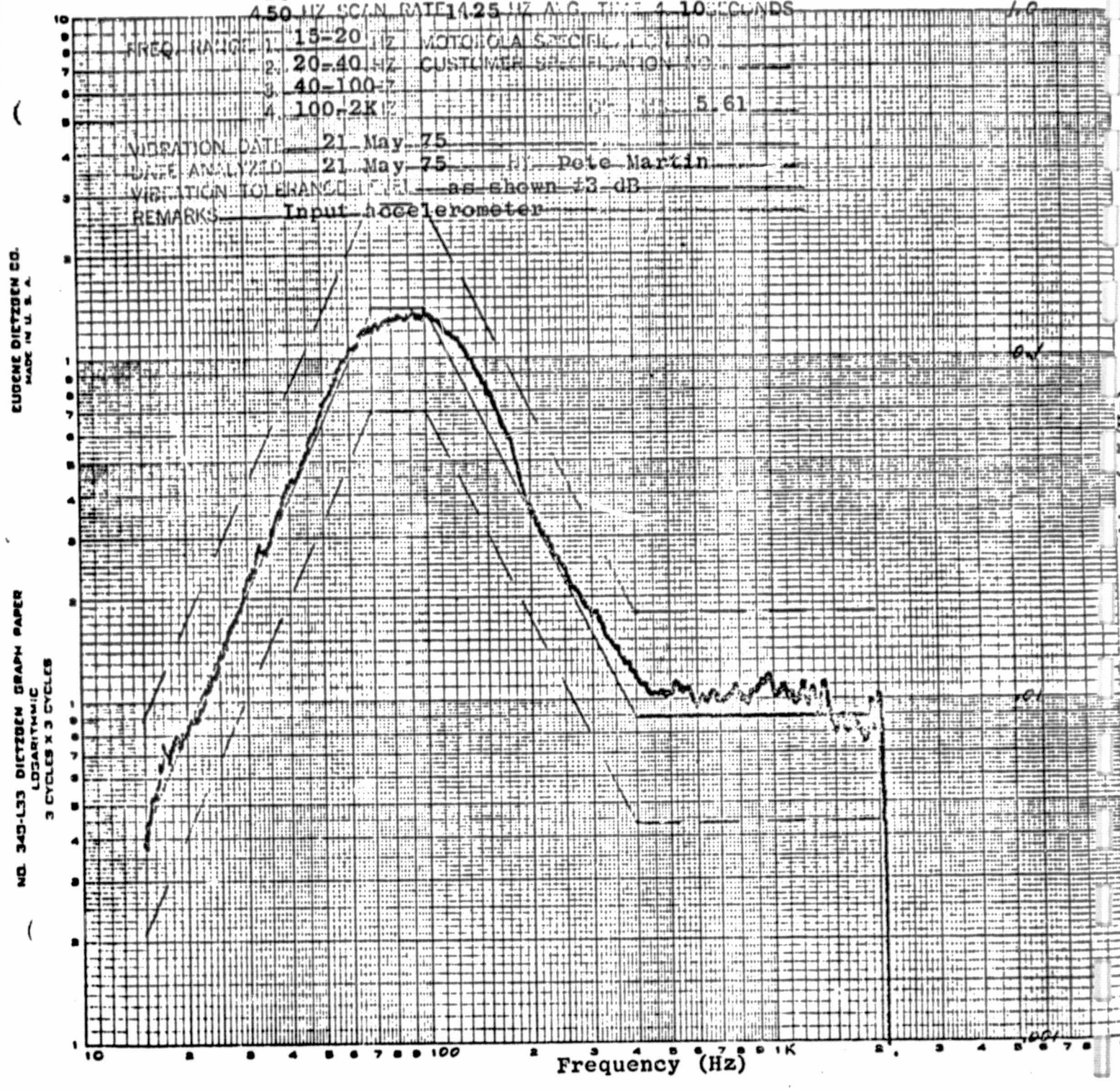
PROJECT 1601-400 UNIT P-W Memory SER. NO. 105

X & Z AXIS SAMPLE (LOOP) TIME 10 SECONDS

FILTER B.W. 1. 5 HZ SCAN RATE 1.125 HZ AVG. TIME 1. 10 SECONDS
2. 10 HZ SCAN RATE 2.25 HZ AVG. TIME 2. 10 SECONDS
3. 20 HZ SCAN RATE 3.5 HZ AVG. TIME 3. 10 SECONDS
4. 50 HZ SCAN RATE 11.25 HZ AVG. TIME 4. 10 SECONDS

FREQ. RANGE 1. 15-20 HZ MOTOROLA SPECIFICATION NO. ----
2. 20-40 HZ CUSTOMER SPECIFICATION NO. ----
3. 40-100 HZ
4. 100-2K HZ

VIBRATION DATE 21 May 75
DATE ANALYZED 21 May 75 BY Pete Martin
VIBRATION TOLERANCE LEVEL as shown ±3 dB
REMARKS Input accelerometer



EUGENE DIETZGEN CO. MADE IN U.S.A.

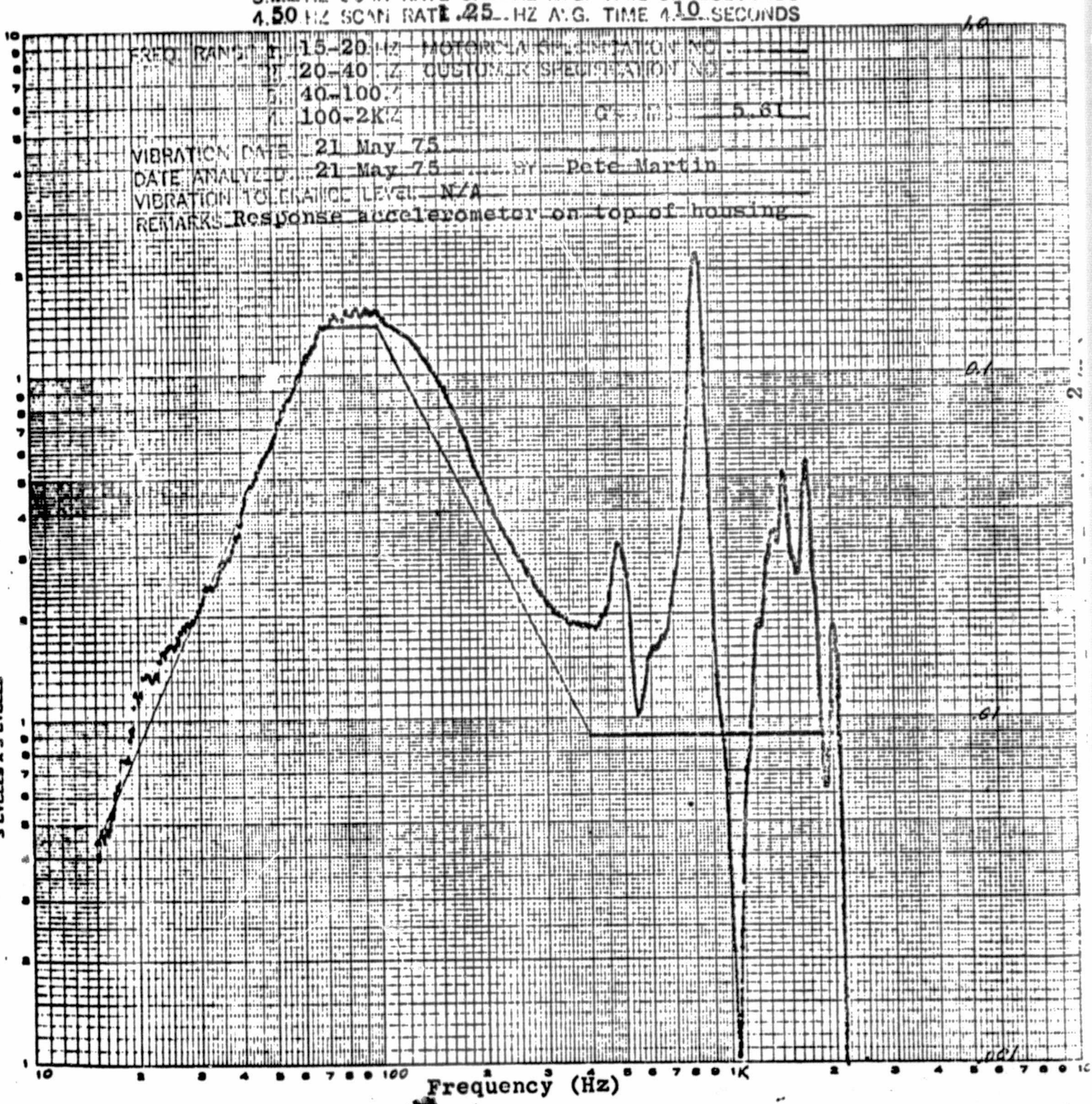
NO. 349-L33 DIETZGEN GRAPH PAPER LOGARITHMIC 3 CYCLES X 3 CYCLES

ORIGINAL PAGE IS
OF POOR QUALITY

PROJECT 4601-400 UNIT P-W Memory SER. NO. 105

X AXIS SAMPLE (LOOP) TIME _____ SECONDS

FILTER B.W. 1. 5 HZ SCAN RATE .125 HZ AVG. TIME 1 10 SECONDS
2. 10 HZ SCAN RATE .25 HZ AVG. TIME 2 10 SECONDS
3. 20 HZ SCAN RATE .5 HZ AVG. TIME 3 10 SECONDS
4. 50 HZ SCAN RATE 1.25 HZ AVG. TIME 4 10 SECONDS



ORIGINAL PAGE IS OF POOR QUALITY

PROJECT 4601-400 UNIT P-W Memory SER. NO. 105

X & Z AXIS SAMPLE (LOOP) TIME 10. SECONDS

FILTER B.W. 1. 5 HZ SCAN RATE 1.125 HZ AVG. TIME 1. 10 SECONDS
2. 10 HZ SCAN RATE 2.25 HZ AVG. TIME 2. 10 SECONDS
3. 20 HZ SCAN RATE 3.5 HZ AVG. TIME 3. 10 SECONDS
4. 50 HZ SCAN RATE 11.25 HZ AVG. TIME 4. 10 SECONDS

FREQ. RANGE 1. 15-20 HZ MOTOROLA SPECIFICATION NO. ____
2. 20-40 HZ CUSTUMER SPECIFICATION NO. ____
3. 40-100 HZ DATE 5-61
4. 100-2K HZ

VIBRATION DATE 21 May 75
DATE ANALYZED 21 May 75 BY Pete Martin
VIBRATION TOLERANCE LEVEL as shown ±3 dB
REMARKS Input accelerometer

1.0
0.1
.01
.001

Acceleration Spectral Density (G^2/Hz)

10 2 3 4 5 6 7 8 9 100 2 3 4 5 6 7 8 9 1K 2 3 4 5 6 7

Frequency (Hz)

EUGENE DIETZGEN CO. MADE IN U.S.A.

NO. 340-L33 DIETZGEN GRAPH PAPER LOGARITHMIC 3 CYCLES X 3 CYCLES

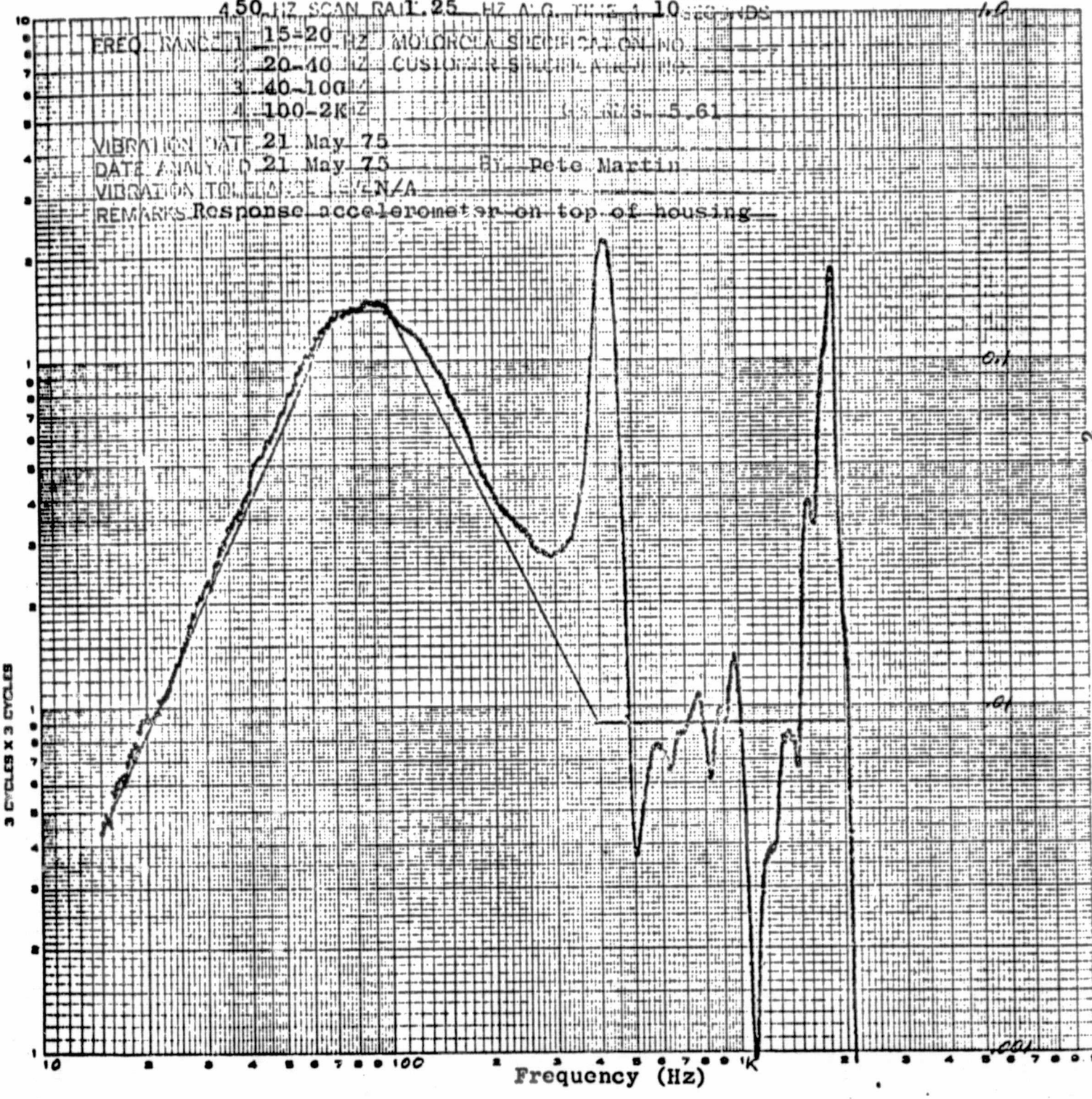
PROJECT 4601-400 UNIT P-W Memory SER. NO. 105

Z AXIS SAMPLE (LOOP) TIME 10 SECONDS

FILTER B.W. 1. 5 HZ SCAN RATE .125 HZ AVG. TIME 1. 10 SECONDS
2. 10 HZ SCAN RATE .25 HZ AVG. TIME 2. 10 SECONDS
3. 20 HZ SCAN RATE .5 HZ AVG. TIME 3. 10 SECONDS
4. 50 HZ SCAN RATE 1.25 HZ AVG. TIME 4. 10 SECONDS

FREQ. RANGE 1. 15-20 HZ MOTOROLA SPECIFICATION NO. ———
2. 20-40 HZ CUSTOMER SPECIFICATION NO. ———
3. 40-100 HZ
4. 100-2K HZ S/C MS-5.61

VIBRATION DATE 21 May 75
DATE ANALYZED 21 May 75 BY Pete Martin
VIBRATION TOLERANCE ± % N/A
REMARKS Response accelerometer on top of housing



EUGENE DIETZGEN CO.
3 CYCLES X 3 CYCLES LOGARITHMIC

ORIGINAL PAGE IS
OF POOR QUALITY

PROJECT 4601-400 UNIT P-W Memory SER. NO. 105

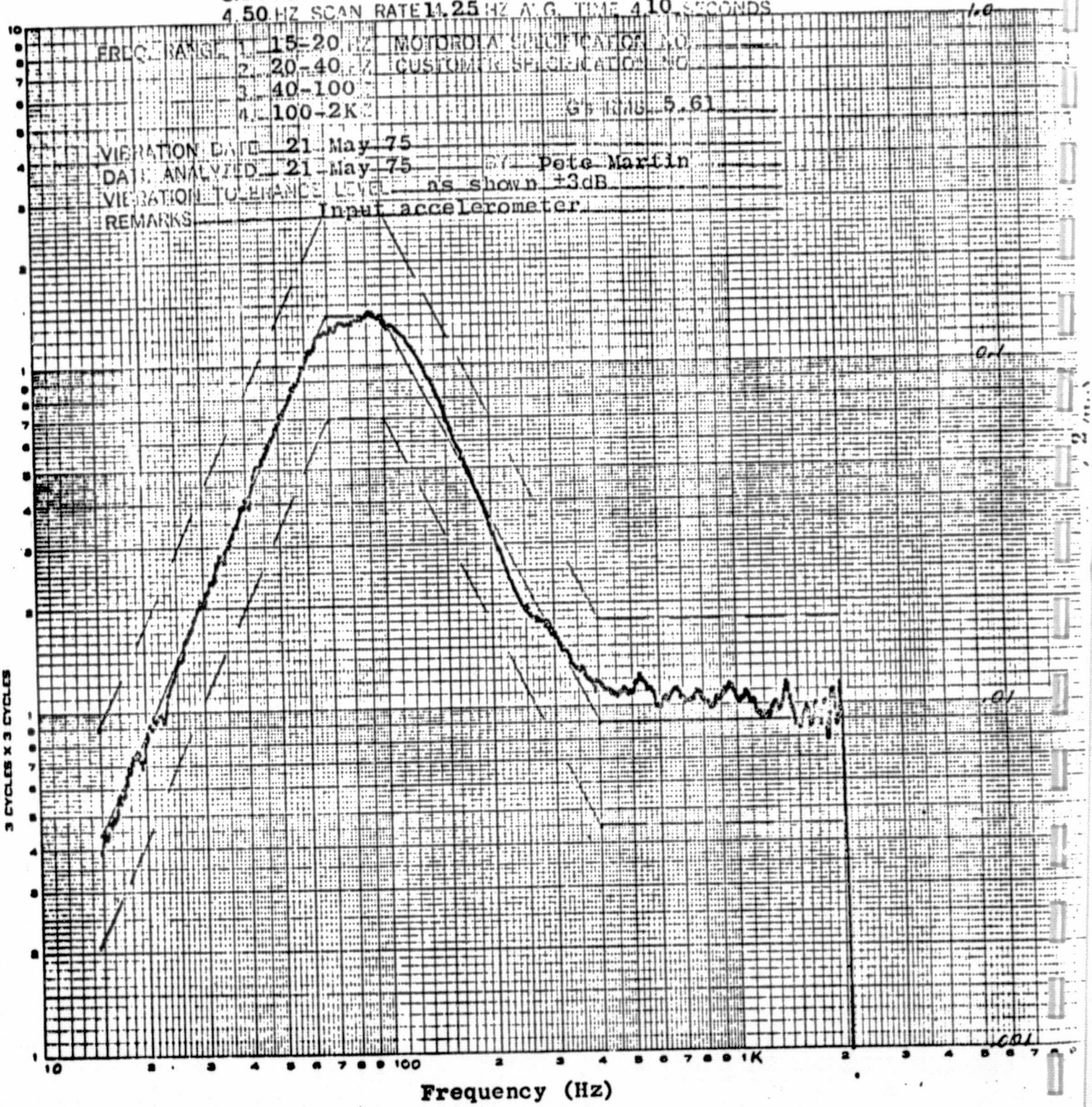
Y AXIS SAMPLE (LOOP) TIME 10 SECONDS

FILTER B.W. 1. 5 HZ SCAN RATE 1.125 HZ AVG. TIME 1.10 SECONDS
2. 10 HZ SCAN RATE 2.25 HZ AVG. TIME 2.10 SECONDS
3. 20 HZ SCAN RATE 3.5 HZ AVG. TIME 3.10 SECONDS
4. 50 HZ SCAN RATE 11.25 HZ AVG. TIME 4.10 SECONDS

FREQ. RANGE 1. 15-20 HZ MOTOROLA SPECIFICATION NO. ———
2. 20-40 HZ CUSTOMER SPECIFICATION NO. ———
3. 40-100
4. 100-2K

G's RMS 5.61

VIBRATION DATE 21 May 75
DATE ANALYZED 21 May 75 BY Pete Martin
VIBRATION TOLERANCE LEVEL as shown ±3dB
REMARKS Input accelerometer



EUGENE DIETZGEN CO. MADE IN U. S. A.

NO. 340-L33 DIETZGEN GRAPH PAPER LOGARITHMIC 3 CYCLES X 3 CYCLES

ATTACHMENT V

ACCEPTANCE TEST DATA SHEET

LOW POWER RANDOM ACCESS

SPACECRAFT MEMORY

PART NO. 01-P13701D

DRAWING NO. 12-P13721D

SERIAL NUMBER 106

(35 PAGES)

* APPLICATION	
NEXT ASSEMBLY	USED ON

* ASTERISK INDICATES DATA WHICH IS NONMANDATORY - FOR INFORMATION ONLY.

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
X1	Initial Release	—	—
X2	Incorporated changes prior to First Usage	3-16-73	H. Tweed
X3	Change -6.9V to -6.1V	6-18-73	H. Tweed
X4	Change 6000mw to 7000mw, pages 10, 17, 19, 30. Change weight from 6.0 to 6.5 pounds, page 2.	7-24-73	H. Tweed
X5	Add weight 5.8 pounds for magnesium chassis MCO S7835.	2-10-75	[signature]
X6	Revised per MCO S7845	4-28-75	[signature]

S/N 106

REV	X1	X4	X1	X3	X1	X1	X1	X1	X1																					
SHEET	27	28	29	30	31	32	33	34	35																					
REV STATUS	REV	X 5	X5	X1	X1	X1	X1	X1	X1	X1	X1	X4	X1	X1	X1	X1	X1	X6	X6	X6	X6	X6	X1	X1	X1	X1	X1	X1		
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26			

FOR ASSOCIATED LISTS SEE

INTERPRET DRAWING IN ACCORDANCE WITH STANDARDS PRESCRIBED BY

UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES AND END USE. FOR TOLERANCES SEE NOTE

DR BY H. Tweed

CHK BY

MFG

PROJ NO. 4339 4601

CONTR NO. NAS5-23163 NAS5-20576

RELEASE NOTICE

APPROVED DATE 1-2-73 H. Tweed

APPROVED DATE

MATERIAL:

MOTOROLA INC.
Government Electronics Division
8201 EAST McDOWELL ROAD
SCOTTSDALE, ARIZONA 85252

ACCEPTANCE TEST DATA SHEET,
LOW POWER RANDOM ACCESS SPACE-
CRAFT MEMORY, PART NO. 01-P13701D

SIZE	CODE IDENT NO.	DWG. NO.
A	94990	12-P13721D

SCALE

SHEET 1 OF 35

1. SCOPE

This test data sheet is to be used to record data as required by the Acceptance Test Procedure for the Low Power Random Access Spacecraft Memory.

2. REFERENCE INFORMATION

2.1 SPECIFICATIONS APPLICABLE

S-562-P-24	Low Power Random Access Spacecraft Memory
12-P13722D	Acceptance Test Procedure, Low Power Random Access Spacecraft Memory

3. TEST DATA

Unit S/N 106 Start Date of Tests 6-17-75

Tested by [signature]

ATP PARA. NO.

3.1 EQUIVALENT TEST EQUIPMENT

428A HP DC MILLIAMP METER

9120A DIG MULITMETER FLUKE

5245L HP COUNTER

4. PHYSICAL CHARACTERISTICS Limit

6.1 WEIGHT

Weight of LP-RASM = 5.58 Pounds ~~6.5 pounds (aluminum)~~ 5.8 pounds (magnesium)

S/N 106

Date of Test 6-17-75

Tested By [signature]

6.2 DIMENSIONS

		Limit
H = ~~2.625~~ 2.903	inches	
W = 8.633	inches	
MW = 8.964	inches	
D = 6.320	inches	
MD = 6.971	inches	
V = H X W X D = 158.4	inches^3	≤ 160 inches^3

MOTOROLA INC. Government Electronics Division	SIZE A	CODE IDENT NO. 94990	DWG NO. 12-P13721D
8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252	SCALE	REVISION	SHEET 3

S/N 106 Date of Test 06-17-75

Tested By [signature]

		Limit
7.4	CHASSIS ISOLATION	
	Impedance ≥10M	≥ 9 megohms
7.5	INPUT SIGNAL LOADING	
7.5.2	Current from INITIATE PULSE to Gnd 1.13 ma	≤ 2 ma
	Current from 2.4V to INITIATE PULSE .95 μa	≤ 20 μa
7.5.3	Current from MEM SEL 1 to Gnd 1.15 ma	≤ 2 ma
	Current from 2.4V to MEM SEL 1 .70 μa	≤ 20 μa
7.5.4	Current from MEM SEL 2 to Gnd 1.16 ma	≤ 2 ma
	Current from 2.4V to MEM SEL 2 .96 μa	≤ 20 μa
	Current from MEM SEL 3 to Gnd 1.16 ma	≤ 2 ma
	Current from 2.4V to MEL SEL 3 .98 μa	≤ 20 μa
	Current from MEM SEL 4 to Gnd 1.15 ma	≤ 2 ma
	Current from 2.4V to MEM SEL 4 .70 μa	≤ 20 μa
7.5.5	Current from READ/WRITE to Gnd .96 ma	≤ 2 ma
	Current from 2.4V to READ/WRITE 2.02 μa	≤ 20 μa
7.5.6	Current from ADDRESS 2^0 to Gnd .94 ma	≤ 2 ma
	Current from 2.4V to ADDRESS 2^0 7.04 μa	≤ 20 μa

S/N 106

Date of Test 06-17-75.

Tested By [signature]

		Limits
Current from ADDRESS 2^1 to Gnd	.94 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^1	6.52 μa	≤ 20 μa
Current from ADDRESS 2^2 to Gnd	1.03 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^2	7.62 μa	≤ 20 μa
Current from ADDRESS 2^3 to Gnd	.96 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^3	.904 μa	≤ 20 μa
Current from ADDRESS 2^4 to Gnd	.99 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^4	9.36 μa	≤ 20 μa

S/N 106

Date of Test 06-17-25

Tested By [signature]

		Limits
Current from ADDRESS 2^5 to Gnd	.88 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^5	4.93 μa	≤ 20μa
Current from ADDRESS 2^6 to Gnd	.92 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^5	6.12 μa	≤ 20μa
Current from ADDRESS 2^7 to Gnd	.96 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^7	5.42 μa	≤ 20μa
Current from ADDRESS 2^8 to Gnd	1.05 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^8	.67 μa	≤ 20μa
Current from ADDRESS 2^9 to Gnd	1.02 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^9	.75 μa	≤ 20μa
Current from ADDRESS 2^{10} to Gnd	.97 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^{10}	2.09 μa	≤ 20μa
Current from ADDRESS 2^{11} to Gnd	.97 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^{11}	2.14 μa	≤ 20μa
Current from DATA IN BIT 0 to Gnd	0.89 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 0	5.09 μa	≤ 20μa

S/N 106

Date of Test 06-17-75

Tested By [signature]

		Limits
Current from DATA IN BIT 1 to Gnd	.96 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 1	5.06 μa	≤ 20 μa
Current from DATA IN BIT 2 to Gnd	.89 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 2	4.65 μa	≤ 20 μa
Current from DATA IN BIT 3 to Gnd	.94 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 3	4.84 μa	≤ 20 μa
Current from DATA IN BIT 4 to Gnd	.94 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 4	4.65 μa	≤ 20 μa
Current from DATA IN BIT 5 to Gnd	.95 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 5	4.60 μa	≤ 20 μa
Current from DATA IN BIT 6 to Gnd	.92 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 6	5.97 μa	≤ 20 μa
Current from DATA IN BIT 7 to Gnd	.89 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 7	5.80 μa	≤ 20 μa
Current from DATA IN BIT 8 to Gnd	.91 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 8	6.26 μa	≤ 20 μa
Current from DATA IN BIT 9 to Gnd	.99 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 9	~~7.3~~ 7.69 μa	≤ 20 μa

MOTOROLA INC. Government Electronics Division 8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252	SIZE A	CODE IDENT NO. 94990	DWG NO. 12-P13721D
	SCALE	REVISION	SHEET 7

S/N 106

Date of Test 06-17-75

Tested By [signature]

		Limits
Current from DATA IN BIT 10 to Gnd	.98 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 10	6.57 μa	≤ 20 μa
Current from DATA IN BIT 11 to Gnd	1.07 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 11	6.51 μa	≤ 20 μa
Current from DATA IN BIT 12 to Gnd	.96 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 12	6.02 μa	≤ 20 μa
Current from DATA IN BIT 13 to Gnd	.95 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 13	6.11 μa	≤ 20 μa
Current from DATA IN BIT 14 to Gnd	.96 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 14	6.03 μa	≤ 20 μa
Current from DATA IN BIT 15 to Gnd	.98 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 15	6.54 μa	≤ 20 μa
Current from DATA IN BIT 16 to Gnd	.96 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 16	7.11 μa	≤ 20 μa
Current from DATA IN BIT 17 to Gnd	.96 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 17	6.95 μa	≤ 20 μa

S/N 106

Date of Test 06-17-75

Tested By

			Limit
7.6	VERIFICATION OF OPEN COLLECTOR ON OUTPUT SIGNALS		
7.6.3	READ COMPLETE voltage	10 mv	≤ 100 mv
7.6.4	DATA OUT BIT 0 voltage	30 mv	≤ 100 mv
	DATA OUT BIT 1 voltage	20 mv	≤ 100 mv
	DATA OUT BIT 2 voltage	20 mv	≤ 100 mv
	DATA OUT BIT 3 voltage	20 mv	≤ 100 mv
	DATA OUT BIT 4 voltage	20 mv	≤ 100 mv
	DATA OUT BIT 5 voltage	30 mv	≤ 100 mv
	DATA OUT BIT 6 voltage	25 mv	≤ 100 mv
	DATA OUT BIT 7 voltage	30 mv	≤ 100 mv
	DATA OUT BIT 8 voltage	10 mv	≤ 100 mv
	DATA OUT BIT 9 voltage	20 mv	≤ 100 mv
	DATA OUT BIT 10 voltage	30 mv	≤ 100 mv
	DATA OUT BIT 11 voltage	30 mv	≤ 100 mv
	DATA OUT BIT 12 voltage	30 mv	≤ 100 mv
	DATA OUT BIT 13 voltage	40 mv	≤ 100 mv
	DATA OUT BIT 14 voltage	30 mv	≤ 100 mv
	DATA OUT BIT 15 voltage	40 mv	≤ 100 mv
	DATA OUT BIT 16 voltage	30 mv	≤ 100 mv
	DATA OUT BIT 17 voltage	40 mv	≤ 100 mv

S/N 106

Date of Test 6-17-75

Tested By

				Limits
7.7	POWER CONSUMPTION (25°C)			
7.7.1	Memory +5V Voltage	5.003	Volts	
	Memory -6.1V voltage	6.100	Volts	
	+5V Current	10.0	ma	
	+5V Power	50.03	mw	
7.7.2	Memory -6.1V Current	3.2	ma	
	Memory -6.1V Power	19.52	mw	
7.7.3	Total Memory Idle Power	69.55	mw	170 mw max
7.7.5	Memory +5V Voltage	5.000	Volts	
	Memory -6.1V Voltage	6.101	Volts	
	+5V Current	670	ma	
	+5V Power	3350	mw	
7.7.6	Memory -6.1V Current	228	ma	
	Memory -6.1V Power	1491	mw	
7.7.7	Total Active Power	4841	mw	7000 mw max.
7.8	READ COMPLETE TIMING			
7.8.5	Delay	410	ns	500 ns max.
	Duration	320	ns	250 ns min 450 ns max.

S/N 106

Date of Test 06-17-75

Tested by [signature]

LIMITS

7.8.7 & 7.8.8 READ COMPLETE/DATA OUTPUT TIMING

DO-0	OK ✓	REJECT
DO-1	OK ✓	REJECT
DO-2	OK ✓	REJECT
DO-3	OK ✓	REJECT
DO-4	OK ✓	REJECT
DO-5	OK ✓	REJECT
DO-6	OK ✓	REJECT
DO-7	OK ✓	REJECT
DO-8	OK ✓	REJECT
DO-9	OK ✓	REJECT
DO-10	OK ✓	REJECT
DO-11	OK ✓	REJECT
DO-12	OK ✓	REJECT
DO-13	OK ✓	REJECT
DO-14	OK ✓	REJECT
DO-15	OK ✓	REJECT
DO-16	OK ✓	REJECT
DO-17	OK ✓	REJECT

REFER TO TEST PROC.

S/N 106

Date of Test 06-17-75
Tested By [signature]

Limits

7.9 SYSTEM FUNCTIONAL TEST

7.9.2 Did an error occur?
No ✓
Yes ____ Address ____ Bits ____ 0 errors

7.9.4 Did an error occur?
No ✓
Yes ____ Address ____ Bits ____ 0 errors

7.9.10 Did an error occur?
No ✓
Yes ____ Address ____ Bits ____ 0 errors

7.9.16 Did an error occur?
No ✓
Yes ____ Address ____ Bits ____ 0 errors

7.10 RANDOM ACCESS CAPABILITY

7.10.6 Did an error occur?
No ✓
Yes ____ Address ____ Bits ____ 0 errors

7.10.7 Did an error occur?
a) No ✓
Yes ____ Address ____ Bits ____ 0 errors

S/N 106

Date of Test 06-17-75
Tested By

Limits (M)

b) No ✓

Yes ____ Address ____ Bits ____ 0 errors

c) No ✓

Yes ____ Address ____ Bits ____ 0 errors

7.11 NON-VOLATILITY TEST

7.11.7 & 7.11.9 Did an error occur?

No ✓

Yes ____ Address ____ Bits ____ 0 errors

7.12 MEMORY SELECT TEST

7.12.3 Address 0000 (Octal). 0000

7.12.4 Address

0001	0000 (Octal)	0000
0010	0000 (Octal)	0000
0011	0000 (Octal)	0000
0100	0000 (Octal)	0000
0101	0000 (Octal)	0000
0110	0000 (Octal)	0000
0111	0000 (Octal)	0000
1000	0000 (Octal)	0000
1001	0000 (Octal)	0000
1010	0000 (Octal)	0000

S/N 106

Date of Test 06-17-75

Tested By

		Limits
Address 1011	0000 (Octal)	0000
1100	0000 (Octal)	0000
1101	0000 (Octal)	0000
1110	0000 (Octal)	0000

7.12.6 Did an error occur?

No ✓

Yes ____ Address ____ Bits ____ 0 errors

7.13 WORST CASE PATTERN TEST

7.13.2 Did an error occur?

No ✓

Yes ____ Address ____ Bits ____ 0 errors

7.13.3 Did an error occur?

No ✓

Yes ____ Address ____ Bits ____ 0 errors

S/N 106

Date of Test 06-17-5

Tested By

Limits (M 47)

7.13.4 a) Did an error occur?

No ✓

Yes _____ Address _____ Bit _____ 0 errors

b) Did an error occur?

No ✓

Yes _____ Address _____ Bit _____ 0 errors

S/N 106

DATE OF TEST 6-29-75

TESTED BY [signature]

8. TEMPERATURE TEST — LIMITS

8.2.1 TIME 0705

8.2.2 LOW TEMPERATURE

THERMISTOR RESISTANCE

150 MINUTES 213 K OHMS

160 MINUTES 216 K OHMS % CHANGE 1.34

170 MINUTES 219 K OHMS % CHANGE _____

180 MINUTES _____ K OHMS % CHANGE _____

190 MINUTES _____ K OHMS % CHANGE _____

8.2.3 DID AN ERROR OCCUR?

NO ✓

YES _____ ADDRESS _____ BITS _____ 0 ERRORS

8.2.4

-6.1 V VOLTAGE	6.402 VOLTS	+5 V VOLTAGE	5.252 VOLTS
-6.1 V CURRENT	14.5 ma	+5 V CURRENT	10.2 ma
-6.1 V POWER	92.82 mw	+5 V POWER	53.57 mw

TOTAL MEMORY IDLE POWER 146.4 mw — 170 mw MAX

8.2.5

-6.1 V VOLTAGE	6.401 VOLTS	+5 V VOLTAGE	5.256 VOLTS
-6.1 V CURRENT	255 ma	+5 V CURRENT	680 ma
-6.1 V POWER	1632 mw	+5 V POWER	3574 mw

TOTAL MEMORY OPERATING POWER 5206 mw — 7000 mw MAX

S/N 106

DATE OF TEST 06-2475

TESTED BY [signature]

LIMITS

8.2.6 DID AN ERROR OCCUR?

NO ✓

YES ___ ADDRESS ___ BIT ___ 0 ERRORS

8.2.8 WC a) DID AN ERROR OCCUR?

NO ✓

YES ___ ADDRESS ___ BIT ___ 0 ERRORS

WC b) DID AN ERROR OCCUR?

NO ✓

YES ___ ADDRESS ___ BIT ___ 0 ERRORS

WC c) DID AN ERROR OCCUR?

NO ✓

YES ___ ADDRESS ___ BIT ___ 0 ERRORS

WC d) DID AN ERROR OCCUR?

NO ✓

YES ___ ADDRESS ___ BIT ___ 0 ERRORS

8.2.9 WC a) DID AN ERROR OCCUR?

NO ✓

YES ___ ADDRESS ___ BIT ___ 0 ERRORS

S/N 106

DATE OF TEST 06-24-75

TESTED BY [signature]

LIMITS

8.2.9 (Cont.)

WC b) DID AN ERROR OCCUR?

NO ✓

YES ___ ADDRESS ___ BIT ___ 0 ERRORS

WC c) DID AN ERROR OCCUR?

NO ✓

YES ___ ADDRESS ___ BIT ___ 0 ERRORS

WC d) DID AN ERROR OCCUR?

NO ✓

YES ___ ADDRESS ___ BIT ___ 0 ERRORS

8.3 INTERMEDIATE TEMPERATURE TEST

TIME 10:37

8.3.2 TIME	THERMISTOR READING.		DID ANY ERROR OCCUR?		
10:47	110	K OHMS	NO ✓	YES ___	0 ERRORS
10:57	4.3	K OHMS	NO ✓	YES ___	0 ERRORS
11:07	2.0	K OHMS	NO ✓	YES ___	0 ERRORS
11:17	9.8	K OHMS	NO ✓	YES ___	0 ERRORS
11:27	3.6	K OHMS	NO ✓	YES ___	0 ERRORS
11:37	3.6	K OHMS	NO ✓	YES ___	0 ERRORS
11:47	3.8	K OHMS	NO ✓	YES ___	0 ERRORS
11:57	2.2	K OHMS	NO ✓	YES ___	0 ERRORS
12:07	1.9	K OHMS	NO ✓	YES ___	0 ERRORS
___	___	K OHMS	NO ___	YES ___	0 ERRORS
___	___	K OHMS	NO ___	YES ___	0 ERRORS
___	___	K OHMS	NO ___	YES ___	0 ERRORS

S/N 106

DATE OF TEST 06-24-75

TESTED BY [signature]

LIMITS

8.3.3 TIME 11:20

8.4 50 MINUTES 1.601 K OHMS

60 MINUTES 1.510 K OHMS % CHANGE 5.1%

70 MINUTES 1.450 K OHMS % CHANGE 4.0%

80 MINUTES 1.433 K OHMS % CHANGE 1.2%

90 MINUTES _____ K OHMS % CHANGE

8.4.1 -6.1 V VOLTAGE 6.407 VOLTS +5 V VOLTAGE 5.251 VOLTS

-6.1 V CURRENT 8.0 ma +5 V CURRENT 11.5 ma

-6.1 V POWER 52.21 mw +5 V POWER 60.38 mw

TOTAL MEMORY IDLE POWER 112.59 mw 170 mw MAX

8.4.2 DID AN ERROR OCCUR?

NO ✓

YES ___ ADDRESS _____ BIT _____ 0 ERRORS

8.4.3 -6.1 V VOLTAGE 6.402 VOLTS +5 V VOLTAGE 5.250 VOLTS

-6.1 V CURRENT 263 ma +5 V VOLTAGE 760 ma

-6.1 V POWER 1696.5 mw +5 V POWER 3990 mw

TOTAL MEMORY OPERATING POWER 56865 mw 7000 mw MAX

8.4.4 WC a) DID AN ERROR OCCUR?

NO ✓

YES ___ ADDRESS _____ BIT _____ 0 ERRORS

S/N 106 DATE OF TEST 06-24-75

TESTED BY

LIMITS

8.4.4 (Cont.)

WC b) DID AN ERROR OCCUR?

NO ✓

YES ___ ADDRESS ___ BIT ___ 0 ERRORS

WC c) DID AN ERROR OCCUR?

NO ✓

YES ___ ADDRESS ___ BIT ___ 0 ERRORS

WC d) DID AN ERROR OCCUR ?

NO ✓

YES ___ ADDRESS ___ BIT ___ 0 ERRORS

8.4.6 WC a) DID AN ERROR OCCUR?

NO ✓

YES ___ ADDRESS ___ BIT ___ 0 ERRORS

WC b) DID AN ERROR OCCUR?

NO ✓

YES ___ ADDRESS ___ BIT ___ 0 ERRORS

WC c) DID AN ERROR OCCUR?

NO ✓

YES ___ ADDRESS ___ BIT ___ 0 ERRORS

WC d) DID AN ERROR OCCUR?

NO ✓

YES ___ ADDRESS ___ BIT ___ 0 ERRORS

8.4.7 DID AN ERROR OCCUR?

NO ✓

YES ___ ADDRESS ___ BIT ___ 0 ERRORS

S/N 106 Date of Test 6-16-75

Tested by [signature]

Limits

9. VACUUM TEST

9.2 Did Any Bit Errors Occur?

No ✓

Yes _____ Address _____ Bits _____ 0 Errors

9.2.1 Fast Decompression

Date 6-18-75 Tested by [signature]

Did Any Bit Errors Occur?

No ✓

Yes _____ Address _____ Bits _____ 0 Errors

9.2.2 Hard Vacuum

Date 6-18-75 Tested by [signature]

Did Any Bit Errors Occur?

No ✓

Yes _____ Address _____ Bits _____ 0 Errors

10. VIBRATION TEST

Date 5-21-75 Tested by [signature]

SINE SWEEP

Axis X - Did Any Bit Errors Occur?

No ✓

Yes _____ Freq _____ Address _____ Bits _____ 0 Errors

S/N 106 Date of Test 6-24-75

Tested by [signature]

Axis Y - Did Any Bit Error Occur? Limits

No ✓

Yes ____ Freq _____ Address ____ Bits _____ 0 Errors

Axis Z - Did Any Bit Errors Occur?

No ✓

Yes ____ Freq _____ Address _____ Bits _____ 0 Errors

RANDOM VIBRATION

Axis X - Did Any Bit Errors Occur?

No ✓

Yes ____ Freq _____ Address _____ Bits _____ 0 Errors

Axis Y - Did Any Bit Errors Occur?

No ✓

Yes ____ Freq _____ Address _____ Bits _____ 0 Errors

Axis Z - Did Any Bit Errors Occur?

No ✓

Yes ____ Freq _____ Address _____ Bits _____ 0 Errors

11. SHOCK TEST

Date 6-18-75 Tested By [signature]

6 MILLISECOND DURATION SHOCK

Y Direction - Did Any Bit Errors Occur?

No ✓

Yes ____ Address _____ Bits _____ 0 Errors

S/N 106

Date of Test 1-16-75

Tested by [illegible]

Limits

Z Direction - Did Any Bit Errors Occur?

No ✓

Yes _____ Address _____ Bits _____ 0 Errors

X Direction - Did Any Bit Errors Occur?

No ✓

Yes _____ Address _____ Bits _____ 0 Errors

12 MILLISECOND DURATION SHOCK

Y Direction - Did Any Bit Errors Occur?

No ✓

Yes _____ Address _____ Bits _____ 0 Errors

Z Direction - Did Any Bit Errors Occur?

No ✓

Yes _____ Address _____ Bits _____ 0 Errors

X Direction - Did Any Bit Errors Occur?

No ✓

Yes _____ Address _____ Bits _____ 0 Errors

S/N 106 Date of Test 6/25/75.

Tested By

			Limit
7.4	CHASSIS ISOLATION		
	Impedance	710 meg Ω	≥ 9 megohms
7.5	INPUT SIGNAL LOADING		
7.5.2	Current from INITIATE PULSE to Gnd	1.15 ma	≤ 2 ma
	Current from 2.4V to INITIATE PULSE	.97 μa	≤ 20 μa
7.5.3	Current from MEM SEL 1 to Gnd	1.15 ma	≤ 2 ma
	Current from 2.4V to MEM SEL 1	~~1.68~~ .68 μa	≤ 20 μa
7.5.4	Current from MEM SEL 2 to Gnd	1.15 ma	≤ 2 ma
	Current from 2.4V to MEM SEL 2	.94 μa	≤ 20 μa
	Current from MEM SEL 3 to Gnd	1.15 ma	≤ 2 ma
	Current from 2.4V to MEL SEL 3	.96 μa	≤ 20 μa
	Current from MEM SEL 4 to Gnd	1.15 ma	≤ 2 ma
	Current from 2.4V to MEM SEL 4	.69 μa	≤ 20 μa
7.5.5	Current from READ/WRITE to Gnd	.96 ma	≤ 2 ma
	Current from 2.4V to READ/WRITE	2.02 μa	≤ 20 μa
7.5.6	Current from ADDRESS 2^0 to Gnd	.94 ma	≤ 2 ma
	Current from 2.4V to ADDRESS 2^0	6.99 μa	≤ 20 μa

S/N 106

Date of Test 6/25/75

Tested By [signature]

		Limits
Current from ADDRESS 2^1 to Gnd	.94 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^1	6.47 μa	≤ 20 μa
Current from ADDRESS 2^2 to Gnd	1.02 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^2	7.59 μa	≤ 20 μa
Current from ADDRESS 2^3 to Gnd	.95 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^3	8.96 μa	≤ 20 μa
Current from ADDRESS 2^4 to Gnd	.98 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^4	9.25 μa	≤ 20 μa

(M 489)

S/N 106

Date of Test 6/25/75

Tested By [signature]

		Limits
Current from ADDRESS 2^5 to Gnd	.84 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^5	4.90 μa	≤ 20μa
Current from ADDRESS 2^6 to Gnd	.91 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^5	6.07 μa	≤ 20μa
Current from ADDRESS 2^7 to Gnd	1.64 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^7	10.81 μa	≤ 20μa
Current from ADDRESS 2^8 to Gnd	1.88 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^8	4.47 μa	≤ 20μa
Current from ADDRESS 2^9 to Gnd	1.93 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^9	3.41 μa	≤ 20μa
Current from ADDRESS 2^{10} to Gnd	1.89 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^{10}	11.64 μa	≤ 20μa
Current from ADDRESS 2^{11} to Gnd	1.88 ma	≤ 2 ma
Current from 2.4V to ADDRESS 2^{11}	9.25 μa	≤ 20μa
Current from DATA IN BIT 0 to Gnd	.89 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 0	5.05 μa	≤ 20μa

S/N 106

Date of Test 6/25/75

Tested By [signature]

		Limits
Current from DATA IN BIT 1 to Gnd	.90 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 1	5.04 μa	≤ 20 μa
Current from DATA IN BIT 2 to Gnd	.89 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 2	4.62 μa	≤ 20 μa
Current from DATA IN BIT 3 to Gnd	.94 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 3	4.82 μa	≤ 20 μa
Current from DATA IN BIT 4 to Gnd	.94 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 4	4.63 μa	≤ 20 μa
Current from DATA IN BIT 5 to Gnd	.94 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 5	4.58 μa	≤ 20 μa
Current from DATA IN BIT 6 to Gnd	.92 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 6	5.92 μa	≤ 20 μa
Current from DATA IN BIT 7 to Gnd	.88 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 7	5.76 μa	≤ 20 μa
Current from DATA IN BIT 8 to Gnd	.90 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 8	6.20 μa	≤ 20 μa
Current from DATA IN BIT 9 to Gnd	.99 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 9	7.62 μa	≤ 20 μa

S/N 106

Date of Test 6/25/73

Tested By [signature]

		Limits
Current from DATA IN BIT 10 to Gnd	.97 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 10	6.43 μa	≤ 20μa
Current from DATA IN BIT 11 to Gnd	1.01 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 11	6.44 μa	≤ 20μa
Current from DATA IN BIT 12 to Gnd	.95 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 12	5.98 μa	≤ 20μa
Current from DATA IN BIT 13 to Gnd	.95 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 14	6.07 μa	≤ 20μa
Current from DATA IN BIT 14 to Gnd	.95 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 14	6.00 μa	≤ 20μa
Current from DATA IN BIT 15 to Gnd	.98 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 15	6.50 μa	≤ 20μa
Current from DATA IN BIT 16 to Gnd	.95 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 17	7.06 μa	≤ 20μa
Current from DATA IN BIT 17 to Gnd	.95 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 17	6.92 μa	≤ 20μa

S/N 106

Date of Test 6/25/75

Tested By

			Limit
7.6	VERIFICATION OF OPEN COLLECTOR ON OUTPUT SIGNALS		
7.6.3	READ COMPLETE voltage	15 mv	≤ 100 mv
7.6.4	DATA OUT BIT 0 voltage	10 mv	≤ 100 mv
	DATA OUT BIT 1 voltage	5 mv	≤ 100 mv
	DATA OUT BIT 2 voltage	0 mv	≤ 100 mv
	DATA OUT BIT 3 voltage	5 mv	≤ 100 mv
	DATA OUT BIT 4 voltage	15 mv	≤ 100 mv
	DATA OUT BIT 5 voltage	15 mv	≤ 100 mv
	DATA OUT BIT 6 voltage	10 mv	≤ 100 mv
	DATA OUT BIT 7 voltage	0 mv	≤ 100 mv
	DATA OUT BIT 8 voltage	0 mv	≤ 100 mv
	DATA OUT BIT 9 voltage	10 mv	≤ 100 mv
	DATA OUT BIT 10 voltage	15 mv	≤ 100 mv
	DATA OUT BIT 11 voltage	10 mv	≤ 100 mv
	DATA OUT BIT 12 voltage	10 mv	≤ 100 mv
	DATA OUT BIT 13 voltage	20 mv	≤ 100 mv
	DATA OUT BIT 14 voltage	15 mv	≤ 100 mv
	DATA OUT BIT 15 voltage	15 mv	≤ 100 mv
	DATA OUT BIT 16 voltage	5 mv	≤ 100 mv
	DATA OUT BIT 17 voltage	20 mv	≤ 100 mv

(M 4/89)

S/N 106

Date of Test 6/25/75

Tested By [signature]

			Limits
7.7	POWER CONSUMPTION (25°C)		
7.7.1	Memory +5V Voltage	+5.006 Volts	
	Memory -6.1V voltage	-6.103 Volts	
	+5V Current	10 ma	
	+5V Power	50.06 mw	
7.7.2	Memory -6.1V Current	3.3 ma	
	Memory -6.1V Power	20.13 mw	
7.7.3	Total Memory Idle Power	70.19 mw	170 mw max
7.7.5	Memory +5V Voltage	+5.007 Volts	
	Memory -6.1V Voltage	-6.105 Volts	
	+5V Current	670 ma	
	+5V Power	3354.69 mw	
7.7.6	Memory -6.1V Current	230 ma	
	Memory -6.1V Power	1404.15 mw	
7.7.7	Total Active Power	4758.84 mw	7000 mw max.
7.8	READ COMPLETE TIMING		
7.8.5	Delay	390 ns	500 ns max.
	Duration	320 ns	250 ns min 450 ns max.

MOTOROLA INC.
Government Electronics Division
8201 E. McDOWELL ROAD
SCOTTSDALE, ARIZONA 85252

SIZE	CODE IDENT NO.	DWG NO.
A	94990	12-P13721D

SCALE | REVISION | SHEET 30

S/N 106

Date of Test 6/25/75

Tested by [signature]

LIMITS

7.8.7 & 7.8.8 READ COMPLETE/DATA OUTPUT TIMING

DO-0	OK ✓	REJECT
DO-1	OK ✓	REJECT
DO-2	OK ✓	REJECT
DO-3	OK ✓	REJECT
DO-4	OK ✓	REJECT
DO-5	OK ✓	REJECT
DO-6	OK ✓	REJECT
DO-7	OK ✓	REJECT
DO-8	OK ✓	REJECT
DO-9	OK ✓	REJECT
DO-10	OK ✓	REJECT
DO-11	OK ✓	REJECT
DO-12	OK ✓	REJECT
DO-13	OK ✓	REJECT
DO-14	OK ✓	REJECT
DO-15	OK ✓	REJECT
DO-16	OK ✓	REJECT
DO-17	OK ✓	REJECT

REFER TO TEST PROC.

S/N 106

Date of Test 6/25/75
Tested By

Limits

7.9 SYSTEM FUNCTIONAL TEST

7.9.2 Did an error occur?

No ✓

Yes ___ Address ___ Bits ___ 0 errors

7.9.4 Did an error occur?

No ✓

Yes ___ Address ___ Bits ___ 0 errors

7.9.10 Did an error occur?

No ✓

Yes ___ Address ___ Bits ___ 0 errors

7.9.16 Did an error occur?

No ✓

Yes ___ Address ___ Bits ___ 0 errors

7.10 RANDOM ACCESS CAPABILITY

7.10.6 Did an error occur?

No ✓

Yes ___ Address ___ Bits ___ 0 errors

7.10.7 Did an error occur?

a) No ✓

Yes ___ Address ___ Bits ___ 0 errors

S/N 106

Date of Test 6/25/75
Tested By

					Limits
	b) No ✓				
	Yes ____	Address ____	Bits ____		0 errors
	c) No ✓				
	Yes ____	Address ____	Bits ____		0 errors
7.11	NON-VOLATILITY TEST				
7.11.7 & 7.11.9	Did an error occur?				
	No ✓				
	Yes ____	Address ____	Bits ____		0 errors
7.12	MEMORY SELECT TEST				
7.12.3	Address 0000 (Octal)				0000
7.12.4	Address 0001 0000 (Octal)				0000
	0010 0000 (Octal)				0000
	0011 0000 (Octal)				0000
	0100 0000 (Octal)				0000
	0101 0000 (Octal)				0000
	0110 0000 (Octal)				0000
	0111 0000 (Octal)				0000
	1000 0000 (Octal)				0000
	1001 0000 (Octal)				0000
	1010 0000 (Octal)				0000

S/N 106

Date of Test 6/25/75

Tested By

		Limits
Address 1011	0000 (Octal)	0000
1100	0000 (Octal)	0000
1101	0000 (Octal)	0000
1110	0000 (Octal)	0000

7.12.6 Did an error occur?

No ✓

Yes _____ Address _____ Bits _____ 0 errors

7.13 WORST CASE PATTERN TEST

7.13.2 Did an error occur?

No ✓

Yes _____ Address _____ Bits _____ 0 errors

7.13.3 Did an error occur?

No ✓

Yes _____ Address _____ Bits _____ 0 errors

S/N 106

Date of Test 6/25/75

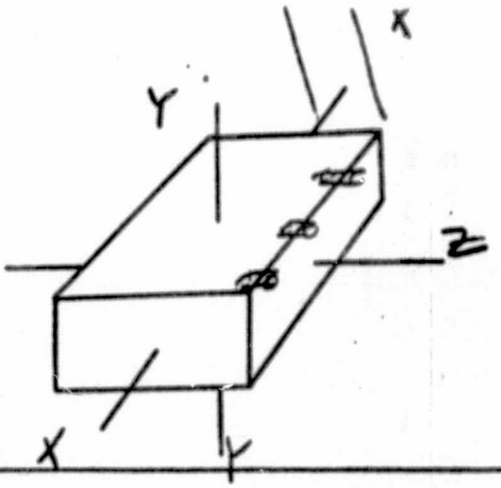
Tested By

		Limits
7.13.4	a) Did an error occur?	
	No ✓	
	Yes ____ Address ____ Bit ____	0 errors
	b) Did an error occur?	
	No ✓	
	Yes ____ Address ____ Bit ____	0 errors

MOTOROLA INC.
Government Electronics Division

VIBRATION TEST

SHEET 1 OF 1 DATE 6-24-75
PROJECT 469 400 UNIT P/W MEMORY
CONTROL NO. 01-07 W.O. NO. 3041
OPERATOR D. Smith
OBSERVER J. Goulden
CYCLE TIME ~~2 min/axis~~ FREQ. 15 TO 2K HZ SHAPED RANDOM
SPEC DETAILS 12-P137220



AXIS / RUN NO.	TIME START	TIME STOP	ACCUM-ULATED VIB. TIME	UNIT SER. NO.	DISPLACEMENT INCHES D.A.	ACCELERATION V RMS V PK G'S / MV (RMS)	REMARKS
Z 1	1725	1727	2 MIN	106	NA	5.6 / 56.1	RESPONSE ACCEL = 6.5g RMS SHAPED RANDOM NOISE
Z 2	1735	2h 1742	4 MIN 21 SEC	106	.33	10-5 / 10-35	5-2KHZ SINE SWEEP
X 3	1810	2h 1817	4 MIN 21 SEC	106	.33	10-5 / 10-35	" " "
X 4	1832	1840	2 MIN	106	NA	5.6 / 56.1	RESPONSE ACCEL = 6.5g RMS SHAPED RANDOM NOISE
Y 5	2024	2026	2 MIN	106	NA	5.6 / 56.1	SHAPED RANDOM NOISE
Y 6	2028	2h 32	4 MIN 1 SEC	106	.33	10-5 / 10-35	5-2KHZ SINE SWEEP. D. Smith
Y 7	2038	2h 2042	1 MIN 37 SEC	106	.33	10-5 / 10-35	5-~~2K~~ 47 HZ SINE SWEEP
Y 8	2050	2h 21 2054	1 MIN 21 SEC	106	.33	10-5 / 10-35	5-2KHZ " "
							END TEST

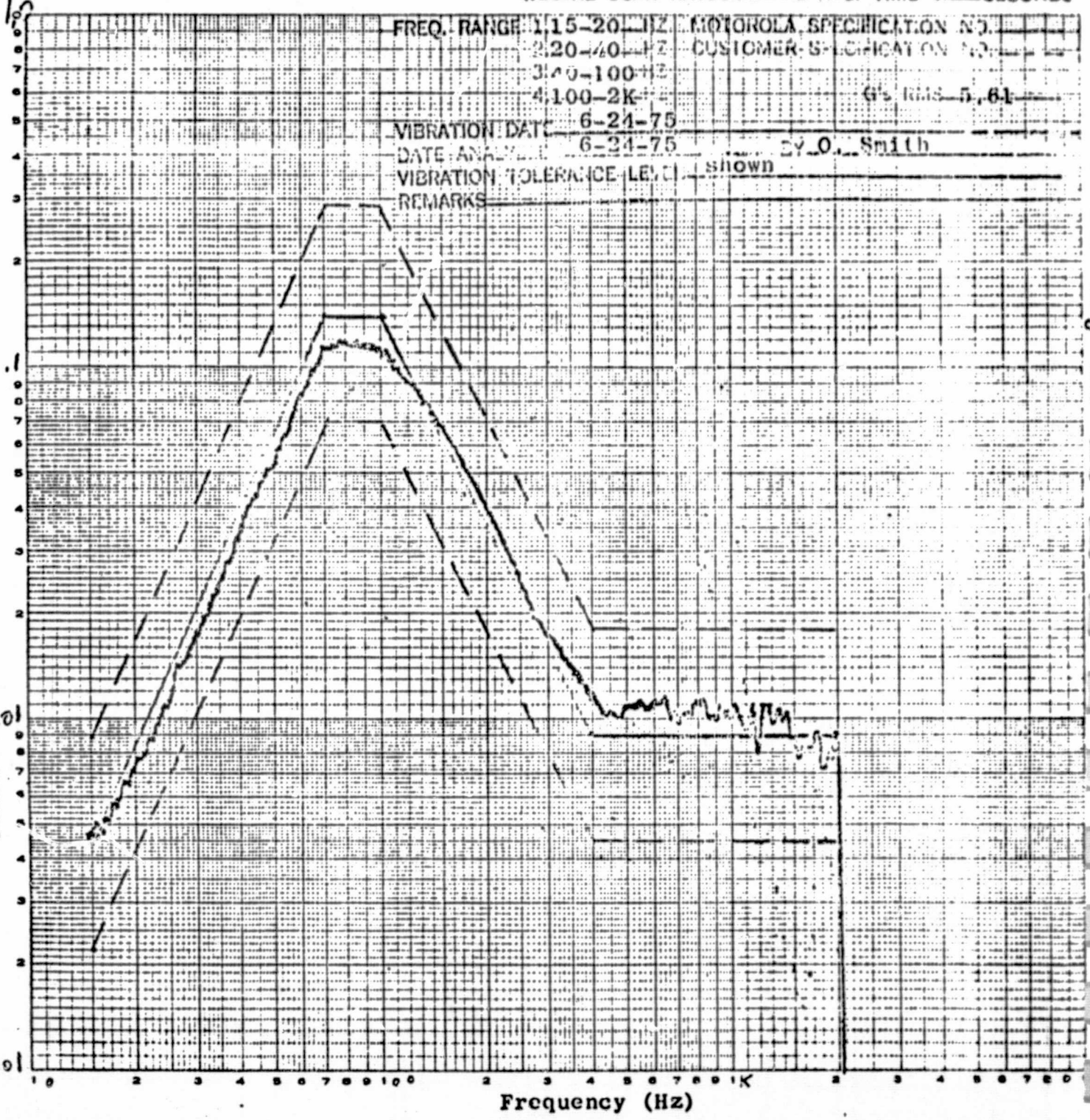
PROJECT 4601-400 UNIT P/W Memory SER. NO. 106

X&Z AXIS SAMPLE (LOOP) TIME 10 SECONDS

FILTER B.W. 1. 5 HZ SCAN RATE 1.125 HZ AVG. TIME 10 SECONDS
2. 10 HZ SCAN RATE 2.25 HZ AVG. TIME 10 SECONDS
3. 20 HZ SCAN RATE 3.5 HZ AVG. TIME 10 SECONDS
4. 50 HZ SCAN RATE 14.25 HZ AVG. TIME 10 SECONDS

FREQ. RANGE 1. 15-20 HZ MOTOROLA SPECIFICATION NO.
2. 20-40 HZ CUSTOMER SPECIFICATION NO.
3. 40-100 HZ
4. 100-2K HZ G's RMS 5.61

VIBRATION DATE 6-24-75
DATE ANALYZED 6-24-75 BY O. Smith
VIBRATION TOLERANCE LEVEL shown
REMARKS



ORIGINAL PAGE IS
OF POOR QUALITY

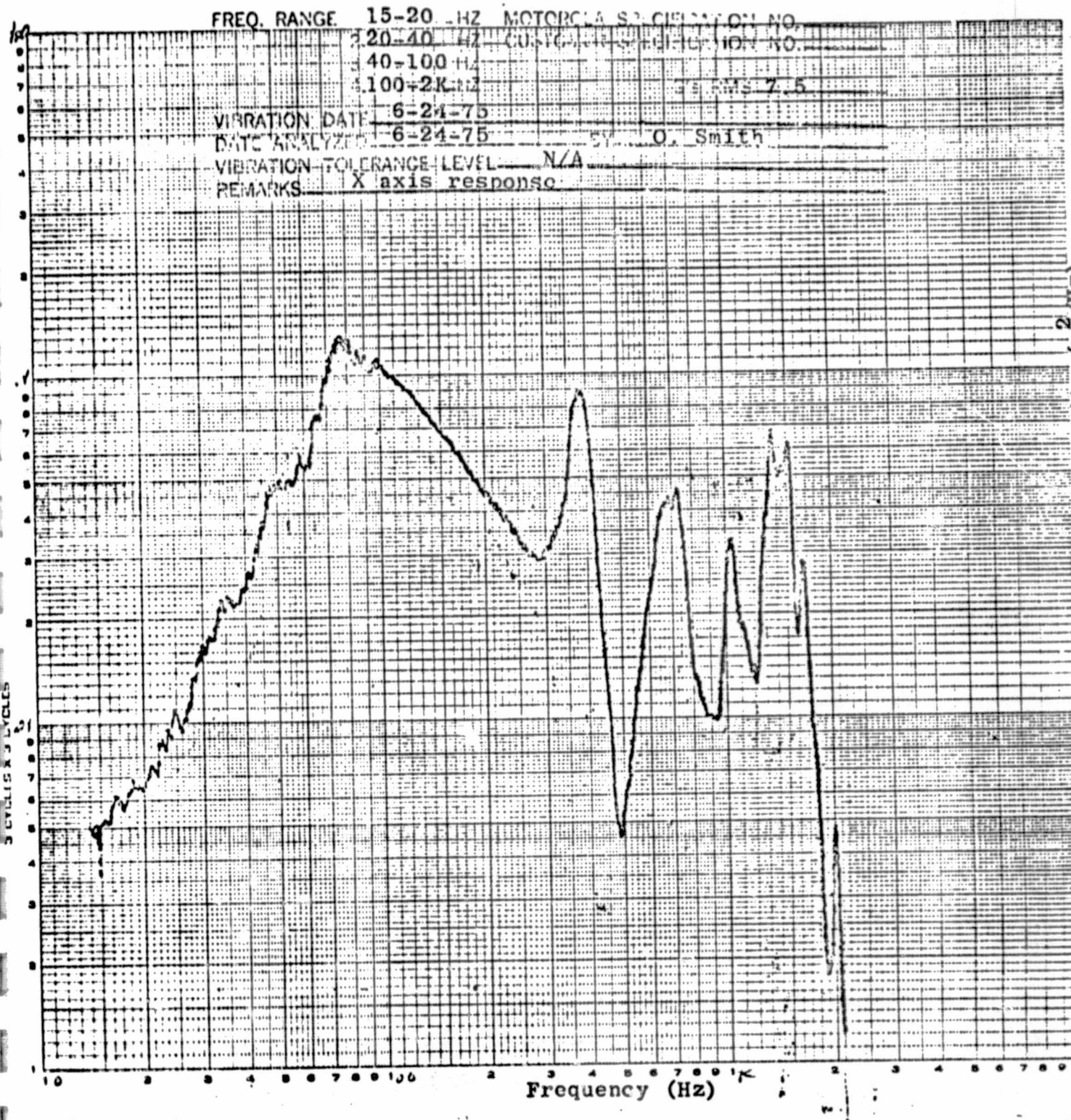
PROJECT 4601-400 UNIT P/W Memory SER. NO. 106

X AXIS SAMPLE (LOOP) TIME 10 SECONDS

FILTER B.W. 1. 5 HZ SCAN RATE 1.125 HZ AVG. TIME 1. 10 SECONDS
2. 10 HZ SCAN RATE 2.25 HZ AVG. TIME 2. 10 SECONDS
3. 20 HZ SCAN RATE 3.5 HZ AVG. TIME 3. 10 SECONDS
4. 50 HZ SCAN RATE 4.25 HZ AVG. TIME 4. 10 SECONDS

FREQ. RANGE 15-20 HZ MOTOROLA SPECIFICATION NO.
20-40 HZ CUSTOMER SPECIFICATION NO.
40-100 HZ
100-2K HZ 7.5 RMS

VIBRATION DATE 6-24-75
DATE ANALYZED 6-24-75 BY O. Smith
VIBRATION TOLERANCE LEVEL N/A
REMARKS X axis response



ORIGINAL PAGE IS
POOR QUALITY

PROJECT 4601-400 UNIT P/W Memory SER. NO. 106

Y AXIS SAMPLE (LOOP) TIME 10 SECONDS

FILTER B.W. 1. 5 HZ SCAN RATE 1.125 HZ AVG. TIME 1. 10 SECONDS
2. 10 HZ SCAN RATE 2.25 HZ AVG. TIME 2. 10 SECONDS
3. 20 HZ SCAN RATE 3.5 HZ AVG. TIME 3. 10 SECONDS
4. 50 HZ SCAN RATE 4.25 HZ AVG. TIME 4. 10 SECONDS

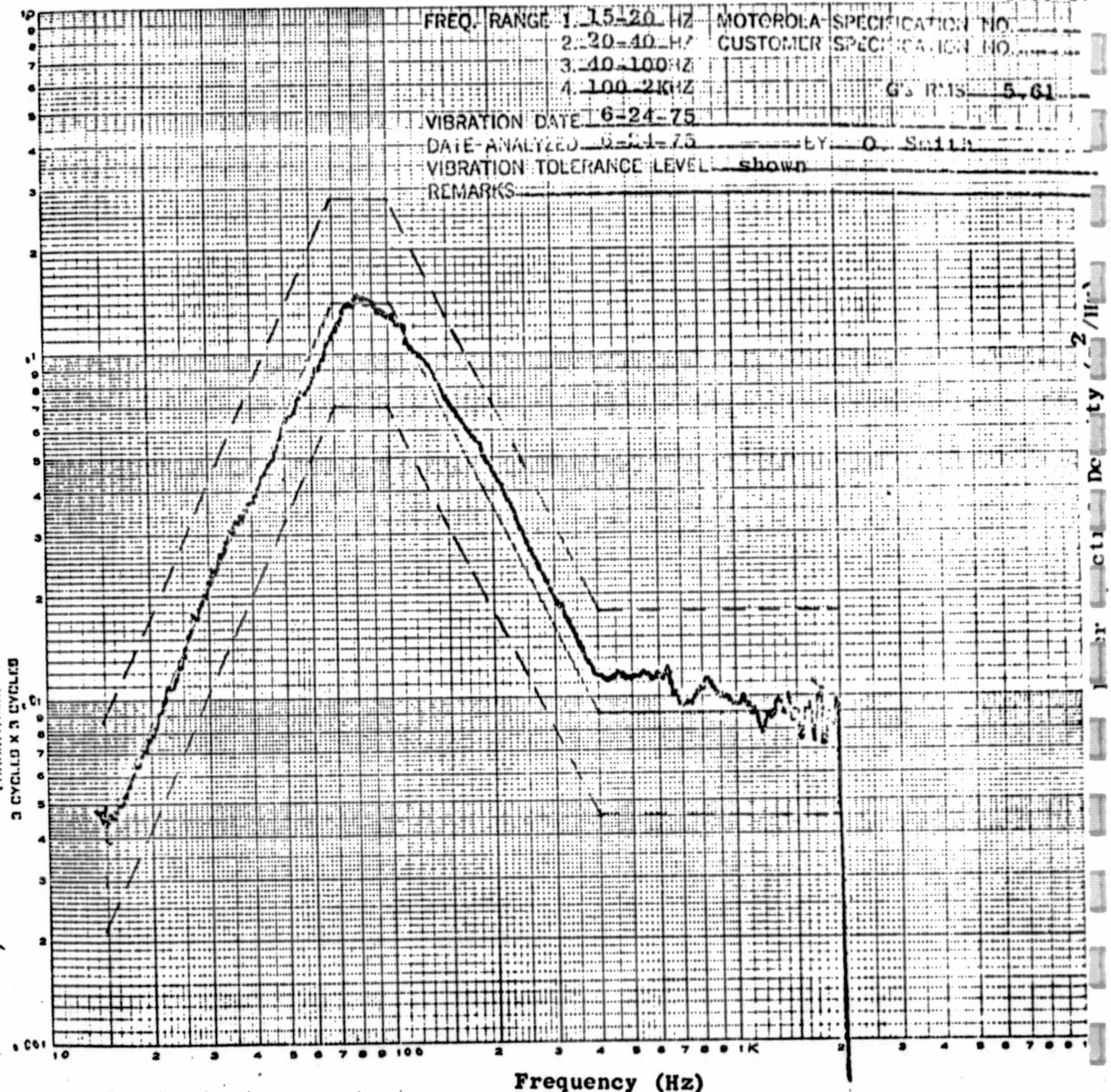
FREQ. RANGE 1. 15-20 HZ MOTOROLA SPECIFICATION NO.
2. 20-40 HZ CUSTOMER SPECIFICATION NO.
3. 40-100 HZ
4. 100-2K HZ G's RMS 5.61

VIBRATION DATE 6-24-75

DATE ANALYZED 6-24-75 BY O. Smith

VIBRATION TOLERANCE LEVEL shown

REMARKS



PROJECT 4601-400 UNIT P/W Memory SER. NO. 106

X&Z AXIS SAMPLE (LOOP) TIME 10 SECONDS

FILTER B.W. 1. 5 HZ SCAN RATE 1.125 HZ AVG. TIME 10 SECONDS
2. 10 HZ SCAN RATE 2.25 HZ AVG. TIME 10 SECONDS
3. 20 HZ SCAN RATE 3.5 HZ AVG. TIME 10 SECONDS
4. 50 HZ SCAN RATE 14.25 HZ AVG. TIME 10 SECONDS

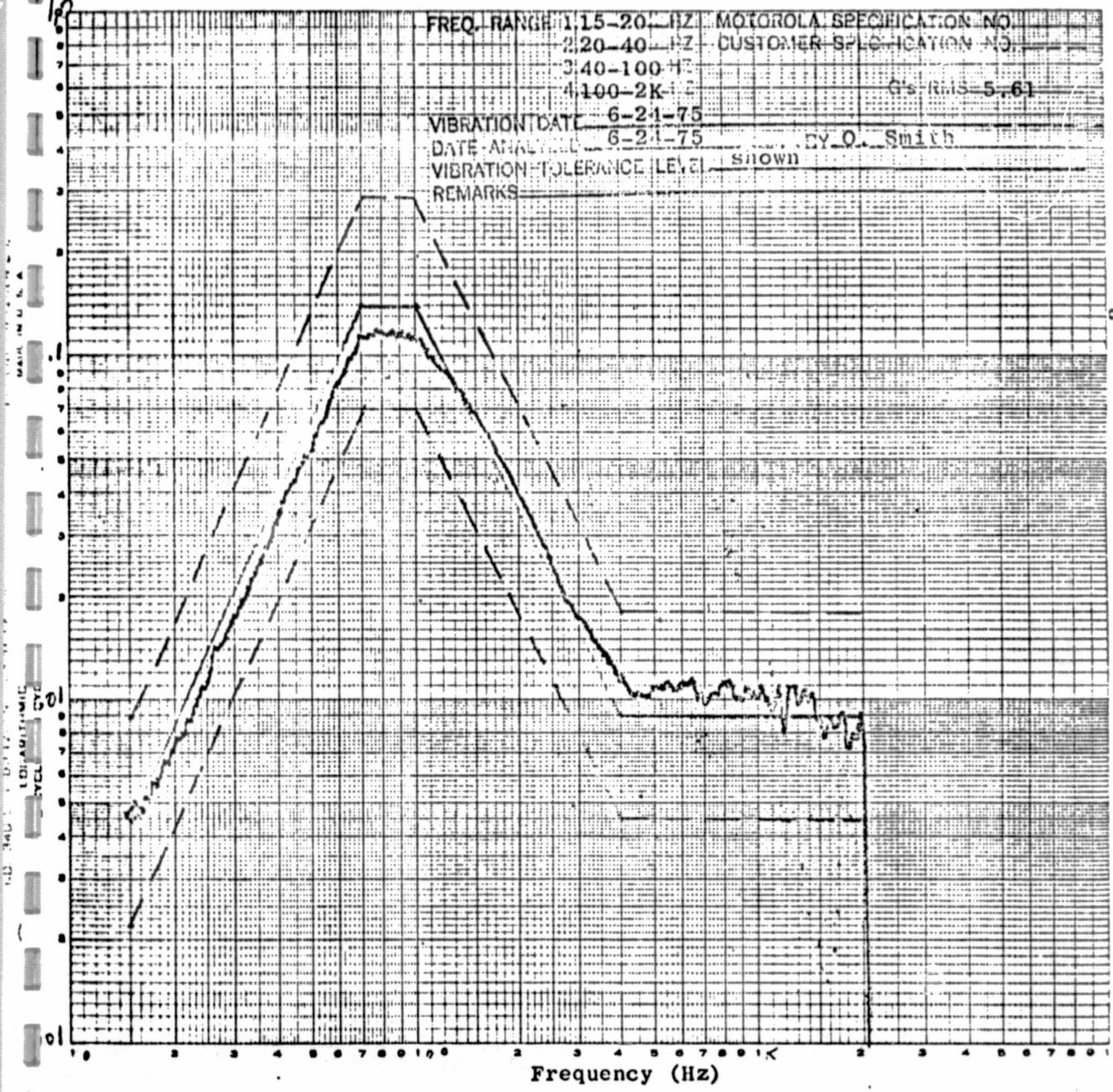
FREQ. RANGE 1. 15-20 HZ MOTOROLA SPECIFICATION NO.
2. 20-40 HZ CUSTOMER SPECIFICATION NO.
3. 40-100 HZ
4. 100-2K HZ G's RMS 5.61

VIBRATION DATE 6-21-75

DATE ANALYZED 6-21-75 BY O. Smith

VIBRATION TOLERANCE LEVEL shown

REMARKS



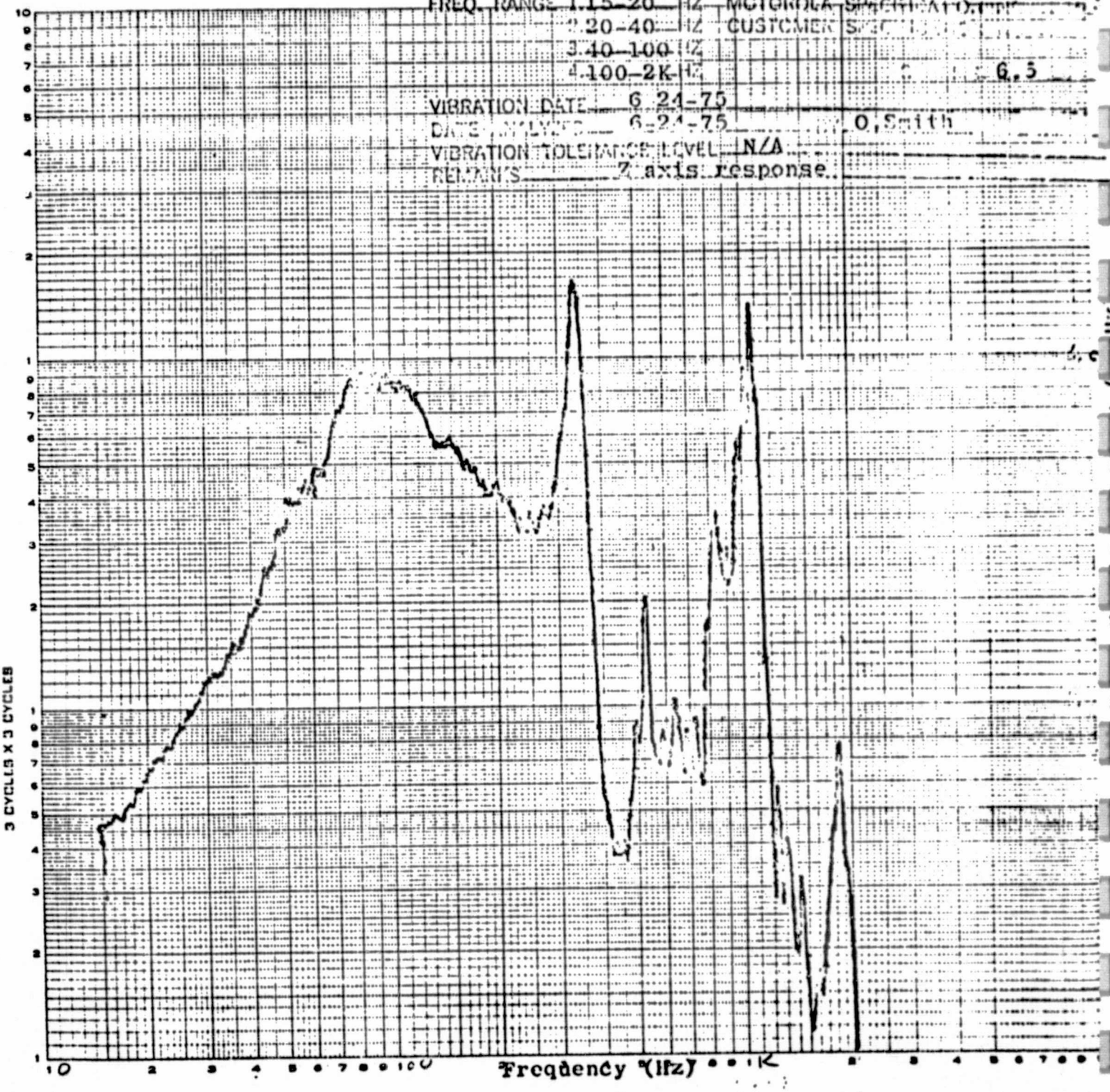
PROJECT 4601-400 UNIT P/W Memory SER. NO. 106

Z AXIS SAMPLE (LOOP) TIME 10 SECONDS

FILTER B.W. 1. 5 HZ SCAN RATE .125 HZ AVG. TIME 1 10 SECONDS
2. 10 HZ SCAN RATE .25 HZ AVG. TIME 2 10
3. 20 HZ SCAN RATE .5 HZ AVG. TIME 3 10
4. 50 HZ SCAN RATE .25 HZ AVG. TIME 4 10

FREQ. RANGE 1. 15-20 HZ MOTOROLA SPECIFICATION
2. 20-40 HZ CUSTOMER SPEC
3. 40-100 HZ
4. 100-2K HZ 6.5

VIBRATION DATE 6-24-75
DATE ANALYZED 6-24-75 O. Smith
VIBRATION TOLERANCE LEVEL N/A
REMARKS Z axis response



3 CYCLES X 3 CYCLES

W.O. 3039

CONTROL 41

HIGH VACUUM TEST

Unit: PLATED WIRE	Project: 4601 - 400	Date: 6-18-75
Model: N/A	Specification: 12-P 13722D	
Serial: 106	Operator: JOE MOLLERE	
Vacuum System No.: 3	Observer: LEE GOULDEN	

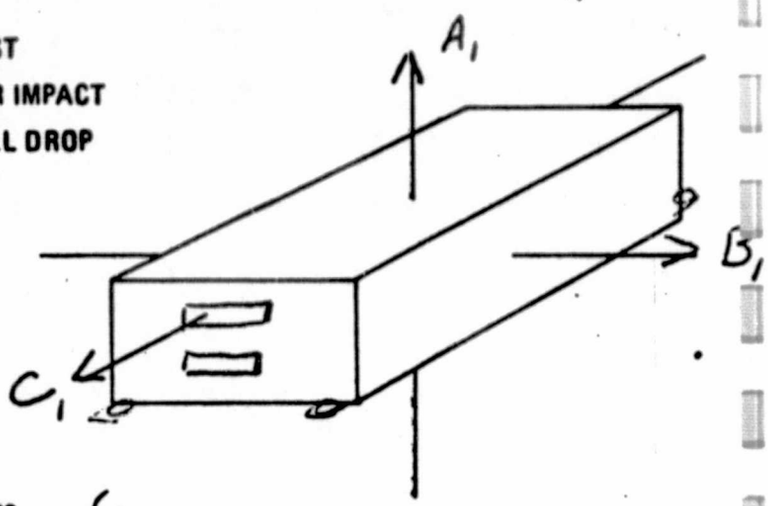
TIME	PRESSURE (mm Hg A)	REMARKS
~~12:32~~	ATM	START TO H. VAC
12:35	700 M	
~~12:45~~	1×10^{-4}	
13:15	38×10^{-5}	
13:45	2.6×10^{-5}	
16:15	1.6×10^{-5}	
14:45	1.2×10^{-5}	
15:10	1×10^{-5}	
15:20	1×10^{-5}	VENT TO ATM.
		END TEST

MOTOROLA INC.
Government Electronics Division

SHOCK TEST (DROP)

PROJECT 4601-400
DATE 18 June 75
SHEET 1 OF 1
W.O. NO. 3040
CONTROL NO. 11
UNIT Plated Wire Memory
SERIAL NO. 106
OPERATOR Pete Martin
OBSERVER Lee Gouldin
VIBRATION MOUNTS NONE
NO. OF DROPS PER ~~FACE~~ AXIS see below TOTAL NO. OF DROPS 6
ACCELERATION 30 G'S
PULSE DURATION 6+12 MS
SPEC DETAILS 12-P13722D as revised by Motorola-Gram from Lee Gouldin dated 6-18-75

TYPE OF TEST
☒ MODULAR IMPACT
☐ FREE FALL DROP



DROP HEIGHT 3/4" + 3 1/2 IN.
PROGRAMMER PRESSURE N/A P.S.I.
TYPE OF WAVESHAPE half sine
BANDPASS FILTER .2 LOW FR. Hz
4300 HIGH FR. Hz

REMARKS
(1) 3 drops at 6 MS and 3 drops at 12 MS
(2) There were 2-6 MS drops on the C_1 axis due to an defective test cable.

PAD AND PLATE CONFIGURATION			
ITEM NO.	PART NO.	DESCRIPTION	
1	MRL 2354	alum plate	T
2	MRL 2795	1" red open	B
3	MRL 2359	alum plate	B
4			
5	1- 8x8x1/8	plastic	
6	2- 8x8x1/8	rubber	
7	3- 8x8x1/16	rubber	
8	3- 1"	blue closed	
9	1- 1"	blue open	

6 MS

AXIS	FACE	1 (6 MS)	2 (6 MS)	3 (12 MS)	4 (12 MS)	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	1	X			X																
	2																				
B	1	X			X																
	2																				
C	1	X	X		X																
	2																				