ELECTRICAL ENGINEERING DEPARTMENT

UNIVERSITY OF TENNESSEE

KNOXVILLE TN 37916

Prepared For

George C. Marshall Space Flight Center
National Aeronautics and Space Administration
Under Contract NAS8-27296/DCN 1-1-40-10230

HIGH-RESOLUTION

WIDTH-MODULATED PULSE REBALANCE ELECTRONICS

FOR STRAPDOWN GYROSCOPES AND ACCELEROMETERS

E. J. Kennedy, T. V. Blalock
W. L. Bryan, and K. Rush

Technical Report TR-EE/EL-2
September 23, 1974

ACKNOWLEDGEMENTS

The authors are grateful for the generous assistance of the staff of the Astrionics Laboratory, MSFC, during the work reported in this paper. The encouragement, advice, and invaluable guidance of Mr. E. H. Berry is especially appreciated. Discussions with and suggestions from Mr. Clyde Jones and Mr. Joe Parker were very helpful. The testing of the rebalance loops at MSFC by Mr. William Kimmons and Mr. Billy Hughes is gratefully acknowledged.

The authors thank Mrs. Beverly Perry for her very skillful preparation of the manuscript.

HIGH RESOLUTION
WIDTH-MODULATED PULSE REBALANCE ELECTRONIC
LOOPS FOR STRAPDOWN GYROSCOPES AND ACCELEROMETERS

ABSTRACT

Three different rebalance electronic loops were designed, implemented, and evaluated. The loops were width-modulated binary types using a 614.4 kHz keying signal. The loops were developed to accommodate the following three inertial sensors with the indicated resolution values: (1) Kearfott 2412 accelerometer - resolution = 260 micro-g/data pulse, (2) Honeywell GG334 Gyroscope - resolution = 3.9 milli-arc-sec/data pulse, (3) Kearfott 2401-009 accelerometer - resolution = 144 milli-g/data pulse.

Design theory, details of the design implementation and experimental results for each loop are presented.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF SYMBOLS

Symbol	Description	Units
ΔA_q	Increment in torque current area	mA-sec/data pulse
B	Elastic restraining torque	dyne-cm/rad
ENV_{sd}	Equivalent noise voltage at synchronous demod. input	volt/$Hz^{1/2}$
ENV_p	Equivalent noise voltage of preamplifier	volt/$Hz^{1/2}$
e_{nc}	Noise voltage at ESP output	volts rms
F	Damping coefficient	dyne-cm-sec/rad
f_i	Interrogation frequency	Hz
f_{cl}	Closed-loop bandwidth	Hz
f_{sg}	Pickoff frequency	Hz
f_z	Frequency of s-domain zero	Hz
f_p	Frequency of s-domain pole	Hz
Δf_{bn}	Noise bandwidth of the bandpass filter	Hz
Δf_n	Noise bandwidth of the G_{dc} block	Hz
G_{dc}	DC amplifier and compensator transfer function	volts dc/volt dc
G_p	Preamplifier gain	volts rms/volt rms
G_b	Bandpass filter gain	volts rms/volt rms
G_a	AC amplifier gain	volts rms/volt rms
G_{sd}	Synchronous demodulator gain	volts dc/volt rms
G_{ct}	Pulse width modulator transfer function	mA/volt dc
G_{pc}	Error signal processor transfer function	volts dc/volt rms

Symbol	Description	Units
G_l	Loop transmission	volts/volt
G_{ac}	Gain of ac section of ESP	volts rms/volt rms
G_m	Gain margin	dB
Δg	Accelerometer data resolution	g/data pulse
H_g	Inertial mass transfer function	rad/dyne-cm
H_{tgp}	Inertial sensor transfer function	rms volts/mA
I	Torque current level	mA
J	Mass moment of inertia	dyne-cm-sec^2/rad
k_p	Pickoff scale factor	rms volts/rad
k_t	Torquer scale factor	dyne-cm/mA
k'_t	Torquer scale factor	deg/mA-sec
k_{dc}	DC amplifier and compensator gain constant	volts dc/volt dc
k_{pc}	Error signal processor gain constant	volts dc/volt rms
k_{oi}	Gyro gain	rad/rad
k_a	Accelerometer scale factor	mA/g
R_r	Ramp slope	volts/sec
R_d	Data rate	pulses/sec
s	Laplace transform variable	rad/sec
T	Torque	dyne-cm
t_i	Interrogation period	sec
ΔT_A	Increment in torque area	dyne-cm-sec
ΔV_{cq}	Data quantization	volts/data pulse
ΔV_{ptcr}	Torque current ripple at pickoff output	volts peak

Symbol	Description	Units
ΔV_{tcr}	Torque current ripple at pickoff output	volts rms
ΔV_{tcro}	Torque current ripple at ESP output	volts rms
V_{sg}	Pickoff excitation	volts rms
V_c	Error signal processor output voltage	volts dc
ε_n	Random noise inaccuracy	rms data pulses
ε_{dc}	DC offset inaccuracy	data pulses
θ	Angle	rad
$\Delta\theta_d$	Gyro data resolution	arc-sec/data pulse
$\Delta\theta_{di}$	Gyro input axis resolution	arc-sec/data pulse
θ_m	Phase margin	degrees
τ_t	Torquer time constant	sec
τ_z	Time constant of s domain zero	sec
τ_p	Time constant of s domain pole	sec

CHAPTER I

INTRODUCTION

The width-modulated pulse rebalance electronics loop developed in the 1972-73 contract period was modified to produce three new high resolution loops for accommodating the Kearfott 2412 and 2401-009 accelerometers, and the Honeywell GG334C gyroscope. The three rebalance loops were implemented in brassboard form and evaluated both at U.T. and MSFC. Four 2412 systems, three 2401-009 systems and one GG334C axis were delivered to MSFC in the period December 1, 1973 to September 23, 1974. Each system consisted of three rebalance loops--one loop for each space axis.

The implementation and evaluation of the new rebalance loops have confirmed the successful realization of the basic design goals which were (1) versatility for accommodating a wide range of inertial sensors with minimum change in loop components, (2) minimization of the required number of power supply voltages, (3) at least a factor-of-two increase in error signal sampling rate, (4) improved performance with special emphasis on the reduction of uncertainties in data output due to all sources of noise, (5) a wide range of available scale factors, (6) reduction of system complexity for improved reliability, and (7) amenability to microcircuit implementation.

Some of the salient new developments resulting from this year's efforts are the following: (1) improved system partitioning for increased reliability and reduction of pickup noise; (2) reduction of the number of power supply voltages to two, a +15V supply and a -15V supply; (3) reduction of the supply current demand of the rebalance electronics; (4) implementation of CMOS logic; (5) design and installation of an automatic overload recovery

circuit for rapid return of the inertial mass to its quiescent position after exposure to an over range rate; (6) development of a new low-power fast comparator for the duty cycle generator; and (7) development of a new H-switch. These new developments will be discussed in detail in other sections of this report.

The general transfer function of the basic sections of width-modulated rebalance loops and the fundamental design considerations are presented in Chapter II. The loop transmission synthesis and the distribution of signal gain for the three specific rebalance loops are given in Chapter III. Chapter IV presents the details of the implementation of each part of the rebalance loop. Some of the more important experimental results are presented and discussed in Chapter V.

CHAPTER II

DESIGN THEORY

The design considerations and formulations necessary for the synthesis of high-resolution width-modulated rebalance electronic loops for strapdown gyroscopes and accelerometers will be presented in this chapter. Some of the design theory presented here was published in last year's report[1] but is repeated for completeness.

The organization of rebalance loops is discussed and the transfer functions of the basic sections are presented. The fundamental considerations in the design of rebalance loops are delineated; these include resolution, sampling constraints, dynamic range, synchronization of loop signals, random noise, gain-bandwidth limitations, transfer function distribution, and accuracy.

Basic Organization of a Width-Modulated Rebalance Loop

The width-modulated rebalance loop has four basic sections as shown in Figure 1. The inertial sensor, gyroscope or accelerometer, has a mass that tends to change position, from a quiescent or null position, under the influence of an external angular rate (gyro) or acceleration (accelerometer). A differential pickoff transducer, excited by a sinusoidal generator, produces an error signal proportional to the motion of the mass. This amplitude modulated error signal is amplified, filtered, demodulated and frequency-domain compensated by the error signal processor. The processed error signal is interrogated by the duty cycle generator to determine the torque current required to return the mass of the inertial sensor to its quiescent position

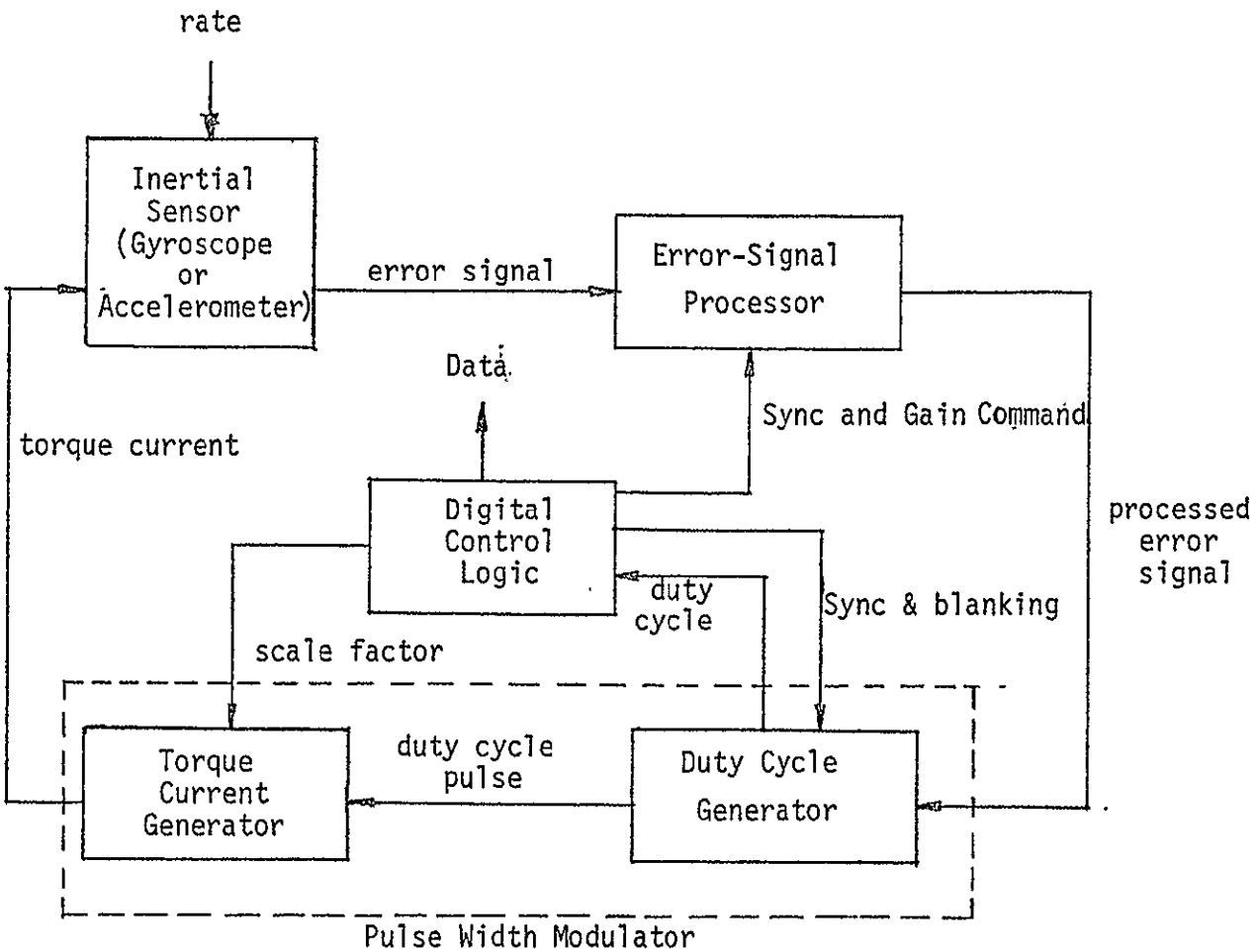


Figure 1. Basic Organization of a Width-Modulated Binary Pulse Rebalance Electronics Loop.

(rebalance the inertial sensor). The duty cycle generator is actually a voltage-to-time converter that transmits a width-modulated pulse to the torque current generator to properly proportion the positive and negative lobes of the square wave of torque current fed to the inertial sensor.

The digital control electronics (DCE) generates the timing and control signals for the proper operation of the loop. The DCE time reference is a highly stable crystal controlled electronic clock. The DCE transmits synchronizing and blanking signals to the duty cycle generator to determine the rate at which the processed error signal is sampled and to set the minimum positive and negative torque currents. The torquing status information is contained in the duty cycle pulse which the DCE uses to generate digital data pulses. The data pulses give a precise measure of the restoring torque applied to the movable mass in the inertial sensor. Knowledge of the restoring torque can then be directly translated into motion experienced by the vehicle to which the inertial sensor is strapped.

By examination of the duty cycle, the DCE may also determine the adequacy of the torque current level for the torquing requirements of the inertial sensor. If the torque level is inadequate, the DCE commands a current level change (scale factor change) in the torque current generator and a change in gain in the error signal processor to maintain constant loop transmission. Some rebalance loops may not require provision for scale factor change in the DCE.

General Transfer Functions of the Basic Sections

The basic elements of the U.T. rebalance electronic loop is shown in Figure 2. The general transfer functions of the three basic sections of the loop are developed in the following material.

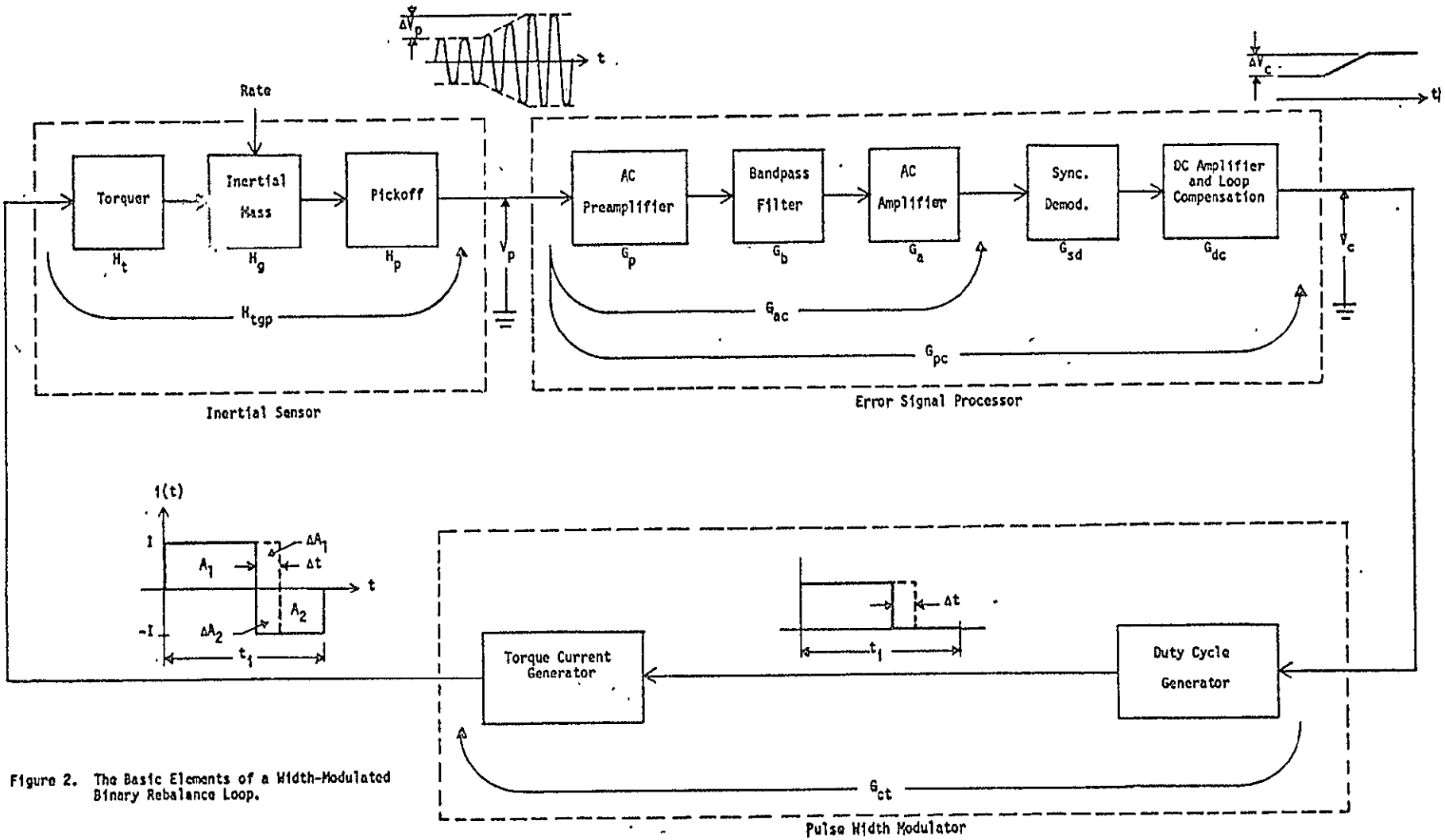


Figure 2. The Basic Elements of a Width-Modulated Binary Rebalance Loop.

Inertial Sensor Transfer Function. The differential equation relating angular motion θ of the inertial mass to the applied torque T is

$$T(t) = J \frac{d^2\theta}{dt^2} + F \frac{d\theta}{dt} + B\,\theta \ , \qquad (1)$$

where J (dyne-cm-sec^2/rad) is the mass moment of inertia, F (dyne-cm-sec/rad) is the damping coefficient, and B (dyne-cm/rad) is the elastic restraining torque. The Laplace transformed version of Equation (1) leads immediately to the transfer function for the inertial mass:

$$H_g = \frac{\theta(s)}{T(s)} = \frac{1}{Js^2 + Fs + B} \quad \text{(rad./dyne-cm)} \qquad (2)$$

The pickoff response time is so short relative to the other time-constants in the system that the transfer can be written simply as

$$H_p = k_p \ \text{(rms volts/rad)} \qquad (3)$$

The torquer transfer can be approximated by a simple low-pass network with a time-constant τ_t which is usually sufficiently short to be negligible relative to other system time-constants:

$$H_t = \frac{k_t}{1 + \tau_t s} \qquad \text{(dyne-cm/mA)} \qquad (4)$$

The torquer scale factor k_t is usually given in its fundamental units of dyne-cm/mA for accelerometers but is often expressed in units of deg/mA-sec for gyroscopes. This gyroscope scale factor k_t' must be multiplied by the damping factor F and the factor $\frac{2\pi}{360}$ to obtain the fundamental scale factor k_t.

That is

$$k_t = k_t' \, F \, \frac{2\pi}{360} \quad \text{(dyne-cm/mA)} \quad . \tag{5}$$

The scale factor k_t' can be obtained by feeding the gyro torquer with a step of current $I_{dc}\, U(t)$ and measuring the float angular velocity $d\theta/dt$ in a time interval after the current turn-on transients have become negligible and before the elastic restraining torque has become significant. In this time interval the torque applied to the gyro float is equal to the second term in the right side of Equation (1); that is, $T(t) = F\, d\theta/dt = k_t\, I_{dc}$.

The overall transfer function for the inertial sensor is

$$H_{tgp} = \frac{k_t\, k_p}{(Js^2 + Fs + B)(1 + \tau_t\, s)} \quad \text{(rms volts/mA)}. \tag{6}$$

For a specific inertial sensor in a specific rebalance loop, the transfer H_{tgp} can often be simplified; however, this simplification can only be accomplished when the design specifications and sensor parameters for the specific system have been determined.

Signal Processor Transfer Function. The error signal processor block of Figure 2 is designed with the dominant time-constants in the dc amplifier and loop compensator section. Thus, in general

$$G_{dc} = \frac{k_{dc}\,(1 + s\,\tau_{z1})(- - - - -)(1 + s\,\tau_{zi})}{(1 + s\,\tau_{p1})(- - - - -)(1 + s\,\tau_{pj})}\,, \tag{7}$$

and if $k_{pc} = G_p\, G_b\, G_a\, G_{sd}\, k_{dc}$, then (Figure 2)

$$G_{pc} = k_{pc} \frac{\sum_{n=1}^{i} (1 + s\,\tau_{zn})}{\sum_{m=1}^{j} (1 + s\,\tau_{pm})} \quad . \tag{8}$$

In all the rebalance loops designed to this time, one zero and at the most three poles have been sufficient for proper shaping of the loop transfer function. Hence, usually

$$G_{pc} = k_{pc} \frac{(1 + s\,\tau_z)}{(1 + s\,\tau_{p1})(1 + s\,\tau_{p2})(1 + s\,\tau_{p3})} \quad . \tag{9}$$

The gain constant k_{pc} is a real number and is the ratio given by (see Figure 2)

$$k_{pc} = \frac{\Delta V_c}{\Delta V_p/\sqrt{2}} \quad \frac{\text{volts dc}}{\text{volts rms}} \quad . \tag{10}$$

Pulse Width Modulator Transfer Function. The principle of operation of the duty cycle generator (DCG) of Figure 2 is illustrated in Figure 3. The DCG detects the time when a standard ramp signal of slope R volts/sec crosses the processed error signal. Thus a change ΔV_c volts in the error signal is converted into a change Δt seconds which is transmitted via a duty cycle pulse to the torque current generator. The ratio of positive torque current area to negative current area is therefore changed as indicated in Figure 2. The conversion process is very fast relative to other response times in the rebalance loop so that G_{ct} (Figure 2) is a real number. The transfer G_{ct} is given by[1]

$$G_{ct} = \frac{2I}{Rt_i} \text{ (mA/volt dc)} \quad . \tag{11}$$

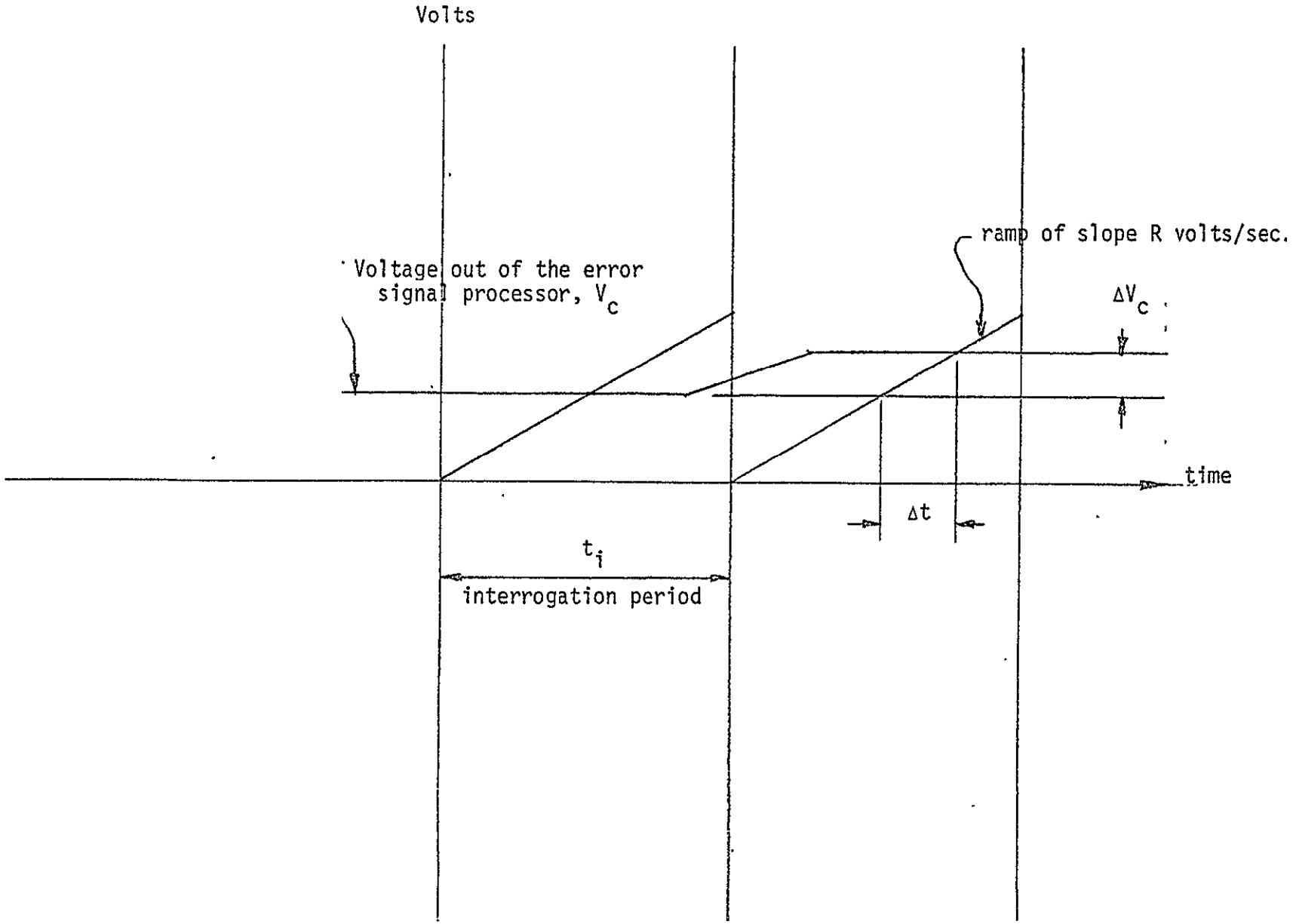


Figure 3. Voltage-to-Time Conversion.

where I is the torque current magnitude in mA, R is the ramp slope in volts/sec., and t_i is the interrogation period in seconds.

Loop Transmission of the Entire Loop. The loop transmission is $G_l = H_{tgp}\, G_{pc}\, G_{ct}$ or

$$G_l = \frac{2k_t k_p k_{pc} I}{Rt_i} \frac{(1 + s\,\tau_z)}{(Js^2 + Fs + B)(1 + \tau_t s)(1 + \tau_{p1} s)(1 + \tau_{p2} s)(1 + \tau_{p3} s)} . \quad (12)$$

The first step in the development of a specific rebalance loop for either a gyroscope or an accelerometer is to synthesize the loop transmission G_l to satisfy loop stability requirements and also the other important design considerations to be discussed in the next section of this chapter.

Fundamental Considerations in the Design of Rebalance Loops

Data Resolution. The synchronization signals fed to the duty cycle generator from the DCE forces the torque current pulse to change width only in discrete increments. The interrogation frequency f_i and the data pulse rate R_d are controlled by the same clock so that the data pulse rate is an integral multiple of f_i. The smallest increment in torque current pulse width is equal to the width of a single data pulse; thus, the torque current resolution is (see Figure 2)

$$\Delta A_q = \frac{2I}{R_d} \quad \text{(mA-sec/data pulse)} . \quad (13)$$

The corresponding increment in torque area applied to the inertial mass is

$$\Delta T_A = k_t \Delta A_q = \frac{2k_t I}{R_d} \quad \text{(dyne-cm-sec)} . \quad (14)$$

But at steady state,

$$\Delta T = F \frac{\Delta\theta}{\Delta t} \quad ,$$

$$\Delta\theta = \frac{1}{F} \Delta T \, \Delta t = \frac{\Delta T_A}{F} \quad .$$

Thus, the data resolution of the system is

$$\Delta\theta_d = \frac{2 \, k_t I}{F \, R_d} \quad \text{(rad/data pulse).} \tag{15}$$

Usually the data resolution is best expressed in arc-secs:

$$\Delta\theta_d = \frac{2 \, k_t I}{F \, R_d} \left(\frac{360}{2\pi}\right) (3600)$$

$$\Delta\theta_d = \frac{7200 \, I}{R_d} \left[\frac{360}{2\pi F} \, k_t\right] \text{, (arc-sec/data pulse) .} \tag{16}$$

where I is in mA, k_t in dyne-cm/mA, R_d in data pulses/sec, and F in dyne-cm-sec./rad. Note that the term in brackets is the torquer scale factor k_t' (degree/mA-sec) usually given for gyroscopes. The angular increment $\Delta\theta_d$ of Equation (16) is the angular motion of the inertial mass due to a one data pulse weight of torque-current area.

For a gyroscope, $\Delta\theta_d$ is the angular increment per data pulse experienced by the float; it is the gyro output axis resolution. The resolution referred to the input axis is given by

$$\Delta\theta_{di} = \frac{\Delta \, \theta_d}{k_{oi}} \quad , \tag{17}$$

where k_{oi} is the ratio of gyro output axis angular motion to input axis angular motion.

The data resolution of an accelerometer is determined from the accelerometer scale factor k_a (mA/g) which is the torquer average current necessary to hold the inertial mass at its quiescent position when the sensitive axis of the accelerometer is in an acceleration field of one g. The average torquer current caused by a single data pulse increment per interrogation period is

$$I_{av} = \Delta A_q \, f_i \quad \text{(mA/data pulse)} . \tag{18}$$

This current corresponds to an acceleration increment of

$$\Delta g = \frac{I_{av}}{k_a} ,$$

$$\Delta g = \frac{2I \, f_i}{k_a \, R_d} \quad \text{(g's/data pulse)} . \tag{19}$$

which is the appropriate data resolution for the accelerometer.

Data Quantization - Dead Band Voltage Increment. The data quantization in volts per data pulse at the input to the duty cycle generator is determined by the ramp rate R volts/sec and the data rate R_d pulses/sec.[1] The total number of data pulses in one interrogation period is $R_d \, t_i$ pulses. The total voltage excursion of the ramp signal in one interrogation period is $R \, t_i$ volts. Therefore, the voltage quantization at the duty cycle generator input is

$$\Delta V_{cq} = \frac{R \, t_i}{R_d \, t_i} = \frac{R}{R_d} \quad \text{(volts/data pulse)}. \tag{20}$$

The voltage increment ΔV_{cq} is also the system deadband. In most of our rebalance loop designs, the noise voltage at the duty cycle generator is comparable to ΔV_{cq} so that the noise voltage behaves as a dither signal and thus keeps the processed error signal sufficiently out of the deadband to eliminate possible control-loop limit-cycling.

Knowledge of the quantity ΔV_{cq} is necessary to evaluate the effects of uncertainties such as noise. These uncertainties are usually determined at the input to the duty cycle generator where they can immediately be translated into a data pulse uncertainty by comparison with ΔV_{cq}.

Sampling Constraints. There are two major sampling constraints that must be considered in designing a width-modulated rebalance loop: the Sampling Theorem and the ramp slope constraint.

The maximum allowable closed-loop bandwidth is limited by the rate at which the processed error signal is sampled. The sampling frequency is just the interrogation frequency f_i. Since the highest frequency that can occur in the error signal is approximately equal to the 3 dB bandwidth of the closed-loop system, then the sampling theorem requires that

$$f_{cl} < \frac{f_i}{2} . \tag{21}$$

The constraint imposed by Equation (21) is easy to satisfy if f_i is high. The systems we have so far developed use f_i = 2.4 kHz. Since typical inertial sensor loops have f_{cl} < 100 Hz, the Equation (21) constraint is easily satisfied in most cases.

For proper operation of the duty cycle generator, the slope of the internal ramp signal that is mixed with the processed error signal V_c (Figure 3)

must be greater than the maximum possible slope of the error signal, otherwise the ramp signal may not cross the processed error signal or may cross more than once in a single interrogation period. To ensure only one crossing per interrogation period,

$$R > \left.\frac{dV_c}{dt}\right|_{max.} \quad . \tag{22}$$

The slope of the error signal is controlled primarily by inertial sensor dynamics. For maximum torque rate at a torque current of value IU(t), the maximum voltage $V_c(t)$ is given by

$$V_c(t)\Big|_{max} = k_{pc} \int_0^t \frac{k_t\, k_p\, I\, dt}{F} \quad , \tag{23}$$

$$\left.\frac{dV_c(t)}{dt}\right|_{max} = \frac{k_{pc}\, k_t\, k_p\, I}{F} \quad . \tag{24}$$

Equation (24) gives the worse case slope (maximum slope) since only the inertial sensor integrating time-constant is assumed to be limiting the slope and also it is assumed that I is being applied continuously. However, we will insist for any specific gyro that

$$R > \frac{k_{pc}\, k_t\, k_p\, I}{F} \qquad \text{(volts/sec.)} \quad , \tag{25}$$

where I is in mA.

The design inequality (25) leads to some interesting constraints on the magnitude of the loop transmission at low frequencies and on the maximum system bandwidth. The magnitude of the loop transmission in the low frequency range where the loop transmission is controlled by the inertial sensor damping coefficient F is from Equation (12)

$$\left|G_1\right|_{\text{low freq.}} = \frac{2\, k_t\, k_p\, k_{pc}\, I}{R t_i}\ \frac{1}{\omega_1 F} \quad . \tag{26}$$

In this low frequency range, ω_1, the magnitude of the loop transmission has a slope of -6 dB/octave. The design inequality (25) then requires that

$$\left|G_1\right|_{\text{low freq.}} < \frac{2}{\omega_1 t_i}$$

$$\left|G_1\right|_{\text{low freq.}} < \frac{f_i}{\pi f_1} \tag{27}$$

The ramp slope constraint (22) is therefore satisfied if inequality (27) is satisfied.

If the high frequency region of the loop transmission has a slope of -6dB/octave or greater, then the maximum possible closed-loop bandwidth of the rebalance loop as constrained by the ramp slope is

$$f_{c1}\Big|_{\max} = \frac{f_i}{\pi} = \frac{\text{interrogation frequency}}{\pi} \quad . \tag{28}$$

Comparison of inequality (21) and Equation (28) show that Equation (28) is the controlling sampling constraint; that is, if (28) is satisfied, then (21) is also satisfied.

Dynamic Range Consuming Signals in the Error Signal Processor. Signal saturation at the output of any section of the error signal processor can seriously degrade the performance of a rebalance loop by greatly reducing the loop gain and/or producing excessive phase shift. Excessive phase shift is especially important because it can lead to reversal of the error signal polarity with a consequent latchup of the loop in a positive feedback mode. Signals that consume dynamic range are torque current ripple, the pickoff quadrature signal, signals produced by over-range operation of the inertial sensor, and noise.

The torque-current square-wave is essentially integrated by the inertial sensor; however, a significant torque current ripple may still amplitude modulate the pickoff signal. The maximum torque current ripple (Figure 4) at the pickoff output occurs when $\alpha = \frac{1}{2}$ and H_{tgp} is approximated by $k_t k_p/Fs$. Under these conditions,

$$\Delta V_{ptcr} = \int_0^{\frac{t_i}{2}} \frac{k_t\, k_p\, I\, dt}{F} \quad . \tag{29}$$

The ripple signal at any point in the error signal processor (ESP) can be easily estimated if the ripple is approximated by a sinusoid of peak-to-peak value ΔV_{ptcr}. The rms voltage level of the sinusoid at the output of the inertial sensor then becomes

$$\Delta V_{tcr} = \frac{k_t\, k_p\, I}{4\sqrt{2}\, f_i F} \text{ (rms volts)} \quad . \tag{30}$$

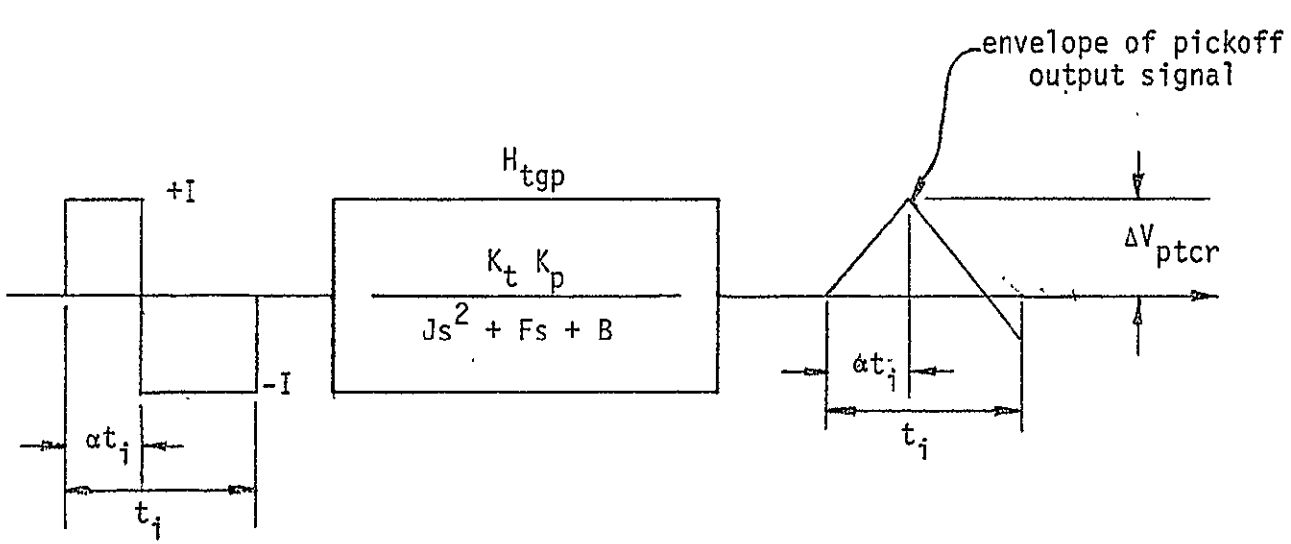


Figure 4. Torque Current Ripple.

The rms value of the torque current ripple at any point in the ESP can be found approximately by multiplying ΔV_{tcr} by the magnitude of the frequency-domain transfer function between the point and the inertial sensor output. The magnitude of the transfer function is computed at a frequency f_i. For example, at the output of the error signal processor the ripple is

$$\Delta V_{tcro} = \Delta V_{tcr} \left| G_{pc}(f_i) \right| . \tag{31}$$

When the inertial mass moves through its null position, the pickoff signal passes through a minimum amplitude and shifts 180° in phase. If the minimum amplitude is greater than zero, the null pick-off signal is forced by the synchronous demodulator to have a phase shift of near 90° relative to the normal pickoff signal which is either in phase or 180° out of phase with the synchronous demodulator drive signal depending on which side of null the inertial mass is positioned. This residual signal at null is termed the quadrature signal and consumes dynamic range in the ESP. The magnitude of the quadrature signal is of great significance in high-gain error-signal processors; it can cause saturation of sections preceding the dc amplifier and loop compensator (Figure 2). The quadrature signal may constrain the distribution of gain between the G_{ac} G_{sd} block and the G_{dc} block in the ESP (Figure 2). For a specific inertial sensor it may be necessary to experimentally reduce the quadrature signal with some network between the pickoff output and the ESP input. In all systems, the quadrature signal effects must be experimentally evaluated since accurate analytical prediction from typical inertial sensor specifications is essentially impossible.

If the inertial sensor experiences a rate environment that is outside the range where the rebalance loop can maintain the inertial mass in its null position, the loop will lose control and the inertial mass will move to one of the two stop positions. At the stop position, the pickoff output signal amplitude is typically many orders of magnitude above the normal operating level. For this condition, several sections of the ESP will usually be in hard saturation. The error signal phase shift associated with this saturation must be controlled to prevent loop latchup. The control is accomplished by properly distributing the ESP transfer function and by using special overload circuits developed for specific rebalance loops. The effects of overrange saturation must be experimentally evaluated in any specific loop.

In some cases, the deleterious effects can be alleviated by a special overload recovery circuit that detects saturation in the G_{dc} block of Figure 2 and commands a high torque current from the torque current generator to keep the inertial mass near the null position. The implementation and performance of this overload circuit will be discussed in later sections of this report.

Two kinds of noise that can use significant dynamic range in the ESP are random noise and extraneous noise (pick-up noise). Random noise levels are usually sufficiently low to be negligible; however, very low frequency high-amplitude noise in a high-gain G_{dc} block may occasionally be significant. Usually, the random noise effect on data pulse uncertainty is much more important than its effect on dynamic range.

The extraneous noise introduced into the ESP through the input, ground lines and/or power lines can be very serious. Extraneous noise signals are usually generated in the system logic section (DCE) and are therefore digital noises that in most cases are synchronized with the data train. Even spin

motor pick-up signals are also usually synchronized. The synchronized extraneous noise, while not contributing to data pulse uncertainty, can consume dynamic range. They are diminished by high common-mode rejection in the ac preamplifier, careful layout and power line filtering in the ESP, and digital signal path control in the DCE. Unsynchronized extraneous noise must be reduced by shielding and power line control; such noise fortunately has negligible effect on dynamic range in most cases.

Synchronization of Rebalance Loop Signals. The expression (12) for the loop transmission of the rebalance electronics loop shows that the magnitude of the loop transmission $|G_1|$ is inversely proportional to the ramp slope R volts/sec. A change in the ramp slope then is reflected as a change in $|G_1|$. Extraneous noise signals that are superposed on the output of the ESP and are also synchronized with the interrogation frequency, f_i, have the same effect on system performance as ramp slope changes during one interrogation period. The equivalent ramp slope changes would always occur at the same times relative to the beginning time of any single interrogation period. Therefore, these synchronized noise signals merely cause a variation of effective loop gain over an interrogation period and consequently have only an indirect and usually a very small effect on system accuracy. It is thus advantageous to synchronize with f_i all system signals which may appear as extraneous signals in the ESP.

In our rebalance loop, all logic signals are synchronized by being traceable to a single, stable digital clock. The interrogation frequency, the data pulse frequency, and the signal generator frequency, are all derived from the clock and are thus synchronized. Whenever possible, gyroscope spin motor power supplies and inertial sensor temperature controllers should also be synchronized with the clock. The torque current is allowed to switch only

with a keying signal derived from the clock so that the torque current ripple is synchronized also.

Even with synchronization, it remains desirable to maintain extraneous noise levels small to avoid dynamic range loss and significant excursions in $|G_1|$.

Random Noise. The dominant source of random noise at the ESP output is usually generated in the ac preamplifier and its associated input circuit including the inertial sensor pick-off network. Good design practice requires the preamplifier gain to be sufficiently high to cause it to be the major source of random noise. A preamplifier gain of 10 is adequate in most cases to cause preamplifier control of random noise. Random noise at the torquer input (perhaps from the torque current generator) is usually negligible at the pick-off output because of the integration by the inertial sensor.

The random noise generated in the ac preamplifier is amplified and filtered by the G_{ac} block of Figure 2. At the input to the synchronous demodulator, the random noise-power selected by the bandpass filter resides in a bandwidth Δf_b centered at the signal generator frequency f_{sg}. The frequency f_{sg} is usually sufficiently high and the bandwidth Δf_b sufficiently narrow to select only a section of the white noise power spectrum of the preamplifier. Thus, the power spectral density near f_{sg} at the input to the synchronous demodulator is approximately

$$(ENV_{sd})^2 = (ENV_p)^2 \, (G_{ac})^2 \quad volt^2/Hz \, , \tag{32}$$

where ENV_p is the equivalent noise voltage of the preamplifier in the white noise region. The noise power is contained in Δf_{bn} which is the noise bandwidth of the bandpass filter.

The exact calculation of the noise power spectrum at the synchronous demodulator output is quite difficult and cumbersome because of the rectification process. However, a reasonable estimate of the output spectrum can easily be computed by noting that the part of the power spectrum that is shifted to lower frequencies by the synchronous demodulator is of primary interest because of the low pass nature of the dc amplifier and compensator block. We will therefore make the pessimistic assumption that all the noise spectrum of Equation (32) is shifted to low frequencies, is white, and extends from f = 0 to f = Δf_{bn}. Then the noise power spectral density at the output of the synchronous demodulator is given by

$$(ENV_{dc})^2 = (ENV_{sd})^2 \ (G_{sd})^2 \tag{33}$$

The noise bandwidth Δf_n of the G_{dc} block (Figure 2) is much less than Δf_{bn} and extends from f = 0 to f = Δf_n. Therefore, the estimate of the rms noise voltage at the output of the ESP is

$$e_{nc} = \sqrt{\overline{\Delta V_{cn}^2}} = \sqrt{(ENV_p)^2 \ (k_{pc})^2 \ \Delta f_n} \qquad \text{(rms volts)} \ . \tag{34}$$

The rms noise voltage e_{nc} should produce less than one data pulse uncertainty. The corresponding constraint on the white equivalent-noise-voltage spectral-density of the preamplifier then becomes from Equations (20) and (34)

$$ENV_p < \frac{R \times 10^9}{R_d \ k_{pc} \ (\Delta f_n)^{1/2}} \ (nV/Hz^{1/2}). \tag{35}$$

Gain-Bandwidth Considerations. The gain and bandwidth of the closed loop system is strongly influenced by accuracy requirements and loop oscillation stability. When the loop transmission is synthesized on a Bode diagram, the G_{pc} (Figure 2) transfer must also be simultaneously considered because of random noise and dc offsets in the G_{dc} block. The low-frequency value of the loop transmission magnitude must be chosen high enough to insure negligible hang-off of the inertial mass from the quiescent position, and to insure that gain drifts due to aging or ambient changes will have negligible effect on accuracy.

Speed-of-response requirements will, of course, influence the choice of closed loop bandwidth for the rebalance loop; however, oscillation stability constraints and the need to limit bandwidth to discriminate against both random and extraneous noise are often the controlling requirements. For example, high resolution and high accuracy systems generally require high values of k_{pc} which lead to high values of noise spectral density at the ESP output. Limiting the rms noise voltage at the ESP output in these cases may constrain the bandwidth of G_{dc} and consequently the bandwidth of the closed loop to be small.

When synthesizing the loop transmission, the usual design goal is to maximize gain-bandwidth product while maintaining both adequate margin against loop oscillations and acceptable accuracy.

Transfer Function Distribution. The first step in the design of a rebalance loop for a specific inertial sensor is the synthesis of the system loop transmission on a Bode diagram. The next step is the proper distribution of the elements of the loop transmission around the loop to satisfy all the design constraints.

The required data resolution is set by the data pulse rate, R_d, the inertial sensor parameters, and the torque current level, I, [See Equations (16) and (19)]. Usually, R_d is made as high as compatibility with DCE and telemetry devices will allow. Thus, for a specific inertial sensor and a given data rate, the resolution requirement fixes I and consequently G_{ct}. Other design constraints must then be addressed by the proper choice and distribution of the ESP transfer function.

High gain in the G_{ac} G_{sd} block of Figure 2 is desirable to minimize low frequency random noise and dc offsets. However, a high quadrature signal, as mentioned earlier, may limit the allowable G_{ac} G_{sd} gain. Furthermore, a complex pole-zero constellation required for loop transmission shaping in the G_{dc} block may influence the gain of that block since, in general, it is easier to realize several poles and/or zeros in a high gain situation. The distribution of gain between the G_{ac} G_{sd} and G_{dc} blocks is also influenced by the type of dynamic-range consuming signals present.

Noise and over-range operation of the inertial sensor are the major influences on gain selection for G_p and G_b. The product G_pG_b is normally chosen sufficiently high to cause preamplifier control of random noise. The preamplifier gain must be low enough to prevent saturation under any condition because of the poor phase shift performance of presently available high CMRR preamplifiers that are suitable for use in rebalance loops. Some saturation is allowable in the bandpass filter; actually this may be desirable since the G_b block can be designed to produce leading phase shift in saturation to compensate for the usual lagging phase shifts in other sections of the ESP.

The ac amplifier, G_a, (Figure 2) is placed between the bandpass filter and the synchronous demodulator because special overload circuits can be

included in it to prevent overloading the demodulator. These overload circuits can limit phase shift to less than 30° even in hard saturation.

Another method of loop gain adjustment is to vary the signal generator drive. For high G_{ct} used with high gain inertial sensors, the required value of k_{pc} may be too low for efficient realization. In this case, where random noise is not usually a problem, the signal generator drive may be advantageously lowered to allow raising k_{pc}.

Accuracy. In this section we will consider the influence of the rebalance electronics on accuracy; that is, we will assume that the inertial sensor is perfect.

Random noise [see Equation (34)] that appears at the output of the ESP produces an inaccuracy that can conveniently be expressed in rms data pulses through the use of the voltage quantization Equation (20). That is

$$\varepsilon_n = \frac{e_{nc}}{\Delta V_{cq}} \text{ (rms data pulses)} . \tag{36}$$

This error ε_n is the error per any interrogation period. Counting data over several interrogation periods reduces the random noise error because the noise has zero mean value and is expected to have an amplitude probability density which is symmetrical about the mean. We try to design for ε_n less than one rms data pulse.

DC offsets due to the G_{sd} and G_{dc} blocks appear at the output of the ESP. These offsets, however, are divided by the dc loop transmission to produce an error

$$E_{dc} = \frac{\Delta V_{cdc}}{G_1(0)} \text{ volts} \tag{37}$$

which can always be made much less than one data pulse by minimizing ΔV_{cdc} and maximizing $G_1(0)$. This error accumulates with time, so it should be kept extremely small--typically a few ppm. The error expressed in data pulses and in terms of the equivalent offset voltage at the input to the synchronous demodulator is

$$\varepsilon_{dc} = \frac{\Delta V_{dcsd}}{\Delta V_{cq}\ H_{tgp}(o)\ G_{ct}\ G_{ac}} \quad \text{(data pulses)} , \tag{38}$$

or

$$\varepsilon_{dc} = \frac{\Delta V_{dcsd}\ B\ R}{\Delta V_{cq}\ k_t\ k_p\ 2If_i\ G_{ac}} \quad \text{(data pulses)} \tag{39}$$

Consideration of the accuracy of the torque current level is treated in great detail in Reference 2. The worse case inaccuracy is about 80 ppm in a constant temperature environment. An inaccuracy of less than 10 ppm should be attainable.

CHAPTER III

DESIGN OF SPECIFIC REBALANCE LOOPS

The first step in the design of a specific rebalance loop is the synthesis of the system loop transmission G_1 given by Equation (12). The low frequency region of G_1 is adjusted first by satisfying the ramp slope constraint given by Equation (27). A reasonable design requirement is to set the low frequency gain so that the processed error signal slope is twice the ramp slope. Then Equation (27) becomes

$$\left|G_1\right|_{\text{low freq}} \leq \frac{f_i}{2\pi f_e} \quad . \tag{40}$$

For reasons delineated in Reference 1, we have selected R_d = 614.4 Kpps and f_i = 2.4 kHz for the three specific loop designs to be discussed here. Thus at f_1 = 0.1 Hz, Equation (40) becomes

$$\left|G_1(0.1\ \text{Hz})\right| \leq 3830 \ . \tag{41}$$

Equation (41) establishes the upper bound on the magnitude of the loop transmission at f = 0.1 Hz. For most rebalance loops, other considerations such as electronic noise and oscillation stability, cause the loop transmission at f = 0.1 Hz to be less than the limit above.

The constraint expressed by Equation (41) and the fundamental considerations discussed in Chapter II were used to synthesize the loop transmissions for the 2412 accelerometer, the GG334C gyroscope, and the 2401-009

accelerometer. The characteristics of these inertial sensors are given in Table I; the respective loop transmission plots are shown in Figures 5, 6, and 7; and the values of the loop transfer parameters are listed in Table II.

The 2412 Accelerometer Rebalance Loop--0-G Experiment

The 2412 accelerometer loop is designed for high resolution (2.6×10^{-4} g/data pulse). This necessitates a low torquer current (1 mA) and consequently a high ESP gain (146,000). The high ESP gain raises the random electronic noise level at the output of the ESP. Thus the closed loop bandwidth must be low to limit electronic noise. The loop transmission of Figure 5 is a compromise among several conflicting requirements. It is very important to plot the ESP transfer simultaneously with the system loop transmission to insure that random noise generated in the ESP are properly reduced by frequency domain filtering before it reaches the output of the ESP.

The rather high calculated value of random noise at the output of the ESP (0.47 rms data pulse) will be much reduced by counting data over many interrogation periods since the noise fluctuates both above and below a fixed mean value. The low-frequency noise is also reduced by the loop transmission. This reduction was not considered in the calculation of ε_n which is therefore a pessimistic value.

The torque current ripple ΔV_{tcro} is negligibly small and, of course, since it is a synchronized signal, its only effect is to cause small localized loop gain changes equivalent to small changes in the ramp slope. The uncertainty caused by dc offsets, however, is significant—44 ppm. This is greatly reduced by experimentally selecting an offset adjusting resistor in the synchronous demodulator to give zero offset under open-loop conditions. However,

TABLE I.

INERTIAL SENSOR PARAMETERS

Parameter	Accelerometer 2412	Gyroscope GG334C	Accelerometer 2401-009
J - mass moment of inertia dyne-cm-sec^2/rad	200	250	24
F - damping coefficient dyne-cm-sec/rad	9×10^6	5×10^5	10^5
B - elastic restraining torque dyne-cm/rad	6540	0	4750
K_p - pickoff sensitivity rms volts/rad	36	18	18
K_t - torquer scale factor dyne-cm/mA	218	290	275
K_t' - torquer scale factor deg./mA-sec		0.0333	
K_a - acceleration scale factor mA/g	30		4.9
K_{oi} - gyro gain deg/deg		0.4	
f_{sg} - pickoff frequency kHz	20	32	20
V_{sg} - pickoff excitation rms volts	4.5	4.5	1.6

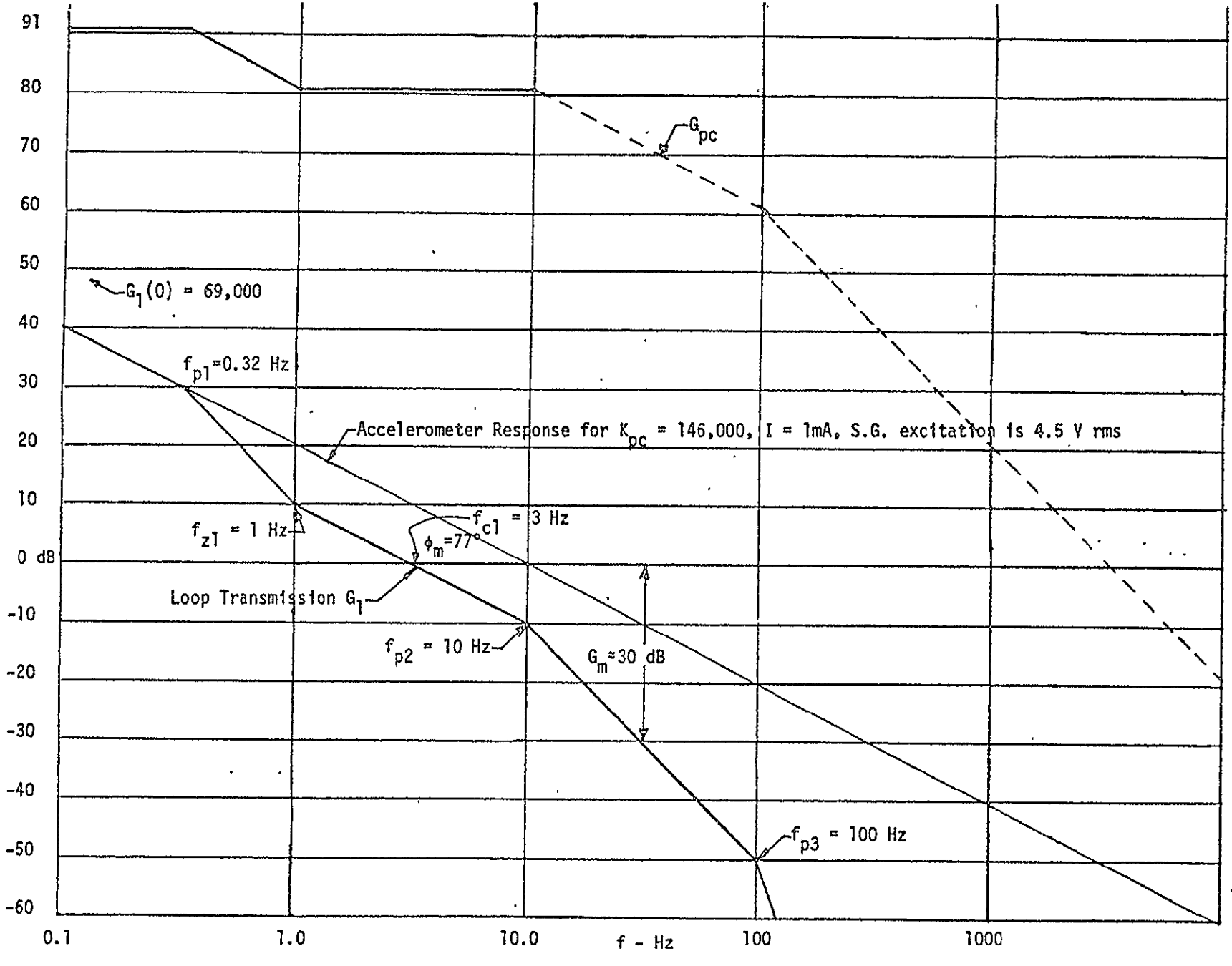


Figure 5. System Loop Transmission and Error Signal Processor Response for the 2412 Accelerometer.

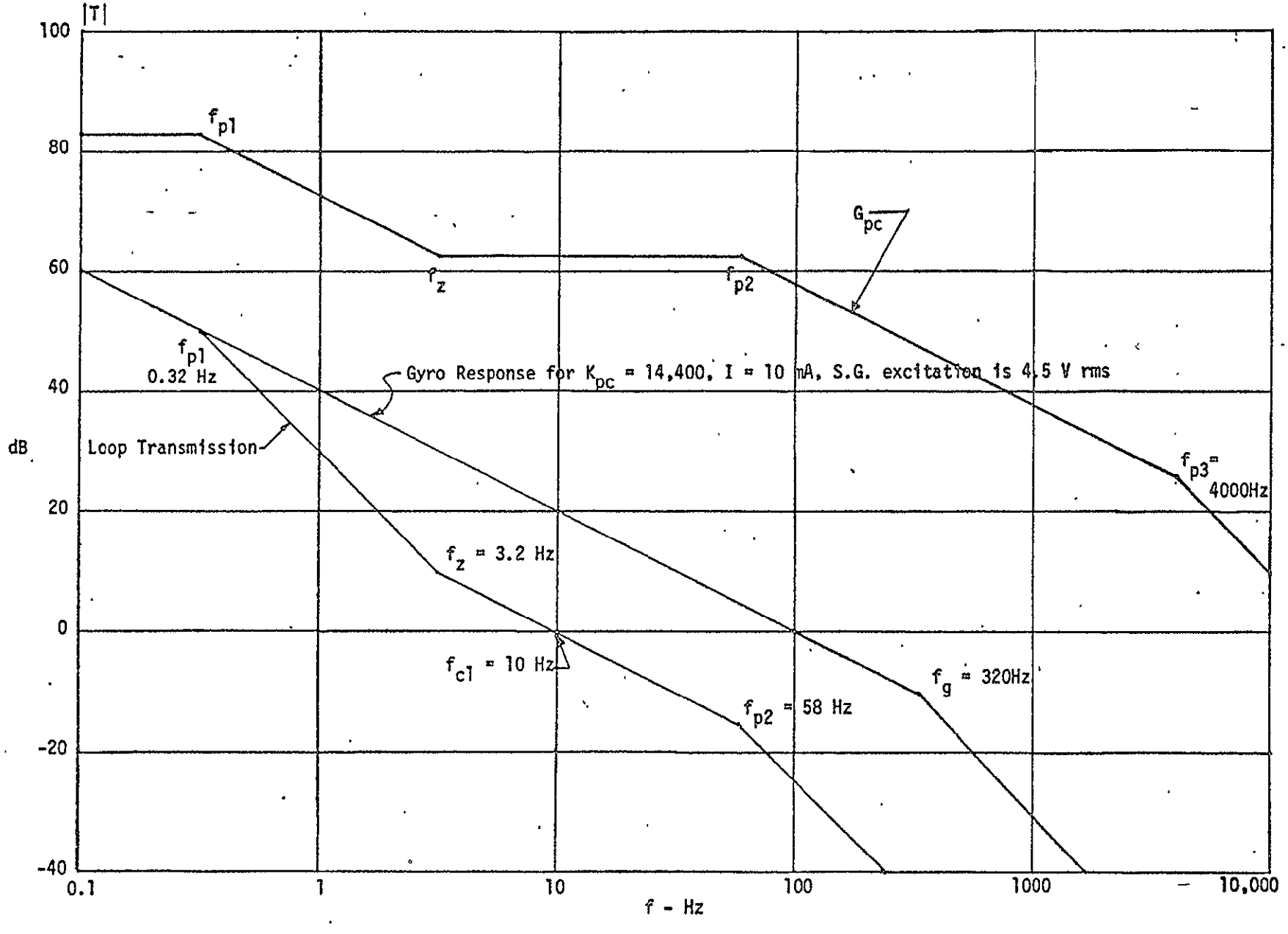


Figure 6. System Loop Transmission and Error Signal Processor Response for the GG334C Gyroscope.

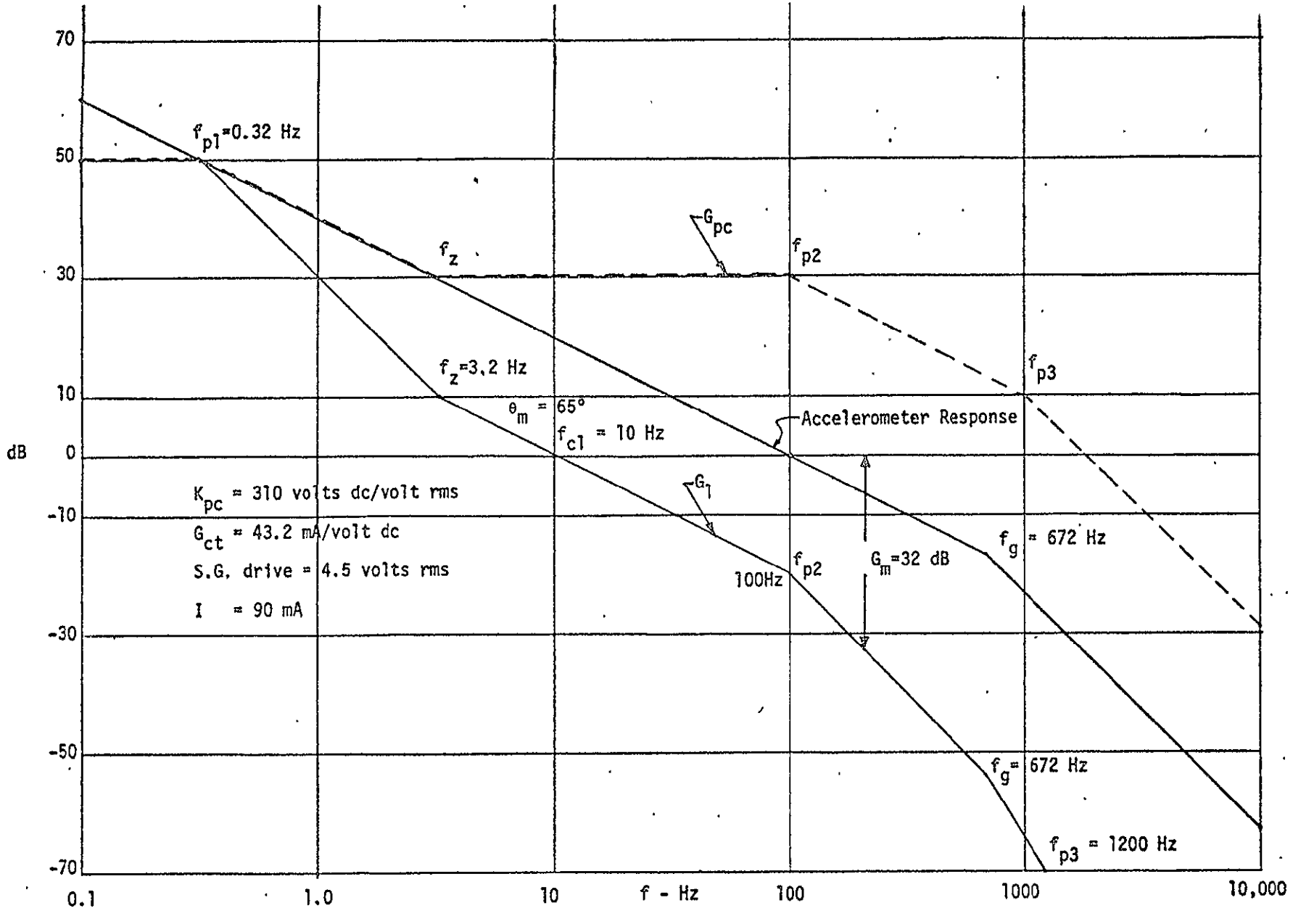


Figure 7. System Loop Transmission and Error Signal Processor Response for the 2401-009 Accelerometer.

TABLE II.

DESIGN VALUES OF THE TRANSFER PARAMETERS OF SPECIFIC REBALANCE LOOPS

Data Rate R_d = 614.4 kpps
Interrogation Frequency = f_i = 2.4 kHz
Ramp Slope R = 10^4 volts/sec
Data Quantization ΔV_{cq} = 16.3 mV/data pulse

Parameter	Units	2412	GG334C	2401-009
I	mA	1	10	90
S.G. Drive	volts rms	4.5	4.5	1.6
G_1(0 Hz)		69,000	∞	13,600
G_1(0.1 Hz)		100	1,000	1,000
f_{c1}	Hz	3	10	10
G_{ct}	mA/volt dc	0.48	4.8	43.2
K_{pc}	volts dc/volt rms	146,000	14,400	315
G_p	volts/volt	10	10	10
G_b	volts/volt	6	6	6
G_a	volts/volt	20	19.4	1.33
G_{sd}	volts dc/volt rms	1.45	1.45	1.45
K_{dc}	volts/volt	83.8	8.6	2.72
f_{t1}	Hz	1	3.2	3.12
f_{p1}	Hz	0.32	0.32	0.33
f_{p2}	Hz	10	58	95
f_{p3}	Hz	100	4000	1230
$\Delta\theta_d$	arc-sec/data pulse		3.94×10^{-3}	
$\Delta\theta_{di}$	arc-sec/data pulse		9.85×10^{-3}	
Δg	g/data pulse	2.6×10^{-4}		0.144
ΔV_{tcro}	volts	1.3×10^{-7}	2.6×10^{-4}	3.3×10^{-4}
ε_n	rms data pulse	0.47	8.2×10^{-3}	4.0×10^{-6}
ε_{dc}	data pulse	4.4×10^{-5}	≈ 0	8.5×10^{-6}

temperature changes and aging effects may generate offsets which will have some effect on accuracy.

The gain was distributed in the ESP to properly control saturation and noise performance. Since the monolithic instrumentation amplifier used as the preamplifier and also in the synchronous demodulator has poor overload characteristics (large phase shift), the preamplifier gain was set sufficiently low to prevent saturation under all expected overload conditions. A special overload circuit in the ac amplifier clamped the input to the synchronous demodulator to prevent its saturation. Although a gain in the ESP of 146,000 for the 2412 loop is rather high, the basic design of the ESP would allow the gain to be increased to about 10^7 with only minor adjustments in component values.

The GG334C Gyroscope Rebalance Loop

The GG334C gyro loop is also designed for high resolution (3.94×10^{-3} arc-sec/data pulse). The ESP was realized by making minor modifications in the 2412 ESP as is clear from Table II. The low required ESP gain allowed operation at a 10 Hz closed-loop bandwidth with very low uncertainty due to random noise (8.2×10^{-3} rms data pulse). The error caused by dc offsets are negligible as a result of the integrating characteristic of the gyro (B is very small).

The loop transmission of Figure 6 was shaped according to the usual requirements already discussed. The pole at f_3 = 4000 Hz is not needed for the shaping but was added in the output stage of the ESP to reduce high frequency digital noise pickup.

The 2401-009 Accelerometer Rebalance Loop--DDH Experiment

The 2401-009 accelerometer loop is a high g range loop requiring a torque current level of 90 mA. Oscillation stability requirements and the decision to maintain the same network topology in the dc amplifier and compensator strongly constrained the shaping of the loop transmission for this accelerometer, as will be clear from a study of Figure 7. The low ESP gain of 315 is difficult to realize because of the very low design gain of the G_{dc} block (2.72). The pole-zero constellation for the G_{dc} block was difficult to implement with reasonable component values for this low gain.

The low ESP gain, however, causes the random noise uncertainty to be extremely low (4×10^{-6} rms data pulse). The dc offset uncertainty is also quite low due primarily to the large torque current.

CHAPTER IV

DESIGN IMPLEMENTATION

The theory developed in the previous sections will be utilized in the practical design implementation for the Error Signal Processing (ESP) system, the Digital Control Electronics (DCE), and the Torque Current Generator (TCG). Much of the initial design details were included in an earlier report,[1] and where feasible are quoted here.

Careful thought was given to the partitioning of the overall design into three distinct printed circuit boards, each board containing one separate electronics group; i.e., the ESP board, the DCE board, and the TCG board. Electronic functions were grouped on each board so as to reduce the number of wiring interconnections as much as possible between boards, and further to keep contamination of the analog signals by the digital control signals to a minimum. Wherever possible, on each board separate ground return lines were utilized for the digital signals and the analog signals.

An investigative search of available semiconductor components was made at the initiation of this project, and those devices having the most desirable specifications for each circuit design were utilized. Also, throughout the project it has been our goal to keep abreast of the state-of-the-art, and to provide injection of new devices and ideas into the overall system design as they became available, in order to provide a continuation of performance improvement. Several of these newer devices, and their performance improvements over devices utilized for earlier designs, will be enumerated in the following discussions. We have, wherever possible, attempted to reduce the number of component semiconductor and capacitor chips required in order to

facilitate the reduction of the circuit board packages to hybrid thick-film integrated circuit layouts.

It was also a design goal to minimize the number of power supplies required. We have achieved a significant improvement over the earlier designs, which required +15V, -15V, +5V, and +35V, in that the present systems obtain all power from +15V and -15V.

The following discussion covers the components utilized in each of the distinct parts of the pulse rebalance electronics loop as shown in Figure 1, namely the ESP, the DCE, and the TCG.

Error Signal Processor (ESP)

As stated in Chapter II, the ESP must amplify, filter, demodulate, and frequency-domain compensate the differential-pickoff output error signal from the Inertial Sensor. The ESP contains the units indicated in Figure 2 and in more detail in Figure 8, namely the AC Preamplifier, the Bandpass Filter, the AC Amplifier, the Synchronous Demodulator, and the DC Amplifier—Loop Compensator. Each of these units is discussed in detail below. The overall circuit diagram for the ESP is shown in Figure 8. Component values for the three systems are shown in Table III.

AC Preamplifier. The Analog Devices AD-520 is utilized for the AC Preamplifier (IC1 of Figure 8) primarily for its very high common-mode rejection ratio (CMRR), good slew-rate of > 2.5 V/μsec, wide bandwidth of 180 kHz, and because it is at present the only one-chip monolithic instrumentation amplifier commercially available. Other reasons for using and characteristics of this device were stated in our previous report.[1] The gain of the preamplifier stage was reduced from an earlier design value of 20 to 10 (equal to the ratio of R2:R1), primarily to ensure that the largest differential input

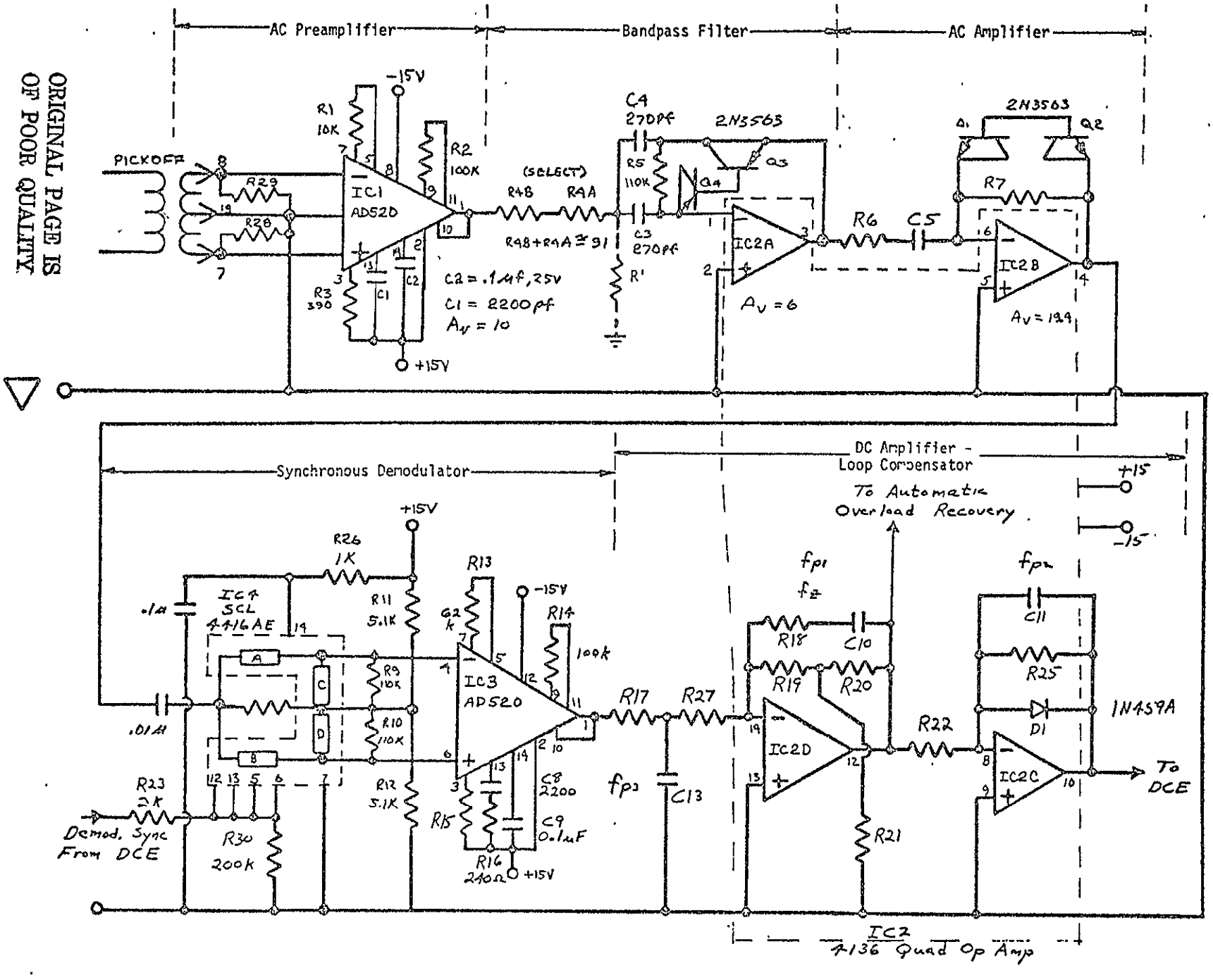


Figure 8. Electrical Schematic Diagram for the Error Signal Processor.

TABLE III.

ERROR SIGNAL PROCESSOR COMPONENT VALUES

Component Symbol	Component Value		
R in KΩ, C in μF	Accelerometer 2412	Gyroscope GG334C	Accelerometer 2401-009
R_6	5.1	5.1	75
R_7	100	100	100
R_{15}	Adjust for	Zero Open-Loop	Torque Current
R_{17}	39	75	33
R_{18}	1590	510	510
R_{19}	100	120	510
R_{20}	33	30	7.5
R_{21}	1	1	1
R_{22}	150	200	430
R_{25}	330	200	430
R_{27}	270	300	1500
C_5	0.1	0.1	0.01
C_{10}	0.1	0.1	0.1
C_{11}	0.047	0.0002	0.0039
C_{13}	0.047	0.047	0.0039

signal from the Inertial Sensor (which would occur when the gyro or accelerometer was at the end of its dynamic range) would not saturate the output of IC1. If the end of its dynamic range) would not saturate the output of IC1. If saturation does occur, the phase shift through the AD520 amplifier becomes excessive, which could produce latchup of the rebalance loop... There are some disadvantages to the use of the AD520, which it now appears that a recent circuit design may correct[3], namely a somewhat high midband input noise voltage of up to 30 nanovolts/$\sqrt{Hz}$, the excess phase shift under output saturation, the large capacitors required for compensation, and at present only a sole-source supplier. Even with these disadvantages the ability to obtain better than 80 dB CMRR without the requirement of typically 4 resistors matched to within $\pm$ 0.1% is of definite advantage when compared to a standard op amp circuit.

Bandpass Filter. The bandpass filter is a tuned RC-Active filter containing the IC2A op amp of Figure 8, with a center frequency set by resistors R', R4, R5, and capacitors C3 and C4. For the values shown in Figure 8, the center frequency f_o is 19.2 kHz, the Q is approximately 1.8, and the center frequency gain H_o is approximately 6.5. These parameters are related by the following design equations[1,4] (with C3 = C4 = C),

$$R4 = \frac{Q}{H_o \omega_o C} ,$$

$$R' = \frac{Q}{(2Q^2 - H_o)\omega_o C} ,$$

$$R5 = \frac{2Q}{\omega_o C} . \qquad (42)$$

Since we chose $2Q^2 = H_o$, this eliminates resistor R'.

The op amp IC2A is really one-fourth of a single monolithic quad chip, the Raytheon RM 4136. Our earlier designs required six-μA748 individual op amp chips to accomplish the ESP function now obtained by one-RM 4136 chip. Further, the 4136 quad amp is entirely frequency compensated by on-chip MOS capacitors, thereby also eliminating six capacitors required in our earlier design. Hence, the overall component count has been lowered significantly. The RM 4136 is more similar to the μA741 amplifier, except that it has twice the slew-rate (1.0 V/μ-sec vs. 0.5), considerably lower equivalent input noise voltage (10 NV/$\sqrt{Hz}$ vs. 30 NV/$\sqrt{Hz}$) than either the 741 or 748, lower input bias current (5 NA vs. 30 NA), and a 3 MHz unity gain-bandwidth vs. 1 MHz for the 741. Other parameters are the same.

A novel feature of the present Bandpass Filter design is the inclusion of positive and negative clamping of the voltage level at the output of IC2A by the action of the emitter-base breakdown of Q3 - Q4 (2N3563). These transistors are utilized rather than Zener diodes, because of very low capacitance (typically < 3 pf) in the reverse direction, low reverse leakage current, and sharp limiting at approximately 5 volts reverse voltage. Another very important characteristic is obtained under saturation, which occurs when the inertial sensor goes to its end stops under full dynamic ranging. In a high gain loop, such as the O - G system, the output voltage of the AC Amplifier (IC2B) will saturate first (due to the same limiting action afforded by Q1 - Q2 of Figure 8), thereby producing a lagging phase shift. Next, however, the previous gain stage IC2A will now saturate, thereby lowering the effective resistance R5, which appears to the bandpass filter as a requirement for a higher value of center frequency f_o. Thus, as the output of IC2A limits due to the clamping action of Q3 - Q4, a leading

phase shift is produced that compensates for the lagging phase shift produced by IC2B. Experimentally, for the 0 - G Rebalance Loop, it was observed that the phase shift at the output of IC2B went from 0° to 35° lagging (as Q1 - Q2 clamped) and then back to approximately 10° (as Q3 - Q4 clamped) under full dynamic range of the accelerometer.

AC Amplifier. The gain of the ac amplifier is equal to -R7/R6 in Figure 8. One-fourth of the RM4136 op-amp is used for IC2B. The emitter-base clamp action of Q1 - Q2 limits the maximum output of the AC Amplifier between approximately $\pm$ 5.5 volts, so as not to forward-bias the CMOS SCL4416A (IC4) quad switch used in the synchronous demodulator. This clamp also minimizes phase-shifts under overload, as mentioned previously. The ac amplifier is a convenient point in the loop to adjust the system gain, as it merely requires a change in resistor R6 and/or R7. None of the present designs required a dual-scale factor capability, hence gain switching used in the earlier designs was eliminated.

Synchronous Demodulator. The design of the synchronous demodulator is basically identical to the design of the last report[1], except that the CMOS CD4016A quad switch was replaced by the SCL4416A quad switch containing an on-chip DPDT wiring, thereby eliminating a CD4007A inverter required for the early design. We were also able to eliminate a 748 op-amp sine-wave-to-+15V square-wave converter stage, as we are now utilizing all CMOS compatible logic.

The synchronous demodulator has a gain of $\frac{2\sqrt{2}}{\pi}$ R14/R13, equal to 1.45. The circuit is a full-wave rectifier, with CMOS switches A and D 'on' while C and B are 'off', for one cycle, and then just reversed for the other cycle. The synchronizing action is obtained by the demodulation-sync signal from the DCE that is in phase with the signal-generator signal to the inertial

sensor. Thus, the output of IC3 is either positive, negative, or zero depending on the amplitude and phase of the pickoff error signal. Adjustment for the quadrature component is most easily made by adjusting resistors R28 and R29 so as to obtain a null at the output of the synchronous demodulator IC3.

The AD520 amplifier chip is also utilized for IC3, primarily for its high CMRR, low offset voltage, and equal input impedance to both sides of the amplifier.

Rather than using both a +7.5V and -7.5V supply for IC4, the unit is floated above ground at +7.5V, thereby requiring one +15V supply voltage. This gives an input dynamic range to the synchronous demodulator of approximately 14V peak-to-peak, which is safely greater than the output clamping at $\pm$ 5.5V of IC2B.

There are two advantages obtained by using the CMOS quad switch as a gating element rather than the more typical bipolar transistors: one is the isolation of the digital drive signal from the analog error signal and secondly, the matching obtained in 'on' resistances between the four units on the same substrate.

DC Amplifier and Loop Compensator. These functions are obtained by op amps IC2C and IC2D of the RM4136 chip of Figure 8, and their associated RC networks. In Figure 8 the voltage transfer function from the output of the synchronous demodulator IC3 to the output of IC2D is

$$\frac{V_o(IC2D)}{V_{in}} = -\left(\frac{R19}{R17 + R27}\right)\left(\frac{R20 + R21}{R21}\right) \times \frac{(1 + s\,R18\,C10)}{\left[1 + s\left(\frac{R17\,R27}{R17 + R27}\right) C13\right]\left\{1 + sC10\left[R18 + R19\left(\frac{R20 + R21}{R21}\right)\right]\right\}}, \quad (43)$$

while the transfer function from the output of IC2D to the output of IC2C is

$$\frac{V_o(IC2C)}{V_o(IC2D)} = - \left(\frac{R25}{R22}\right) \left(\frac{1}{1 + s\ R25\ C11}\right), \qquad (44)$$

for $V_o(IC2C) > - 0.5V$. Thus, the overall transfer function for this block contains one zero and three poles, which can conveniently be chosen to satisfy the design requirements for τ_z, τ_{p1}, τ_{p2} and τ_{p3} of Equation (9).

The diode clamp D1 limits the dc output of IC2C to a lower limit of -0.5V, in order that the input requirements for the duty cycle generator, which follows the ESP block, not be exceeded. In actual operation, the zero torque level (no error signal) at the output of IC2C is shifted to +2V, with a total linear dynamic range of 0V to +4V. This requirement is explained in more detail in the next section.

For high resolution requirements, it is necessary that the dc offsets of IC3, IC2D, and IC2C be nulled out, so that with zero input error signal to IC1, the output of IC2C is at a dc level corresponding to zero torque (+2V dc). This is usually accomplished by adjusting resistor R15, thereby adjusting the dc output of the synchronous demodulator. The allowable offsets can be calculated, for a required accuracy, from Equations (38) or (39).

The amplified error signal used for the automatic overload recovery circuit (ORC) is obtained from the output of IC2D, thereby giving a dynamic range of $\pm$14 volt. The operation of the ORC is explained in detail later in this report.

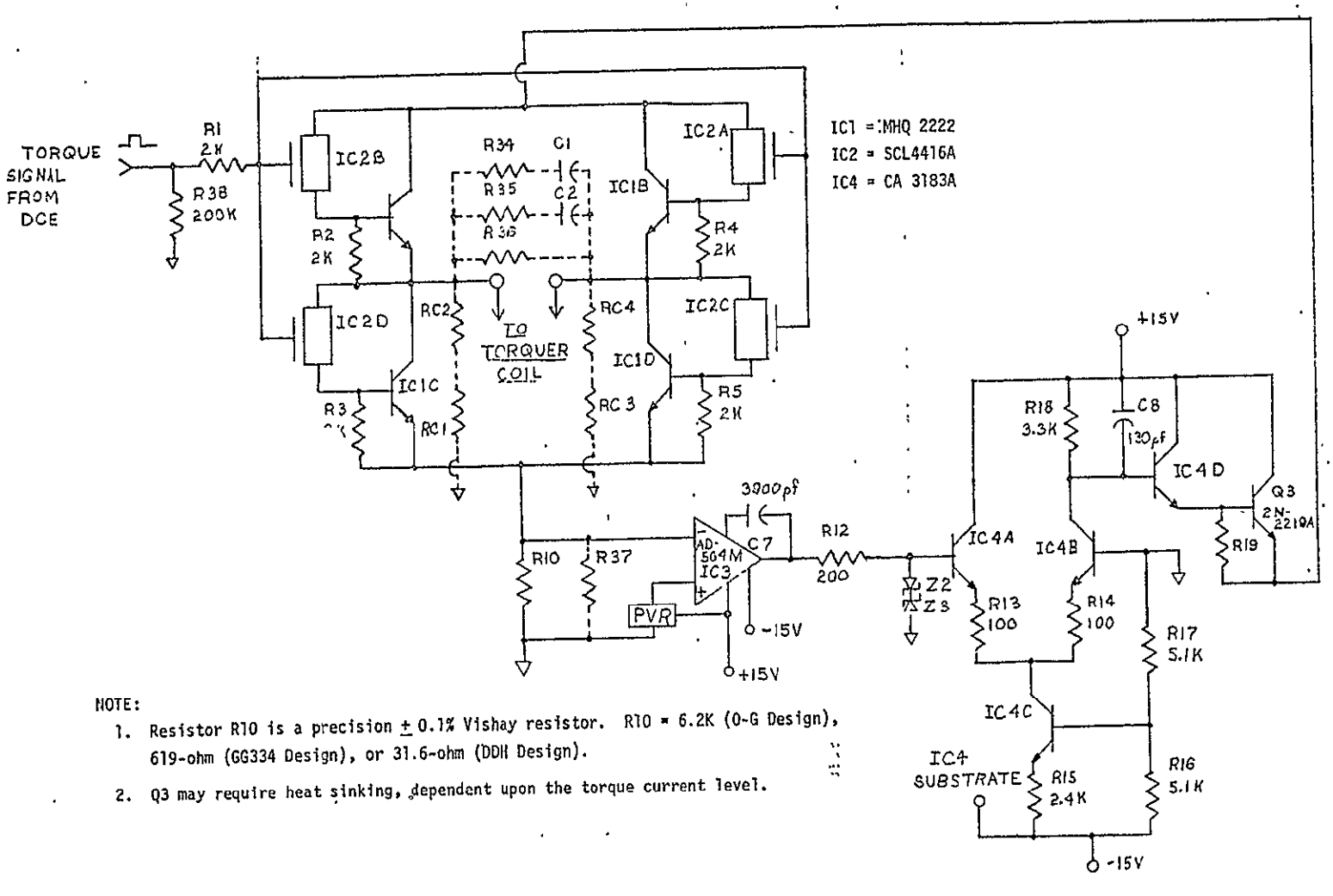
Torque Current Generator (TCG)

The TCG has probably the most severe requirement of high accuracy and low drift of any element within an electronic rebalance loop for an inertial sensor. The rebalancing torquer for the gyro or accelerometer must be driven by current pulses of precise shape, accuracy, and amplitude.

The basic diagram for the TCG is shown in Figure 9, and is an improved version of that utilized during the last contract period[1]. Since we are now using all CMOS logic, the buffers utilized in last year's design are no longer required. Further, since the TCG operates from ± 15 volt, it is possible to use the CMOS SCL4416A DPDT quad bilateral switch to control the turn-on of the H-Switch.

Many of the design features of the TCG resulted from a detailed study by R. D. McKnight.[2] The TCG consists of a dc feedback loop containing a current regulator, comprising a precision voltage reference (PVR), a comparator operational amplifier, a level shifting amplifier and a power transistor current driver; the H-Switch, or bridge circuit, which determines the direction of the current through the torquer, with the amount of current per unit time determined by the torque signal command from the digital control electronics; and, for very low torque currents as in the O-G experiment, an overload recovery circuit (ORC).

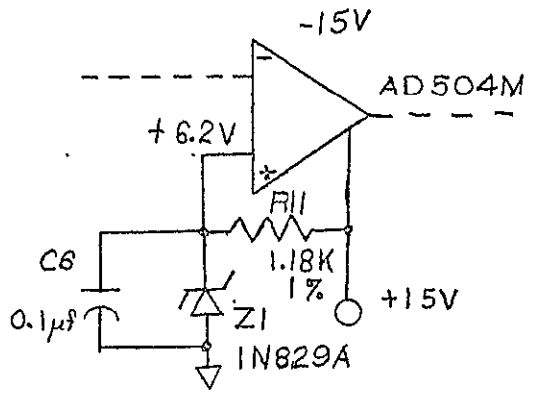
Current Regulator. The torque current is determined by the comparison between a 1N829A precision voltage reference Zener diode of 6.2V, and a precision resistor R10 (these are indicated in Figures 9 and 10a). If the loop gain is high, the torque current is thus equal to 6.2V/R10. The 1N829A reference diode Z1 has a stability of typically 5ppm/°C, while the resistor R10 is a Vishay type S102, ± 0.1% accuracy, with a stability of ± 1 ppm/°C



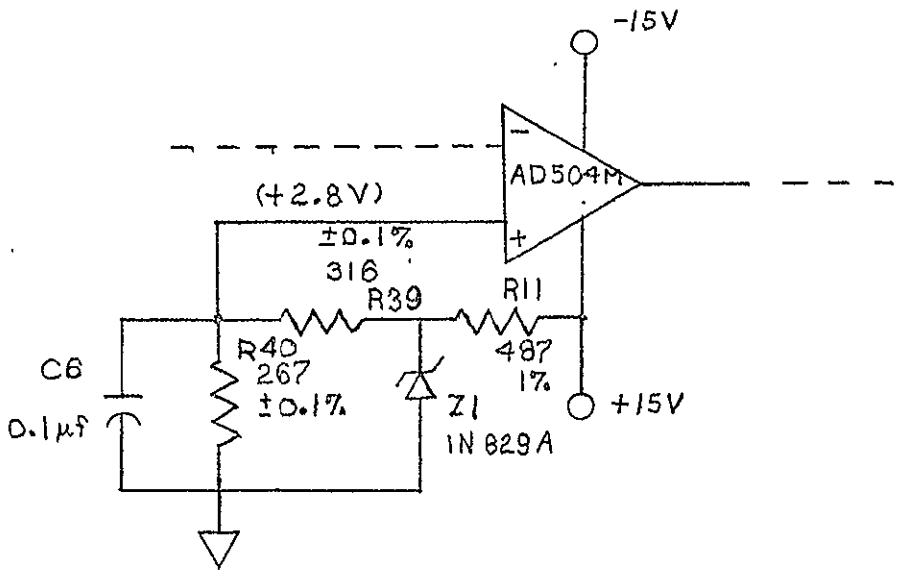
NOTE:

1. Resistor R10 is a precision ± 0.1% Vishay resistor. R10 = 6.2K (O-G Design), 619-ohm (GG334 Design), or 31.6-ohm (DDH Design).
2. Q3 may require heat sinking, dependent upon the torque current level.

Figure 9. Electrical Schematic Diagram for the Torque Current Generator.



(a) PVR Utilized for O-G Experiment and Modified GG334 Loop.



(b) PVR Utilized for DDH Experiment.

Figure 10. Precision Voltage Reference Circuits.

from 0° to 60°C. The full-scale torque currents were 1mA for the Q - G loop, 10 mA for the modified GG334 gyro loop, and 90 mA for the DDH loop. In order to still utilize ± 15V supplies, for the DDH loop it was necessary to divide the 6.2V reference voltage, using two precision resistors R39 and R40, down to +2.8V as indicated in the circuit of Figure 10b. In all the TCG designs, resistors R37, R36, RC1-RC4 of Figure 9 are normally not used, but are available to alter the torquer current value, and provide bias error adjustment for the inertial sensor.

If the accuracy of the torque current is to be better than 1 ppm, it is necessary that the loop transmission gain be greater than 10^6, so that the 6.2V reference is exactly reproduced across R10. The AD504M comparator IC3 has a gain of approximately 8×10^6, while the differential level-shifting amplifier of IC4 has a gain of approximately 13. The feedback attenuation due to the H-Switch impedance and R10 is between 1/4 and 1 depending upon the inertial sensor used, hence, the loop transmission gain is between 1×10^8 (160 dB) and 2.4×10^7 (148 dB). The overall closed-loop bandwidth for the TCG is about 150 kHz.

The AD504M is used for the comparator function (IC3) in Figure 9 because it currently is the best available monolithic op amp for high gain (8×10^6), unnulled offset drift (0.5 μV/°C and 0.2 NA/°C), low flicker noise (0.6 μV p-p max from 0.1 Hz to 10 Hz) and good CMRR with the inputs at +6.2V (110 dB min.). The output of IC3 is short-circuit limited at 25 mA. The R12, Z2-Z3 network of Figure 9 limits the maximum input voltage to IC4A to ± 5.3V, in order not to exceed the BV_{EBO} ratings of the CA3183A unit.

A reduction of component count was achieved by using a monolithic npn array, the CA3183A (IC4), for the transistors in the differential level-

shifting stage. This stage shifts the dc voltage from typically 0 volts at the output of IC3 to the required value (8 to 12V) at the top of the H-Switch. Transistor Q3 is a medium power unit (2N2219A) that can supply a torque current of up to 200 mA.

McKnight[2] has calculated the total equivalent rms input noise for the TCG as approximately 21 μV_{rms} over an earlier 200 kHz bandwidth design. This noise is due primarily to the Zener noise of the 1N829A diode Z1. For the present design of 150 kHz bandwidth the value should be about 18 μV_{rms}. This corresponds to a short-term uncertainty in the torque current value of 18 μV_{rms}/6.2V, or 3 ppm rms deviation. Since this noise is random, its contribution is negligible for a long-term count.

H-Switch. The H-Switch, or bridge circuit, routes the precision torque current to the torquer coil of the inertial sensor, upon command from the torque signal from the DCE. Isolation from the digital control signal is achieved by the use of the SCL 4416A DPDT quad CMOS switch (IC2), which has an input gate leakage of typically less that 1×10^{-10} ampere at the operating temperature of the inertial sensor. Each of the quad CMOS switches together with one of the MHQ2222 transistors forms an FET-bipolar composite switch. When the digital torque signal command is high (+14V), CMOS switches 2A and 2D are 'on', while 2B and 2C are 'off'. Thus, bipolar transistors 1B and 1C are conducting, while 1A and 1D are turned off. Hence, the torque current flows from the top of the bridge through 1B, through the torquer coil, and through 1C to R10. When the digital torque signal command goes low (0V), the process is just reversed, with torque current flowing through 1A, through the torquer coil, and through 1D.

Resistors R36 and RC1-RC4 are normally not used, but permit the torquer current to be scaled to a lower value, while also allowing a bias error compensation for the inertial sensor. The RC network of R35C2 and R34C1 allow compensation of the RL characteristic of the torquer coil, thereby making the torquer appear as a resistor to the H-Switch.

Bipolar transistors 1A-1D are discrete 2N2222 transistor chips packaged in a 14 pin ceramic package for convenience. In the early investigations of the H-Switch, we attempted to utilize a monolithic npn CA 3183A array for these transistors, but found that torque current requirements of greater than 30 mA produced a voltage drop across the ohmic collector resistance of the monolithic devices, which in turn caused the pnp substrate transistor in the monolithic chip to be forward-biased. This condition produced a large by-pass current around the H-Switch to ground, and in some cases could eventually destroy the monolithic chip. It is therefore imperative that discrete chip bipolar transistors be used in the H-Switch circuit.

The use of the CMOS SCL 4416A (IC2) quad switch having equal r_{on} and C_{in} values, as well as the use of the MHQ2222 bipolar quad (IC1), permits nearly equal rise and fall times of the current through the torquer in either direction. This significantly reduces the bias errors due to unequal rise- and fall-times, and due to transient feedthrough currents in the H-Switch.

Overload Recovery Circuit (ORC). The ORC is useful when an inertial sensor requires a very low torque current, such as the 1mA full-scale requirement for the Zero-Gravity Accelerometer experiment. The ORC senses when the loop is outside its dynamic range, and then switches to a large torque current to reduce the recovery time of the loop. When the amplified error signal in

the ESP drops back within the dynamic range, the ORC reverts back to the original scaled precision torque current value.

This system can best be illustrated by referring to the diagrams for the basic TCG (Figure 9), the ORC circuit of Figure 11, and to the ESP circuit of Figure 8. For the 0-G design the full-scale torque current is 7/8 mA corresponding to 7/240 g for the Kearfott 2412 accelerometer. It is important that the loop be able to recover rapidly from an overload condition (which is greater than 10 g at launch), so that as much useful data as possible can be obtained during the relative short period that the vehicle is in an environment of $\leq$ 1/30 g. The ORC senses the output dc voltage of IC2D of the ESP, Figure 8. The output is taken at that point instead of at the output of the next stage (IC2C), since there the lower limit is clamped at -0.5V. A full-scale output of $\pm$ 1mA torque current corresponds to an error signal output of IC2C of 0 to +4V. Since for the 0-G design the gain of IC2C is -5.3, this is a full-scale dynamic range of 0 to -0.75 volt at the output of IC2D.

For convenience, the sense voltages are set at approximately +10V and -10V to trigger the ORC. The output of IC2D (Figure 8) is sensed by two op amp Schmidt trigger comparators, IC6A and IC6B (Figure 11), so that if the output of IC2D is $\geq$ 10V, the output of IC6A is high (+14V), while IC6B is low (-14V). Diode D1 of Figure 11 will conduct while D2 will be off. Thus, the output of IC6C will be high (+14V), thereby turning 'on' the SCL 4416A transmission gates 5A and 5D while turning 'off' gates 5B and 5C. The new torquer current is thus determined by Q1 and R9, and is 6.2V/121-ohm, or 51 mA. This overload current is thus equivalent to a full-scale of $\pm$ 51mA/30 mA/g or $\pm$ 1.7 g for the Kearfott 2412 accelerometer. The same action occurs

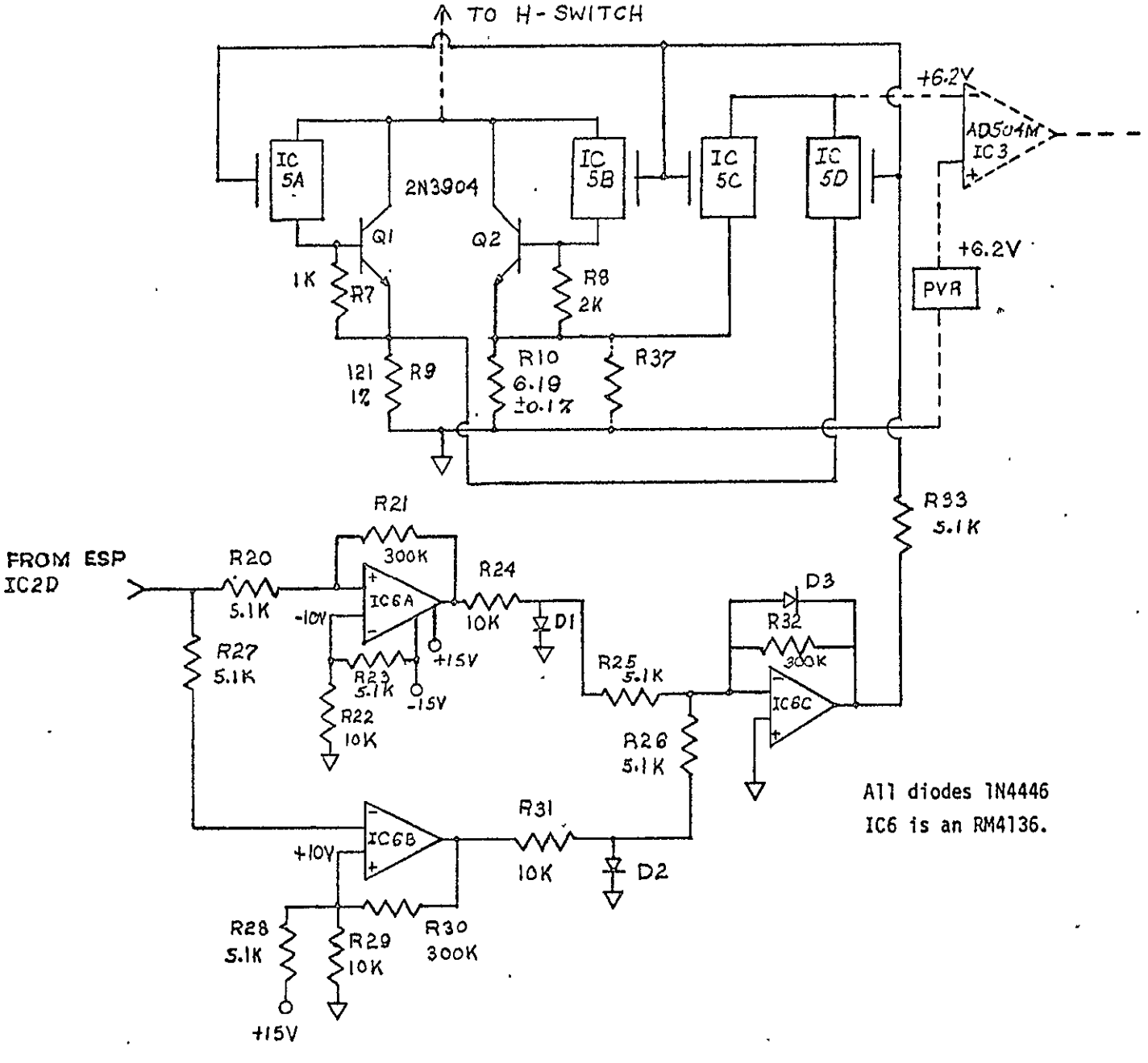


Figure 11. Overload Recovery Circuit for the O-G Experiment.

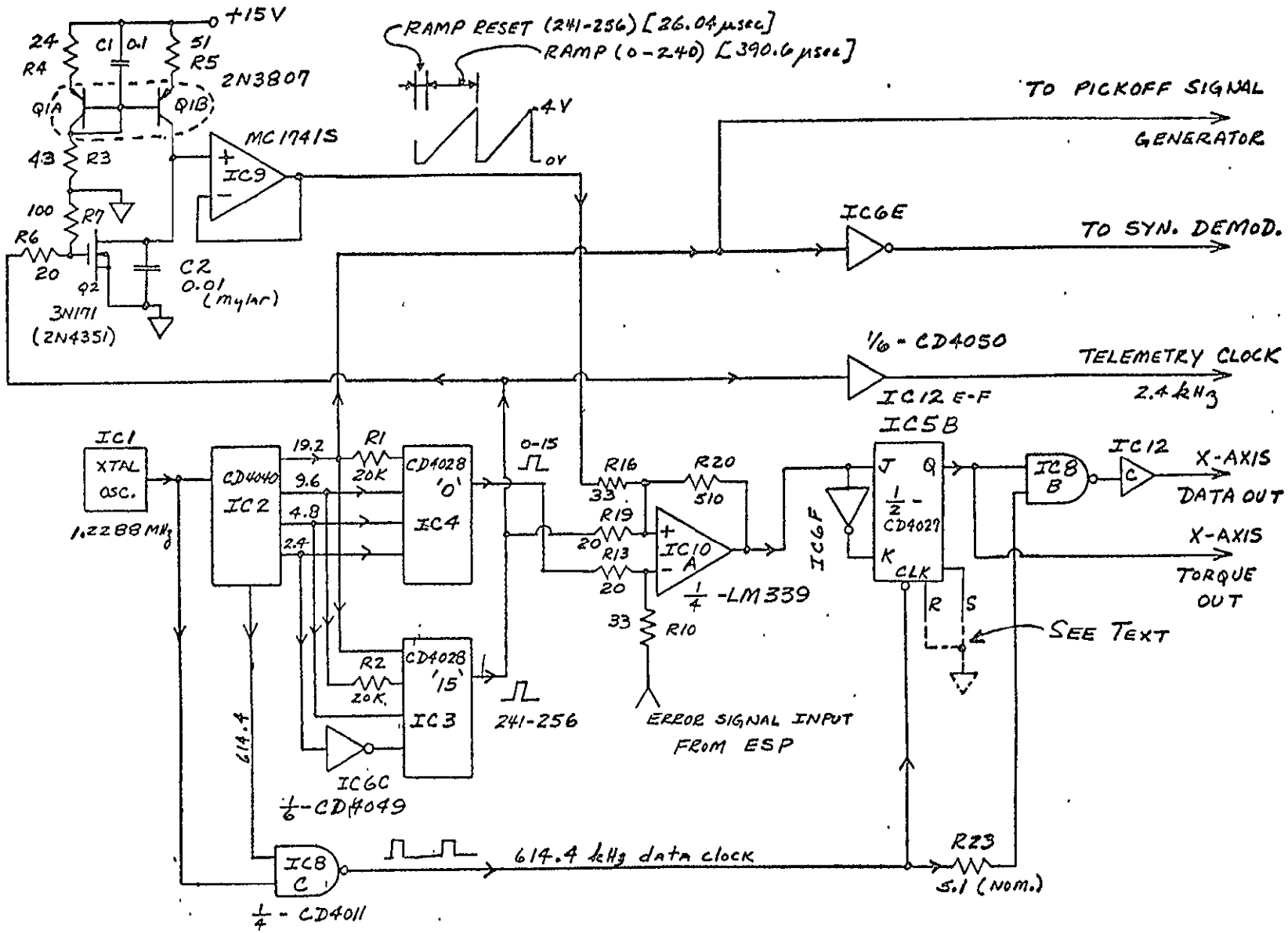
when the output voltage of IC2D is $\leq$ -10V, which now produces a high state at the output of IC6B, causing D2 to conduct, and a low state at the output of IC6A, producing again a high (+14V) output to the SCL4416A gate. When the signal from IC2D is less than |10V|, both outputs of IC6A and IC6B are high, producing a low output of IC6C (-0.5V), thereby keeping the SCL 4416A gates 5B and 5C 'on' while 5A and 5D are 'off'. The torquer current is thus the precision value of 6.2V/6.19K, or $\pm$ 1mA.

In order to prevent false recurrence of triggering at the $\pm$ 10V levels, a hysteresis of 0.3V was designed into the IC6A and IC6B trigger comparators.

It is also possible to obtain torquering information while the ORC is operative, since the torque current is known, as well as the scale factor. All that would be required additionally would be the polarity of the signal from the output of IC2D and the pulse count from the output of IC6C, which could feed a two-input CD4011A Nand, gated with the 614.4 kHz clock signal, to produce an output data train whose frequency would be directly proportional to the g-rate from $\pm$ 7/240 g to $\pm$ 1.7 g. The accuracy of this data would not be as good as that for the normal 1 mA ($\pm$ 1/30 g) data, since the threshold trigger levels of the IC6A and IC6B comparators are not very precise.

Digital Control Electronics (DCE)

The DCE brassboard system comprises a digital function generator, a ramp generator, a duty cycle generator, a data and torque generator, and the pickoff sinusoidal signal generator. The circuit for one axis of a three-axis DCE is shown in Figure 12. The digital electronics has been converted from the TTL design of last year, which required approximately 5V at 0.5 amp, to CMOS logic that now requires 15V at only 10 mA.



NOTE: ALL RESISTORS IN KILOHMS, ALL CAPACITORS IN MICROFARADS.

Figure 12. Digital Control Electronics (x-axis).

Digital Function Generator. The logic is controlled by a precision hybrid IC CMOS crystal oscillator (IC1) manufactured by Q-Tech Corporation. The output is a square-wave signal of 1.2288 MHz, with a stability within 0.3 ppm/°C and 10 ppm/year. This frequency is counted down by a CD4040, 12-stage binary counter (IC2) to obtain the four binary control frequencies of 19.2 kHz, 9.6 kHz, 4.8 kHz, and 2.4 kHz. For a gyro, it is also possible to use the 4.8 kHz output to drive a divide-by-6 counter and obtain a 3-phase output, 800 Hz, synchronized signal for the spin-motor power supply.

The four binary control frequencies feed two CD4028 BCD-to-decimal decoder circuits, IC3 and IC4, with these two units arranged in a 4-bit BCD to hexadecimal conversion circuit.[5] The output from pin 3 of IC4 is thus the "0" hexadecimal pulse, 26.04 microseconds wide, occurring once every 416.64 μsec, or at a rate of 2.4 kHz, the basic system interrogation frequency, f_i. Similarly, the output from pin 4 of IC3 is the "15" pulse, again 26.04 μsec wide, and at system rate of f_i.

During evaluation of CMOS components from several manufacturers it was found that often a fast 'race' pulse (less than 50 nsec wide) occurred in these outputs, due probably to unequal time delays though the parallel-sequenced data buses internal to the CD4028 chip. This 'race' pulse would produce a reset of the ramp circuitry if it occurred on the "15" pulse line, hence it had to be eliminated. Various experiments indicated these effects could most often be eliminated by addition of extra time delay in the 19.2 kHz line for IC4 and the 9.6 kHz line feeding IC3, and was most easily accomplished by adding two series 20 K-ohm resistors, R1 and R2. Even with these additions, it was found that experimental selection of IC3 and IC4 was required.

The basic data clock frequency is 614.4 kHz and is obtained by the NAND operation of the 1.2288 MHz and the 614.4 kHz frequencies. This produces an

output pulse from IC8C that is high for 0.4 μsec and low for 1.22 μsec. Thus, in the basic interrogation frequency interval of 1/2.4 kHz (416.67 μsec), there are 256 data pulse intervals. Hence the '0' and '15' pulse outputs from IC3 and IC4 occupy the first 16 and last 16 data pulse intervals, 0-15 and 241-256, respectively.

Ramp Generator - Duty Cycle Generator. The analog-to-digital conversion process for the width-modulated binary rebalance electronics loop is accomplished by comparing the amplified error signal output from the ESP to a linear ramp voltage from IC9, and determining the time-of-crossing by a comparator amplifier IC10A.

The ramp voltage is obtained by charging a capacitor C2 with a current source of 0.1 mA, obtained by Q1A, Q1B, and resistors R3-R5. The unity-gain follower IC9 acts as a high-impedance input buffer, so that the output voltage from IC9 is a voltage, increasing linearly with time at the rate of 0.01V/μsec. The ramp is reset once every interrogation period by the 241-256 pulse from IC3. Thus, the charge is removed from C2 through the 'ON' resistance of Q2 during this 26 μsec interval. It was necessary to use a mylar capacitor for C2, since the peak discharge current of the capacitor can be greater than 100 mA, which can cause a non-linear dielectric effect if a normal ceramic capacitor is used for C2.

The comparator amplifier IC10A is a quad unit, the LM339. The reset Q-15 and 241-256 pulses are also mixed at the comparator input, with appropriate division in relation to the ramp and the error signal, so that whenever the 0-15 reset pulse is present, the output of the comparator IC10A will be low (0 volts), regardless of the amplitude of either the error signal or the ramp within an interval of $\pm$ 15 volts. Similarly, whenever the 241-256 reset pulse

is present the output of IC10A will be high (+15V), regardless of the other signals. This process ensures that the torque signal will always be applied for at least 16 data pulses (26 μsec), regardless of whether the torque is positive or negative.

It has recently occurred to us that the same blanking operation obtained in the comparator can be implemented in a much better fashion by letting the 0-15 pulse drive the reset line of the following CD4027 J-K Flip-Flop IC5B, and use the 241-256 pulse to drive the set line of IC5B. Thus, noise pickup and pulse coupling on the input lines to the IC10A comparator, that can cause a jump in the output level of the comparator and hence a jump in the output data, could be easily filtered out. This would eliminate the present signal mixing by resistors R19 and R23. It is intended that future versions of the DCE incorporate this improvement.

The present use of the comparator IC10A and the mixing process replaces the use of a mixer op-amp and a quad NAND-gate comparator utilized in the Hamilton-Standard logic, and our earlier TTL design. In attempting to implement this latter type of duty cycle generator with CMOS logic, it was found that the slow rise-time of the signal from the mixer op-amp (.01V/μsec) produced a condition where both the p- and n-channel MOS transistors in the CD4011 NAND gate comparator were in the 'ON' condition for a long time, which produced drain currents of >10 mA during this period. Indeed, further checking disclosed maximum pulse rise-times for a switching function in CMOS to be rated at 0.5V/μsec. Further, by the use of the LM339 for both mixing and comparison, we utilize one chip versus six chips required for the previous TTL duty cycle generator design for a three-axis system.

Data-Torque Generator. The output pulse from the IC10A mixer-comparator drives a CD4027 J-K Flip-Flop (IC5B) that is clocked by the 614.4 kHz data clock. The output of IC5B is thus a pulse whose width is directly proportional to the crossing of the error signal and the ramp, and at the interrogation frequency f_i of 2.4 kHz. For zero pulse rebalance condition the duty cycle of this torque pulse is 50%, indicating an equal positive and negative torque current to the inertial sensor. A net positive or negative torque is then a duty cycle of either greater than or less than 50%.

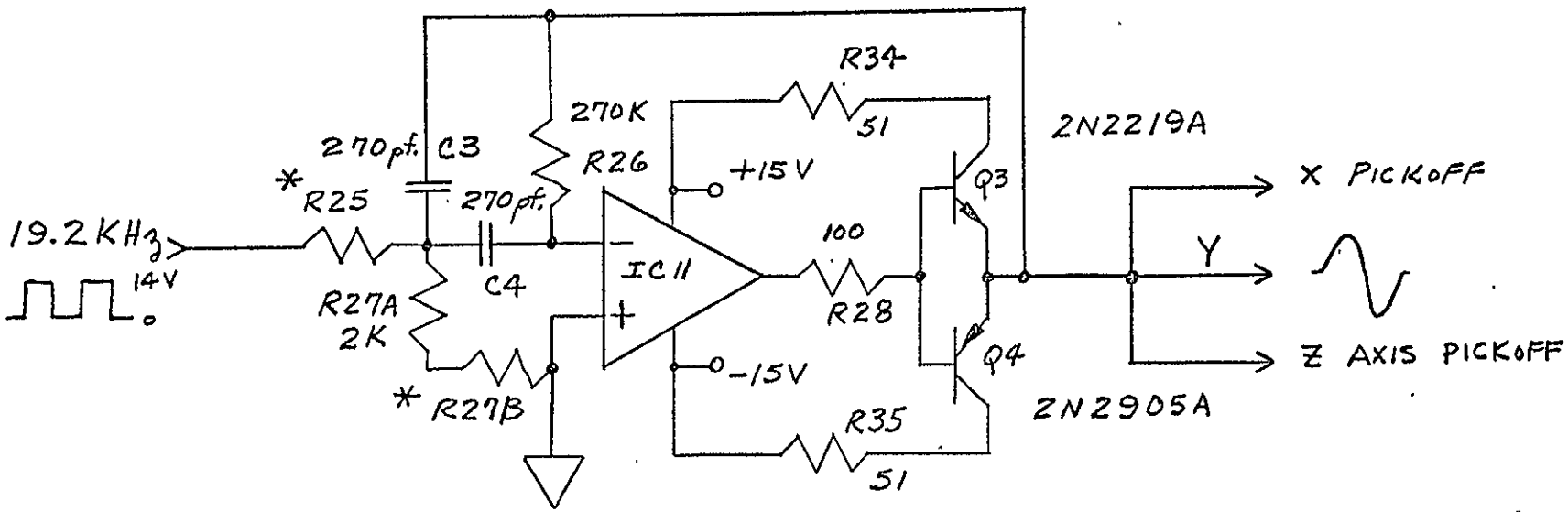
The output of IC5B is applied, along with the 614.4 kHz clock, to a NAND gate, IC8B. The output of IC8B is thus a series of pulses, whose total count is directly proportional to the amount of positive, or negative, torque applied to the torquer coil of the inertial sensor. In order to drive a possibly large capacitive load the IC12C (CD4050) buffer is added to interface the data. An output count of 614,400/2, or 307,200 pps, would be indicative of a 50% duty cycle for the torque signal out, or zero net torque to the inertial sensor. The largest positive (or negative) torque would occur for a count of (256-16) x 2400, or 576,000 pps; while the largest negative (or positive) torque would occur for a count of 16 x 2400, or 38,400 pps.

Other logic outputs are (1) the signal to feed the synchronous demodulator, which is the 19.2 kHz output from IC2, and interfaced by IC6E, a CD4049 driver, and (2) the same 19.2 kHz signal to convert to a sine-wave for the pickoff signal generator, and (3) the 241-256 blanking pulse, interfaced by an IC12-CD4050 driver, to act as a 2.4 kHz clock for telemetry purposes.

Sinusoidal Signal Generator. The sine wave drive signal to the pickoff input for the inertial sensor is obtained by feeding the 19.2 kHz output square wave from IC2 through an RC bandpass filter. The circuit is shown in Figure

13 and is the same RC active filter used previously in the ESP design. In order to produce a smoothed sine-wave output from the square-wave input signal, it is necessary to increase the Q over the design used for the ESP. For the circuit of Figure 4.6, the Q is equal to 4.5. For 4.5V rms output the value of R25 is equal to 150 k-ohms, while for the DDH experiment the value is reduced to 470 k-ohms for 1.5V rms output. Resistor R27B is adjusted to align the zero crossing of the sine-wave with the pulse edge of the 19.2 kHz signal in, thereby producing minimum phase shift.

To increase the output drive power, Q3 and Q4 are connected as Class B complementary emitter followers.



* R25 SELECTED FOR GAIN REQUIREMENTS. R27B SELECTED FOR MINIMUM PHASE SHIFT (NOM. R27B = 820-OHM)

IC 11 IS AN MC 1741S.

Figure 13. Signal Generator.

CHAPTER V

SYSTEM BRASSBOARD EVALUATION

A number of tests were performed to check for proper operation of each brassboard system. These inspections and measurements are discussed and results presented in this chapter. More precise measurements (accuracy, stability, etc.) have been or will be performed by the MSFC staff in their well equipped inertial sensor test laboratory. Some of the preliminary MSFC results are also published in this chapter.

Checkout for Proper Operation

A careful inspection of certain key signals in the rebalance loop is essential to determine proper loop operation. Although a loop may be stable and appear to be operating properly, certain malfunctions may actually exist but become evident only for some specific operating (or rate) situation. An educated inspection with the oscilloscope of some key loop signals usually will reveal the improper operation.

Inspection of Loop Signals. The ramp signal of the duty cycle generator at R16 of Figure 12 was inspected for linearity, voltage levels (≈ 0 to +4 volts) and extraneous noise. The ramp signal normally has a considerable amount of data train pickup which does not impair the operation of the duty cycle generator. Other pickup signals may cause improper firing of the comparator (IC10, Figure 12); this can be checked by applying a slow ramp signal to the error signal input to IC10 and checking for pulse "jumps" in the data train.

The blanking signals at R19 and R20 of Figure 12 were inspected for proper width (16 data pulses), rise time (<< 1 data pulse width), amplitude (≈ 15V), and absense of "race" spikes. The race spikes were present in several systems and were eliminated by proper selection of the CD4028 CMOS chips. The race problem was discussed in Chapter IV.

The data pulse (IC12, Figure 12) was at a voltage level of approximately 14 volts for 1.22 μsec. The data pulse 10-90% rise and fall times were less than 50 nsec. Data pulse splatter was inspected to obtain a qualitative measure of system uncertainty. Data pulse splatter was much less than one data pulse for all the rebalance loops.

Four key signals in the ESP (Figure 8) were inspected: the preamplifier output, the ac amplifier output, the synchronous demodulator output, and the ESP output to the DCE. The preamplifier output signal was inspected while the inertial mass was moved over its entire range to confirm that the preamplifier would never saturate. The ac amplifier output was inspected to confirm that (1) the quadrature signal was sufficiently low, (2) the linear-signal phase-shift was negligible, and (3) that phase shift under all overload conditions was small enough to maintain loop stability against oscillations and latchup.

For the condition of zero input to the ESP (input short circuited), the dc level at the output of the ESP was checked by viewing the data train (IC12, Figure 12). The dc level was adjusted to set the data train to the zero torque position by varying R15, Figure 8. This quiescent dc level at the ESP output should be about 2V.

The torque current pulse was inspected by observing the voltage pulse across the compensated torquer with a dual channel oscilloscope set for an

ac differential measurement. This pulse was observed to confirm proper compensation and torque current level.

Checkout Measurements. The closed loop response was measured for all axes in all systems. The output signal of a function generator was connected through a resistor with value in the range 62K - 100K to the junction of R13 and R10 at the comparator input (IC10, Figure 12) and the resulting closed-loop response signal was observed with an oscilloscope at the output of the ESP. This technique permits the measurement of system response for a variety of input signals such as sinusoids, square waves, etc. With a sinusoidal input, the 3 dB closed-loop frequency response was measured and found to be in the range 2.5 - 3.5 Hz (design value = 3 Hz) for the 2412 loops, 11 Hz (design value = 10 Hz) for the GG334 loop, and 7.5 - 8 Hz (design value = 10 Hz) for the 2401-009 loop. The midband signal at the ESP output was set at 1V peak-to-peak for this measurement.

The original design gain of K_{pc} = 146,000 for the 2412 loop (Table II) was found experimentally to be too high to give the 3 Hz design closed-loop bandwidth. Consequently, the gain K_{pc} was lowered to 41,000 to obtain f_{cl} = 3 Hz. The ESP parameter values in Table III are for K_{pc} = 41,000. We suspect that the discrepancy in the gain values was due to an incorrect inertial sensor parameter, perhaps the value of F, the damping coefficient.

The overshoot in the step response was in the range 0-10% for the 2412 loops, 25% for the GG334C loop, and 35-60% for the 2401-009 loops. The unexpected high overshoot for the 2401-009 loops has not yet been explained; however, each axis of all three systems was checked for adequate gain margin by raising the ESP gain (lower the value of R6, Figure 8). The design gain margin of about 32 dB was experimentally confirmed in all cases.

With the signal generator fully loaded, the supply current was measured for each axis. There was little difference among the current values for each specific system. The nominal current values for a single axis rebalance loop was +68 mA, -44 mA for the 2412 loops; +55 mA, -25 mA for the GG334C loop; and +165 mA, -47 mA for the 2401-009 loops.

The data pulse uncertainty per interrogation period was estimated by viewing the data splatter. This uncertainty for all axes of all the systems was less than 0.1 data pulse.

Some Important Experimental Measurements

There have been several initial tests performed on the various systems delivered during this contract period, concerning the overall accuracy and stability of the data. In Figure 14 are presented data indicating the experimentally measured error for one axis of a Zero Gravity Experiment brassboard system utilizing the Kearfott 2412 accelerometer. The data was obtained by MSFC personnel utilizing a laser interferometer for angular measurement. It can be seen that the observable error is less than 10 μg for either positive or negative torque, up to the full-scale g-input range of 1/30 g, for this particular accelerometer.

In Figures 15 and 16 experimental data is shown for the output data counts for one axis each of two of the brassboard systems delivered for the DDH Experiment. This data was taken at U.T.K. using a Kearfott 2401-009 accelerometer, cushioned and positioned horizontally on a laboratory table. There were undoubtedly small local acceleration transients which are included in the data, and hence the spread in data counts should be somewhat pessimistic. The data presents both 1 sec. and 10 sec. count intervals, for the DDH brassboard that had the largest observed variation (DDH1-Y axis), and

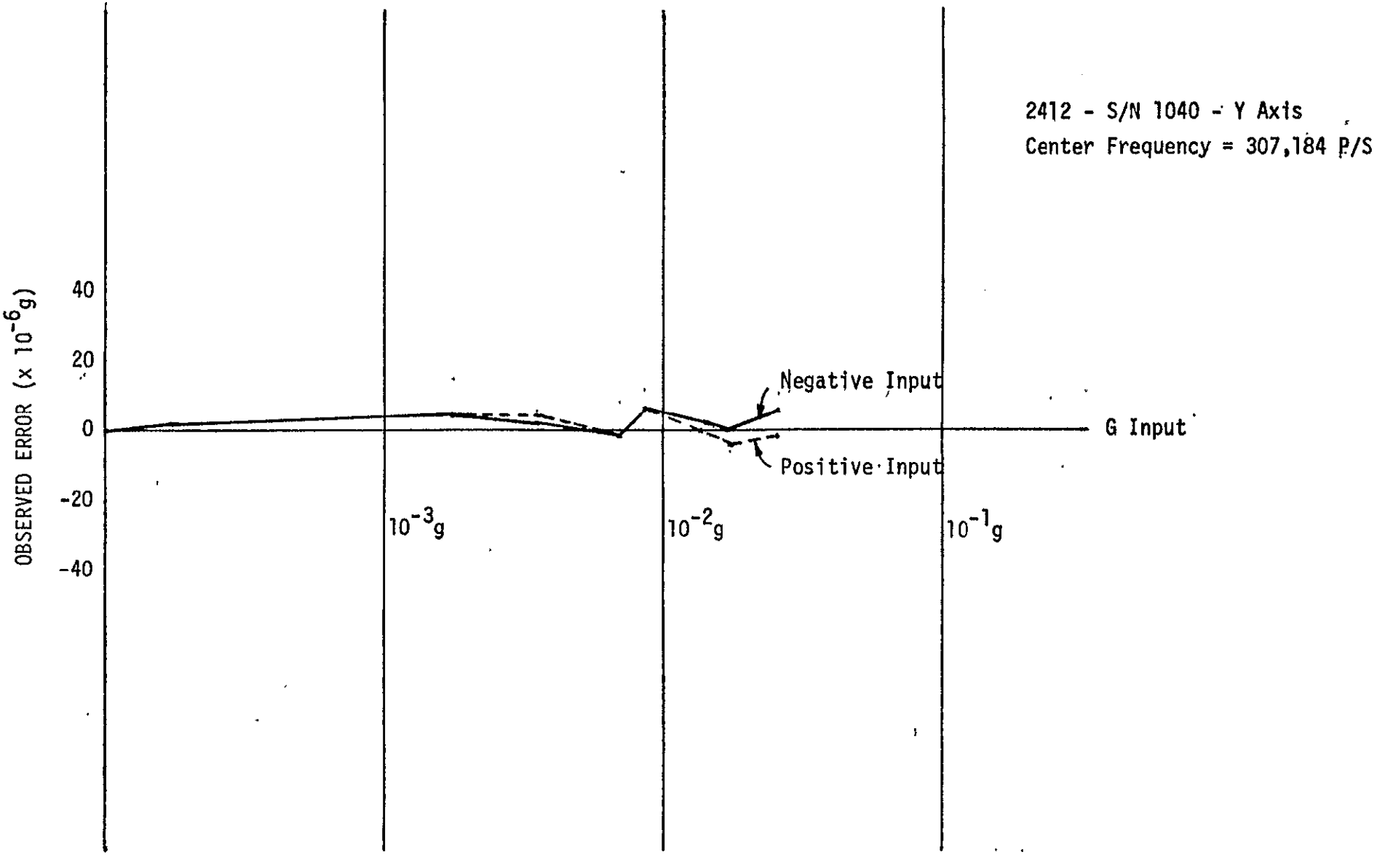


Figure 14. Experimentally Measured Error for One Axis of O-G Brassboard System.

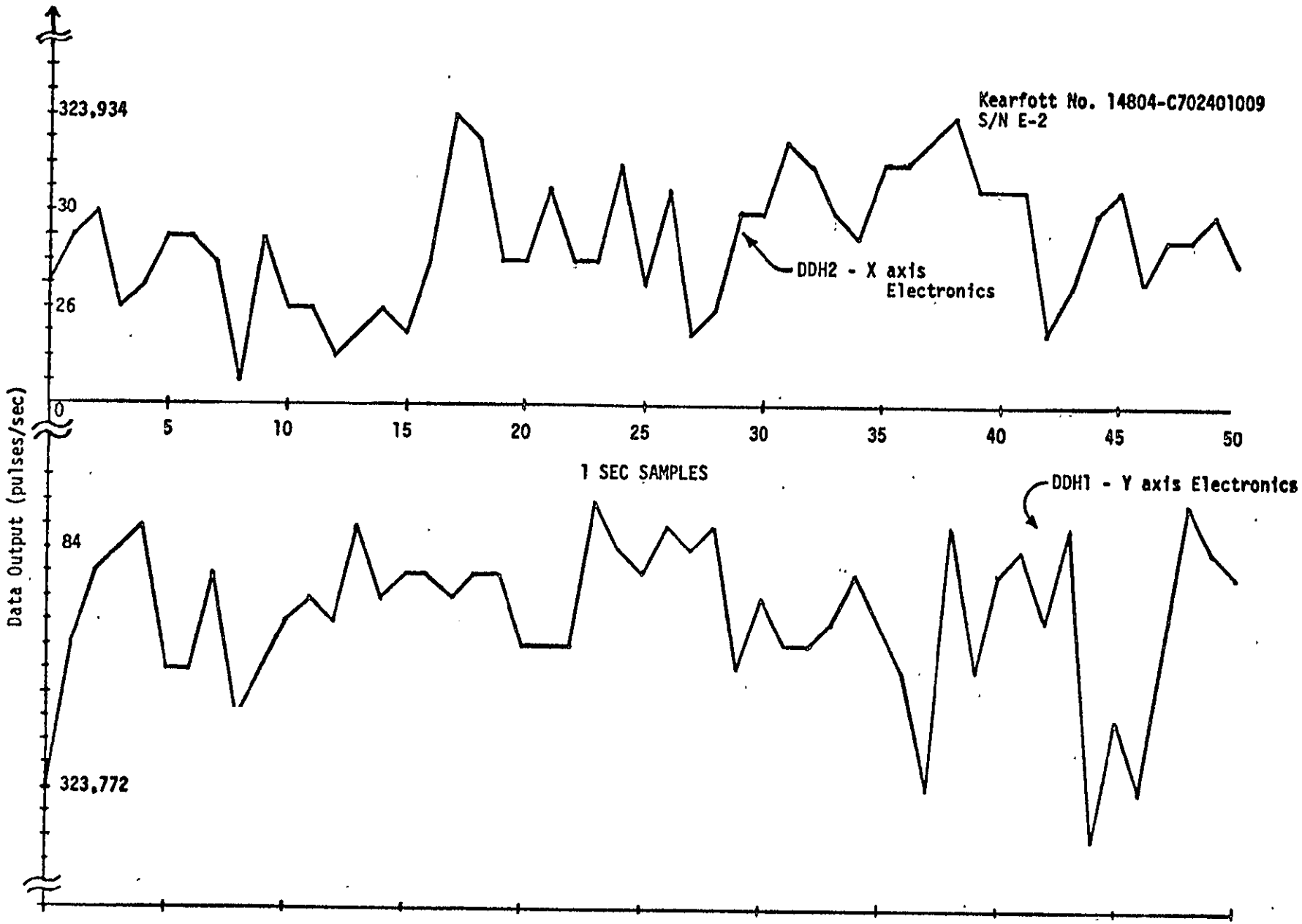


Figure 15. Output 1-Second Data for Two DDH System Axes with Zero Acceleration Input.

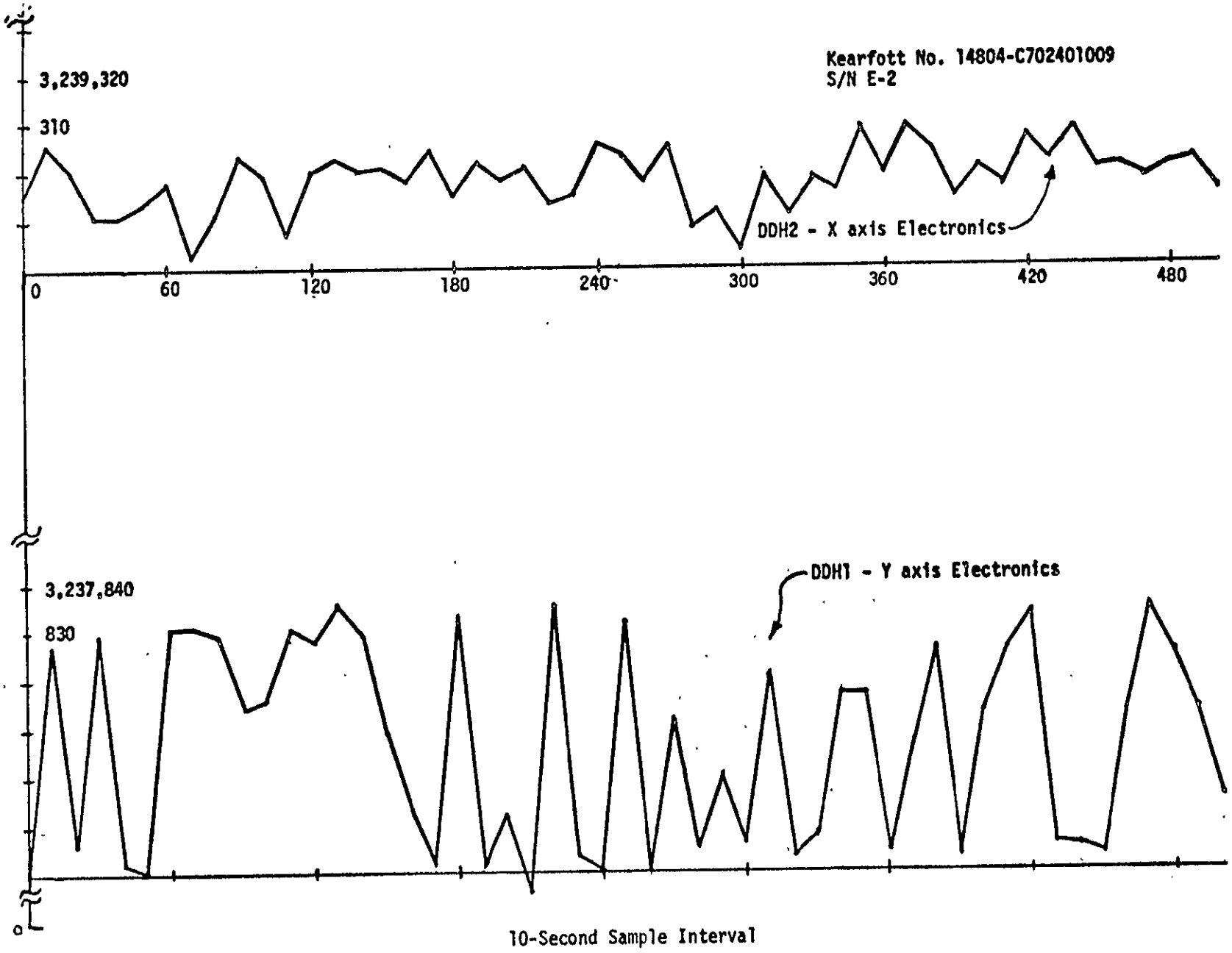


Figure 16. Output 10-Second Data for Two DDH System Axes, with Zero Acceleration Input.

for the brassboard system having the least observed variation (DDH2-X axis). The standard deviations for the data of Figures 15 and 16 are the following: the DDH1-Y axis, σ(1-sec) = 3.56 counts (11 ppm), and σ(10-sec) = 20.9 counts (6.5 ppm); the DDH2-X axis, σ(1-sec) = 2.65 counts (8.2 ppm) and σ(10-sec) = 6.1 counts (1.9 ppm). The data of these figures appears random in nature.

Some Unresolved Uncertainties

For a pulse rebalance loop there appear to be minute variations in the data output counts that are not attributable to random noise limits of the ESP. In some instances these variations appear almost cyclic in nature, with a period dependent upon the observation time of the counter. These variations are typically less than $\pm$ 30 ppm deviations, and for most instances are less than $\pm$ 20 ppm deviations.

We have not had sufficient time to investigate this phenomenon fully, but it appears to be mostly attributable to variations in the DCE itself, since for a constant input level to the DCE, in an open-loop condition, we found that output data shows a 2 to 5 count spread, for 1-sec sample intervals.

REFERENCES

1. T. V. Blalock, E. J. Kennedy, and R. D. McKnight, "Development of a Width-Modulated Pulse Rebalance Electronics Loop for Strapdown Gyroscopes", Scientific Report S-25, Department of Electrical Engineering, University of Tennessee, July 13, 1973.

2. R. D. McKnight, T. V. Blalock, and E. J. Kennedy, "Design of a Torque Current Generator for Strapdown Gyroscopes", Technical Report TR-EE/EL-1, Electrical Engineering Department, University of Tennessee, August 1, 1974

3. Kenneth Rush, "Development of a Low-Noise, High CMRR Instrumentation Amplifier", M.S. Thesis, University of Tennessee, To be published.

4. G. E. Tobey, J. G. Graeme, L. P. Huelsman, Editors. Operational Amplifiers, Design and Application, Burr-Brown Research Corporation, McGraw Hill Book Company, 1971.

5. RCA 1974 COS/MOS Data Book SSD-203B, p. 145, RCA Corporation, Somerville, N.J., November, 1973.