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CONCEPT STUDY PHASE I REPORT

FUTURE APPLICATIONS OF ASSOCIATIVE PROCESSOR SYSTEMS TO OPERATIONAL KSC SYSTEMS FOR OPTIMIZING COST AND ENHANCING PERFORMANCE CHARACTERISTICS

PREPARED FOR
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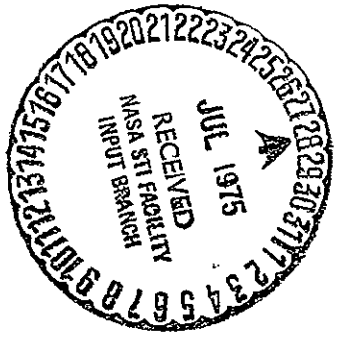

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FOREWARD

A new computer technology has risen with performance capabilities beyond any imaginable objectives attainable by the conventional computer. The internal memory operation in conventional computers limits them to doing only one operation at a time, but newly developed memory addressing techniques allow thousands of operations to be performed simultaneously.

The benefits of such technology would provide a whole new way of thinking for approaching space vehicle checkout. This new technology will allow literally thousands of parameters to be checked for out-of-tolerance conditions simultaneously or thousands of arithmetic computations to be performed within one memory machine cycle. The capability for a simultaneous total space vehicle instant status sampling of all subsystems is now a reality. It is no longer necessary to rely on conventional concepts where subsystem routines are stationed in software loops waiting for servicing by the conventional computer. Now it can be done all at once, no subsystem has to wait for a loop in a sequential manner; instead, all subsystems can operate in a parallel concept.

The application of associative memory technology to launch vehicle testing and Space Shuttle checkout could reduce checkout time. Associative parallel processors of the types employed by the Safeguard Systems for the Advanced Ballistic Missile Defense Agency, or being tested by the FAA for future air traffic control, are capable of handling bulk data processing in single operation cycles, while conventional sequential processors can only handle a single data quantity in a single cycle This feature of associative parallel processors can find application to processing data bases in which a large percentage of the data is of a like nature, such as a discrete event or digital quantities conveying like-measurement information such as voltage and current levels. The KSC launch vehicle and shuttle systems have a high percentage of data which is in the bulk category. The application of a parallel processor using associative addressing (content addressed) provides a high throughput capability (effective number of instructions executed per second) for processing operations of identical nature A tradeoff between use of sequential processors and associative parallel processors would enhance the speed in

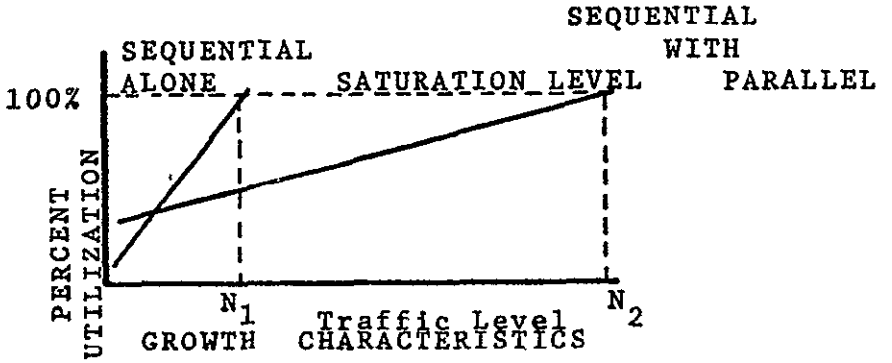


FIGURE 1

KSC checkout operations and extend the growth capabilities of the overall checkout system - reference Figure 1. The associative memory technology also provides a computer concept capable of satisfying the simultaneous multi-processing requirements of acoustic voice analysis, payload systems, aerial topographic analysis, digital analysis, communication multiplexing and fast searches of a rapidly changing large data base such as the KSC Launch Processor System data base.

1.1 PURPOSE

The purpose of this study is to demonstrate the application of associative memory processor equipment in relieving the task burden done by conventional host processor type equipment and demonstrate how it would enhance system efficiency and speed. This includes comparative theoretical performance analysis, showing expanded growth capabilities, demonstration of actual hardware in a simulated environment and a recommended new technology applications document related to KSC Operational Systems. This is the first report of three study phases which are described in the following study approach.

1.2 APPROACH

1 2.1 Concept Study Phase

This study phase is to perform documentation searches, explain operational characteristics, identify other Government and industry installations which have

successfully utilized the new technology for application in environment similar to those found at KSC.

1.2.2 Development Phase

This study phase is to identify actual hardware systems available and analysis of specific hardware systems through contacts and travel to other agencies. It should define demonstration requirements for a simulated environment and implementation of required hardware It should show the obvious gains and potential gains (maximum and minimum) with various levels of tradeoff with concepts which are in current planning at KSC.

1.2 3 Demonstration Phase

This study phase is for the demonstration of a system in a simulated environment under typically worst case conditions comparing the performance characteristics with conventional sequential systems. The results will be to ultimately provide design reference documentation involving commercially available operational type hardware for a parallel associative processor as a support system to candidate host hardware in KSC operational areas. Each Phase will be covered by a published interim report to stimulate interest in the new technology and to supply critical information to potential users with application requirements

1 3 HISTORY

Since writing the proposal for this study a number of available library documents have been reviewed and additional information solicited from industry sources. The following comment is a review of how this particular study effort got started. A report on the extent of Digital Computer Monitoring and Control in other areas outside NASA was requested of the writer in the spring of 1973. In the course of the ensuing investigation to cover all possible uses of Digital Computer Control Technology, information indicative to basic system architecture and design appeared to show much similarity among different control systems scattered throughout the United States These obvious similarities were manifest in data handling, processing,and control techniques utilizing time shared or multi-programmed mainframes which were basically general purpose machines programmed to share the computers resources among a number of operational job activities which are concomitantly resident in the main memory storage of the computer. The problems and limitations appeared to be a common condition in that the ability of the central system to communicate with time shared remote terminals or subsystems depends on the gross amount of data being processed at any given time regardless of data similarities. All manner of tricks and devices were utilized in efforts to get around overload situations with these essentially sequential (process only one parameter at a time) machines. Such elaborate schemes

as remote programmed control terminals with core memory for temporary storage, fast recall auxiliary disc or memory storage, multi-CDU systems with partitioned memory and multiprogrammed systems[1] all were par for the course

In the search for this information, some interesting material was uncovered in the air traffic control area The FAA has recognized the shortcomings of the sequential mainframe systems and invested in a new technology which the United States Air Force was developing under contract The system was reported in technical journals by personnel from various industry sources such as Bell Laboratories, Minneapolis-Honeywell, and Goodyear Aerospace Corporation For readers desiring references, a list is included in the Appendix The government agencies extensively involved in this technology are Rome Air Development Center, Rome, N. Y , Safe Guard Systems Office, Washington, D. C , Army Ballistic Missile Agency, Huntsville, Alabama, and the Air Force Materials Laboratory, Wright-Patterson Air Force Base, Dayton, Ohio. The new technology is a deviation from the use of conventional computer architecture The internal memory operation in conventional computers limits them to doing only one operation at a time, but this new technology allows thousands of operations to be performed simultaneously

The benefits of such technology would provide a new approach to computerized space vehicle checkout. This new technology will allow literally thousands of parameters to be processed simultaneously within one machine memory cycle. The capability for simultaneous instant parameter sampling and processing for all subsystems becomes a reality.

2.0 DEFINITION OF ASSOCIATIVE PROCESSING

The concept is called Associative Addressed Memory Processing. With this architecture concept, it is not necessary for subsystem routines to sequentially process each individual parameter to achieve results Under this concept, all parameters with a common relationship regardless of the subsystem or quantity can be simultaneously processed within one machine cycle. What this means in terms of actual operations is that iteration time spent in the mainframe executive loop is not a function of the gross quantity of data traffic that requires processing Such tasks which under conventional architecture consume large fractions of the loop time can be radically reduced in time utilized which frees the system for servicing the functioning subsystems This would, in effect, allow the central mainframe to become operationally transparent to the functioning subsystems and control terminals An explanation

of the conceptual differences between a conventional memory addressing scheme and the associative memory addressing scheme would be appropriate at this point for the reader. In conventional systems, the memory address information is reduced through address decoder logic to a single word location in memory. Information is either read out or written into the specified memory location through bit parallel buffer registers All data leaving or entering the memory array passes through the memory buffer registers in parallel one word at a time during each memory cycle. This location addressed scheme limits the conventional sequential machine to only a single memory word operation in a given memory cycle. Thus, to process the total word content in the memory array requires an equal number of conventional sequential machine memory cycles. In the conventional system, information is handled by processing elements one word at a time which is located in a specified memory location within the array Innovations to improve the high speed data processing characteristics of the sequential system were initiated such as multiple processing elements communicating with a common memory. The memory was partitioned to allow the processing elements to operate in parallel with selected banks of the memory. Such innovations (refer to Figure 2) brought the super computer concepts into being. The number of data words processed over a given time period is a function of the

number of processing elements and dependent on whether processing requires data from the same memory bank which causes memory queing delays while one processing element waits upon another To accomplish high-speed processing of large rapidly changing data bases, a very real limitation exists in sequential location addressed memory systems to process any more than a few arithmetic operations simultaneously

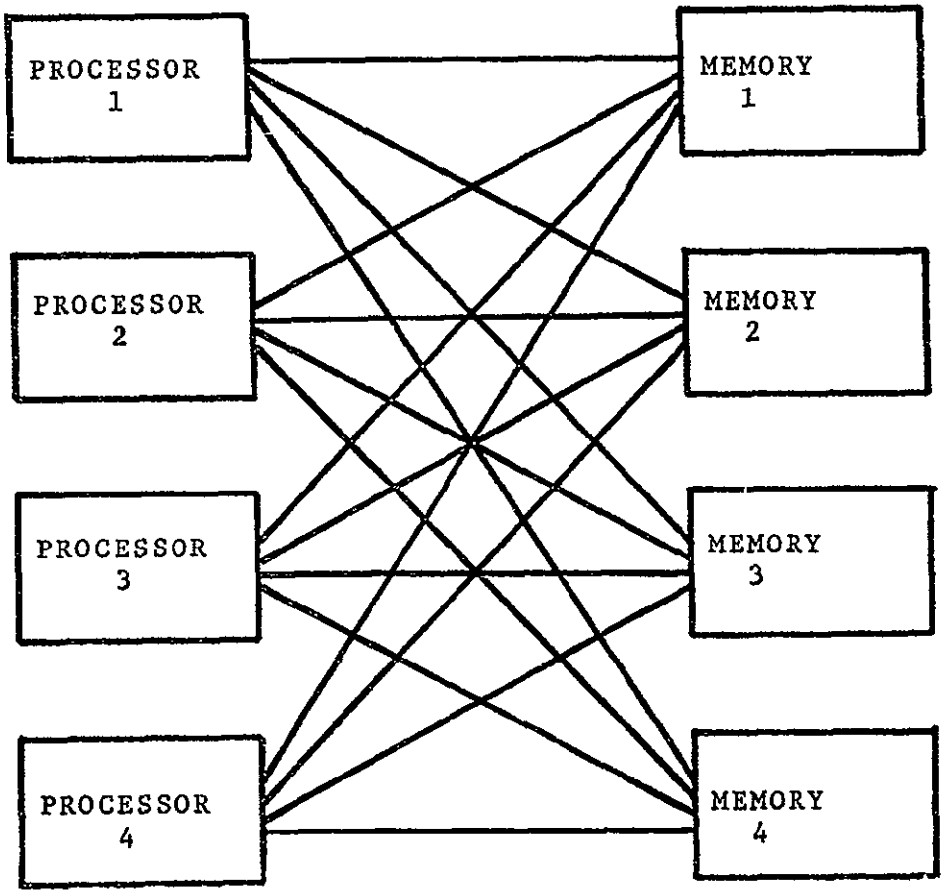


FIGURE 2

3 0 SYSTEM ARCHITECTURE

The description of solid state associative memory technology was not possible due to proprietary patent litigation by the corporate source being in process. The following description applies to a plated wire concept This information was more readily available from literature sources although it has now been outmoded with recent solid state architecture. For the introductory intent of this article, it will suffice to explain the basic principals to the reader With the preceeding basic sequential system characteristics in mind, the reader is now given the associative memory processor characteristics. In the associative addressed memory, address information is contained within the bit contents of each word stored in memory - they may also be considered as word identifier address bits. The retrieval of words from memory involves a search to match the word content address bits with search address identifier instruction bits When the interrogation drivers stimulate the bits along the plated wire memory lines (refer to Figure 3) the resulting bit output information is sensed by the response store logic at the end of each plated wire memory line. The response store logic responders are attached on a one-to-one basis to each plated wire Each responder operates serially by bit on the data as it is pulsed out of the plated wires by the interrogation driver logic. All the

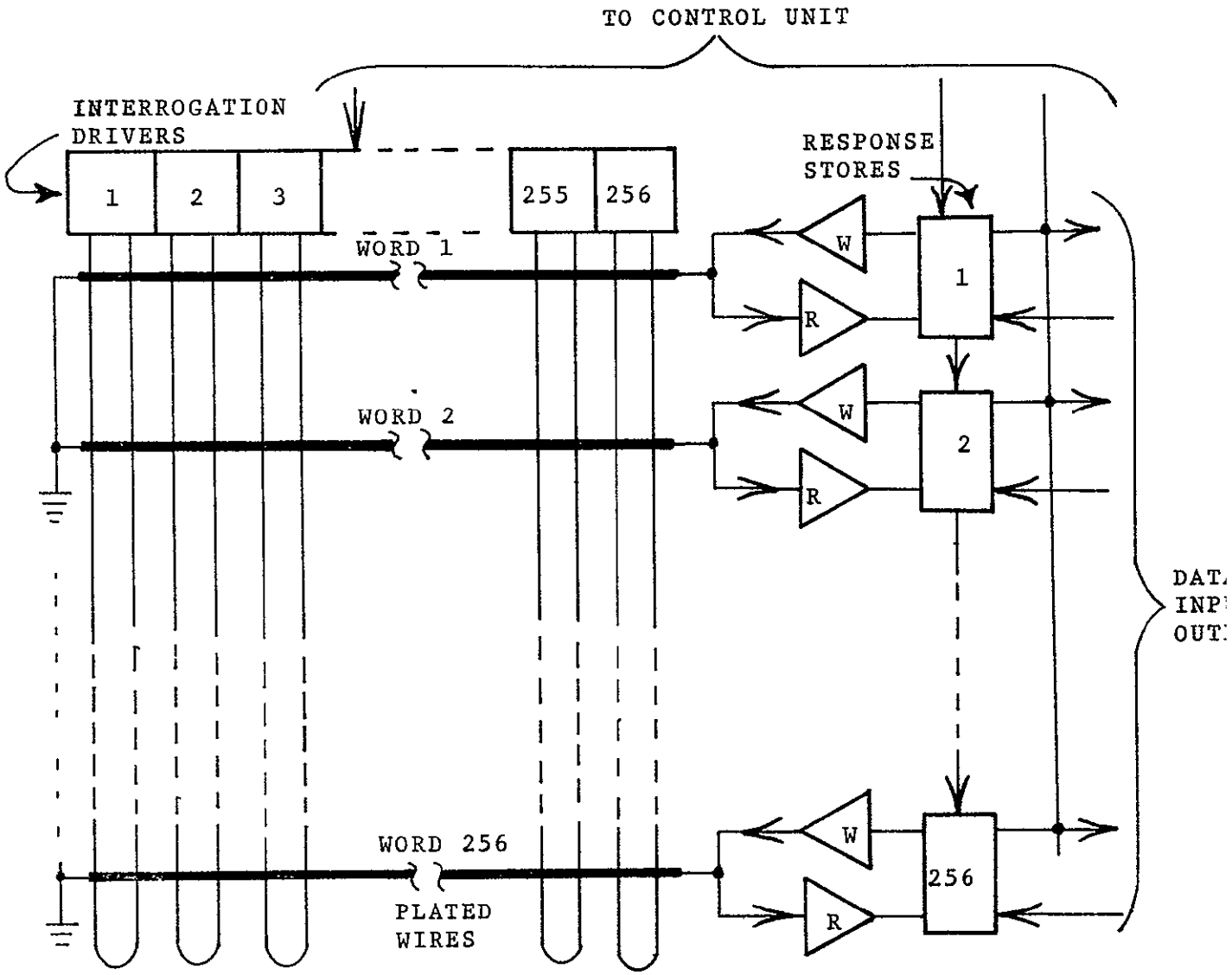

TO CONTROL UNIT
INTERROGATION DRIVERS
1
2
3
255
256
RESPONSE STORES
WORD 1
WORD 2
WORD 256
W
R
1
2
256
PLATED WIRES
DAT
INP
OUT

FIGURE 3

individual responders simultaneously execute the same instruction being sent from the control unit. Only the desired word or words with the correct identifier bits will respond to the instruction, this being accomplished by the responder logic operations Individual responders act as an arithmetic unit attached to a one word memory, effectively, the equivalent of many one word memory digital processors all operating in parallel During a single instruction cycle from the control unit, the data bit information from every word in the plated wires can be simultaneously processed in parallel by associated responder logic. The time required for the total memory processing is equal to the time for processing a single plated wire word While words in the conventional memory are only 12 to 48 bits long, words in the associative array, are likely to be hundreds of bits long. The lengthy words can be divided into subwords under program control Because the words are readout of memory in a serial bit manner, the instruction cycle is considerable longer in terms of single word processing when compared to a conventional machine memory operation which reads words bit parallel. When compared to a conventional machine operation time for performing a bulk word memory processing operation, the conventional machine goes out of favor because only single word processing per instruction is possible with the

conventional machine while the associative memory machine can process all words in memory per slightly longer instruction time. To better explain this point, an example follows Consider a highspeed 0.5 micro sec cycle time conventional machine processing all word bits in parallel that can retrieve and add two 24 bit words and store the sum in approximately 3 micro sec. An associative processor machine with equivalent speed logic processing in word serial bit parallel would take 28 micro sec to do the same thing. On the other hand, if 3,000 word pairs were to be added together, the associative processor would <u>still</u> take 28 micro sec, whereas, the conventional machine would take 9,000 micro sec

The ability of the associative processor to execute a single instruction simultaneously on many data words eliminates the need for most program loops found in conventional systems which must repeat loop instructions to process distributed data locations Because associative memory modules do not use conventional location addressing, they can operate in parallel under a common control logic with each module responding to the same instruction sequence This feature makes memory expansion a simple problem limited by hardware physical factors only without any reflected additional software requirements. The software does not concern itself with where information is

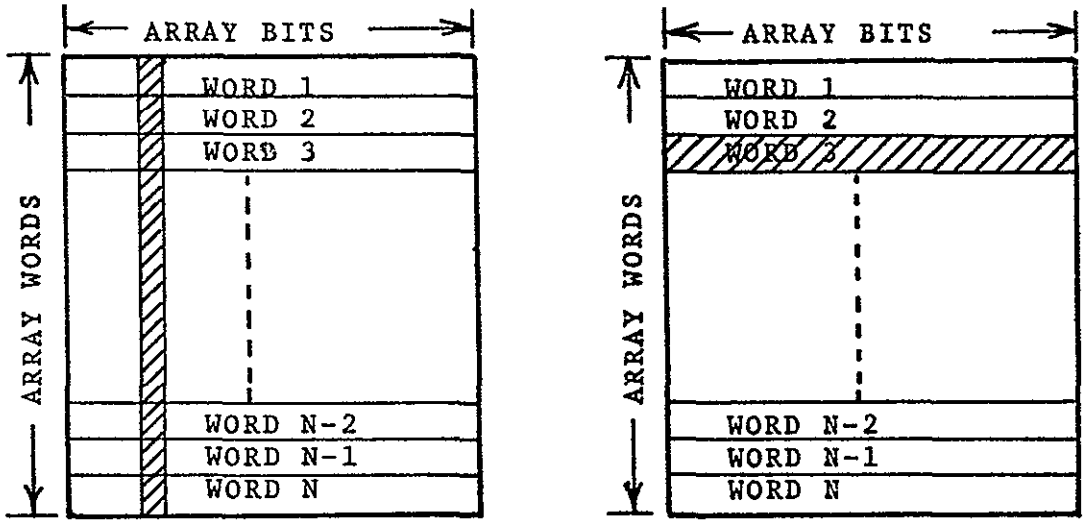
located because it communicates with all memory elements simultaneously, therefore, it is independent of the size or number of memory elements (expansion) of the system Since the physical location of information in memory is not important, then completely unrelated classes and types of data can be stored in the same memory module This creates freedom from adherence to a designated memory map for particular information quantities which conventional systems are bound to.

The preceeding discussion covered a brief introduction and some advantages of associative processing The following discussion will review some operational hardware concepts which are available for applications from industry The concepts delineated in reference literature define the typical associative memory architecture as follows

The heart of the system is the associative memory array which has multi-dimensional access. A simple explanation of this is described pictorially by the diagram in Figure 4 as a bit slice access across the word axis or along the word axis. The interrogation or communication of the array occurs as one bit from many parallel stored words (bit slice) or all the bits serially stored along a single word or words (word slice).

Data in the memory are addressed by means of the contents or some property of the contents. Each word of memory is broken into variable sized groups of bits called fields (refer to Figure 5)

These fields do not have to be made up of adjacent sets of bits although customary practice is to do so The access mode bus selects a stencil pattern of word length bits to select the field or fields desired for communications. The address bus can position the stencil in memory to select the word or words for desired communication. The access bus selects a stencil pattern as follows.



BIT SLICE ACCESS WORD SLICE ACCESS

FIGURE 4

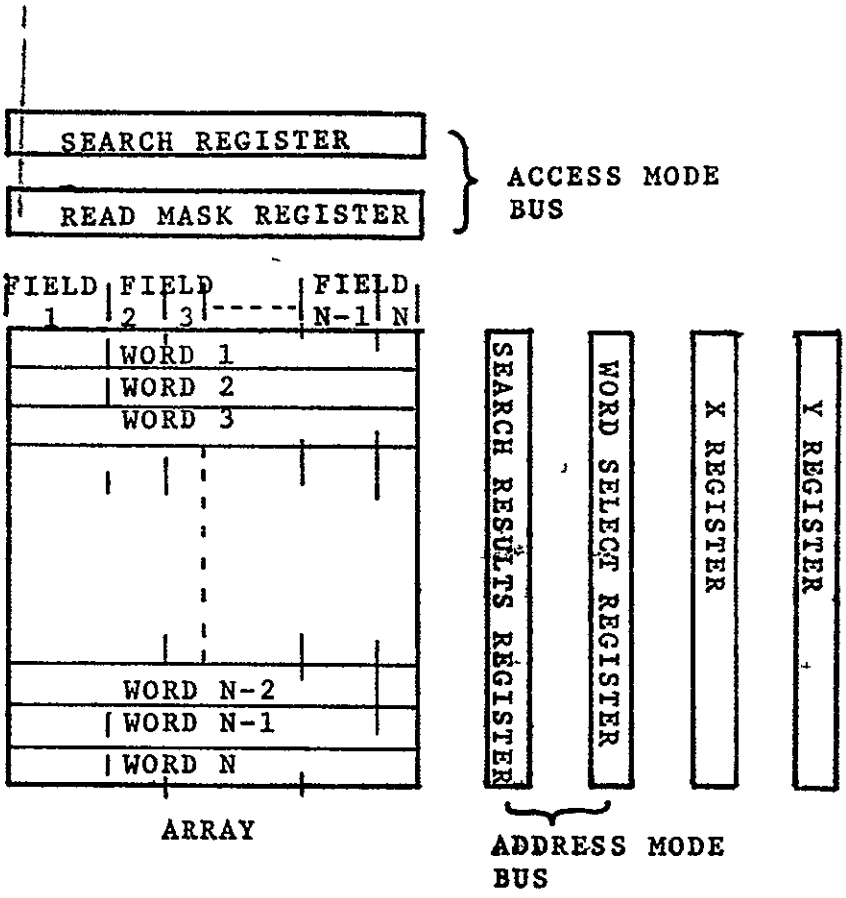

SEARCH REGISTER
READ MASK REGISTER
ACCESS MODE BUS
FIELD 1
FIELD 2
3
FIELD N-1
N
WORD 1
WORD 2
WORD 3
WORD N-2
WORD N-1
WORD N
ARRAY
SEARCH RESULTS REGISTER
WORD SELECT REGISTER
X REGISTER
Y REGISTER
ADDRESS MODE BUS

FIGURE 5

The search register receives an externally supplied word from the control unit This word has a relation to words that are contained in memory. The read mask register receives a designated pattern which identifies the bit positions or fields to be allowed in the search. The address bus selects the word or words to be communicated with as follows The word select register receives a designated pattern which selects the word or words to be communicated with The search results register stores a stencil of the words in memory that respond to the associative memory search using the relationships allowed by the read mask register, search register, and word select register. The array module has parallel processing elements at the end of each word which function on a per word basis in a bit serial way The processing elements are represented by X and Y registers which read out memory array words in bit parallel but serially process the individual bits from each word All of the responding memory words identified by the combined operations of the access bus and address bus are individually processed bit serial, but simultaneously together through parallel operation.

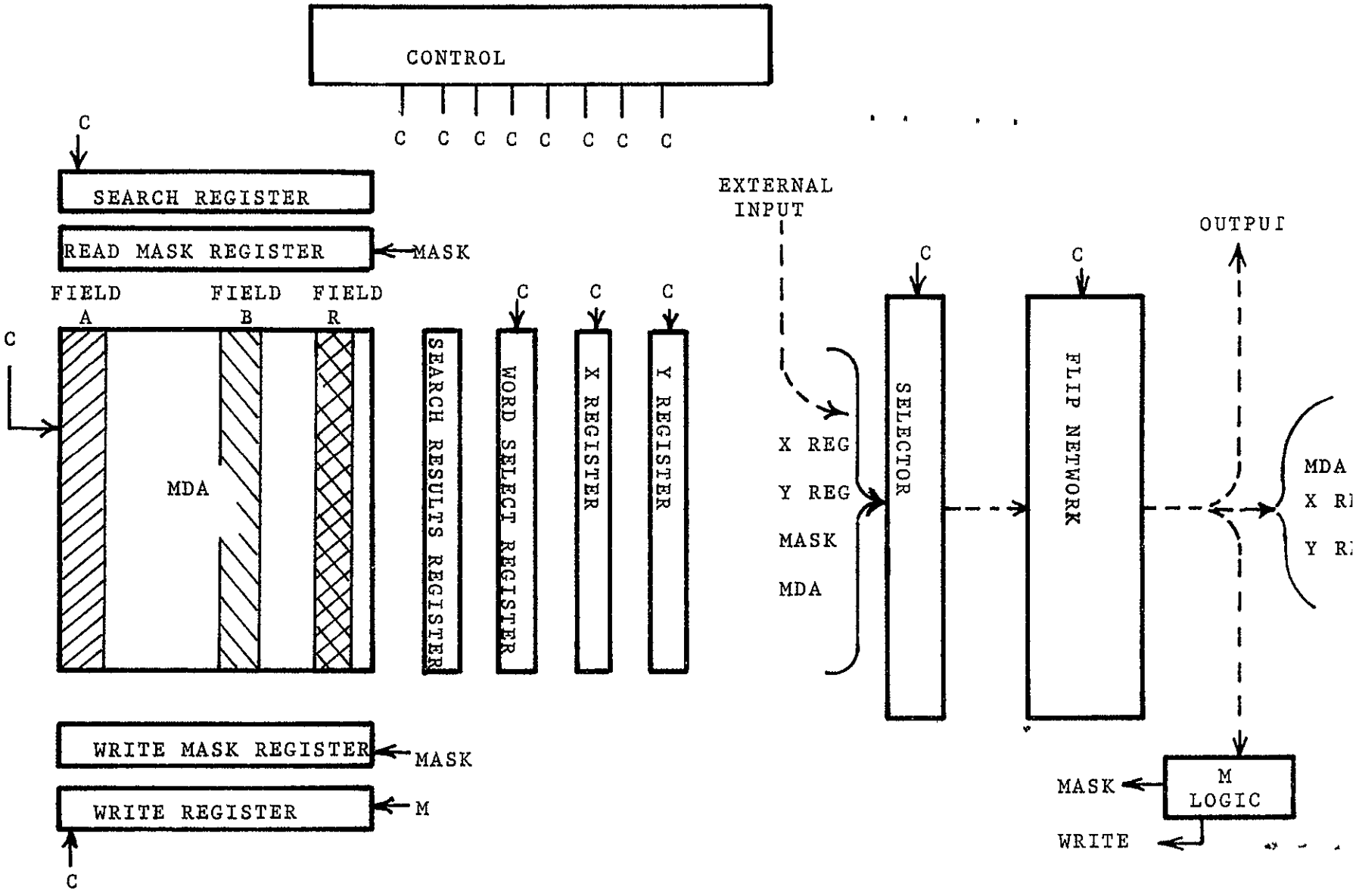
As a brief example to illustrate the (AM) associative memory operation, an 8 word AM with four 3-bit fields is shown in Figure 6. For example, word 7 has not been selected as shown by the contents of the word select register.

	101	110	000	000		SEARCH REGISTER
	111	000	000	000		MASK REGISTER
WORD 1	110	111	101	000	0	1
WORD 2	011	101	101	100	0	1
WORD 3	101	011	001	000	1	1
WORD 4	010	101	110	010	0	1
WORD 5	110	011	010	110	0	1
WORD 6	101	110	001	000	1	1
WORD 7	101	100	000	100	0	0
WORD 8	111	001	100	001	0	1
FIELD	1	2	3	4	SEARCH RESULTS REGISTER	WORD SELECT REGISTER

FIGURE 6

The contents of the mask register show that only the first field of the search register is to be included in the search. An equality search operation in the associative memory will result in the simultaneous comparison of the

contents of the first field of the search register to the contents of the corresponding field of all stored words It should be noted that only stored words 3 and 6 satisfy the search and are identified by 1's placed in the search results register after the search. The seventh word was not in the set of words designated for performance of the search by the word select register. As an example of possible X and Y processing register functions, the addition of paired quantities in two different fields (A & B) and storage in a results field (R) can occur in the same instruction (refer to Figure 7). This occurs within the same memory cycle by logic routing through a selector circuit and flip network. In the associative multi-dimensional access (MDA) memory, memory accesses (both read & write accesses) are controlled by the address and access mode buses The associative array module processing elements communicate through a controlled logic network A selector chooses a parallel multi bit source item from either the MDA memory readout bus, mask register, X register, Y register or input from outside source The bits of the source item travel through the flip network where manipulation or permutation of the bits in various ways occurs It is possible by program control for the permuted source item



ASSOCIATIVE ARRAY MODULE

FIGURE 7

to be presented to various destinations as the MDA memory write bus, mask register, X register, Y register and outside destination. The permutations of the flip network allow interprocessing element communications A processing element can read data from another processing element either directly from its registers or indirectly from the MDA memory Through program control, the flip network can permute the multi-bit data source item as a whole or divide it into groups and permute within groups This gives the programmer a great deal of freedom in using the processing capability of the processing elements. At one stage of a program, the capability could be applied to many bits of one or a few items of data, at another stage, it could be applied to one or a few bits of many items of data.

The multidimensional memory structure is not limited to a square array in formating data storage within the array For example, byte sized data quantities can be arranged as records stored in a single array. The claims made in available literature for bipolar solid state IC type associative memory array modules are pictorially described in Figures 8 and 9 Recently developed solid state

associative read write technology allows either word slice or bit slice operations to be performed in bit parallel mode. Such a file record as shown in Figure 8 can be accessed several ways as illustrated in Figures 9A, 9B, 9C.

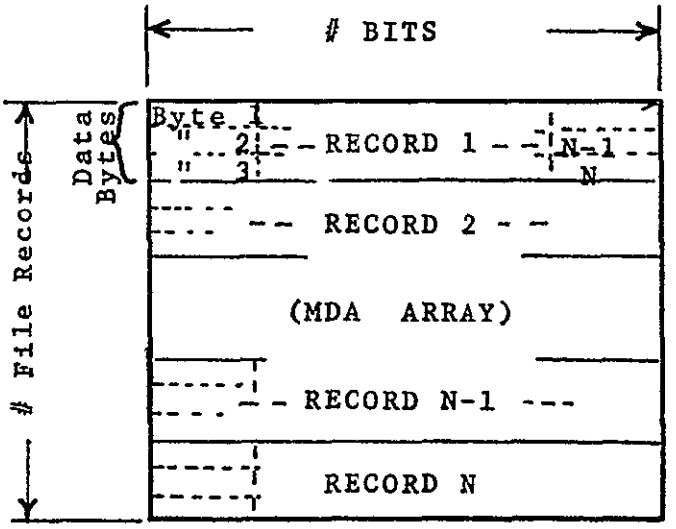
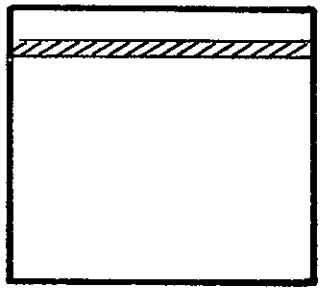


FIGURE 8

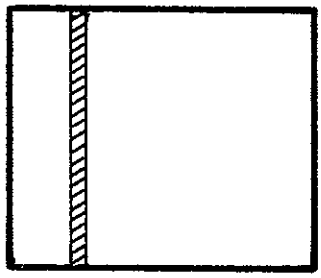
ACCESS TO CONSECUTIVE BYTES OF A RECORD IN PARALLEL (TO INPUT AND OUTPUT RECORDS)

A



ACCESS TO CORRESPONDING BITS FROM BYTES OF ALL RECORDS IN PARALLEL (TO SEARCH KEY FIELDS OF THE DATA)

B



ACCESS A BIT FROM EACH RECORD BYTE IN PARALLEL. (TO SEARCH TOTAL RECORD FOR PRESENCE OF A PARTICULAR BYTE)

C

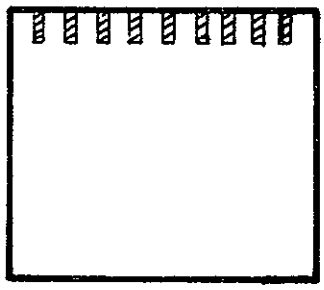


FIGURE 9

External control of the associative memory module is by means of the associative processor control unit and control memory. The control unit contains registers and necessary logic and receives instructions from the control memory Data is communicated to and from the control memory through the associative processor control unit Multiple associative memory modules can be controlled by this same control unit. One mode of control allows parallel data operations of 1 bit per nano second and practical higher bandwidths of 32 bits per nano second with yet higher attainable rates. The associative processor memory module can communicate with a parallel head disc system which is interfaced in such a way that parallel input/output data transfers of all the data channels can occur with the associative array module It is possible to communicate in such a way that every other disc sector or data surface can be read or written and processed in a matter of approximately 100 microsecs per sector Complex searches can be performed in this time frame if 100 microsec is not sufficient time to process an array, a bit map of searched sectors is kept. This bit map will allow minimization of rotational delay (refer to Figure 10). At speeds of 100 microsec for a sector to pass under the read/write heads, the entire disc surface or data base can be searched or processed in two disc revolutions Associative array modules are placed under control of a parallel control unit for input/output control via program operation

when performing parallel input/output functions. Control of associative arrays can be dynamically switched real time to effect interarray data transfers and array modules can be independently program controlled for either parallel or associative operation in real time. The parallel control unit can also communicate with the control memory for instructions and data transfers for array operations concurrent with the associative control unit (refer to Figure 11). The control memory holds associative processing control programs, parallel control programs, and microprogram subroutines A sequential minicomputer interfaces with the control memory to communicate with the standard peripheral

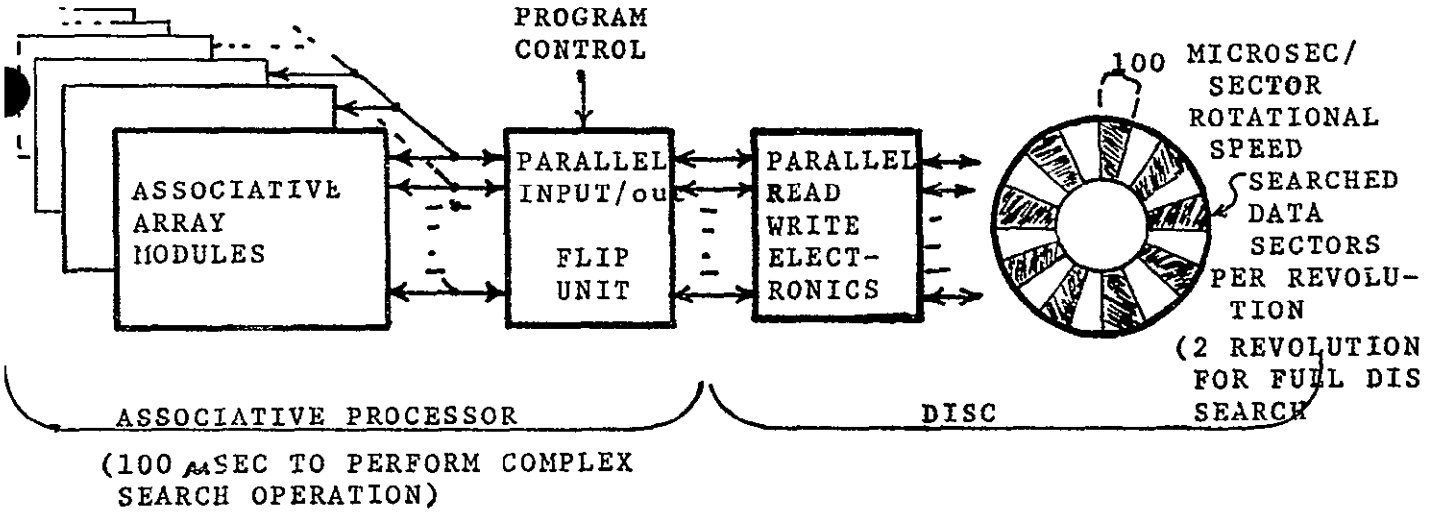
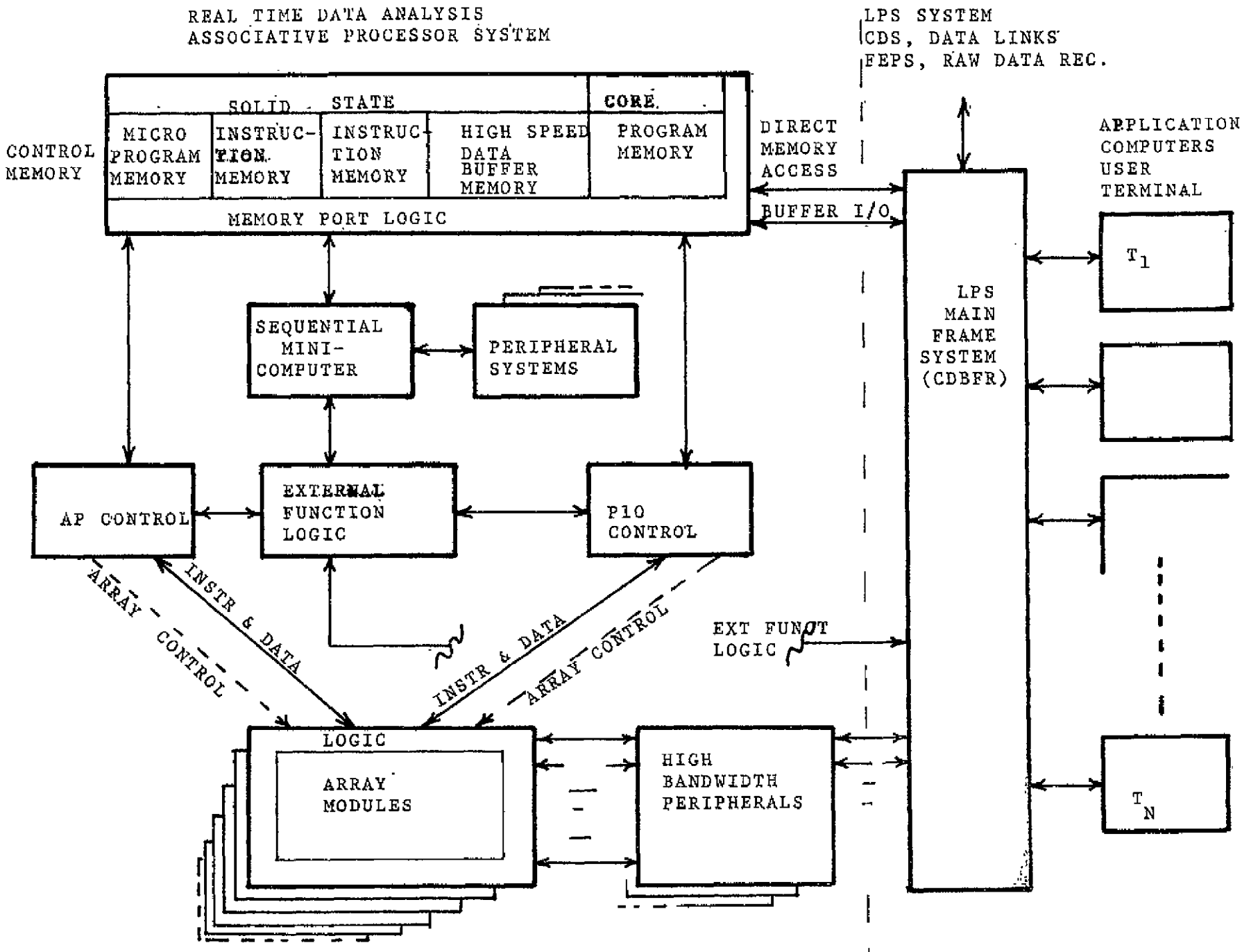


FIGURE 10

hardware for performance monitoring A concept interface is drawn in with Figure 11 for shuttle Launch Processor System operations.



CONCEPT FOR SHUTTLE LAUNCH PROCESSOR SYSTEM

FIGURE 11

4.0 APPLICATIONS

The following information discloses associative processing applications being pursued by other agencies and to present some heuristic discussions for KSC personnel. In a recent interim study report sponsored by the U. S. Army Engineering Topographic Laboratory (Reference 44) titled "Application of Associative Array Processing for Topographic Data Reduction", several interesting findings appear.

In ETL's stereo mappers (AS-11BX), aerial stereo photographic data is used to provide model area criteria for a STARAN Associative Array Processor (AAP) (Reference 32) This process performed coordinate transformation from model coordinates to local coordinates and interpolation of elevation data to produce regularly spaced elevations which ultimately would be used in a digital topographic data base. The number of AS-11BX's which could be supported was validated for 65 and estimated to 74 which exceeds the number that would exist in any one installation. In practical terms, this would allow simultaneous support of additional post processing tasks.

For ETL's raster processing with automated cartography digital processing of properly positioned line and character data produces the appropriate map symbology. The objective was to evaluate various time-consuming raster processing functions for associative array processing. The raster processing functions evaluated were registration mark detection, line separation, character recognition, line thinning, vectorization, skew correction, line break detection, line smoothing, and line symbol generation. The essential difference between what is presently implemented in ETL's IBM 360/40 program and that proposed for the STARAN AAP is the method used to represent the map image. The IBM 360/40 represents lines as a series of vectors and requires the creation of vector lists, whereas the AAP stores the map image (one area at a time) directly (intact) in the associative array memory fields whereby the total field format is logically processed using AAP field-to-field processing power The IBM 360/40 utilized time consuming raster-to-vector-to-raster conversions required by a sequential processor. The raster processing functions evaluated for STARAN application required approximately 9 1/2 hours of 360/40 processing time and were estimated to require 52 seconds of STARAN AAP time

The ETL Simultaneous Multi-Exposure Analytical Calibration (SMAC) Program is an operational software program implemented on a Univac 1108 sequential computer. The program involves an analytical camera calibration technique that uses known stellar data. The main emphasis of this study was directed toward an evaluation of the effectiveness with which the STARAN associative array processor could perform various SMAC related search and matrix operations. The search operations involved exact match searches of the BOSS catalog and a between limits search of the Smithsonian Astronomical Observatory (SAO) catalog. For various size matrices, matrix addition, subtraction, multiplication, and inversion were evaluated. A comparison of the results with the Univac 1108 execution time provided by ETL reveals an apparent STARAN AAP advantage of about 40.1.

The study is still in progress and is being conducted for the Computer Sciences Laboratory (CSL) of the U. S. Army Engineering Topographic Laboratory (ETL) by the Goodyear Aerospace Corporation. The intent is to analyze the applicability of an associative array processor to ETL data processing The contract was executed in two phases.

Phase I consisted of the Functional Survey and Detailed Planning for a brief evaluation of many of ETL's data processing problems to determine their suitability to associative array processing. Phase II consisted of study, validation and documentation of selected tasks involving systems analysis and algorithm structuring in detail

The STARAN Customer Evaluation and Training Facility (Reference 34) was utilized to implement the selected validation tasks in a real time environment. This is similar to the way Saturn Apollo System Development Facility at Marshall Space Flight Center was used to validate the Saturn Apollo Software. For details on the topics mentioned and others in the ETL study, it is suggested that the reader refer to Reference 44

To provide the reader with some hint of the software savings when using associative array processing, the following information was drawn from the Parallel Element Processing Ensemble (PEPE) System, Programmer and Users Manual (Reference 27) The PEPE system utilizes associative array

processing and has a long history of development by numerous industry groups for military application (References 4, 5, 19, 20, 26, 28). The efficiency of associative array processing power is illustrated by the following example. Think of a multi-file data base which is to be processed as follows

Perform Procedure A on each file. If the result of A is less than Y (a data file entry), perform procedure B If the result is equal to or greater than Y, perform procedure C

The flow charts for this process are shown in Figures 12 and 13. If the execution times are designated T_A, T_B, and T_C, the expression for total iteration time is

$$T_{run} = MT_A + (M-n)T_B + nT_C$$

Where M is the number of files and n is the number of files where the result of A is not less than Y. Note that the T_{run} is a function of both the number of files and the data within those files.

If the data files are assigned to associative array processing elements the processing time becomes.

$$T_{run} = T_A + T_B + T_C$$

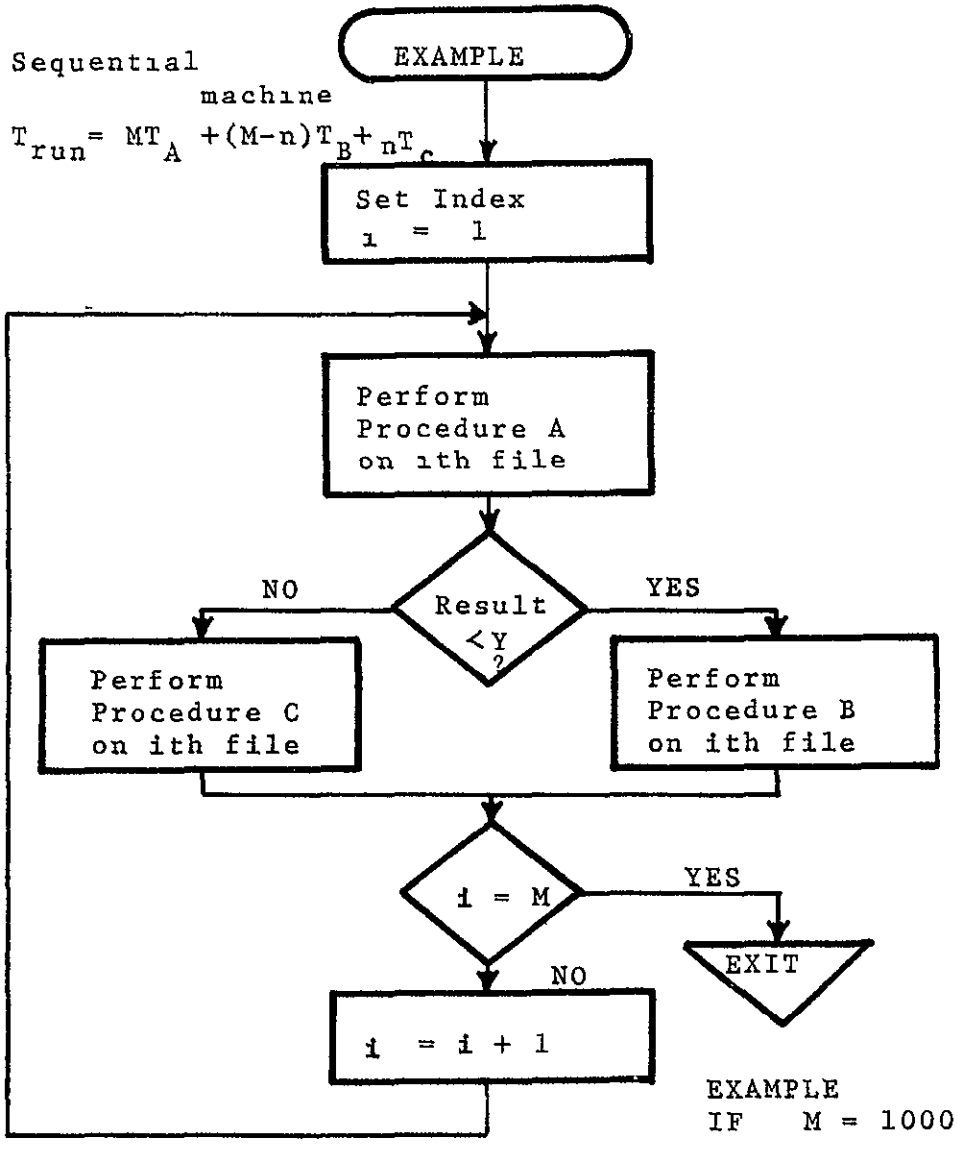


FIGURE 12 SEQUENTIAL

$T_{run} = 1000T_A + 500T_B + 500T_C$

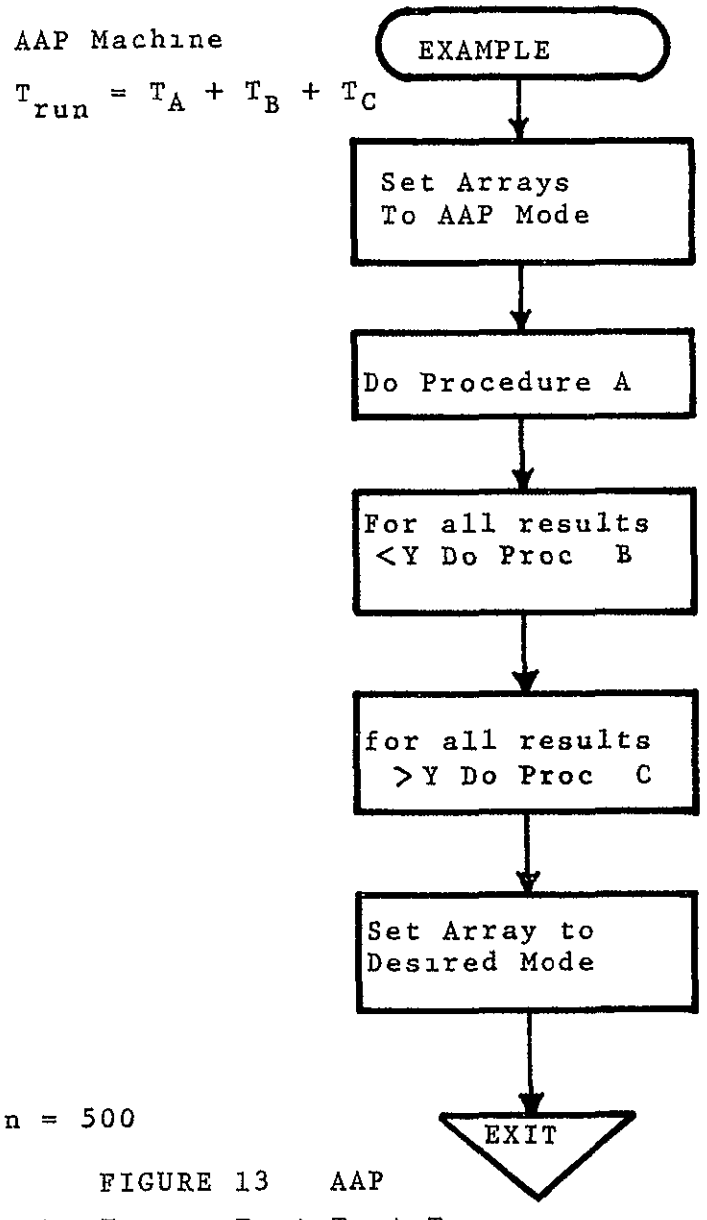


FIGURE 13 AAP

$T_{run} = T_A + T_B + T_C$

FLOW DIAGRAM OF IDENTICAL PROBLEM FOR DETERMINATION OF TOTAL RUN TIME EXECUTED ON CONVENTIONAL SEQUENTIAL PROCESSOR AND ON ASSOCIATIVE ARRAY PROCESSOR

Note that there is now no dependence on M or n even though their magnitudes may be very large. This is a very real consideration for virtually all dynamically changing large data base operations. For the AAP machine, the program is not concerned with physical record location in the arrays, nor is it necessary to order data tables by key since any datum can be located in one parallel search. The reader should also note the elimination of the conventional programming loop.

For the benefit of readers who are programmer types, some connotations from Reference 32 are listed below for their benefit.

1. In real time applications the programmer can easily time out his initial flow diagram since programming loops in the conventional sense are eliminated. This single consequence of associative processing can save much of the reprogramming effort invariably found necessary during the testing phase of conventional attacks on real time problems

2. He can conserve on execution time (and array memory space) by defining fields to use only as many bits as are required by the application.

3. He has no need for overhead-generating techniques such as indexed file constructions, linked lists, or sort and merge operations usually needed in a conventional computer. This capability results in a significant reduction both in the number of instructions which must be written and executed and the amount of memory required.

Research has been done by Honeywell Systems, Inc., on the use of associative processing for voice compression, data concentration, and asynchronous multiplexing onto a highspeed transmission facility for the Rome Air Development Center. The study is titled "Evaluation of The Use of An Associative Processor in Communication Multiplexing" (Reference 31). This study covers the multiplexing and multiplexing of transmitting and receiving combined multiple channel digitized voice mixed with real time data over a high speed data link The voice channels studied were comprised of byte samples at 8000 times a second. The study states that voice quality can be dynamically adjusted to absorb varying levels of activity in real time digital data channels. The mixed channels experiment indicated voice signals can tolerate a large amount of distortion before becoming unintelligible, whereas a few errors or lost data in the input to a computer may render useless all the information from the particular source. A computer simulation was written to accept six channels of digitized voice from a magnetic tape input. The tape formats were linear coded at 8000 samples/second and designed to appear the same as a data link input to the Associative Communication Multiplexer (ACM) simulation program. The ACM compression, noise suppression and

output selection functions were performed by simulation techniques and a six channel digital voice tape similar to the input tape was generated. The signal digitization operations were performed in parallel over all channels in the ACM The voice signals were compressed by ACM utilization of a specially developed Peak/Valley Interpolator algorithm (PVI) which causes transmission of the most significant extreme signal points and other samples in order of significance as channel capacity allowed. The waveform reconstruction was by first order interpolation, i e , straight line connection of transmitted points Under normal conditions, PVI would operate to transmit all significant extreme samples and many intermediate ones, thus providing ample information for accurate waveform reconstruction. Increasing overall data transmission activity would result in the loss only of the intermediate and extrema samples of least significance for the voice channels This work is being continued with a follow on contract to determine the best design of an associative processor for the compression and multiplexing of multiple voice and data channels onto a high speed digital transmission line This program will investigate

software design and interface hardware fabrication for the RADC Associative Processor (RADCAP, Reference 42) test facility to develop an Associative Buffer Concentrator (ABC) engineering model. This model will serve as a test vehicle to verify the design specification for a stand alone ABC.

5 0 POTENTIAL APPLICATIONS

The following discussion covers some candidate applications for associative processing that should be explored further in future study work. One such effort should be to investigate a means of rapidly interrogating data bases derived from high speed data links like the type being utilized between the Space Shuttle vehicle and ground checkout systems. This effort should comprise the data base handling at least of.

1. A consistent ordered data base
2. A complex unordered data base

The techniques for performing the following functions should be developed

a Scalefactor and unit conversions by simultaneous parallel operation for a data base.

b Data compression by simultaneous parallel operation for a data base

c. Parallel data point source and destination routing

- automatic patching of data points
- format separation and data classifier
- fast parallel scanning of data points

d Response to user request for

- random access of data points
- on call realtime data requests
- on call real time patching of data source and destination routing (patch modifier)

e. Technique for satisfying (d) under simultaneous multi-user request conditions

f. Parallel real-time data point trend and performance analysis under static and dynamic test conditions

- dynamic tolerance checking under test
- limit checking under static conditions
- error flagging

g Alternate schemes for either of the listed function a through f.

A typical condidate data base source is described in Figure 14 consisting of 128 Kbs containing data point assigned time slot fields of operational instrumentation data combined with (Case 1.) a group of fixed width fields of onboard computer data point sets with varying content identifiable data sets or (Case 2.) combined with a group of variable width fields of onboard computer data sets with varying content identifiable data sets.

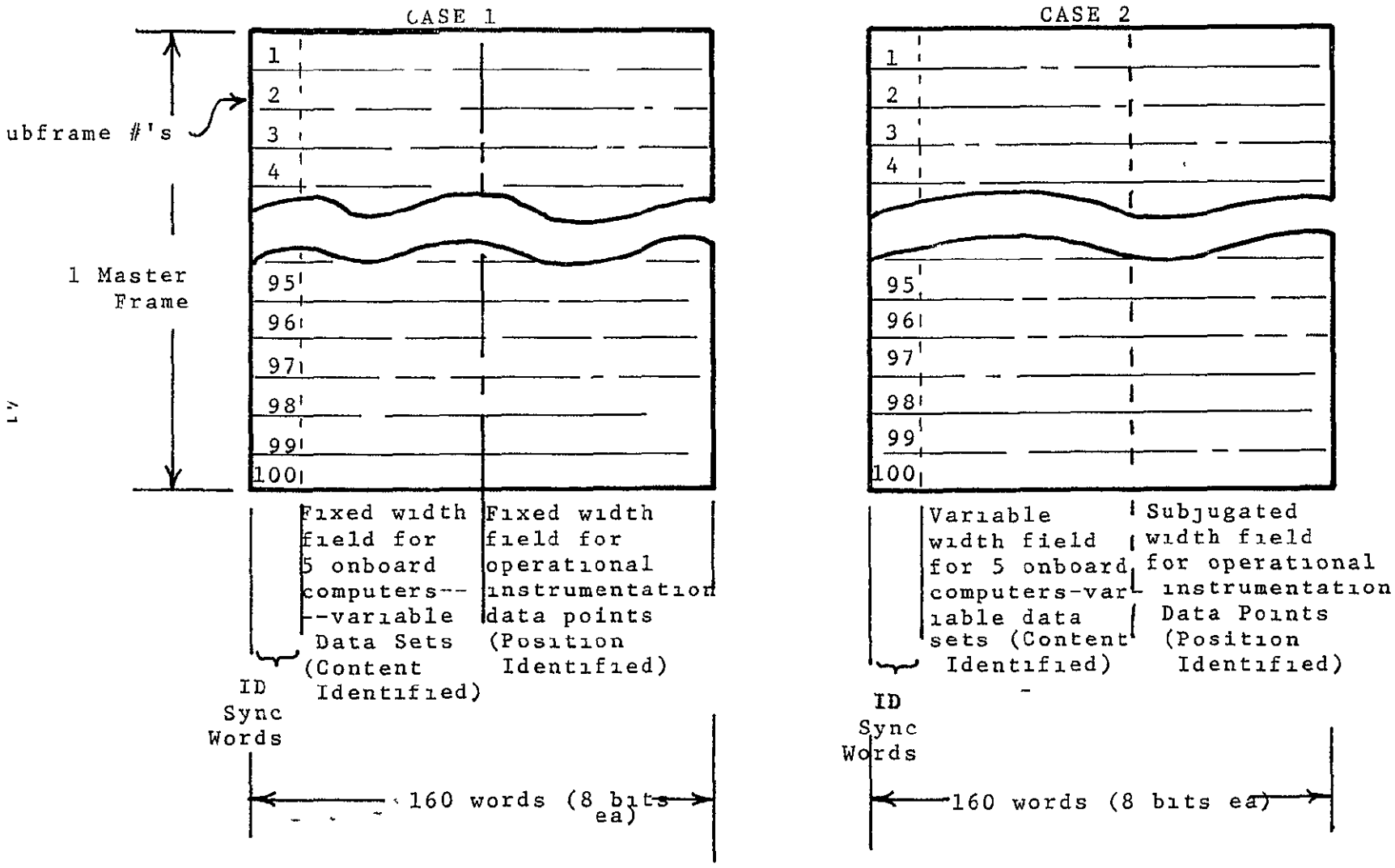

CASE 1
CASE 2
ubframe #'s
1 Master Frame
1
2
3
4
95
96
97
98
99
100
Fixed width field for 5 onboard computers--variable Data Sets (Content Identified)
Fixed width field for operational instrumentation data points (Position Identified)
ID Sync Words
160 words (8 bits ea)
Variable width field for 5 onboard computers-variable data sets (Content Identified)
Subjugated width field for operational instrumentation Data Points (Position Identified)
ID Sync Words
160 words (8 bits ea)

FIGURE 14

Specification for Data Link Architecture

128 kilo bits per second PCM rate

1 master frame per second

1 synchronization header word per subframe

100 subframes per master frame

160 8 bit words per subframe

4 8 bit words per I.D synchronization word as defined (3 words = sync code, 1 word = frame count and format I.D)

Some possible ways of developing techniques for a few of the stated functions might be as hinted in the following discussions

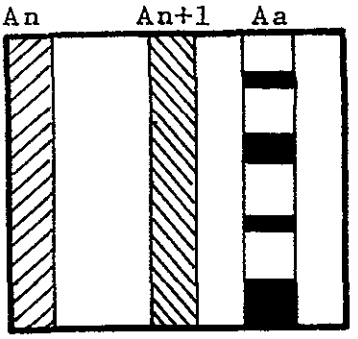
For the compression of an ordered data base, a field-to-field compare could be used Since previous discussions have indicated input/output methods, it will only be stated that data contained in a data link subframe might be arranged in the associative multidimensional array as shown in Figure 15 The data quantities in the fields designated An, An+1 are the previous and present

data point quantities of the same subframe in the master frame. In this case, the data points would be in the same position relative to each other or the same constant position relationship as found in the data link subframe. By a single field-to-field compare instruction, all the An and associated An+1 data points can identify all quantities which have changed since the last subframe occurrence and store the results in field Aa as shown.

If desired, this operation could be done with a number of subframes simultaneously within the same instruction cycle

For scale factor and conversion factor multiply operations the data points in field Aa could be multiplied by their common factors in field C to produce the resulting scaled and converted data points in field Aa' in a single instruction period (Reference Figure 16). The data point information in field Aa' could be outputed to the respective user terminals by combining associated identify tags to each respective data point. The identity tags could be in field ID (Reference Figure 17) and would define all needed criteria for routing the data points to either displays, printers, or inputs to application programs.

FIGURE 15



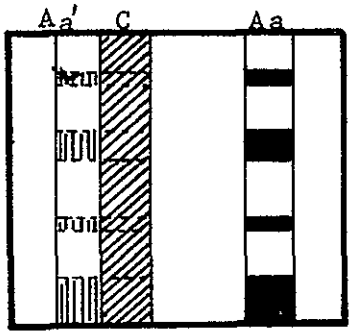
An = Previous values

An+1 = Present values

Aa = Changed values

COMPRESSION OF ORDERED DATA BASE
(By one instruction, compare field An with A_{n+1} and Load changes in field A_a)

FIGURE 16

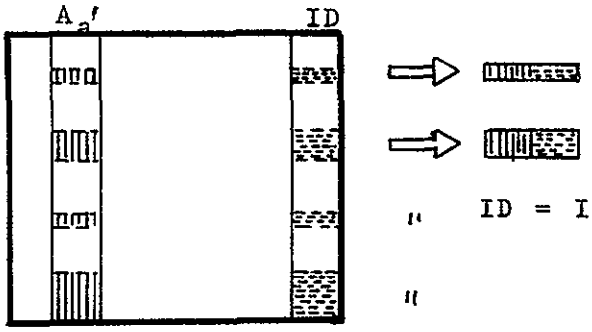


C = Scale factor values

A'_a = Converted values

SCALE FACTOR CONVERSION OF ORDERED DATA BASE
(By one instruction, multiply field A_a by field C and load into field A_a')

FIGURE 17

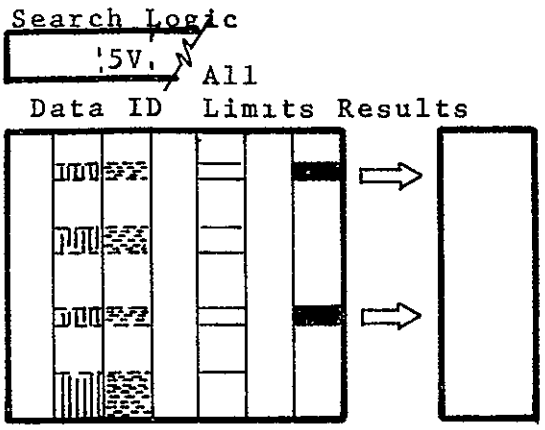


ID = Identity tags

INPUT/OUTPUT COMPRESSED DATA QUANTITIES
(By one instruction, readout values in field A_a' with corresponding tags in ID field)

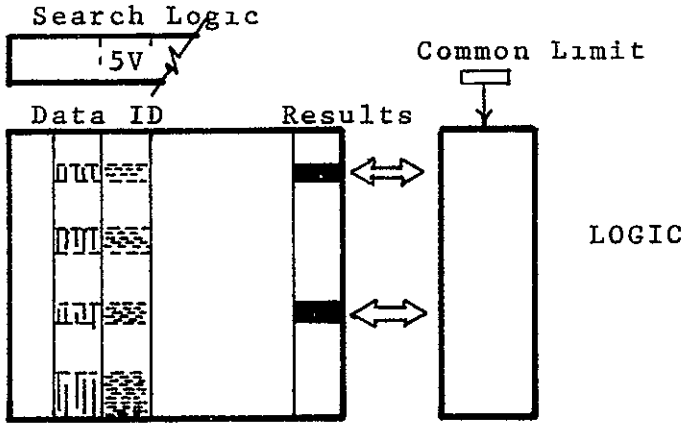
The following methods might be used for limit checking, refer to Figures 18 and 19. If all data points within the data base are assigned identity tags upon storage into the array as shown by the data field and ID field in Figure 18, then an associative search for any desired class of data point measurements can be made. The ID field could simultaneously provide the identity of all 5V measurements for all subsystems under test as set up by the search register in Figure 17 If all of the particular individual limits for each data point are stored in the all limits field, then an associative greater-than-less-than field to field instruction will produce any out of limit results. The out of limits results field will identify the data points and magnitudes of the out of limit 5 volt measurements. Out of limit checking for the entire data base would take relatively few associative instruction cycles An alternate scheme for the 5 volt limit check previously described would be to use a common limit quantity if circumstances allow, refer to Figure 19. The greater-than-less-than associative instruction will process all responding data points and place the results in the results field.

FIGURE 18



LIMIT CHECK DATA BASE FOR ALL 5V DATA POINTS
(By one instruction, compare data field with limits field for only 5V data points & store in results field)

FIGURE 19



ALTERNATE (USING A COMMON LIMIT VALUE)
(By one instruction, use common limit and compare with 5V data points and store in results field)

FOR THE EXAMPLE FIGURES ABOVE, ONLY THE 5V CLASS DATA POINTS WILL RESPOND THRU ID SELECTION

The previously described compression and limit checking schemes could have been performed in the associative arrays with the data orientated in other modes. Many styles of data organization are possible in the arrays for whatever applications the user wishes. More details on this are found in References 41, 45, 46, 47, 33, 32, where the reader may study further, the impressive repertoire of associative processor instructions.

Other potential applications would be in the area of software translator programs where associative array operations could be utilized as a fast interpreter. Some of the unique features of the associative memory could be investigated for the protective "fail soft" capability since the associative memory can continue to function with failed word elements thru use of the word inhibit/select register operation It is not intended in this document to cover all possible applications, but only to arouse the interest of the reader.

6 0 SUMMARY

This study develops a conceptual image of associative processing technology for the reader. Information for the subject material was drawn from the reference materials. The document preparer makes no original claims to any of the information in this document The intent was to promote interest in the subject. The material presented is a mixture of the Honeywell and Goodyear technology. For commercial applications these appear to be paramount sources of state-of-the-art information. The F.A.A. information concerning associative processing applications to air traffic control was not available due to competitive activity in this area which should be concluded in mid-1974 The information should become available soon after this time. The most surprising single fact was in the area of cost where a basic stand alone mainframe operational associative processor system was quoted by the vendor for $333,000 with additional array modules at $90,000 each The next phases of the study will require contractor activity, and it is hoped that they will fulfill the stated objectives.

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