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CONTAMINATION CONTROL IN HYBRID MICROELECTRONIC MODULES

SELECTION AND EVALUATION OF COATING MATERIALS
FINAL REPORT – PART 2 OF THREE PARTS

APRIL 1975

AEROSPACE GROUPS
HUGHES
HUGHES AIRCRAFT COMPANY
CULVER CITY, CALIFORNIA

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R. P. Himmel

Microcircuit Department
Developmental Products Laboratory

Prepared for
National Aeronautics & Space Administration
George C. Marshall Space Flight Center
Alabama 35812

AEROSPACE GROUPS
Hughes Aircraft Company • Culver City, California 90230

PREFACE

This document was prepared by the Hughes Aircraft Company, Culver City, California, in fulfillment of NASA Contract 8-30876, "Contamination Control in Hybrid Microelectronic Modules." The work was sponsored and administered by the George C. Marshall Space Flight Center, Alabama, with Mr. S. V. Caruso serving as the MSFC Technical Manager.

The Hughes program manager was Mr. R. Y. Scapple, Manager of the Microcircuit Department. The principal investigator was Mr. R. P. Himmel, Head of the Microcircuit Technology Section. Principal participants in the program were Messrs. A. R. Mastro and A. Koudounaris. Valuable support was also provided by various members of the Hughes Technical Staff, including F. Z. Keister, F. W. Oberin, and K. Yamamoto.

This report, Part 2 (of 3 parts) of the Final Report, covers the work conducted from May 1974 through April 1975 and described in Tasks II and III of the contractual Statement of Work. The objective of these tasks was to "select, test, and evaluate electrically and thermally stable coating materials for contamination control of hybrid microcircuits."

There have been no inventions, discoveries, improvements, or innovations made under this contract.

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INTRODUCTION AND SUMMARY

Contamination control is a significant problem in the manufacture of hybrid microelectronic modules because contamination within a sealed hybrid package can be a cause of reduced reliability. Under a contract (NAS 8-30876) from the George C. Marshall Space Flight Center, the Hughes Aircraft Company conducted a program directed towards a solution of this contamination problem. The program was divided into four tasks.

The object of Task I was to identify the various types of contaminants that are found in hybrids and, in addition, to identify the critical manufacturing processes during which these contaminants can be introduced into the hybrid. Task I is documented in a separate report (Final Report – Part 1). Tasks II and III, described in this document, were directed specifically at the selection, test, and evaluation of organic coating materials for contamination control. Task IV covered the development of guidelines for the fabrication of hybrid microcircuit modules. These guidelines, documented in a separate report (Final Report – Part 3), include a processing specification for contamination control and a source control document for coating materials.

Contamination may manifest itself in many forms, such as outgassing products, corrosive chemical residues, small pieces of wire, and various other types of loose particles. These contaminants may be introduced into a hybrid package during certain of the fabrication processes. Especially critical are the processes of component mounting, wire bonding, rework, and package sealing. Most of these contaminants can be detected by a thorough pre-seal visual inspection of the hybrid. Cleaning will remove many of the loose particles and chemical residues. However, the probability always

exists that some contaminants may escape the cleaning processes and the visual inspections. There is also a possibility that new contamination, such as moisture or solder balls, may be introduced while the cover is sealed on the hybrid package. Thus, in addition to special precautions and process controls, it was felt that the use of a protective organic coating applied to the hybrid microcircuit might act as further insurance against potential contaminants, especially those contaminants introduced during package sealing.

This report (Final Report — Part 2) presents the results of the search for a suitable organic coating, which is intended to be applied to the hybrid before sealing. The coated hybrid would then be hermetically sealed in an inert atmosphere. The coating is not intended to encapsulate the hybrid, nor to form a heavy coating barrier against mechanical damage or moisture, nor to replace the hermetic package. Rather the coating is intended to provide an insulating and protective shield over the substrate, chip components, circuitry, and wire bonds in order to protect them from subsequent loose particles and to immobilize any loose particles that might have escaped the cleaning, visual inspection, or other contaminant detection processes.

The basic requirements for a hybrid microcircuit coating material are that the coating itself should not be a source of contamination and it should not in any way degrade the hybrid's electrical or thermal performance. The coatings evaluated for this program are all commercially available, capable of being reworked, and capable of passing the screening requirements of MIL-STD-883, Method 5004, Condition A.

Under Task II of this program, potential hybrid microcircuit coatings were surveyed, and preliminary screening tests were conducted on several candidate coatings, including polyimides, silicones, and epoxies. The selection was narrowed to three silicone coatings and three epoxy coatings for final screening tests. Screening tests included flex-adhesion, method of application, stress during cure, repairability, laser trim-through capability, solvent resistance, outgassing, effect on wire bond strength, effect on thick and thin film resistors, effect on transistor chips, voltage breakdown, and insulation resistance. At the conclusion of the screening tests, two coatings

were selected for final evaluation: a Dow Corning silicone coating (DC 90-711) and a Union Carbide epoxy coating (ERL 4289) with a dimer acid hardener.

Under Task III of this program, the two best coatings from Task II were evaluated to determine their suitability for use as a conformal coating over the hybrid microcircuit (including chips and wire bonds) inside a hermetically sealed package. Evaluations included ease of coating application and repair and effect on thin film and thick film resistors, beam leads, wire bonds, transistor chips, and capacitor chips. The coatings were also tested for such properties as insulation resistance, voltage breakdown strength, and capability of immobilizing loose particles inside the packages.

Thirty-two hybrid microcircuit test specimens were prepared. Some specimens were coated with the epoxy and some with the silicone; the remainder were left uncoated as control samples. These hybrids were then sealed and submitted to a series of sequential environmental tests including stabilization bake, thermal shock, temperature cycling, mechanical shock, acceleration, and high temperature reverse bias burn-in. The selected coatings were found to be electrically, mechanically, and chemically compatible with all components and materials normally used in hybrid microcircuits. The only exception to this result was a slight adverse effect on certain thick film resistors and on ultrasonic wire bonds. The coatings passed all package screening requirements of MIL-STD-883, Method 5004, Condition A.

1.0 TASK II: SELECTION OF COATING MATERIALS

1.1 RESULTS OF A SURVEY OF COATING MATERIALS

A wide spectrum of coatings was available for consideration. These were narrowed down to certain basic chemical classes, including polyimides, silicones, epoxies, and vapor deposited Parylene, which were judged able to meet the stringent requirements. (Parylene has been investigated elsewhere[1] for microcircuit coating applications and was therefore not included in this evaluation.)

Consideration was given to available data on physical, chemical, mechanical, thermal endurance, and electrical properties. The purity of the coating materials was considered important. Silicone junction coatings have been employed on microcircuitry extensively in the past and are especially well known for their low concentration of alkali and halogen ion impurities (measured as low as several parts per million). Finding pure epoxy resins has, in the past, been difficult; the recent availability of cycloaliphatic epoxies has, however, solved this problem. Polyimides posed no problem with regard to the availability of pure resins; it was, however, difficult to adequately cure these compounds at sufficiently low temperatures that did not adversely affect the microcircuits.

Reports from prior funded efforts have indicated certain characteristic modes of potential failure:

1. Deposited coatings were too thick, imposing an added load in the Y-direction during acceleration; vibration, impact or temperature cycling resulted in broken wire bonds.
2. Coatings were not fully cured, resulting in poor adhesion to the substrate. This characteristic caused the entire film (with the

leads still embedded in the coating) to lift and resulted in broken wire bonds.

3. Coatings were not adequately screened for chemical compatibility, and large changes occurred in thick and thin film resistors during thermal or thermal-humidity aging.

1.2 PRELIMINARY SCREENING TESTS OF CANDIDATE COATINGS

Candidate coatings were subjected to preliminary screening tests to insure that those selected for further testing would impose no limitation on the performance capabilities of the hybrid microcircuit. Acceptable coatings had to satisfy the following criteria:

- Maintain their physical, mechanical, and electrical integrity over a sustained period of exposure to high temperature
- Experience minimum degradation (weight loss) under thermal-vacuum conditions
- Maintain flexibility and adhesion and yet transmit minimum stress under extended repetitive cycles of thermal shock
- Be chemically compatible and non-reactive with the other components of the hybrid microcircuit
- Be capable of fully curing at a temperature not greater than 150°C.

The pitfalls that can occur through the use of improper coatings are sometimes insidious. These include thick film resistor drift (especially under long duration thermal and/or thermal-humidity exposures), semiconductor device degradation (primarily due to ionic contamination), early lead bond failure (particularly during thermal cycling), and conductor or thin film electrochemical attack (accelerated by temperature, voltage, and humidity or ionic species within the coating). Specific examples of the erratic effects produced on thick film resistors by incompatible coatings can be found in the literature.[2, 3]

1.2.1 Flex-Adhesion Tests

To determine whether a material could be expected to survive repeated thermal shock, a flex-adhesion test was performed. Some of the coatings initially considered during this investigation and screened by this

test are shown in Table 1. For the flex-adhesion test, each coating was deposited as a cured film, 0.013 to 0.025 mm (0.5 to 1.0 mil) thick, on a 0.1 mm (4 mil) thick aluminum strip; the coated strip was flexed through an arc of 180 degrees across a 3.2 mm (1/8 inch) diameter mandrel for 100 cycles. The coating was then scribed in a cross-hatch pattern of 2.5 mm (0.1 inch) squares and exposed to a tape-pull test. The number of squares that lifted was recorded as a percentage of the total number of squares in the stress-affected zone. Typical modes of failure were cracking, peeling, and lifting of the coating from the aluminum strip.

1.2.2 Application Characteristics

When the polyimides were deposited on a ceramic substrate, they showed difficulty in properly wetting the surface; as a result the coating pulled back from the edges and exhibited a somewhat uneven thickness after

TABLE 1. FLEX-ADHESION TEST RESULTS

Type	Coating	Number of Flex-Adhesion Cycles	Percentage of Coating Removed	Cure Schedule*
Polyimides	Rhodia 605, Rhodia Co.	10	100	A
		100	0	B
	NR150A, E.I duPont Co.	1	100	A
		5	100	B
Silicones	Dow Corning Co			
	GP77	30	40	A
	DC 90-720	30	40	
	DC 6101	100	0	
	62-047-WE	100	0	
	DC 90-711	100	0	
Epoxies	Union Carbide Co.			
	ERL 4221+dimer acid	100	0	
	ERL 4289+dimer acid	100	0	
	ERL 4289+HHPA	100	0	A

*Cure Schedules A: 25°C (1 hr) + 100°C (1 hr) + 150°C (5 hrs)
B: Schedule A + 230°C (1/4 hr)
(1) HHPA: hexahydraphthalic anhydride

cure. The silicones offered superb wetting properties, and the cycloaliphatic epoxies were a close second.

It was theorized that the spraying pressure might have a potentially degrading effect on wire bond strengths. To test this theory aluminum wire bonds, 0.0254 mm (0.001 inch) thick, were sprayed with epoxy at three different line air pressures from 8 to 50 psi. No evidence of degradation was observed, as shown in Table 2.

1.2.3 Stress Transmittal Through Coating

To evaluate the intensity of stress transmitted by a coating to a thin metallic element (simulating a wire bond), the following test was devised. Varying thicknesses of coatings were applied to 0.1 mm (4 mil) thick aluminum sheets and cured. The specimens were then subjected to thermal cycling from -65°C to 150°C for 100 cycles. When applied thin, all of the flexible coatings (such as DC 90-711, R6101, ERL 4221, and ERL 4289) passed without any deformation to the aluminum. The rigid materials (such as 62-047WE, 90-720, and DC 648) and the thick flexible coatings curled in multiple convolutions (see Figure 1).

The rigid silicone 62-047 WE caused suprisingly strong deformation to the aluminum even with a thin coating. In view of this result, consideration was given to dropping this coating from further consideration; it was retained, however, because it not only had passed all previous screenings

TABLE 2. WIRE BOND DEGRADATION VS AIR PRESSURE OF SPRAY

Spraying Pressure	Original Number of Wire Bonds Sprayed with Epoxy in Four Passes	Number of Wire Bonds Broken After Coating Cure to Thickness of 0.018 mm (0.7 mil)	Number of Wire Bonds Broken After 100 Cycles at -65 to 150°C
345 kPa (50 psi)	36	0	0
173 kPa (25 psi)	29	0	0
55 kPa (8 psi)	26	0	0

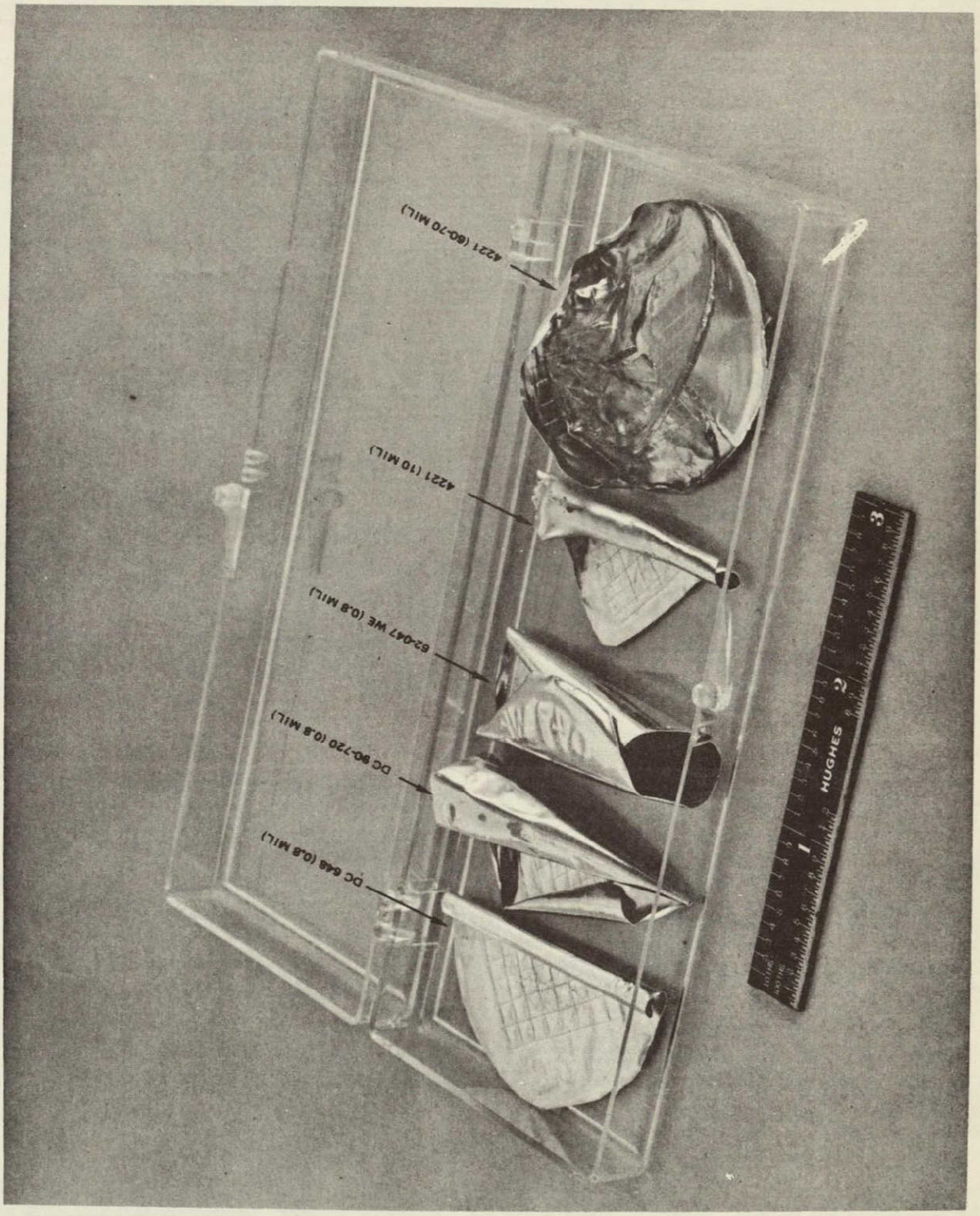

Figure 1. Mechanical "strip" samples after temperature cycling.

but had been used in numerous other studies on actual production hardware as a highly recommended coating for microcircuits. It was felt that the rigid silicone would serve as a useful comparison.

1.2.4 Results of Coating Selection Tests

As a result of the screening tests, the six best performers, listed in Table 3, were selected for further testing.

1.3 SCREENING TESTS ON SIX CANDIDATE COATINGS

After the selection of the six coatings, the next step was to determine the two best candidates, which would then be used in the final test program. The two best coatings were selected on the basis of the following screening tests:

- Repairability of coating
- Laser trimming of resistors through the coating
- Solvent resistance
- Outgassing characteristics at 150, 175, and 200°C

TABLE 3. CANDIDATE COATINGS

Designation	Formulation or Trade Name	Source
S1 S2 S3	DC 90-711 R6101 62-047 WE	Dow Corning Corp., Midland, Mich.
E4	ERL 4221 plus dimer acid	Resins: Union Carbide Corp., Bound Brook, N.J.
E5	ERL 4289 plus dimer acid	Dimer acid: Emery Ind., Cincinnati, Ohio
E8	ERL 4289 plus HHPA (hexahydraphthalic anhydride)	HHPA: Allied Chemical Co., El Segundo, Calif.

- Effect of the coating of wire bonds
- Effect of the coating on thick film and thin film resistors
- Suitability after temperature cycling and thermal aging
- Effect of the coating on transistor chips
- Voltage breakdown and insulation resistance

1.3.1 Coating of Test Specimens

To prepare specimens of the candidate coating materials for the various screening tests, they were first diluted with chemically pure toluene to a 30 percent (by weight) solids content. They were then sprayed on the applicable test specimen with a Binks Wren B gun. Line air pressure was maintained at 55 to 83 kPa (8-12 psi gage). Spraying was accomplished in four separate passes, specimens being rotated 90 degrees after each pass. A period of eight minutes drying time was allowed between passes, followed by a 1-hour dry at room temperature, plus 1 hour at 100°C, plus 5 hours at +150°C.

1.3.2 Laser Trimming Through the Coating

Both thick and thin film resistors, coated with all the candidate formulations, were laser trimmed successfully, as evidenced by scanning electron microscope (SEM) pictures. In general, the silicones appeared to vaporize both in the region directly under the beam and adjacent to it (see Figure 2). The epoxies, in comparison, presented a different appearance, with residual coating material remaining over the trim cut (see Figure 3).

1.3.3 Removal and Replacement of Devices

Repair was successful for all of the coatings. The chip (and coating) removal was accomplished by heating the specimen to about 200°C to soften the epoxy adhering the chip to the specimen and using a miniature chisel tool. This procedure could be performed in a few seconds to prevent damage to other components. The chip mounting site was then carefully cleaned and a new chip attached, again with conductive epoxy. After the conductive epoxy and wire attachments were cured, the strength of the bond was measured. All of the new wires exhibited acceptable bond strength (>1 gm).

Figure 2. Laser-trimmed thin film resistor through DC 62-047 WE silicone coating (SEM photo at 162X).

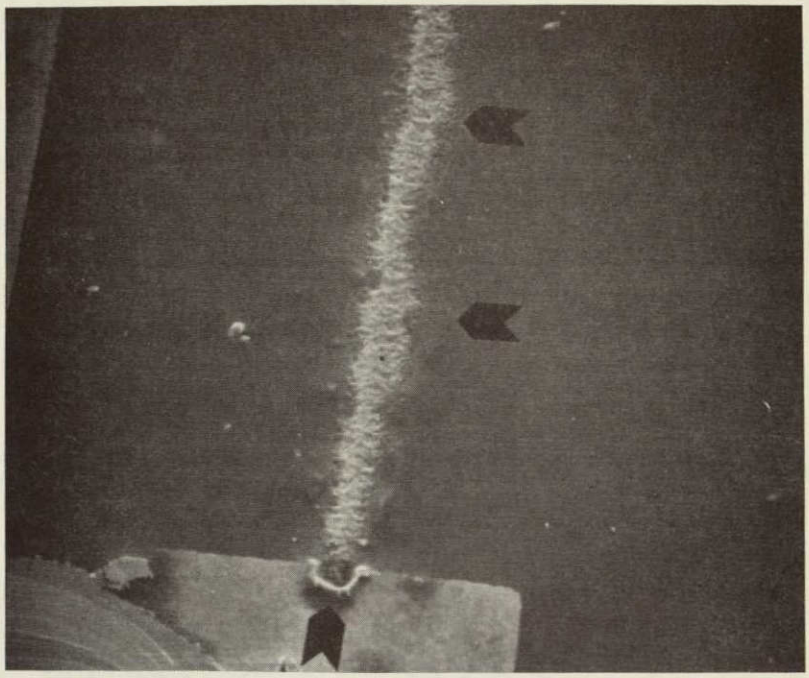

Figure 3. Laser-trimmed thin film resistor through E8 epoxy coating (SEM photo at 192X).

While this test established, within defined conditions, the repairability of the coatings, it was not intended to show the integrity of the repaired chip and interconnection wires. The reliability of such repairs was determined in the final test program.

1.3.4 Coating Repair

The coatings were repaired at the laser-affected zone or the chip-removal zone by the localized application of additional coating. Adhesion of the new coating to the old coating was excellent for all the candidates.

1.3.5 Solvent Resistance of Candidate Coatings

Because the application of coatings to microcircuits will be performed just before hermetic sealing, no cleaning will normally be required after

coating. In the event that a repair to a sealed package is desired, however, cleaning may become necessary. For this reason, a solvent-resistance test was included in the candidate coating screening tests. The test sequence was

1. Deposit coating on test specimen (aluminum cup)
2. Cure coating
3. Expose coating to exaggerated cleaning cycle
4. Perform visual examination of coating
5. Perform weight loss measurement

The cleaning sequence followed in step 3 is given in Table 4.

Solvent resistance data as a function of cure are presented in Table 5. The weight loss which the coating experiences from the solvent cleaning cycle is directly dependent on whether the coating is fully cured. It is obvious from the data that S3 is not fully cured at 150°C. Except for S3 which exhibited high solubility and E8 which gave somewhat erratic solubilities in small localized areas (showed bubbles), all the remaining candidate coatings were considered acceptable in terms of solvent resistance in a typical cleaning cycle.

TABLE 4. HYBRID MICROCIRCUIT CLEANING PROCEDURE

Cleaning Sequence		Normal Cleaning Time (Minutes)	Cleaning Time Used In This Test (Minutes)
Step	Method		
1	Methyl Alcohol Soak	1	2
2	Vapor-degrease (Freon TF)	1	2
3	Water Soak (D.I. water)	10	15
4	Nitrogen Gas Dry	-	-
5	Air Bake (125°C)	15	15

TABLE 5. WEIGHT LOSS OF COATINGS SUBJECTED TO SOLVENT CLEANING AS A FUNCTION OF CURE

Coating Material	Weight Loss (percent)		
	(150°C) 6 hours	(150°C) 24 hours	Full Cure[1]
S1	0.10	0.00	0.01
S2	0.26	0.13	0.01
S3	2.28	1.25	0.28
E4	0.18	0.05	0.02
E5	0.08	(+)0.03[2]	0.00
E8	0.13	Not tested	Not tested

[1] Full cure is: 25°C 1 hour
plus 125°C 4 hours
plus 200°C 16 hours
plus 250°C 1 hour

[2] Weight gain

1.3.6 Exposure to Thermal-Vacuum

To determine the outgassing characteristics of the coatings, each material was deposited on the surface of a glass tube, cured, sealed within a larger glass tube (see Figure 4) which was evacuated to 10^{-6} Torr, and subjected to the following (using one specimen for each test condition):

1. 200°C, 10 minutes
2. 175°C, 1 hour
3. 150°C, 1000 hours

Residual gasses were analyzed by a mass spectrophotometer and volatile condensible materials by infrared spectroscopy. Weight losses were calculated from initial and terminal weight measurements. Results are shown in Tables 6 and 7.

A thick-film substrate with gold metallization was exposed to the collecting condensate resulting from the thermal-vacuum exposures in

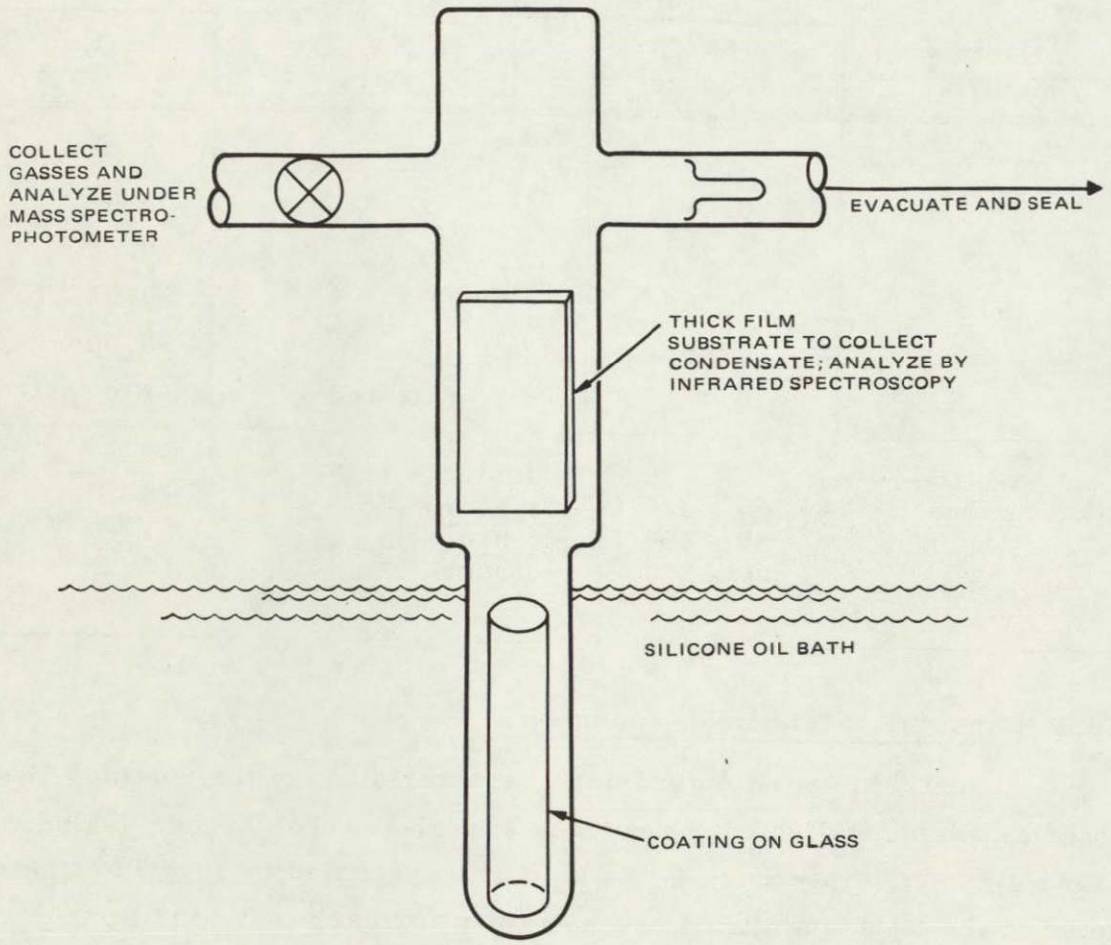

Figure 4. Apparatus for Thermal-Vacuum Outgassing.

TABLE 6. PERCENT TOTAL WEIGHT LOSS OF COATINGS IN THERMAL-VACUUM ENVIRONMENT

Tests at 133 μPa (10^{-6} Torr)	Percent Total Weight Loss					
	S1	S2	S3	E4	E5	E8
200°C, 10 minutes	1.27	1.01	2.60	0.33	1.12	2.67
175°C, 30 minutes	1.66	1.17	2.61	0.69	1.69	5.19
150°C, 1000 hours	1.13	0.99	2.76	3.43	4.95	3.25

TABLE 7. ANALYSES OF RESIDUAL GAS AND CONDENSATE AFTER THERMAL-VACUUM EXPOSURE OF COATINGS

Test Condition	Coating	Mass Spectroscopic Analysis of Residual Gas*	Infrared Analysis of Condensate
200°C 10 minutes	S1	H_2, N_2, CO, CO_2, C_6H_6	Dimethyl siloxane
	S2	N_2, CO, H_2, CO_2, C_6H_6	Dimethyl siloxane
	S3	H_2, N_2, CO, C_6H_6	Methylphenyl siloxane
	E4	CO, H_2O, H_2, CO_2, C_4	Indeterminate
	E5	CO, CO_2, H_2	
	E8	H_2O, H_2, CO_2	
175°C 30 minutes	S1	H_2, N_2, CO, H_2O, CO_2, C_6H_6	Dimethyl siloxane
	S2	N_2, H_2, C_6H_6	Dimethyl siloxane
	S3	N_2, CO, H_2, C_6H_6	Methylphenyl siloxane
	E4	CO, CO_2, H_2, C_4, C_5	Indeterminate
	E5	CO, H_2, CO_2	
	E8	CO, CO_2, C_6H_6, toluene	
150°C 1000 hours	S1	H_2, CH_4, C_6H_6	Dimethyl siloxane
	S2	H_2, CH_4, C_6H_6	Dimethyl siloxane
	S3	H_2, C_6H_6	Methylphenyl siloxane
	E4	H_2O, H_2, CO, CO_2, C_4	Indeterminate
	E5	H_2, H_2O, CO, CO_2, C_4, C_5	
	E8	H_2O, H_2, CO, CO_2, C_4	

*Listed in order of relative preponderance

Table 7. This substrate was examined for corrosion at the end of 1000 hours at 150°C. None was found.

1.3.7 Thermal-Mechanical Effects

Mechanical compatibility of the coatings with typical hybrid microcircuits was determined with the use of a test specimen containing certain elements of a hybrid microcircuit (see Figure 5). The test specimen contained one thick and one thin film substrate adhesively bonded to a rigid aluminum carrier. The substrate contained resistors, conductors, and interconnection wires (see Table 8 for details). The test sequence is shown in Figure 6; visual and electrical tests at designated test points included resistor values, interconnection wire continuity, and inspection at 30X. Despite the severity of this test, none of the coatings was found to cause damage to wire bonds or instability of coated resistors (resistor data are given in Table 9).

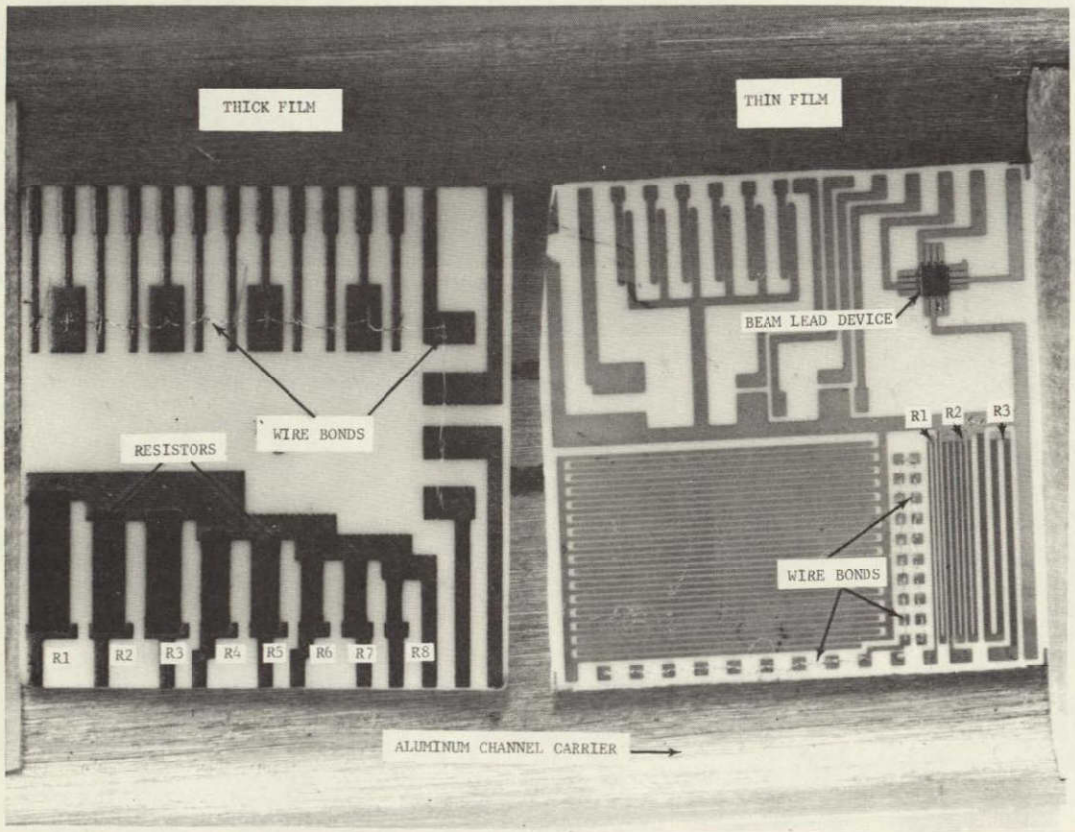

Figure 5. Specimens for mechanical screening tests of candidate coatings.

TABLE 8. DESCRIPTION OF MECHANICAL SCREENING TEST SPECIMENS

Part*	Thick Film	Thin Film
Substrate		
Material	96 percent alumina	99 percent alumina
Dimensions	19.050 x 19.050 x 0.635 mm (3/4 x 3/4 x 0.025 inch)	19.050 x 19.050 x 0.635 mm (3/4 x 3/4 x 0.025 inch)
Conductors	Au (ESL 8835 material)	Plated Au/evaporated Ni/evaporated Ni Cr. Dielectric breakdown patterns (6). Interdigitated capacitor (1).
Resistors	(ESL 3800 Series material) R1, R2: 10 Ω/□ R3, R4, R5: 100 KΩ/□ R6, R7, R8: 1 KΩ/□ All resistors were overglazed; R1, R3, and R6 were laser trimmed	3 Ni Cr resistors (not trimmed) 100 Ω/□ and 225 Ω/□ resistive material
Wire Bonds	Interconnected bonds (15) Au wire, 0.051 mm (0.002 inch) diameter, thermocompression bonded	Interconnected bonds (28) Au wire, 0.051 mm (0.002 inch) diameter, thermocompression bonded
Devices on each substrate	None	Beam lead integrated circuit (nonfunctional)
Carrier	Aluminum channel (open—two substrates were epoxy bonded to the carrier, one thick and one thin film.	

*Actual typical parts are shown in Figure 5.

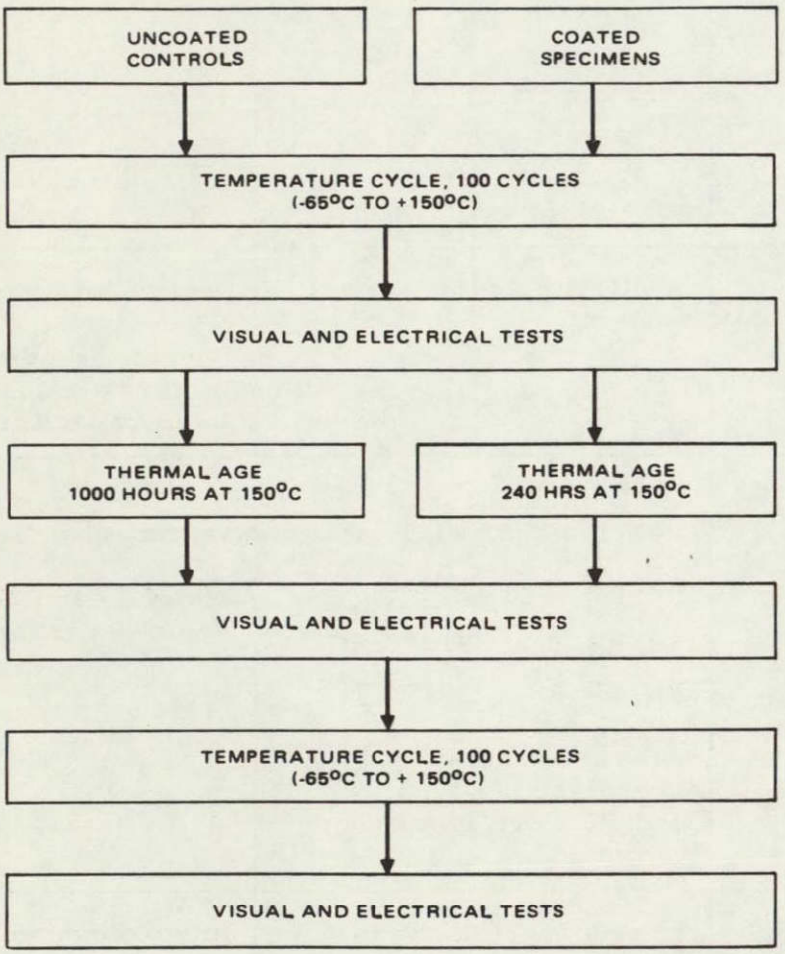

Figure 6. Mechanical screening test sequence for candidate coating materials.

TABLE 9. AVERAGE RESISTANCE CHANGE OF COATED THICK AND THIN FILM RESISTORS IN AIR

Coating	Thin Film, percentage		Thick Film, percentage	
	1000 Hrs 150°C	240 Hrs 150°C +200 Cycles (-65 to 150°C)	1000 Hrs 150°C	240 Hrs 150°C +200 Cycles (-65 to 150°C)
Control*	0.07	0.04	-0.07	-0.13
S1	0.01	0.03	-0.08	-0.14
S2	0.13	0.09	-0.04	-0.16
S3	0.13	0.11	-0.04	-0.09
E4	0.12	0.07	-0.04	-0.10
E5	0.11	0.03	-0.02	-0.15
E8	0.25	0.01	-0.05	-0.10

*No coating

1.3.8 Electrical-Thermal Tests

The test specimen utilized for the electrical screening tests is shown in Figure 7. It consisted of two thin-film substrates housed in a 2.5 x 5.1 cm (1 x 2 inch) hybrid package. The package was dry nitrogen-filled and hermetically sealed.

The thin film substrates were attached to the package bottom with epoxy. The thin film substrate and pattern network were of the same material as that used for the mechanical test samples discussed previously. Attached to the thin film substrates were one 2N2907-1 (PNP); one 2N2219-A (NPN) active chip; and 28 gold wire interconnections, 0.051 mm (2 mil) diameter, thermocompression bonded. Interconnections between the substrate and the package leads were also made with gold wire. The test specimens are described more fully in Table 10.

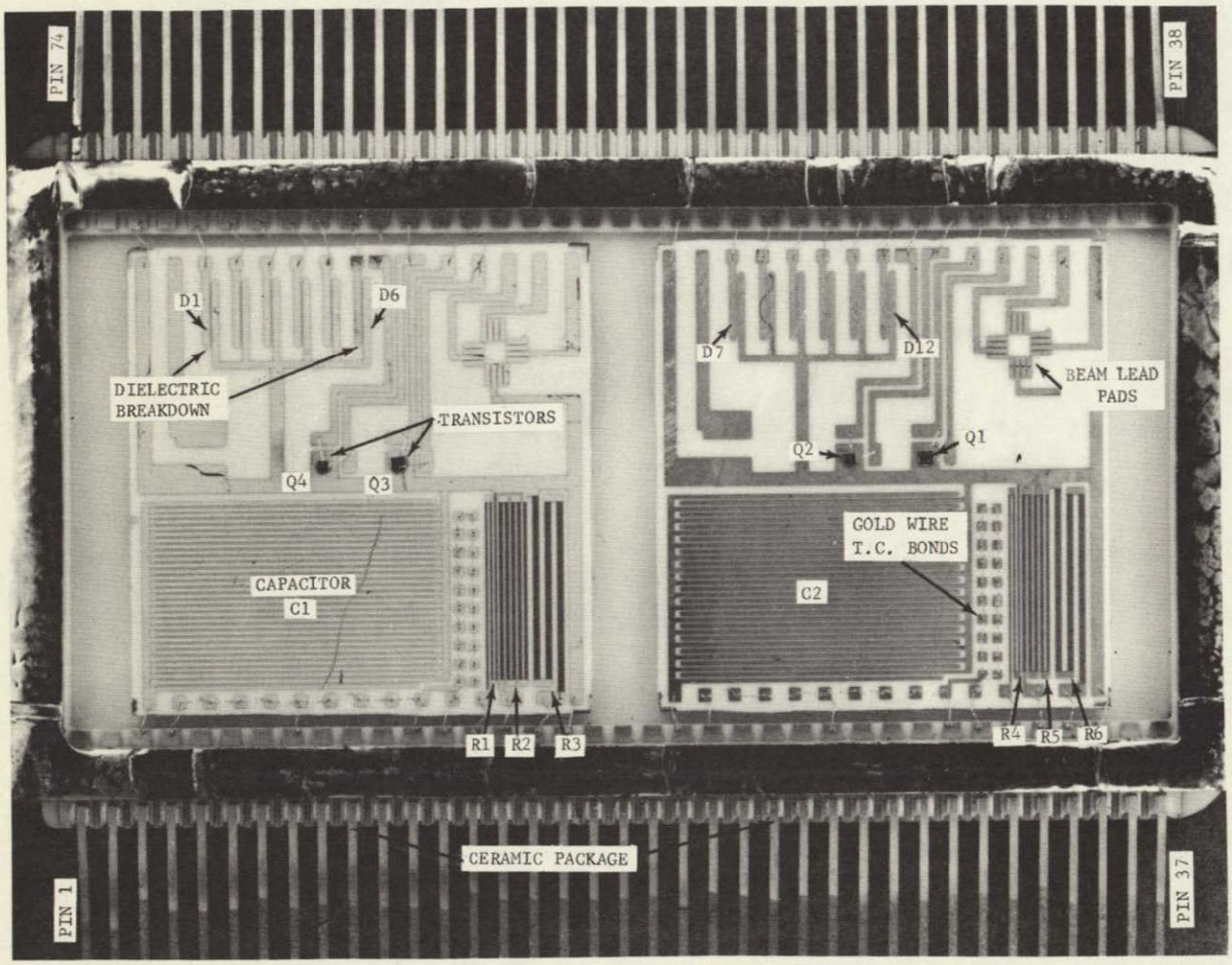

Figure 7. Electrical test specimens.

TABLE 10. DESCRIPTION OF TEST SPECIMENS USED FOR ELECTRICAL-THERMAL TEST

Part*	Description
Substrates	Two thin film substrates per package
Material	99 percent alumina
Dimensions	19.050 x 19.050 x 0.653 mm (3/4 x 3/4 x 0.025 inch)
Conductors	Plated Au/evaporated Ni/evaporated Ni Cr Dielectric breakdown patterns (6) — Interdigitated capacitor (1)
Resistors	Ni Cr, untrimmed (3) 100 Ω/□ and 225 Ω/□ resistive material
Wire bonds	Interconnected bonds (28) per substrate plus 40 leads to the package Au wire, 0.051 mm (0.002 inch) diameter, thermocompression bonded
Devices	Two transistor chips per substrate Q1 and Q3: 2N2907-1 (PNP) Q2 and A4: 2N2219-A (NPN)
Package	Ceramic package, American Lava type, 25.4 x 50.8 mm (1 x 2 inch). Hand soldered, sealed hermetically with Sn10 solder in dry nitrogen atmosphere
*A typical specimen is shown in Figure 7.	

The electrical test sequence is shown in Figure 8. Electrical tests performed before this sequence and at the designated points in Figure 8 included:

- Resistor values
- Continuity of interconnection wires

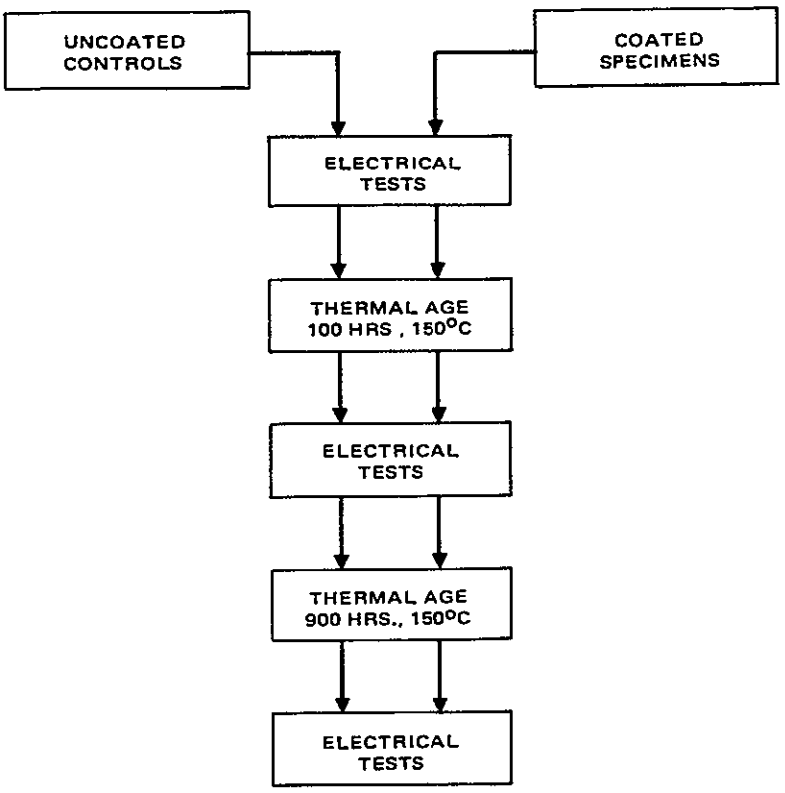

Figure 8. Electrical performance evaluation of candidate coating materials.

- Transistor gain (h_{FE})
- Transistor leakage (I_{CBO})
- Dielectric breakdown
- Insulation resistance
- Capacitance and dissipation factor (interdigitated capacitor)

In general, the results of this test indicated no degradation to the various circuit elements and very little difference between the coatings tested. Coated thin film resistors drifted about a tenth of one percent, the same amount as the uncoated control resistors. All interconnection wires survived the test intact.

The dielectric breakdown voltage for the various coatings is shown in Table 11. The coatings were found to increase the dielectric breakdown of the test pattern by two to three times. There was also a trend toward

TABLE 11. DIELECTRIC VOLTAGE BREAKDOWN OF COATED THIN FILMS IN HERMETICALLY SEALED PACKAGES

Coatings over Thin Films	Readings* in Volts		
	Initial (in Package)	Aged at 150°C	
		100 Hrs	1000 Hrs
Control (No Coating)	800	650	550
S1	1700	1700	1400
S2	2050	1700	1450
S3	1700	2000	1750
E4	1850	2050	1600
E5	1600	1850	1200
E8	1500	1200	1300

*Each reading is an average of two specimens

lower breakdown levels in most of the coatings with elevated temperature storage but this factor is not considered significant. Also considered insignificant are the different values for the different coatings because all exceed the value for normal microcircuit applications.

Insulation resistance was measured on the interdigitated capacitor C1. There were no significant differences between the coated test pattern and the uncoated control pattern; all readings were above 3×10^9 ohms after package sealing (Table 12). The insulation resistance of coating S2 dropped by an order of magnitude during elevated temperature storage: all others remained fairly constant.

The capacitance and dissipation factors were also measured on the interdigitated capacitor C1. None of the coatings was found to increase the small (25 pf) capacitance of the test pattern, and no significant increase was seen in the dissipation factor as a result of coating.

Active devices were used in this test only to uncover rather gross problems with the coatings. The devices used were not expected to uncover subtle differences between coatings because (1) devices were not chosen for sensitivity to surface contamination and (2) they were not powered during the elevated temperature storage (reverse bias was incorporated in the

TABLE 12. INSULATION RESISTANCE OF COATED THIN FILMS IN HERMETICALLY SEALED PACKAGES

Coating over Thin Films	Readings* in Megohms at 100 volts		
	Initial (in Package)	Aged at 150°C	
		100 hrs	1000 hrs
Control (No Coating)	5000K	5000K	2750K
S1	5000K	5000K	2750K
S2	4500K	875K	375K
S3	5000K	5000K	2590K
E4	>5000K	>5000K	>5000K
E5	>5000K	>5000K	>5000K
E8	3000K	>5000K	>5000K

*Each reading is an average of 2 specimens

final phase of the study). It was found that there were no significant differences between either the gain (h_{FE}) or leakage (I_{CBO}) on devices which were uncoated or coated with any of the materials tested.

1.3.9 Wire Bond Tests

To determine the effect of the coatings on the bond strength of typical microcircuit interconnection wires, the following test was performed:

1. A number of thick and thin film metallized substrates was bonded with both aluminum (ultrasonic) and gold (thermocompression) wires.
2. Initial bond strengths were measured on a sample of wires from each group.
3. The substrates were coated and cured.
4. Bond strengths were measured on the remaining (coated) wires.

Data from these measurements were reduced to yield average pull strengths and standard deviations (Table 13).

TABLE 13. EFFECT OF CANDIDATE COATINGS ON WIRE BOND STRENGTH

Coating	Substrate Type[1]	Coating B = Before A = After	Average Pull Strength[2] (gms)	Standard Deviation (gms)	Apparent Change due to Coating (%)	Change With Correction Factor[3] (%)
S1	Thin	B	10.8	1.4	-31.6	- 1.6
		A	7.4	2.1		
	Thick	B	33.4	5.4	- 0.7	- 0.7
		A	33.2	5.1		
S2	Thin	B	9.4	1.4	- 1.0	+29.0
		A	9.3	2.0		
	Thick	B	25.1	5.0	+ 5.6	+ 5.6
		A	26.5	5.0		
S3	Thin	B	9.7	2.0	+14.9	+44.9
		A	11.1	3.9		
	Thick	B	24.0	7.3	+45.8	+45.8
		A	35.0	4.7		
E4	Thin	B	9.0	2.9	+12.6	+42.6
		A	10.2	2.5		
	Thick	B	24.6	10.1	+40.0	+40.0
		A	34.5	4.8		
E5	Thin	B	11.4	1.8	+ 3.2	+33.2
		A	11.8	1.0		
	Thick	B	28.3	5.4	+17.7	+17.7
		A	33.3	3.6		
E8	Thin	B	10.1	1.3	+19.2	+49.2
		A	12.1	1.4		
	Thick	B	28.2	5.0	+22.2	+22.2
		A	34.4	6.7		

[1]Thin film substrates were bonded with 0.001 inch aluminum wires. Thick film substrates were bonded with 0.002 inch gold wires.

[2]The sample size for each sub-group was 17 to 26 wires.

[3]Assumes 30 percent bond strength degradation due to temperature exposure (i.e., coating cure cycle) for the uncoated aluminum wires and no degradation for the gold wires.

In analyzing these data, two factors should be kept in mind: First, the measured pull strengths exhibited relatively large standard deviations which need to be considered in comparing group average value differences. Second, it is a demonstrable fact that aluminum wire bonds decrease in strength with exposure to elevated temperature.[6,7,8,9] Since the coatings required a curing cycle of 150°C for six hours and since this curing cycle occurred after the initial bond strengths were measured, the second bond measurements would be expected to be lower in the absence of the coatings. The expected reduction in strength is about 30 percent. With these factors in mind, the following may be concluded from the test:

- The epoxy coatings improved wire bond strengths.
- Among the silicone coatings, S3 provided greater strengthening than S1 or S2.
- None of the coatings tested exhibited a detrimental effect on bond strength.

Throughout the candidate coating screening tests, the basis for evaluation was a comparison of the performance of the coated microcircuits with that of uncoated controls. In most cases this comparison came out favorably. In the case of voltage breakdown and wire bond strength, the coatings actually improved the performance of the uncoated comparison group.

1.4 FINAL COATING SELECTION

The results of the candidate coating screening tests were used to select the "best" two coatings for further testing to the requirements of MIL-STD-883. In weighing the comparative behavior of the various coatings, the needs of the intended application were placed foremost. In this investigation the coating was intended for protection of microcircuits contained in hermetically sealed packages. The coating was intended to be applied after the assembly, test, and repair of the microcircuit, just before the package sealing operation.

While all the coating materials were amenable to formulation and application by spraying, the E8 material was found to be significantly more difficult to mix properly. This property was evidenced also in the thermal-vacuum outgassing test, during which this material exhibited inconsistent

results, and during cleaning operations when it exhibited a tendency to absorb solvents and blister.

The weight-loss portion of the thermal-vacuum test uncovered a limitation of the S3 material. Its weight loss was rather high compared with that of the other silicone materials under test, a result that indicated incomplete curing. This result was confirmed in the solvent-resistance test; it was found that S3 required a temperature of 250°C to fully cure (in this study, 150°C was chosen as the highest acceptable curing temperature to insure no degradation to the underlying microcircuit).

Of the six coating materials chosen for screening tests, only two were found to be unacceptable: the silicone DC 62-047 WE (S3) and the epoxy ERL 4289 with HHPA (E8). The remaining coating materials (two silicones, two epoxies), although exposed to a number of rather harsh tests, displayed excellent compatibility with the microcircuit test specimens. On the basis of slight differences in overall performance, two of the candidate coatings, the silicone DC 90-711 (S1) and the epoxy ERL 4289 with dimer acid hardener (E5), were chosen for further evaluation. This evaluation was intended to expose more subtle effects of coatings on microcircuits. Further work was also required to show the performance of the selected coatings under testing to the requirements of MIL-STD-883.

Evaluation of the two selected coatings (S1 and E5) was accomplished as Task III of this program. The findings are contained in the following section.

2.0 TASK III: TEST PROGRAM

2.1 PREPARATION AND DESCRIPTION OF TEST SPECIMENS

Of the six coatings submitted to the screening tests, two were selected for final evaluation:

- S1: Dow Corning DC 90-711, a silicone
- E5: Union Carbide ERL 4289, an ultra pure epoxy with dimer acid as catalyst

Thirty-two specimens were prepared with each coating to evaluate performance under the stresses of environmental testing per MIL-STD-883. Each specimen included a thin and thick film substrate with test patterns and devices as detailed in Table 14. Figure 9 shows a typical hybrid test specimen after assembly and before sealing. The substrates were placed in a 25 x 50 mm (1 x 2 inch) ceramic package. The 32 specimens were divided into three groups: 12 coated with S1, 12 with E5, and eight controls with no coating. These groups were further divided into subgroups which had contaminants and/or repairs as shown in Figure 10.

2.1.1 Coating and Repair of Test Specimens

The coatings were sprayed and cured on all specimens except the control group. Repairs were then performed on the repair group. Repairs consisted of removing a transistor die Q2 (NPN, 2N2219-A) and a chip capacitor C2, cleaning off the area, and epoxy bonding a replacement. Aluminum wires, 0.025 mm (0.001 inch) in diameter, ultrasonically bonded, were used to interconnect the transistors. Thermocompression bonded gold

TABLE 14. DESCRIPTION OF ENVIRONMENTAL TEST SPECIMENS

Part	Thick Film	Thin Film
Substrate		
Material	96 percent alumina	99 percent alumina
Dimensions	19.050 x 19.050 x 0.635 mm (3/4 x 3/4 x 0.025 inch)	19.050 x 19.050 x 0.635 mm (3/4 x 3/4 x 0.025 inch)
Conductors	Au (ESL 8835)	Plated Au/evaporated Ni/evaporated Ni Cr. Dielectric breakdown patterns (6). Interdigitated capacitor (1).
Resistors	(ESL 3800 Series) R1, R2: 10 Ω/□ R3, R4, R5: 100 KΩ/□ R6, R7, R8: 1 KΩ/□ All resistors overglazed; R1, R3, R6 laser trimmed	Ni Cr, untrimmed (3) 100 Ω/□ and 225 Ω/□ substrates
Wire Bonds	11 aluminum 0.025 mm (0.001 inch) diameter, ultrasonic bonded 27 gold, 0.051 mm (0.002 inch) diameter thermocompression bonded	32 aluminum 0.025 mm (0.001 inch) diameter ultrasonic bonded 24 gold, 0.051 mm (0.002 inch) diameter, thermocompression bonded
Devices	Chip capacitor per Hughes Specification 93307-27C 18,000 pF, 50V	Two transistor chips Q1: 2N2907-1 (PNP) Q2: 2N2219-A (NPN)

(Continued next page)

(Table 14, concluded)

Part	Thick Film	Thin Film
Devices (cont)	1.91 x 1.27 mm (0.075 x 0.050 inch) K1200 type	One beam lead device TI No. BL54LS00Y (quad 2-input NAND gate)
Package	Ceramic package, American Lava 25.4 x 50.8 mm (1 x 2 inch). Hand solder sealed with Sn10 solder in dry nitrogen atmosphere.	

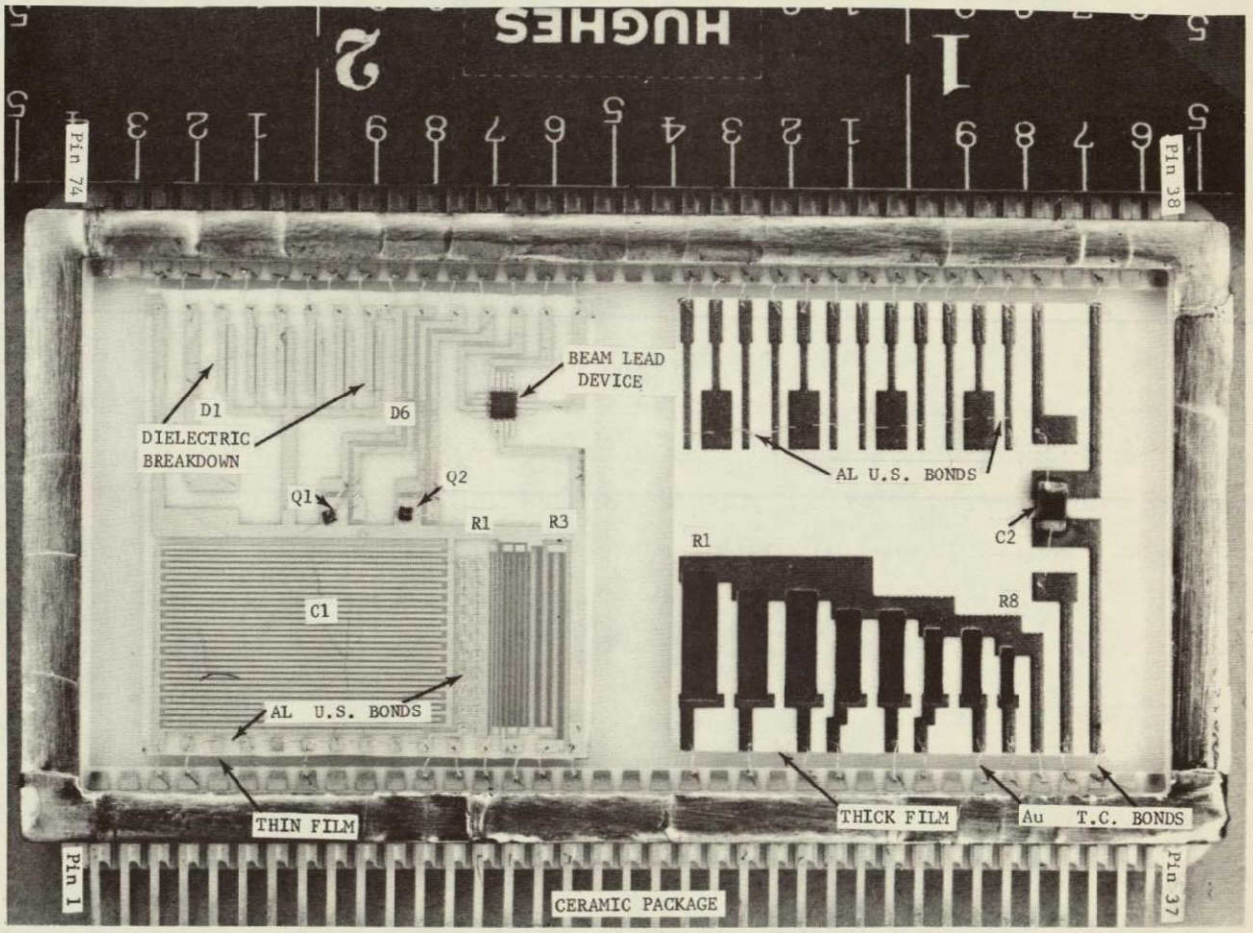

Figure 9. Test package for final coating tests.

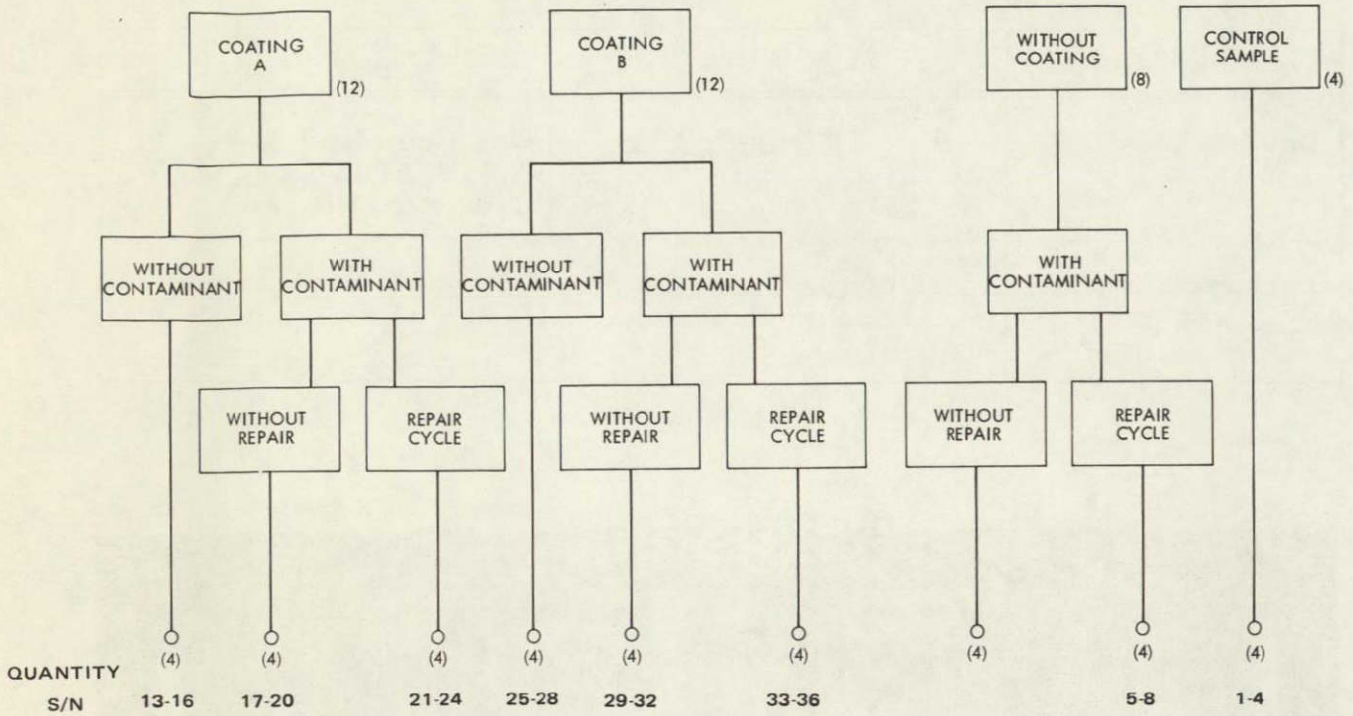

Figure 10. Test specimen lot categorization.

wire, 0.51 mm (0.002 inch) in diameter, was used for capacitor and substrates-to-package interconnection. The replaced devices were tested electrically and then recoated. Spray coating was not advisable at this stage because the overspray would cause excessive build-up in the unrepaired area. Instead, a droplet of coating material was applied to the repair region. The coatings in both cases were diluted to 60 percent solids with chemically pure toluene. The standard coating curing cycle was used.

2.1.2 Addition of Contaminants to Test Specimens

Contaminants were placed inside these packages that were designated to be contaminated. Contaminant selection was based on the conclusions from the study in Task I of the program and on discussions with the MSFC

Program Technical Manager. Each of the contaminated packages received an identical set of contaminants (Figure 11) consisting of:

- Six solder balls, 0.152 to 0.229 mm (0.006-0.009 inch in diameter
- Two pieces of aluminum wire, 0.025 mm (0.001 inch) in diameter, and 2.540 mm (0.100 inch) long
- Two pieces of gold wire, 0.051 mm (0.002 inch) in diameter, and 2.540 mm (0.100 inch) long
- About six or more assorted size broken-up pieces of silicon chips

Package sealing was preceded by a vacuum bake and a two hour, dry nitrogen bake at 150°C. Parts were hand solder-sealed with Sn10 solder (no flux) and then fine and gross leak tested. Parts that failed were repaired with Sn96 solder until all specimens passed the leak test. Figure 12 presents the sequence followed in completing the fabrication of the test specimens.

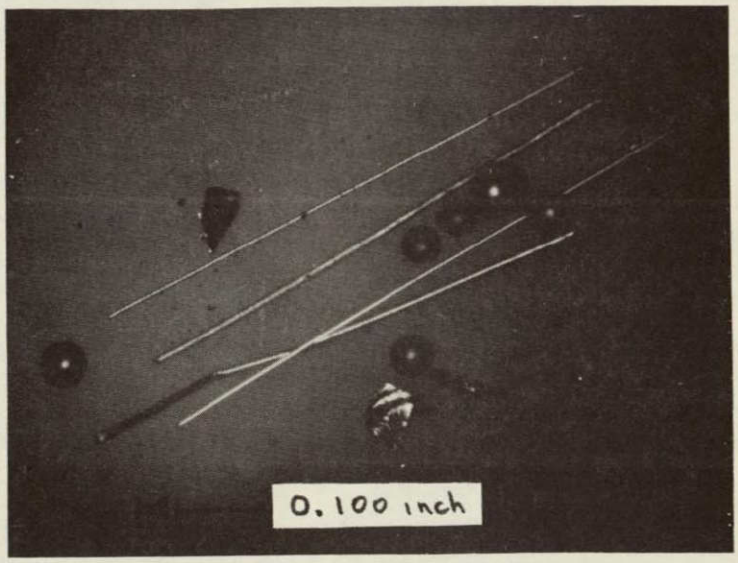

Figure 11. Set of particulate contaminants placed in test specimens.

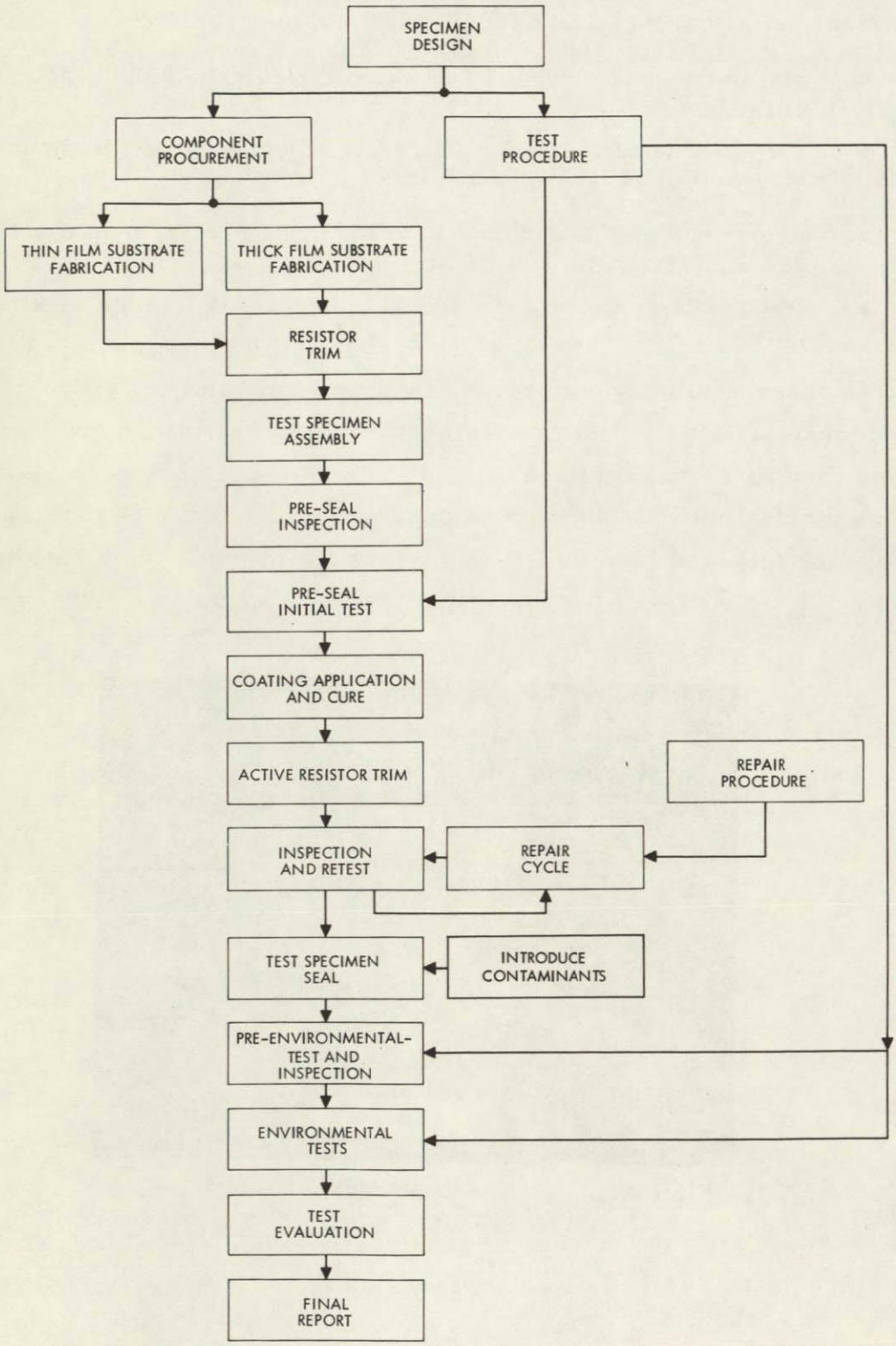

Figure 12. Test program flow sequence.

2.2 DESCRIPTION OF TEST PROCEDURES

The test program followed the sequence shown in Figure 13. A detailed description of these tests follows.

2.2.1 Leak Test

Fine leak testing was conducted per MIL-STD-883, Method 1014, by pressurizing the parts at 2 atmospheres for 2-1/2 hours in helium and using a mass spectrometer to leak test the packages within the next 30 minutes. Parts were required to leak less than 5×10^{-7} standard atmosphere cc/sec. Gross leak testing was done in fluorocarbon fluid FC 43 at 125°C.

2.2.2 PIN Test

The Particle Impact Noise (PIN) test was conducted per Hughes test procedure 908054, Rev. B. The frequency was 40 Hz and the displacement 2.54 mm (0.1 inch), or 8 g acceleration. Audio (speaker) and visual (oscilloscope) criteria were used to monitor the results.

2.2.3 Electrical Tests

The following electrical measurements were taken on each test specimen.

- Resistance value on seven thick film resistors and three thin film resistors
- Transistor parameters: h_{FE} and I_{CBO} on two transistors
- Dielectric breakdown
- Insulation resistance (of thin film interdigitated capacitor)
- Capacitance and dissipation factor at 400 Hz of the interdigitated capacitor and the chip capacitor
- Continuity tests through the ultrasonic wire bonds and the beam lead device.

The measurements were taken using the following test equipment.

- Resistance value. Five place digital ohmmeter with an accuracy of 0.01 percent.

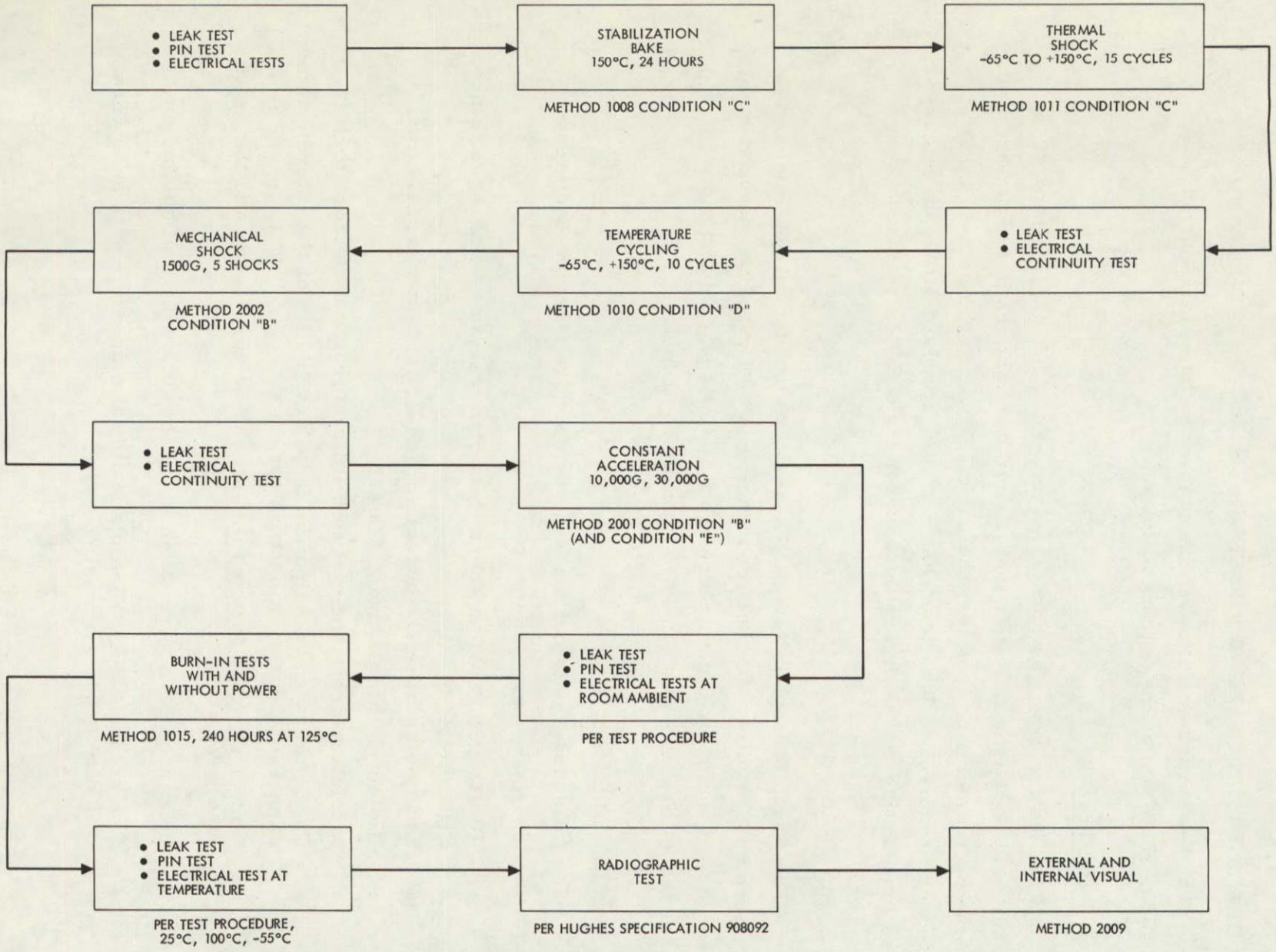

Figure 13. Environmental test flow for final test phase.
("Method" indicates per MIL-STD-883)

- Transistor parameters. The gain (i.e., h_{FE}) was measured on a Tektronix Type 575 transistor curve tracer. The specification for the two transistors used was for a minimum h_{FE} of 75. Leakage (i.e., I_{CBO}) was measured at 50 volts using a Hewlett-Packard HP 425 microammeter. The specification for Q1 (2N2907-1) was 20 μA maximum and for Q2 (2N2219-A), 10 μA maximum.
- Dielectric breakdown. Measured with an Associated Research Model 422 AC Hypot Tester. Breakdown tests were done on specially designed parallel conductor strips; six such strips were etched on the thin-film substrates spaced 0.127 mm (0.005 inch) apart and 6.35 mm (0.25 inch) long. Each strip was used once only.
- Insulation resistance. Measured with Industrial Instruments Model L-7 Megohmeter.
- Capacitance and dissipation factor. General Radio Automatic Capacitance Bridge Model 1673. Measurements were made at three frequencies: 120, 400, and 1000 Hz.
- Continuity tests were made using a volt-ohm-milliammeter.

2.2.4 Stabilization Bake

Stabilization baking was done in a forced draft oven at +150°C for 24 hours according to the requirements of Method 5004, para 3.1.2, of MIL-STD-883.

2.2.5 Thermal Shock

Thermal shock was done per MIL-STD-883. Condition C of Method 1011 requires liquid immersion for a minimum of 5 minutes at -65°C and +150°C with a maximum transfer time of 10 seconds, 15 cycles total. The liquids used were alcohol/dry ice and hot peanut oil.

2.2.6 Temperature Cycling

Temperature cycling consisted of ten cycles at -65 to +150°C in air. This test is much more benign than the preceding one. Indications are that it caused no additional degradation to the specimens.

2.2.7 Mechanical Shock

The specimens were subjected to five shocks at 1500 g with a Jolta Model M-500 drop tester. All parts passed this test.

2.2.8 Constant Acceleration

The acceleration level was planned to be 10,000 g. Recent test data on other similar packages had shown, however, that 10,000 g is near the upper limit that these packages can withstand. Two test specimens were subjected to 10,000 g without cracking and without any wire bonds failing. Four additional parts were placed in the centrifuge and tested: one broke up into many pieces. It was decided to subject the balance to 5,000 g in order not to risk losing any more test specimens.

To further test the coatings under high acceleration conditions, separate specimens were prepared in smaller packages as follows: thin film substrates, approximately 2.38 mm (0.094 inch) square, were epoxy bonded on TO-5 headers. A transistor was then epoxy bonded onto the substrate and aluminum wire bonds, 0.025 mm (0.001 inch) in diameter, were made between the chip and the substrate. The posts of the header were connected to the substrate with gold wire, 0.051 mm (0.002 inch) in diameter (Figure 14). A set of seven such specimens was coated with E5 and another set with S1; six were left uncoated. All parts were left unsealed to allow for visual examination. The parts were checked visually and for electrical continuity and then acceleration tested to 30,000 g. Visual and continuity tests showed no damage to any of the specimens.

2.2.9 Burn-In

Burn-in testing was conducted at +125°C for 240 hours. Half the hybrids were without power. The rest were electrically connected so that each of the transistors (Q1 and Q2) had reverse bias applied to the collector-base junction (HTRB test). The bias was 80 percent (48 volts) of the nominal 60 V breakdown voltage (V_{CB}). The bias was applied to determine whether "channeling" would occur. Channeling results in a conductive path on the

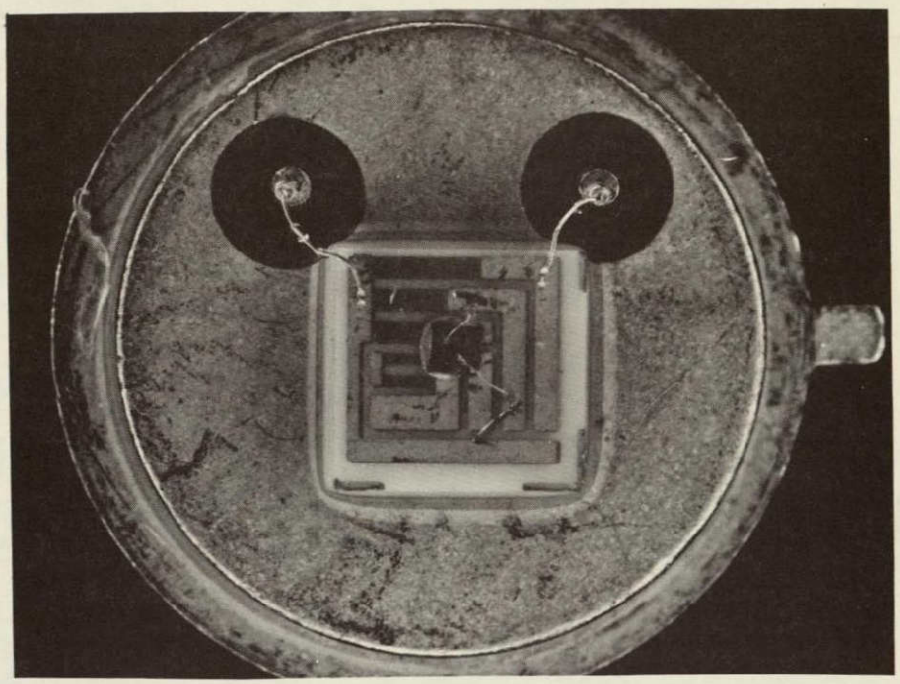

Figure 14. TO-5 header specimen for high acceleration testing (30, 000 g).

surface of the silicon chip and is thought to be caused by defective dice, surface contaminants, or unsuitable coatings. The prime purpose here, of course, was to determine whether either of the coatings would contribute to channeling compared with the uncoated control specimens. Power was applied to the parts before heating and was continued till after the parts had cooled to room temperature following the 240 hour exposure. This procedure has been found to be effective for the detection of channeling effects.

One thin film resistor, R3 (9000 ohms), of the parts biased during burn-in, was subjected to a continuous voltage of 20 V. This condition was intended to reveal possible electrolytic effects that would have resulted in the erosion of conductors and/or resistors. Such a phenomenon has been observed by others (References 4 and 5) and is attributed to ionic impurities in the epoxies.

2.2.10 Electrical Tests at Temperature

As shown in Figure 13, the final electrical tests of all transistor parameters were done at three temperatures (-55, +25, and +100°C). All other transistor electrical tests were done at room temperature.

2.2.11 Radiographic Test

X-ray photographs of all the specimens were taken, and the photographs were examined at 30X magnification.

2.2.12 External and Internal Visual

To determine any visible effects of the tests, it was necessary to remove the lid of the package. This step was done by wicking the solder off the perimeter of the lid with a soldering iron and a flux-impregnated copper braid. The presence of broken wire bonds, location of contaminants (purposely placed and otherwise), and integrity of the coating were noted.

2.3 TEST RESULTS AND DISCUSSIONS

2.3.1 Leak Tests

The leak test data are summarized in Table 15. Detailed results are provided in the appendix (Table A-1). All the failures in hermeticity occurred

TABLE 15. LEAK TEST FAILURES

Step after which Leak Test was Performed	Ratio of Failed Specimens to Total Number		
	S1 Coating	E5 Coating	Control
Sealing	0/12	0/12	0/8
Thermal shock	5/12	3/12	2/8
Mechanical shock	5/12	3/12	2/8
Acceleration	5/11	3/12	2/8
Burn-in	3/11	2/12	2/8

during thermal shock, and it is reasonable to assume that the parts which leaked (the majority of the failures were gross leak failures) that had some peanut oil in them from the high temperature bath. Interestingly, two S1-coated and one E5-coated leakers passed the leak tests after burn-in. The explanation for that is that the peanut oil polymerized during burn-in and sealed the leak. It was verified during the internal visual inspection (after lid removal) that some of the leakers had a yellowish deposit inside which was probably polymerized peanut oil.

From Table 15 it can be seen that five of 12 (42 percent) S1-coated, three of 12 (25 percent) E5-coated, and two of eight (25 percent) control specimens went through the bulk of the environmental testing as leakers. This unplanned condition allowed evaluation of the effects of the tests not only on hermetic hybrids but also on leaky hybrids.

2.3.2 PIN Test

A summary of the PIN test failures is shown in Table 16. These results are for the PIN test after the completion of burn-in. Detailed PIN test results are shown in the appendix (Table A-2).

The test specimens that contained no contaminants should all have passed the PIN test. In fact, one of the E5 specimens failed. This failure was found to be caused by a loose chip capacitor. Taking this into consideration, the results of the contaminant-free packages were as expected.

Parts with contaminants should all have failed. Three of four of the control specimens did. The coated parts, however, showed only one out of eight failures. This result indicated that the coatings served to hold the

TABLE 16. PIN TEST RESULTS AFTER BURN-IN

Condition	Ratio of Failed Specimens to Total Number		
	S1	E5	Control
Without contaminants	0/3	1/4	0/4
With contaminants	1/8	1/8	3/4

contaminants and keep them from moving about inside the package. This conclusion was verified when the packages were opened and inspected.

2.3.3 Thick and Thin Film Resistor Test

The percentage changes in the resistors are shown in Table 17. More extensive data are in the appendix (Table A-3). Twelve specimens were coated with S1 and 12 with E5; there were eight control specimens. Each specimen contained three thin film and eight thick film resistors.

The total percentage changes in the resistors were within acceptable limits for the thin film and thick film resistors with the possible exception of the 10 Ω/□ thick film resistor, which averaged about 1 percent change after all the environmental tests. This is not unexpected, as the 10 Ω/□ ink is the least stable of the three ink types used. Also, the measurement error is greater on the low value resistors (about 0.5 percent). There were no significant differences in the resistor changes of specimens which leaked and those which did not. The main conclusion that can be drawn from Table 17 is that there was no significant difference between either of the sets of coated specimens (S1 and E5) and the control specimens. It can thus be deduced that the coatings do not significantly affect thin or thick film resistors.

TABLE 17. RESISTOR CHANGES AFTER COMPLETION OF ENVIRONMENTAL TESTS

Type of Resistor	Total Percentage Change		
	Twelve S1 Specimens	Twelve E5 Specimens	Eight Control Specimens
Thin Film	0.06%	0.04%	0.04%
Thick Film			
10 Ω/□	1.03%	1.02%	0.90%
1 KΩ/□	0.01%	0.01%	-0.01%
100 KΩ/□	0.00%	0.02%	0 02%

Table 18 displays the values for thin film resistor R3 before and after burn-in. This resistor was powered at 20 milliwatts for 240 hours at an ambient of +125°C. The voltage field from this resistor to the adjacent conductor was intended to determine the electrolytic effects of the coatings. Resistor R3 stability is compared to the stability of the same resistor on

TABLE 18. EFFECT OF BURN-IN ON RESISTOR R3

All resistance values are in kilohms.

Coating	With Power				Without Power			
	Number	Before BI	After BI	%ΔR	Number	Before BI	After BI	%ΔR
S1	14	16.934	16.934	0.00	16	9.9369	9.9377	0.01
	15	15.947	15.948	0.01	19	18.733	18.734	0.01
	17	9.4777	9.4787	0.01	20	17.421	17.425	0.02
	18	20.712	20.715	0.01	23	19.325	19.328	0.02
	21	9.6030	9.6053	0.02	24	14.153	14.153	0.00
	22	18.143	18.150	0.04				
	Average Change %			0.015	Average Change %			0.01
E5	26	15.021	15.015	-0.04	25	13.344	13.344	0.00
	27	17.853	17.857	0.02	28	15.547	15.547	0.00
	30	9.2470	9.2484	0.02	29	15.127	15.130	0.02
	31	8.8165	8.8172	0.01	32	14.902	14.903	0.01
	35	14.541	14.544	0.02	33	13.851	13.854	0.02
	36	16.185	16.189	0.02	34	16.463	16.466	0.02
	Average Change %			0.02	Average Change %			0.01
Control	2	16.369	16.370	0.01	1	18.273	18.274	0.01
	3	15.416	15.418	0.01	4	16.200	16.204	0.02
	5	15.952	15.953	0.01	6	16.258	16.258	0.00
	8	8.6211	8.6214	0.00	7	18.416	18.417	0.01
	Average Change %			0.01	Average Change %			0.01

specimens that did not have power applied during burn-in. The average change for S1 with power is 0.015 percent and without power, 0.01 percent. For E5 it is 0.02 percent and 0.01 percent without. For the controls it is the same (as it should be). The percentage changes in resistance values with and without power were so slight that they can be attributed to the inaccuracy of the measuring instrument or to the heating effect of the applied power. For example, the average percentage difference in the resistors coated with S1 with and without power is only 0.005 percent (i.e., 0.015 percent minus 0.01 percent). For a 20,000 ohm resistor, this is only 1 ohm. Since the resistors appeared to exhibit no visual change (i.e., such as corrosion) and since the change in resistance was so small, it must be concluded that, from a practical standpoint, there was no significant difference due to the coatings and that neither coating exhibited any electrolytic effect.

2.3.4 Transistor Tests

A summation of the results of the HTRB (high temperature reverse bias) burn-in test on the PNP and NPN transistors is shown in Table 19. Detailed results are given in Table A-4 of the appendix.

TABLE 19. RESULTS OF TRANSISTOR ELECTRICAL TESTS

Identification of Transistor	Sample Size	Number of Failures			Total No. of Failures	Remarks
		After Sealing	After Acceleration	After HTRB Burn-in		
Coated with S1	22	0	1	0	1	Open wire bond
Coated with E5	24	1(1)	0	4(2)	5	(1) Open wire bond (2) Three of the 4 failures were wire bonds. The other was a high I_{CBO}.
Not coated	16	0	0	0	0	

A total of six failures out of 62 transistors occurred. Of the six failures, however, five were wire bond failures. Only one failure was a transistor electrical failure (i.e., excessive leakage current I_{CBO}). It would thus appear that the E5 epoxy coating is possibly more degrading to aluminum ultrasonic wire bonds than the S1 silicone coating, but it cannot be concluded that the E5 coating is more harmful to active devices. This result, in fact, is shown to be exactly the case in a later discussion of the wire bond test results, in which the E5 was found to be the poorer of the two coatings. Although stronger, E5 is unyielding under thermal differences.

Discounting all wire bond-related failures, only one failure of 24 (i.e., 4 percent) can be attributed to any sort of "channeling" or other semiconductor surface phenomenon caused by the silicone or epoxy coatings. This single failure occurred on an NPN chip coated with the epoxy E5. It is felt that this is too small a sample size from which to draw any firm conclusions on the effects of the coating. For this reason, it is concluded that there was no difference in transistor electrical failures regardless of whether:

1. The transistor was NPN or PNP
2. The package was hermetic or was a leaker
3. The package was deliberately filled with contaminants
4. The transistor had been repaired
5. The transistor was coated with S1, E5, or not coated.

2.3.5 Dielectric Breakdown Test

The results of the dielectric breakdown test are summarized in Table 20. These results represent the voltage breakdown values observed after the completion of the environmental tests listed previously in Figure 13.

These data show an increase in voltage breakdown as a result of the coating. Although the S1 coating may appear slightly superior to E5, the nature of this test and the accuracy of the Hypot tester would negate such a slight difference in average readings (i.e., 1200 volts V versus 1166 V).

TABLE 20. DIELECTRIC BREAKDOWN TEST RESULTS

Item	Voltage Breakdown Values, volts		
	S1 Coating	E5 Coating	Control (No coating)
Average breakdown voltage	1200	1166	737
Standard deviation	126	293	358
Number of specimens	11	12	8
Minimum reading	1000	600	500
Maximum reading	1400	1400	1600

There appears no question, however, that both coatings were considerably better than no coating at all. The results were about the same whether the packages were hermetic or not. The dielectric breakdown of all the specimens showed a marked improvement after the parts were sealed in dry nitrogen.

2.3.6 Insulation Resistance Test

The interdigitated capacitor C1 (see Figure 9) was used for checking the insulation resistance. As with all the other electrical measurements, readings were taken before coating, after sealing, after acceleration testing, and after burn-in. The data show that the majority of specimens, coated and uncoated, exceeded 5×10^{12} ohms, which was the upper limit of the measuring instrument. In essence, this test gave no negative information, since none of the parts failed. The insulation resistance of the alumina substrate was improved slightly by coating with either S1 or E5 on 25 percent of the samples. On only two samples did the coating lower the insulation resistance. S1 appeared to be better than E5. The actual readings are given in Table A-5 in the appendix.

2.3.7 Capacitance Test

The test results on the chip capacitor and the interdigitated planar capacitor are given in Table 21. Specific capacitance reading for each of the

TABLE 21. AVERAGE PERCENTAGE CAPACITANCE CHANGE

Type of Capacitor	Average Capacitance Change, percent		
	Coated with S1	Coated with E5	Control (No Coating)
C1 — Interdigitated thin film capacitor (approximate value = 25 picofarads)	+7 σ = 5.5	+1.04 σ = 4.48	+2.55 σ = 8.74
C2 — Chip capacitor (approximate value = 17 nanofarads)	+0.09 σ = 1.04	-0.39 σ = 1.93	+1.01 σ = 0.32

62 capacitors tested are given in Table A-6 in the appendix. The values in Table 21 represent the average percentage capacitance change (and standard deviation) of the specimens before coating until after completion of all the environmental tests. The value of the thin film interdigitated capacitor was found to be about 25 pf and was subject to a rather large measurement error. This accounts for the large scatter in the data. The chip capacitor value was much higher and yielded more accurate measurements. The results indicate no significant variation between the three groups. Measurements of the dissipation factor were also made but did not yield any meaningful data and therefore are omitted from this report.

2.3.8 Wire Bond Continuity Test

Each specimen had 28 aluminum wires and 40 gold wires. All wire bonds were pretested before sealing by nondestructively pulling the loops. Aluminum wires were nondestructively pulled with a 1 gm force and gold wires with 3 gms. Electrical continuity tests and visual examination of the specimens after completion of environmental exposure revealed a number of broken wire bonds. The results are given in Table 22. These data indicate that the E5 epoxy coating caused 10 percent aluminum wire bond failures and no gold wire failures. S1 was better than E5, having only 3.6 percent

TABLE 22. SUMMARY OF INTERCONNECTION FAILURES DUE TO ENVIRONMENTAL TESTING

Item	S1 Coating	E5 Coating	Control (No Coating)
Number of aluminum wire failures	11	31	3
Total number of aluminum wires	308	308	196
Percentage of aluminum wire failures	3.6%	10.0%	1.5%
Number of gold wire failures	1	0	0
Total number of gold wires	440	440	280
Percentage of gold wire failures	0.2%	0%	0%
Number of beam lead failures	0	0	0
Total number of beam lead devices	12	12	8
Percentage of failures	0%	0%	0%

aluminum wire failures and 0.2 percent gold wire failures. The controls were best with 1.5 percent aluminum wire failures and no gold wire failures. There were no beam lead device bond failures.

It should be noted that practically all the wire bond failures occurred in packages that exhibited gross leaks. Thus moisture could have entered these packages and contributed to the wire bond failures. If this was the case, it would appear that the coatings did not protect the wire bonds from this moisture or other atmospheric contaminant.

2.3.9 Final Visual Inspection

When all tests were completed, the parts were X-rayed, delidded, and inspected. This allowed determination of the exact number of wire bond failures, because most continuity loops contained more than one wire. It was found in one of the E5 coated specimens that a chip capacitor had detached from the substrate. It is not known when this failure occurred but it did result in destroying practically all of the wire bonds in that specimen. It would appear that the epoxy coating does not insure against chip components coming loose. Similarly, one of the control specimens also contained a loose chip capacitor, and here too, the loose wire bonds were discounted, although the transistors and the wires were unaffected.

Visual examination of the coated specimens showed that in both the S1 and E5 specimens the purposely introduced contaminants such as wires, pieces of silicone, and solder balls adhered fairly well to the coating and seemed to be immobilized. They were not, however, in electrical contact with the substrate to cause circuit malfunctions. The contaminants were placed in the package after coating. The PIN test results confirm the conclusion that the coatings serve as a kind of "flypaper," entrapping contaminants on their surface. The coatings would probably immobilize contaminants under them.

Visual inspection also verified that some of the leak failures had peanut oil in them. The peanut oil had solidified, probably as a result of the burn-in, and appeared as a yellowish coating or a stain on the circuit and inside the cover. As previously mentioned, no direct correlation was found between the presence of a leak and electrical degradation. The coatings appeared unaffected by any of the tests and were still smooth and continuous. ES had darkened slightly.

The X-rays made before delidding showed the dislocated capacitors. Broken wire bonds were undetectable, and aluminum wires were not visible. Gold wires were visible, as were the solder ball contaminants (see Figures 15 and 16). As an inspection tool, X-rays are of limited usefulness.

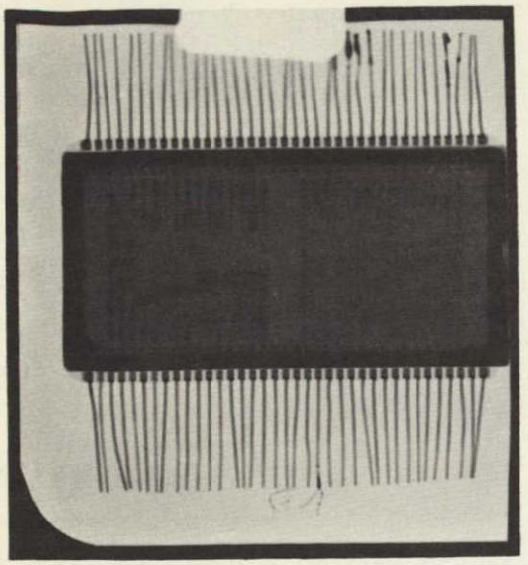

Figure 15. X-ray photograph of specimen No. 8 showing:

1. capacitor chip dislodged, lower left-hand corner
2. broken solder seal, middle right-hand side
3. contaminants (solder balls), lower left corner

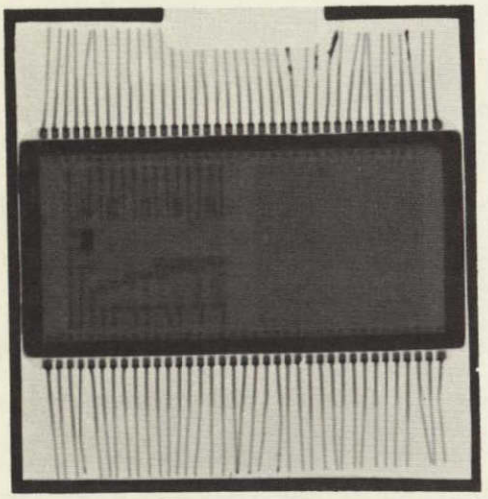

Figure 16. X-ray photograph of specimen No. 20 showing contaminants:

1. gold wire, far right
2. solder balls, middle left

3.0 CONCLUSIONS

As a result of the efforts on Tasks II and III, the following conclusions were reached.

- Both the epoxy and silicone coatings entrapped contaminants on their surfaces and prevented such contaminants (e.g., solder balls, loose wires, etc.) from causing either electrical or mechanical damage inside the sealed hybrid.
- Neither coating caused any significant effect (good or bad) on either thick film or thin film resistors. No electrolytic or visual effect was noticed on any of the coated resistors, even after power-on tests at +125°C. Coated resistors could be trimmed through the coating.
- Neither coating caused any degradation in the electrical properties of either NPN or PNP transistor chips, even after a 240 hour high temperature reverse bias test.
- Neither coating caused any degradation in the electrical or mechanical properties of capacitor chips.
- Both coatings appeared to adversely affect aluminum ultrasonic wire bonds, but not gold thermocompression wire bonds. The effect was noticed after thermal shock and, in some instances, after mechanical shock and acceleration. The epoxy coating was worse than the silicone coating.
- Both coatings had adequate electrical properties, such as dielectric breakdown strength (300 to 400 volts per mil) and insulation resistance ($>5 \times 10^{12}$ ohms).
- Both coatings could be applied evenly by spraying and could subsequently be removed for rework.
- Both coatings were sufficiently flexible to withstand normal stresses encountered in thermal shock and temperature cycling, and both could withstand the normal solvents used in hybrid cleaning processes.
- Although both coatings outgassed to some extent after 1000 hours at +150°C, the outgassing products were not considered harmful.

- The coatings were chemically stable in air for 10 minutes at +200°C, for 30 minutes at +175°C, and for 1000 hours at +150°C. They did not degrade, melt, or discolor under any of the environmental exposures.

Finally, the silicone coating appeared to be slightly superior to the epoxy coating; the difference, however, was slight. The basic purpose of the coating was to protect the hybrid microcircuit from contamination — to "passivate" the hybrid. A secondary purpose was to immobilize particles. Both coatings performed these functions, and both coatings were electrically and thermally stable. The coatings improved even the dielectric strength of the substrate. Nevertheless, the test specimens without coatings performed as well, or better, than the coated specimens. The coatings do appear to have a slight adverse affect on wire bonds and on certain thick film resistors.

A decision concerning the utilization of coatings in microcircuits needs to be made on an individual circuit (or perhaps process) basis. The benefit gained in protection from loose particles needs to be weighed against the required additional processing cost and the minor adverse effects incurred by the use of coatings.

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APPENDIX

CONTENTS

TABLE A-1. LEAK TEST RESULTS

Specimen Description			Fine Leak Test (atm. cc/sec.) and Gross Leak Test Results (Pass or Fail)[3]				
No.	Coating	Cont & Repair[4]	After Sealing	Thermal Shock	Mechanical Shock	Acceleration	Burn-in
13	S1		2.0×10^{-9} P*	3.0×10^{-8} P	4.0×10^{-9} P	Note (1)	
14			3.2×10^{-9} P	3.2×10^{-8} P	7.0×10^{-9} P	3.5×10^{-9} P	4.4×10^{-8} P
15			3.0×10^{-9} P	3.0×10^{-8} P	4.2×10^{-9} P	9.0×10^{-9} P	9.2×10^{-9} P
16			1.0×10^{-9} P*	2.2×10^{-8} P	3.8×10^{-9} P	1.0×10^{-9} P	9.0×10^{-9} P
17		C	1.6×10^{-7} P	1.8×10^{-8} P	4.0×10^{-9} P	1.5×10^{-9} P	7.8×10^{-9} P
18		C	2.6×10^{-8} P	5.9×10^{-6} P	F	6.0×10^{-6} F	6.2×10^{-9} P (2)
19		C	2.2×10^{-9} P	2.4×10^{-8} P	9.6×10^{-9} P	8.0×10^{-9} P	3.0×10^{-8} P
20		C	1.6×10^{-9} P	7.6×10^{-9} P	4.0×10^{-9} P	1.8×10^{-9} P	1.4×10^{-9} P
21		CR	4.0×10^{-8} P	F F	F	F F	5.2×10^{-6} F
22		CR	5.4×10^{-9} P	F F	F	F	9.2×10^{-9} P (2)
23		CR	3.8×10^{-8} P	F F	F	F	P F
24		CR	1.0×10^{-9} P	F F	F	F	P F

(Continued next page)

*Indicates reworked packages

Note 1: This part broke during acceleration testing.

Note 2: These parts were checked twice and did pass gross leak test.

Note 3: P = pass; F = fail .

Note 4: C = contaminants deliberately placed inside these packages

CR = contaminants inside package and Q2 and C2 replaced and recoated prior to sealing package, simulating repair

(Table A-1, concluded)

Specimen Description			Fine Leak Test (Atm. cc/sec.) and Gross Leak Test Results (Pass or Fail)[3]				
No	Coating	Cont & Repair[4]	After Sealing	Thermal Shock	Mechanical Shock	Acceleration	Burn-in
25	E5		4.2×10^{-8} P*	2.4×10^{-9} P	5.0×10^{-9} P	1.8×10^{-9} P	1.4×10^{-8} P
26			7.4×10^{-9} P	2.4×10^{-9} P	8.4×10^{-9} P	4.8×10^{-9} P	5.2×10^{-9} P
27			7.2×10^{-8} P	1.6×10^{-9} P	4.2×10^{-9} P	2.0×10^{-9} P	5.4×10^{-9} P
28			5.0×10^{-9} P	1.0×10^{-9} P	3.0×10^{-9} P	1.6×10^{-9} P	5.0×10^{-9} P
29		C	3.4×10^{-9} P	F F	F	F	P F
30		C	1.2×10^{-9} P	F F	F	F	1.2×10^{-8} F
31		C	1.5×10^{-9} P	1.2×10^{-9} P	3.8×10^{-9} P	1.0×10^{-9} P	4.2×10^{9} P
32		C	1.0×10^{-9} P	1.7×10^{-9} P	3.4×10^{-9} P	1.2×10^{-9} P	2.8×10^{-8} P
33		CR	4.0×10^{-8} P	1.2×10^{-9} P	3.0×10^{-9} P	0.8×10^{-9} P	1.4×10^{-9} P
34		CR	1.2×10^{-9} P	2.4×10^{9} P	4.2×10^{-9} P	2.2×10^{-9} P	1.0×10^{-9} P
35		CR	3.0×10^{-8} P	2.0×10^{-7} P	? P	9.4×10^{-9} P	3.8×10^{-9} P
36		CR	4.2×10^{-8} P	F F	F F	F F	4.6×10^{-9} P (2)
1	Control		6.4×10^{-9} P*	3.2×10^{-8} P	4.4×10^{-9} P	4.4×10^{-9} P	2.0×10^{-8} P
2			5.0×10^{-9} P*	6.2×10^{-9} P	7.8×10^{-9} P	1.4×10^{-8} P	1.7×10^{-7} P
3			4.8×10^{-7} P*	6.0×10^{-6} P	F F	6.0×10^{-7} F	6.0×10^{-6} F
4			2.8×10^{-9} P*	2.8×10^{-8} P	6.0×10^{-9} P	4.2×10^{-9} P	1.2×10^{-8} P
5		C	1.0×10^{-9} P	2.8×10^{-8} P	5.0×10^{-9} P	2.0×10^{-9} P	5.0×10^{-8} P
6		C	1.0×10^{-8} P	1.5×10^{-9} P	3.2×10^{-9} P	2.2×10^{-8} P	2.0×10^{-9} P
7		C	1.0×10^{-9} P	2.5×10^{-9}	3.4×10^{-9} P	2.0×10^{-9} P	8.0×10^{-9} P
8		C	8.8×10^{-9} P	F F	F F	1.0×10^{9} F	4.2×10^{-6} P

*Indicates reworked packages

TABLE A-2. PIN TEST RESULTS

Specimen Description			PIN Test Results		
No.	Coating	Cont. & Repair ①	After Sealing	After Acceleration	After burn-in
13	S1		P	broke-up during accel*	-
14			P	P	P
15			P	P	P
16			P	P	P
17		C	P	P*	P
18		C	F	P	F
19		C	F	P	P
20		C	P	P	P
21		CR	P	P	P
22		CR	P	P	P
23		CR	P	P	P
24		CR	P	P	P
25	E5		P	F	F
26			F	P	P
27			P	F	P
28			P	F	P
29		C	P	P	P
30		C	F	P	P
31		C	P	F	P
32		C	P	F	P
33		CR	F	F	P
34		CR	F	F	F
35		CR	P	F	P
36		CR	F	P	P
1	Control		F	F*	P
2			P	P*	P
3			F	F*	P
4			P	F*	P
5		C	F	F	F
6		C	F	F	F
7		C	F	F	F
8		C	P	P	P

*These parts were subjected to 10,000 g. All others 5,000 g.

① C: contaminants deliberately placed inside the package
R: repairs made prior to sealing - Q2 & C2 replaced
P = Pass; F = Fail

TABLE A-3. EFFECT OF COATINGS ON RESISTORS – PERCENT CHANGE AFTER ENVIRONMENTAL TESTING

Specimen	Part No.	Thin Film Resistors			Thick Film Resistors							
					10 ohm/sq. ink		1 KΩ/sq. ink			100 KΩ/sq. ink		
		R1	R2	R3	R1	R2	R6	R7	R8	R3	R4	R5
S1 Coating	14	.04	.03	.02	1.16	52	.05	02	.03	.02	.01	.00
	15	.04	.03	.02	.60	.98	.05	.02	.01	.04	.02	.03
	16	.04	.04	.06	4.33	.27	.09	-.20	-.38	.01	.00	.00
	17	.04	.02	.05	1.41	1.59	.05	.03	.03	.01	.01	.00
	(1) (18)	.06	.04	.03	.62	.94	04	.02	.02	-.03	-.03	-.03
	19	.03	.03	.02	1.03	1.00	.06	.01	.01	.02	.00	.00
	20	.44	.13	.14	.60	1.01	-.04	.15	.03	.01	.00	.00
	(21)	.06	.04	.06	1.39	1.02	.04	.01	.02		.02	.01
	(22)	.11	.05	.06	.67	1.07	.15	.00	.02	.04	-.02	-.03
	(23)	.09	.04	.04	.43	.18	-.02	-.01	-.01	.01	-.01	.00
	(24)	.04	.03	.03	.74	1.09	.00	-.02	-.02	.00	.00	.00
Average % ΔR		.06%			1.03%		.01%			.00%		
Standard deviation		σ = .07			σ = .82		σ = .09			σ = .02		

(1) Circled specimens were leakers

(Continued next page)

(Table A-3, continued)

Specimen	Part No.	Thin Film Resistors			Thick Film Resistors							
					10 ohm/sq. ink		1 K Ω/sq. ink			100 K Ω/sq. ink		
		R1	R2	R3	R1	R2	R6	R7	R8	R3	R4	R5
E5 Coating	25	.03	.03	.03	.75	1.00	.18	.01	.02	.09	.00	.01
	26	.04	.03	.03	.88	1.16	.22	.02	.01		.03	.03
	27	.03	.03	.03	2.10	1.21	.03	-.02	-.02	.02	.01	.01
	28	.03	.02	.02	1.00	1.02		-.03	-.02	.02	.01	.00
	(29)	.04	.04	.03	.75	.58	.02	.00	-.01	-.05	.01	.01
	(30)	.01	.04	.04	.48	+.55	.03	.00	-.01	-.02	-.01	.00
	31	.03	.02	.01	1.66	1.53	.20	-.01	-.01	.18	-.01	.06
	32	.03	.04	.03	.80	1.06	.01	-.02	-.01	.01	.02	.00
	33	.04	.04	.04	.81	1.17	-.01	-.04	-.11	.02	.01	-.01
	34	.06	.06	.06	1.21	.88	.04	-.01	.00	.03	.02	.02
	35	.06	.05	.06	.72	1.32	-.02	-.01	-.01	.07	.02	.02
	(36)	.05	.04	.06	.86	1.05	.15	-.01	.00	.02	.01	.01
Average % ΔR		.04%			1.02%		.01%			.02%		
Standard deviation		σ = .01			σ = .37		σ = .07			σ = .04		

(1) Circled specimens were leakers

(Continued next page)

(Table A-3, concluded)

Specimen	Part No.	Thin Film Resistors			Thick Film Resistors							
					10 ohm/sq. ink		1 K Ω/sq. ink			100 K Ω/sq. ink		
		R1	R2	R3	R1	R2	R6	R7	R8	R3	R4	R5
Control (no coating)	1	.03	.03	.02	.67	1.44	-.30	-.24		-.19		-.51
	2	.04	.04	.02	1.01	1.43	.05	.02	.02	.02	.00	.01
	(3)	.05	.05	.03	.80	1.24	-.04	-.02	-.15	-.07	.31	.33
	4		.05	.03	.95	1.34	.05	.01	.01	.03	.01	.01
	5	.03	.01	.02	.77	.90	.03	.02	.02	.03	.02	.01
	6	.04	.04	.02	.83	.80	.07	.01	.02	.04	.02	.02
	7	.17	.03	.02	1.02	.87	.05	.02	.01	.03	.39	.00
	(8)	.03	.03	.05	.47	-.19	.03	.02	.03	.01	-.01	-.01
Average % ΔR		.04%			.90%		-.019%			.02%		
Standard deviation		σ = .03			σ = .40		σ = .09			σ = .17		

(1) Circled specimens were leakers

TABLE A-4. TRANSISTOR TEST RESULTS

All transistors pass initial tests before coating.

No.	Coating	Contam Repair	Transistor	After Sealing		Acceleration		Burn-in		
				h_{FE}	I_{CBO}	h_{FE}	I_{CBO}	Bias Applied	h_{FE}	I_{CBO}
13	S1		Q1	P	P	Package broke-up in Accel.				
			Q2	P	P					
14			Q1	P	P	P	P	Yes	P	P
			Q2	P	P	P	P		P	P
15			Q1	P	P	P	P	Yes	P	P
			Q2	P	P	P	P		P	P
16			Q1	P	P	P	P	No	P	P
			Q2	P	P	P	P		P	P
17		C	Q1	P	P	P	P	Yes	P	P
(1)			Q2	P	P	P	P		P	P
18		C	Q1	P	P	P	P	Yes	P	P
			Q2	P	P	P	P		P	P
19		C	Q1	P	P	P	P	No	P	P
			Q2	P	P	P	P		P	P
20		C	Q1	P	P	P	P	No	P	P
			Q2	P	P	P	P		P	P
21		CR	Q1	P	P	P	P	Yes	P	P
			Q2	P	P	Open	P		Open	P
22		CR	Q1	P	P	P	P	Yes	P	P
			Q2	P	P	P	P		P	P
23		CR	Q1	P	P	P	P	No	P	P
			Q2	P	P	P	P		P	P
24		CR	Q1	P	P	P	P	No	P	P
			Q2	P	P	P	P		P	P

Q1: 2N2907-1 PNP - h_{FE}: 75 min (@ 10v, 10 mA) I_{CBO}: 20 μA @ 50v

Q2: 2N2219-A NPN - h_{FE}: 75 min (@ 10v, 10 mA) I_{CBO}: 10 μA @ 50v

(1) Circled parts are leakers. All others are hermetic.

(2) Broken wire bond

(3) External C-E short

(Continued next page)

(Table A-4, continued)

No.	Coating	Contam Repair	Transistor	After Sealing		Acceleration		Burn-in		
				h_{FE}	I_{CBO}	h_{FE}	I_{CBO}	Bias Applied	h_{FE}	I_{CBO}
25	E5		Q1	P	P	P	P	No	Open	Open (2)
			Q2	Open	P	Open	P		Open	P
26			Q1	P	P	P	P	Yes	P	P
			Q2	P	P	P	P		P	P
27			Q1	P	P	P	P	Yes	P	P
			Q2	P	P	P	P		P (3)	P
28			Q1	P	P	P	P	No	F (3)	P
			Q2	P	P	P	P		P	P
(29)	E5	C	Q1	P	P	P	P	No	P	P
			Q2	P	P	P	P		P	P
(30)		C	Q1	P	P	F	P	Yes	?	P
			Q2	P	P	P	P		P	P
31		C	Q1	P	P	P	P	Yes	P	P
			Q2	P	P	P	P		F	F
32		C	Q1	P	P	P	P	No	P	P
			Q2	P	P	P	P		P	P
33		CR	Q1	P	P	P	P	No	P	P
			Q2	P	P	P	P		P	P
34		CR	Q1	P	P	P	P	No	P	P
			Q2	P	P	P	P		P	P
35		CR	Q1	P	P	P	P	Yes	P	P
			Q2	P	P	P	P		P	P
36		CR	Q1	P	P	P	P	Yes	P	P
			Q2	P	P	P	P		Open	Open*
1	C		Q1	P	P	P	P	No	P	P
	O		Q2	P	P	P	P		P	P
2	N		Q1	P	P	P	P	Yes	P	P
	T		Q2	P	P	P	P		P	P
(3)	R		Q1	P	P	P	P	Yes	P	P
	O		Q2	P	P	P	P		P	P
4	L		Q1	P	P	P	P	No	P	P
			Q2	P	P	P	P		P	P

Q1: 2N2907-1 PNP - h_{FE}: 75 min (@ 10v, 10 mA) I_{CBO}: 20 µA @ 50v

Q2: 2N2219-A NPN - h_{FE}: 75 min (@ 10v, 10 mA) I_{CBO}: 10 µA @ 50v

(1) Circled parts are leakers. All others are hermetic.

(2) Broken wire bond

(3) External C-E short

*heavy coating

(Continued next page)

(Table A-4, concluded)

No.	Coating	Contam Repair	Transistor	After Sealing		Acceleration		Burn-in		
				h_{FE}	I_{CBO}	h_{FE}	I_{CBO}	Bias Applied	h_{FE}	I_{CBO}
5	C	C	Q1	P	P	P	P	Yes	P	P
	O		Q2	P	P	P	P		P	P
6	N	C	Q1	P	P	P	P	No	P	P
	T		Q2	P	P	P	P		P	P
7	R	C	Q1	P	P	P	P	No	P	P
	O		Q2	P	P	P	P		P	P
8	L	C	Q1	P	P	P	P	Yes	P	P
			Q2	P	P	P	P		P	P

Q1: 2N2907-1 PNP - h_{FE}: 75 min (@ 10v, 10 mA) I_{CBO}: 20 μA @ 50v

Q2: 2N2219-A NPN - h_{FE}: 75 min (@ 10v, 10 mA) I_{CBO}: 10 μA @ 50v

(1) Circled parts are leakers. All others are hermetic.

(2) Broken wire bond

(3) External C-E short

TABLE A-5. INSULATION RESISTANCE TEST RESULTS

All values in megohms

Package Number	Coating	Before Coating	After Sealing	After Acceleration	After Burn-in
13	S1	1,000 K	4,000 K	Broke	
14		>5,000 K	>5,000 K	>5,000 K	>5,000 K
15		>5,000 K	>5,000 K	>5,000 K	>5,000 K
16		1,000 K	>5,000 K	>5,000 K	>5,000 K
17		>5,000 K	>5,000 K	>5,000 K	>5,000 K
18		>5,000 K	>5,000 K	>5,000 K	>5,000 K
19		>5,000 K	>5,000 K	>5,000 K	>5,000 K
20		500 K	>5,000 K	>5,000 K	100 K
21		>5,000 K	>5,000 K	>5,000 K	>5,000 K
22		>5,000 K	>5,000 K	>5,000 K	550 K
23		>5,000 K	3,000 K	>5,000 K	>5,000 K
24		>5,000 K	>5,000 K	>5,000 K	>5,000 K
25	E5	>5,000 K	280	600	100
26		>5,000 K	>5,000 K	>5,000 K	>5,000 K
27		>5,000 K	>5,000 K	>5,000 K	>5,000 K
28		>5,000 K	>5,000 K	>5,000 K	>5,000 K
29		>5,000 K	>5,000 K	>5,000 K	>5,000 K
30		>5,000 K	>5,000 K	>5,000 K	>5,000 K
31		600 K	>5,000 K	>5,000 K	>5,000 K
32		600 K	>5,000 K	>5,000 K	12 K
33		>5,000 K	>5,000 K	>5,000 K	8 K
34		>5,000 K	>5,000 K	>5,000 K	>5,000 K
35		6	16 K	500 K	20
36		>5,000 K	>5,000 K	>5,000 K	>5,000 K
1	Control	>5,000 K	>5,000 K	>5,000 K	>5,000 K
2		500 K	>5,000 K	>5,000 K	>5,000 K
3		>5,000 K	>5,000 K	>5,000 K	>5,000 K
4		>5,000 K	>5,000 K	>5,000 K	>5,000 K
5		500 K	>5,000 K	>5,000 K	20 K
6		>5,000 K	>5,000 K	>5,000 K	>5,000 K
7		>5,000 K	>5,000 K	>5,000 K	>5,000 K
8		>5,000 K	>5,000 K	>5,000 K	>5,000 K

TABLE A-6. CAPACITANCE MEASUREMENTS

Specimen		C1 Interdigitated Thin Film (pf)				C2, K1200 Chip (values in nf)			
		Before Coating	After Burn-in	Δ%	$\bar{x}/\sigma$	Before Coating	After Burn-in	Δ%	$\bar{x}/\sigma$
S1	14	24.44	26.40	8.02		17.50	17.71	1.20	
	15	24.68	25.64	3.89		17.26	17.21	-.29	
	16	21.60	26.40	22.22		17.89	18.05	.89	
	17	21.78	24.10	10.65		17.03	17.16	.76	
	18	26.56	28.12	5.87		17.91	17.97	.34	
	19	24.97	26.15	4.73		16.99	17.23	1.41	
	20	22.31	23.08	3.45		19.16	19.35	.99	
	21	21.71	22.52	3 73		17.21	17.08	-.76	
	22	22.51	24.02	6.71		17.07	16.80	-1.58	
	23	26.14	27.09	3.63	$\bar{x}$ = 7.00%	16.93	16.79	-.83	$\bar{x}$ = .09
	24	25.45	26 50	4.13	σ = 5.5	18.01	17.81	-1.11	σ = 1.04
E5	25	24.13	24.70	2.36		16.68	detached		
	26	25.18	24.35	-3.30		17.96	18.24	1.56	
	27	24.08	25.21	4.69		17.15	17.20	.29	
	28	23.80	24.37	2.39		19.21	19.28	.36	
	29	23.19	23.62	1.85		17 11	17.15	.23	
	30	22.04	22.32	1.27		17.16	17.18	.12	
	31	23.52	23.73	.89		17.82	17.93	.62	
	32	27.50	26.26	-4.51		18.61	18.74	.70	
	33	26.76	25.14	-6.05		17.03	16.93	-.59	
	34	25.90	25.24	-2.55		17.36	17.19	-.98	
	35	24.62	26.75	8.65	$\bar{x}$ = 1.04	17.45	17.30	-.86	$\bar{x}$ = -.39
	36	22.42	23.93	6.74	σ = 4.48	17.35	16.35	-5.76	σ = 1.93
Control	1	21.54	25.30	17.46		17.97	18.22	1.39	
	2	24.51	23.75	-3.10		16.73	16.81	.48	
	3	22.44	22.42	-.09		16.55	16.72	1.03	
	4	22.54	26.04	15.53		17.20	17.40	1.16	
	5	23.81	23.14	-2.81		18.93	19.07	.74	
	6	22.18	22.07	-.50		17.53	17.70	.97	
	7	23.34	22.28	-4.54	$\bar{x}$ = 2.55	19.47	19.72	1.28	$\bar{x}$ = 1.01
	8	22.90	22.54	-1.57	σ = 8.74	18.19	detached		σ = .32