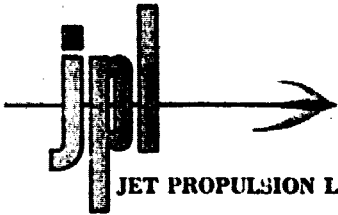# General Disclaimer

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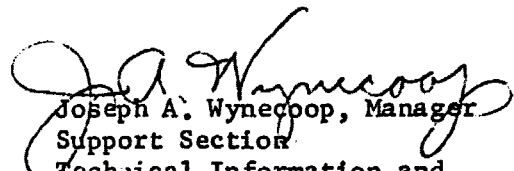Maryland 21240

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954145 J.H. Gustincic, Consulting Engr. - Final Report, 25 November 1975

954290 Solarex Corporation - 1st Quarterly Report, December 1975

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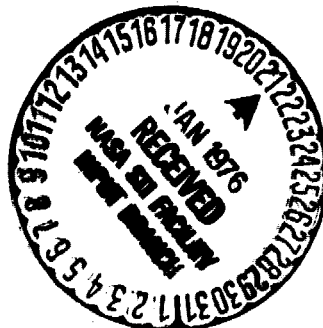
(NASA-CR-146080) DEVELOPMENT OF A HIGH
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Quarterly Report (Solarex Corp., Rockville,
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DEVELOPMENT OF A HIGH EFFICIENCY
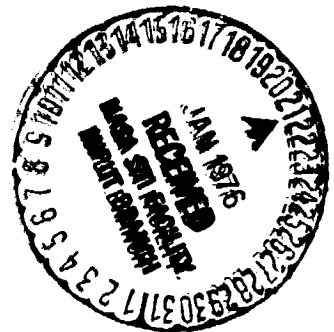
THIN SILICON SOLAR CELL

JPL Contract No. 954290

December, 1975

First Quarterly Report

Report No. SX/105/1Q

by

Joseph Lindmayer, et al

SOLAREX CORPORATION

1335 Piccard Drive

Rockville, Md. 20850

TECHNICAL CONTENT STATEMENT

This report contains information prepared by Solarex Corporation under JPL subcontract. Its content is not necessarily endorsed by the Jet Propulsion Laboratory, California Institute of Technology, or the National Aeronautics and Space Administration.

I. ABSTRACT

Efforts in this first quarter of the contract have been concentrated on altering processing temperatures in experimental processing and studying the relationships among the resulting cell performance parameters. Diffusion temperature variation results in a fairly distinct optimum cell performance for diffusion temperatures in the immediate vicinity of 850°C. Variation of alloy/diffusion temperature for backside p^+-p formation as yet shows no clear trend.

An additional effort was also devoted to redesign of the metallization gridline pattern for both minimum light blockage and minimum fill factor alteration due to series resistance.

Efforts on improvement of tantalum oxide antireflection coatings were begun in the last month.

Fifty 2 cm x 2 cm cells having a range of thicknesses is being submitted to JPL as the first sample group. These cells were processed under conditions tentatively identified during this first contractual quarter's experiments as being optimal for resulting cell performance.

II. TABLE OF CONTENTS

III. SUMMARY

The purpose of this investigation is to improve process
parameters which influence high-efficiency, thin silicon solar
cell performance. In the course of this contractual effort, a
significant number of solar cells nominally 4 cm^2 will be fabri-
cated and analyzed, of which 500 are to be submitted to JPL for
evaluation. This investigation is both experimental and theo-
retical in nature, as feedback to changes in experimental
process parameters requires analysis of cell performance
parameters and comparison to modelled properties for assessment
of probable underlying physical phenomena which can be altered
experimentally.

During this first contractual quarter, the main process
variables investigated were the temperatures for formation of
the front junction and the alloyed bottom-face layer. It has
been tentatively concluded that there is a relatively optimum
temperature range for phosphorus diffusion, centered at 850°C.
At this diffusion temperature, there is a peak in cell performance
for the process presently employed. The data obtained from
measurement of numerous cell electrical parameters is presented
in graphical form, which shows that the performance peaks at a
diffusion temperature of 850°C.

Data on the effect of alloy temperature variation has so
far not shown such a clear trend as did the phosphorus diffusion
temperature experiments, but will be a subject of further experi-
mentation in the coming quarter.

Redesign of the metallization gridline configuration was completed in this quarter, to produce a pattern with considerably reduced linewidth. The minimum gridline size will be 5 microns, which is nearer to the limits of the maskmaking art for a 2 cm x 2 cm cell, (although far from the limits of single-line resolution). This new geometry should be ready for use by the end of December, and be employed in the second contractual quarter on experimental cells.

Investigation of effects resulting from altering tantalum oxide antireflection coating conditions were just begun in the last month of the quarter.

IV. TECHNICAL DISCUSSION

A. General Considerations

The purpose of this investigation is to improve process
parameters which influence high-efficiency, thin silicon solar
cells performance. There is already a large body of background
work in device theory for high efficiency possibility prediction,
but as real devices have approached ever higher efficiencies,
a host of previously neglected interactions become the limiting factors.
Proceeding from the fact that prior experimentation has shown
minor process changes can alter efficiency percentiles, this
investigation is an application of combined experimental and
theoretical approaches to improving performance. This is to be
accomplished by mapping the interaction effects produced by any
one process parameter variation, e.g., simultaneous changes in
spectral response, photovoltage and fill factor caused by changing
diffusion temperatures.

Although a large body of device theory has long been developed,
there is presently no specific data concerning the specific origins
of detrimental effects restraining improvement of already high-
efficiency silicon cells. Although one could theoretically relate
less than optimal "red end" spectral response to bulk recombination
center excesses or too-weak rear carrier-reflecting fields, the
sources of such deviations from ideal are vaguely understood at
best. Quite often, an empirical attempt to improve one performance

parameter by a process variation produces a compensating reduction in another, resulting in no net improvement. This investigation is therefore directed to mapping <u>both</u> the optimum ranges of process steps and the directions of changes produced outside the optimum ranges for measurable cell parameters. In this way, the presently unpredictable physical, chemical and metallurgical interactions can be assessed and controlled for overall optimization of cell performance.

B.   Diffusion Temperature

A series of experiments was carried out to assess the influence that the temperature of phosphorus diffusion has on the performance of high-efficiency silicon solar cells. Over twenty cells were processed at each experimental temperature to assure a sample large enough so that extraneous effects from individual cell faults could be weeded out of the resulting performance characteristics, without reducing confidence in the results.

The silicon surface preparation was standardized to a common hydrofluoric-nitric-acetic acid etch, followed by a water rinse, hydrofluoric acid etch and another rinse to remove any variable residual oxide. The diffusion employed argon carrier gas and phospine as the source of phosphorus. Diffusions were performed isochronally over a temperature range spanning 750°C to 900°C. Upon completion of cell fabrication five parameters were measured* under a Xenon simulator:

$$I_{sc}, I_{sc} \text{ (Blue)}, I_{sc} \text{ (red)}, V_{oc}, \text{ and } P_{max}$$

---

*Without antireflective coating, to avoid possible data scatter from additional variations.

where I_{sc} (Blue) is the current produced with a 3 mm thick Corning Glass #9788 blue filter inserted in the light path and I_{sc} (Red) is the current with a red filter inserted which eliminates the wavelengths passed by the blue filter, in order to provide a two-part spectral response measurement.

The results of the diffusion experiments are shown graphically in Figures 1 and 2. Interestingly, the blue response is first flat and then decreases with rising diffusion temperature as the junction moves deeper into the cell. However, the red response undergoes an increase around 830°C which is not particularly expected, but could be due to an interaction effect such as, for example, increased heavy-metal gettering on the increasingly phosphorus-rich back. If recombination-center densities were reduced at the back side before aluminum application, such an improved red response would result.

The fill factor increases monotonically with diffusion temperature as seen in Figure 2. At the lower temperatures, this increase is to be expected, since the series sheet resistance of the phosphorus-diffused layer becomes less significant as the temperature of iso-chronal diffusion is increased. However, the situation is more complicated, because the diffusion at lower temperatures tends to be by advancement of a solid-solubility layer rather than an error-function or Gaussian limited-source system, which would provide increased lattice strain and attendant increased excess current in the junction forward characteristic.

The monotonic increase in the open-circuit voltage is also expected, since the integral of the phosphorus dopant introduced
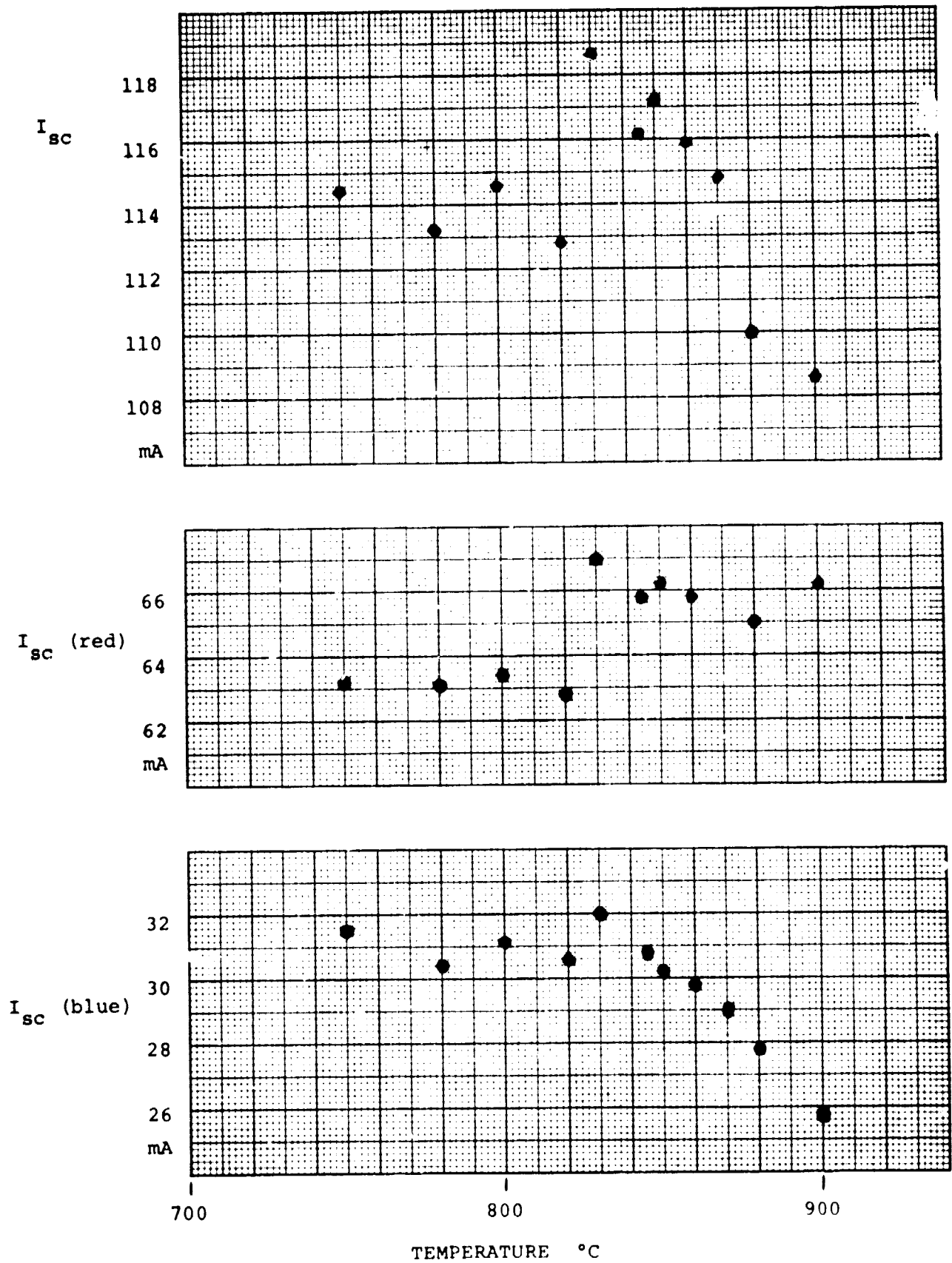
FIGURE 1.   CHANGES IN I_{sc} AND RED & BLUE COMPONENTS WITH
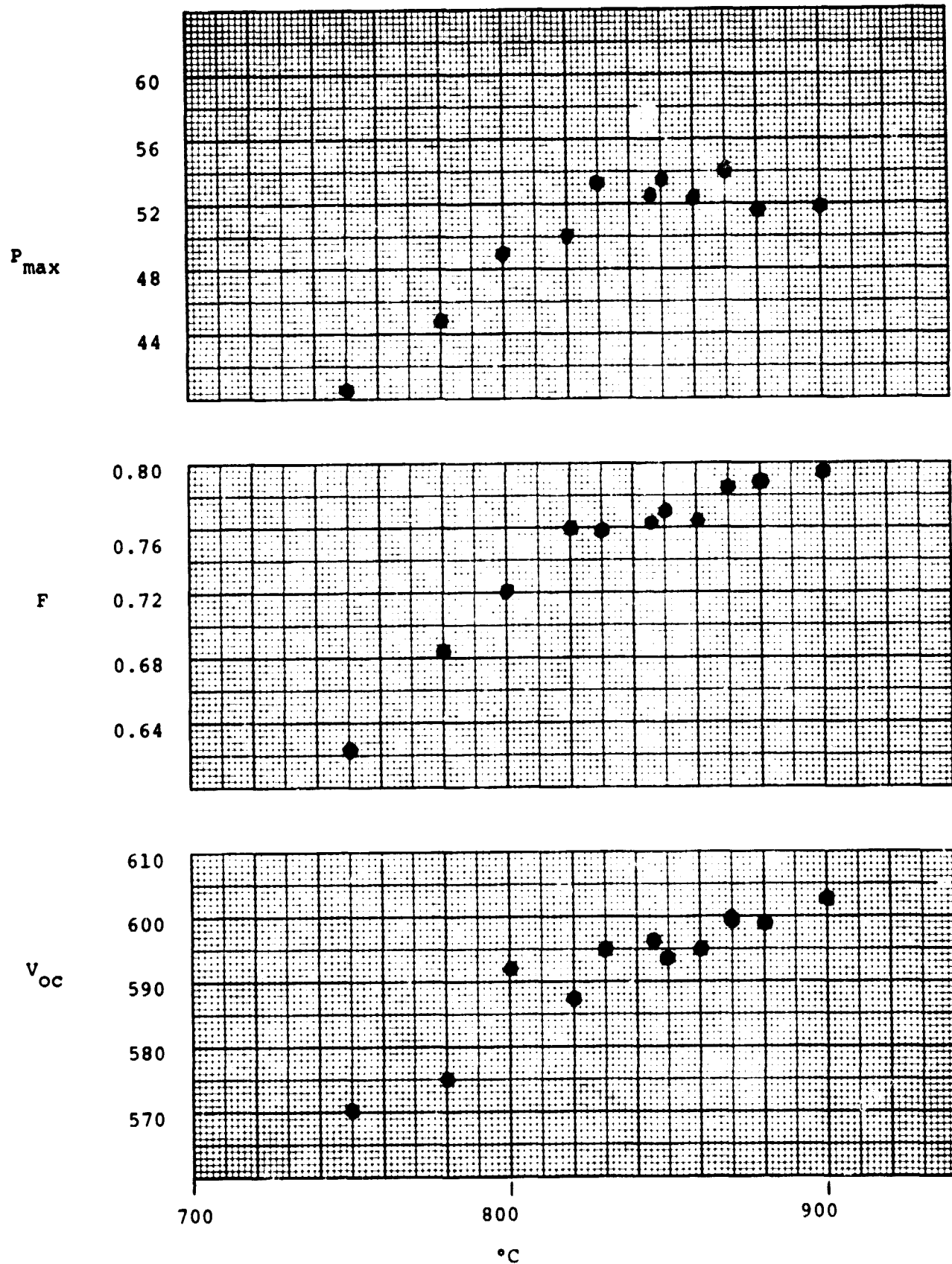PHOSPHORUS DIFFUSION TEMPERATURE.

FIGURE 2. CHANGES IN P_{max}, FILL FACTOR AND V_{oc} WITH PHOSPHORUS DIFFUSION TEMPERATURE.

rises with diffusion temperature and increases the Fermi level
displacement at the junction.

The maximum output power rises with temperature as V_{oc},
F and I_{sc} increase up to the neighborhood of 850°C. Thereafter,
I_{sc} falls due to the fall in blue spectral response, but the
continued increase of V_{oc} and F slow the fall of P_{max}.

All of the diffusion experiments to date employed phosphine
in an argon carrier gas with traces of oxygen. Changes in phos-
phorus source to such materials as phosphorus oxychloride ($POCl_3$)
will be a subject of experimental mapping in the coming months.

C. Alloyed p^+ Bottom-Face Layer

Variations in alloying temperature for cells diffused at
850°C have not as yet shown such clear trends in effects on
device parameters as the diffusion experiments. One difficulty
is in separating the variables controlled. Alloying at temperatures
at or above the temperature just experienced by the cell during
diffusion produces further diffusion of phosphorus. Consequently,
alloying cycles at temperatures above 850°C tend to degrade I_{sc}
(Blue) and P_{max}, which at least shows that improvement of I_{sc} (Red)
is not capable of compensating the other reductions. For temper-
atures below 850°C, the effect of varying alloying temperatures has
produced scattered results which also do not agree with previous
experiments that showed asymptotic improvement toward lower tem-
peratures.

Considerable further effort on alloying experimentation will
be applied in the coming quarters.

D. Gridline Optimization

Ideally, a solar cell should have a front-surface current-collecting grid which has such a fine line structure as to shadow the least possible area, has a finger spacing that only allows negligible series resistance in the phosphorus-diffused layer, and has negligible series resistance in the metal lines themselves. From past experience in both solar cell and integrated circuit processing, and discussions with maskmakers, it was decided that 5 microns (0.0002") would be a reproducible minimum linewidth in the gridline pattern. Narrower lines can be produced, but reproducibility would suffer by the time the line height had been built up for conductance optimization. In addition, finer lines require considerably higher tooling costs, which seem to increase with the inverse of minimum linewidth below 5 microns.

Each of the finest gridlines picks up current from an area extending halfway toward the adjacent gridline, with an average source distance half of that. Therefore, each gridline gets current from both sides from an equivalent line-source distance 1/4 of the gridline spacing. In order not to measurably degrade the fill factor of the cell by the series resistance of the phosphorus-diffused layer, the voltage drop in the n-type layer should not exceed 1/2% of the voltage at P_{max}. The voltage at P_{max} is approximately 470-480 mV for high-efficiency cells with good fill factors, which predicates a series-resistance-induced voltage drop of 2.4 mV at AMO illumunation. The current density

for high-efficiency cells under AM0 illumination is approximately 40 mA/cm^2. For phosphorus diffusion, such as discussed in Part B above, the n-layer sheet resistance is very near 80 ohms per square. The resulting current-source to gridline distance should then be held under 500 microns to satisfy the voltage drop requirement.

Because the majority of the maskmakers contacted work in English units, the individual gridline (Chevron[r] in all Solarex designs) spacing was rounded off to 0.070", which is 10% closer than 4X 500 microns. For symmetry of current flow to two 1x2 mm contacts three sub-busses were used, as in previous designs. The sub-buss linewidth design starts at 5 microns and widens by 5 microns for each grid juncture to avoid voltage drops in the metal film, reaching 55 microns (0.0022") at the contact end. The interconnecting buss between the contact pads was kept at 100 microns, as in previous designs. The resulting surface shadowing, at this design stage, is only 2%. The linewidth growth as the metal layer is thickened to achieve the required conductance will probably result in a final coverage nearer 3%; somewhat a function of deposition technique details. In coming processing efforts, attempts will be made to hold the very small coverage of this new Solarex design.

The lowest bid was received for art work in November and a purchase order was placed for delivery of masks in late December.

E. Antireflective Coating

During the last month of this quarter, efforts commenced on improvement of antireflective coating properties. Mostly, these consisted of greater attention to surface cleaning techniques for

the cells, attention to the condition of the evaporant source
and deposition schedules. The various samples collected will
be measured for reflection and bandwidth (index) effects during
the coming month, and the data will be included in the next report
along with additional experimental results during that period.

F.   Sample Cells

At this time, the first 50 samples of 2cm x 2cm cells processed
during the quarter are being submitted to JPL for evaluation. They
were diffused at 850°C, which is tentatively considered optimum at
this time. The cells have a range of thicknesses, from approximately
140 microns (0.0055") to 500 microns (0.016"). The antireflective
coating is tantalum oxide, applied under the present cleaning and
deposition conditions (solvent cleaning, dilute HF for oxide trace
removal, alcohol rinsing). Figure 3 shows representative AMO I-V
characteristics for a thick and a thin cell from the group of cells
submitted to JPL for evaluation. Figure 4 and Figure 5 are plots
of some sampled values of short-circuit and maximum power output
at AMO. Note the low reduction rates with decreasing thickness,
which indicate good short wavelength performance in the cells
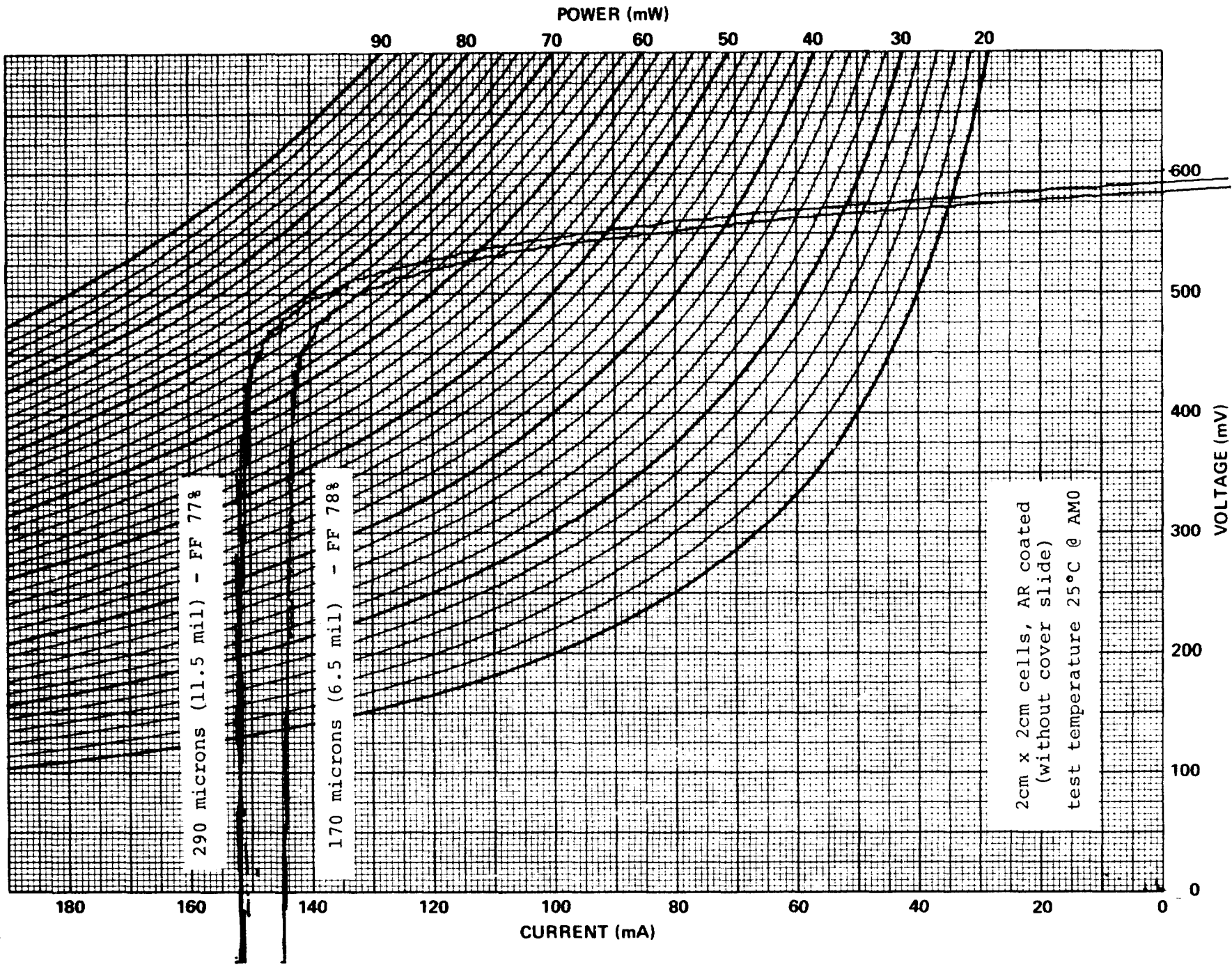being fabricated with the present process.

FIGURE 3.   I-V CHARACTERISTICS MEASURED AT AM0 FOR TWO
THICKNESSES OF SAMPLE CELLS.

-15-

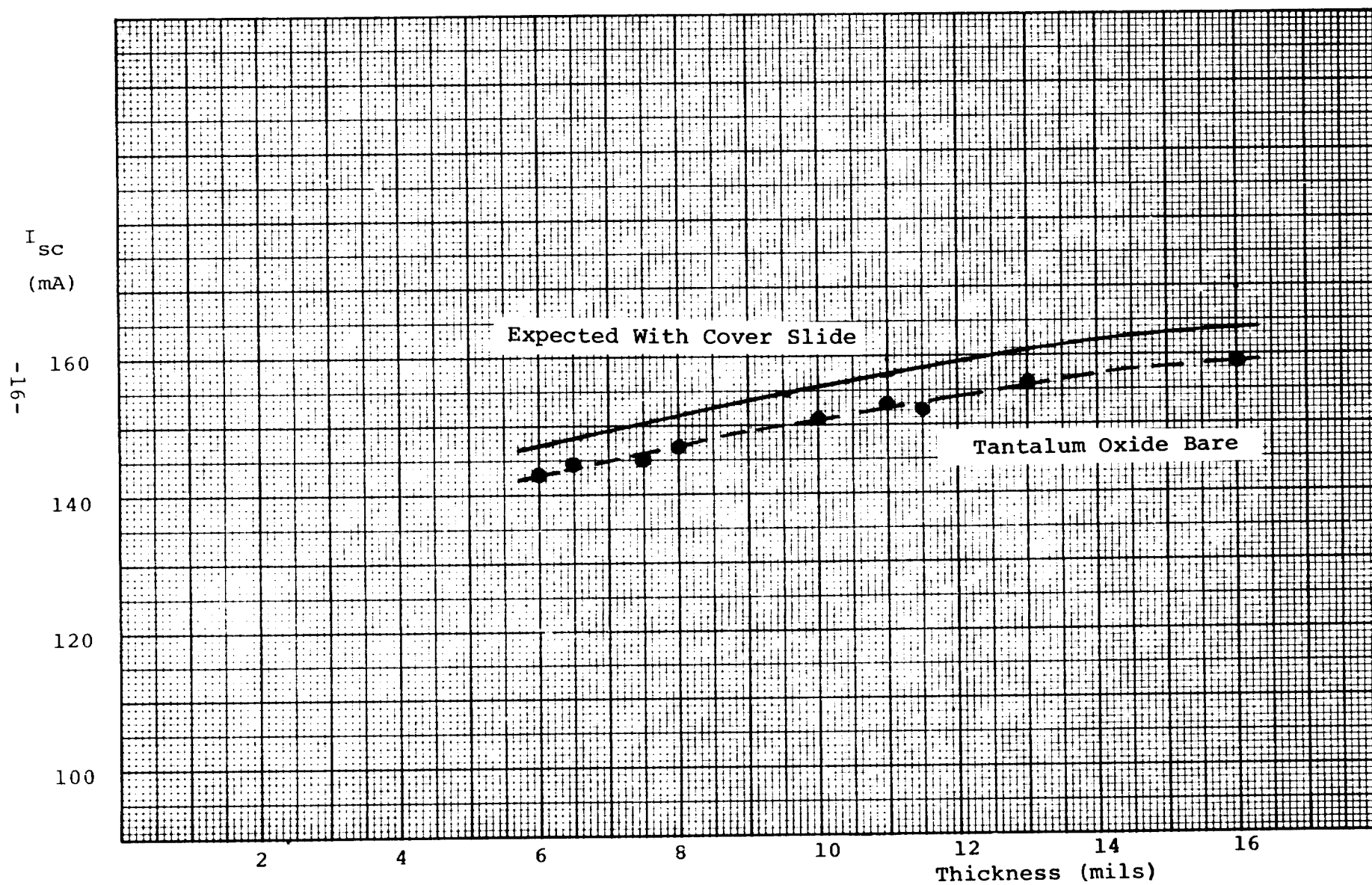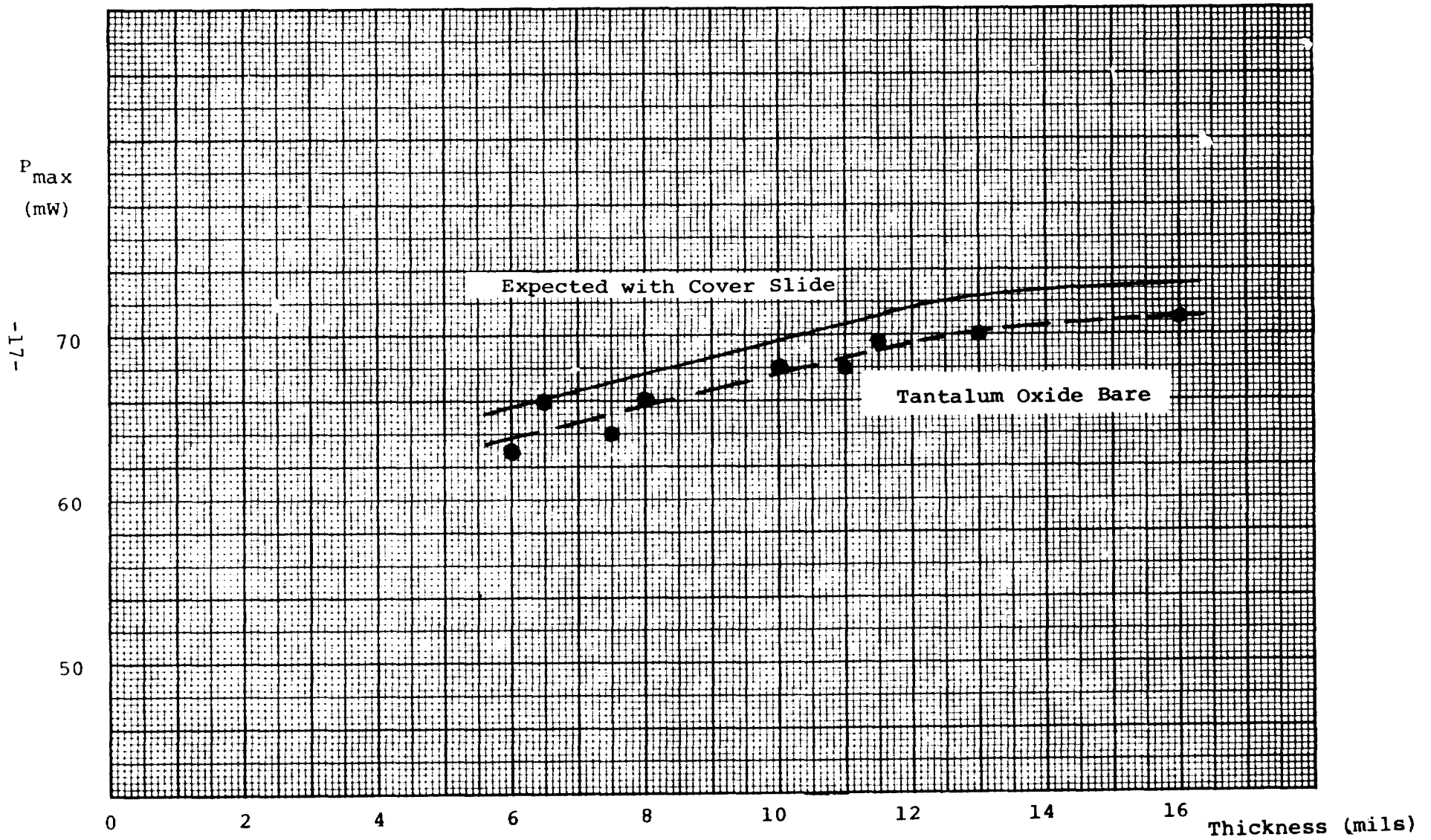FIGURE 4. VARIATION OF I_{sc} WITH THICKNESS FOR SAMPLE CELLS.

FIGURE 5.   VARIATION OF P_{max} WITH THICKNESS FOR SAMPLE CELLS.

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V. CONCLUSIONS

A. The initial efforts on conditions for front junction formation
with phosphine as a dopant source indicate that 850°C could be
tentatively picked as an optimum region. Interactions with
the large number of other variables may well change this con-
clusion as the effort proceeds.

B. At the present state, there is no clear trend to an optimum
temperature range for bottom-face aluminum alloying, except
that it should not exceed the 850°C diffusion temperature
to avoid interaction with the diffusion.

C. A Solarex Chevron[R] metallization pattern has been designed
which, by itself, produces only 2% front surface shadowing.
It will be attempted to hold actual coverage to 3% on
finished cells to be processed in the coming quarter.

D. The 50 sample cells submitted show the good fill factors
and slow fall-off of performance with decreasing cell
thickness representative of the present state of processing.

VI. NEXT QUARTER ACTIVITIES

During the coming quarter, the new gridline configuration will be employed and attempts will be made to achieve minimum shadowing, the effects of alloying temperature will be mapped further, antireflective coating experimentation will be pursued, and stability evaluations will be made in the last month of the quarter. Front-junction formation and p^+ layer formation interaction effects will be under continuous study.

During the coming quarter, efforts will commence on front-surface texturing for improved optical coupling and bottom-face treatments (coupled with alloying studies) to improve internal reflection of usable photons of longer wavelength.

In addition, one hundred (100) evaluation samples will be submitted to JPL during the coming quarter.