NASA CR-144722

TDRSS MULTIMODE TRANSPONDER PROGRAM S-BAND MODIFICATION

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19 DECEMBER 1975

Final Report for Period May 1974 — November 1975

(NASA-CR-144722) TDRSS MULTIMODE TRANSPONDER PROGRAM S-BAND MODIFICATION Final Report, May 1974 - Nov. 1975 (Magnavox Research Labs.) 150 p HC $6.00 CSCL 14B

N76-16164

Unclas
G3/19 09988

Prepared for

GODDARD SPACE FLIGHT CENTER
Greenbelt, Maryland 20771

TECHNICAL REPORT STANDARD TITLE PAGE

1. Report No.	2. Government Accession No.	3. Recipient's Catalog No.
4. Title and Subtitle TDRSS MULTIMODE TRANSPONDER PROGRAM S-BAND MODIFICATION FINAL REPORT		5. Report Date 19 December 1975
		6. Performing Organization Code
7. Author(s) Joseph E. Mackey		8. Performing Organization Report No. R-5188
9. Performing Organization Name and Address The Magnavox Company Magnavox Research Laboratories 2829 Maricopa Street Torrance, California 90503		10. Work Unit No.
		11. Contract or Grant No. NAS5-20330
		13. Type of Report and Period Covered Type III May 1974 to 19 December 1975
12. Sponsoring Agency Name and Address National Aeronautics and Space Administration Goddard Space Flight Center Greenbelt, Maryland 20771		14. Sponsoring Agency Code
15. Supplementary Notes		

16. Abstract

This report contains a complete description of the S-Band TDRS Multimode Transponder and its associated ground support equipment. The transponder will demonstrate candidate modulation techniques to provide the required information for the design of an eventual S-Band transponder suitable for installation in a user satellite, capable of operating as part of a Tracking and Data Relay Satellite (TDRS) system.

17. Key Words	18. Distribution Statement
Modulation Evaluation, S-Band	

19. Security Classif. (of this report)	20. Security Classif. (of this page)	21. No. of Pages	22. Price
Unclassified	Unclassified		

Form DOT F 1700.7 (8-69)

PREFACE

This report dated 19 December 1975 contains a description of the equipment designed and fabricated on a program entitled "TDRSS Multimode Transponder". The results of the Phase I design study effort were previously published in a report designated Magnavox Research Laboratories Report No. R-4403 on 15 July 1973. The equipment which was subsequently developed during Phase II was described in MRL Report No. R-4754 written but not distributed on 15 March 1974. A description of the equipment modified for S-Band operation is presented in this report. This work was accomplished by the Magnavox Research Laboratories of Torrance, California and complies with the requirements of Contract Number NAS5-20330.

This report contains a complete description of the TDRSS Multimode Transponder and its associated ground support equipment. The transponder will demonstrate candidate modulation techniques to provide the required information for the design of an eventual S-Band transponder suitable for installation in a user satellite, capable of operating as part of a Tracking and Data Relay Satellite (TDRS) system.

Magnavox wishes to acknowledge the assistance of Mr. Pat Mitchell, NASA Technical Officer and Mr. Leonard Deerkoski of the TDRSS program office at the Goddard Space Flight Center.

This report was prepared by Messrs. J. Mackey, P. Fisher, S. Zapp and R. Updegraff.

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INTRODUCTION

1.1 PROGRAM BACKGROUND

To provide a virtual real time data acquisition and tracking capability, the TDRS system concept was developed by NASA. This capability would be used by low, medium, and high-data-rate users consisting of manned and unmanned scientific satellites. The TDRS system would provide the data acquisition and tracking capability for those manned and unmanned missions whose orbits were less than 5,000 kilometers.

Currently, unmanned scientific satellites are supported by the STDN (MSFN unified with STADAN) network consisting of ground stations strategically located on the globe. These stations are connected to a communications center, at the Goddard Space Flight Center, through NASCOM facilities. Manned missions are also supported by STDN. A second network, the Deep Space Network (DSN), also services NASA. The DSN is operated by JPL, services deep space exploration missions and can be used as backup for manned missions.

Subsequent to the Initial Phase A study which established important TDRSS concepts, NASA-Goddard contracted several detailed VHF link communications studies. Among these were: (1) the multipath modulation study conducted by Magnavox under Contract NAS5-10744, (2) the multipath modulation study conducted by Hekimian Laboratories under NAS5-10749, and (3) the VHF communication study for low-data-rate users conducted by Hughes Aircraft under Contract NAS5-11602. As a result, two prime candidate systems evolved. Pseudonoise modulation was recommended by Magnavox and Hughes while adaptive burst communications (ABC) were recommended by Hekimian. Hughes considered a narrowband forward link with a wideband return link, while the Magnavox considered a narrowband PN forward link and options of either wideband or narrowband PN return links.

NASA issued to industry an RFP, dated May 1971, for a configuration and trade-off study of the TDRS system. Subsequently, two contractors, North American Rockwell and Hughes Aircraft, were awarded system trade-off studies. Next, NASA issued an RFP for a multimode transponder to be used on board a low-date-rate, unmanned, scientific satellite. Shortly afterward this RFP was amended to permit the design of a multimode transponder for installation and use on board an aircraft simulating a user spacecraft as part of a TDRS system. On March 1, 1972, a contract (NAS5-20330) for the design and development of a multimode transponder was awarded to Magnavox Research Laboratories.

In June 1972, MRL presented to NASA the results of the Phase I portion of the Multimode Transponder development program. It included the system analysis used to identify hardware parameters, identified all known technical problems associated with hardware implementation and provided a complete multimode transponder design.

In September 1973, acceptance testing of the Multimode Transponder and its associated test equipment was successfully completed. The VHF/UHF antenna developed under Phase II of the contract was shipped to NASA-Goddard Space Flight Center. The Multimode Transponder equipment was placed in bonded stores at Magnavox pending completion of TDRSS test plans.

In October 1973, preliminary meetings were held to discuss modification of the Multimode Transponder to convert to S-Band RF frequencies and to interface with an Adaptive Ground Implemented Phased Array system for system integration testing at the Applied Physics Laboratory of Johns Hopkins University.

In May 1974, Magnavox began the redesign and modification of the Multimode Transponder equipment to S-Band frequencies under amendments to Contract NAS5-20330. This report describes the completed equipment as modified for laboratory simulation of the TDRS system.

In September 1975, the S-Band Multimode Transponder equipment was delivered to the Applied Physics Laboratory of Johns Hopkins University for acceptance testing and interface with an Adaptive Ground Implemented Phased Array (AGIPA) system. The TDRSS laboratory simulation testing is in progress at this writing.

1.2 BASIC TDRSS CONCEPTS

The Tracking and Data Relay Satellite (TDRS) system concept considers use of two relay satellites. One TDRSS satellite is located at 14 degrees west, the other at 144 degrees west resulting in a total separation of 130 degrees. The two TDRSS satellites are active repeaters (amplifiers). The forward link is defined as the link from the ground station to TDRSS to user spacecraft, the return link is from user to TDRSS to ground station. Forward user-TDRSS links and return user-TDRSS links are S-band frequencies on. TDRSS-ground station links are in the Ku band.

Unmanned scientific satellites are required to dump accumulated data upon command as they pass over designed ground stations. Scientific data is accumulated on board by means of tape records and is transmitted to the appropriate ground station at greater than real-time speed. The TDRS system will circumvent the need for on-board recorders by providing essentially real-time data transfer and tracking commands for user spacecraft.

In addition to providing forward and return link data transfer, the TDRS system must provide real-time tracking of range and range-rate measurements of the spacecraft users. This can be accomplished through the use of one or two TDRS systems. Simultaneous tracking of a user with both TDRS system is accomplished when the user is in the field of view of both TDRS systems.

Regardless of tracking techniques used, the range and Doppler tracking uncertainty requirements below have been applied in the TDRSS configuration.

Systematic Range Errors

Less than 100 meters

Random Range Errors

Less than 15 meters

Doppler Uncertainties

Systematic 10 centimeters per second

Random Range Rate Errors

Ten centimeters per second for a Doppler observation interval of one second or one centimeter per second for a Doppler observation of 10 seconds.

1.3 PROGRAM OBJECTIVES — S-BAND MODIFICATION

The purpose of this effort was to provide NASA with a design and an engineering model of an S-Band Multimode Transponder and its associated ground support equipment. The transponder will demonstrate the modulation techniques specified herein. The Multimode Transponder will provide the required information for the design of an S-Band transponder suitable for installation on a low altitude (5000 km or less) earth orbiting satellite, capable of operating as part of a Tracking and Data Relay Satellite (TDRS) system consisting of one or more geosynchronous satellites together with the associated ground equipment.

The transponder shall be designed, to the extent possible, to minimize weight, power consumption and cost. Reliability, shock and vibration specification shall be consistent with standard commercial specifications. The transponder shall be designed to meet all the electrical performance requirements of a space flight model, but not the packaging, reliability and space qualifications of a space flight model.

The Multimode Transponder (MMT) along with the associated ground support equipment (MTAR) will be designed to demonstrate the following modulation techniques:

FORWARD LINK

- SQPN — STAGGERED QUADRIPHASE PN MODULATION
- FREQUENCY HOP PREAMBLE FOR ACQUISITION
- 2^{18} CHIP PN CODE LENGTH

RETURN LINK

- SQPN — STAGGERED QUADRIPHASE PN MODULATION
- 2^{18} CHIP PN CODE — TRANSPOND MODE
- 2^{15} CHIP PN CODE — RETURN ONLY MODE
- ASYNCHRONOUS DATA MODE
- DUAL DATA MODE
- CONVOLUTIONAL ENCODING AND DECODING

SYSTEM

- S-BAND TRANSMIT AND RECEIVE
- AGIPA INTERFACE
- DOPPLER CORRECTION
- RANGE CORRECTION

The following functions will be simulated with various combinations of the transponder subunits and associated ground equipment:

a. Reception, demodulation, and delivery to the user spacecraft of command signals received by the transponder via the forward link.

b. Acceptance, modulation, and transmission via the return link of the telemetry data generated by the spacecraft user.

c. Reception via forward link, processing on board, and retransmission via return link of coded signals suitable for ranging and range-rate determination.

1.4 REPORT CONTENT

Section I of this report contains the historical background for the TDRSS Multimode Transponder program and briefly outlines the objectives and tasks associated with the program.

Section II presents the TDRSS Multimode Transponder equipment configuration. It summarizes the modes of operation and provides a basic functional description of the equipment and provides the rationale for some of the design features.

Section III contains a detailed functional description of the TDRSS Multimode Transponder design which consists of two major groupings of equipment; namely, the Multimode Transponder equipment (MMT) and Multimode Transponder and Receiver equipment (MTAR).

Section IV provides a detailed mechanical description of all major assemblies. Equipment capability with respect to environment and interface are discussed and size, weight and power specifications are included.

Section V presents the resulting equipment characteristics and performance. The equipment specification has been updated to include all contract modifications. A copy of the acceptance test data is included.

Section VI includes the conclusions and recommendations for future application.

SECTION II
SYSTEM DESCRIPTION

System concepts for the TDRSS Multimode Transponder equipment are described in this section. The terminal equipment configurations are shown, the various modes of operation are summarized, and a basic functional description i presented to provide insight to the system concepts which are presented in the latter portions of this report. This section also describes the operational procedures for the equipment and provides a rationale for many of the design features.

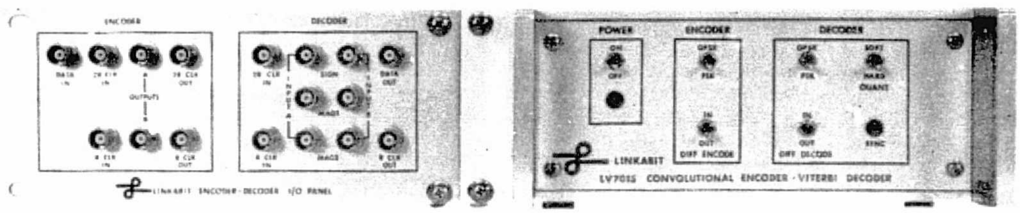
2.1 EQUIPMENT CONFIGURATION

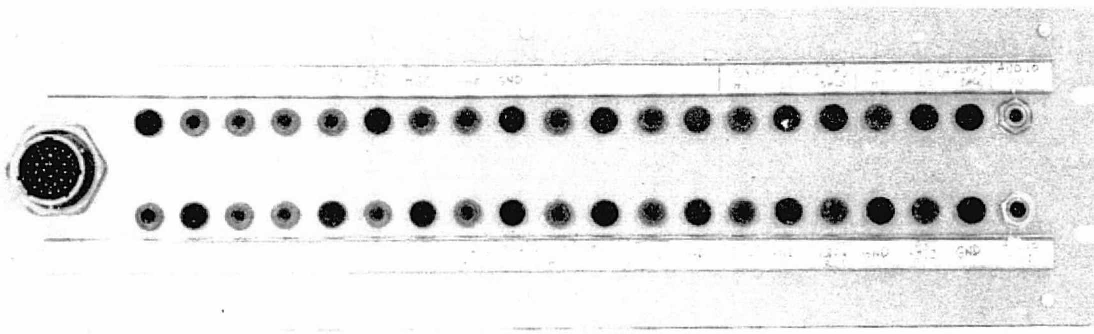
2.1.1 MTAR EQUIPMENT

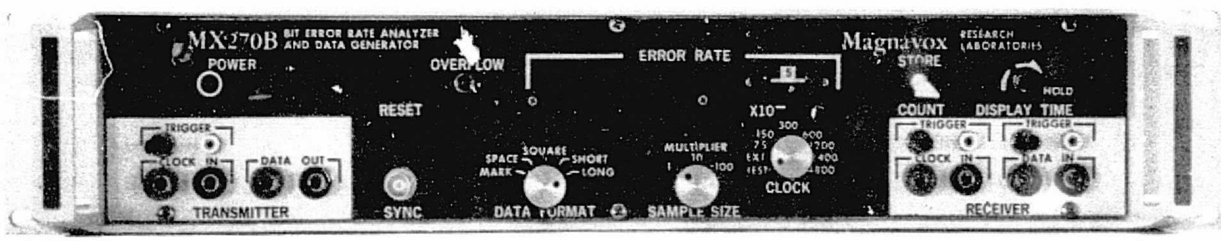
The complement of equipment which comprises the Multimode Transmitter and Receiver (MTAR) equipment is depicted in figure 2-1. This equipment performs the functions of transmit and receive equipment for an eventual TDRSS ground station. The MTAR equipment group consists of seven major chassis: (1) Control-Display Panel, (2) Signal Processor, (3) Receiver-Transmitter, (4) Power Supply, (5) MX 270B Bit Error Rate Analyzer, (6) Signal Monitor Panel and (7) LV7015 Convolutional Encoder-Viterbi Decoder.

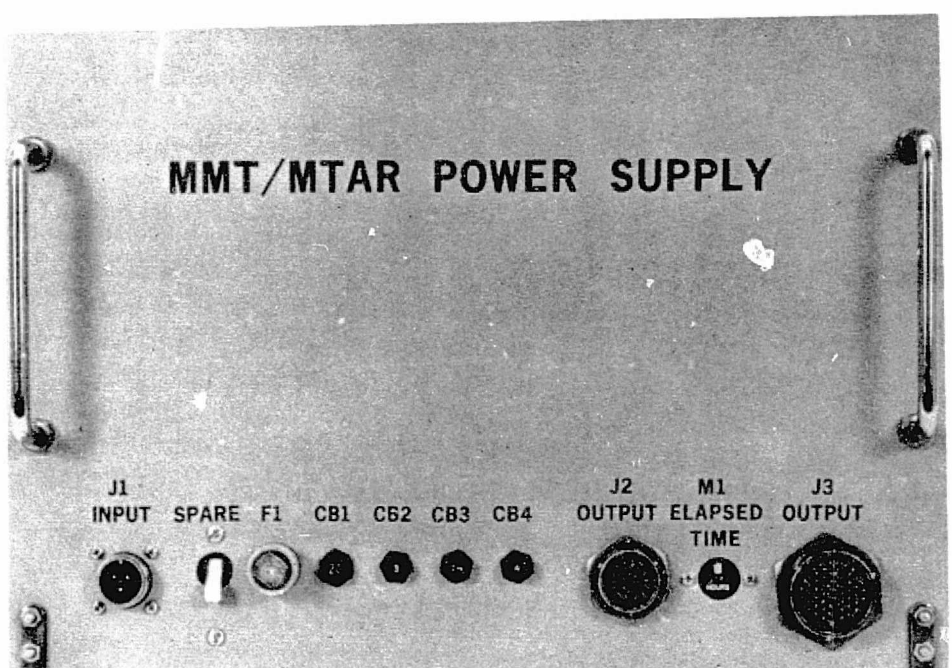
2.1.2 MMT EQUIPMENT

Figure 2-2 reveals the configuration of the Multimode Transponder (MMT) equipment. This group of equipment simulates the functions of a transponder which will be part of an eventual TDRSS user transponder satellite. This equipment group consists of six major assemblies: (1) Power Supply, (2) Receiver-Transmitter, (3) Signal Processor, (4) Control-Display Panel, (5) MX 270B Bit Error Rate Analyzer and (6) Signal Monitor Panel.









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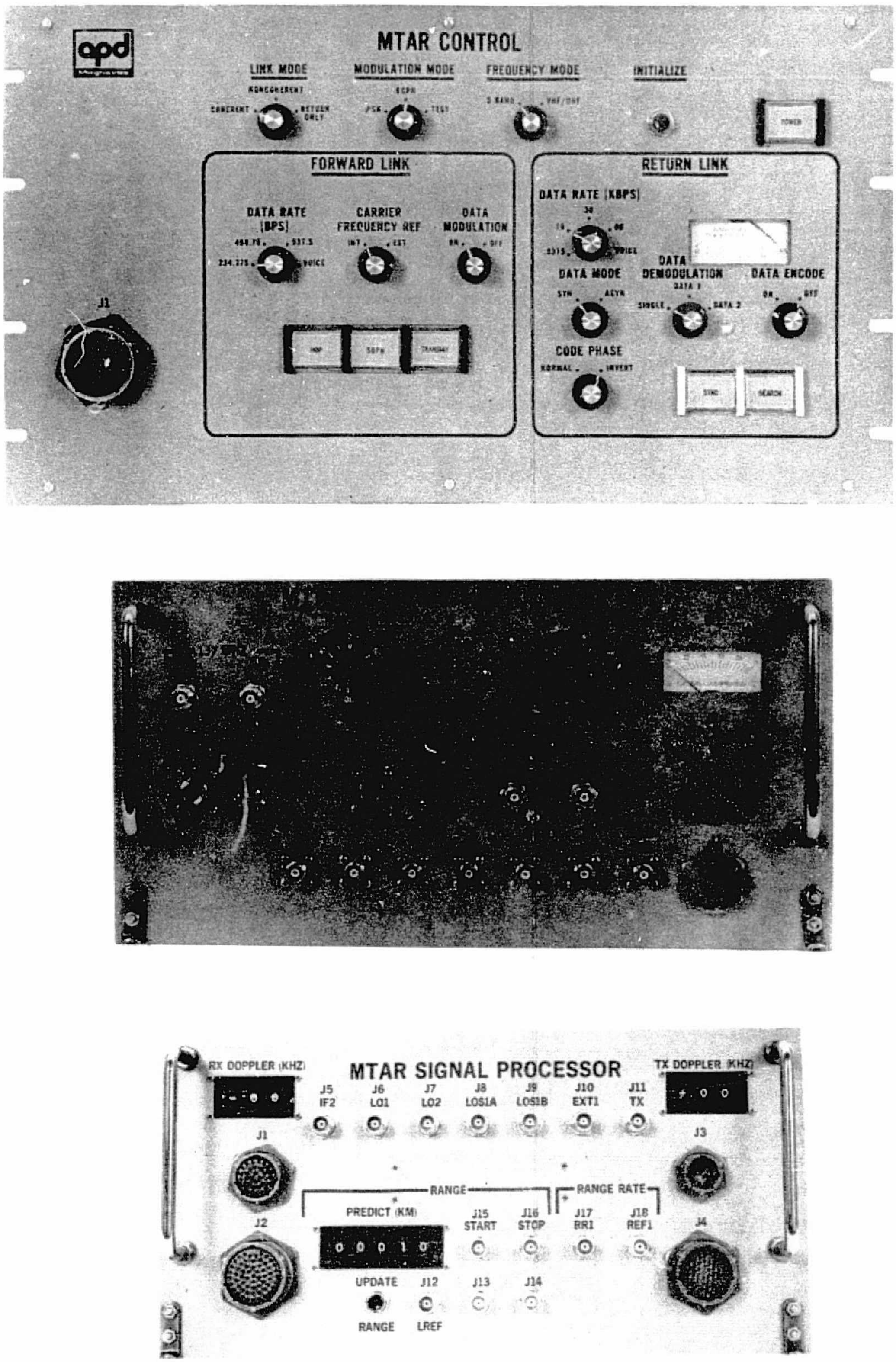
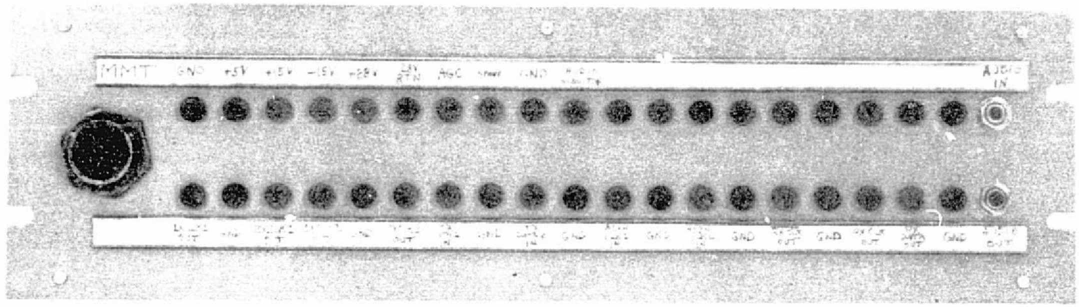
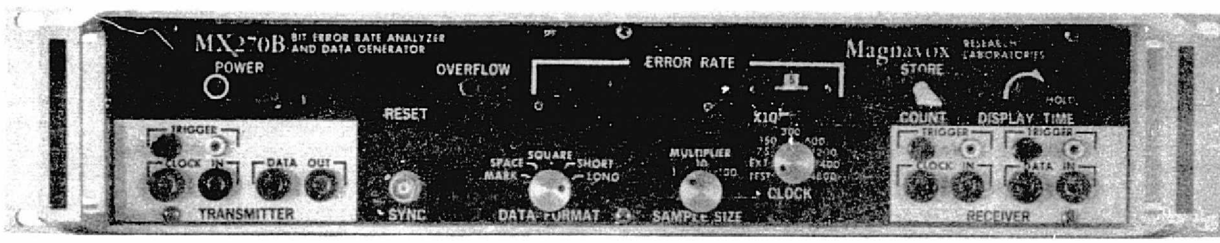
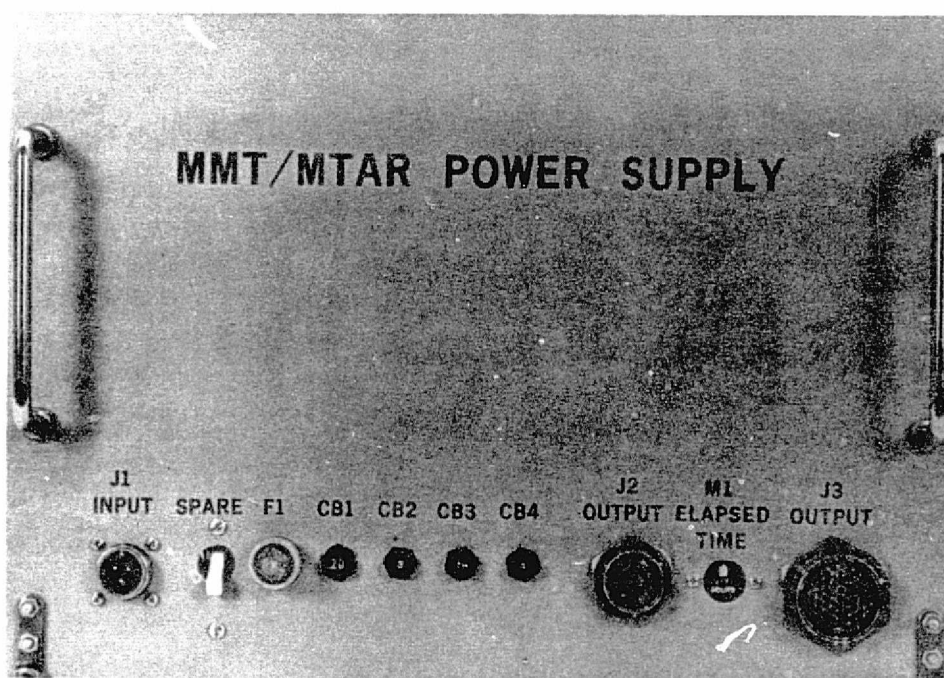


Figure 2-1. Multimode Transmitter and Receiver (MTAR) Equipment







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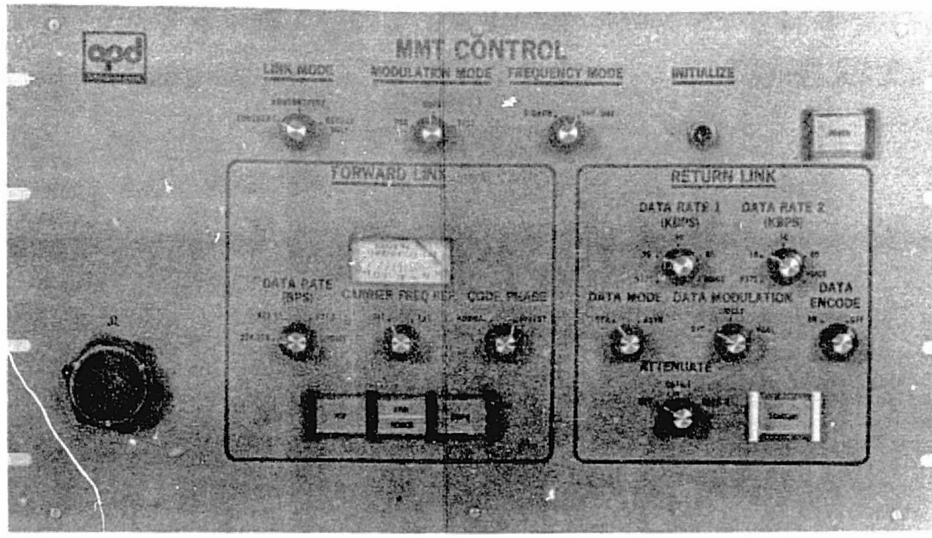

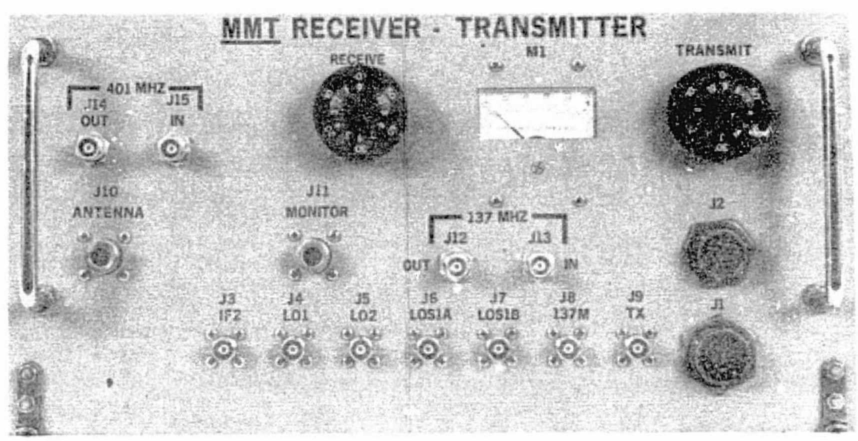

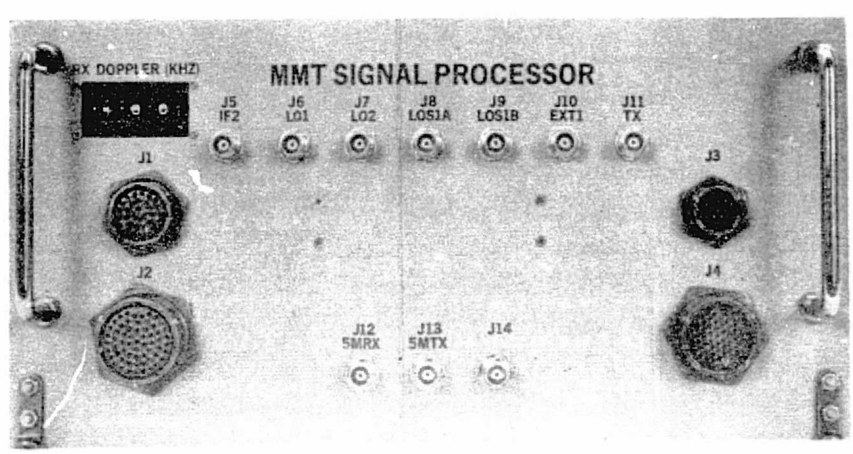

Figure 2-2. Multimode Transponder (MMT) Equipment

2.1.3 SYSTEM TEST INTERFACE

The MMT and MTAR equipments are designed to be used in a laboratory simulation of the TDRS system. The MMT represents the functions that could be implemented in a multiple access user transponder operating at S-Band. The MTAR represents compatible ground station transmit and receive functions. Figure 2-3 depicts the MMT and MTAR relationships for TDRSS simulation.

The setup for TDRSS simulation tests at Applied Physics Laboratory is shown in figure 2-4. The diplexer shown is part of the MMT equipment. The antenna shown connected to the MMT diplexer is part of the laboratory equipment. Although not shown, the MTAR equipment includes a diplexer and S-Band circuitry for MMT/MTAR back-to-back testing. The MMT and MTAR equipments use the MX 270B to generate and analyze digital data for measurement of link performance in terms of bit error rates.

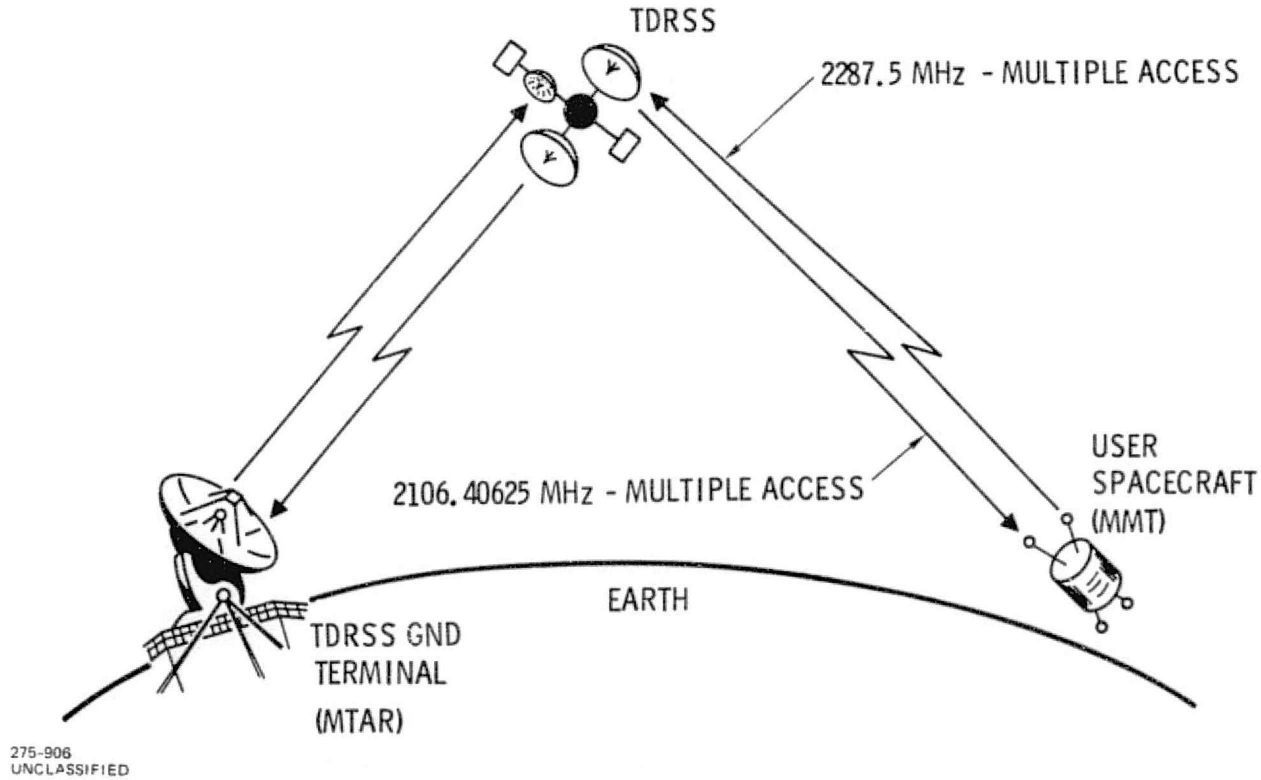

Figure 2-3. TDRSS Configuration

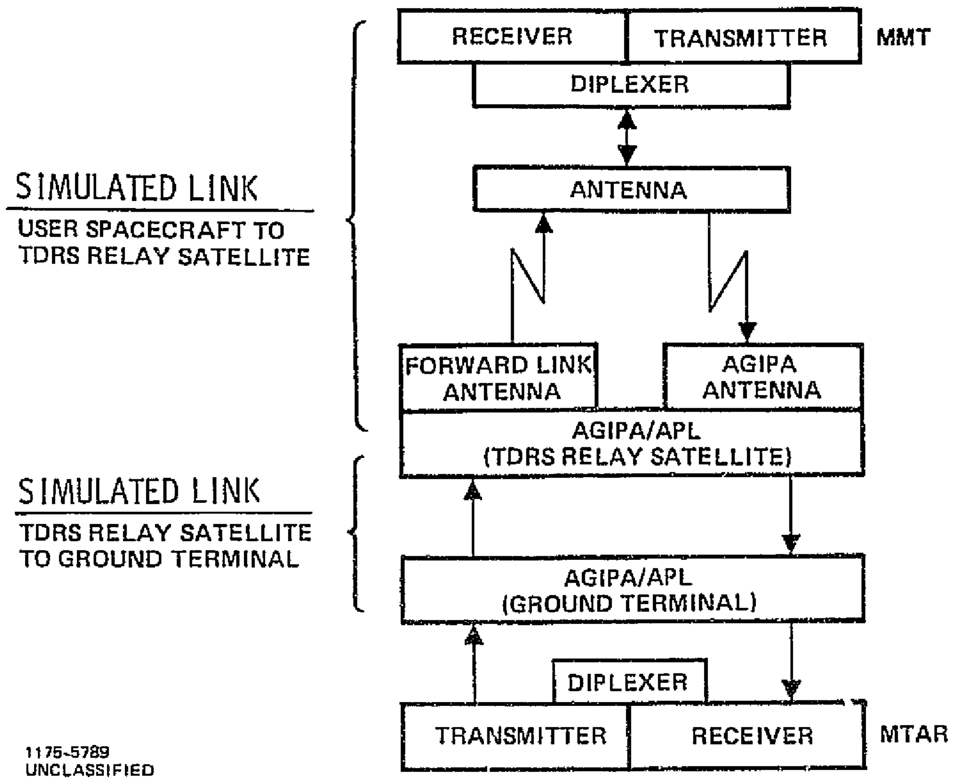

Figure 2-4. TDRSS Simulation

2.2 SYSTEM OPERATION

The MMT/MTAR operational parameters were designed to provide NASA with flexible laboratory equipment for TDRSS simulation testing. The operational modes and selectable data rates represent an S-Band multiple access user. The code and data rates are a compromise resulting from the economical implementation of the S-Band modification of the earlier VHF/UHF equipment.

2.2.1 CONTROL FUNCTIONS

The selectable modes of operation include modulation mode, link mode, data rates and data modes on the return link. The forward link is the transmission from the MTAR to the MMT. The return link is the transmission from the MMT to the MTAR. The carrier frequencies for the forward and return links are shown in figure 2-5. The MMT and MTAR may be operated directly back-to-back using the S-Band diplexer shown on the MTAR.

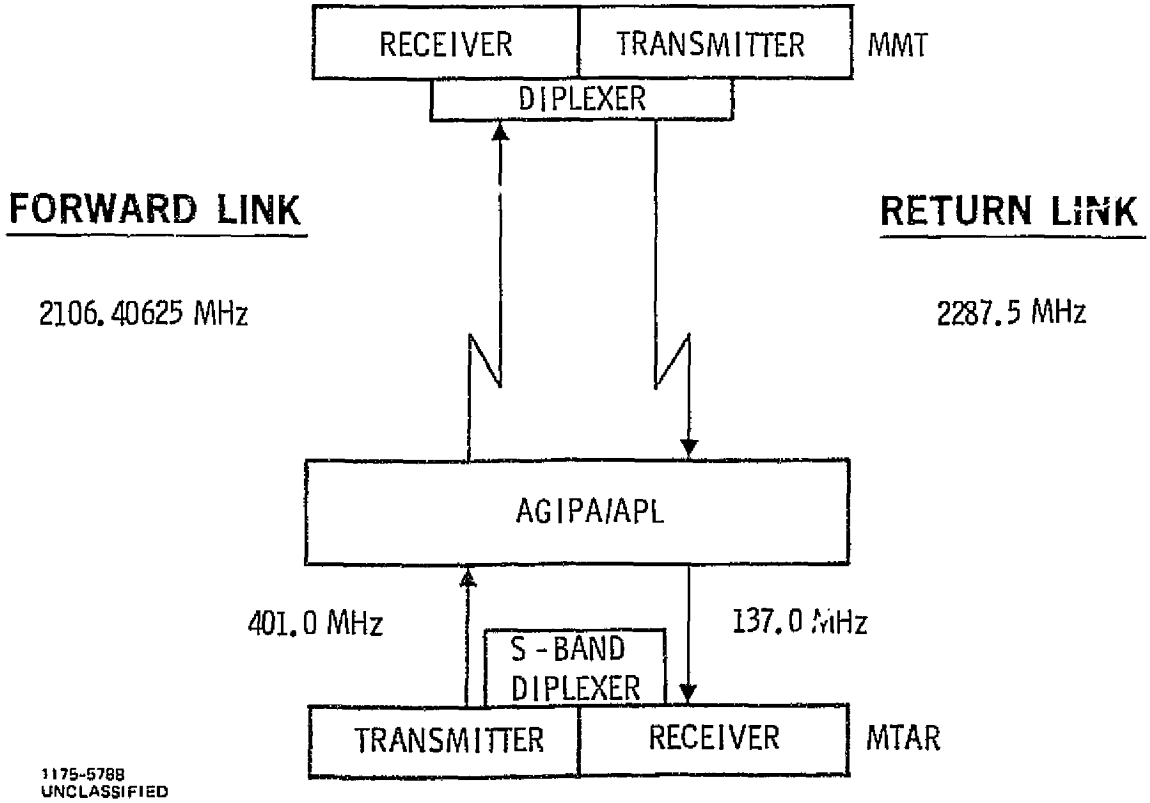

Figure 2-5. Frequencies Plan

The control panel selectable modulation modes are PSK, SQPN and TEST. The PSK mode is phase shift keying where the digital data is biphase modulated on the RF carrier.

In staggered quadriphase pseudonoise (SQPN) modulation mode a frequency hop preamble is used in the forward link for signal acquisition. The equipment automatically switches from frequency hop to SQPN. The SQPN mode does not employ an acquisition preamble on the return link. The TEST mode holds the forward link in frequency hop mode for testing purposes.

The control panel selectable link modes are coherent transpond, noncoherent transpond and return only. In coherent transpond the MMT does a coherent carrier and code turnaround of the MTAR signal. Range and range rate measurements can be made in coherent transpond mode. Noncoherent transpond mode uses separate carrier and code oscillators for the return link. The established return link is preserved when the forward link is dropped to go service another user. The return only mode enables the MMT to establish the return link without the necessity of acquiring the forward link each time. The return only mode makes use of a code short enough for the MTAR receiver to search the entire length of the code. Since the forward link (in SQPN) always uses the frequency hop preamble for signal acquisition, the link mode selection really determines the characteristics of the return link.

The forward and return link data rates and data modes are shown in figure 2-6. The forward link modulates a single data stream which is synchronous with the SQPN code. The return link can modulate single or dual data simultaneously with capability to demodulate only one data stream in the MTAR receiver. The data can be either synchronous or asynchronous with the SQPN code. Convolutional encoding can be applied to the return link data for evaluation of the bit error rate improvement with encoding.

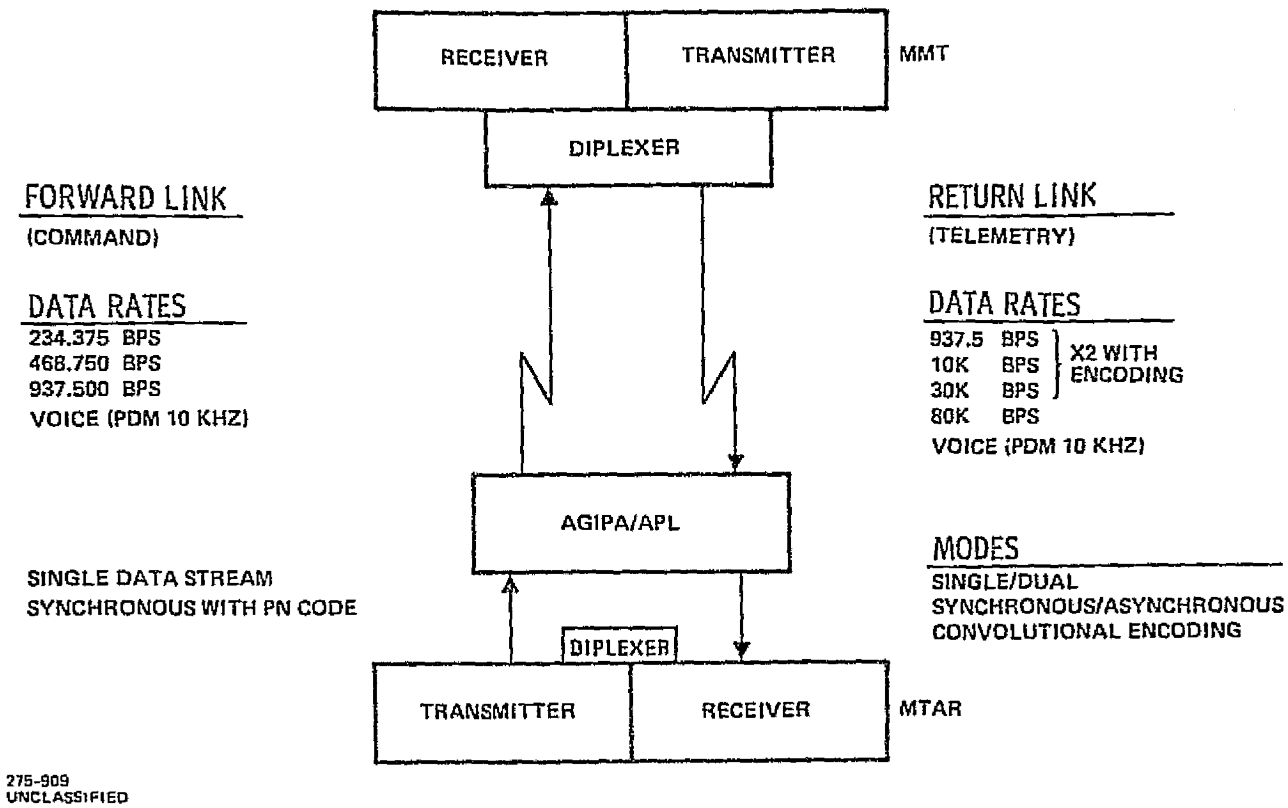

Figure 2-6. Data Rates and Modes

2.2.2 OPERATIONAL PROCEDURES

The MMT and MTAR equipments were designed for laboratory simulation of TDRSS operation. With the MMT simulating a user spacecraft each control panel switch setting represents the command status sent via the forward link. The MTAR control panel settings would be selected by station personnel in a TDRSS ground terminal. Both range and range rate corrections are applied at the ground terminal to simplify the spacecraft hardware.

The MMT and MTAR controls were designed for the following operational scenario.

2.2.2.1 Forward Link

The acquisition sequence on a forward link of the multiple access service is as follows:

a. Ground station directs a transmit beam from TDRSS to user.

b. Inserts user address which selects preamble hopping code and the subsequent PN code to be transmitted.

c. Inserts a priori range rate information (doppler estimates plus estimate of satellite VCO offset due to long term drift).

d. Transmit FH preamble for 16 seconds and switches to PN mode.

e. Meanwhile, satellite receiver, upon acquiring FH signal, switches to PN mode and begins a PN search, acquires and subsequently establishes a PN track mode.

f. Ground station transmits command data.

2.2.2.2 Return Link

The acquisition sequence on a return link of a multiple access service is as follows:

a. Perform forward link acquisition.

b. User receives a command message: (1) If command message does not request a return link response, no return mode occurs. (A return link may already be established.) (2) If the command message requests a coherent transpond mode, all transmit frequencies are synthesized from the receiver VCO. (3) If the command message requests a noncoherent transpond mode, all transmit frequencies are synthesized from a fixed frequency reference oscillator.

c. In coherent transpond mode, the return link transmit PN coder is synchronized to the receiver PN code and, if applicable, the return link antenna is pointed and a PN transmission begins.

d. AGIPA is supplied with pointing information for initial acquisition. Meanwhile, the ground receiver gets a range and range rate estimate and begins a PN search.

e. When PN acquisition is accomplished, a two way range and range rate measurement is made in a coherent transpond mode.

f. After return link acquisition is completed, a command word is sent to the user to begin a telemetry data dump.

g. If the return link is to be retained when the forward link is dropped to go service another user, then a command message is sent to put the user spacecraft in noncoherent transpond mode.

2.2.2.3 Return Only Link

After forward link acquisition, the user spacecraft can be commanded to the return only mode in which the return link transmission is initiated by the user.

a. Perform forward link acquisition.

b. User receives command message for return only mode.

c. Ground terminal receiver is switched to return only mode. The receiver uses a short PN code sequence and searches the entire code length.

d. Return link transmission and data dump is controlled by user.

e. Ground receiver searches until PN signal is acquired and demodulates data.

f. When the user ends a transmission, the ground receiver goes back to a continuous search mode.

2.3 BASIC FUNCTIONAL DESCRIPTION

The Multimode Transponder (MMT) and Multimode Transmitter and Receiver (MTAR) equipments are designed to form a two-way digital communications link for laboratory simulation of the TDRS system. The back-to-back equipment configuration is shown in figure 2-7. The forward link is defined as the transmission from the MTAR transmitter to the MMT receiver. The return link is defined as the transmission from the MMT transmitter to the MTAR receiver. In addition to the S-Band links shown two of the original VHF/UHF frequencies were preserved for interface to the TDRSS laboratory equipment.

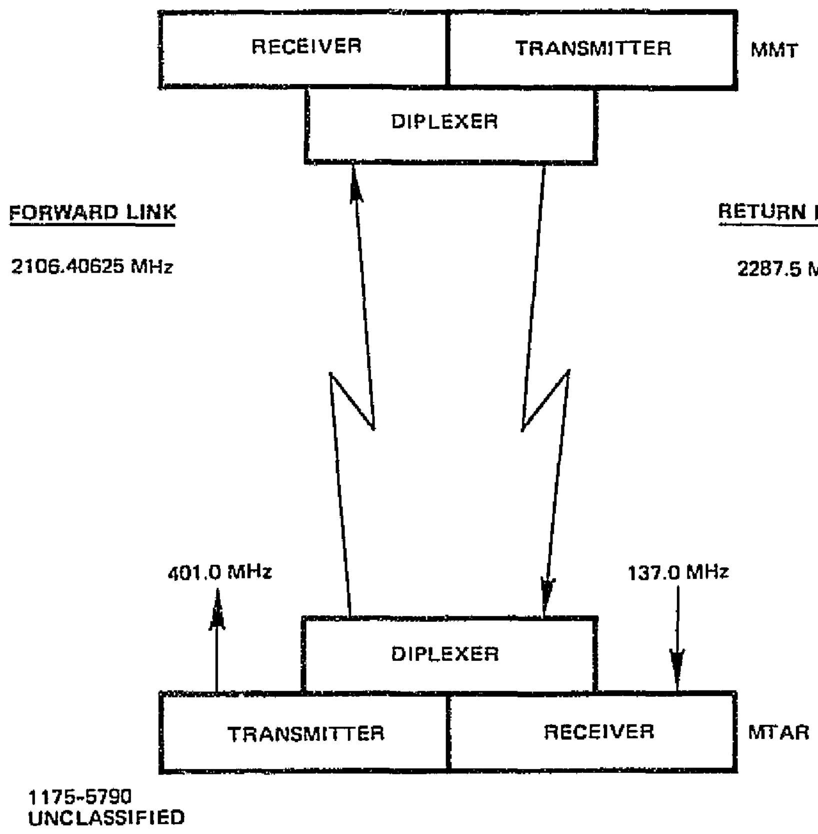

Figure 2-7. Two-Way Digital Communications Link for Laboratory Simulation

2.3.1 MTAR FUNCTIONAL DESCRIPTION

The MTAR simplified block diagram is shown in figure 2-8. A digital data stream representing forward link command data is modulated on an RF carrier synthesized from either an internal oscillator or an external frequency reference. The transmit signal can be used directly at 401 MHz or converted to S-Band (2106.40625 MHz). The receiver demodulates the return link data stream which represents telemetry data from a user spacecraft. The receiver can demodulate either the S-Band signal (2287.5 MHz) or a 137 MHz signal.

In the MTAR, five receive local oscillator signals and three transmit LO signals are syntheiszed. The transmit and receive IF chains are shown in figure 2-9. The receive LO's are synthesized from the carrier track VCO in the receiver.

2.3.2 MMT FUNCTIONAL DESCRIPTION

The MMT simplified block diagram is shown in figure 2-10. The command data is demodulated from the received forward link signal. The forward link S-Band signal is centered at 2106.40625 MHz. The transmit RF carrier frequency of 2287.5 MHz

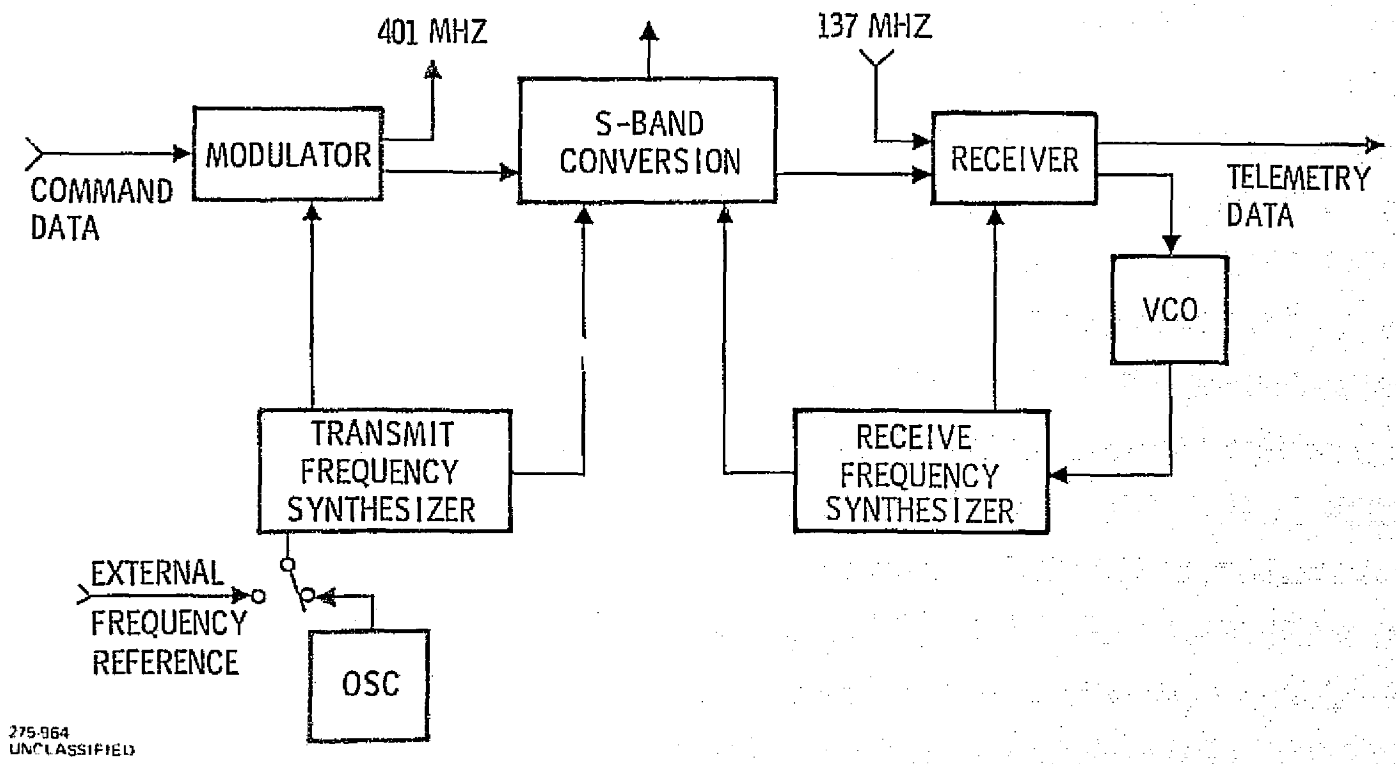

Figure 2-8. MTAR Simplified Block Diagram

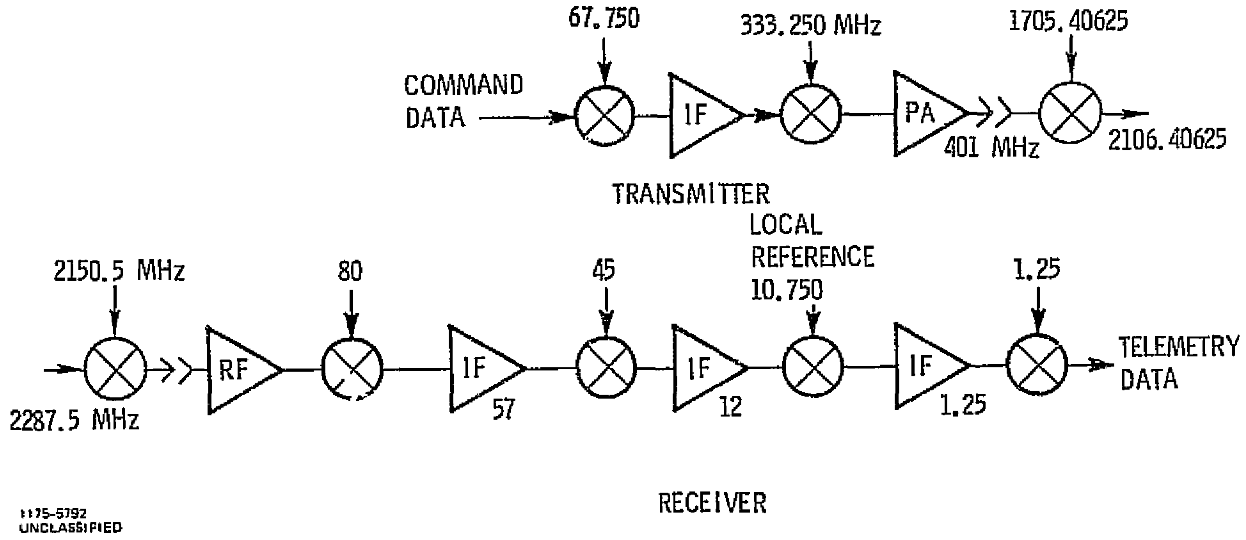

Figure 2-9. MTAR Transmit and Receive IF Chains

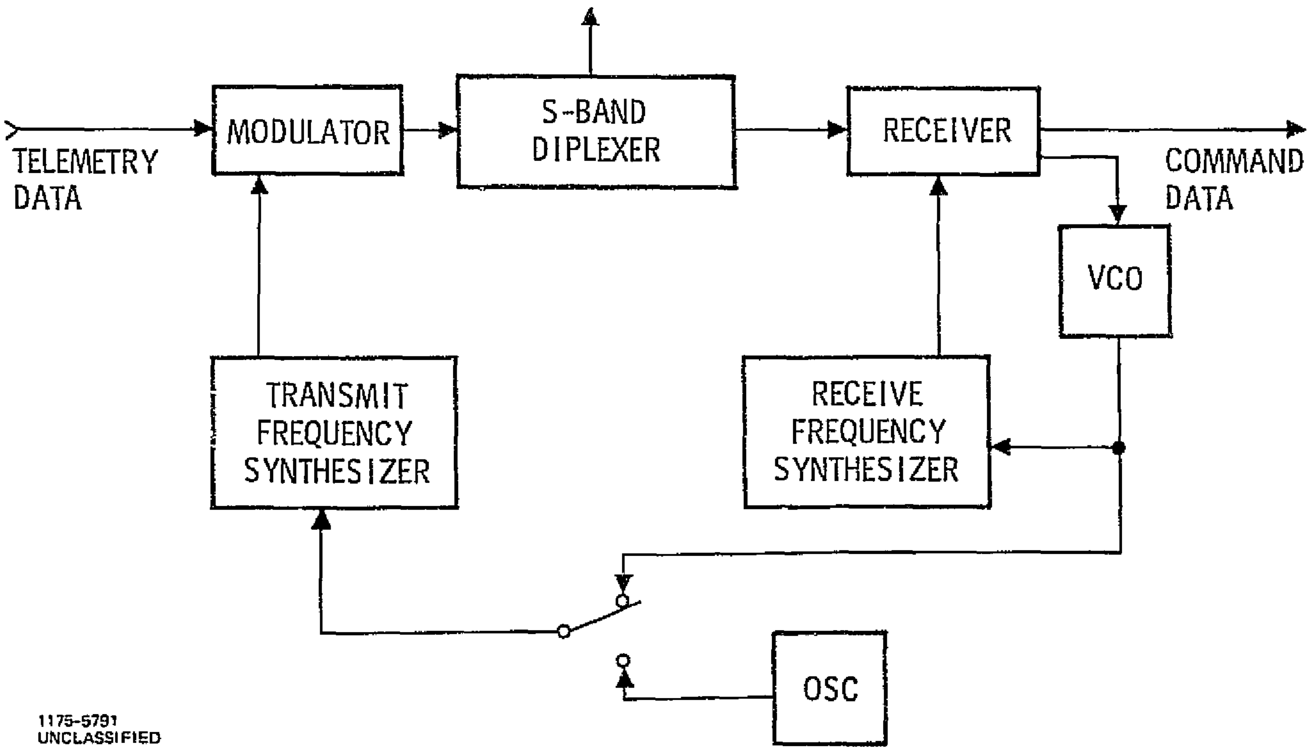

Figure 2-10. MMT Simplified Block Diagram

is synthesized from either the receiver VCO or an internal oscillator. Digital data representing telemetry data is modulated on the return link carrier.

In the MMT five receiver local oscillator signals and two transmit LO signals are synthesized. The transmit and receive IF chains are shown in figure 2-11.

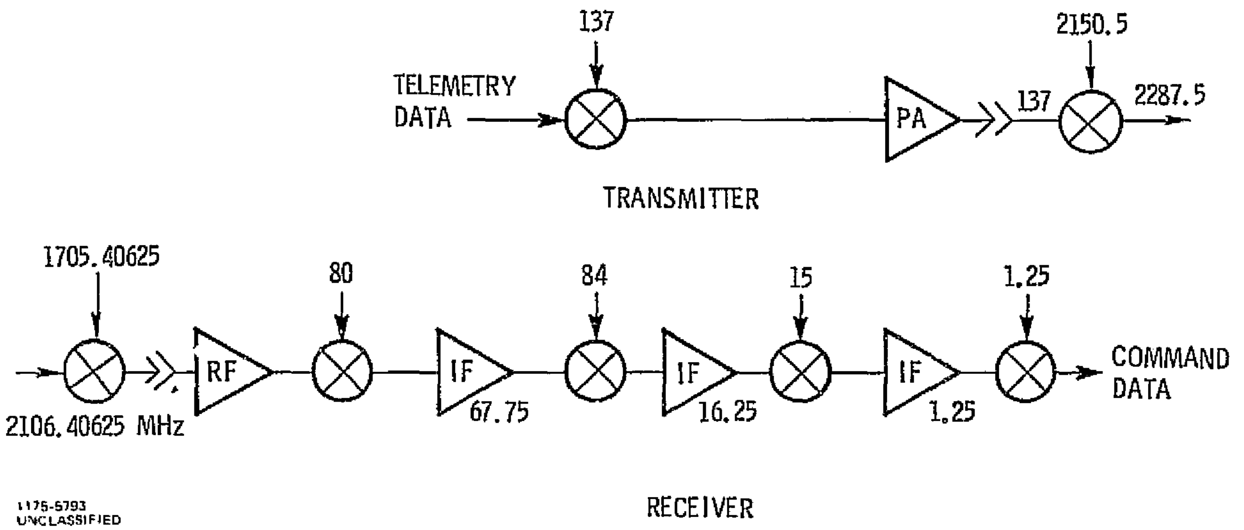

Figure 2-11. MMT Transmit and Receive IF Chains

2.4 SYSTEM DESIGN

Rationale for the TDRSS Multimode Transponder System design is presented in this section. The concepts for the pertinent implementation techniques are described and many of the important operational sequences are summarized in the following discussions.

2.4.1 DESIGN PARAMETERS

The design parameters used for the modification of the MMT/MTAR equipments to simulate the TDRS system are listed below.

FORWARD LINK — WAVEFORM PARAMETERS

PREAMBLE:

TYPE	PSEUDORANDOM FREQUENCY HOP
CODE GENERATION	PRIMITIVE ROOT
CODE PERIOD	256 HOPS
HOP RATE	2.5 kHz
SPACING	10.0 kHz
REPETITION INTERVAL	102.4 MS

PN MODULATION:

TYPE	SQPN - STAGGERED QUADRIPHASE PSEUDONOISE
CODE FAMILY	MAXIMAL CODE PAIRS AUGMENTED BY ONE CHIP
CODE PERIOD	2^{18} CODE CHIPS
PN CHIP RATE	2.56 MHz
REPETITION INTERVAL	102.4 MS

PSK MODULATION:

TYPE	PSK - BIPHASE PHASE SHIFT KEYING

FORWARD LINK — RF SIGNAL PARAMETERS

TRANSMIT	OUTPUT FROM MTAR
FREQUENCY	401 MHZ (WITH DOPPLER COMPENSATION)
SIGNAL LEVEL	-4 dBm
BANDWIDTH	5 MHz
RECEIVE	INPUT TO MMT
FREQUENCY	2106.40625 MHz
FREQUENCY UNCERTAINTY	700 Hz NOMINAL, 3000 Hz MAXIMUM
NOISE FIGURE	5.0 dB MAX
MAXIMUM SIGNAL PLUS NOISE	-100 dBm
MINIMUM SIGNAL	-136 dBm

FORWARD LINK — DIGITAL DATA PARAMETERS

COMMAND DATA:

MODULATION	SYNCHRONOUS BIPHASE DIFFERENTIAL, NRZ-M
RATES (CONTROL PANEL SWITCH SELECT)	234.375 BPS
	468.75 BPS
	937.5 BPS
	10K PDM VOICE
WORD LENGTH	MX 270 FOR TESTING
EXTERNAL INTERFACE	TTL COMPATIBLE

DATA CLOCK:

TX CLOCK	SYNCHRONOUS, MTAR SUPPLIED
RX CLOCK	SYNCHRONOUS, MMT SUPPLIED
EXTERNAL INTERFACE	TTL COMPATIBLE

RETURN LINK — WAVEFORM PARAMETERS

PN MODULATION:

TYPE	SQPN - STAGGERED QUADRIPHASE PSEUDONOISE
CODE FAMILY	MAXIMAL CODE PAIRS AUGMENTED BY ONE CHIP
CODE PERIOD	2^{18} CHIPS - TRANSPOND MODE
	2^{15} CHIPS - RETURN ONLY MODE
PN CHIP RATE	2.56 MHz
REPETITION INTERVAL	102.4 MS - TRANSPOND MODE
	12.8 MS - RETURN ONLY MODE

PSK MODULATION:

TYPE	PSK - BIPHASE PHASE SHIFT KEYING

RETURN LINK — RF SIGNAL PARAMETERS

TRANSMIT	OUTPUT FROM MMT
FREQUENCY	2287.5 MHz
SIGNAL LEVEL	-25 dBm
RECEIVE	INPUT TO MTAR
FREQUENCY	137 MHz (WITH DOPPLER COMPENSATION)
FREQUENCY UNCERTAINTY	700 Hz NOMINAL, 3000 Hz MAXIMUM
SIGNAL LEVEL	-100 dBm
BANDWIDTH	5 MHz

RETURN LINK — DIGITAL DATA PARAMETERS

TELEMETRY DATA:

MODULATION	SYNCHRONOUS OR ASYNCHRONOUS BIPHASE DIFFERENTIAL, NRZ-M
SINGLE DATA INPUT	BIPHASE DATA MODULO-TWO ADDED TO BOTH CODES OF THE MAXIMAL PAIR
DUAL DATA INPUT	EACH OF TWO DATA STREAMS MODULO-TWO ADDED TO INDIVIDUAL CODES. SELECT ONE DATA STREAM FOR DEMODULATION AT THE MTAR

RATES (CONTROL PANEL SWITCH SELECT)	937.5 BPS, 10K BPS, 30K BPS, 80K BPS — Without Encoding; 1875 BPS, 20K BPS, 60K BPS — With Encoding
	10K PDM VOICE
WORD LENGTH	MX 270 FOR TESTING
EXTERNAL INTERFACE	TTL COMPATIBLE
DATA ENCODING:	
TYPE	CONVOLUTIONAL, NONSYSTEMATIC, TRANSPARENT
CONSTRAINT LENGTH	7
CODE RATE	1/2
DATA DECODING:	
TYPE	EXTERNAL USING LINKABIT CORP. MODEL LV7015 VITERBI DECODER
INTERFACE	3 BIT QUANTIZATION (FOR SOFT DECISION DECODING)
DATA CLOCK:	
TX CLOCK	SYNCHRONOUS, MMT SUPPLIED ASYCHRONOUS, USER SUPPLIED
RX CLOCK	SYNCHRONOUS OR ASYCHRONOUS, MTAR SUPPLIED
EXTERNAL INTERFACE	TTL COMPATIBLE

<u>AGIPA INTERFACE</u>

TRANSMIT (FORWARD LINK)	OUTPUT FROM MTAR
FREQUENCY	401 MHz
SIGNAL LEVEL	-4 dBm
BANDWIDTH	5 MHz
IMPEDANCE	50 OHMS
CONNECTOR	SMA

RECEIVE (RETURN LINK)	INPUT TO MTAR
FREQUENCY	137 MHz
SIGNAL LEVEL	-100 dBm
BANDWIDTH	5 MHz
IMPEDANCE	50 OHMS
CONNECTOR	SMA
LOCAL REFERENCE	OUTPUT FROM MTAR
FREQUENCY	10.75 MHz
SIGNAL LEVEL	-10 dBm
BANDWIDTH	5 MHz
IMPEDANCE	50 OHMS
CONNECTOR	SMA
FREQUENCY REFERENCE	INPUT TO MTAR
FREQUENCY	5 MHz
SIGNAL LEVEL	0 dBm
IMPEDANCE	50 OHMS
CONNECTOR	SMA
IN SYNC (DATA ON)	OUTPUT FROM MTAR
SIGNAL LEVEL	TTL (LOW = SYNC) SN75110 DRIVING TWISTED PAIR
DIGITAL DATA CLOCK	OUTPUT FROM MTAR TTL - SN75110 DRIVING TWISTED PAIR

2.4.2 MODULATION TECHNIQUES

The MMT/MTAR equipments use three types of modulation for the forward and return link communications signals. The PSK mode is conventional biphase phase shift keying. The SQPN is staggered quadriphase pseudonoise. The frequency hop preamble used for forward link acquisition is a distinct modulation type even though its only function is to aid the SQPN link acquisition.

2.4.2.1 Frequency Hop

Frequency hop modulation is used to shorten the time required to establish an SQPN forward link. Assuming there is no prior real-time code relationship the entire 2^{18} chip or 102.4 ms time uncertainty must be resolved. At a search rate of 50 chips per second it could take 87 minutes to search the entire 2^{18} chip code length. Use of the frequency hop preamble reduces the forward link acquisition time to 15 seconds.

2.4.2.1.1 Frequency Hop Acquisition

The frequency hop preamble shortens acquisition time by dividing the PN code sequence into 256 discrete time slots. The PN code sequence is synchronized to the hop sequence as shown in figure 2-12. For example, frequency hop period number one is coincident with the first 1024 chips of the PN code sequence.

Hop search occurs at the same rate as PN code search. When the frequency hop mode resolves the transmit-receive time uncertainty to within one hop frequency slot, the maximum PN code uncertainty is reduced from 262,144 chips to less than 1024 chips. This is done in the time it would take to search 256 PN code chips. After the transmitter switches from hop mode to PN mode, the receiver searches out the remaining time uncertainty.

Since PN synchronization requires full coincidence, the switch to PN from a condition of 25 percent hop coincidence would require the PN search to move the receive code 300 microseconds (3/4 hop) later in time. At a search rate of 50 chips per second, this would take over 30 seconds for two search passes. After hop coincidence is declared the MMT enables a hop track loop for 5 seconds before switching to PN. The hop track reduces the time difference to less than 20 microseconds. The PN search of ± 64 chips takes approximately 5 seconds for two passes. Thus the hop track implementation results in a net acquisition time improvement of up to 20 seconds.

2.4.2.1.2 Frequency Hop Signal

The frequency hop signal consists of a timed pseudorandom sequence of carrier frequencies. The frequency spacing is 10 kHz with 128 frequencies above the nominal carrier frequency and 128 frequencies lower than the nominal carrier frequency.

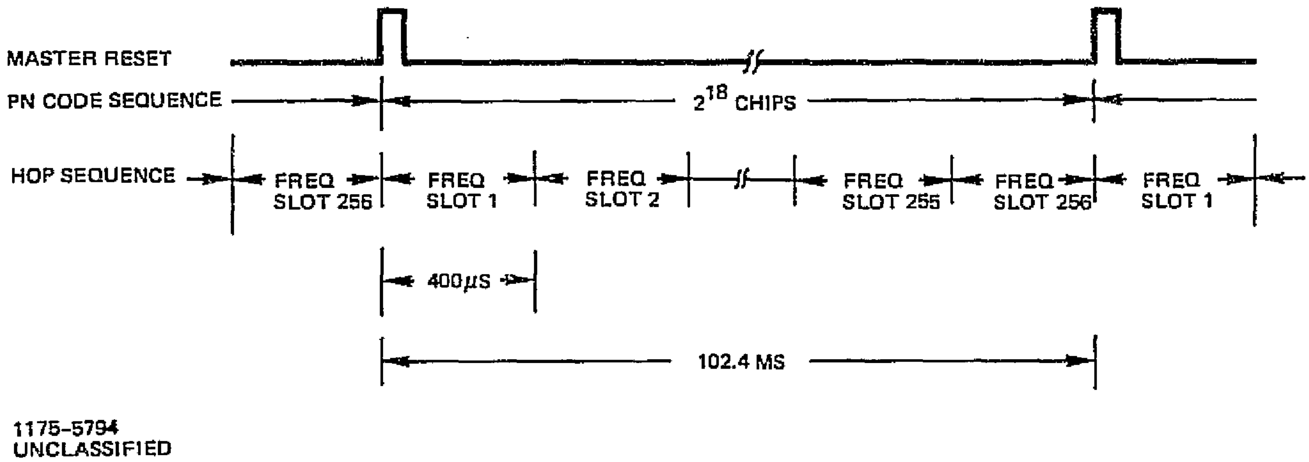

Figure 2-12. Hop and PN Code Timing

Each frequency is held for 400 microseconds so that the 256 step sequence is repeated every 102.4 milliseconds.

In the MMT/MTAR implementation it was found that with a minimal addition of hardware the time uncertainty for the PN search to resolve could be reduced from 300 microseconds to approximately 20 microseconds. The hop search is in 1/4 hop period steps. With a strong signal input the sequential detector can declare hop sync and stop search with only 1/4 hop period coincidence as shown in figure 2-13. In figure 2-13 assume that the receive loop sequence was searched to the point shown by moving from left to right 1/4 hop at a time.

The carrier frequency offsets are accomplished by using a digitally controlled vector addition to rotate the phase of the modulator output. The rate of vector rotation determines the offset from the nominal carrier frequency. By using two balance modulators with an inphase and a quadrature carrier eight different output carrier phases can be obtained. Figure 2-14 shows the sequence of carrier vector rotation.

The I and Q are quadrature carriers whose amplitudes are either 1 or 0 and whose phases are either 0° or 180°, depending on the desired phase shift of I + Q. To phase modulate the output carrier by 360°, we simply carry out the addition steps 1 to 8 as indicated. For -360° modulation, we reverse the order of steps (i.e., 8 to 1). In any case, the stepping rate determines the amount of frequency offset from an unmodulated carrier. Because I and Q are constant-amplitude sinusoids, I + Q will have a 3-dB amplitude variation but this is removed by putting the output through a limiter.

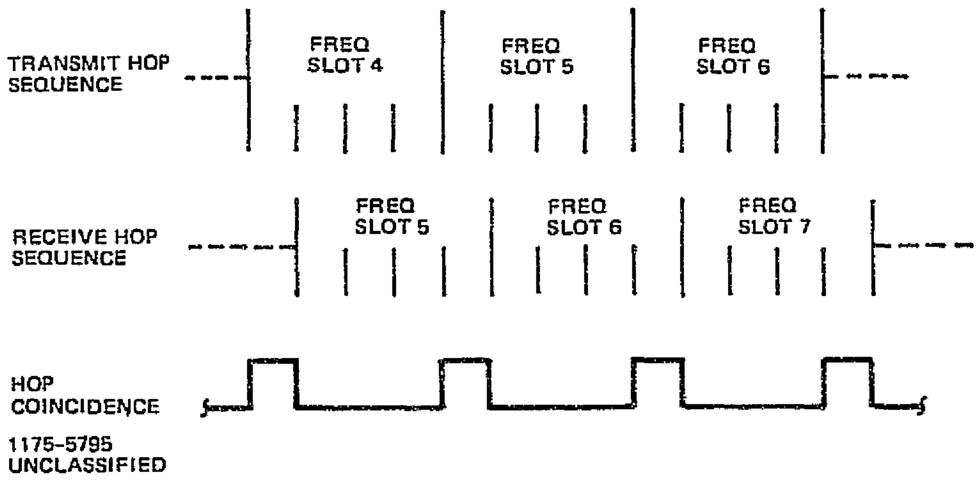

Figure 2-13. Strong Signal Hop Coincidence

STEPS	1	2	3	4	5	6	7	8	1
I	→	→	·	←	←	←	·	→	→
Q	·	↑	↑	↑	·	↓	↓	↓	·
I + Q	→	↗	↑	↖	←	↙	↓	↘	→

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Figure 2-14. Carrier Phase Rotation

The implementation to carry out the vector addition of I and Q is shown in figure 2-15. The balance modulators generate the two phases, 0° and 180°, of the quadrature carriers which are gated to the I and Q summation in accordance with the vector diagram. In frequency hop mode, C1, C2, G1 and G2 are logical functions of a 3-bit U/D counter's content which represents the eight vector steps. The eight steps are clocked in sequence with the signals to the modulator gated in the following manner:

$$C1 = \begin{cases} 1 & \text{for steps 1, 2, 8} \\ 0 & \text{otherwise} \end{cases}$$

$$C2 = \begin{cases} 1 & \text{for steps 2, 3, 4} \\ 0 & \text{otherwise} \end{cases}$$

$$G1 = \begin{cases} 1 & \text{(open switch) for steps 3, 7} \\ 0 & \text{(close switch) otherwise} \end{cases}$$

$$G2 = \begin{cases} 1 & \text{(open switch) for steps 1, 5} \\ 0 & \text{(close switch) otherwise} \end{cases}$$

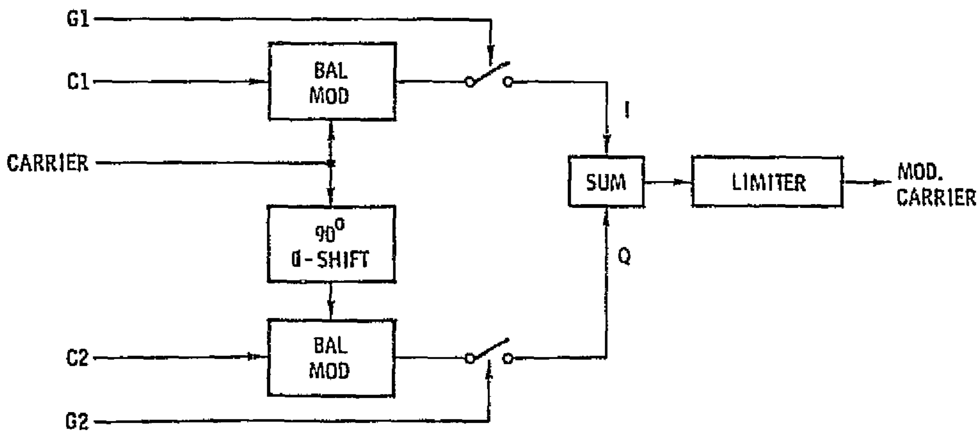

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Figure 2-15. Modulator for FH and SQPN

The sequence of offset frequencies or rates of vector rotation are stored in a 256-word programmable memory. The hop sequence code was generated by the primitive root technique. The technique is based on the existence of a primitive root g such that the sequence g^i forms N distinct numbers modulo p. The sequence has a period N = p-1. The frequency hop code for the MMT/MTAR uses the prime number 257 to generate a 256-word sequence using the primitive root 27. The sequence is listed below with a few of the carrier offset frequencies.

Frequency Slot Number	Carrier Offset Frequency
1	+ 10 kHz
2	+ 270 kHz
3	- 870 kHz
4	- 230 kHz
5	- 940 kHz
6	+ 830 kHz
.	.
.	.
.	.
.	.
255	+1040 kHz
256	-1100 kHz

2.4.2.2 Staggered Quadriphase Pseudonoise

The modulator implementation used for frequency hop can be easily adapted for use with staggered quadriphase pseudonoise (SQPN) modulation. To use the modulator in figure 2-15 for SQPN we close the switches at the outputs of the two balance modulators and replace the C1 and C2 hop codes with two pseudonoise codes. Since all of the signals mentioned are TTL digital signals, the addition of a few logic gates will allow conversion from one mode to the other at the flip of a switch.

The staggered quadriphase pseudonoise waveform is generated by summing two biphase modulated quadrature carriers which have been modulated by two PN sequences displaced 1/2 chip with respect to each other. Figure 2-16 shows the SQPN implementation with the addition of a half chip delay for one of the codes. The PN code delay is part of the digital conversion for SQPN modulation and is not used in frequency hop mode.

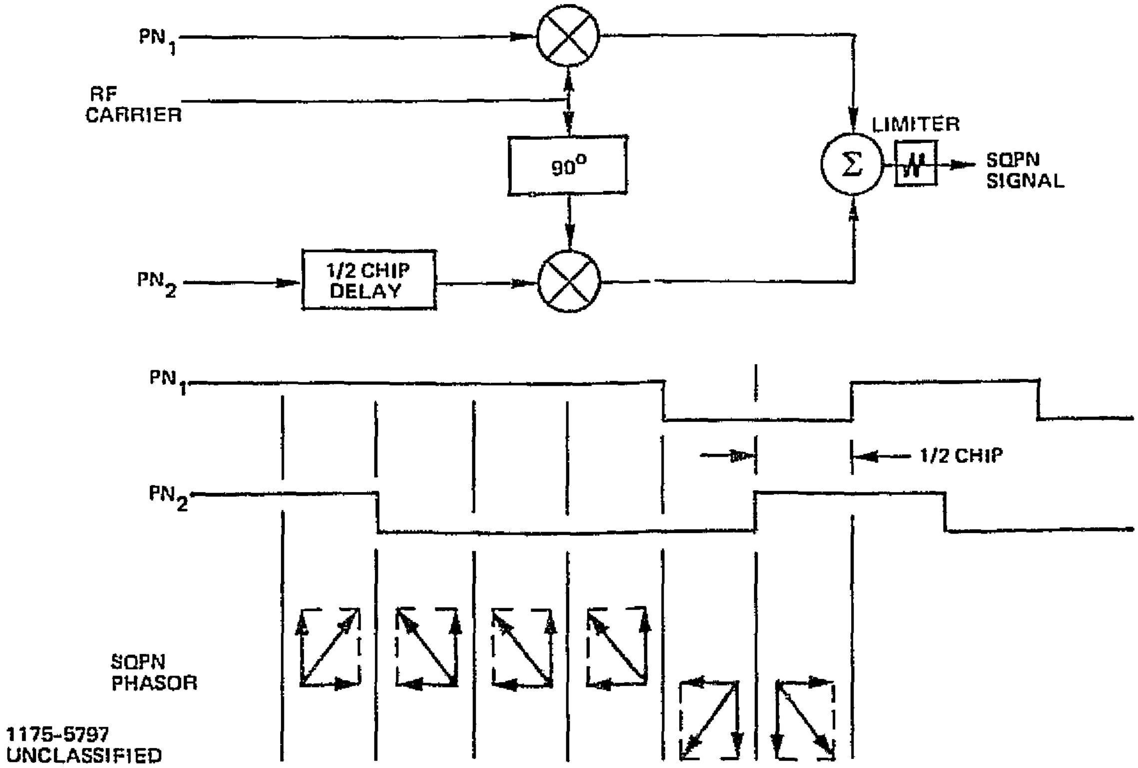

Figure 2-16. Staggered Quadriphase Pseudonoise

Figure 2-16 shows the resulting carrier phase transitions for each 1/2 chip of the codes. The characteristics of the SQPN spectrum are obtained by limiting the maximum phase change to 90°. As shown, the resultant phase rotation can only be 0 or $\pi/2$ during any code chip transition. The SQPN sidelobes can be filtered to eliminate adjacent channel interference. The sidelobes are not regenerated after passage through a nonlinear device.

2.4.3 RECEIVER DESIGN

The basic MMT receiver is capable of detecting hop correlation with up to 3 kHz of doppler offset, correcting for the doppler offset to within 100 Hz, performing a timed hop track, detecting SQPN correlation and tracking both the carrier and the code. The signal acquisition sequence is determined by the program in the system controller. The receiver functions are enabled by and provide decision feedback to the controller.

Both frequency hop and SQPN are coded time sequence modulations. The MMT receiver correlates or decodes the received signal by mixing it with a locally generated signal containing the same code sequence. When the locally generated signal is timed to line up with the code on the received signal, the mixer output is a narrowband signal containing the data modulation and doppler frequency offset of the received carrier. The mixer where this occurs is often referred to as the correlator. As shown in figure 2-17, the local reference signal is made by modulating the 15 MHz local oscillator signal with either the hop sequence or the SQPN code.

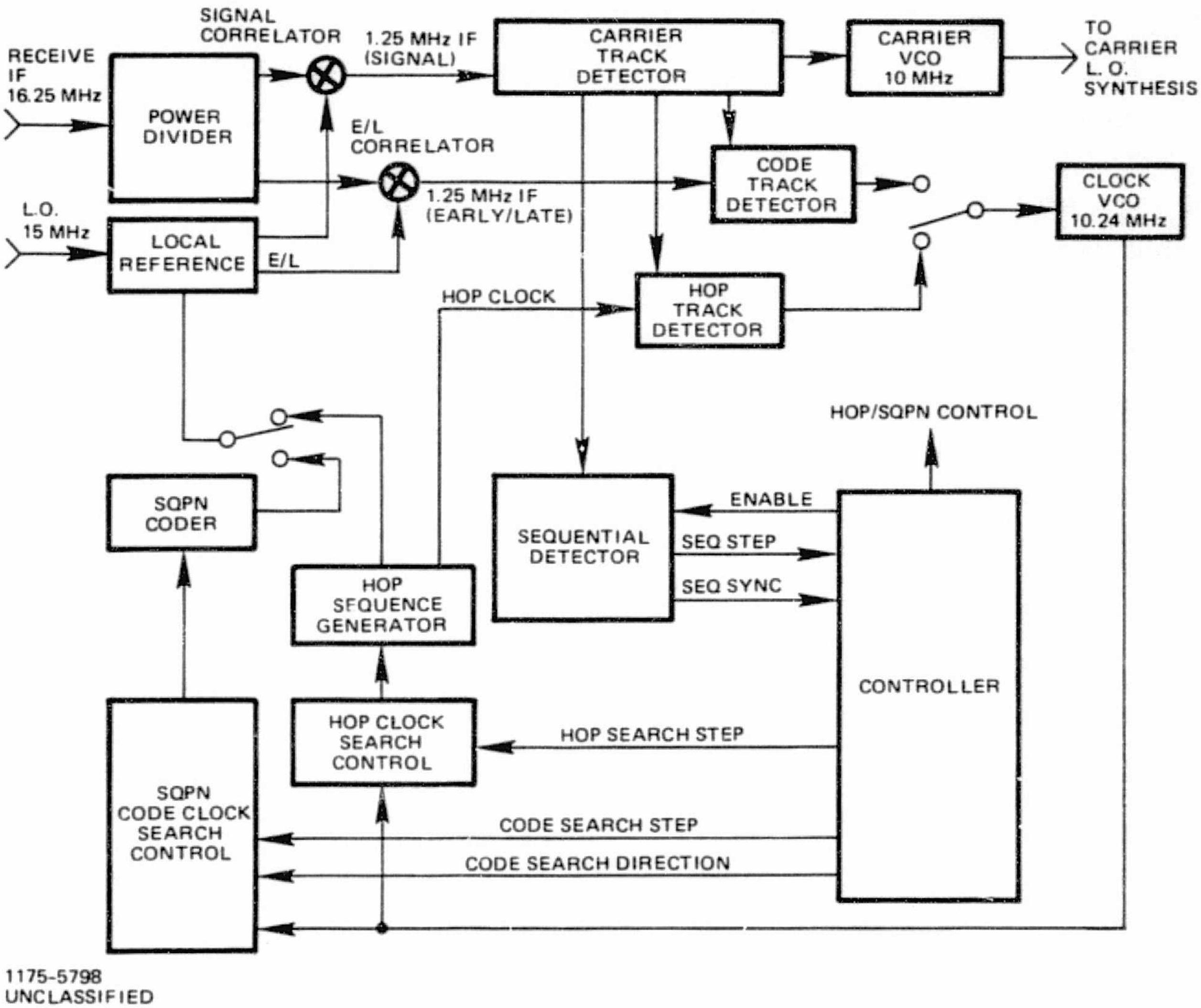

Figure 2-17. MMT Acquisition and Track Configuration

In the MMT receiver, the frequency hop signal is acquired first and then the receiver switches to SQPN. The search and track functions for hop and SQPN are different although some of the implementation is used for both modes. Both modes use the sequential detector to detect correlation. The sequential detector is a non-coherent detector using an integrate and dump technique to test for signal build up. When the sequential detector has looked for a sufficient length of time to determine that correlation has not been reached, a step pulse is sent to the controller. The controller sends a search pulse to the appropriate clock control which causes the locally generated code to precess the time equivalent to 1/4 of a code bit. When correlation is reached, the search stops and the controller advances to the next step in the acquisition sequence.

The code tracking for SQPN mode is derived from a correlator with the local reference signal present only for the code transitions. The early/late reference is gated on for 1/2 chip before and 1/2 chip after each state change of the code. The detected error signal corrects the clock VCO which provides the code clock reference frequency. The hop sequence tracking compares the detected carrier signal with the hop clock for the locally generated sequence. The detected error signal corrects the clock VCO which drives the hop sequence generator.

The signal demodulator portion of the MMT receiver is implemented with an acquisition sequence interface with the controller. The sequence of code search, track and automatic frequency correction is determined by the controller program. A functional block diagram of the MMT signal demodulator is shown in figure 2-18. This description follows the approximate sequence of events performed for signal acquisition. When the receiver is in the initialized condition waiting for the hop preamble, all three loop filters are dumped and the automatic frequency control (AFC) function is disabled. At initialization a load zero offset command returns the AFC to the nominal center frequency position. The controller performs hop search by retarding the relative time of the locally generated hop sequence by 1/4 hop slot each time the sequential detector dismisses and outputs a sequential step pulse.

When the locally generated hop sequence is in coincidence with the received hop sequence, the sequential detector declares sequential sync and stops putting out sequential step pulses. When the locally generated and received hop sequences are in

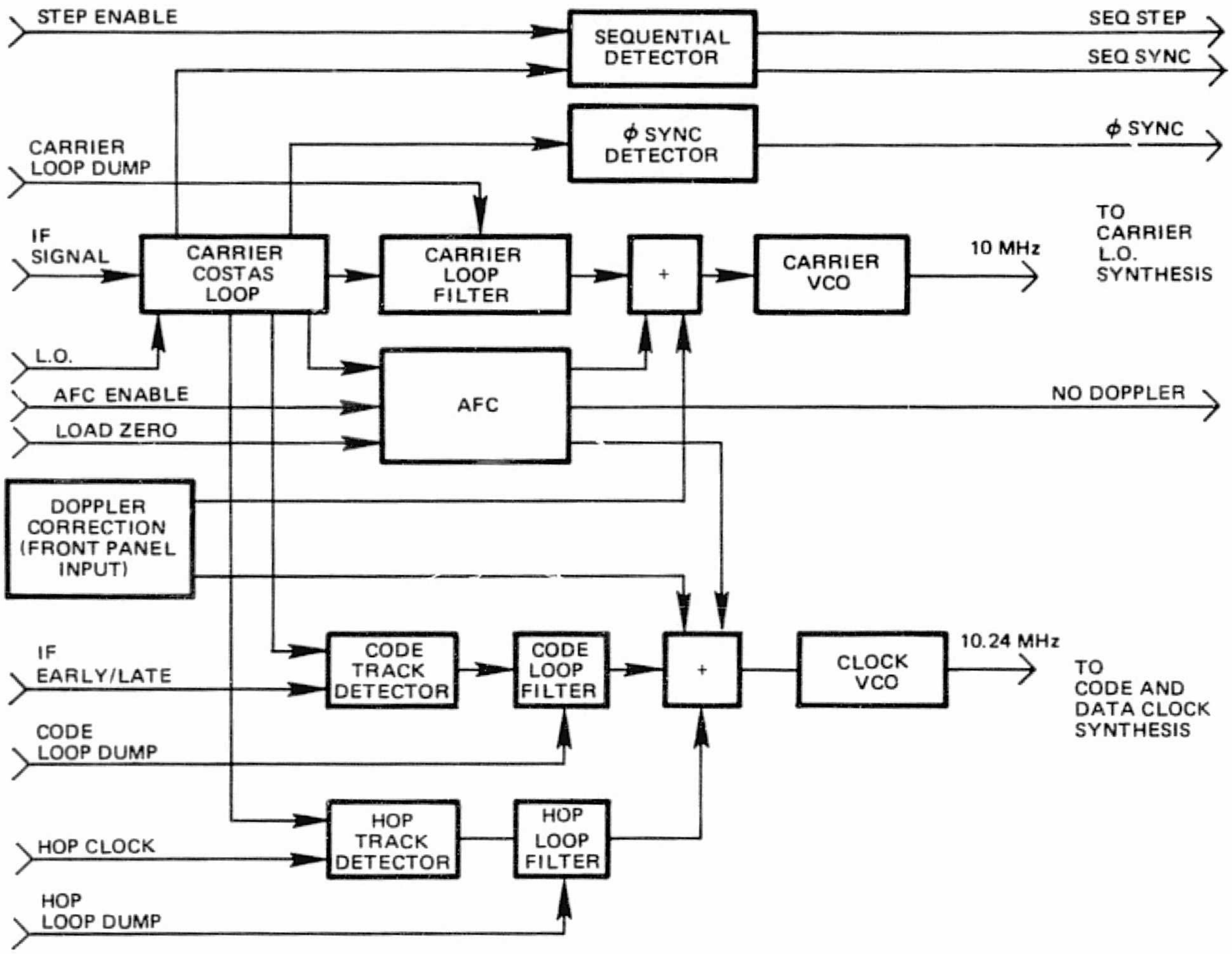

Figure 2-18. MMT Signal Demodulator

coincidence, the carrier frequency offsets cancel out in the correlator mixer. The resultant IF signal has only the doppler offset of the received signal. In order to detect the signal at the required threshold level with up to 3 kHz of doppler, the sequential detector consists of five sections of 600 Hz bandwidth. The five filters cover the band from 0 to 3000 Hz.

After the detection of hop coincidence, the hop loop filter is enabled. The hop search can stop the local hop sequence at any point from nearly complete hop time slot coincidence to less than 1/4 slot coincidence. With a strong signal 1/4 hop time coincidence is sufficient to declare hop coincidence (see figure 2-13). Near threshold full hop slot coincidence will be necessary for adequate signal build-up in the sequential detector.

The hop track detector compares the detected hop slot coincidence time with the hop clock used for the hop local reference signal. The filtered output of the hop track detector slews the clock VCO which provides the reference for the hop timing. As shown in figure 2-19, during the fixed hop track time the code loop filter and automatic frequency correction are disabled. The hop loop filter output is the only dynamic signal controlling the VCO at that time. The five seconds of hop track mode reduce the code time uncertainty to less than 20 microseconds. The hop track remains enabled until the doppler correction is completed.

Next, the AFC is enabled to perform the doppler correction. The maximum of ±3 kHz of carrier doppler is resolved to within 100 Hz of nominal frequency. A correction voltage is applied to the carrier VCO which is the frequency reference for the local oscillator synthesis. Correction with appropriate scaling is also applied to the clock VCO which is the frequency reference for the hop code, PN code and data clocks. The AFC is implemented to detect the sign of the offset and step in 100 Hz increments from nominal to 3000 Hz. A detector stops the search to tell the controller that doppler correction is complete. The frequency discriminator output voltage will also be within the window of the detector with no receiver input signal.

When doppler correction is completed, the controller switches from hop to SQPN mode. The local reference signal to the correlator is now the SQPN signal. While in hop, the SQPN code timing was derived from the hop sequence. Thus the hop mode reduced the time uncertainty between the received SQPN code and the locally generated SQPN code to less than 20 microseconds. When the MMT switches from hop mode to SQPN mode, the SQPN code timing is released from the hop timing in order to perform a bidirectional code search to resolve the remaining time uncertainty.

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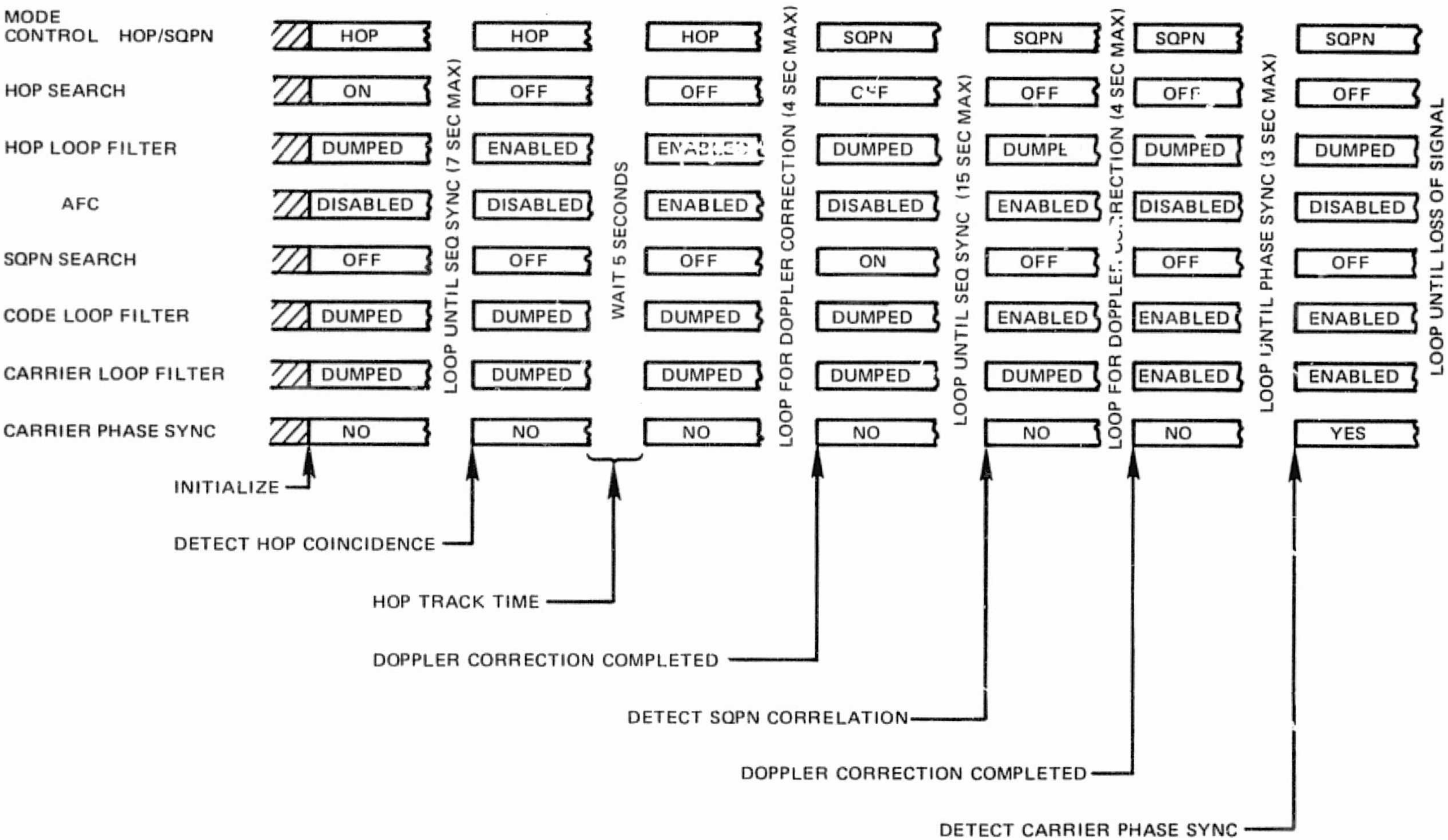

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Figure 2-19. MMT Hop Acquisition Sequence

SECTION III
FUNCTIONAL DESCRIPTION

The Multimode Transponder (MMT) and the Multimode Transmitter and Receiver (MTAR) units functional description is provided in this section.

3.1 GENERAL DESCRIPTION

This section contains a description of the MTAR (simulated ground terminal) and the MMT (simulated user spacecraft) equipment developed for evaluating candidate modulation techniques and signal acquisition procedures for TDRSS.

The MTAR equipment consists of five chassis plus data error rate test equipment and interconnecting cables.

a. The Receiver-Transmitter contains the RF to IF sections for both the receiver and the transmitter.

b. The Signal Processor contains all circuits from IF to baseband for both the receiver and the transmitter.

c. The Control Panel houses all mode selection switches and indicates the operational status of the equipment.

d. The Monitor Panel provides input/output jacks for interconnection to external equipment and signal monitoring.

e. The Power Supply provides all DC supply potentials to the other four chassis.

The MMT equipment also consists of five chassis which are similar in function and appearance to the MTAR equipment. The MMT equipment includes data error rate test equipment and interconnecting cables.

3.1.1 MTAR EQUIPMENT

The MTAR consists of a receiver and transmitter capable of operating at either VHF/UHF or S-Band frequency. The transmitter functional block diagram is shown in figure 3-1. The UHF output frequency is 401 MHz. For S-Band operation the 401 MHz is coherently translated to 2106.40625 MHz.

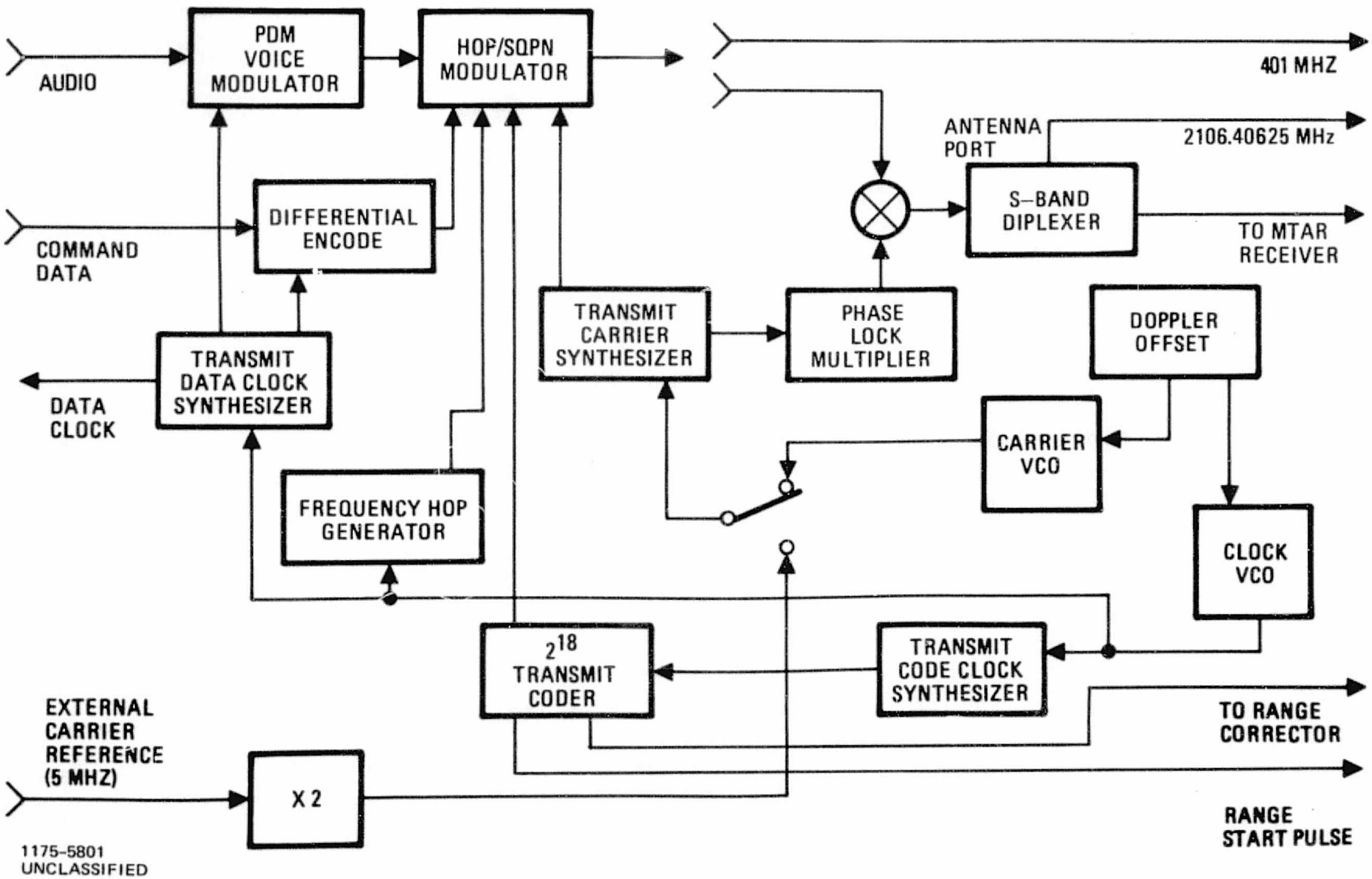

Figure 3-1. MTAR Transmitter, Block Diagram

The MTAR transmit carrier is synthesized from a crystal controlled VCO which can be manually offset to compensate for Doppler. In PSK mode digital data or PDM voice is balance modulated on the carrier. In SQPN mode the baseband data is balance modulated on the carrier via a staggered quadriphase pseudo-noise technique. A frequency hop preamble is used to speed up the SQPN acquisition time for the forward link. For initial acquisition the MTAR transmits a frequency hop modulation for a fixed length of time and then switches to SQPN modulation.

A clock VCO provides a stable frequency reference for the PN coder, the frequency hop sequence generator and the transmit digital data clock. The transmit clock VCO can be manually offset to compensate for Doppler. The transmit coder puts out a range start pulse which represents the PN code all ones vector. The transmit code start pulse is used with the receive code stop pulse to measure round trip range (time) via the MMT coherent transponder.

The MTAR receiver functional block diagram is shown in figure 3-2. The MTAR receiver can operate at either 137 MHz or 2287.5 MHz determined by appropriate RF connections on the front panel. The carrier local oscillator signals are synthesized from the carrier VCO.

The fourth mixer stage serves as the correlator in the SQPN mode of operation. The local reference circuitry balance modulates the receiver pseudo-noise codes with the 10.75 MHz local oscillator signal. When the code on the received signal is in phase with the locally generated code, a narrowband IF signal results.

In the SQPN mode the code tracking loop keeps the receiver reference code in phase with the code on the received signal. In the receiver, the incoming signal goes to a separate correlator and 1.25 MHz IF amplifier. The local reference provides this correlator with an early-late code from which a tracking error signal is derived. The error signal is filtered and drives the control line of the clock VCO. The clock VCO provides the frequency reference for both the code clock and data clock synthesis. The controller performs code search by advancing or retarding the code clock. In the conventional PSK mode the clock VCO and synthesizer are used to recover the received digital data clock.

The range correct function uses the range predict selected on the front panel to phase the 2^{18} receive code with respect to the MTAR transmit code phase. By centering the receive coder search at the predicted round trip propagation time the

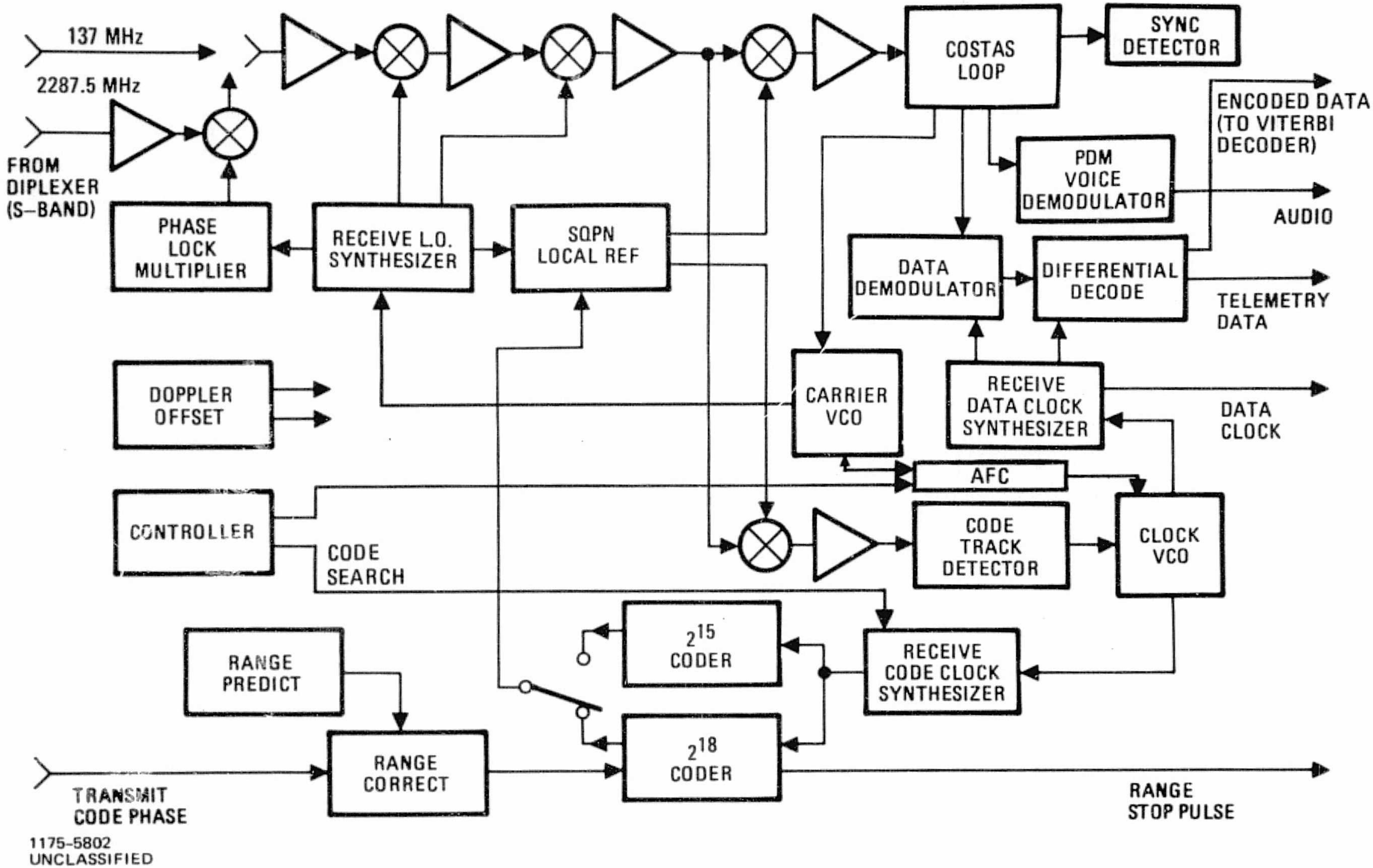

Figure 3-2. MTAR Receiver, Block Diagram

search aperture and resultant return link acquisition time can be kept short. Range correction is not applied to the 2^{15} coder. The 2^{15} coder is used in "return only" mode where there is no coherent turnaround of the forward link signal.

The anticipated Doppler frequency offset for the TDRS system is much greater than the carrier loop bandwidth. The coarse frequency correction is entered manually on the front panel using satellite ephemeris predict information. An automatic frequency control resolves ±3 kHz to allow for system and predict inaccuracies.

The demodulated digital data is differentially decoded. When in the convolutional encode mode a soft decision interface outputs the encoded data to a Viterbi decoder.

3.1.2 MMT EQUIPMENT

The MMT functions as a transponder receiving the forward link signal transmitted by the MTAR and transmitting a return link signal back to the MTAR. In the coherent mode the MMT transmit carrier signal is synthesized from the receiver VCO tracking the received signal. In the noncoherent mode the MMT transmit carrier signal is synthesized from an internal crystal controlled oscillator.

The MMT receiver functional block diagram is shown in figure 3-3. In S-Band operation the receive signal is a nominal 2106.40625 MHz. The MMT receiver demodulates either the frequency hop modulation or the SQPN modulation. The fourth mixer stage serves as the correlator for either modulation. When the locally generated sequence (hop or PN code) is in phase with the received signal, a narrowband IF signal results.

For initial forward link acquisition the MMT receiver searches in frequency hop mode until signal correlation is detected. In addition to hop search the controller directs the sequence of events necessary to complete the signal acquisition. After hop search stops, an automatic frequency correction is performed and the hop track function is enabled. The hop track brings the local reference and received signals to within 20 microseconds of each other. The receiver switches to SQPN mode and waits for the MTAR transmitter to switch to SQPN. Since the hop and SQPN codes are time related, the time uncertainty for SQPN search is on the order of the 20 microseconds obtained by hop track.

In the SQPN mode the code tracking loop keeps the receiver reference code in phase with the code on the received signal. A separate correlator and 1.25 MHz IF

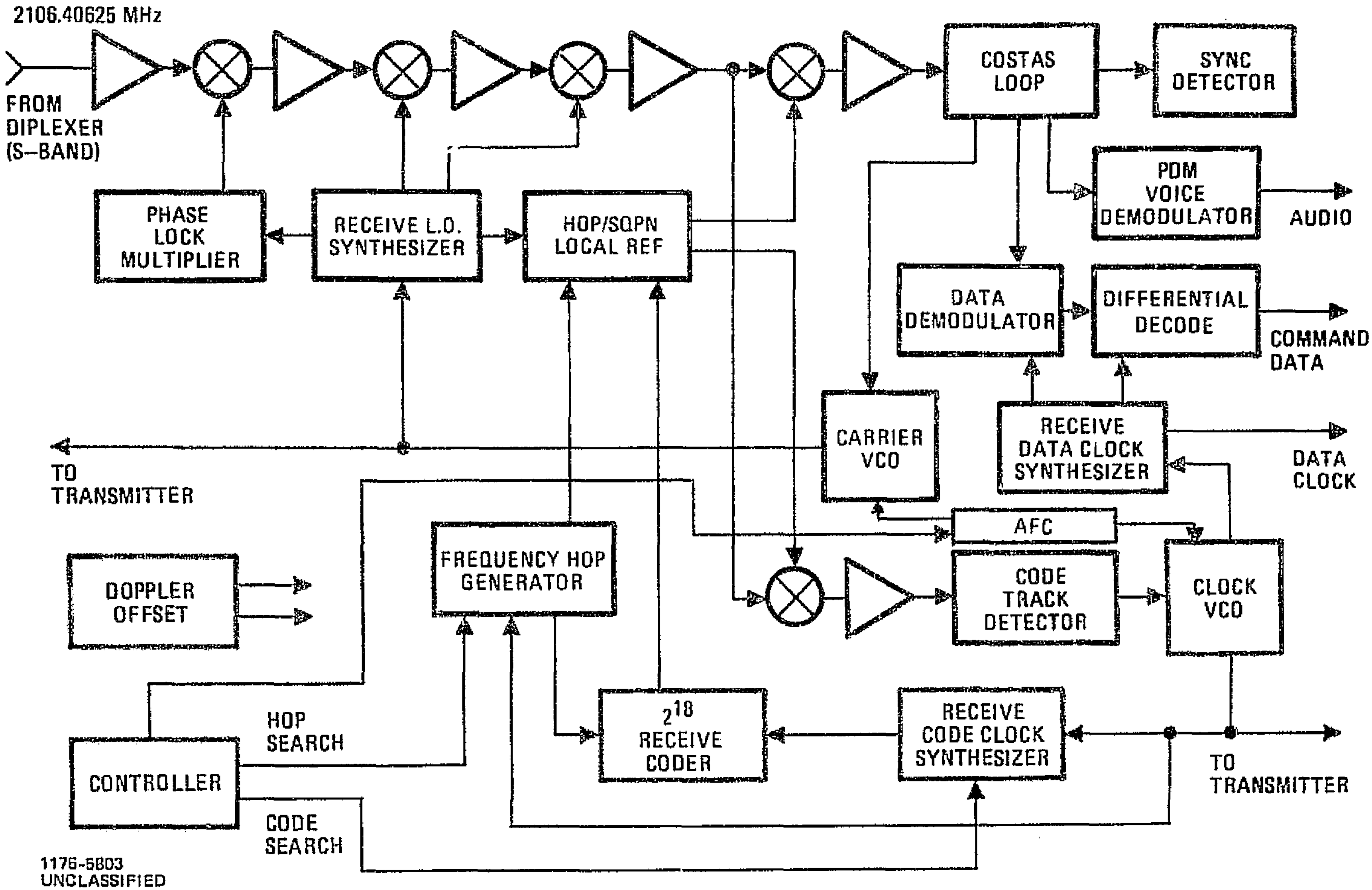

Figure 3-3. MMT Receiver, Block Diagram

amplifier is used for code tracking. The local reference provides this correlator with an early-late code from which a tracking error signal is derived. The error signal is filtered and drives the control line of the clock VCO to provide the frequency reference for both the code clock and data clock synthesis. The controller performs code search by advancing or retarding the code clock with an IPM in the code clock synthesizer. In the conventional PSK mode the clock VCO drives a data clock IPM to recover the clock for the received digital data.

The MMT implementation includes front panel manual frequency offset to compensate for simulated Doppler offsets set at the MTAR transmitter. A laboratory setup will simulate a Doppler frequency with a carrier offset rather than with actual relative motion of the transmitter and receiver. An automatic frequency control resolves ±3 kHz to allow for system inaccuracies.

The MMT transmitter functional block diagram is shown in figure 3-4. The S-Band output frequency of the MMT transmitter is 2287.5 MHz. The MMT transmit carrier is synthesized from either the receiver VCO or an internal carrier oscillator. The clock for code and data clock synthesis comes from either the code track VCO or an internal clock oscillator.

In PSK mode, digital data on PDM voice is balance modulated on the carrier. In SQPN mode the baseband data is balance modulated on the carrier with a staggered quadriphase pseudo-noise technique. For coherent and noncoherent link modes a 2^{18} chip code length is used. Return only mode uses a 2^{15} chip code length.

Convolutional encoding may be applied to the digital data transmitted on the return link. Return link digital data is differentially encoded. When the dual data mode is selected, a different data stream may be applied to each of the two balanced mixers in the SQPN modulator. In the synchronous data mode a data clock output drives the external data source. In the asynchronous mode an external data source must provide a data clock to the MMT.

3.2 MMT (SIMULATED USER TRANSPONDER)

The Multimode Transponder (MMT) consists of a receiver-transmitter chassis, signal processor chassis, control panel, signal monitor panel and power supply chassis. This section gives a detailed functional description of each of these assemblies. The error rate test equipment used with the MMT is described in section 3.4.

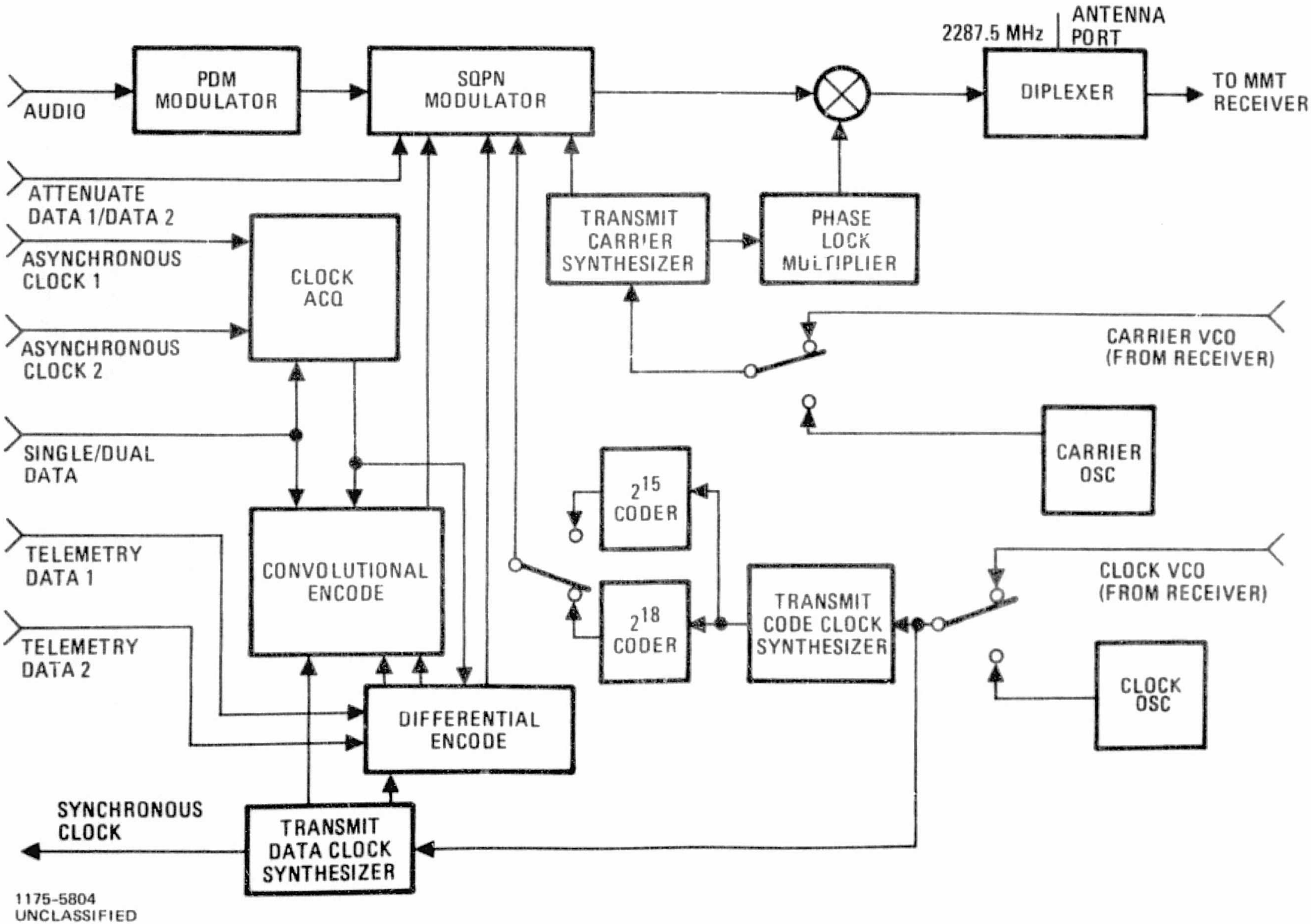

Figure 3-4. MMT Transmitter Block Diagram

3.2.1 RECEIVER-TRANSMITTER CHASSIS

The receiver-transmitter chassis contains the high frequency elements that connect directly to an antenna with both transmit and receive signals. The transmit section of the RT chassis converts a modulated 137 MHz signal to the S-Band transmit frequency of 2287.5 MHz. The receive section amplifies and converts the 2106.40625 MHz signal to a 16.25 MHz intermediate frequency. Figure 3-5 shows the front and top views of the MMT RT chassis. Figure 3-6 is a block diagram of the MMT receiver-transmitter chassis.

The S-Band modification task of contract NAS5-20330 implemented the conversion of the original VHF/UHF frequencies to S-Band frequencies. The 137 MHz transmit signal is accessible by removing a front panel jumper cable. The 401 MHz receive input is also available by removing a front panel jumper cable.

As shown in figure 3-6 the local oscillator for conversion of the 137 MHz modulator output to S-Band is obtained by multiplying the 18.7 MHz L.O. input by 115 in a phase lock multiplier. The 18.7 MHz L.O. is coherent with the 137 MHz transmit carrier signal. Signal monitor jacks are provided for both the 137 MHz and 2287.5 MHz transmit signals. The 2287.5 MHz monitor output is amplified to provide at least 0 dBm signal power to drive a frequency counter. Individual power switches are mounted in the chassis for the transmit PLM and the transmit monitor amplifer to aid in isolating any interference with other equipment in the laboratory setup.

A diplexer is used to isolate the receiver input from the transmit signal. The received signal is amplified and converted in three IF steps to 16.25 MHz. The last two IF stages are enclosed in a shielded assembly. The schematic of the MMT IF assembly is Drawing X498733. The 67.75 MHz IF stage is where the system AGC is applied. The AGC control voltage is developed in the signal demodulator and is brought to the RT chassis on pin K of connector J2. When the equipment modification was completed, pin K was the only pin used on connector J2. For testing and troubleshooting the AGC can be disabled giving maximum RF gain by simply disconnecting the cable to J2. The receive local oscillator signals are synthesized in the signal processor chassis and brought to the RT chassis via coaxial cables.

3.2.2 SIGNAL PROCESSOR CHASSIS

The MMT signal processor chassis contains the receiver circuitry from the 16.25 MHz IF down to baseband processing and transmit baseband and modulation

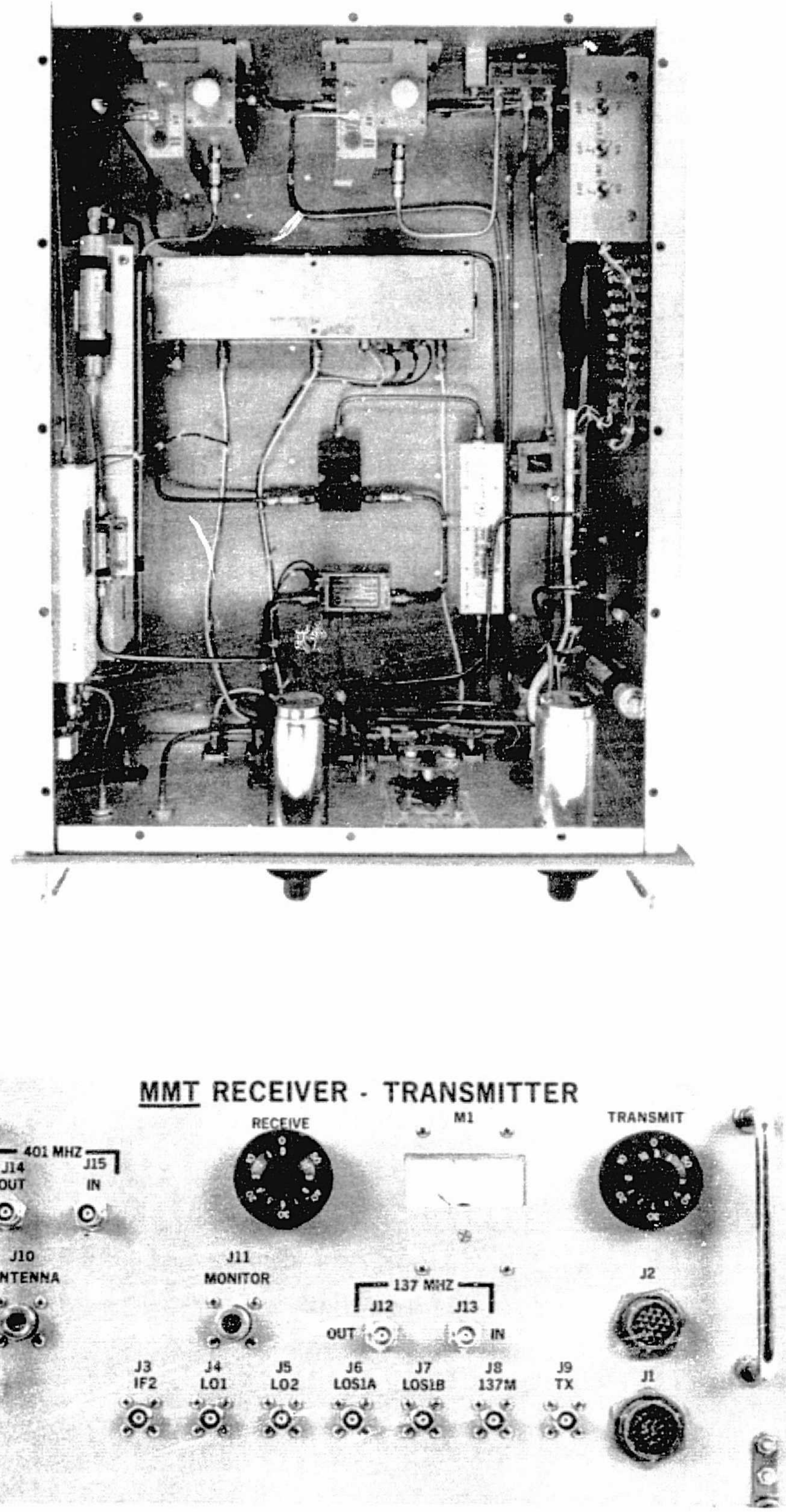

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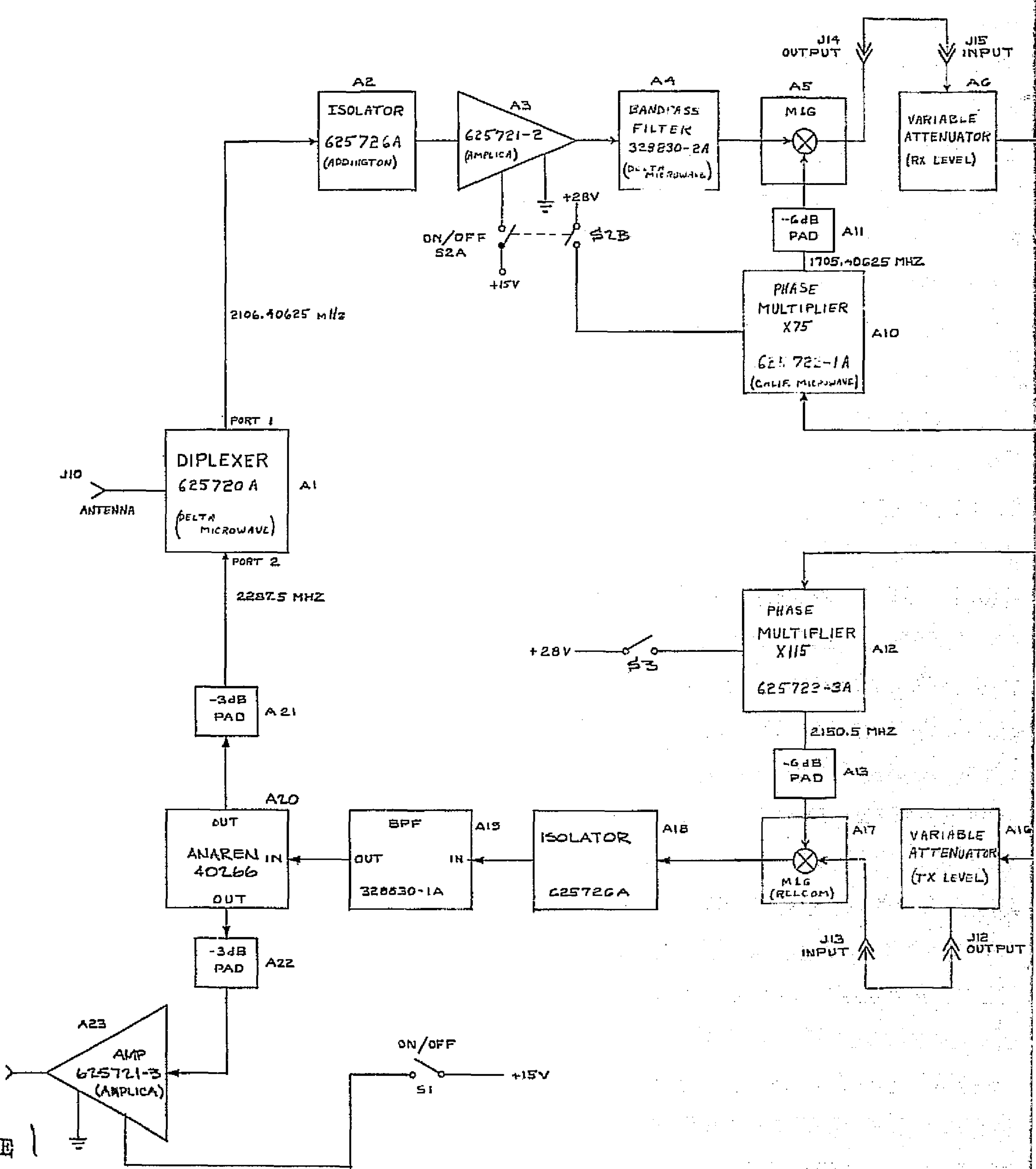
Figure 3-5. MMT Receiver-Transmitter, Front and Top Views



FOLDOUT FRAME 1

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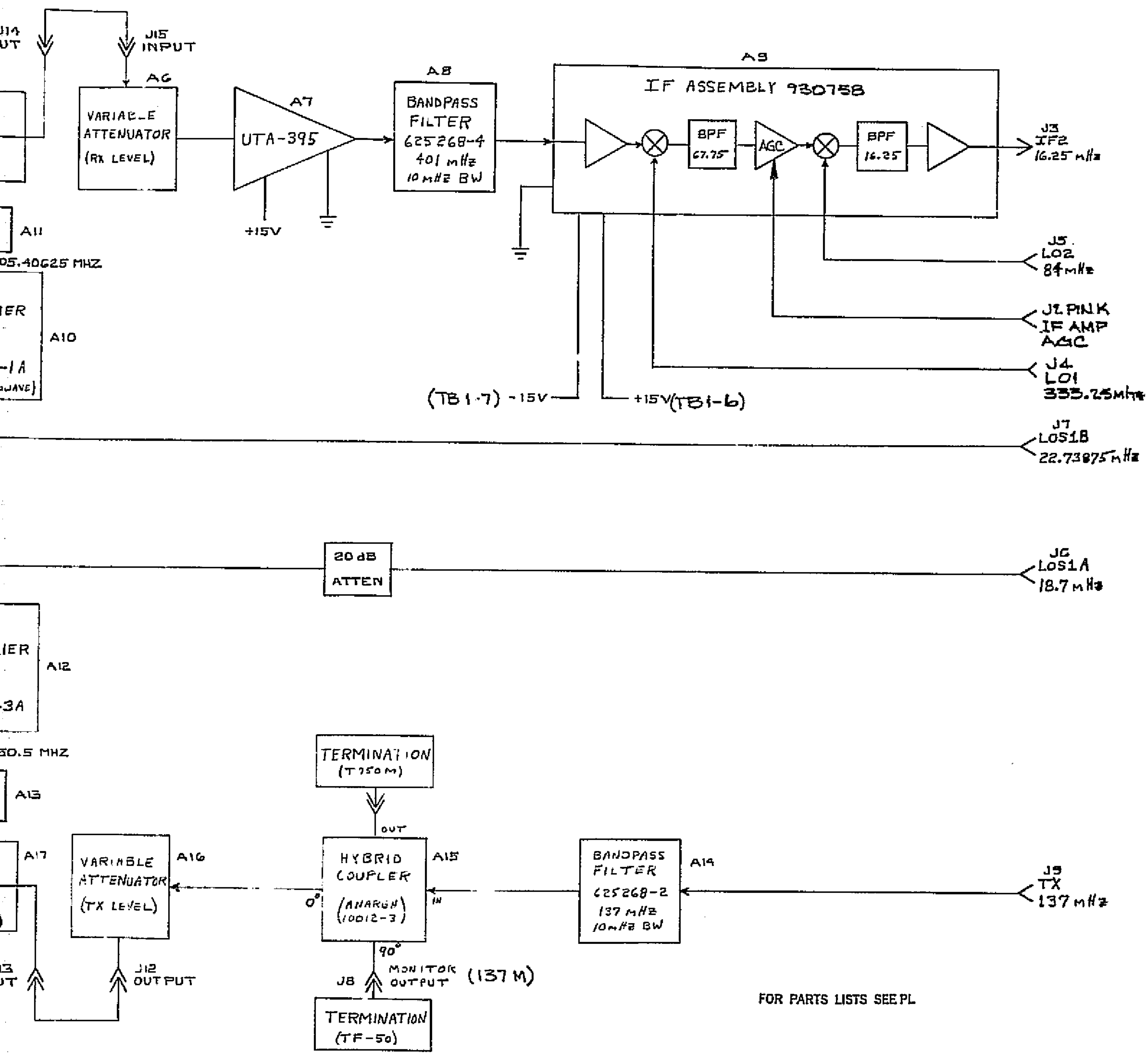

FOLDOUT FRAME 2

Figure 3-6. MMT Receiver-Transmitter Block Diagram circuitry. The MMT signal processor is made up of plug-in printed circuit boards. Table 3-1 gives a list of the board nomenclature showing location in the MMT chassis.

Table 3-1. MMT Printed Circuit Board Data

Assembly Dwg. No.	PC Board Nomenclature	Schematic Dwg. No.	Location	Quantity
X918051A	Code & Data Clock Synth.	X498701A	2A08	1
X918052A	Coder No. 1	X498702A	2A06	1
X918053A	Coder No. 2	X498703A	2A07	1
X918054A	Controller No. 1	X498704A	3A03	1
X918074A	Controller No. 2	X498724A	3A02	1
X918055A	MMT Local Reference/ Correlator	X498705A	2A09	1
X918061A	Receive Filter	X498711A	3A09	1
X918088A	MMT Detector	X498712A	3A08	1
X918091A	MMT VCO	X498726A	3A07	1
X918096A	MMT Frequency Discriminator	X498735A	3A10	1
X918069A	Frequency Hop	X498719A	1A09	1
X918063A	MMT Data Recovery	X498713A	1A03	1
X918095A	MMT Oscillator	X498764A	2A05	1
X918066	PDM Voice	X498716	2A02	1
X918067	MMT/MTAR Synth. No. 1	X498717	1A06 & 3A06	2
X918068	MMT Synthesizer No. 2	X498718	1A05 & 3A05	2
X918086A	MMT Data Input	X498736	1A08	1
X918070A	TX Data Processor	X498720A	1A02	1
X918072A	MMT Modulator	X498722A	2A03	1
X918089	18.7 MHz Synth.	X498739	1A01	1
X918081	22.73875 MHz Output	X498731	2A01	1
X918082	27.3875 MHz Synth.	X498732	3A01	1

Figure 3-7 shows the front and top views of the MMT signal processor chassis. The printed circuit board locations in the signal processor chassis are identified by a four character number. The first number identifies the row with 1, 2 and 3 indicating the front, middle and rear rows respectively. The last two digits locate slots 1 through 10 in each row. The second character is an A in the MMT signal processor chassis and a B in the MTAR signal processor chassis.

3.2.2.1 Frequency Synthesis

The signal processor chassis contains the frequency synthesis circuitry for the receive local oscillator signals and the transmit carrier. Since the S-Band conversion for the transmit and receive functions is located in the RT chassis, the S-band L.O.'s are cabled from the signal processor to the RT at relatively low frequencies. Phase lock multipliers in the RT multiply the S-Band L.O. signals. The 18.7 MHz transmit L.O. is multipled by 115 to 2150.5 MHz. The 22.73875 MHz receive L.O. is multiplied by 75 to 1705.40625 MHz.

The S-Band modification effort added the necessary coherent S-band synthesis while retaining the old VHF/UHF synthesis. Figure 3-8 shows the reference frequency distribution and synthesis configuration of the MMT. Printed circuit board nomenclature, location in the signal processor chassis and connector pin numbers are shown.

The MMT must be capable of functioning either as a coherent transponder or in a mode with the forward and return links completely independent of each other. In the coherent mode the transmit carrier and code clock frequency references are phase coherent with the received signal. This is done by using the receiver carrier and code VCO's as the references for the transmit synthesis. The two switches shown on the MMT oscillator board (2A05) in figure 3-8 are shown in the coherent position. The outputs of board 2A05 drive the transmit carrier and code synthesis. Both the noncoherent and return only modes selectable with the link mode switch on the control panel would use the crystal oscillators located on board 2A05 for transmit references.

Note that the signal processor front panel manual Doppler correction is applied to the receiver VCO's. This is to compensate for the simulated forward link Doppler offset that may be applied to the MTAR transmit signal. Note that any Doppler offset on the forward link is turned around only in the coherent link mode. In the noncoherent and return only link modes the MMT receiver can track the forward link

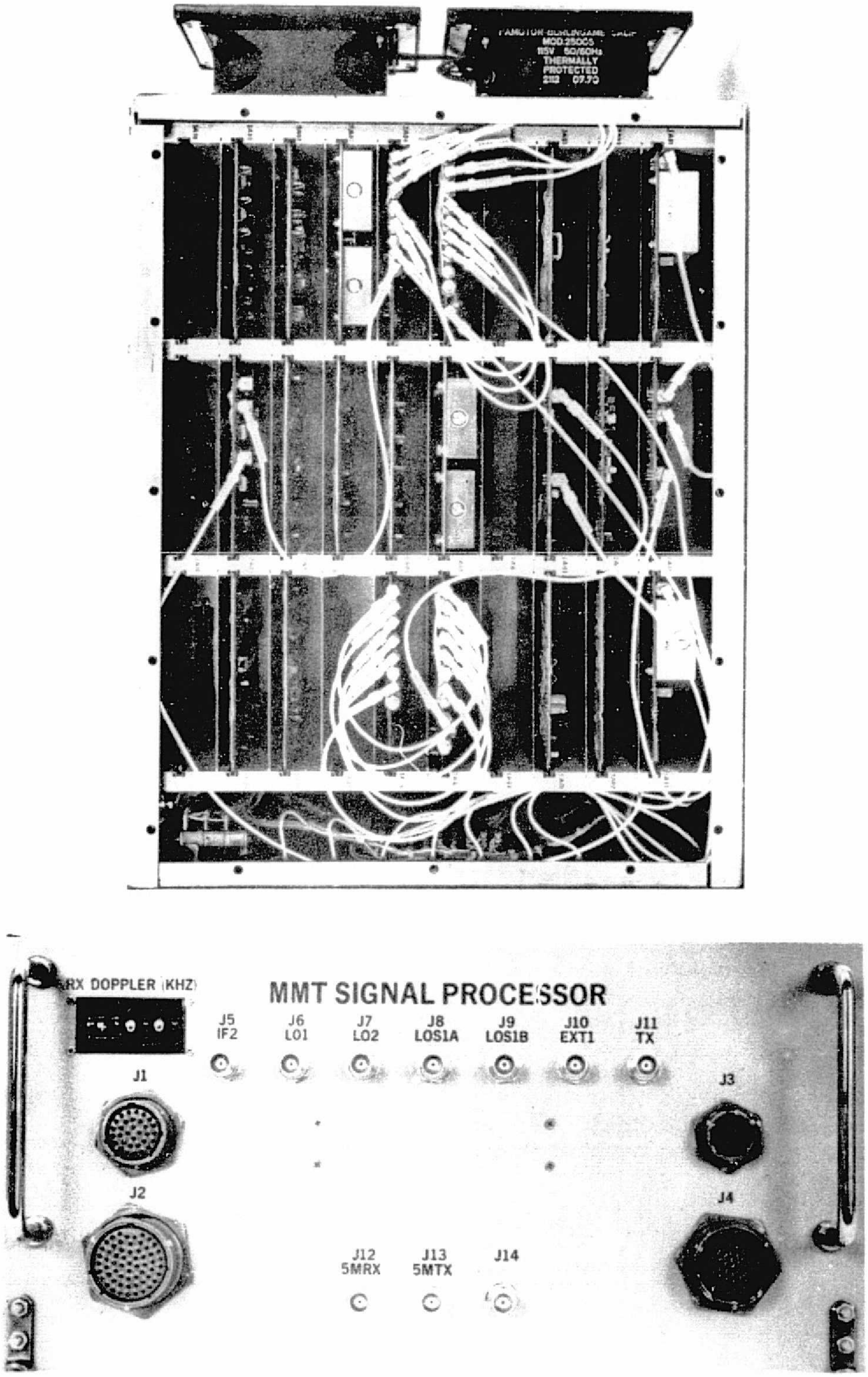

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Figure 3-7. MMT Signal Processor, Front and Top Views

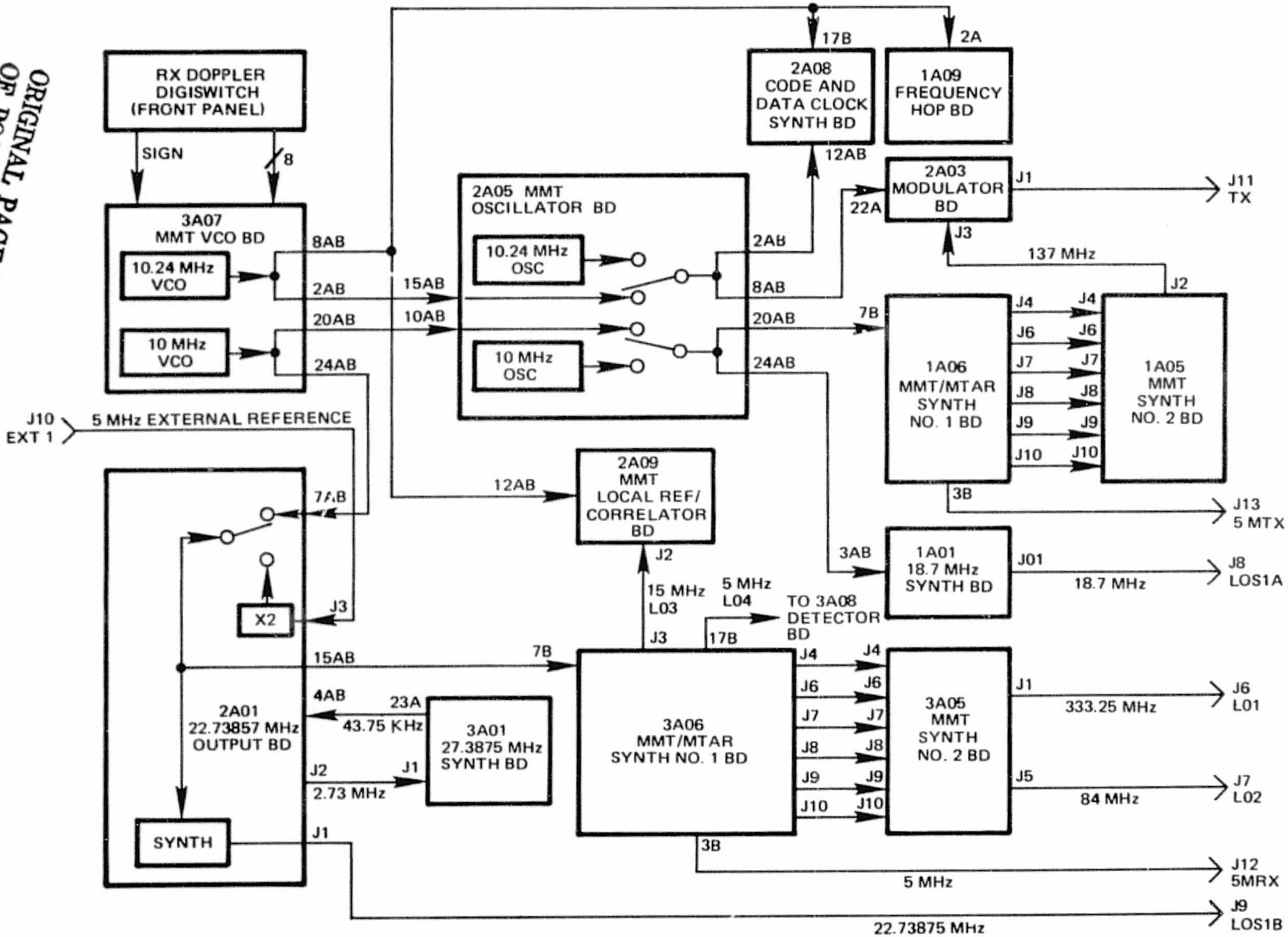

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Figure 3-8. MMT Reference Frequency Distribution signal but the return link frequencies are determined by the crystal oscillators located on board 2A05.

The external 5 MHz reference function was designed into the 22.73875 MHz synthesizer board (2A01) primarily for use in the MTAR. Since the same PC board is used in both the MMT and MTAR, the external function was wired in the MMT but would only be used under certain troubleshooting circumstances. As shown in figure 3-8 the function in the MMT allows the receiver carrier VCO to be replaced by an external frequency source to drive the receive L.O. synthesis.

The VHF/UHF frequency synthesis function uses two unique boards. The 3A05 and 3A06 set of boards is used for the receiver L.O. synthesis. The 1A05 and 1A06 set of boards is used for the transmit carrier synthesis. The two sets of boards are identical with different outputs used for the transmit and receive functions. Figure 3-9 is a functional diagram of the circuitry contained on the two boards.

Three printed circuit boards are used to synthesize the coherent local oscillator signals for S-band translation of the MMT transmit and receive signals. Figure 3-10 is a functional diagram of these three boards. The 18.7 MHz synthesizer board (1A01) generates the LOS1A signal used for S-band transmit conversion in the MMT. The 27.3875 MHz synthesizer board (3A01) and the 22.73875 MHz output board (2A01) combine to generate the LOS1B signal used for S-band receive conversion in the MMT.

3.2.2.2 Receiver

The MMT receive signal budget is shown in figure 3-11. The precorrelation bandwidth is determined by the code rate. The postcorrelation bandwidth is set by the digital data rate selected. Figure 3-12 is a detailed block diagram of the MMT postcorrelation receiver. The receiver functions determined by the controller include step enable, carrier loop dump, code loop dump, hop loop dump, AFC enable and AFC load. The receiver decisions fed back to the controller include sequential step, sequential sync, no Doppler and phase sync.

The MMT receiver boards include the MMT VCO board (3A07), the MMT detector board (3A08), the receive filter board (3A09) and the MMT frequency discriminator board (3A10).

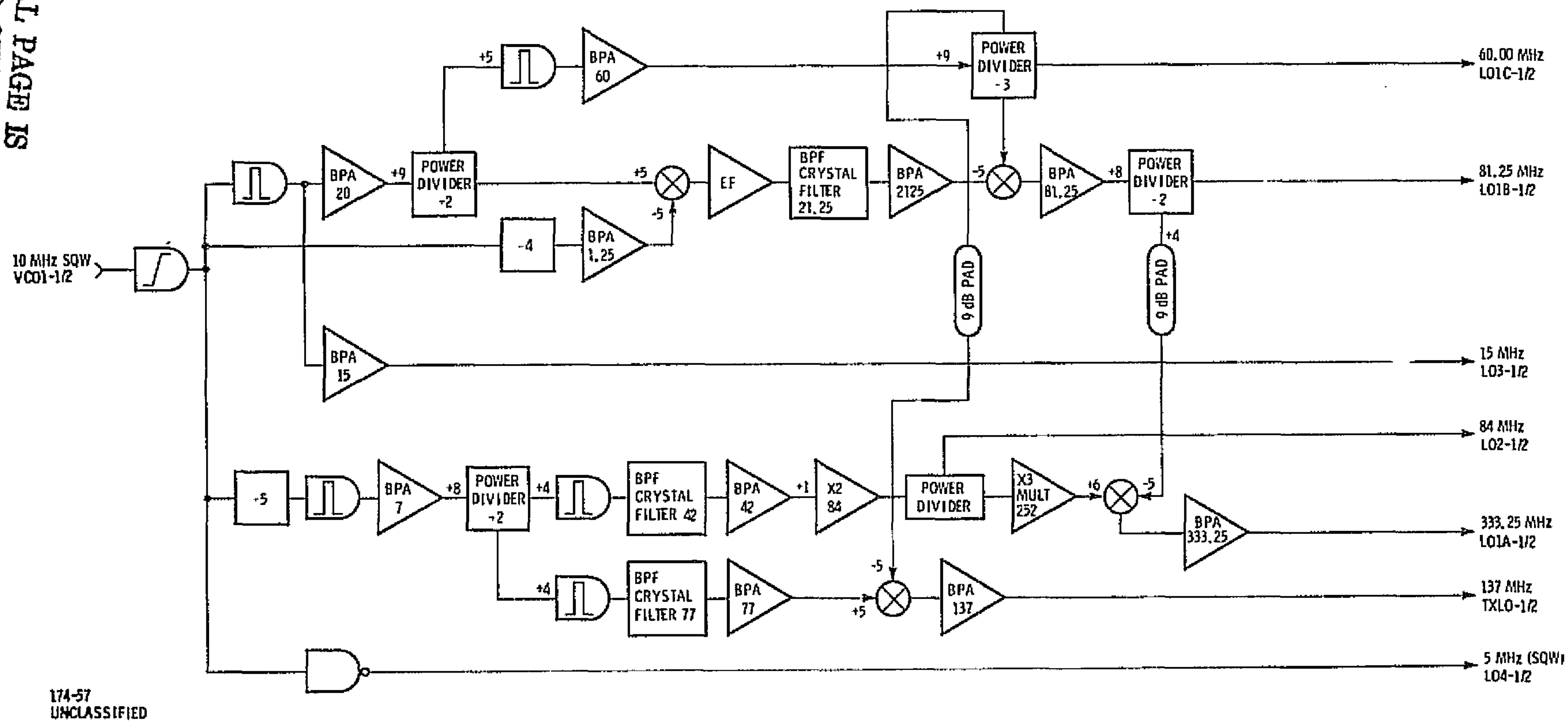

Figure 3-9. MMT VHF/UHF Synthesis

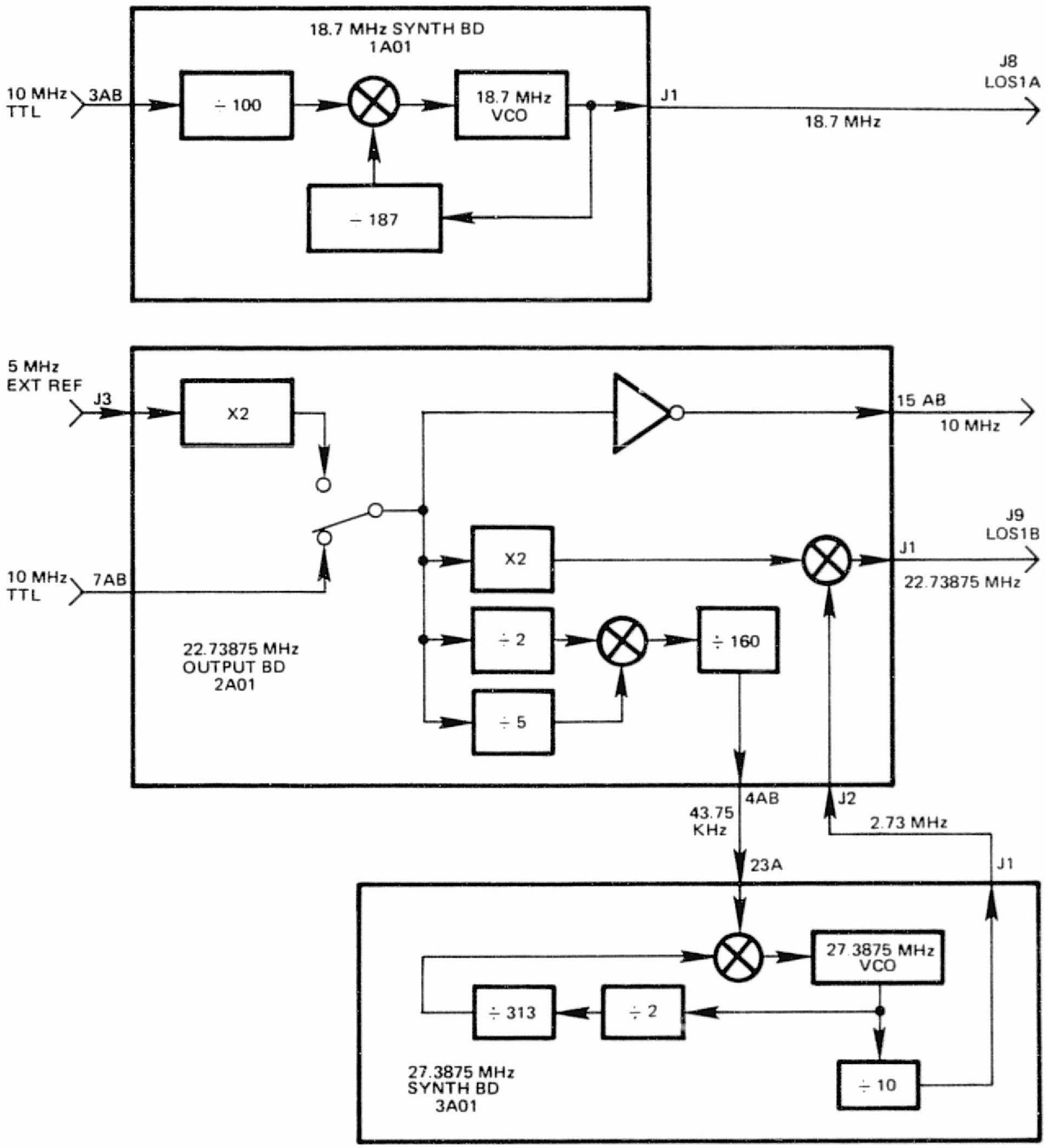

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Figure 3-10. MMT S-Band Synthesis

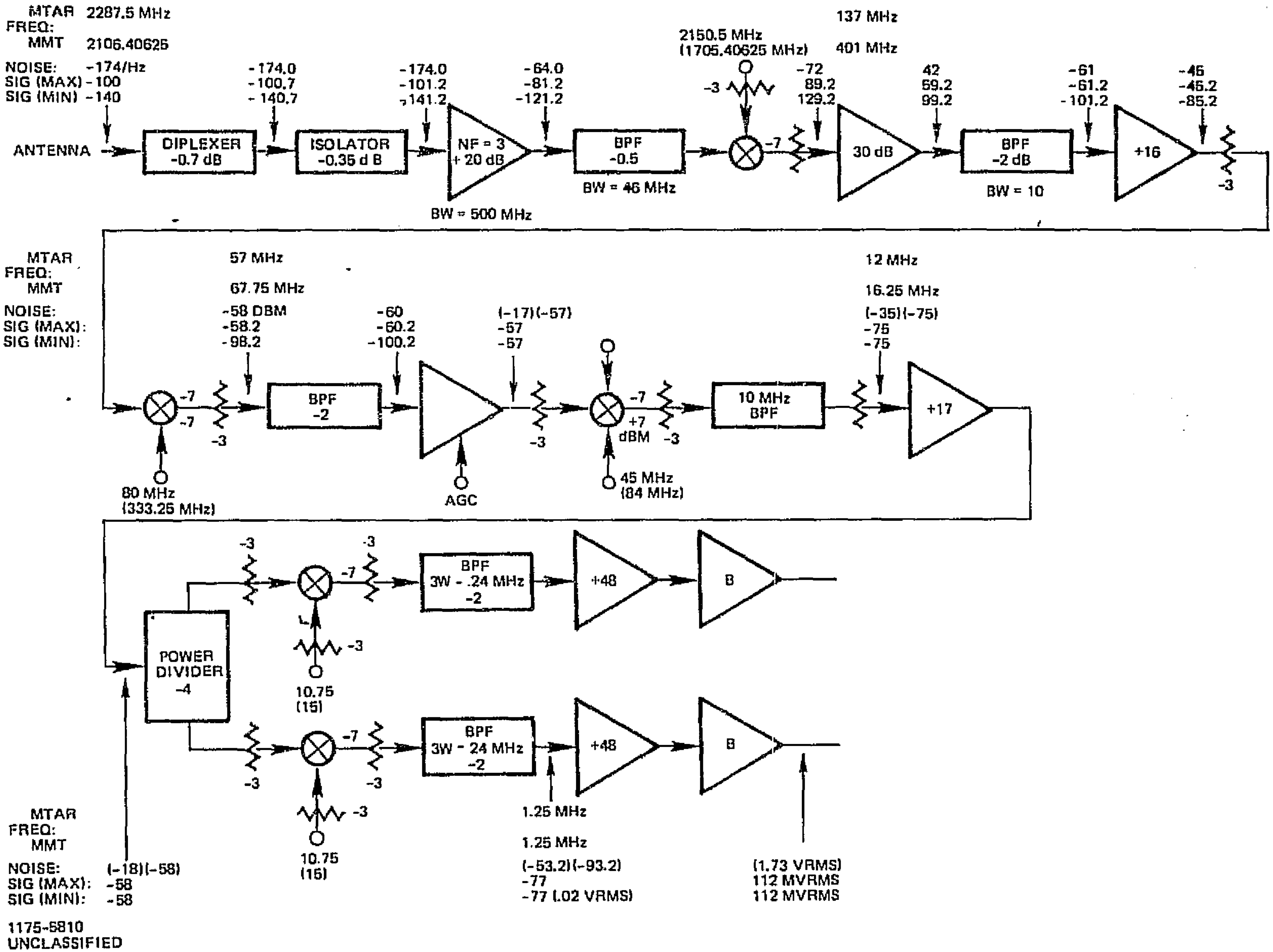

Figure 3-11. Receiver Signal Budget

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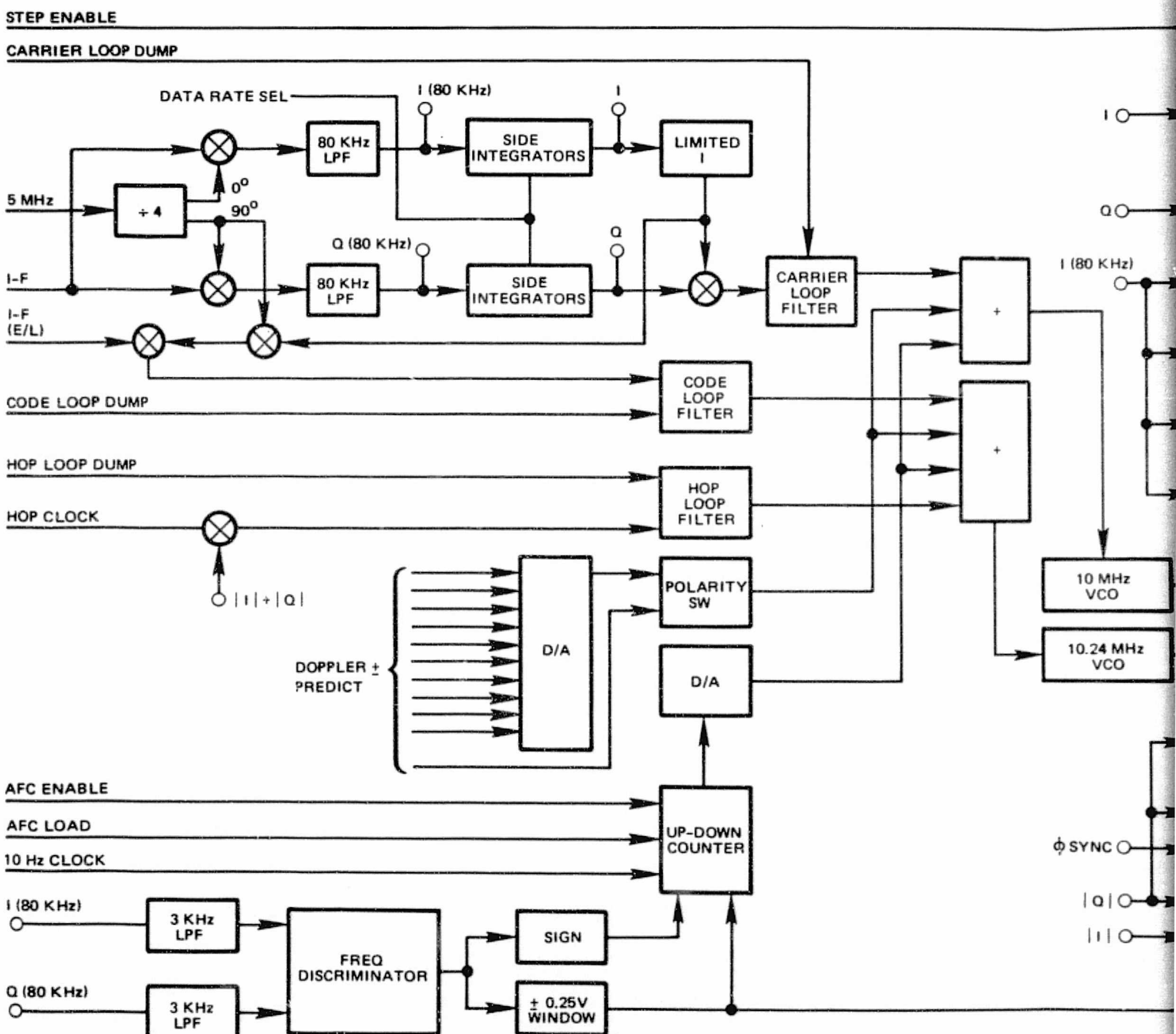

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.DOUT FRAME /

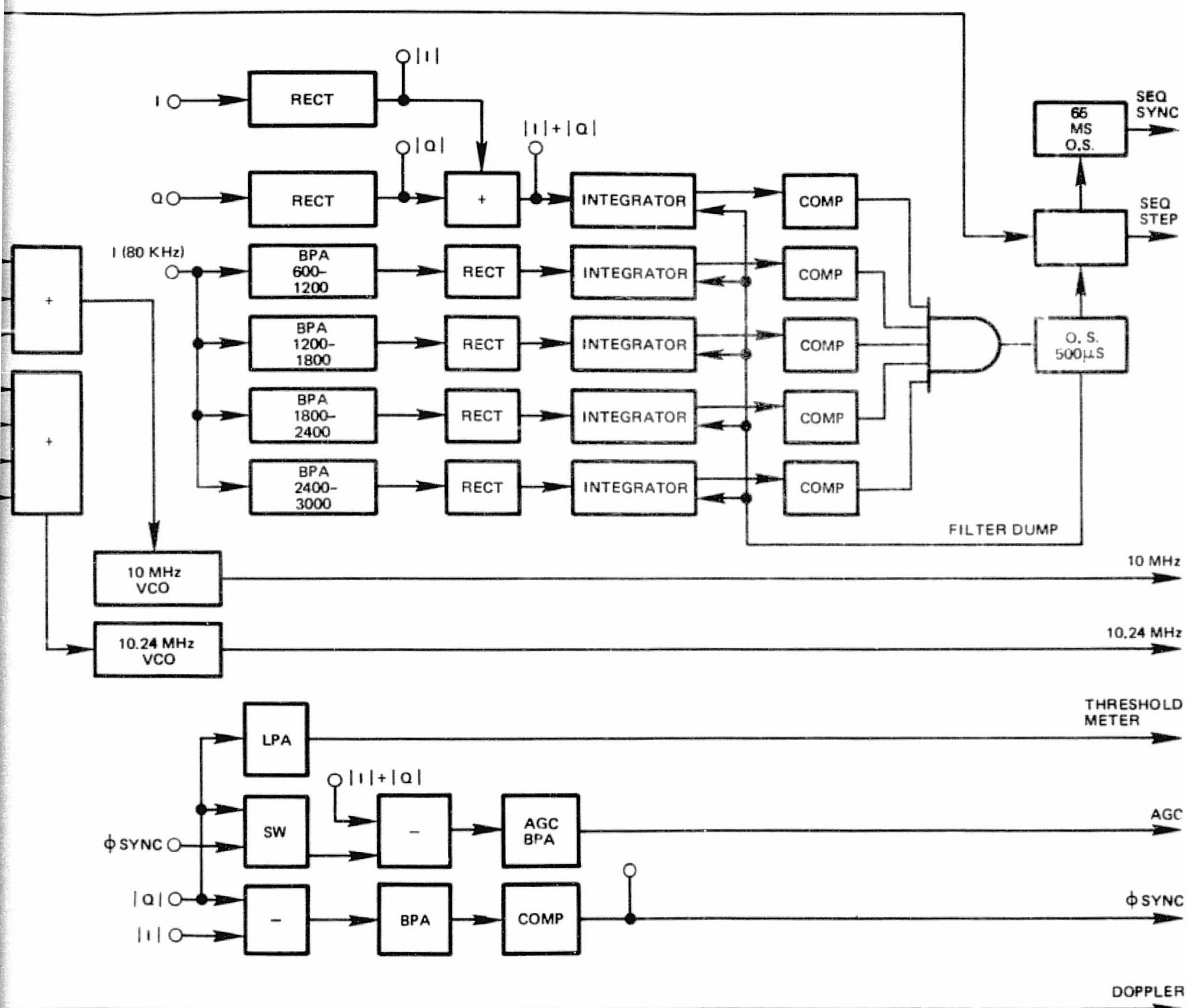

Figure 3-12. Receiver Detailed Block Diagram

3.2.2.3 Controller

The MMT/MTAR controller block diagram is shown in figure 3-13. The controller ROM program and flowchart are shown in figure 3-14. The controller program includes the system operation commands for both the MMT and MTAR. A hard-wired input in each chassis tells the controller which unit program to follow. The MMT uses Controller Board No. 1 (3A03) and Controller Board No. 2 (3A02).

The controller consists of two printed circuit boards, Controller Board 1 and Controller Board 2. Controller Board 1 consists of a program counter, ROM memory, decoder logic, timer, input multiplexers upon which jump decisions within the program are made based on input signals, a digital Incremental Phase Modulator (IPM) signal generator, and output lines from the ROM memory which go to Controller Board 2.

3.2.2.3.1 Controller Board 1

Controller Board 2 contains decode, logic and various flip-flops to generate output control signals, and a timer used on the MTAR for transmitting the frequency hop signal for 15 seconds during initial forward link acquisition by the MMT.

The program counter consisting of integrated circuits U1G and U9G is an 8-bit binary counter that operates from a 4 kHz clock input, and has a direct reset input (INITIALIZE). The counter's 8 binary output lines go to the ROM's (U2E) 8 binary inputs. The ROM's 8 binary outputs come back to the program counter's preset inputs and can thus cause the counter to jump to a binary number other than the next number in a normal binary counting sequence. The counter will then proceed counting from this new number.

The ROM memory (U2E) is a 2048 bit memory organized as 256 8-bit memory locations. That is there are eight inputs coming from the program counter that select one of 256 addresses (2^8). The selected address enables its 8-bit word (or binary pattern) to then appear at the 8 output pins of the ROM package. The 8 output lines go the preset inputs of the program counter and timer and to decoder logic that enables the timer, IPM signal generator, and input select multiplexers. The ROM output lines also go to Controller Board 2. The ROM is electrically programmable and is erased with ultraviolet light.

The decoder logic consisting of U72G, U72J, U11C and various gates enables the timer, IPM Signal Generator, and input select multiplexers. Only one of

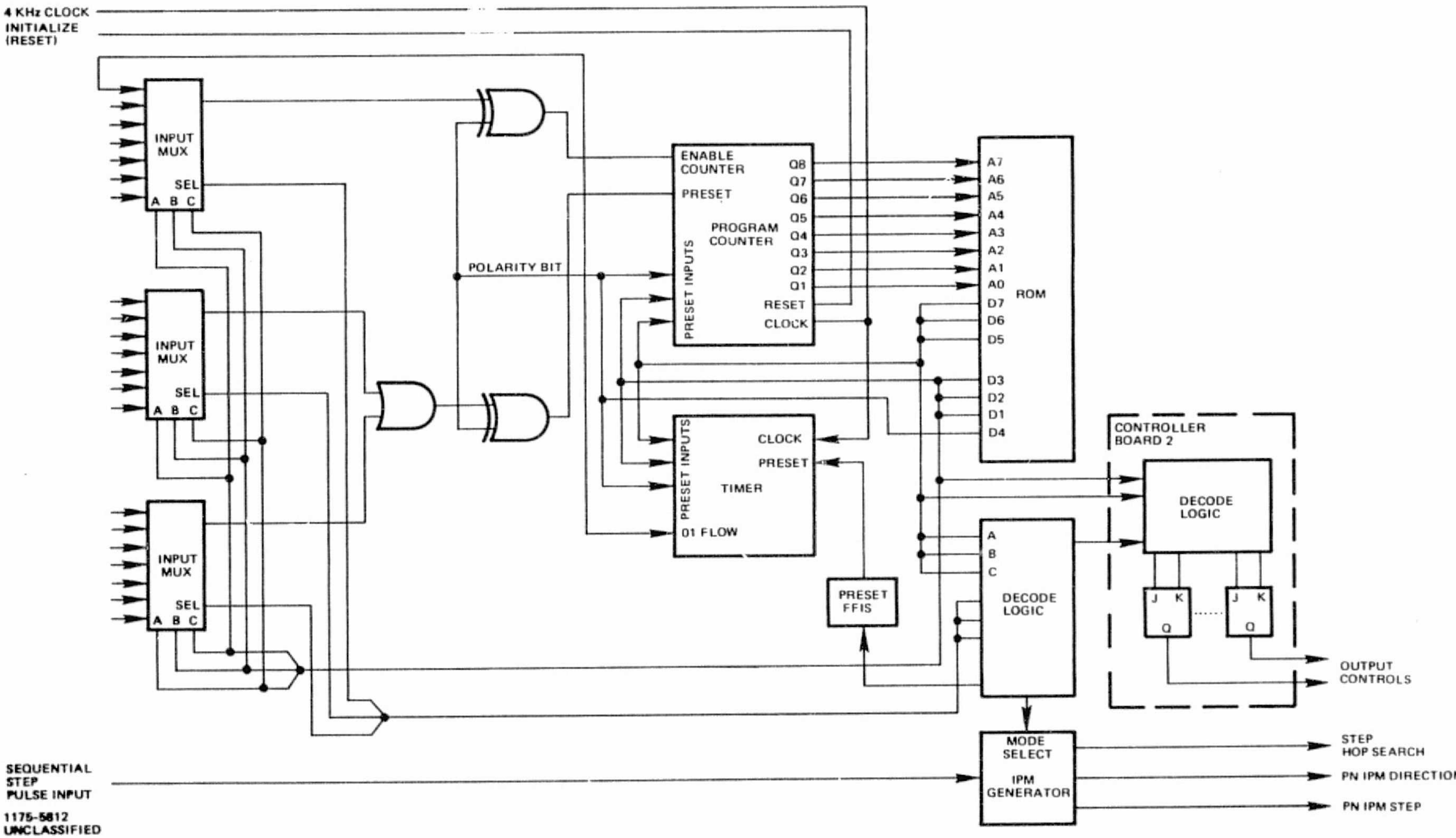

Figure 3-13. Controller Block Diagram

TDRS CONTROLLER BOARD I
ROM INSTRUCTION SET

	HEX	ROM OUTPUT $D_8\ D_7\ D_6\ D_5\ D_4\ D_3\ D_2\ D_1$	COMMENT
OUTPUTS (NOTE 1)	00	0 0 0 0 0 0 0 0	ADVANCE PROGRAM
	01	0 0 0 0 0 0 0 1	DISABLE φ SYNC DISPLAY (1)
	02	0 0 0 0 0 0 1 0	ENABLE φ SYNC DISPLAY (0)
	03	0 0 0 0 0 0 1 1	DISABLE SEARCH DISPLAY (1)
	04	0 0 0 0 0 1 0 0	ENABLE SEARCH DISPLAY (0)
	05	0 0 0 0 0 1 0 1	DISABLE SQPN DISPLAY (1)
	06	0 0 0 0 0 1 1 0	ENABLE SQPN DISPLAY (0)
	40	0 1 0 0 0 0 0 0	SET TIMER WITH NEXT 2 ROM OUTPUTS
	41	0 1 0 0 0 0 0 1	ENABLE PN SHORT SEARCH (±64 CHIPS)
	42	0 1 0 0 0 0 1 0	ENABLE PN LONG SEARCH (±224 CHIPS)
	43	0 1 0 0 0 0 1 1	ENABLE PN SEARCH (UNIDIRECTIONAL)
	44	0 1 0 0 0 1 0 0	ENABLE HOP SEARCH
	45	0 1 0 0 0 1 0 1	STOP SEARCH
	60	0 1 1 0 0 0 0 0	DISABLE HOP DISPLAY (FH/PN, HOP ACQ) (1)
	61	0 1 1 0 0 0 0 1	ENABLE HOP DISPLAY (0)
	62	0 1 1 0 0 0 1 0	DISABLE LOAD AFC (0)
	63	0 1 1 0 0 0 1 1	ENABLE LOAD AFC (1)
	64	0 1 1 0 0 1 0 0	DISABLE AFC (0)
	65	0 1 1 0 0 1 0 1	ENABLE AFC (1)
	66	0 1 1 0 0 1 1 0	FORCE SINGLE DATA (1)
	67	0 1 1 0 0 1 1 1	DISABLE SINGLE DATA (0)
	70	0 1 1 1 0 0 0 0	DUMP CARRIER LOOP FILTER (1)
	71	0 1 1 1 0 0 0 1	ENABLE CARRIER LOOP FILTER (0)
	72	0 1 1 1 0 0 1 0	DUMP HOP LOOP FILTER (1)
	73	0 1 1 1 0 0 1 1	ENABLE HOP LOOP FILTER (0)
	74	0 1 1 1 0 1 0 0	DUMP CODE LOOP FILTER (1)
	75	0 1 1 1 0 1 0 1	ENABLE CODE LOOP FILTER (0)
JUMPS (NOTES 1,2,3)	10	0 0 0 1 0 0 0 0	LET TIMER ELAPSE (PROGRAM WAITS)
	19	0 0 0 1 1 0 0 1	WAIT IF "TEST" (0)
	28	0 0 1 0 1 0 0 0	JUMP IF TIMER ELAPSED (0)
	20	0 0 1 0 0 0 0 0	JUMP IF TIMER NOT ELAPSED (1)
	21	0 0 1 0 0 0 0 1	JUMP IF NOT MMT (MTAR) (1)
	2A	0 0 1 0 1 0 1 0	JUMP IF TEST SWITCH 1 (0)
	2B	0 0 1 0 1 0 1 1	JUMP IF PSK (0)
	24	0 0 1 0 0 1 0 0	JUMP IF NOT RETURN ONLY (1)
	25	0 0 1 0 0 1 0 1	JUMP IF NOT SINGLE DATA (1)
	30	0 0 1 1 0 0 0 0	JUMP IF SEQ DETECTOR SYNC (1)
	31	0 0 1 1 0 0 0 1	JUMP IF φ SYNC (1)
	3A	0 0 1 1 1 0 1 0	JUMP IF DOPPLER NOT CORRECTED (0)
	3B	0 0 1 1 1 0 1 1	UNCONDITIONAL JUMP (0)

NOTES:

1. LOGIC 0 0.0VDC TO +0.8VDC
   LOGIC 1 ≥ +2.0VDC
2. ALL JUMP INSTRUCTIONS EXCEPT "LET" OR "WAIT" USE THE NEXT ROM ADDRESS FOR THE JUMP ADDRESS.
3. ALL JUMP INSTRUCTIONS USE ROM OUTPUT D_4 TO DETERMINE IF THE JUMP WILL BE PERFORMED. IF D_4 IS LOGIC 0, THE INPUT CONDITION MUST BE LOGIC 1 AND VICE VERSA.
4. ROM ADDRESSES NOT LISTED CONTAIN A 00000000 PATTERN. WHEN ROM IS ERASED WITH ULTRAVIOLET LIGHT, ALL ADDRESSES CONTAIN A 00000000 PATTERN.
5. WHEN THE 16-BIT TIMER IS ADDRESSED, IT TAKES TWO ADDITIONAL PROGRAM INSTRUCTIONS TO FIRST LOAD IN THE 8 LEAST SIGNIFICANT BITS AND THEN THE 8 MOST SIGNIFICANT BITS. THE TIMER STARTS COUNTING FROM THE NUMBER LOADED IN UNTIL THE COUNTER CONTAINS ALL 1'S AND THEN STOPS. THE MAXIMUM TIME DURATION OF THE COUNTER IS APPROXIMATELY 16.4 SEC. IT IS CONVENIENT TO APPROXIMATE COUNTING FROM 1 TO 16 SEC BY PROGRAMMING THE 4 MSB'S (16 COMBINATIONS) WITH 1'S & 0'S AND ALL OTHER BITS WITH 0'S

TDRS

	ROM ADDRESS $A_7\ A_6\ A_5\ A_4\ A_3\ A_2\ A_1\ A_0$	CCTA
INITIAL CONDITIONS	0 0 0 0 0 0 0 0	000
	0 0 0 0 0 0 0 1	001
	0 0 0 0 0 0 1 0	002
	0 0 0 0 0 0 1 1	003
	0 0 0 0 0 1 0 0	004
	0 0 0 0 0 1 0 1	005
	0 0 0 0 0 1 1 0	006
	0 0 0 0 0 1 1 1	007
	0 0 0 0 1 0 0 0	010
	0 0 0 0 1 0 0 1	011
	0 0 0 0 1 0 1 0	012
	0 0 0 0 1 0 1 1	013
	0 0 0 0 1 1 0 0	014
	0 0 0 0 1 1 0 1	015
	0 0 0 0 1 1 1 0	016
	0 0 0 0 1 1 1 1	017
	0 0 0 1 0 0 0 0	020
	0 0 0 1 0 0 0 1	021
	0 0 0 1 0 0 1 0	022
	0 0 0 1 0 0 1 1	023
	0 0 0 1 0 1 0 0	024
	0 0 0 1 0 1 0 1	025
	0 0 0 1 0 1 1 0	026
	0 0 0 1 0 1 1 1	027
	0 0 0 1 1 0 0 0	030
	0 0 0 1 1 0 0 1	031
	0 0 0 1 1 0 1 0	032
	0 0 0 1 1 0 1 1	033
	0 0 0 1 1 1 0 0	034
	0 0 0 1 1 1 0 1	035
	0 0 0 1 1 1 1 0	036
HOP SEARCH	0 0 0 1 1 1 1 1	037

5. CONTINUED
SUBTRACT THE TIME DESIRED IN SECONDS
CONVERT THIS NUMBER TO BINARY FOR THE

EXAMPLE: ALLOW TIMER TO ELAPSE
16−5=11 → 1011

ROM ADDRES	OUTPUT	COMMEN
XXXXXX00	01000000	SET TIM
XXXXXX01	00000000	TIMER
XXXXXX10	10110000	TIMER

FOLDOUT FRAME /

TDRS CONTROLLER BOARD I
ROM PROGRAM

	ROM ADDRESS		ROM OUTPUT		
	A_7 A_6 A_5 A_4 A_3 A_2 A_1 A_0	OCTAL	OCTAL	HEX	D_8 D_7 D_6 D_5 D_4 D_3 D_2 D_1	COMMENT
IAL ITIONS	0 0 0 0 0 0 0 0	000	000	00	0 0 0 0 0 0 0 0	ADVANCE
	0 0 0 0 0 0 0 1	001	001	01	0 0 0 0 0 0 0 1	DISABLE φ SYNC DISPLAY
	0 0 0 0 0 0 1 0	002	003	03	0 0 0 0 0 0 1 1	DISABLE SEARCH DISPLAY
	0 0 0 0 0 0 1 1	003	005	05	0 0 0 0 0 1 0 1	DISABLE SQPN DISPLAY
	0 0 0 0 0 1 0 0	004	105	45	0 1 0 0 0 1 0 1	STOP SEARCH
	0 0 0 0 0 1 0 1	005	140	60	0 1 1 0 0 0 0 0	DISABLE HOP DISPLAY
	0 0 0 0 0 1 1 0	006	144	64	0 1 1 0 0 1 0 0	DISABLE AFC
	0 0 0 0 0 1 1 1	007	142	62	0 1 1 0 0 0 1 0	DISABLE LOAD AFC
	0 0 0 0 1 0 0 0	010	143	63	0 1 1 0 0 0 1 1	ENABLE LOAD AFC
	0 0 0 0 1 0 0 1	011	142	62	0 1 1 0 0 0 1 0	DISABLE LOAD AFC
	0 0 0 0 1 0 1 0	012	146	66	0 1 1 0 0 1 1 0	FORCE SINGLE DATA
	0 0 0 0 1 0 1 1	013	160	70	0 1 1 1 0 0 0 0	DUMP CARRIER LOOP FILTER
	0 0 0 0 1 1 0 0	014	162	72	0 1 1 1 0 0 1 0	DUMP HOP LOOP FILTER
	0 0 0 0 1 1 0 1	015	164	74	0 1 1 1 0 1 0 0	DUMP CODE LOOP FILTER
	0 0 0 0 1 1 1 0	016	000	00	0 0 0 0 0 0 0 0	ADVANCE
	0 0 0 0 1 1 1 1	017	004	04	0 0 0 0 0 1 0 0	ENABLE SEARCH DISPLAY
	0 0 0 1 0 0 0 0	020	053	2B	0 0 1 0 1 0 1 1	JUMP IF PSK
	0 0 0 1 0 0 0 1	021	131	59	0 1 0 1 0 0 0 1	JUMP ADDRESS
	0 0 0 1 0 0 1 0	022	073	3B	0 0 1 1 1 0 1 1	UNCOND JUMP
	0 0 0 1 0 0 1 1	023	035	1D	0 0 0 1 1 1 0 1	JUMP ADDRESS
	0 0 0 1 0 1 0 0	024	000	00	0 0 0 0 0 0 0 0	ADVANCE
	0 0 0 1 0 1 0 1	025	000	00	↑	↑
	0 0 0 1 0 1 1 0	026	000	00		
	0 0 0 1 0 1 1 1	027	000	00		
	0 0 0 1 1 0 0 0	030	000	00		
	0 0 0 1 1 0 0 1	031	000	00		
	0 0 0 1 1 0 1 0	032	000	00		
	0 0 0 1 1 0 1 1	033	000	00	↓	↓
	0 0 0 1 1 1 0 0	034	000	00	0 0 0 0 0 0 0 0	ADVANCE
	0 0 0 1 1 1 0 1	035	041	21	0 0 1 0 0 0 0 1	JUMP IF NOT MMT
	0 0 0 1 1 1 1 0	036	073	3B	0 0 1 1 1 0 1 1	JUMP ADDRESS
OP EARCH	0 0 0 1 1 1 1 1	037	104	44	0 1 0 0 0 1 0 0	ENABLE HOP SEARCH

CONTINUED
SUBTRACT THE TIME DESIRED IN SECONDS FROM 16 AND CONVERT THIS NUMBER TO BINARY FOR THE FOUR MSB'S.

EXAMPLE: ALLOW TIMER TO ELAPSE 5 SEC.
16-5=11 → 1011

ROM ADDRES	OUTPUT	COMMENT
XXXXXX00	01000000	SET TIMER T=5SEC
XXXXXX01	00000000	TIMER LSB'S
XXXXXX10	10110000	TIMER MSB'S

Figure 3-14. Controller Program
(Sheet 1 of 4)

ROM PROGRAM CONTINUED

	ROM ADDRESS $A_7\ A_6\ A_5\ A_4\ A_3\ A_2\ A_1\ A_0$	OCTAL	HEX	ROM OUTPUT $D_8\ D_7\ D_6\ D_5\ D_4\ D_3\ D_2\ D_1$	COMMENT	
HOP SEARCH	0 0 1 0 0 0 0 0	040	141	61	0 1 1 0 0 0 0 1	ENABLE HOP DISPLAY	
	0 0 1 0 0 0 0 1	041	140	40	0 1 0 0 0 0 0 0	SET TIMER T= 7SEC	
	0 0 1 0 0 0 1 0	042	000	00	0 0 0 0 0 0 0 0	TIMER LSB'S	HOP TRACK
	0 0 1 0 0 0 1 1	043	220	90	1 0 0 1 0 0 0 0	TIMER MSB'S	
	0 0 1 0 0 1 0 0	044	073	3B	0 0 1 1 1 0 1 1	UNCOND JUMP	
	0 0 1 0 0 1 0 1	045	050	28	0 0 1 0 1 0 0 0	JUMP ADDRESS	
	0 0 1 0 0 1 1 0	046	000	00	0 0 0 0 0 0 0 0	ADVANCE	
	0 0 1 0 0 1 1 1	047	000	00	0 0 0 0 0 0 0 0	ADVANCE	
	0 0 1 0 1 0 0 0	050	060	30	0 0 1 1 0 0 0 0	JMP IF SEQ DET SYNC	
	0 0 1 0 1 0 0 1	051	117	4F	0 1 0 0 1 1 1 1	JMP ADDR	FREQUENCY CORRECTION & 1/2 PSK
	0 0 1 0 1 0 1 0	052	052	2A	0 0 1 0 1 0 1 0	JMP IF TEST SW 1	
	0 0 1 0 1 0 1 1	053	050	28	0 0 1 0 1 0 0 0	JMP ADDR	
	0 0 1 0 1 1 0 0	054	050	28	0 0 1 0 1 0 0 0	JMP IF TIMER ELAPSED	
	0 0 1 0 1 1 0 1	055	000	00	0 0 0 0 0 0 0 0	JMP ADDR	
	0 0 1 0 1 1 1 0	056	073	3B	0 0 1 1 1 0 1 1	UNCOND JMP	
	0 0 1 0 1 1 1 1	057	050	28	0 0 1 0 1 0 0 0	JMP ADDR	
	0 0 1 1 0 0 0 0	060	000	00	0 0 0 0 0 0 0 0	ADVANCE	
	0 0 1 1 0 0 0 1	061	000	00			
	0 0 1 1 0 0 1 0	062	000	00			
	0 0 1 1 0 0 1 1	063	000	00			
	0 0 1 1 0 1 0 0	064	000	00			
	0 0 1 1 0 1 0 1	065	000	00			
	0 0 1 1 0 1 1 0	066	000	00			
	0 0 1 1 0 1 1 1	067	000	00			
	0 0 1 1 1 0 0 0	070	000	00			PN SHORT SEARCH
	0 0 1 1 1 0 0 1	071	000	00			
	0 0 1 1 1 0 1 0	072	000	00	0 0 0 0 0 0 0 0	ADVANCE	
MTAR PN SEARCH	0 0 1 1 1 0 1 1	073	006	06	0 0 0 0 0 1 1 0	ENABLE SQPN DISPLAY	
	0 0 1 1 1 1 0 0	074	044	24	0 0 1 0 0 1 0 0	JMP IF NOT RETURN ONLY	
	0 0 1 1 1 1 0 1	075	101	41	0 1 0 0 0 0 0 1	JMP ADDR	
	0 0 1 1 1 1 1 0	076	103	43	0 1 0 0 0 0 1 1	EN PN SEARCH	
	0 0 1 1 1 1 1 1	077	073	3B	0 0 1 1 1 0 1 1	UNCOND JMP	
	0 1 0 0 0 0 0 0	100	102	42	0 1 0 0 0 0 1 0	JMP ADDR	
	0 1 0 0 0 0 0 1	101	102	42	0 1 0 0 0 0 1 0	ENABLE PN LONG SEARCH	
	0 1 0 0 0 0 1 0	102	100	40	0 1 0 0 0 0 0 0	SET TIMER T= 16 SEC	
	0 1 0 0 0 0 1 1	103	000	00	0 0 0 0 0 0 0 0	T LSB'S	
	0 1 0 0 0 1 0 0	104	000	00	0 0 0 0 0 0 0 0	T MSB'S	
	0 1 0 0 0 1 0 1	105	073	3B	0 0 1 1 1 0 1 1	UNCOND JMP	
	0 1 0 0 0 1 1 0	106	050	28	0 0 1 0 1 0 0 0	JMP ADDR	
	0 1 0 0 0 1 1 1	107	000	00	0 0 0 0 0 0 0 0	ADVANCE	
	0 1 0 0 1 0 0 0	110	000	00			
	0 1 0 0 1 0 0 1	111	000	00			CODE & CARRIER LOOP ACQ & TRACK & 1/2 PSK
	0 1 0 0 1 0 1 0	112	000	00			
	0 1 0 0 1 0 1 1	113	000	00			
	0 1 0 0 1 1 0 0	114	000	00			
	0 1 0 0 1 1 0 1	115	000	00			
	0 1 0 0 1 1 1 0	116	000	00	0 0 0 0 0 0 0 0	ADVANCE	
	0 1 0 0 1 1 1 1	117	105	45	0 1 0 0 0 1 0 1	STOP SEARCH	

ROGRAM CONTINUED

	ROM ADDRESS $A_7\ A_6\ A_5\ A_4\ A_3\ A_2\ A_1\ A_0$	OCTAL	ROM OUTPUT OCTAL	HEX	$D_8\ D_7\ D_6\ D_5\ D_4\ D_3\ D_2\ D_1$	COMMENT
	0 1 0 1 0 0 0 0	120	041	21	0 0 1 0 0 0 0 1	JMP IF NOT MMT
	0 1 0 1 0 0 0 1	121	233	9B	1 0 0 1 1 0 1 1	JMP ADDR
HOP TRACK	0 1 0 1 0 0 1 0	122	163	73	0 1 1 1 0 0 1 1	EN HOP LOOP FILTER
	0 1 0 1 0 0 1 1	123	100	40	0 1 0 0 0 0 0 0	SET TIMER T=5 SEC
	0 1 0 1 0 1 0 0	124	000	00	0 0 0 0 0 0 0 0	T LSB'S
	0 1 0 1 0 1 0 1	125	260	B0	1 0 1 1 0 0 0 0	T MSB'S
	0 1 0 1 0 1 1 0	126	020	10	0 0 0 1 0 0 0 0	LET TIMER ELAPSE
	0 1 0 1 0 1 1 1	127	052	2A	0 0 1 0 1 0 1 0	JMP IF TEST SW 1
	0 1 0 1 1 0 0 0	130	127	57	0 1 0 1 0 1 1 1	JMP IF ADDR
FREQUENCY CORRECTION	0 1 0 1 1 0 0 1	131	145	65	0 1 1 0 0 1 0 1	ENABLE AFC
&	0 1 0 1 1 0 1 0	132	100	40	0 1 0 0 0 0 0 0	SET TIMER T=4 SEC
½ PSK	0 1 0 1 1 0 1 1	133	000	00	0 0 0 0 0 0 0 0	T LSB'S
	0 1 0 1 1 1 0 0	134	300	C0	1 1 0 0 0 0 0 0	T MSB'S
	0 1 0 1 1 1 0 1	135	050	28	0 0 1 0 1 0 0 0	JMP IF TIMER ELAPSED
	0 1 0 1 1 1 1 0	136	000	00	0 0 0 0 0 0 0 0	JMP ADDR
	0 1 0 1 1 1 1 1	137	072	3A	0 0 1 1 1 0 1 0	JMP IF DOPPLER NOT CORRECTED
	0 1 1 0 0 0 0 0	140	135	5D	0 1 0 1 1 1 0 1	JMP ADDR
	0 1 1 0 0 0 0 1	141	031	19	0 0 0 1 1 0 0 1	WAIT IF TEST
	0 1 1 0 0 0 1 0	142	140	60	0 1 1 0 0 0 0 0	DISABLE HOP DISPLAY
	0 1 1 0 0 0 1 1	143	162	72	0 1 1 1 0 0 1 0	DUMP HOP LOOP FILTER
	0 1 1 0 0 1 0 0	144	144	64	0 1 1 0 0 1 0 0	DISABLE AFC
	0 1 1 0 0 1 0 1	145	073	3B	0 0 1 1 1 0 1 1	UNCOND JMP
	0 1 1 0 0 1 1 0	146	260	B0	1 0 1 1 0 0 0 0	JMP ADDR
	0 1 1 0 0 1 1 1	147	006	06	0 0 0 0 0 1 1 0	EN SQPN DISPLAY
PN SHORT SEARCH	0 1 1 0 1 0 0 0	150	100	40	0 1 0 0 0 0 0 0	SET TIMER T=15 SEC
	0 1 1 0 1 0 0 1	151	000	00	0 0 0 0 0 0 0 0	T LSB'S
	0 1 1 0 1 0 1 0	152	001	01	0 0 0 0 0 0 0 1	T MSB'S
	0 1 1 0 1 0 1 1	153	101	41	0 1 0 0 0 0 0 1	EN PN SHORT SEARCH
	0 1 1 0 1 1 0 0	154	060	30	0 0 1 1 0 0 0 0	JMP IF SEQ DET SYNC
	0 1 1 0 1 1 0 1	155	242	A2	1 0 1 0 0 0 1 0	JMP ADDR
	0 1 1 0 1 1 1 0	156	052	2A	0 0 1 0 1 0 1 0	JMP IF TEST SW 1
	0 1 1 0 1 1 1 1	157	154	6C	0 1 1 0 1 1 0 0	JMP ADDR
	0 1 1 1 0 0 0 0	160	050	28	0 0 1 0 1 0 0 0	JMP IF TIMER ELAPSED
	0 1 1 1 0 0 0 1	161	000	00	0 0 0 0 0 0 0 0	JMP ADDR
	0 1 1 1 0 0 1 0	162	073	3B	0 0 1 1 1 0 1 1	UNCOND JMP
	0 1 1 1 0 0 1 1	163	154	6C	0 1 1 0 1 1 0 0	JMP ADDR
	0 1 1 1 0 1 0 0	164	000	00	0 0 0 0 0 0 0 0	ADVANCE
	0 1 1 1 0 1 0 1	165	000	00	0 0 0 0 0 0 0 0	ADVANCE
	0 1 1 1 0 1 1 0	166	000	00	0 0 0 0 0 0 0 0	ADVANCE
	0 1 1 1 0 1 1 1	167	000	00	0 0 0 0 0 0 0 0	ADVANCE
	0 1 1 1 1 0 0 0	170	000	00	0 0 0 0 0 0 0 0	ADVANCE
CODE & CARRIER	0 1 1 1 1 0 0 1	171	000	00	0 0 0 0 0 0 0 0	ADVANCE
LOOP ACQ & TRACK	0 1 1 1 1 0 1 0	172	161	71	0 1 1 1 0 0 0 1	EN CARRIER LOOP FILTER
& ½ PSK	0 1 1 1 1 0 1 1	173	100	40	0 1 0 0 0 0 0 0	SET TIMER T=3 SEC
	0 1 1 1 1 1 0 0	174	000	00	0 0 0 0 0 0 0 0	T LSB'S
	0 1 1 1 1 1 0 1	175	320	D0	1 1 0 1 0 0 0 0	T MSB'S
	0 1 1 1 1 1 1 0	176	061	31	0 0 1 1 0 0 0 1	JMP IF φ SYNC
	0 1 1 1 1 1 1 1	177	211	89	1 0 0 0 1 0 0 1	JMP ADDR

Figure 3-14. Controller Program (Sheet 2 of 4)

ROM PROGRAM CONTINUED

ROM ADDRESS $A_7 A_6 A_5 A_4 A_3 A_2 A_1 A_0$	ROM OUTPUT OCTAL		HEX	$D_8 D_7 D_6 D_5 D_4 D_3 D_2 D_1$	COMMENT
1 0 0 0 0 0 0 0	200	146	66	0 1 1 0 0 1 1 0	FORCE SINGLE DATA
1 0 0 0 0 0 0 1	201	001	01	0 0 0 0 0 0 0 1	DISABLE Φ SYNC DISPLAY
1 0 0 0 0 0 1 0	202	004	04	0 0 0 0 0 1 0 0	ENABLE SEARCH DISPLAY
1 0 0 0 0 0 1 1	203	052	2A	0 0 1 0 1 0 1 0	JMP IF TEST SW 1
1 0 0 0 0 1 0 0	204	176	7E	0 1 1 1 1 1 1 0	JMP ADDR
1 0 0 0 0 1 0 1	205	050	28	0 0 1 0 1 0 0 0	JMP IF TIMER ELAPSED
1 0 0 0 0 1 1 0	206	216	8E	1 0 0 0 1 1 1 0	JMP ADDR
1 0 0 0 0 1 1 1	207	073	3B	0 0 1 1 1 0 1 1	UNCOND JMP
1 0 0 0 1 0 0 0	210	176	7E	0 1 1 1 1 1 1 0	JMP ADDR
1 0 0 0 1 0 0 1	211	147	67	0 1 1 0 0 1 1 1	DISABLE SINGLE DATA
1 0 0 0 1 0 1 0	212	003	03	0 0 0 0 0 0 1 1	DISABLE SEARCH DISPLAY
1 0 0 0 1 0 1 1	213	002	02	0 0 0 0 0 0 1 0	EN Φ SYNC DISPLAY
1 0 0 0 1 1 0 0	214	073	3B	0 0 1 1 1 0 1 1	UNCOND JMP
1 0 0 0 1 1 0 1	215	173	7B	0 1 1 1 1 0 1 1	JMP ADDR
1 0 0 0 1 1 1 0	216	053	2B	0 0 1 0 1 0 1 1	JMP IF PSK
1 0 0 0 1 1 1 1	217	000	00	0 0 0 0 0 0 0 0	JMP ADDR
1 0 0 1 0 0 0 0	220	164	74	0 1 1 1 0 1 0 0	DUMP CODE LOOP FILTER
1 0 0 1 0 0 0 1	221	160	70	0 1 1 1 0 0 0 0	DUMP CARRIER LOOP FILTER
1 0 0 1 0 0 1 0	222	100	40	0 1 0 0 0 0 0 0	SET TIMER T=3 SEC
1 0 0 1 0 0 1 1	223	000	00	0 0 0 0 0 0 0 0	T LSB'S
1 0 0 1 0 1 0 0	224	320	D0	1 1 0 1 0 0 0 0	T MSB'S
1 0 0 1 0 1 0 1	225	020	10	0 0 0 1 0 0 0 0	LET TIMER ELAPSE
1 0 0 1 0 1 1 0	226	100	40	0 1 0 0 0 0 0 0	SET TIMER T=5 SEC
1 0 0 1 0 1 1 1	227	000	00	0 0 0 0 0 0 0 0	T LSB'S
1 0 0 1 1 0 0 0	230	260	B0	1 0 1 1 0 0 0 0	T MSB'S
1 0 0 1 1 0 0 1	231	073	3B	0 0 1 1 1 0 1 1	UNCOND JMP
1 0 0 1 1 0 1 0	232	153	6B	0 1 1 0 1 0 1 1	JMP ADDR
1 0 0 1 1 0 1 1	233	165	75	0 1 1 1 0 1 0 1	EN CODE LOOP FILTER
1 0 0 1 1 1 0 0	234	073	3B	0 0 1 1 1 0 1 1	UNCOND JMP
1 0 0 1 1 1 0 1	235	131	59	0 1 0 1 1 0 0 1	JMP ADDR
1 0 0 1 1 1 1 0	236	000	00	0 0 0 0 0 0 0 0	ADVANCE
1 0 0 1 1 1 1 1	237	000	00	0 0 0 0 0 0 0 0	ADVANCE
1 0 1 0 0 0 0 0	240	073	3B	0 0 1 1 1 0 1 1	UNCOND JMP
1 0 1 0 0 0 0 1	241	000	00	0 0 0 0 0 0 0 0	JMP ADDR
1 0 1 0 0 0 1 0	242	105	45	0 1 0 0 0 1 0 1	STOP SEARCH
1 0 1 0 0 0 1 1	243	165	75	0 1 1 1 0 1 0 1	EN CODE LOOP FILTER
1 0 1 0 0 1 0 0	244	145	65	0 1 1 0 0 1 0 1	ENABLE AFC
1 0 1 0 0 1 0 1	245	100	40	0 1 0 0 0 0 0 0	SET TIMER T=4 SEC
1 0 1 0 0 1 1 0	246	000	00	0 0 0 0 0 0 0 0	T LSB'S
1 0 1 0 0 1 1 1	247	300	C0	1 1 0 0 0 0 0 0	T MSB'S
1 0 1 0 1 0 0 0	250	050	28	0 0 1 0 1 0 0 0	JMP IF TIMER ELAPSED
1 0 1 0 1 0 0 1	251	000	00	0 0 0 0 0 0 0 0	JMP ADDR
1 0 1 0 1 0 1 0	252	072	3A	0 0 1 1 1 0 1 0	JMP IF DOPPLER NOT CORRECTED
1 0 1 0 1 0 1 1	253	250	A8	1 0 1 0 1 0 0 0	JMP ADDR
1 0 1 0 1 1 0 0	254	144	64	0 1 1 0 0 1 0 0	DISABLE AFC
1 0 1 0 1 1 0 1	255	073	3B	0 0 1 1 1 0 1 1	UNCOND JMP
1 0 1 0 1 1 1 0	256	172	7A	0 1 1 1 1 0 1 0	JMP ADDR
1 0 1 0 1 1 1 1	257	000	00	0 0 0 0 0 0 0 0	ADVANCE

ATA
C DISPLAY
DISPLAY
D 1

ELAPSED

DATA
DISPLAY
PLAY

P FILTER
OOP FILTER
= 3 SEC

ELAPSE
= 5 SEC

FILTER

P FILTER
C
T = 4 SEC

E ELAPSED

LER NOT CORRECTED

	ROM ADDRESS	ROM OUTPUT				
	A A A A A A A A	OCTAL		HEX	D D D D D D D D	COMMENT
	1 0 1 1 0 0 0 0	260	053	2B	0 0 1 0 1 0 1 1	JMP IF PSK
	1 0 1 1 0 0 0 1	261	172	7A	0 1 1 1 1 0 1 0	JMP ADDR
	1 0 1 1 0 0 1 0	262	041	21	0 0 1 0 0 0 0 1	JMP IF NOT MMT
	1 0 1 1 0 0 1 1	263	172	7A	0 1 1 1 1 0 1 0	JMP ADDR
	1 0 1 1 0 1 0 0	264	073	3B	0 0 1 1 1 0 1 1	UNCOND JMP
	1 0 1 1 0 1 0 1	265	147	67	0 1 1 0 0 1 1 1	JMP ADDR
(NOTE 4)	1 1 0 0 0 0 0 0	300	073	3B	0 0 1 1 1 0 1 1	UNCOND JMP
	1 1 0 0 0 0 0 1	301	000	00	0 0 0 0 0 0 0 0	JMP ADDR
	1 1 1 0 0 0 0 0	340	073	3B	0 0 1 1 1 0 1 1	UNCOND JMP
	1 1 1 0 0 0 0 1	341	000	00	0 0 0 0 0 0 0 0	JMP ADDR

Figure 3-14. Controller Program (Sheet 3 of 4)

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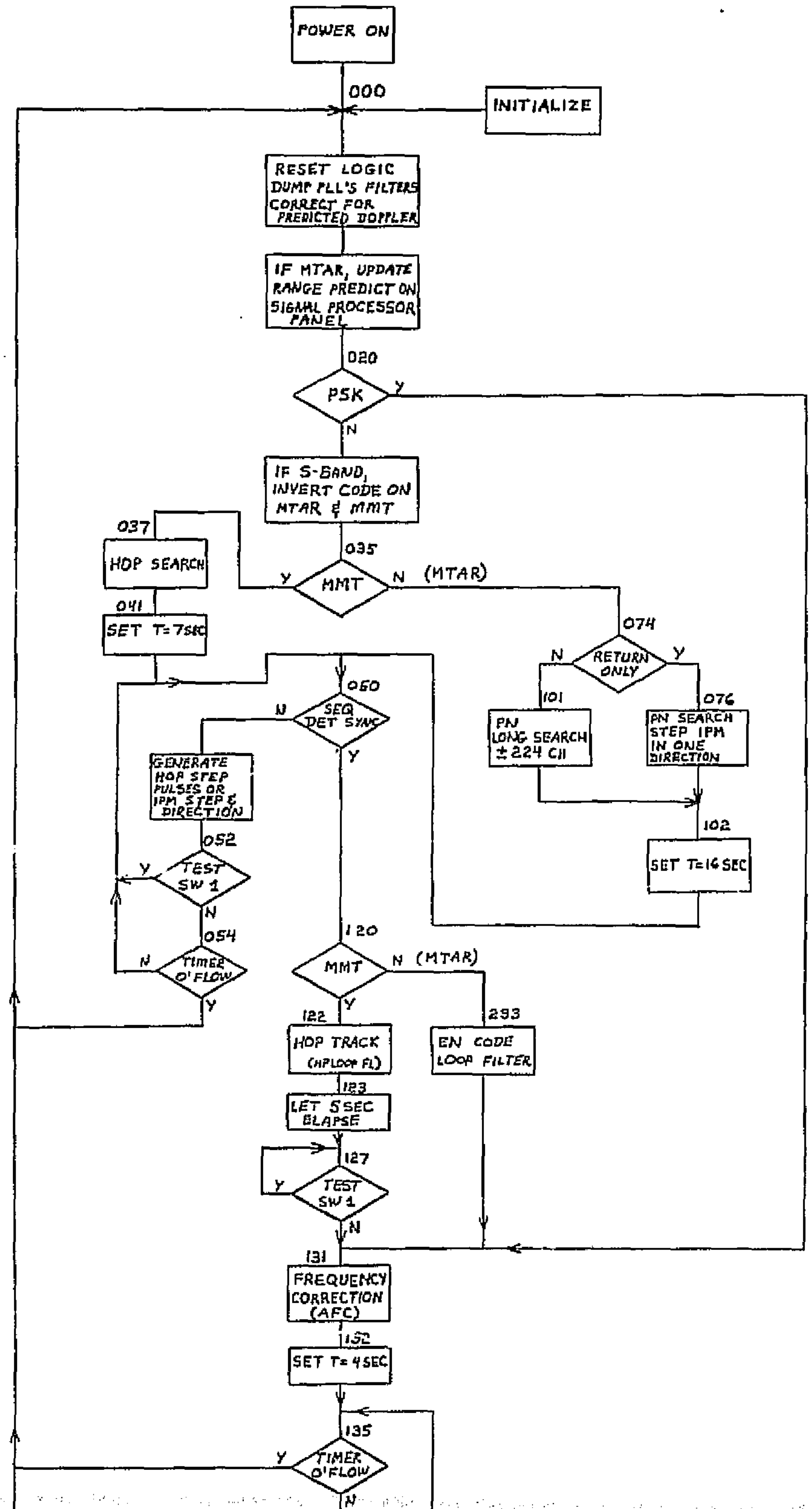

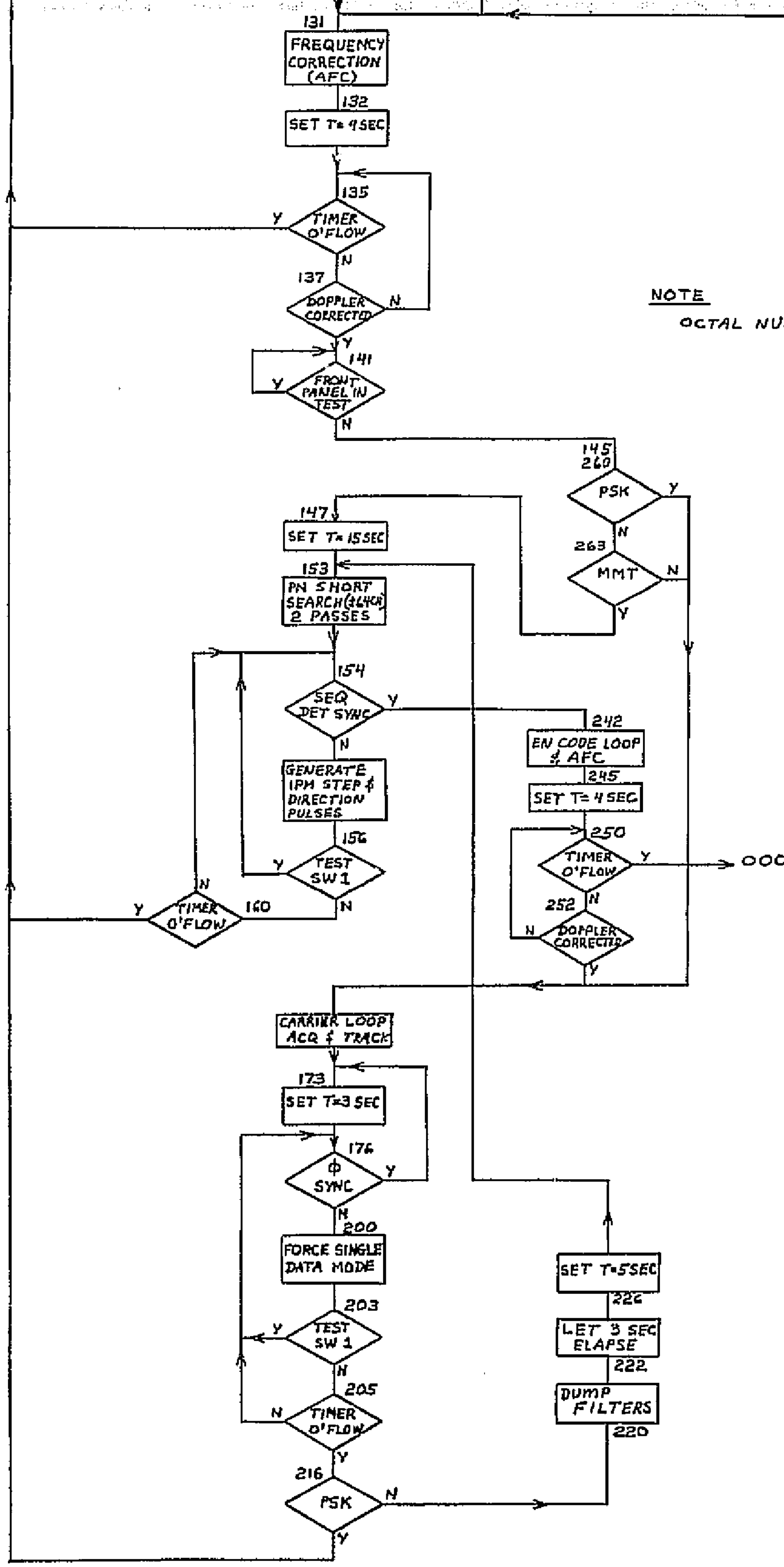

NOTE

OCTAL NUMBERS INDICATE PROGRAM COUNTER LOCATION

Figure 3-14. Controller Program (Sheet 4 of 4)

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the above items is addressed at any instant by the decoder logic based on the ROM output. The timer and IPM signal generator can run independently while the input multiplexers are being addressed to determine jump conditions or control outputs are being enabled on Controller Board 2.

Various input signals can be checked by the input multiplexers U80A, U80C, and U80E to determine if a logic 0 or 1 is present based on the sign bit D4 output from the ROM and the exclusive OR comparators of U73E. Based on the outputs of the exclusive OR's U73E-1 and U73E-2, the program counter U1G and U9G can be stopped until the input condition changes or the contents of the program counter can be changed to agree with the counter preset inputs from the ROM. This corresponds to the program jumping to a new location in the program.

The timer is a 16-bit counter consisting of U1J, U9J, U17J and U25J, flip-flop U33J and several gates that is first addressed by one ROM instruction and then preset with the next two 8-bit ROM instructions. It then begins counting to an all 1's condition at which time it stops. The maximum time the counter can elapse is approximately 16.6 seconds. While the counter is running other inputs can be monitored to see if a jump instruction is to be performed, control outputs can be enabled, and the timer itself can be checked to see if it has elapsed.

The IPM (incremental phase modulator) generator consists of programmable counter U41E, U49E and U49G, IPM direction counter U57E and various gates, and mode select flip-flops U56J and U64J and various gates. The counter is clocked by sequential step pulses from the Sequential Filter Board.

There are four different search modes that the IPM generator can be selected by the ROM output to perform: PN short search, PN long search, PN one-way search, and frequency hop search. Whenever PN short or long search are requested U56J-1 or -2 are set and flip-flops U35G-1 and -2 allow a 2 clock delay while counter U41E, U49E and U49G are preset. For PN short search, the counter increments 256 1/4-chips or 64 chips while 256 step pulses are outputted, then the IPM direction counter U57E changes polarity from logic 1 to 0. The counter then generates 512 step pulses and then the direction line again changes polarity to logic 0 and continues to change polarity after each 512 step pulses.

For PN long search, 896 1/4-chip step pulses are generated (224 chips) and then the direction counter changes polarity from logic 1 to logic 0 and then changes polarity after each 1792 step pulses.

For PN one way frequency hop searches only step pulses are gated out. The IPM direction line doesn't change polarity.

3.2.2.3.2 Controller Board 2

The controller board receives inputs from the ROM of Controller Board 1 and decodes the signals through decoder IC's U50E, U50A, U57C, U50G, and U42J to enable and disable various JK flip-flops and thereby generates or disables various control signals.

The timer is used on the MTAR for transmitting the frequency hop signal for 15 seconds during initial forward link acquisition by the MMT.

3.2.3 CONTROL PANEL

The MMT control panel contains the mode selector switches and indicator lamps for the MMT equipment. The MMT control panel is pictured in figure 3-15.

The control functions are listed below:

MMT CONTROL:

LINK MODE	- COHERENT (transpond) NONCOHERENT (transpond) RETURN ONLY
MODULATION MODE	- PSK SQPN (Receiver searches in hop until hop acquisition; then switches to SQPN) TEST (HOP) (Receiver program stops when hop track condition is reached)
FREQUENCY MODE	- S-BAND VHF/UHF
INITIALIZE (Push switch)	- INITIALIZE FUNCTION

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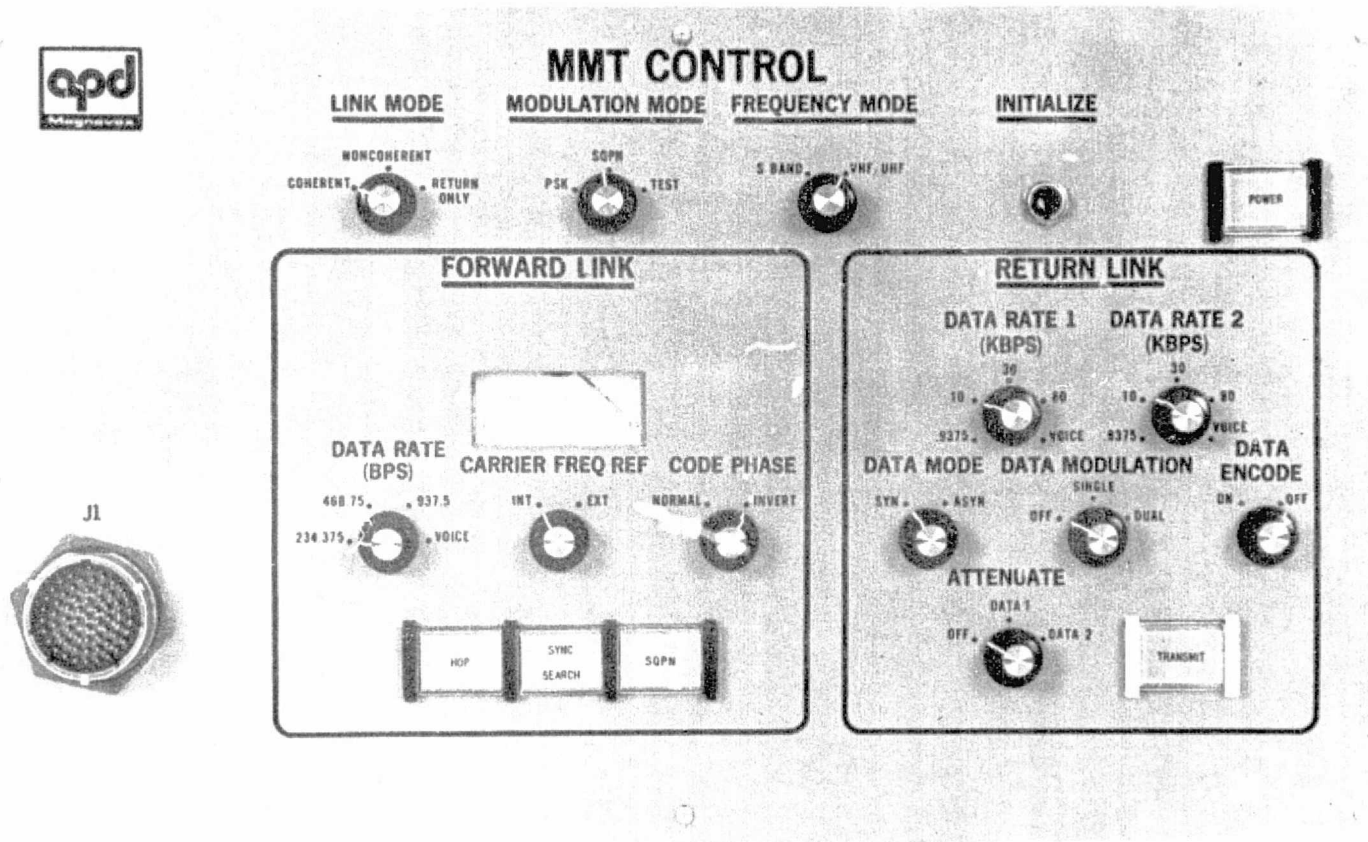

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Figure 3-15. MMT Control Panel

FORWARD LINK:

DATA RATE (BPS)	- 234.375 468.75 937.5 VOICE (10K PDM)
CARRIER FREQ REF	- INT EXT (special test mode only)
CODE PHASE	- NORMAL INVERT

RETURN LINK:

DATA RATE 1 (KBPS)	- 937.5 10 30 80 VOICE (10K PDM)
DATA RATE 2 (KBPS)	- 937.5 10 30 80 VOICE (10K PDM)
DATA MODE	- SYN (Synchronous) ASYN (Asynchronous)
DATA MODULATION	- OFF SINGLE DUAL
DATA ENCODE	- ON (Convolutional encode) OFF
ATTENUATE	- OFF DATA 1 DATA 2

The indicator lamps are listed below:

Indicator	Function
POWER	- Lighted when +28V power supply is on.
HOP	- Lighted when the forward link receiver is in the frequency hop mode.
SYNC	- Lighted when the forward link receiver has acquired carrier phase sync.
SEARCH	- Lighted when either hop search or SQPN search is operative.
SQPN	- Lighted when the forward link receiver is in staggered quadriphase pseudo-noise mode.
TRANSMIT	- Both switch and indicator to turn transmit power on or off. (Output power reduced by more than 20 dB)

The MMT control signals are listed in table 3-2. A zero (0) = GND; a one (1) represents a positive voltage with a 1K resistor to +5V.

3.2.4 SIGNAL MONITOR PANEL

The MMT signal monitor panel provides banana jacks for digital data and data clock input and output to error rate test equipment. Table 3-3 presents a list of the monitor signals. The monitor panel is pictured in figure 3-16.

3.2.5 POWER SUPPLY

The MMT power supply chassis contains four regulated power supply modules to supply DC voltages of +28V, +15V, -15V and +5V to the RF/IF chassis and the signal processor chassis. The MMT/MTAR power supply is illustrated in figure 3-17.

The power supply module specifications allow prime input power to be 105-125 vac, 50-400 Hz. These power supply modules feature short circuit and over-voltage protection. Full specifications are contained in drawing number X625196.

Table 3-2. MMT Control Signals List

Mode	Signal Name	Switch Positions				
Modulation Mode		PSK	SQPN	TEST (RX Hop)		
	MMDE1 MMDE2 MMDE3	1 0 1	1 1 0	0 1 1		
Link Mode		Coherent	Noncoherent	Return Only		
	LMDE1 LMDE2 LMDE3	0 1 1	1 0 1	1 1 0		
Data Rate (Forward Link-Receive)		234.375 BPS	468.75 BPS	937.5 BPS	Voice	
	FDRTE1R FDRTE2R FDRTE3R	0 0 0	1 0 0	0 1 0	1 1 1	
Carrier Frequency Reference		Internal VCO	EXT (Test)			
	RFINEX	0	1			
Code Phase (Receive)		Normal	Invert			
	CDPHRX	0	1			
Data Rate (Digital Data No. 1) Return Link		937.5 BPS	10K BPS	30K BPS	80K BPS	Voice
	RD1R1T RD1R2T RD1R3T	0 1 0	0 0 1	1 1 0	1 0 1	1 1 1
Data Rate (Digital Data No. 2) Return Link		937.5 BPS	10K BPS	30K BPS	80K BPS	Voice
	RD2R1T RD2R2T RD2R3T	0 1 0	0 0 1	1 1 0	1 0 1	1 1 1
Data Modulation		OFF	Single	Dual		
	DTMOD1 DTMOD2 DTMOD3	0 1 1	1 0 1	1 1 0		
Attenuate		OFF	Data 1	Data 2		
	ATTEN2 ATTEN1	0 0	0 1	1 0		
Convolutional Data Encode		ON	OFF			
	ENCODE	0	1			
Data Mode		Synchronous	Asynchronous			
	DSYASY	0	1			
Transmit		ON	OFF			
	TXON	0	1			
Freq Hop Acquisition Mode		ON (Hop)	OFF (PN)		From Controller	
	HOPACQ	0	1			
Initialize Switch		Released	Pressed			
	INITNO INITNC	 0	0 			

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Table 3-3. MMT Monitor Signals List

J1	Symbol	Signal Description
A	MP5V	+5 Volt Power Supply Access
B	MP15V	+15 Volt Power Supply Access
C	M-15V	-15 Volt Power Supply Access
D	MP28V	+28 Volt Power Supply Access
E	MRT28V	+28 Volt Return
F	GDPLATE	Chassis Ground
G	AUDIN1	Transmit Audio Input (Ground) } Configured for
H	AUDIN2	Transmit Audio Input (Signal) } Carbon Mike
J	SPARE	(Impedence: 600Ω, Input: 80 to 1400 mV rms)
K	AUDHI	Received Audio, 6.7 VRMS
L	AUDLO1	Received Audio Output } Balanced Pair,
M	AUDLO2	Received Audio Output } 600Ω, 3 VRMS
N	SYNCBL	}
P	SYNCYL	} TSP (Not Used MMT)
R	GROUND	}
S	CLKBL	}
T	CLKYL	} TSP (Not Used MMT)
U	GROUND	}
V	2XCLK1	Output 2X Data 1 Clock
W	1XCLK1	Output 1X Data 1 Clock
X	1XCLK2	Output 1X Data 2 Clock
Y	2XCLK2	Output 2X Data 2 Clock
Z	TXDATA1	Input Data Signal 1
a	TXDATA2	Input Data Signal 2
b	ASYNCLK2	Input Asynchronous Clock (Data 2)
c	ASYNCLK1	Input Asynchronous Clock (Data 1)
d	RXCLKBAR	Output Inverted RX Data Clock
e	RXDATA	Output Receive Data
f	RXCLK	Output Receive Data Clock
g	AGC	Monitor AGC voltage
h	GROUND	
j	GROUND	

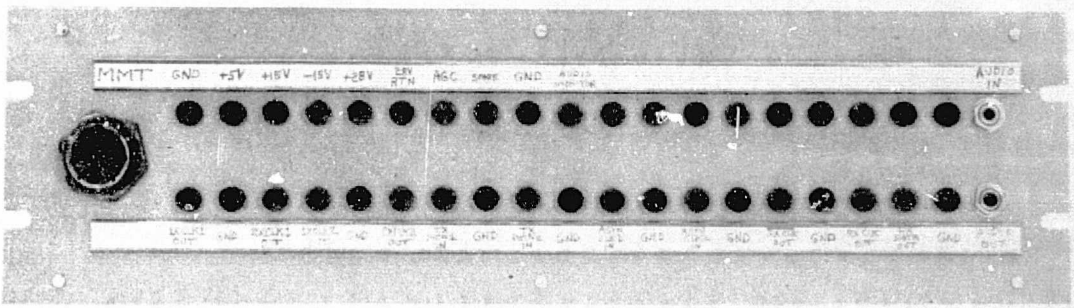

Figure 3-16. MMT Signal Monitor Panel

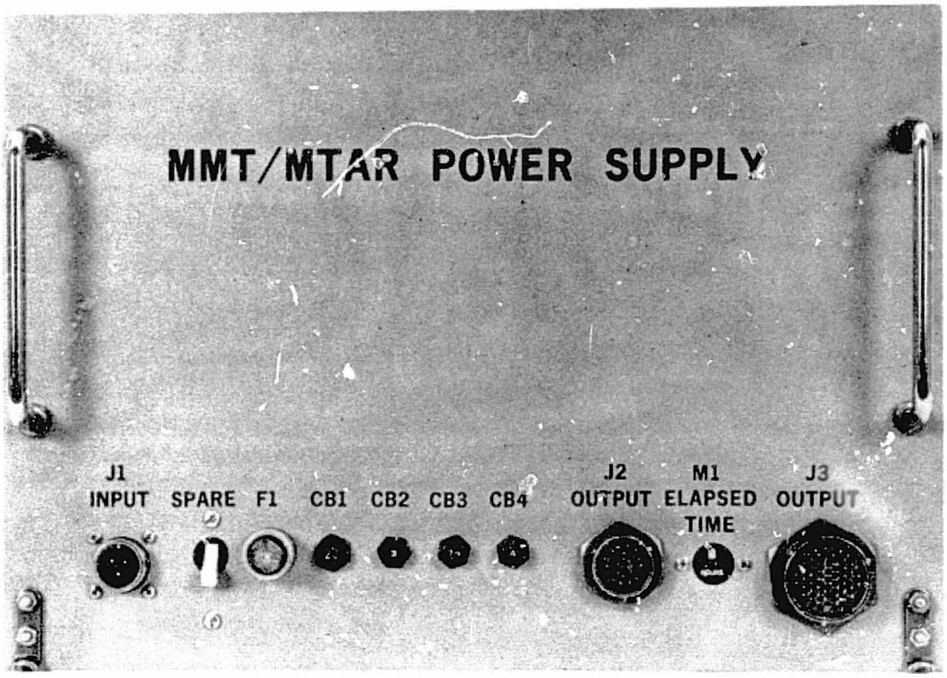

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Figure 3-17. MMT/MTAR Power Supply Chassis

The estimated DC power requirements for the MMT are listed below.

+28V	20 watts
+15V	6 watts
-15V	3 watts
+ 5V	50 watts

3.3 MTAR (SIMULATED GROUND TERMINAL EQUIPMENT)

The Multimode Transmitter and Receiver (MTAR) consists of a receiver-transmitter chassis, signal processor chassis, control panel, signal monitor panel and power supply chassis. This section gives a detailed functional description of each of these assemblies. The error rate test equipment used with the MTAR is described in section 3.4.

3.3.1 RECEIVER-TRANSMITTER CHASSIS

The receiver-transmitter chassis contains the high frequency elements that connect directly to an antenna with both transmit and receive signals. The transmit section of the RT chassis converts a modulated 401 MHz signal to the S-band transmit frequency of 2106. 40625 MHz. The receive section amplifies and converts the

2287.5 MHz signal to a 12 MHz intermediate frequency. Figure 3-18 shows the front and top views of the MTAR RT chassis. Figure 3-19 is a block diagram of the MTAR receiver-transmitter chassis.

The S-band modification task of Contract NAS5-20330 implemented the conversion of the original VHF/UHF frequencies to S-band frequencies. The 401 MHz transmit signal is accessible by removing a front panel jumper cable. The 137 MHz receive input is also available by removing a front panel jumper cable.

As shown in figure 3-20 the local oscillator for conversion of the 401 MHz modulator output to the S-band is obtained by multiplying the 22.73895 MHz L.O. input by 75 in a phase lock multiplier. The 22.73875 MHz L.O. is coherent with the 401 MHz transmit carrier signal. Signal monitor jacks are provided for both the 401 MHz and 2106.40625 MHz transmit signals. The 2106.40625 MHz monitor output is amplified to provide at least 0 dBm signal power to drive a frequency counter. Individual power switches are mounted in the chassis for the transmit PLM and the transmit monitor amplifer to aid in isolating any interference with other equipment in the laboratory setup.

A diplexer is used to isolate the receiver input from the transmit signal. The received signal is amplified and converted in three IF steps to 12 MHz. The last two IF stages are enclosed in a shielded assembly. The schematic of the MTAR IF assembly is Drawing X498734. The system AGC is applied to the 57 MHz IF stage. The AGC control voltage is developed in the signal demodulator and is brought to the RT chassis on pin K of connector J2. When the equipment modification was completed, pin K was the only pin used on connector J2. For testing and troubleshooting the AGC can be disabled giving maximum RF gain by simply disconnecting the cable to J2. The receive local oscillator signals are synthesized in the signal processor chassis and brought to the RT chassis via coaxial cables.

3.3.2 SIGNAL PROCESSOR CHASSIS

The MTAR signal processor chassis contains the receiver circuitry from the 12 MHz IF down to baseband processing as well as the transmit baseband and modulation circuitry. The MTAR signal processor is made up of plug-in printed circuit boards. Table 3-4 lists the board nomenclature showing location in the MTAR chassis.

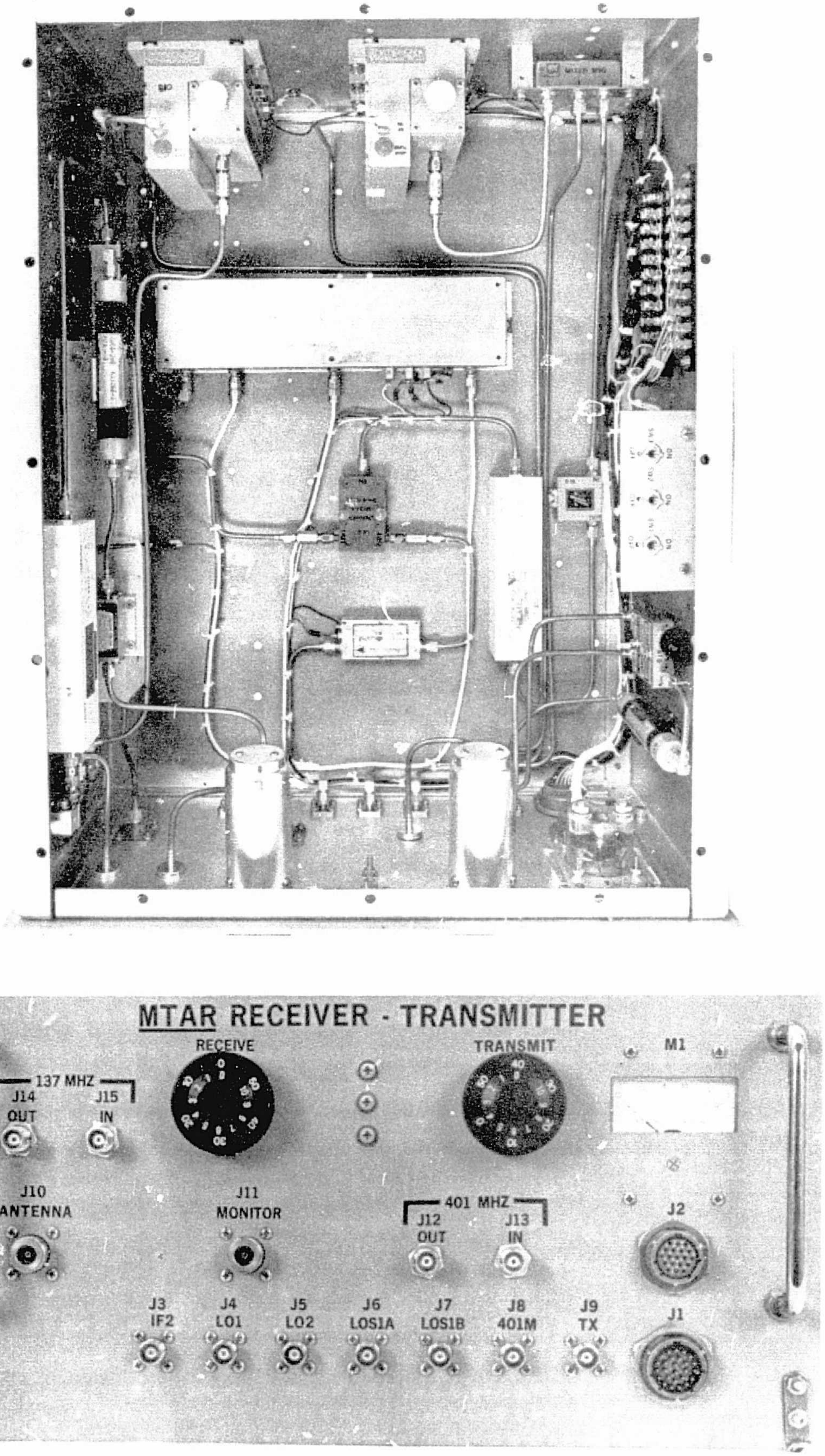

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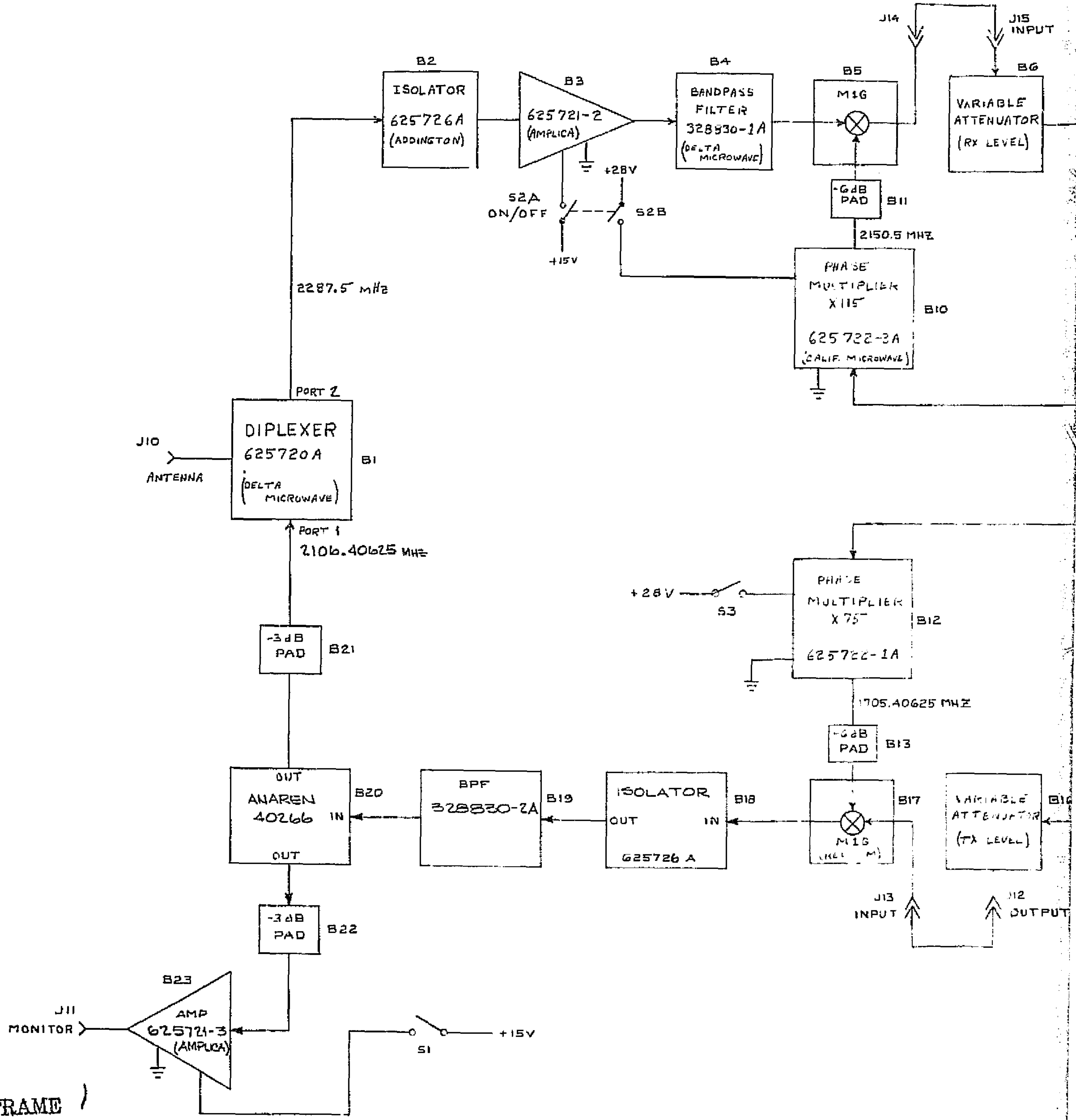
Figure 3-18. MTAR Receiver-Transmitter, Front and Top Views



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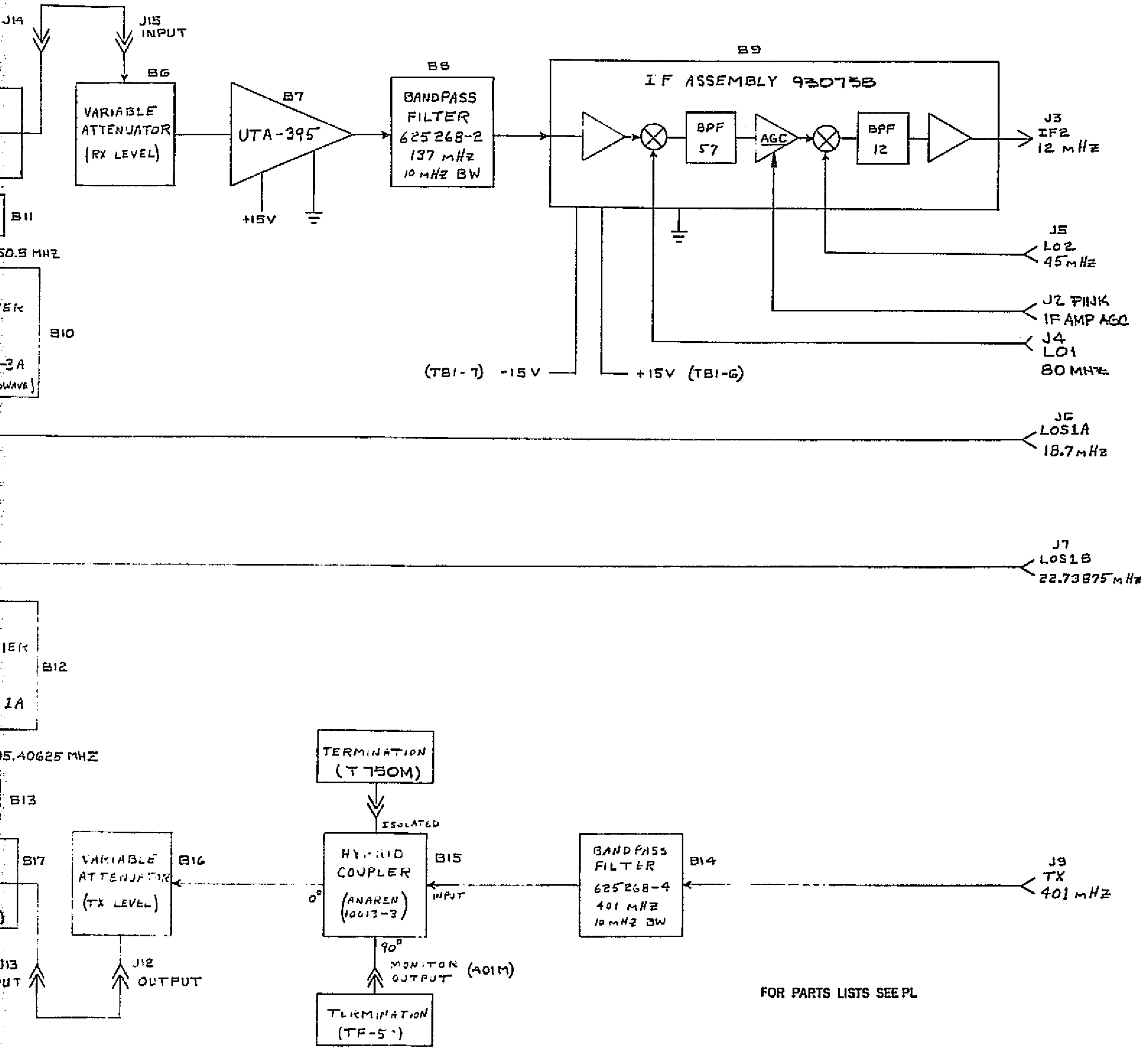

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FOLDOUT FRAME 2

Figure 3-19. MTAR RT Block Diagram

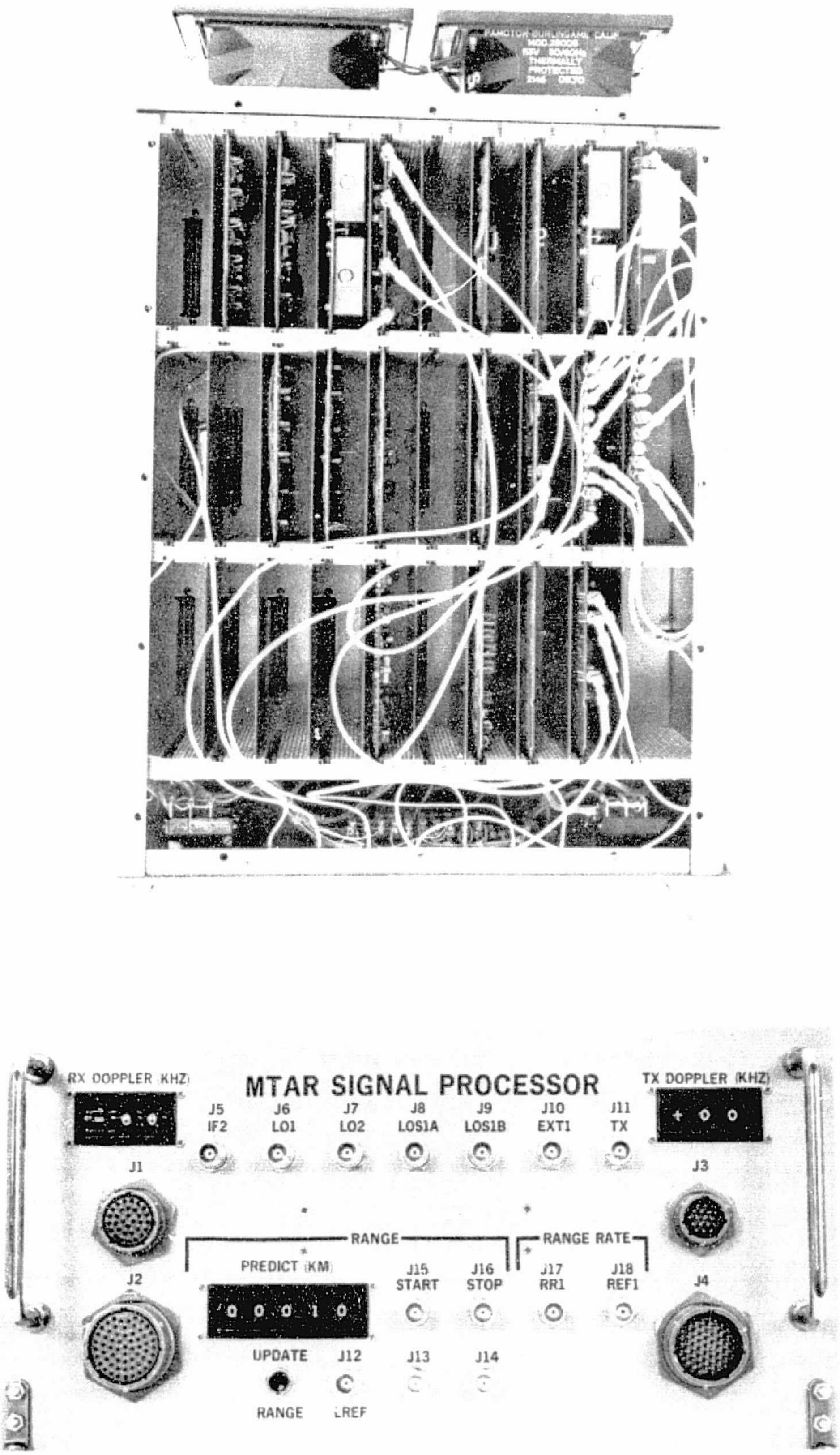

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Figure 3-20. MTAR Signal Processor, Front and Top Views

Table 3-4. MTAR Printed Circuit Board Data

Assembly Dwg. No.	PC Board Nomenclature	Schematic Dwg. No.	Location	Quantity
X918051A	Code & Data Clock Synth.	X498701A	2B06	1
X918052A	Coder No. 1	X498702A	2B08	1
X918053A	Coder No. 2	X498703A	2B07	1
X918054A	Controller No. 1	X498704A	3B04	1
X918074A	Controller No. 2	X498724A	3B03	1
X918056A	MTAR Local Reference/ Correlator	X498705A	2B09	1
X918061A	Receive Filter	X498711A	3B09	1
X918062A	MTAR Detector	X498712A	3B08	1
X918076A	MTAR VCO	X498726A	3B07	1
X918085A	MTAR Frequency Discriminator	X498735A	3B10	1
X918069A	Frequency Hop	X498719A	2B04	1
X918087A	MTAR Data Recovery	X498737A	1B04	1
X918075A	Frequency Reference	X498725A	3B02	1
X918066	PDM Voice	X498716	1B06	1
X918067	MMT/MTAR Synth. No. 1	X498717	2B01	1
X918077	MTAR Synth. No. 2	X498727	2B02	1
X918078	MTAR Synth. No. 3	X498728	3B06	1
X918070A	TX Data Processor	X498720A	1B03	1
X918073A	MTAR Modulator	X498723A	2B03	1
X918089	18.7 MHz Synth.	X498739	3B01	1
X918081	22.73875 MHz Output	X498731	1B02	1
X918082	27.3875 MHz Synth.	X498732	1B01	1

Figure 3-20 shows the front and top views of the MTAR signal processor chassis. The printed circuit board locations in the signal processor chassis are identified by a four character number. The first number identifies the row with 1, 2, and 3 indicating the front, middle and rear rows respectively. The last two digits locate slots 1 through 10 in each row. The second character is a B in the MTAR signal processor chassis and an A in the MMT signal processor chassis.

3.3.2.1 Frequency Synthesis

The signal processor chassis contains the frequency synthesis circuitry for the receive local oscillator signals and the transmit carrier. Since the S-band conversion for the transmit and receive functions is located in the RT chassis, the S-band L.O.'s are cabled from the signal processor to the RT at relatively low frequencies. Phase lock multipliers in the RT multiply the S-band L.O. signals. The 22.73875 MHz transmit L.O. is multiplied by 75 to 1705.40625 MHz. The 18.7 MHz receive L.O. is multiplied by 115 to 2150.5 MHz.

The S-band modification effort added the necessary coherent S-band synthesis while retaining the old VHF/UHF synthesis. Figure 3-21 shows the VHF/UHF synthesis. In the MTAR the transmit and receive L.O. synthesis functions are independent. The receive L.O. synthesis is contained on MTAR Synthesizer Board No. 3 (3B06). The transmit synthesis is contained on Synthesizer Board No. 1 (2B01) and MTAR synthesizer Board No. 2 (2B02).

The S-band synthesis in the MTAR uses the same circuitry as the MMT except that the transmit and receive functions are reversed. The S-band synthesis is shown in figure 3-10. In the MTAR the 18.7 MHz synthesizer board (3B01) generates the LOS1A signal used for the S-band receive conversion. The 27.3875 MHz synthesizer board (1B01) and the 22.73875 MHz output board (1B02) combine to generate the LOS1B signal used for S-band transmit conversion in the MTAR. The transmit carrier frequency is synthesized either from an internal 10 MHz oscillator (3B02) or from an external 5 MHz reference signal. The circuitry for switching the carrier reference frequency source is located on the 22.73875 MHz output board (1B02) and is controlled from a control panel switch.

3.3.2.2 Receiver

The MTAR receiver is very similar to the MMT receiver. Since there is no frequency hop preamble for the return link, the frequency hop detector and loop filter circuits are not included in the MTAR receiver. The bandwidths of the Costas loop side integrations correspond to the return link data rates. With the above noted differences the MTAR receiver can be shown by the detailed block diagram, figure 3-12.

The MTAR receiver boards include the MTAR VCO board (3B07), the MTAR detector board (3B08), the receive filter board (3B09) and the MTAR frequency discriminator board (3B10).

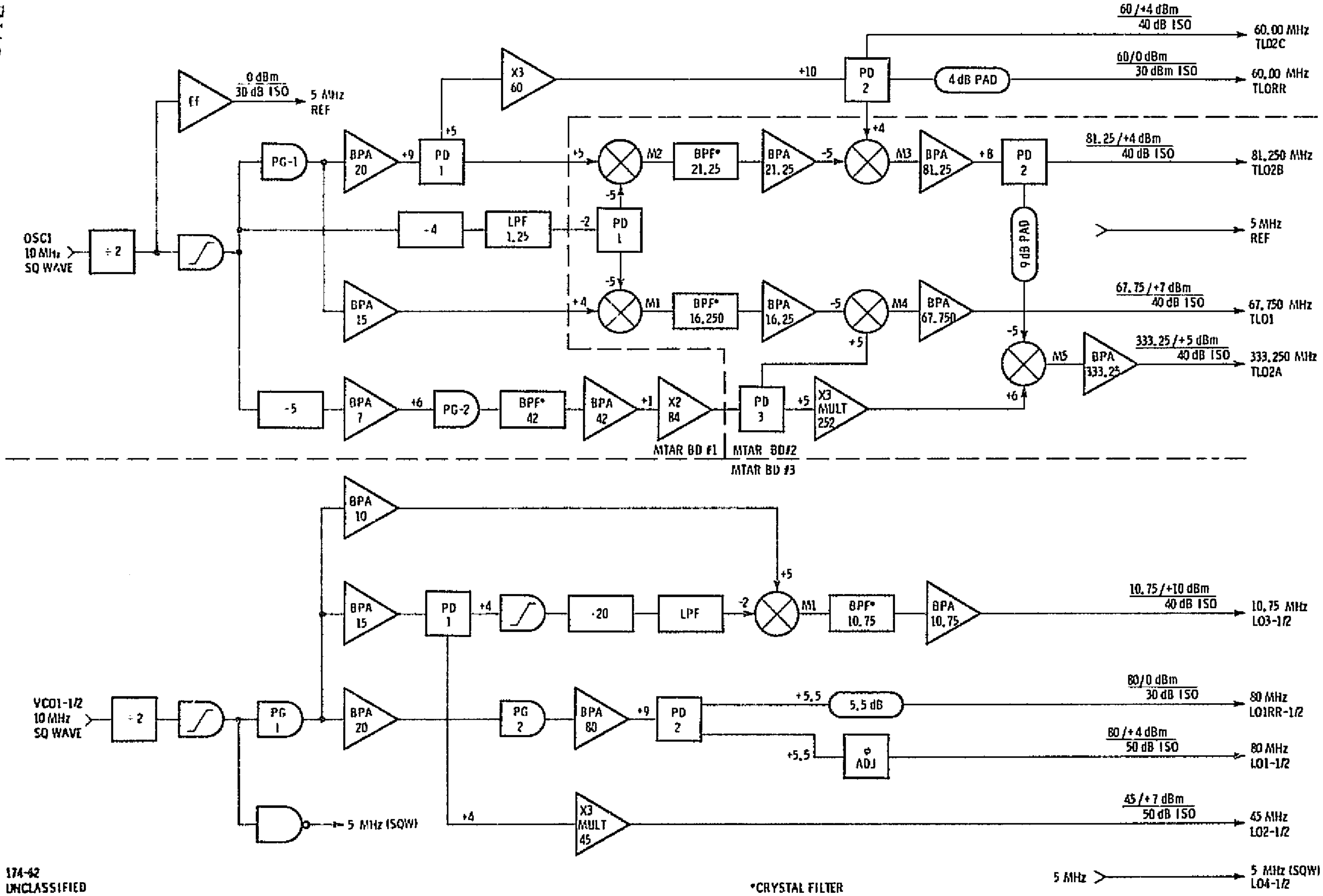

Figure 3-21. MTAR VHF/UHF Synthesis

3.3.2.3 Controller

The MMT/MTAR controller block diagram is shown in figure 3-13. The controller ROM program and flowchart are shown in figure 3-14. The controller program includes the system operation commands for both the MMT and MTAR. A hard-wired input in each chassis tells the controller which unit program to follow. The MTAR controller uses Controller Board No. 1 (3B04) and Controller Board No. 2 (3B03).

3.3.3 CONTROL PANEL

The MTAR control panel contains the mode selector switches and indicator lamps for the MTAR equipment. The MTAR control panel is pictured in figure 3-22.

The MTAR control functions are listed below:

MTAR CONTROL:

LINK MODE	- COHERENT transpond NONCOHERENT transpond RETURN ONLY
MODULATION MODE	- PSK SQPN (transmits hop preamble with timed switch to SQPN) TEST (transmitter stays in hop mode)
FREQUENCY MODE (return link)	- S-BAND VHF/UHF
INITIALIZE (Push Button)	- INITIALIZES FUNCTION

FORWARD LINK:

DATA RATE (BPS)	- 234.375 468.750 937.500 VOICE (10K PDM)

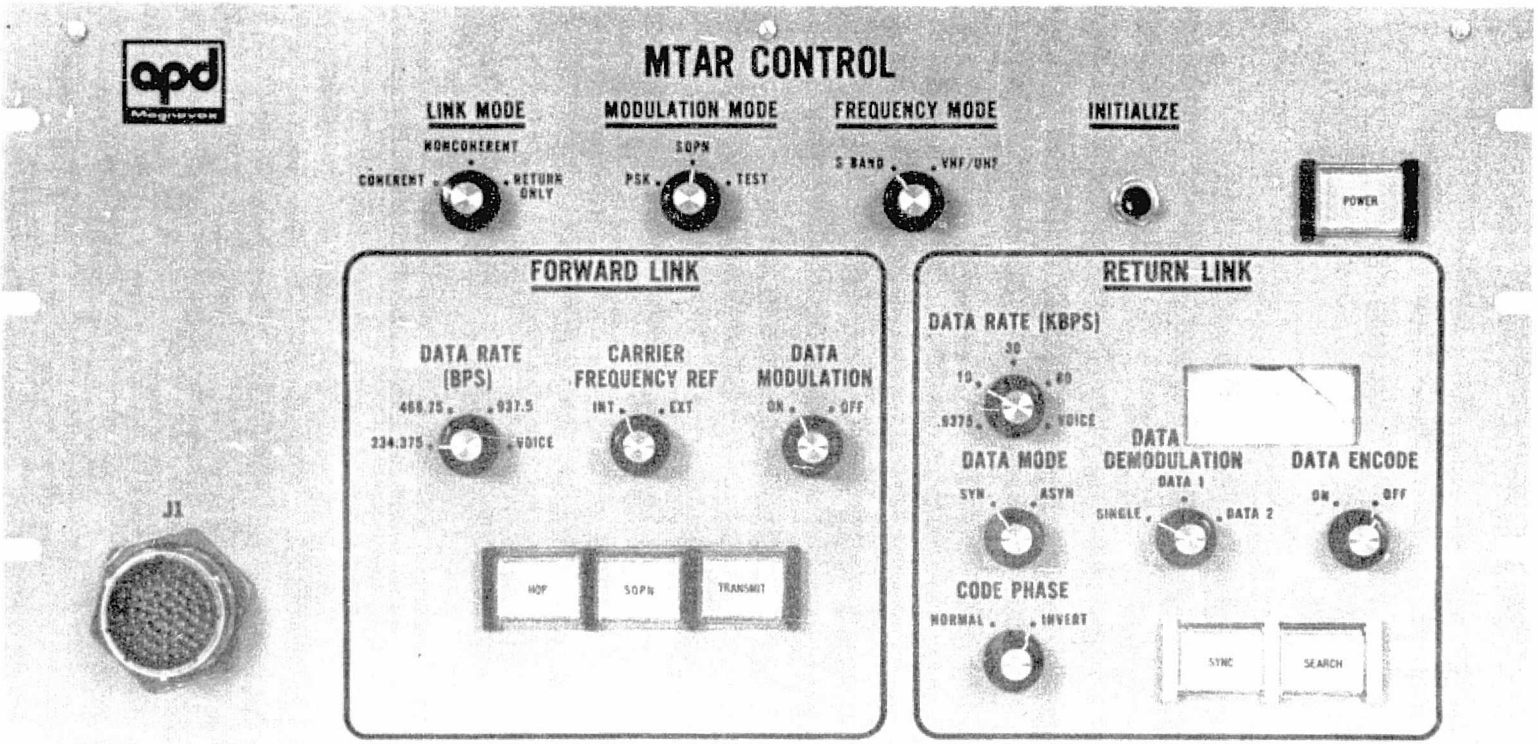

Figure 3-22. MTAR Control Panel

CARRIER FREQUENCY REF	- INT (Internal) EXT (External)
DATA MODULATION	- ON OFF

RETURN LINK:

DATA RATE (KBPS)	- 937.5 10 30 80 VOICE (10K PDM)
DATA MODE	- SYN (Synchronous) ASYN (Asynchronous)
DATA DEMODULATION	- SINGLE DATA 1 (Dual) DATA 2 (Dual)
DATA ENCODE	- ON (Informs receiver circuits that the data on the receive signal is convolutional encoded at the MMT transmit) OFF
CODE PHASE	- NORMAL INVERT

The indicator lamps are listed below:

Indicator	Function
POWER	- Lighted when +28V power supply is on.
HOP	- Both momentary switch and indicator for the frequency hop transmit mode. Pressing the switch starts the 15-second hop preamble timer.
SQPN	- Lighted when the forward link transmitter is in staggered quadriphase pseudo-noise mode. Also lighted when modulation mode switch is in test position.

Indicator	Function
TRANSMIT	- Both switch and indicator to turn transmit power on or off. (Output power reduced by more than 20 dB.)
SYNC	- Lighted when the return link receiver has acquired carrier phase sync.
SEARCH	- Lighted when any of the SQPN code search modes is operative.

The MTAR control signals are listed in table 3-4. A zero (o) = GND; a one (1) represents a positive voltage with a 1K resistor to +5V.

3.3.4 SIGNAL MONITOR PANEL

The MTAR signal monitor panel provides banana jacks for digital data and data clock input and output to error rate test equipment. In addition line driver output lines for interface to the AGIPA equipment are located on the MTAR signal monitor panel. Table 3-5 presents a list of the monitor signals. The monitor panel is pictured in figure 3-23.

3.3.5 POWER SUPPLY

The MTAR power supply chassis contains four regulated power supply modules to supply DC voltages of +25V, +15V, -15V and +5V to the RF/IF chassis and the signal processor chassis. The MMT and MTAR power supply chassis are interchangeable.

The power supply module specifications allow prime input power to be 105-125 VAC, 50-400 Hz. These power supply modules feature short circuit and over-voltage protection. Full specifications are contained in Drawing X625196.

The estimated DC power requirements for the MTAR are listed below.

+28V	20 watts
+15V	6 watts
-15V	3 watts
+ 5V	50 watts

Table 3-5. MTAR Control Signals List

Mode	Signal Name	Switch Positions				
		PSK	SQPN	TEST (TX HOP)		
Modulation Mode	MMDE1 MMDE2 MMDE3	1 0 1	1 1 0	0 1 1		
		Coherent	Noncoherent	Return Only		
Link Mode	LMDE1 LMDE2 LMDE3	0 1 1	1 0 1	1 1 0		
Data Rate (Forward Link - Transmit)		234.375 BPS	468.75 BPS	937.5 BPS	Voice	
	FDRTE1T FDRTE2T FDRTE3T	0 0 0	1 0 0	0 1 0	1 1 1	
		ON	OFF			
Data Modulation	DATMD	0	1			
		Internal OSC	External			
Carrier Frequency Reference	RFINEX	0	1			
		ON	OFF			
Transmit	TXON	0	1			
Data Rate (Return Link-Receive)		937.5 BPS	10K BPS	30K BPS	80K BPS	Voice
	RDRTE1R RDRTE2R RDRTE3R	0 1 0	0 0 1	1 1 0	1 0 1	1 1 1
		Single	Dual Data 1	Dual Data 2		
Data Demodulation	DTDMD1 DTDMD2 DTDMD3	1 1 0	0 1 1	1 0 1		
		Synchronous	Asynchronous			
Data Mode	DSYASY	0	1			
		Normal	Invert			
Code Phase (Receive)	CDPHRX	0	1			
		ON	OFF			
Convolutional Data Encode	ENCODE	0	1			
		ON (Hop)	OFF (PN)			
Freq Hop Acquisition Mode	XMTHOP	0	1		From Controller	
		Released	Pressed			
Initialize Switch	INITNO		0			
	INITNC	0				
		S-Band	VHF/UHF			
Frequency Mode	BANDSW	0	1			

Table 3-5. MTAR Monitor Signals List

J1	Symbol	Signal Description
A	MP5V	+5 Volt Power Supply Access
B	MP15V	+15 Volt Power Supply Access
C	M-15V	-15 Volt Power Supply Access
D	MP28V	+28 Volt Power Supply Access
E	MRT28V	+28 Volt Return
F	GDPLATE	Chassis Ground
G	AUDIN1	Transmit Audio Input (Ground) } Configured for
H	AUDIN2	Transmit Audio Input (Signal) } Carbon Mike
J	--	(Impedance: 600Ω, Input: 80 to 1400 mV rms)
K	AUDHI	Received Audio, 6.7 VRMS
L	AUDLO1	Received Audio Output } Balanced Pair,
M	AUDLO2	Received Audio Output } 600Ω, 3 vrms
N	SYNCBL	} TSP SYNC
P	SYNCYL	} Line Driver Output
R	GROUND	} to AGIPA
S	CLKBL	} TSP RX Data Clock
T	CLKYL	} Line Driver Output
U	GROUND	} to AGIPA
V	TXCLK	Output 1X Data Clock
W	TXCLKBAR	Output Inverted 1X Data Clock
X	TXDATA	Input Transmit Digital Data
Y	RDTMSB	SIGN } Soft decision interface
Z	RDT2SB	MAG 1 } output to Viterbi
a	RDTLSB	MAG 2 } decoder.
b	RDTRTN	Ground
c	RXCLK	Output RX Data Clock
d	RXCLKBAR	Output Inverted RX Data Clock
e	RXDATA	Output Receive Data
f	RXDATABAR	Output Inverted Receive Data
g	AGC	Monitor AGC voltage
h	GROUND	
j	GROUND	

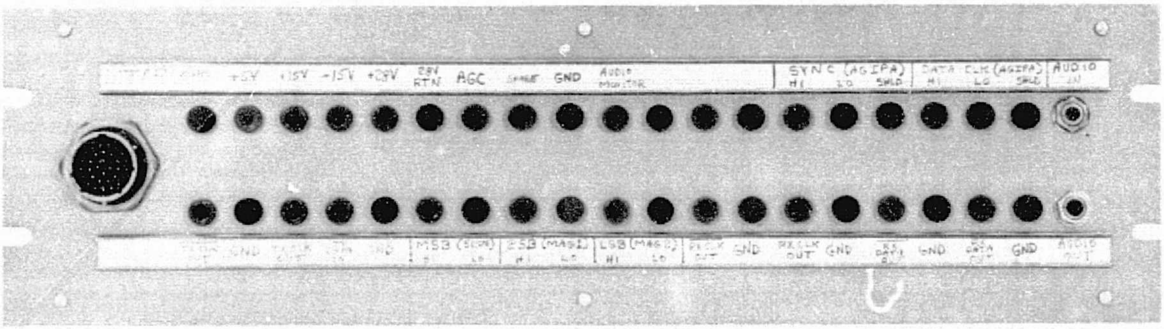

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Figure 3-23. MTAR Signal Monitor Panel

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3.4 SYSTEM TEST

The MMT/MTAR system link performance is evaluated by measuring digital data error rate performance for both forward and return links. The MX 270B bit error rate analyzer and data generator is the instrument used for performance measurement. Convolutional encoding can be selected for the return link. A Linkabit Corp. Model LV7015 instrument is used for Viterbi decoding at the MTAR.

3.4.1 BIT ERROR RATE MEASUREMENT

For system performance measurement connect the equipment as shown in figure 3-24. The transmit signal from each unit is attenuated to obtain the desired signal threshold at the opposite receiver. The MX 270B provides the data bit stream for transmit and measures the error rate of the received digital data. The MMT is connected to its MX 270B as shown in figure 3-25. The MTAR is connected to its MX 270B as shown in figure 3-26.

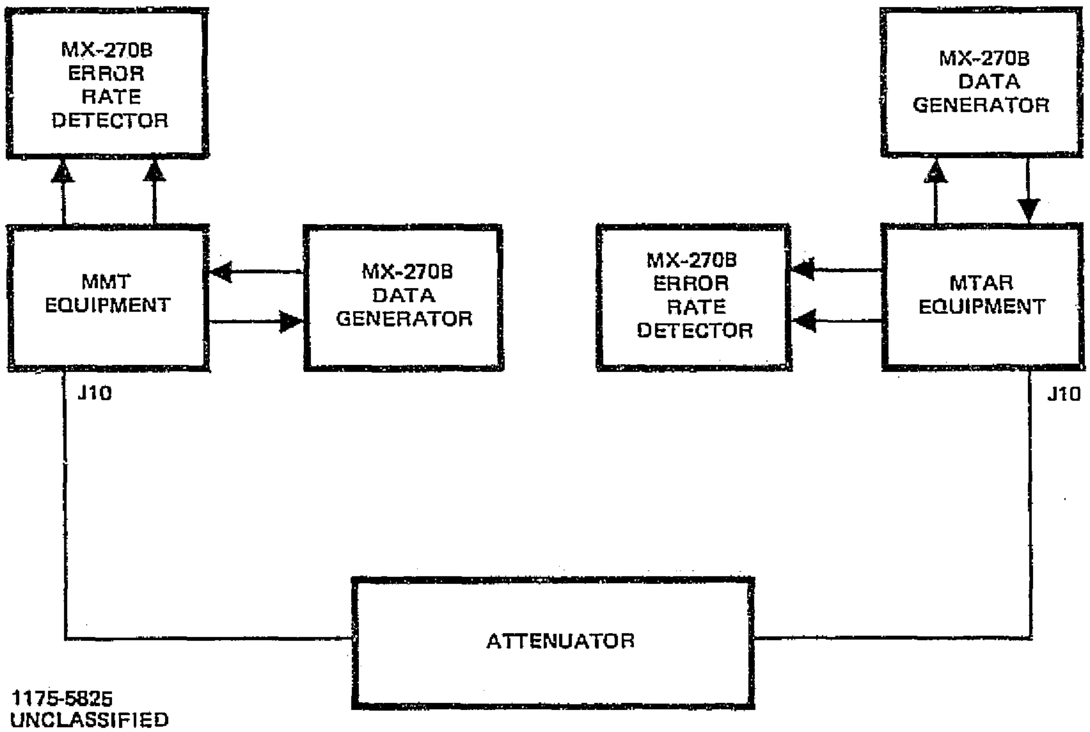

Figure 3-24. Back-to-Back Test Setup

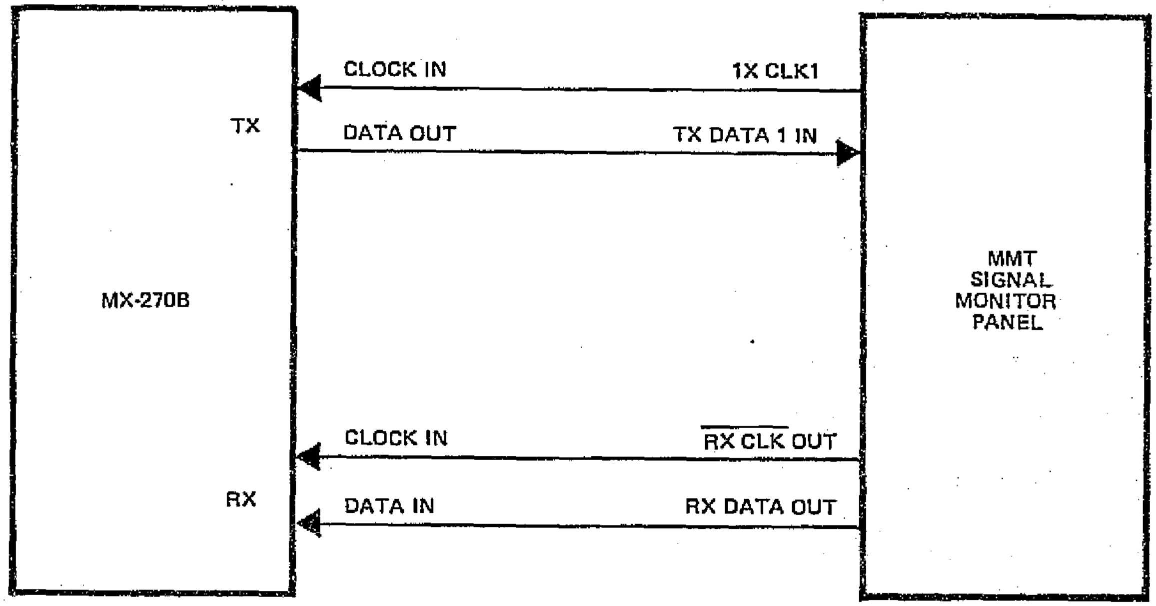

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Figure 3-25. MMT Error Rate Setup

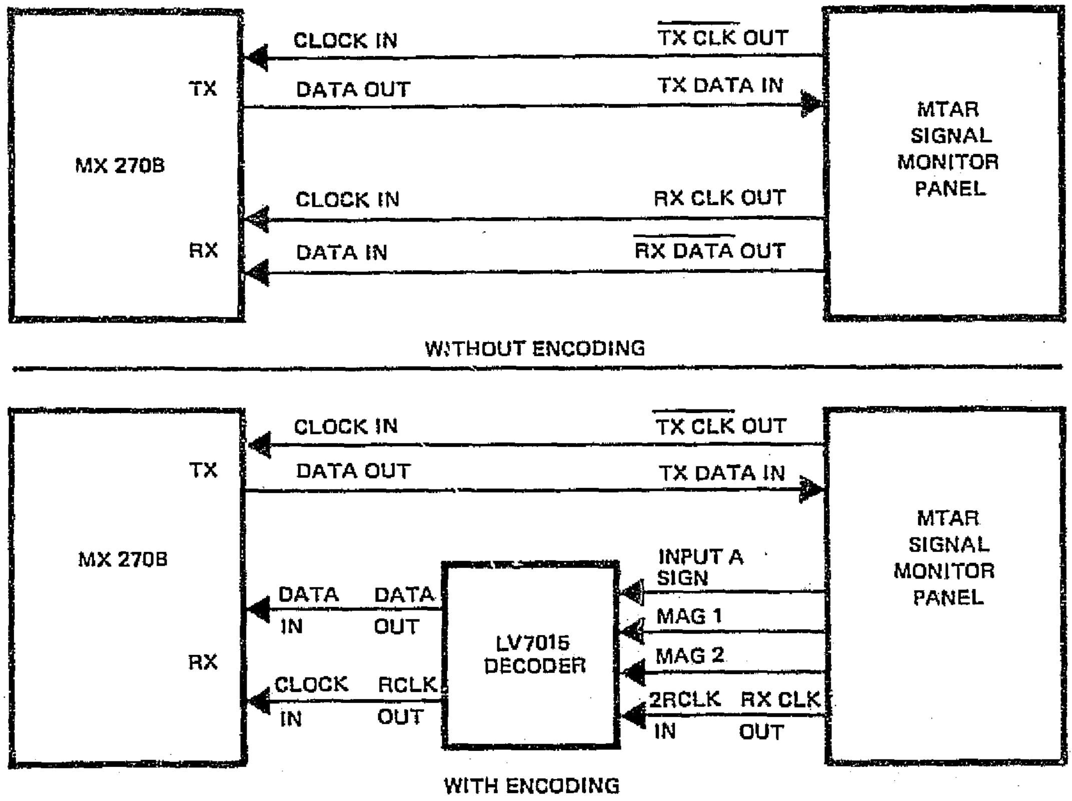

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Figure 3-26. MTAR Error Rate Setup

3.4.2 MX 270B

The MX 270B, shown in figure 3-27, provides a direct readout of error rate performance for digital communications modems. During operation, test data for the modem channel is clocked out of the MX 270B transmitter section at any rate up to 10 megabits per second. Similarly, the modem clocks data into the MX 270B receiver section. The received sequence is compared bit-by-bit with an internally generated sequence.

A simplified block diagram of the MX 270B is shown in figure 3-28. There are four basic sections in the MX 270B: a) transmitter, b) receiver, c) counter, and d) power supply. During operation, a clock pulse received from an external (or internal) source generates a data pattern selected by the front-panel controls. The modem under test demodulates the data pattern and supplies the demodulated data pattern along with the data clock back into the receiver section of the MX 270B. The MX 270B then injection loads a similar data pattern generator and compares the injection loaded pattern with the modem demodulated data pattern in a bit-by-bit comparison to generate an error pattern. This error pattern is then counted over a selected number of bits determined by the X10⁻ front panel control and the SAMPLE SIZE control. The selected sample size error rate is then displayed on the ERROR RATE indicator.

3.4.3 LV7015

The Linkabit Model LV7015, shown in figure 3-29, is a full duplex, constraint length 7, rate 1/2, convolutional encoder-Viterbi decoder. The LV7015 can be operated at any data rate up to 100 Kilobits/sec (200 K code symbols/sec.). The data

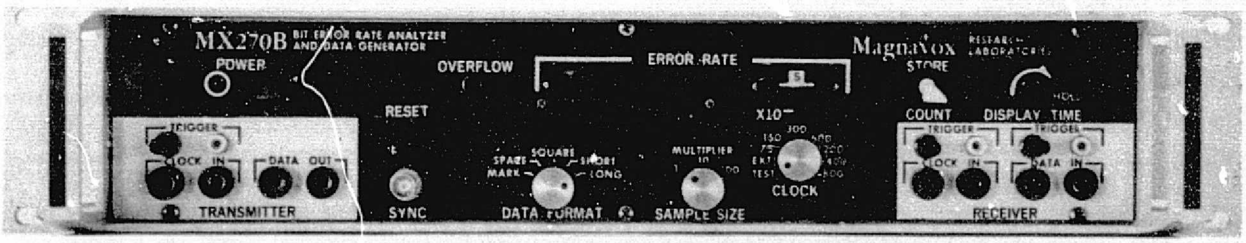

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Figure 3-27. MX 270B Bit Error Rate Analyzer

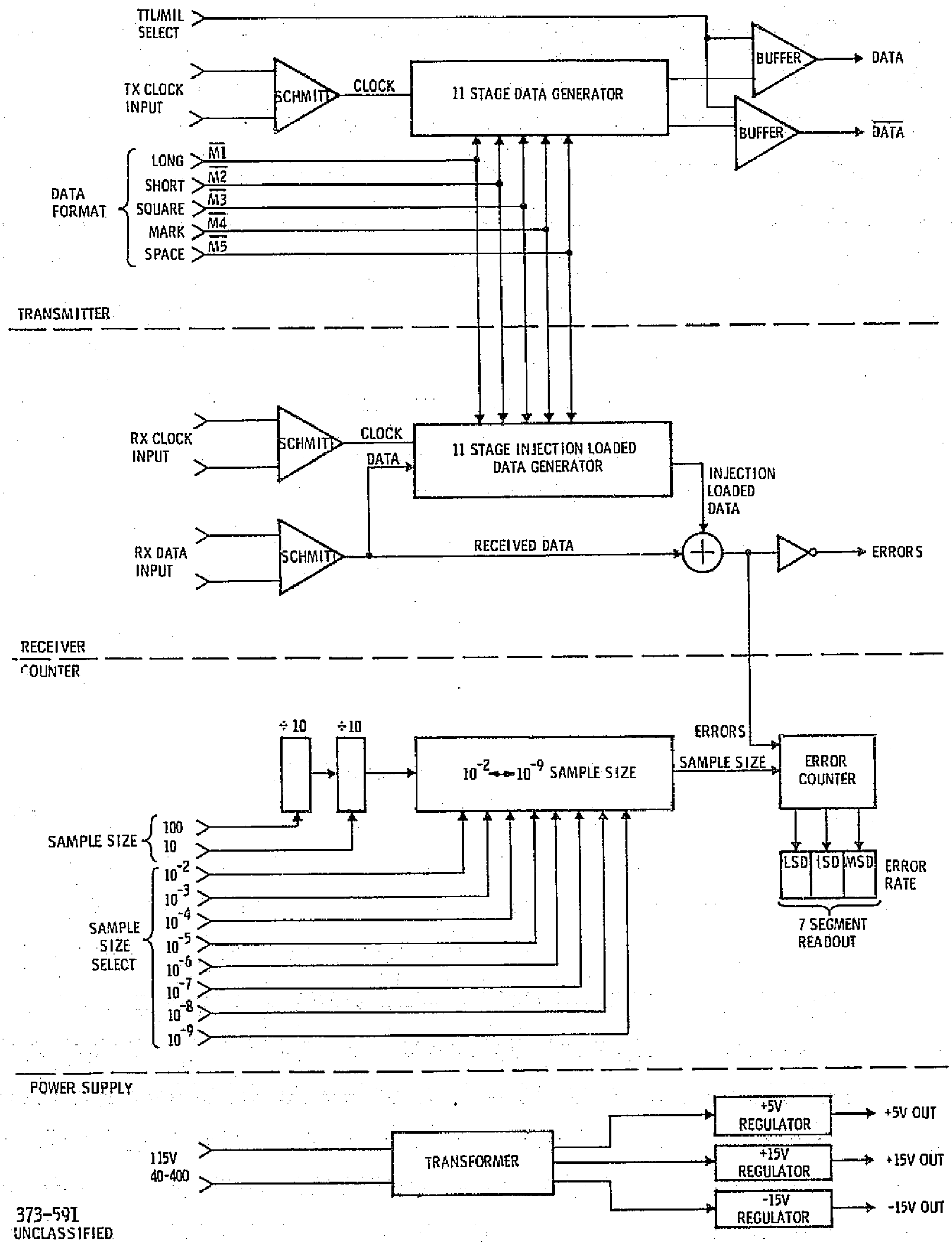

Figure 3-28. MX 270B Functional Block Diagram

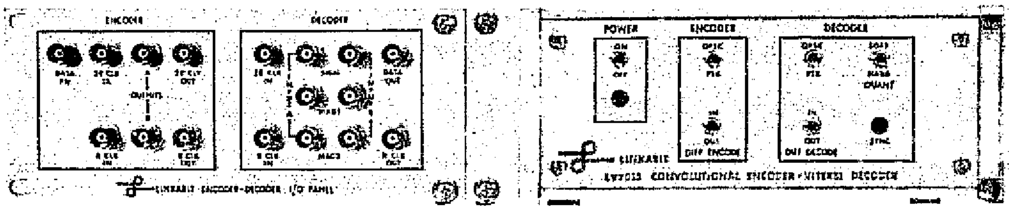

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Figure 3-29. Linkabit LV7015

rate is determined by the clocks input to the encoder and decoder sections. The encoder and decoder portions of the LV7015 may be operated completely independently. The Viterbi decoder accepts as input either hard (2 level) or soft (8 level) quantized received data. A coding gain (savings in required energy per bit-to-noise ratio relative to ideal coherent PSK modulation in additive white Gaussian noise) in excess of 5 dB is provided by the LV7015 at a 10^{-5} bit error rate when operating in the soft quantized mode. A corresponding gain of greater than 3 dB is attained in the hard quantized mode.

The LV7015 uses a code which is transparent to 180° carrier phase ambiguities (received data sign inversion) which may occur when received carrier phase is tracked using only the modulated received signal. Switch selectable differential data encoding and decoding enables the LV7015 to operate when received data sign ambiguity exists.

3.4.4 FRONT PANEL MONITOR JACKS

The MMT and MTAR signal processor and receiver-transmitter chassis have a number of front panel monitor jacks for system troubleshooting and test.

3.4.4.1 MTAR Signal Processor J18 (Ref 1)

This 5 MHz output signal can be used to determine how close to nominal frequency the MTAR transmit signal is. For each cycle of frequency offset at 5 MHz the the S-band transmit signal is offset by 421 hertz.

3.4.4.2 MMT Signal Processor J12 (5 MRx)

This 5 MHz output signal can be used to determine how close to nominal frequency the MMT receive carrier VCO is. Press the initialize switch while measuring the frequency to hold the AFC at the nominal center of its range.

3.4.4.3 MMT Signal Processor J13 (5 MTx)

This 5 MHz output signal can be used to determine how close to nominal frequency the MMT transmit carrier oscillator is. Place the MMT link mode switch in noncoherent mode. For each cycle of frequency offset at 5 MHz the S-band transmit carrier is offset by 457.5 hertz.

3.4.4.4 MTAR Signal Processor J15 (START)

This positive going pulse represents the SQPN all ones vector for the forward link transmit code. Terminate the cable with 50 ohms.

3.4.4.5 MTAR Signal Processor J16 (STOP)

This inverted pulse represents the SQPN all ones vector for the return link receive code. Terminate the cable with 50 ohms. With both links in sync in coherent mode, the J16 (STOP) pulse will follow the J15 (START) pulse by approximately 8.3 microseconds (using short signal cables).

3.4.4.6 MMT Signal Processor J14 (no label)

This positive going pulse represents the SQPN all ones vector for the forward link receive code. Terminate the cable with 50 ohms. With the forward link in sync, the MMT J14 pulse will follow the MTAR J15 pulse by approximately 200 nanoseconds (using short signal cables).

SECTION IV
MECHANICAL DESCRIPTION

This section provides a detailed mechanical description of each of the major assemblies which are included in the Multimode Transponder equipment group. The dimensions, weight and construction technique is given for each major unit.

4.1 MAJOR ASSEMBLIES

The TDRSS Multimode Transponder equipment complement consists of the MMT system and the MTAR ground system. Mechanically, the two systems are nearly identical with the chief differences being panel layouts and/or placement of electronics.

Each system consists of six assemblies: signal processor, receiver-transmitter, control panel, power supply, bit error rate analyzer and a signal monitor panel. In addition a Linkabit LV7015 is supplied with the MTAR equipment. A Multimode Transponder equipment list is shown in table 4-1.

Table 4-1. Multimode Transponder Equipment List

Nomenclature	P/N	S/N
MTAR Control Panel	911438	1
MTAR Signal Processor	930770	1
MTAR Receiver-Transmitter	930754	1
MMT/MTAR Power Supply	930753	1
MTAR Monitor Panel	911814	1
MMT Control Panel	911437	1
MMT Signal Processor	930771	1
MMT Receiver-Transmitter	930755	1
MMT/MTAR Power Supply	930753	2
MMT Monitor Panel	911815	1
MX 270B Bit Error Rate Analyzer	918654	1
MX 270B Bit Error Rate Analyzer	918654	2
Linkabit Encoder/Decoder	LV7015	

4.2 RECEIVER-TRANSMITTER

The Receiver-Transmitter chassis contains all the RF subassemblies down to the 2nd IF for the receiver and the RF conversion for the transmitter. Basic construction of the unit is a simple brazed sheet aluminum box. The case is RF sealed by utilization of RF gasketing at the top cover. Since power dissipation is low and cooling is by natural convection, conduction and radiation to the case is adequate. All input-output power and signal connectors as well as the power attenuator(s) are located on the front panel. A standard holddown arrangement is provided for mounting in a MS 91405 type mounting tray. Access to all components is from the top. The cover is provided with 1/4 turn fasteners to speed removal.

Pertinent mechanical specifications include:

Size	15.38W x 7.63H x 18.10L
Cooling	Natural convection
Weight	MTAR = 30 lbs
	MMT = 30 lbs
Construction	Sheet aluminum riveted assembly

4.3 SIGNAL PROCESSOR

The Signal Processor chassis contains most of the IF subassemblies and all of the baseband processing for both the receive and transmit functions. Basic construction of the unit is sheet aluminum, with internal honeycomb sections that impart structural strength in addition to the primary task of providing free passage of cooling air and RFI protection between rows of circuit boards. A standard holddown arrangement is provided for mounting in an MS 91405 type mounting tray.

Pertinent mechanical specifications include:

Size	15.38W x 7.63H x 18.10L
Cooling	Forced air convection
Circuit Cards	27
Card Size	Nominal 4 x 6
Weight	36 lbs
Construction	Sheet aluminum riveted assembly with honeycomb sections between card rows.

The signal processor is a basic 1-1/2 ATR size, 15.38 inches wide x 7.63 inches high x 18.10 inches long. The design is generally in accordance with the requirements of MIL-C-172. Structural and environmental design was based upon installation aboard a transport type aircraft like a C-121G. See figure 4-1 for an illustration of the basic chassis configuration.

All interface connectors are located on the front panel. Both the top and bottom covers are provided with 1/4 turn fasteners to enhance removal and reduce downtime. Access to test points on the circuit boards and module cans is provided from the top of the unit. All wiring with the exception of some RF module coax interconnects is done from the bottom. Both front and rear panels are detachable to provide easy access during wiring and/or service operations. Basic circuit card layout is divided into functional groupings. As indicated in figure 4-1, the boards are separated into three rows with honeycomb sections between rows providing RF protection. In addition, metallic shields are located between individual boards to provide increased isolation.

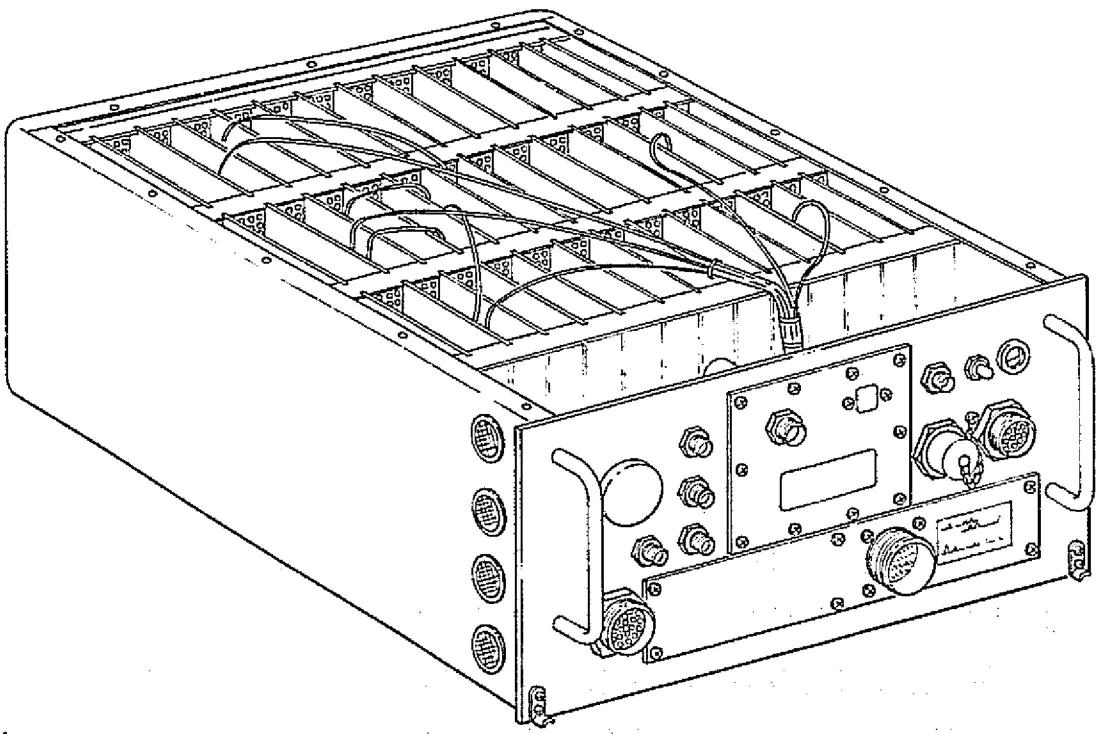

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Figure 4-1. Basic Signal Processor Chassis Configuration

4.3.1 PRINTED CIRCUIT SUBASSEMBLIES

The internal board rack is divided into three sections separated from each other by the honeycomb partitions. Each section is further divided into functional groupings of printed circuit board separated by RF shields. Packaging of the circuit elements makes broad use of microelectronic techniques. The circuit boards, supported in the case by means of metallic card slides, plugged into printed circuit edge connectors located on the connector plate at the bottom of the unit. All like voltages are assigned the same pin location for all circuit boards and connectors. All circuit boards are 4.00 inches by 6.00 inches with 50 edge contacts for input-output power and signal connections. In addition, each card will have an edge contact at the top which provides 20 test-point connections.

There are basically two types of printed circuit board subassemblies. The first type is a multilayer (4 layers) printed circuit board used where the design dictates the use of ground and voltage planes or high density layouts to minimize influence from the surrounding environment. The second type is a 2-layer board in a universal configuration where all the circuits are point-to-point wired. This second technique is cost effective for low quantity fabrication (1-6 pieces), is suitable for most logic circuits and lends itself to easy modification during checkout and system integration.

4.4 CONTROL PANEL

The control panels contain the mode control switches and indicator lights. All components are mounted on a front plate designed for 19-inch rack mount installation. A dust cover box mounts on the rear of the panel.

Pertinent mechanical specifications include:

Size	19.0W x 10.47H x 4.1L
Cooling	Natural convection
Weight	6 lbs
Construction	Aluminum

4.5 SIGNAL MONITOR PANEL

The Signal Monitor Panels contain the baseband input/output signal interface jacks and signal monitor jacks. Two rows of banana jacks with adjacent label strips provide flexibility for system test connections. The jacks are mounted on a front plate designed for 19-inch rack mount installation. A dust cover box mounts on the rear of the panel.

Pertinent mechanical specifications include:

Size	19.0W x 5.22H x 4.1L
Cooling	None
Weight	3 lbs
Construction	Aluminum

4.6 POWER SUPPLY

The power supply chassis provide the DC voltages for the other system units. The prime power requirements are as follows:

Voltage:	115 vac
Current:	8 amps, max.
Frequency:	60-400 Hz
Phases:	Single phase

The power supply output potentials are as follows:

+28 vdc
+15 vdc
-15 vdc
+ 5 vdc

The power supply chassis is 15.38 inches wide x 10.69 inches high x 18.10 inches long. Structural and environmental design is based upon installation aboard a transport type aircraft. Basically, this unit is constructed of sheet aluminum with stiffening devices to support module weight. Since prepackaged power supply modules are used, wiring is accessible from the bottom of the unit. Each module has a forced-air heat exchanger which extends into the air plenum. A standard holddown arrangement is provided for mounting in an MS 91405 type mounting tray. Both top and bottom covers are provided with 1/4 turn fasteners to expedite installation and maintenance.

Pertinent mechanical specifications for the MMT/MTAR Power Supply include:

Size	15.38W x 10.00H x 19.56L
Cooling	Forced Air convection
Weight	65 lbs
Construction	Sheet aluminum riveted assembly

The front panel contains two hardwire connectors to interface with the Signal Processor and Receiver-Transmitter assemblies. A third hardwire connector is used to input prime power. A prime power fuse is located on the front panel. Each power supply output potential is protected with a resettable fuse also located on the front panel.

The cooling technique used for the power supplies is illustrated in figure 4-2. A single 115 vac fan forces air from the rear of the assembly, through module heat sinks and out air exhaust holes located along the front sides of the chassis.

4.7 ENVIRONMENTAL CONSIDERATIONS

The TDRSS multimode transponder equipment has been designed to meet the functional requirements, when exposed to the service condition environments specified in table 4-2.

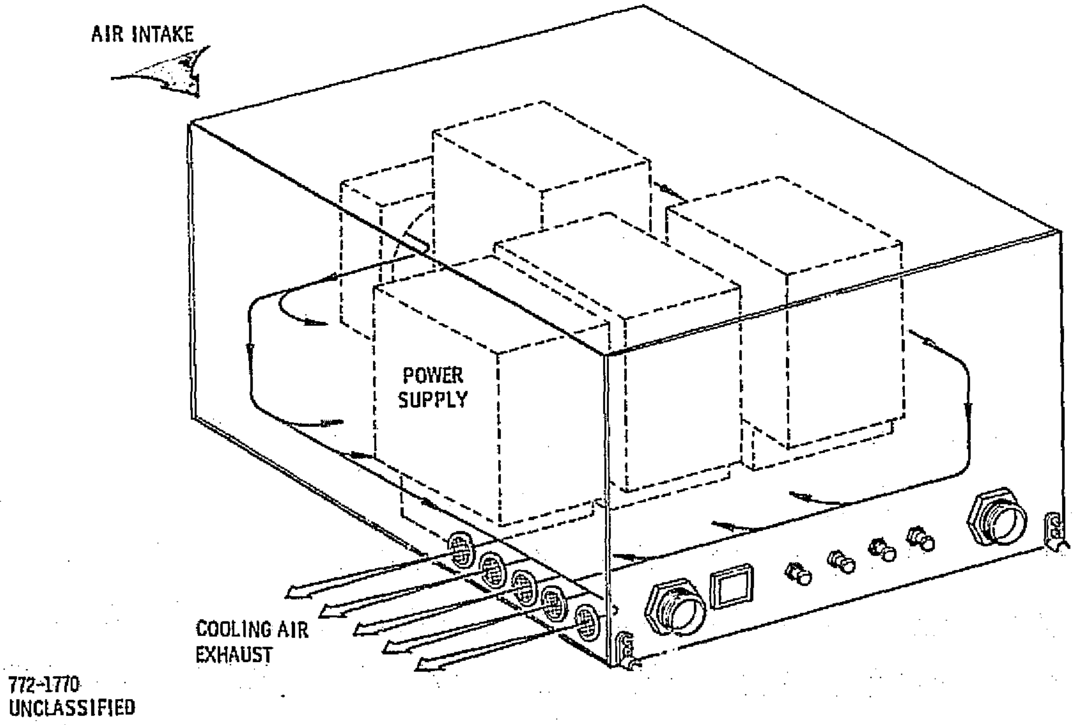

Figure 4-2. Power Supply Cooling Technique

Table 4-2. Environmental Service Conditions

Environment	STRESS LEVEL	
	Operating	Non-Operating
Thermal	32°F (0°C) to 122°F (50°C)	-25°F (-32°C) to 158F (65°C)
Relative Humidity	As low as 5% at 122°F (50°C); As High as 100% at All Temperatures From 32°F (0°C) to 85°F With Condensation At All Temperatures Lower Than 85°F (29°C)	Same as operating
Altitude	Up to 10,000 Feet Above Sea Level	Up to 25,000 Feet Above Sea Level
Vibration	5 Hz to 30 Hz: .02 inch double amplitude 30 Hz to 500 Hz: 1g	
Shock	As Encountered During Bench Handling	

4.7.1 ELECTROMAGNETIC INTERFERENCE

The equipment was designed to operate satisfactorily in the intended installations without experiencing or creating abnormal EMI conditions. To accomplish this objective, care was taken to conform to established EMI/RFI design practices. Shielded components were connected via feed-through filters and coax lines.

Where RFI shielding was required in the board rack, a conductive plate was installed between boards with grounding provided by conductive bonding along the sides. As was noted earlier, the honeycomb sections in the signal processor units provide RFI protection between the rows of circuit boards while allowing a relatively unimpeded flow of cooling air from the forced-air cooling source.

Separate ground busses were maintained for signal neutral and case grounds. Provision was made to tie these busses to case ground inside the equipment. Potential sources of high-level interference and parasitics such as frequency dividers, local oscillators and circuits sensitive to interference were individually packaged in their own shielded cases. Shielding at the chassis level was accomplished by utilizing overlapping riveted joints and oriented wire-silicone rubber gaskets at the top and bottom covers.

4.7.2 THERMAL CONSIDERATIONS

The cooling design was based on satisfying the requirements for installation in a transport aircraft of the C-121G type. Since the quality of the cooling air (cabin air) is suitable for direct flow through the electronics, a simple fan-filter assembly attached to the rear of both the signal processor and power supply was all that was required. Cooling air therefore enters the enclosures at the rear and exhausts at the sides just behind the front panel. No air passes directly out the front of the boxes where it could cause discomfort to an operator.

Honeycomb partitions allow free passage of air through the Signal Processor electronics. Power dissipation in the Signal Processor is approximately 125 watts. By using a fan which is rated at 110 CFM at free delivery, the airstream temperature rise does not exceed 5 degrees C.

4.8 MAINTAINABILITY

In the Signal Processor, virtually all circuitry is packaged on plug-in printed circuit boards. Removal of the top cover provides access to all boards in the rack. Test points are provided along the top edge of most boards to assist in fault isolation. All circuit boards plug into edge connectors located in the lower portion of the case. Faulty boards can, therefore, be simply extracted and replaced. Removal of the bottom cover permits access to the connector back-plane wiring and the main wiring harness. Both covers utilize quick-turn fasteners to facilitate openings and closings. Since each module in the Power Supply is a self-contained unit, maintainability problems are minimized.

Removal of the Receiver-Transmitter unit cover (which also utilizes quick-turn fasteners) provides ready access to all elements of the electronics. Removal of the Control Display unit dust cover provides access to all components.

SECTION V
EQUIPMENT CHARACTERISTICS AND PERFORMANCE

This section contains a description of the electrical characteristics of the Multimode Transponder equipment. It sets forth the technical specification to which the equipment was designed and includes a copy of the raw test data taken during acceptance testing at Applied Physics Laboratories in October 1975.

5.1 EQUIPMENT SPECIFICATION

The technical requirements for the MMT and MTAR equipments (the two major equipment groups of the Multimode Transponder equipment) are presented in this section. These technical requirements were updated from the original contract Statement-of-Work to include all contract modifications prior to delivery of equipment. The final modified configuration of the equipment is designed for use in a series of laboratory tests in which the MMT operates at S-band and the MTAR interfaces to the TDRSS simulation equipment at VHF/UHF frequencies. The MTAR also operates at S-band for back-to-back performance evaluation.

5.2 TECHNICAL REQUIREMENTS FOR THE MMT

5.2.1 RECEIVER NOISE FIGURE

The receiver noise figure shall not exceed 5 dB.

5.2.2 SELECTIVITY

The image rejection shall be at least 60 dB. Rejection of interfering signals more than 1.5 bandwidths away from the center frequency shall be at least 40 dB.

5.2.3 INPUTS

The inputs to the transponder will be S-band command and ranging signals, telemetry data, clock signals, power, and operational housekeeping commands. The contractor shall supply simulators for necessary input signals which would normally be generated by the user spacecraft. Mode control and other transponder controls shall be provided by a contractor supplied control panel.

5.2.3.1 S-Band Signals

The MMT will operate as a coherent transponder with a 2287.5 MHz center frequency for transmission and a 2106.40625 MHz center frequency for reception. All signal L.O. frequencies for the transponder shall be coherently synthesized from a single tracking 10 MHz VCO.

5.2.3.2 Command Signals

In all modes of operation except during the frequently hop preamble the transponder shall accept command signals from the ground and relayed through the relay satellite at rates of 234.375 BPS, 468.75 BPS or 937.5 BPS. These data rates enable the digital data to be synchronous with the PN code in SQPN mode. Provisions shall be made for switching between bit rates on the multimode transponder control panel.

5.2.3.3 Telemetry Data

In all modes of operation, the transponder shall accept telemetry data for transmission to the ground over the return link in the form of a binary bit stream at discrete rates of 937.5 BPS, 10 KBPS, 30 KBPS or 80 KBPS. Provision is made for either single or dual data transmission in the SQPN mode over the return link. Provisions shall be made for selecting a particular rate by manual selection at the control panel. Capability shall be incorporated on the return link to pass digital data that is asynchronous with the PN code.

5.2.3.4 Voice Coding

A voice channel shall be incorporated into the transponder with all modes of operation. Pulse Duration Modulation technique shall be used. A qualitative voice test for acceptable intelligibility at threshold operation will be performed.

5.2.3.5 Convolutional Encoding

Convolutional encoding shall be incorporated on the return link for the 937.5 BPS, 10 KBPS and 30 KBPS data rates. The encoding will be rate 1/2 with constraint length seven. The convolutional encoding shall be switched in and out by manual control.

5.2.3.6 Power

The Multimode Transponder is to operate properly when supplied power from a 58 Hz to 62 Hz source at 115 volts ±10%.

5.2.4 OUTPUTS

The outputs of the transponder will be S-Band telemetry data and simulated user spacecraft commands.

5.2.4.1 S-Band Signals

The transmitter shall provide an S-Band output signal level of -25 dBm nominal into a 50 ohm resistive load.

5.2.4.2 Ranging Signals

The transponder, when interrogated over the forward link by a received ranging signal, shall process this signal and retransmit over the return link a ranging signal suitable for the determination of system range and range rate at the ground station. The ranging system resolution in the absence of any communications channel noise (near infinite signal to noise ratio) shall allow range determination with a maximum systematic error of 2.0 m and a maximum rms random error of 1.0 m, and shall allow determination of range rate with a maximum systematic error of 0.1 cm/sec and a maximum rms random error of 0.1 cm/sec.

5.2.4.3 Command Signals

The transponder shall demodulate the received command signal and deliver the resulting signal to an MX-270 for bit error rate measurement at specified link signal conditions.

5.2.5 MODES OF OPERATION

The transponder shall be capable of operating in two modes: conventional phase shift keying (PSK) and staggered quadriphase pseudorandom noise (SQPN). Provision shall be made for selecting the operating mode from the front panel.

5.2.5.1 Conventional Mode

Operation in the conventional mode for both the forward and the return links shall be in general conformance with the system planned for the GSFC Mark 1 TDRS.

5.2.5.1.1 Modulation

In the conventional mode, the modulation for both the forward and the return links shall be PSK with a phase shift of $\pm 90^{\circ}$.

5.2.5.2 SQPN Mode

Operation in the SQPN mode, for both the forward and the return links, shall be in general conformance with the system planned for the GSFC Mark 1 TDRS. The SQPN mode shall be usable for receiving commands and ranging signals over the forward link, and for transmitting telemetry data and ranging signals over the return link.

5.2.5.2.1 Frequency Hop Preamble

A frequency hop preamble is incorporated in the forward link for signal acquisition. The frequency hop code length equals 2^8 hop chips and the rate equals $2^8/2^{18}$ X PN chip rate.

5.2.5.2.2 PN Code

The pseudonoise code length shall be 2^{18} chips at a 2.56 MCPS rate for transpond mode on both forward and return links. In the "Return Only" mode provided for the return link the PN code length is 2^{15} chips at a 2.56 MCPS rate.

5.2.5.2.3 Multiple Access

Consideration shall be given to the requirement that several user spacecraft utilize the same carrier frequency for the return link simultaneously, discrimination between signals being achieved by the use of orthogonal or quasi-orthogonal coding and of proper address codes.

5.2.6 TEST EQUIPMENT

The contractor shall supply two MX 270 Bit Error Rate Analyzers for the purpose of (1) generating the required data rates, or (2) for measuring received data error rates.

5.3 TECHNICAL REQUIREMENTS FOR THE MTAR

5.3.1 INTRODUCTION

The MTAR is to perform the same function radio communication wise as the conceptual transmitter and receiver aboard the TDRS. However, their principal function is to supply to and receive signals from the multimode transponder in a number of test configurations in which the MTAR is always ground based. The MTAR is to be fully compatible with the Multimode Transponder. Since this equipment is to be utilized in engineering tests only, it is to be fabricated using the best commercial practices.

The transmitter will supply a signal in the frequency band utilized by the multimode transponder at a level of -25 dBm into a 50 ohm load which represents an antenna. This signal shall be capable of being modulated according to the following modes of operation:

a. Staggered quadriphase pseudonoise (SQPN) in which two PN streams are modulo-two added with NRZ data and then balance modulated on two RF carriers phase shifted 90° from each other. The two resultant biphase signals are then summed to produce a quadriphase output.

b. Conventional mode (PSK) in which NRZ data modulates the carrier as PSK in a straightforward manner.

In the PN mode the PN code must have good auto- and cross-correlation properties so that the correlation hash-out of the correlator in the multimode transponder will cause a minimum false alarm rate before synchronization is established. Measurement of range will be facilitated by measuring the transit time of code sequences. Additional ambiguity resolution, if required, will be supplied by the channel. Range is determined to a resolution corresponding to a small fraction of PN bit (chip).

In the PN mode, pulses derived from the all-ones vector in the transmitted signal and the all-ones vector in the received and demodulated signal together with auxiliary range ambiguity signals from the data channel will be accessible to the peripheral equipment.

5.3.2 ELECTRICAL SPECIFICATIONS

5.3.2.1 Transmitter Signal Stability

The phase, amplitude and frequency stability of the transmitter signals and the modulation thereon shall be, in the absence of any type of interfering signal including additive channel noise, sufficient to accomplish the following:

a. Supply command data to the Mutlimode Transponder (MMT) with a 30 dB SNR over the dyanmic range of the system.

b. Supply range signals to the MMT which when processed by the MMT and returned to the ground receiver will cause a range uncertainty of 1.0 meter maximum in a one-second averaging time.

c. Supply signal which can be synthesized back to the original carrier component in the MMT and subsequently at the output of the ground receiver sufficient to providing a range rate signal having an uncertainty of 0.1 cm maximum in 10 seconds averaging time.

5.3.2.2 Transmission Power Levels

The ground transmitter shall be capable, in the SQPN and PSK modes, of supplying -25 dBm at S-Band into a 50 ohm load. A transmit signal level of -4 dBm at 401 MHz is provided for the interface to laboratory equipment.

The transmitter output level shall be capable of being reduced by 30 dB in 1 dB steps or in a continuously variable fashion calibrated to 1 dB.

5.3.2.3 Transmitter Output Frequency

The frequency of transmission shall be compatible with the Multimode Transponder.

5.3.2.4 Transmitter Signal Formats and Modulation

The ground transmitter will supply a data clock signal to the data source. (MX-270) The data source is to supply NRZ data of various types including a random bit stream to the ground transmitter.

5.3.2.4.1 SQPN Mode

In the SQPN mode the digital data stream is modulo-2 added to two PN codes and then balance modulated on two RF carriers which are summed to produce the staggered quadriphase signal.

5.3.2.4.2 PSK Mode (Conventional)

In the PSK mode the input data stream PSK modulates directly a carrier component such that the result is DPSK. The baseband modulation signal in all modes is to be applied to an external connector for purposes of interfacing with other transmitters.

5.3.2.4.3 Frequency Hop Preamble

A frequency hop preamble is incorporated in the forward link for signal acquisition. The frequency hop code length equals 2^8 hop chips and the rate equals $2^8/2^{18}$ X PN chip rate.

5.3.2.5 PN Code

The PN code generated in the ground transmitter shall be fully compatible with the requirements for the Multimode Transponder. The pseudonoise code length shall be 2^{18} chips at a 2.56 MCPS rate for transpond mode on both forward and return links. In the "Return Only" mode provided for the return link the PN code length is 2^{15} chips at a 2.56 MCPS rate.

5.3.2.6 Equipment Interface

Front panel access on the MTAR shall be provided for the first IF of the receiver (137 MHz) and transmitter (401 MHz) for signal interface with the AGIPA system. The MTAR shall provide the 10.75 MHz SQPN correlator reference signal for the AGIPA demultiplexer at a nominal signal level of -10 dBm into a 50 ohm load. The MTAR will provide a data clock and "receiver sync" signals at TTL levels to the AGIPA equipment.

5.3.2.7 Receiving System Sensitivity (All Modes)

The system being simulated here, i.e., User Spacecraft/TDRS S-Band communication links, will have at times, because of RFI and multipath, a negative communication margin. Therefore, it is required that the ground receiver system have both an acquisition and operating sensitivity which is close to the theoretical optimum. Because the Multimode Transponder will code its transmitted signal with forward error control the theoretically optimum sensitivity in the data link for a bit error (BER) of 10^{-5} is specified as: $E/N_0 = 5$ dB where N_0 includes all extraneous signals including receiver noise, sky noise, RFI, and multipath effects. The sensitivity of the ground receiver shall be within 2 dB of the theoretical optimum for both acquisition and operation based upon the E/N_0 relationship as described above over the dynamic range of the receiver (specified below).

5.3.2.8 Receiver Dynamic Range

In the forward link at the minimum data rate of 234.375 BPS (without encoding) and system noise figure of 5 dB the threshold signal level is -133 dBm. In the return link at the minimum data rate of 937.5 BPS the threshold signal level is -132 dBm with encoding and -127 dBm without encoding. The dynamic range of the receiver shall extend from -100 dBm to the minimum signal level at the selected data rate.

5.3.2.9 Acquisition Time of the Ground Receiver

The acquisition time for the PN mode without diversity, shall be a maximum of 50 seconds with a desired acquisition time being ten seconds or less at all received signals and formats where the system, after acquisition, can output data with a bit error rate (BER) no greater than 10^{-5}.

5.3.2.10 Acquisition with Doppler

Correction for up to ±60 kHz doppler offset is manually entered at the MTAR for both forward and return links. The receiver is designed to search out ±3 kHz of frequency uncertainty.

5.3.2.11 Ground Receiver and Signal Processor Bandwidths

The bandwidths involved with the ground receiving function are to be compatible with the signal emitted by the Multimode Transponder for the various modes.

5.3.2.12 Data Output

The received and demodulated data stream shall be applied to a connector for external accessibility. The voltage level of this data stream shall be the standard logic format utilized throughout the system. It is assumed for the PN mode that throughout the MTAR and Multimode Transponder the data rate is coherent with the PN sequence rate such that bit synchronization is readily available once code synchronization is established. The contractor shall utilize the coherency in establishing bit synchronization. In addition capability shall be incorporated on the return link to pass digital data that is asynchronous with the PN code. Selection of synchronous or asynchronous data mode is made with a front panel switch.

5.3.2.13 Range Signals (PN Mode)

The range signals will be supplied in the form of start and stop pulses. These signals are fed into an internal counter equipped with a printer such that a tabulation of two-way range in seconds is produced. Multiplying these numbers by a determinable constant results in the actual range. The gate start pulse is derived from the all-ones condition in the ground transmitter. The gate stop pulse is derived from the all-ones condition of the local PN code signal which is synchronized through a 1 Hz code tracking bandwidth to the received PN code signal.

5.4 TEST DATA

The following pages are a copy of the actual test data taken during acceptance testing at Appli..d Physics Laboratories, Laurel, Maryland.

APPLICATION		REVISIONS			
NEXT ASSY	USED ON	LTR.	DESCRIPTION	DATE	APPROVED

PRECEDING PAGE BLANK NOT FILMED

ACCEPTANCE TEST DATA SHEET

Assembly Drawing No. 705612

SERIAL NO. OF TEST ITEM ____________

Acceptance Test Procedure No. 977140

ORIGINAL PAGE IS OF POOR QUALITY

PROD. TESTER ____________ Date ________

R & Q A Approval ____________ Date ________

DOD QAR Approval ____________ Date ________

REV																									
SHEET	27	28	29	30	31	32	33	34																	

REV STATUS OF SHEETS	REV																									
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26

ORIGN	J. Mackey 7/25/75
CHK	
APVD	
APVD	
APVD	
CONTR. DEGN. APPVL.	
GOVT. CONTR. NO.	
GOVT ACTIVITY APPROVAL	

Magnavox RESEARCH LABORATORIES TORRANCE, CALIFORNIA

S-BAND TDRS MULTIMODE TRANSPONDER

SIZE	CODE IDENT NO	DRAWING NO
A	12813	977141
SCALE	DWG LEVEL	SHEET 1 OF 24

SUBJECT: S-BAND TDRS MULTIMODE TRANSPONDER

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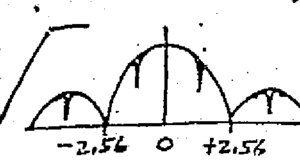
6.1	MODES OF OPERATION	STATUS
6.1.1	Modulation	OK
	PN Modulation	OK
	Frequency HOP Preamble	OK
	PSK Modulation	OK
6.1.2	RF Frequencies	



Nulls @ ±1.25MHz appear in PN spectrum. This is ½ PN Chip Rate. ? Why?

	FREQUENCY
MMT (J11)	TX Att. set to 0dB Non-Coherent Mode Data OFF f = 2287.507 MHz
MTAR (J11)	TX Att. set to 0dB Non-Coherent Mode Data OFF f = 2106.412
MTAR (J8)	f = 401.001040 MHz

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6.1.3 Data Rates

MTAR DATA RATE SELECTED	DATA CLOCK RATE Measured @ MTAR Test Panel: "TX CLK OUT"
234.375 BPS	234.4 Hz
468.75 BPS	468.8 Hz
937.5 BPS	937.5 Hz

MMT DATA RATE SELECTED	DATA CLOCK RATE Measured @ MMT Test Panel: "1XCLK1 OUT"
937.5 BPS	937.5 Hz
10 K BPS	10.0001 KHz
30 K BPS	30.0001 KHz
80 K BPS	80.0004 KHz

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6.1.4 PN Code Rates

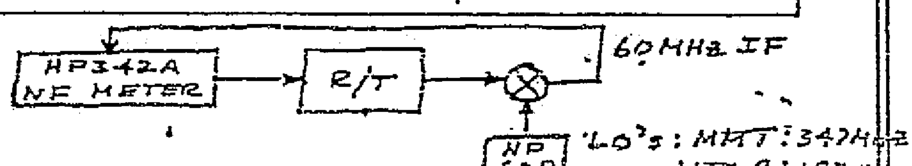
	CODE CLOCK RATE
MMT	Measured @ CODER BOARD #1 Location 2A06 – Pin 2A f = 2.560014 MHz
MTAR	Measured @ CODER BOARD #2 Location 2B07 – Pin 2A f = 2.560040 MHz

6.2 RECEIVER CHARACTERISTICS

6.2.1 Noise Figure

	NOISE FIGURE (dB)
MMT	4.5 dB
MTAR	4.8 dB

NF TEST SETUP:



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6.2.2 Receiver Selectivity

Measured by HP Spectrum Analyzer (RF Section - 8553L)

		FREQUENCY (MHz)			
		1 dB	3 dB	6 dB	~~40 dB~~ ~25dB*
MTAR $f_c = 12MHz$ $BW_{3dB} \sim 5.8MHz$	f_H	13.6	15.0	16.0	19.4
	f_L	9.5	9.2	8.5	5.0
MMT $f_c = 16.25MHz$ $BW_{3dB} \sim 8.0MHz$	f_H	19.25	20.25	21.25	26.25
	f_L	14.25	12.25	11.25	5.25

* Measurement limited by thermal noise level.

6.2.3 Image Rejection

CHANNEL FREQUENCY	IMAGE FREQUENCY	IMAGE REJECTION* (dB)
MTAR 2287.5 MHz	2013.5 MHz	>80dB
MMT 2106.40625 MHz	1304.40625 MHz	>80dB

*Note: Input to MTAR limited to -30dBm to avoid front-end damage.

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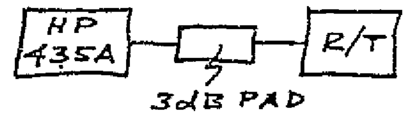
6.3 TRANSMITTER CHARACTERISTICS

6.3.1a Transmit Power – MTAR

Test Setup:



RT J10		TRANSMIT OUTPUT [dBm]			
		0 dB attn.	3 dB attn.	10 dB attn.	20 dB attn.
MTAR ~~MMT~~	PSK	-20.0	-23.4	-30*	-40*
	SQPN	-20.0	-23.4	-30*	-40*

*Measured on Spectrum Analyzer

RT J11		MONITOR OUTPUT [dBm]			
		0 dB attn.	3 dB attn.	10 dB attn.	20 dB attn.
MTAR	PSK	+2.2	-0.8	-7.4	-17.4
	SQPN	+2.1	-0.9	-7.5	-17.5

ACCEPTANCE TEST DATA SHEET

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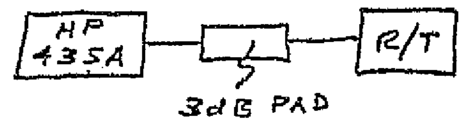
6.3 TRANSMITTER CHARACTERISTICS

Test Setup:



6.3.1 b. Transmit Power - MMT

RT J10		TRANSMIT OUTPUT [dBm]			
		0 dB attn.	3 dB attn.	10 dB attn.	20 dB attn.
MMT	PSK	-11.0	-13.7	-21.2	-31.2*
	SQPN	-10.8	-13.5	-21.0	-31.0*

*Measured on Spectrum Analyzer

RT J11		MONITOR OUTPUT [dBm]			
		0 dB attn.	3 dB attn.	10 dB attn.	20 dB attn.
MMT ~~MTAR~~	PSK	+11.8	+9.4	+2.7	-7.2
	SQPN	+12.0	+9.6	+3.0	-7.0

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6.3.2 Spurious Noise Output

		SPURIOUS OUTPUT LEVEL (dB) [dB below fundamental]
MTAR	401 MHz (J12)	0 dB Reference: 401 MHz → -17 dBm 802 (2nd. harm.): 30 dB 401 ± 0.7 MHz : 45 dB 401 ± 2.8 MHz : 50 dB
MTAR	2106.40625 MHz ~~2287.5 MHz~~ ~~(J12)~~ (J10)	0 dB Reference: 2106.40625 MHz → -20 dBm 2106.4 ± 3 MHz : 38 dB " ± 0.5 MHz : 35 dB " ± 240 KHz : 45 dB " ± 100 KHz : 36 dB
MMT	137 MHz (J12)	0 dB Reference: 137 MHz → +1.5 dBm 274 (2nd. harm.): 20 dB 137 ± 4.5 MHz : 54 dB ± 2.6 MHz : 48 dB ± 240 KHz : 54 dB
MMT	2287.5 MHz ~~2106.40625 MHz~~ (J10)	0 dB Reference: 2287.5 MHz → -11 dBm 2287.5 ± 7.0 MHz : 53 dB ± 4.5 MHz : 53 dB ± 2.7 MHz : 48 dB ± 70 KHz : 45 dB

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TEST RUN AT 10^{-5} BER C/N SPEC. ADDITIONALLY, ACTUAL THRESHOLD (TH) WAS DETERMINED REGARDLESS OF BER.

6.4 SIGNAL ACQUISITION

Note: — Indicates "Did Not Acquire"
SP.: ATP Specification
TH: Actual Threshold

CASE	SIGNAL LEVEL [dBm]	SUCCESSES/3 TRIALS	ACQUISITION TIME [sec.]
937.5 BPS PSK I	−124 (SP) −132 −133 −134 (TH)	3/3 3/3 3/3 2/3	1.5, 5, 5 3, 2.5, 5 4, 6, 7 20, 11, —
234.375 BPS SQPN II	−130 (SP) −131 (TH) −132	3/3 2/3 0/3	25, 18, 24 20, —, 25 —, —, —
937.5 BPS SQPN III	−124 (SP) −125 (TH) −126	2/3 2/3 0/3	8, 8, — 10, —, 8 —, —, —
30 KBPS PSK IV*	−109 (SP) −117 −118 (TH) −119	3/3 3/3 2/3 0/3	4, 6, 5 3, 4, 5 1, 20, — —, —, —
937.5 BPS PSK V	−124 (SP) −128 −129 −130 (TH) −131	3/3 3/3 3/3 3/3 1/3	6, 6, 6 3, 7, 22 11, 5, 5 4, 4, 5 —, —, 6
30 KBPS SQPN VI* RETURN ONLY	−109 (SP) −122 −123 (TH) −124	3/3 3/3 2/2 0/2	Maximum Acq. times CI's set off by max. t.: 4 min 50 sec, 4'45", 3'57" 4'50", 4'20", 4'30" 4'58", 4'44" —, —

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* ACQUISITION WITH DATA OFF.

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6.5 DATA DEMODULATION

6.5.1 Forward Link

PSK

DATA RATE	C/N_0 (dB)	SIGNAL LEVEL (dBm)	ERROR RATE	SAMPLE TIME
234.375 BPS	~~38~~ 39	-130	0	7.1 min. 10^5 Blocks
	~~37~~ 38	-131	0	
	~~36~~ 37	-132	1.7×10^{-4} 1.5×10^{-4} 2.1×10^{-4}	
	~~35~~ 36	-133	5.0×10^{-4} 8.2×10^{-4} 4.0×10^{-4}	
	~~34~~ 35	-134	1.4×10^{-3} 1.4×10^{-3} 1.1×10^{-3}	
	~~33~~ 34	-135	4.25×10^{-3} 4.72×10^{-3} 4.52×10^{-3}	
	~~32~~ 33			

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6.5.1 Forward Link (Cont.)

PSK

DATA RATE	C/N_0 (dB)	SIGNAL LEVEL (dBm)	ERROR RATE	SAMPLE TIME
468.75 BPS	41	-128	0	3.55 min. 10^5 Blocks
	40	-129	0	
	39	-130	1.3×10^{-4} 0.8×10^{-4} 0.6×10^{-4}	
	38	-131	1.02×10^{-3} 6.4×10^{-4} 7.2×10^{-4}	
	37	-132	2.02×10^{-3} 1.65×10^{-3} 1.82×10^{-3}	
	36	-133	6.49×10^{-3} 6.66×10^{-3} 7.54×10^{-3}	
	35			

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6.5.1 Forward Link (Cont.)

PSK

DATA RATE	C/N_0 (dB)	SIGNAL LEVEL (dBm)	ERROR RATE	SAMPLE TIME
937.5 BPS	44			1.78 min. 10⁵ Blocks
	43	-126	0	
	42	-127	0.4×10^{-4} 0.2×10^{-4} 0.8×10^{-4}	
	41	-128	1.2×10^{-4} 1.2×10^{-4} 3.2×10^{-4}	
	40	-129	10.4×10^{-4} 7.6×10^{-4} 8.4×10^{-4}	
	39	-130	2.15×10^{-3} 2.54×10^{-3} 2.47×10^{-3}	
	38	-131	7.33×10^{-3} 8.32×10^{-3} 8.59×10^{-3}	

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6.5.1 Forward Link (Cont.)

SQPN

DATA RATE	C/N_0 (dB)	SIGNAL LEVEL (dBm)	ERROR RATE	SAMPLE TIME
234.375 BPS	~~38~~ 40	−129	0	7.1 min. 10^5 Blocks
	~~37~~ 39	−130	0.9×10^{-4} 0.7×10^{-4} 0.4×10^{-4}	All Single Errors (VCO Loop slips)
	~~36~~ 38	−131	1.3×10^{-4} 0.9×10^{-4} 1.3×10^{-4}	
	~~35~~ 37	−132	3.3×10^{-4} 2.4×10^{-4} 3.1×10^{-4}	
	~~34~~ 36	−133	6.0×10^{-4} 7.1×10^{-4} 7.4×10^{-4}	
	~~33~~ 35	−134	2.16×10^{-3} 2.02×10^{-3} 2.45×10^{-3}	
	~~32~~ 34	−135	6.47×10^{-3} 7.21×10^{-3} 6.89×10^{-3}	
468.75 BPS	41	−128	0	3.55 min. 10^5 Blocks
	40	−129	0.7×10^{-4} 1.2×10^{-4} 1.0×10^{-4}	)
	39	−130	1.7×10^{-4} 1.5×10^{-4} 1.4×10^{-4}	
	38	−131	7.0×10^{-4} 8.8×10^{-4} 7.7×10^{-4}	
	37	−132	2.08×10^{-3} 2.06×10^{-3} 2.58×10^{-3}	
	36	−133	7.75×10^{-3} 7.05×10^{-3} 8.12×10^{-3}	
	35			

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6.5.1 Forward Link (Cont.)

SQPN (~1dB Loss vs. PSK – See pg. 11)

DATA RATE	C/N_0 (dB)	SIGNAL LEVEL (dBm)	ERROR RATE	SAMPLE TIME
937.5 BPS	44	−125	0 0.2×10^{-4} 0	1.78 min. 10^5 Blocks
	43	−126	0.4×10^{-4} 1.0×10^{-4} 1.4×10^{-4}	
	42	−127	3.8×10^{-4} 2.8×10^{-4} 2.8×10^{-4}	
HAD TO REMOVE DATA TO ACQ. IN SQPN →	41	−128	1.55×10^{-3} 1.60×10^{-3} 1.72×10^{-3}	
	40	−129	5.40×10^{-3} 4.62×10^{-3} 4.92×10^{-3}	
	39	−130	7.87×10^{-3} 7.28×10^{-3} 6.90×10^{-3}	
	38	−131		

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6.5.2 Return Link

PSK

DATA RATE	C/N_0 (dB)	SIGNAL LEVEL (dBm)	ERROR RATE	SAMPLE TIME
937.5 BPS	~~44~~ 43	-126	0	1.78 min. 10^5 Blocks
	~~43~~ 42	-127	0	
~10dB	~~42~~ 41	-128	0.8×10^{-4} 0.8×10^{-4} 0.4×10^{-4}	
	~~41~~ 40	-129	3.0×10^{-4} 3.4×10^{-4} 2.2×10^{-4}	
	~~40~~ 39	-130	7.4×10^{-4} 8.8×10^{-4} 9.0×10^{-4}	
	~~39~~ 38	-131	3.04×10^{-3} 4.38×10^{-3} 3.74×10^{-3}	
	~~38~~ 37	-132	9.64×10^{-3} 9.31×10^{-3} 8.08×10^{-3}	
10 K BPS	~~54~~ 53	-116	0	100 sec. 10^6 Blocks
	~~53~~ 52	-117	0.6×10^{-5} 0.2×10^{-5} 1.4×10^{-5}	
	~~52~~ 51	-118	8.8×10^{-5} 4.9×10^{-5} 7.4×10^{-5}	
	~~51~~ 50	-119	5.76×10^{-4} 4.94×10^{-4} 6.14×10^{-4}	
	~~50~~ 49	-120	1.69×10^{-3} 1.74×10^{-3} 1.73×10^{-3}	
	~~49~~ 48	-121		
	~~48~~ 47			

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6.5.2 Return Link (Cont.)

PSK

DATA RATE	C/N_0 (dB)	SIGNAL LEVEL (dBm)	ERROR RATE	SAMPLE TIME
30 K BPS	59	−110	0	33 sec. 10^6 Blocks
	58	−111	0 0.2×10^{-5} 0	→ 1 Error
	57	−112	1.2×10^{-5} 6.4×10^{-5} 6.6×10^{-5}	
	56	−113	3.6×10^{-5} 6.6×10^{-5} 5.6×10^{-5}	
~4.5 dB vs. 4.2 dB BW Change	55	−114	2.98×10^{-4} 2.20×10^{-4} 2.80×10^{-4}	
	54	−115	1.05×10^{-3} 1.05×10^{-3} 1.06×10^{-3}	
	53	−116		—
80 K BPS	63	−106	0	12.5 sec. 10^6 Blocks
	62	−107	0.4×10^{-5} 0.6×10^{-5} 0.2×10^{-5}	)
	61	−108	1.8×10^{-5} 3.2×10^{-5} 1.6×10^{-5}	
	60	−109	1.32×10^{-4} 1.44×10^{-4} 1.52×10^{-4}	
	59	−110	6.10×10^{-4} 6.64×10^{-4} 6.40×10^{-4}	
	58	−111	2.22×10^{-3} 2.11×10^{-3} 2.06×10^{-3}	
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6.5.2 Return Link (Cont.)

SQPN

DATA RATE	C/N_0 (dB)	SIGNAL LEVEL: (dBm)	ERROR RATE	SAMPLE TIME
937.5 BPS	~~44~~ 42	−127	0	1.78 min. 10^5 Blocks
	~~43~~ 41	−128	1.0×10^{-4} 0.6×10^{-4} 0.6×10^{-4}	
	~~42~~ 40	−129	3.6×10^{-4} 4.8×10^{-4} 3.8×10^{-4}	
	~~41~~ 39	−130	8.6×10^{-4} 7.6×10^{-4} 9.0×10^{-4}	
	~~40~~ 38	−131	3.18×10^{-3} 3.32×10^{-3} 3.32×10^{-3}	
~10dB	~~39~~ 37	−132	7.58×10^{-3} 7.30×10^{-3} 7.76×10^{-3}	
	~~38~~			
10 K BPS	~~54~~ 53	−116	0	100 sec. 10^6 Blocks
	~~53~~ 52	−117	0.4×10^{-5} 1.8×10^{-5} 0.4×10^{-5}	
	~~52~~ 51	−118	8.0×10^{-5} 9.6×10^{-5} 7.0×10^{-5}	
	~~51~~ 50	−119	5.98×10^{-4} 5.82×10^{-4} 6.09×10^{-4}	
	~~50~~ 49	−120	1.02×10^{-3} 1.08×10^{-3} 1.20×10^{-3}	
	~~49~~ 48			
	~~48~~ 47			

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6.5.2 Return Link (Cont.)

SQPN

DATA RATE	C/N_0 (dB)	SIGNAL LEVEL (dBm)	ERROR RATE	SAMPLE TIME
30 K BPS	59	-110	0	33 sec. 10^6 Blocks
	58	-111	0	
	57	-112	0.6×10^{-5} 0.2×10^{-5} 0.2×10^{-5}	
	56	-113	4.6×10^{-5} 5.0×10^{-5} 5.0×10^{-5}	
	55	-114	3.79×10^{-4} 3.40×10^{-4} 3.39×10^{-4}	
~4.7dB vs. 4.2dB BW Change	54	-115	1.17×10^{-3} 1.21×10^{-3} 1.13×10^{-3}	
	53			
80 K BPS	63	-106	0	12.5 sec. 10^6 Blocks
	62	-107	0.6×10^{-5} 0 0.2×10^{-5}	
	61	-108	2.9×10^{-5} 3.4×10^{-5} 1.9×10^{-5}	
	60	-109	1.46×10^{-4} 2.22×10^{-4} 1.84×10^{-4}	
	59	-110	7.26×10^{-4} 7.34×10^{-4} 7.12×10^{-4}	
	58	-111	2.46×10^{-3} 2.46×10^{-3} 2.40×10^{-3}	
	57			

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6.5.2 Return Link (Cont.)

~~SQPN~~ RETURN ONLY

DATA RATE	C/N_0 (dB)	SIGNAL LEVEL: (dBm)	ERROR RATE	SAMPLE TIME
937.5 BPS	~~44~~ 42	-127	1.0 × 10⁻⁴ 1.5 × 10⁻⁴ 2.2 × 10⁻⁴	1.78 min. 10⁵ Blocks
	~~43~~ 41	-128	4.0 × 10⁻⁴ 4.0 × 10⁻⁴ 3.2 × 10⁻⁴	
	~~42~~ 40	-129	1.52 × 10⁻³ 7.0 × 10⁻⁴ 8.0 × 10⁻⁴	
	~~41~~ 39	-130	1.32 × 10⁻³ 1.10 × 10⁻³ 1.42 × 10⁻³	
	~~40~~ 38	-131	4.12 × 10⁻³ 4.80 × 10⁻³ 4.39 × 10⁻³	
	~~39~~ 37	-132	1.05 × 10⁻² 1.11 × 10⁻² 1.05 × 10⁻²	
	~~38~~ 36			—
10 K BPS	54	-115	0	100 sec. 10⁶ Blocks
	53	-116	0.2 × 10⁻⁵ 0 6.2 × 10⁻⁵	)
	52	-117	6.4 × 10⁻⁵ 1.6 × 10⁻⁵ 0.4 × 10⁻⁵	
	51	-118	5.0 × 10⁻⁵ 7.0 × 10⁻⁵ 9.6 × 10⁻⁵	
	50	-119	5.32 × 10⁻⁴ 4.44 × 10⁻⁴ 4.32 × 10⁻⁴	
	49	-120	1.62 × 10⁻³ 1.74 × 10⁻³ 1.68 × 10⁻³	
	48			—

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6.5.2 Return Link (Cont.)

~~PSK~~ RETURN ONLY

DATA RATE	C/N_0 (dB)	SIGNAL LEVEL (dBm)	ERROR RATE	SAMPLE TIME
30 K BPS	59	-110	0	33 sec, 10^6 Blocks
	58	-111	0	
	57	-112	0.6×10^{-5} 0.5×10^{-5} 0.6×10^{-5}	
	56	-113	5.5×10^{-5} 5.4×10^{-5} 5.4×10^{-5}	
	55	-114	3.42×10^{-4} 3.44×10^{-4} 3.36×10^{-4}	
	54	-115	1.25×10^{-3} 1.23×10^{-3} 1.27×10^{-3}	
	53			
80 K BPS	63	-106	0	12.5 sec, 10^6 Blocks
	62	-107	0.2×10^{-5} 0.2×10^{-5} 0.2×10^{-5}	
	61	-108	4.8×10^{-5} 1.6×10^{-5} 3.6×10^{-5}	
	60	-109	2.30×10^{-4} 2.14×10^{-4} 2.09×10^{-4}	
	59			
	58			
	57			

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6.6 Data Encoding

PSK

DATA RATE	C/N_0 (dB)	SIGNAL LEVEL (dBm)	ERROR RATE	SAMPLE TIME
937.5 BPS	41	-128		1.78 min. 10^5 Blocks
	40	-129		
	39	-130	0	
	38	-131	1.1×10^{-4} 0.5×10^{-4} 0.8×10^{-4}	
	37	-132	MTAR IN & OUT OF LOCK	
	36			
	35			
10 K BPS	51	-118		
	50	-119	0	
	49	-120	0	
	48	-121	1.4×10^{-5} 0.4×10^{-5} 6.4×10^{-5}	
	47	-122	1.8×10^{-5} 2.0×10^{-5} DROPPED LOCK 1.6×10^{-5}	HAD TO REACQ.
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6.6 Data Encoding (Cont.)

PSK

DATA RATE	C/N_0 (dB)	SIGNAL LEVEL (dBm)	ERROR RATE	SAMPLE TIME
30 K BPS	56	-113		33 sec. 10^6 Blocks
	55	-114	0	
	54	-115	0	
	53	-116	0	
	52	-117	0.2×10^{-5} 0.2×10^{-5} 3.4×10^{-5} 3.0×10^{-5} 0.8×10^{-5}	COMPARE TO UNCODED 30KBPS PSK @ -112 dBm
	51	-118	2.82×10^{-4} 1.82×10^{-4} 4.50×10^{-4}	
	50	-119	VITERBI DECODER IN & OUT OF SYNC	

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6.6 Data Encoding (Cont.)

SQPN

DATA RATE	C/N_0 (dB)	SIGNAL LEVEL (dBm)	ERROR RATE	SAMPLE TIME
937.5 BPS	41	-128		1.78 min. 10^5 Blocks
	40	-129	0	
	39	-130	0	
	38	-131	0.6 x 10^-4 0.8 x 10^-4 0.8 x 10^-4	
	37	-132	MTAR IN & OUT OF LOCK	
	36			
	35			
10 K BPS	51	-118		100 sec. 10^6 Blocks
	50	-119	0	
	49	-120	0	
	48	-121	0.6 x 10^-5 0 0	
	47	-122	2.8 x 10^-5 7.4 x 10^-5 2.2 x 10^-5	
	46	-123	VITERBI DECODER IN & OUT OF SYNC	
	45			

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6.6 Data Encoding (Cont.)

SQPN

DATA RATE	C/N_0 (dB)	SIGNAL LEVEL (dBm)	ERROR RATE	SAMPLE TIME
30 K BPS	56	-113		33 sec, 10^6 Blocks
	55	-114	0	
	54	-115	0	
	53	-116	0 0 0	5 dB improvement vs. Uncoded 30KBPS (See pg. 17a)
	52	-117	2.98×10^{-4} 5.6×10^{-5} 1.82×10^{-4}	
	51	-118	VITERBI DECODER & MTAR IN & OUT OF SYNC	
	50			

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6.7 VOICE MODE PERFORMANCE N/A

LINK	MODE	SIGNAL LEVEL (dBm)	C/N_0 (dB)
FORWARD	PSK		
	SQPN		
RETURN	PSK		
	SQPN		

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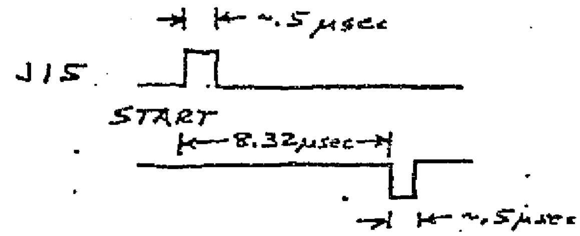
6.8 RANGE MEASUREMENT



C/N_0 (dB)	RMS ERROR (~~MICROSECONDS~~) (NANOSECONDS)	
42 dB KAY ATT. = 64dB	RMS JITTER	7.515 nsec. 7.114 nsec. 7.382 nsec.
	RANGE	8.3253 μsec. 8.3246 μsec.
82 dB KAY ATT. = 24dB	RMS JITTER	0.9275 nsec. 0.9521 nsec. 0.7720 nsec.
	RANGE	8.3264 μsec. 8.3263 μsec.

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6.9 RANGE RATE PERFORMANCE

RMS JITTER ON 80 MHZ SIGNAL @ J17 (RRI) ON MTAR SIGNAL PROCESSOR

RMS RANGE RATE ERROR

C/N_0 (dB)	RMS ERROR (Hz)
42 dB	7.5502 7.8957 7.9293 7.7087 7.5683
82 dB	7.5061 7.4335 7.4417 7.3315

AVE. FREQ. OF 80 MHZ SIGNAL @ J17 (RRI) ON MTAR SIGNAL PROCESSOR

MEAN RANGE RATE ERROR

C/N_0 (dB)	AVERAGE FREQUENCY (MHz)	
42 dB	80.000031081 .000031689 .000031828 .000032081	80.000032402 .000032927 .000033536 .000034130
82 dB	80.000033573 .000032999 .000032639 .000032151	80.000032081 .000031845 .000031582 .000031728

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SECTION VI

CONCLUSIONS

This report contains a description of the S-Band Multimode Transponder and its associated ground support and test equipment. Candidate modes of operation considered for use in an eventual tracking and data relay system were implemented in this design. System trade-off studies during Phase I identified the foreseeable technical problems of the eventual TDRSS user. The Phase II implementation and subsequent TDRSS telecommunications study resulted in a design approach to satisfy the TDRSS telecommunications performance objectives. The S-Band Multimode Transponder is the implementation of the selected configuration. Theoretical performance calculations can be verified with laboratory tests on real hardware.

The design goals for the MMT/MTAR equipment have been met. The flexibility of the equipment as a laboratory tool has been demonstrated in the TDRSS simulation testing at Applied Physics Laboratories.

6.1 MODIFICATIONS TO IMPROVE EXISTING EQUIPMENT

It is now evident, after integrating and testing the Multimode Transponder equipment, that some improvement in reliability and performance could be realized through equipment modification. These modifications are discussed in this section. Not only should these modifications be incorporated into the existing Multimode Transponder equipment, but they should be considered for inclusion into future TDRSS User Satellite equipment.

6.1.1 CORRELATION FREQUENCY

In future equipment the correlation process should be designed to take place at a higher IF stage than in the MMT/MTAR equipment. In the interest of economy during implementation of the S-Band modification the IF stage frequencies (and hence local oscillator synthesis) were not changed. When the code rate was increased to 2.56 MHz, the precorrelation IF bandwidth had to be increased. The result is that noise within the IF bandwidth at the mixer image frequency maps into the postcorrelator receiver bandwidth. A performance improvement of 3 dB can be obtained by correlating at a higher frequency IF stage so that the image can be rejected.

The main tradeoff consideration in correlating at a higher frequency is that a dual IF chain is necessary for all stages after correlation. The early/late PN code tracking requires a separate correlator and a separate IF chain in addition to the signal correlator and IF chain.

An additional consideration that favors higher frequency correlation is the implementation of the 90° RF carrier phase shifts to generate the staggered quadriphase pseudonoise local reference signal. In the MMT/MTAR equipment discrete components were used. At higher frequencies (50 – 100 MHz) the more stable hybrid configurations are available.

6.1.2 OPTIMIZATION OF ACQUISITION SEQUENCE

The forward link acquisition using the frequency hop preamble is implemented in MMT/MTAR equipment with minimum predetermined times allowed for worst case conditions. Use of a detectable switch from frequency hop to SQPN should be considered to shorten the acquisition time. Since all of the receiver functions involved are programmable, only the transmit function would require hardware changes. The controller program is changed by erasing and reprogramming a programmable Read Only Memory.