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APPLICATION OF LSI TO SIGNAL DETECTION: THE DELTIC DFPCC

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16. ABSTRACT

This report deals with the development of a serial mode signal processor referred to as a DELTIC DFPCC, where the term DELTIC stands for "delay line time compression" and DFPCC stands for "difference frequency polarity coincident correlator". The thrust of the reported work was to apply large scale integrated circuit (LSI) technology to the implementation of the signal processor. The purpose of such a processor is to detect in the presence of background noise a signal whose information is coded into the zero crossings of the waveform. Chapter 1 discusses several approaches to signal processing and points out the unique features of the DELTIC DFPCC which include versatility in handling a variety of signals and relative simplicity in terms of implementation. Chapter 2 gives a theoretical performance model for the analysis and design of the DELTIC DFPCC. The model predicts the expected value of the output signal, which is pulse like, as a function of the input signal to noise ratio. Chapter 3 summarizes the design requirements and discusses the circuit design approaches used which are particularly amenable to microminiaturization and LSI. Chapter 4 gives the experimental results obtained with the prototype system which was breadboarded with LSI, MSI and SSI components. The agreement between theoretical and experimental results confirms the usefulness of the performance model. Chapter 5 compares the DELTIC DFPCC with several recently reported LSI schemes for signal processing such as CCD transversal filters and surface charge correlators. It is concluded that the DELTIC DFPCC is simpler and in some cases more versatile than other systems with the drawback being a limited bandwidth available. With established LSI technology low frequency systems applicable to sonar and similar problems are presently feasible.

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1. INTRODUCTION

This report describes a prototype signal processor which was developed for LSI implementation. Succeeding chapters describe the system operational principles, design criteria, schemes for implementation, and experimental results obtained with the prototype system. The concluding chapter summarizes the results and conclusions and discusses the possibilities for further work. The remainder of this chapter discusses the nature of the particular problem to be solved and outlines the possible approaches including the one implemented here. First the detection problem under consideration is discussed in the following section.

1.1 The Signal Detection Problem

The typical signal of interest has the mathematical form:

$$S(t) = A(t) \cos (2\pi F_c t + \phi(t) + 0) \qquad (1.1)$$

where $A(t)$ and $\phi(t)$ correspond to amplitude and phase modulation functions, F_c is the carrier frequency, and θ is a randomly varying phase angle. This signal may represent a sonar or radar return or simply a transmitted information symbol. The signal is received with background noise, $n(t)$ which is usually assumed to be gaussian and white. Typically, $s(t)$ will be in the form of a pulse train, and the problem is to determine with low false alarm probability whether or not a pulse has occurred on the basis of the results from measurement of the signal plus noise. The processing system typically does not replicate the input waveform but rather constructs an output pulse with amplitude

sufficiently above the noise level so that the threshold type decision can be made.

The signal input to the processor is of the form:

$$y(t) = s(t) + n(t) \tag{1.2}$$

It is well known that the optimum linear detector for implementing the decision scheme, i.e., maximizing the signal to noise ratio, is a matched filter.[1] The impulse response for the matched filter is:

$$h(t) = s(t_o - t) \tag{1.3}$$

where t_o is a time delay implemented in order to make the filter causal, i.e., a physically realizable scheme which does not require an output to occur before the input does.

The output of such a filter can be expressed as:

$$r(t) = \int_{-\infty}^{\infty} y(\tau)h(t - \tau)d\tau \tag{1.4}$$

or

$$r(t) = \int_{-}^{t} y(t - \tau)h(\tau)d\tau \tag{1.5}$$

For a band limited pulse of bandwidth W and time duration T, the matched filter gives the output signal to noise ratio (SNR), λ_o, in terms of the input SNR, λ_i, as:

$$\lambda_o = 2\ TW\ \lambda_i \tag{1.6}$$

Since out of band noise can generally be eliminated at the input with a bandpass filter, the input SNR will be inversely proportional to the bandwidth W. Therefore the matched filter processor allows the choice of a

bandwidth to meet other systems requirement without having to pay the penalty of a reduced SNR.

The following section discusses some possible approaches to implementation.

1.2 Methods for Implementation

The most straightforward approach for implementing the optimum detector is to design a linear, analog circuit with the impulse response given by (1.3). In practice, the signals which are used result in impulse responses which are too complex for convenient implementation using this approach.

All other schemes rely on sampling. The delay line filter is such a scheme. Suppose that the sampling period is T_s so that time is given by $t_n = n\,T_s$. In practice the integrals of (1.4) and (1.5) may be carried out over a finite time interval for processing a single pulse in y(t). Therefore, the integrals can be approximated as a finite sum of samples. Figure 1.1 illustrate a delay line with each memory location storing one sample with the most recent sample at the right edge of the delay line and samples being propagated to the left, so that the geometry corresponds to a plot of $y(t_n)$ with the usual positive axis definition. Tap weights on the line are adjusted according to $h(R - mT_s)$ where R is the time length of the delay line and m is the tap location number from the left edge.

The CCD delay line is a practical element for constructing the delay line filter. It operates as a sampled data device; however, there is no quantization of signal levels within the dynamic range of the the device. The difficulty is in obtaining the taps and physically realizing the tap weights in a manner that is flexible, reasonably accurate, and not bulky and unwieldy.

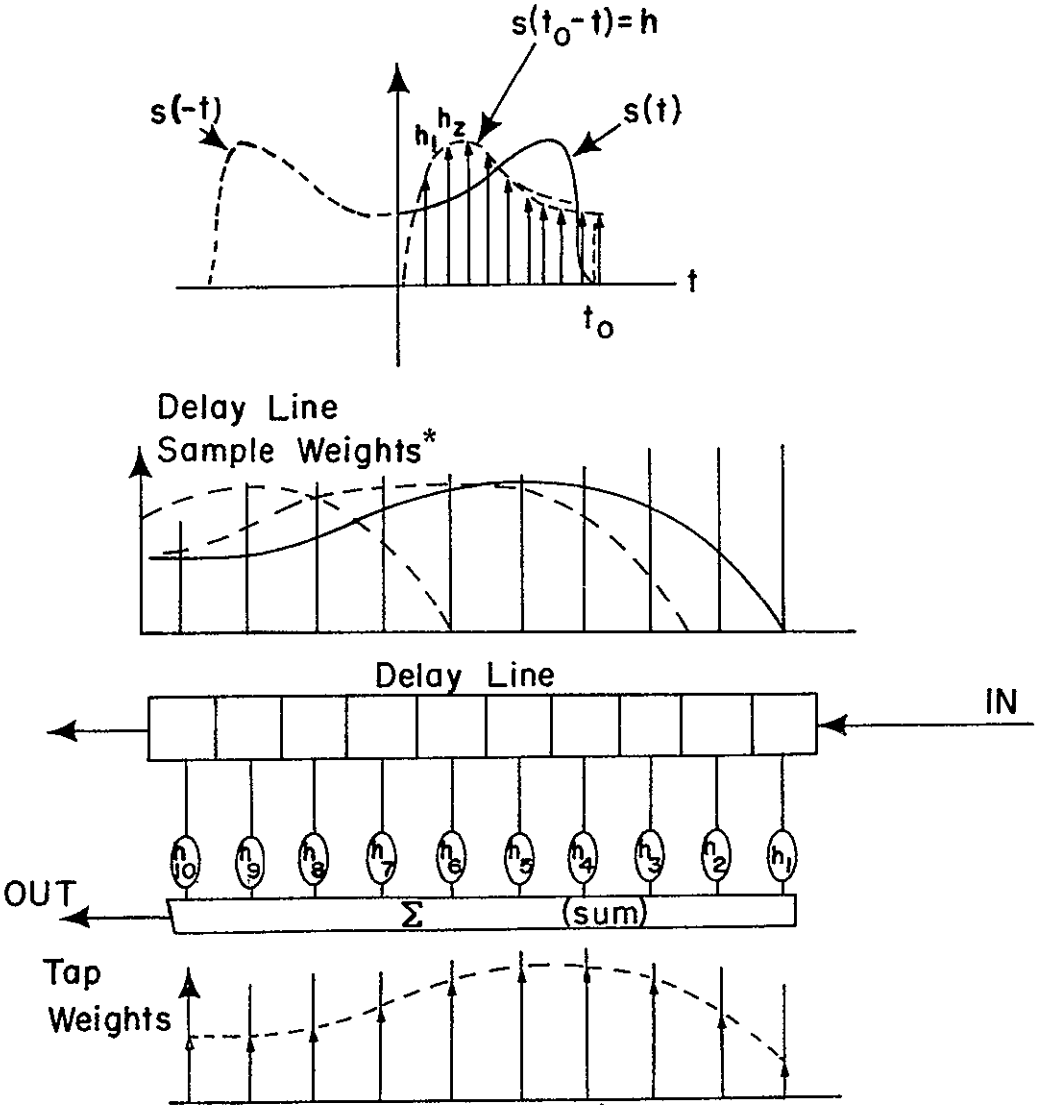

Figure 1.1 Illustration of Delay Line Filter Operation and Tap Weight Construction.

*Figure implies a shifting of the signal through the delay line with time.

A more generalized concept of a digital signal processor is shown in Figure 1.2. Here the upper memory operates in a serial clocked mode. During each clock interval the memory is sensed by nondestructive readout (NDRO), and the content of each location is multiplied in a parallel mode with the content of a corresponding fixed (lower) register. All of the products are summed in parallel. The fixed memory contains the tap weight values. Such an implementation is called a correlator.

The difficulty with this concept arises when a large number of quantization levels are involved. If this is the case, then the memory becomes more complex and the digital multiplication and summing for parallel operation requires a large amount of circuitry. Such a scheme may become practical if the signal is quantized to two levels.[2] Recently the use of an exotic analog memory scheme in conjunction with analog CCD delay line memory has been proposed as a simplifying technique avoiding complex digital operations.[3]

The digital processor implementation is simplified if the multiply and sum operations are done in a serial mode of operation. This mode of operation is illustrated in Figure 1.3. During a sampling interval the signal and reference memories are parallel read (NDRO) into shift registers. In the interim period before the next read operation, i.e., a sample period T_s, the shift registers are read out serially and the contents multiplied and summed. Figure 1.4 illustrates that only two serial memories are actually required. Here recirculation from the last location on the reference and next to last location on the signal memory accomplishes the function. When the next sample is loaded into the signal memory, all samples shift one location, and the memory is ready for another

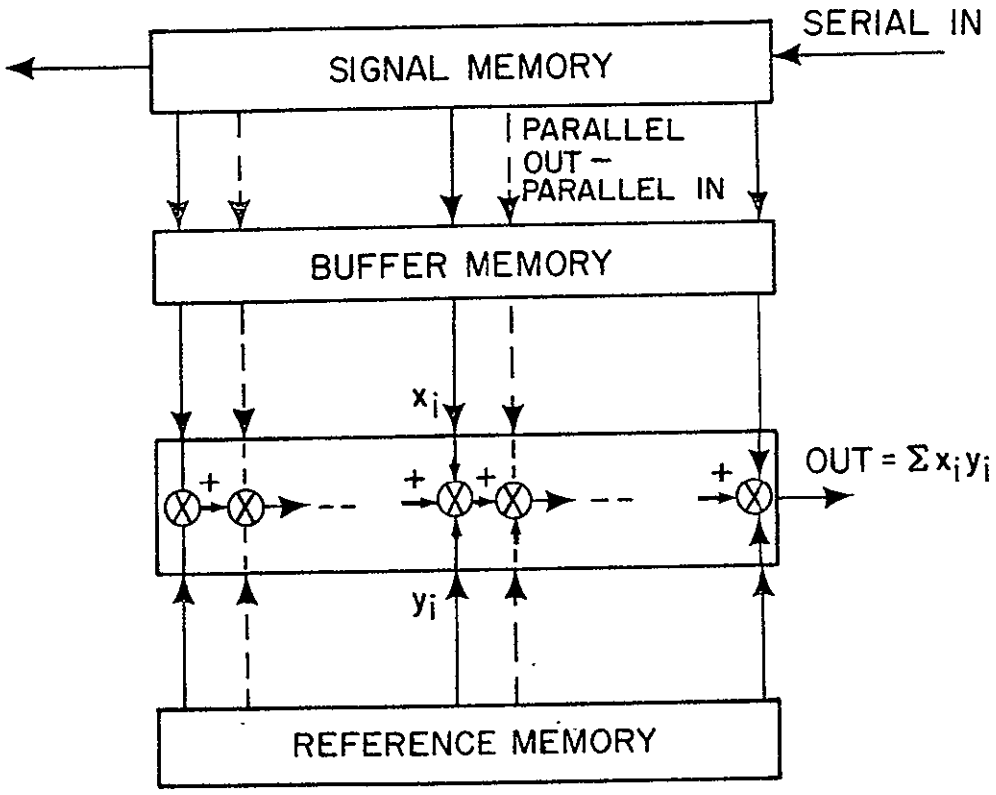

Figure 1.2 Parallel Mode Signal Processor. (Correlator)

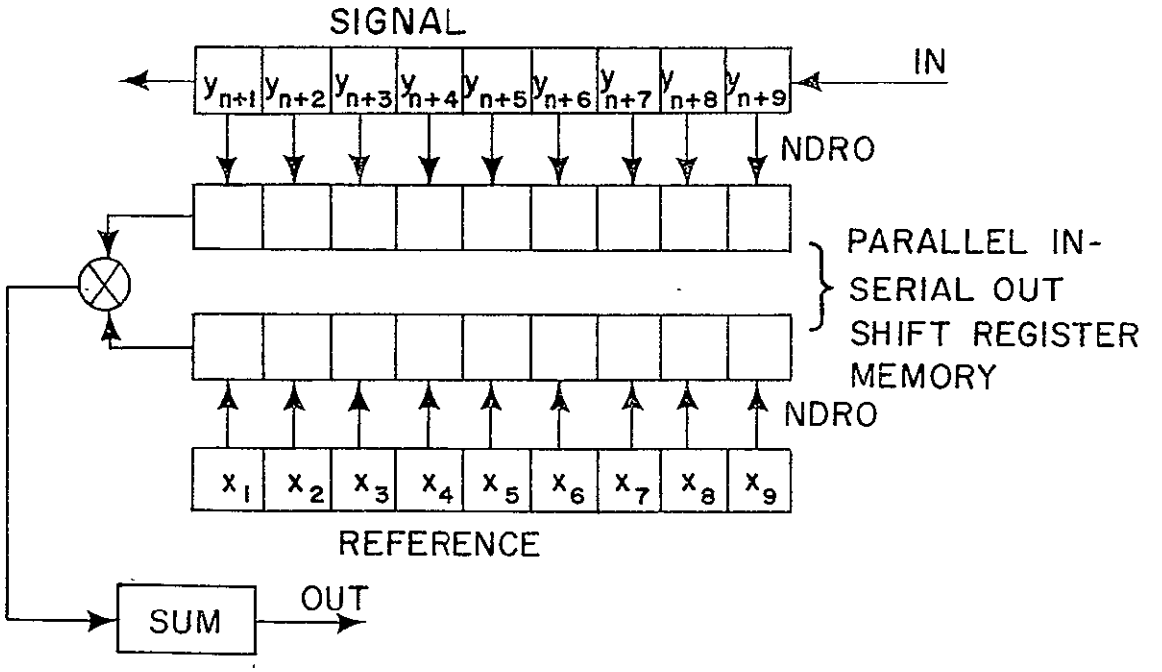

Figure 1.3 Serial Mode Signal Processor. (Correlator)

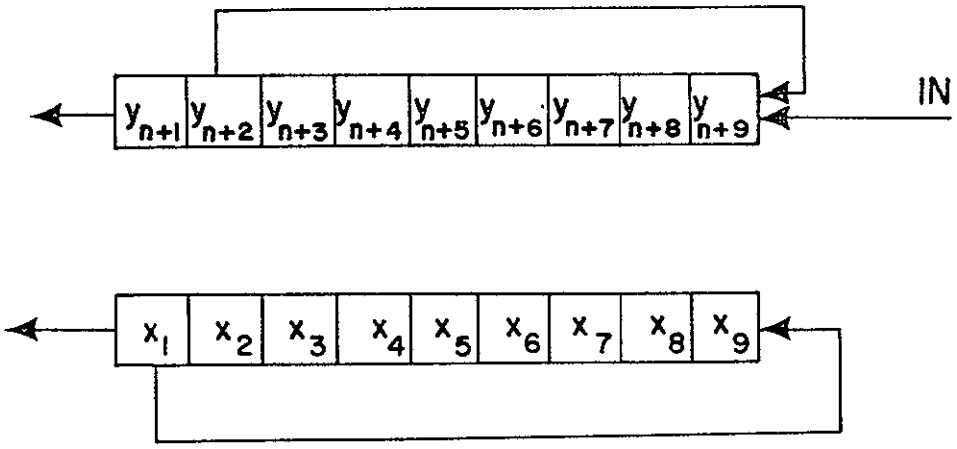

Figure 1.4 Recirculation Principle for Reducing the Memory Requirement of the Serial Processor.

readout. Figure 1.5 shows a microphotograph of a DELTIC serial memory developed at MSFC during the course of this work. It operates with binary level signals utilizing the principle illustrated in Figure 1.4.

Although less hardware is required for the serial processor than for the parallel, it is still a very complex system in term of component count if a large number of quantization levels is to be used. As in all serial vs. parallel digital systems, the reduction in complexity is at the cost of reduced ultimate speed because the serial memory must be exercised at a much higher rate.

1.3 The Random Phase Problem

All of the preceding schemes will fail if directly applied for signals with a random phase angle θ. Since θ is an unknown the correct response function or reference signal is not known. For any fixed h(t), the output of the system will vary with the cosine of variations in θ. In practice this would result in fading of the output as θ varies.

Two principles which are used for solving this problem are: (1) a difference frequency scheme, and (2) a quadrature detection scheme. Both methods require that the incoming signal be heterodyned with a reference frequency, and both give an output with rms value independent of θ. The difference frequency scheme will usually require less hardware for implementation. For the processors discussed in the last section, the difference frequency method requires that both the x and y signals be mixed with different LO signals before being loaded into memory. The output is then a modulated carrier signal with the carrier frequency proportional to the difference in the LO frequencies.

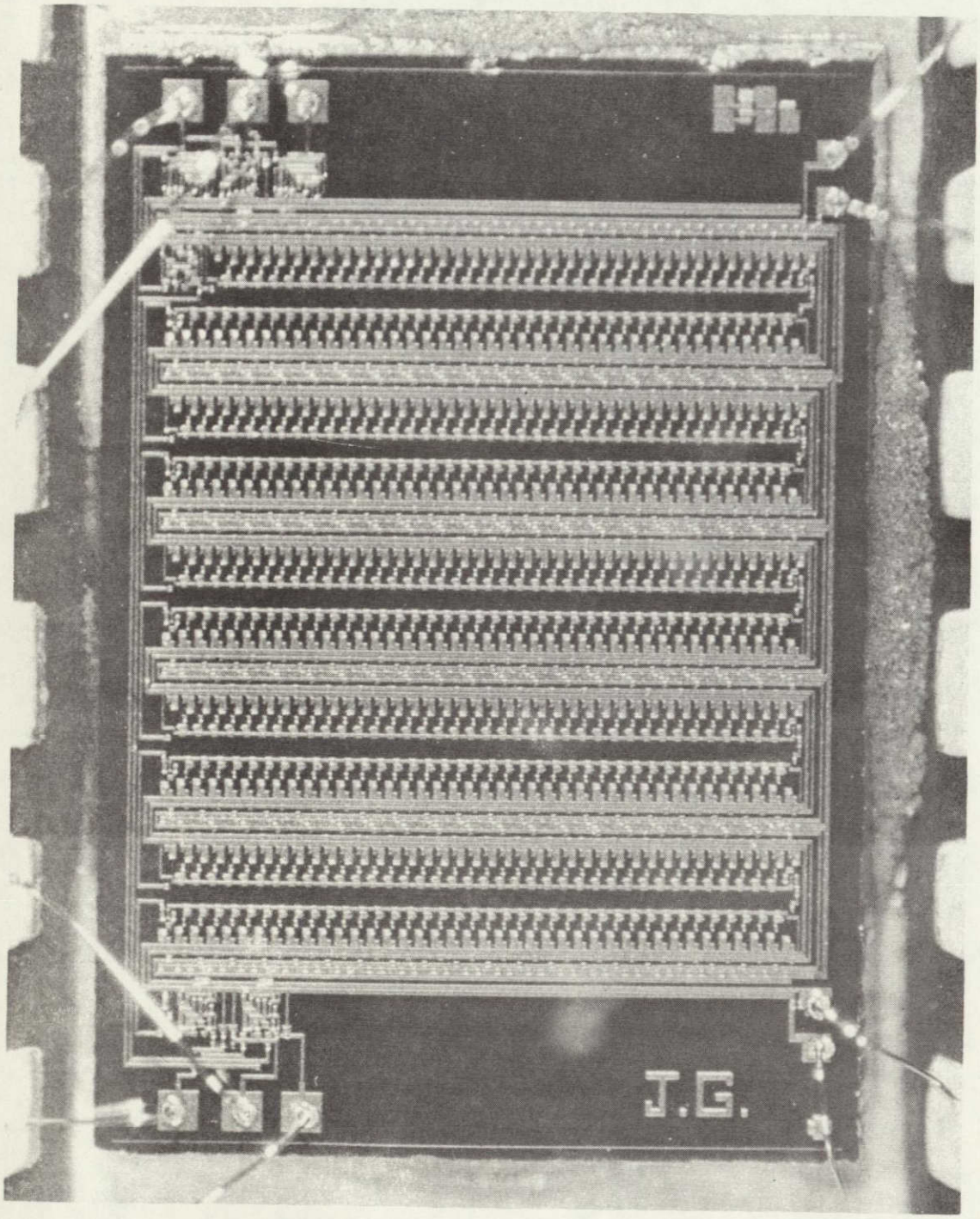

Figure 1.5 Photomicrograph of a DELTIC serial memory. This circuit contains 1230 PMOS transistors for implementing a 200 bit memory with input and output gating. Recirculation principle utilized here is illustrated in Figure 1.4.

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1.4 LSI Implementations

Practical signal detectors based on the preceding principles are very complex systems. It is desirable to use LSI techniques for implementation for several reasons: (1) Reliability, (2) Low power requirement, (3) Compactness, and, (4) possible economy. The first three items should result from the application of MOS LSI technology to any of the preceding detection schemes. Economy depends upon design and fabrication complexity and on the volume demand for the product. Demand will be affected in most cases by the versatility of application.

From the standpoint of simplicity, each scheme discussed in section (1.2) benefits greatly by using signals with binary levels. This means that information must be coded in the zero crossings and causes no severe restrictions in most cases. In this case tap weights for a delay line have binary values and the memories required have simple, one-bit words. Multiplication operations can be accomplished with digital gates. If a large number of quantization levels are required, then the CCD tapped delay line realization appears to be the simplest unless precision tap weights are required. A very convenient technique for tapping the CCD delay line with moderate tap weight accuracy was recently reported.[4] This involved sensing the charging current to split transfer electrodes and the tap weight is proportional to the relative electrode sizes. Use of CCD's for analog signal and reference memories in the correlator implementations would pose a problem because of the need for refreshing the reference memory, no trivial matter for analog signals. Exotic analog memory techniques, such as the MNOS analog memory, for the reference memory are yet unproved. Also, if analog signals are used then an analog multiplier is

also required, which will be difficult to realize if high speed performance, wide dynamic range, and linearity are required.

When binary level signals are used, the correlator scheme with signal and reference memories appears to have an advantage over tapped delay line filters. Although binary tap weights are much more simply implemented than analog weights, tap weight adjustment appears to be less convenient and versatile than loading a memory as in the case of the correlator processor.

As previously mentioned, the trade-off between parallel and serial mode operation is simplicity vs. speed of operation. Since simplicity is so obviously desirable, it is of interest to estimate the speed limitations for serial mode operation. The limitation can safely be assumed to be due to the serial memory operation. The tradeoff to accommodate a given memory speed capability is between maximum signal bandwidth and processing gain, or maximum signal to noise ratio improvement. This can be shown as follows.

Assume that the signal is sampled at the Nyquist rate, i.e., $f_s = 2\ W$. Then the number of samples required in memory for signal length of T seconds is:

$$N = f_s T = 2\ WT \tag{1.7}$$

The clock rate for the memory for a serial output is:

$$f_c = N f_s = 2\ NW \tag{1.8}$$

Since $N = 2\ WT$ is the maximum signal to noise ratio improvement available, the maximum bandwidth for given f_c and N is:

$$W < f_c/2\ N \tag{1.9}$$

Buried layer CCD shift registers have been operated at over 100 MHz. Assuming that this will be a reasonable limit, then for a processing gain of 200 the maximum signal bandwidth which can be handled is 250 KHz or less. For larger bandwidths it would seem likely that parallel mode processors would be required.

1.5 Conclusions

The correlator type of signal processor with serial mode signal and reference memories should be capable ultimately of handling signal bandwidths of 250 KHz with an SNR improvement of 100. Such a signal processor will be simple and versatile for signals with information coded in the zero crossings, i.e., frequency or phase modulated. It is concluded that such a signal processor would have considerable utility and is worthy of further development.

The next chapter discusses the theory of operation for a DELTIC DFPCC system which is a correlation processor with serial memories and which can be implemented with MOS LSI technology.

2. THEORY OF THE DELTIC DFPCC[5,6,7,8,9]

The term DELTIC is an abbreviation for "delay line time compression", and the letters DFPCC represent "difference frequency polarity coincident correlator". Figure 2.1 gives a block diagram of this type of signal processor. The DELTICs are shift register type serial memories with loading and recirculation capabilities in which time gated segments of the preprocessed signal and reference waveform are stored. The difference frequency results from heterodyning the incoming and reference signals with different LO frequencies in order to eliminate the random phase problem discussed in section 1.3. The term "polarity coincidence correlator" describes a signal processor in which infinite clipping is used to create a binary level signal so that all information is coded into the instantaneous frequency or zero crossings of the signals to be correlated.

In this chapter the theory of operation of the DELTIC DFPCC is discussed and theoretical results describing the system performance capability are given. First a general description of the system operation is presented in the following section.

2.1 General Description of System Operation[9]

The following discussion refers to the block diagram in Figure 2.1. The processor action can be described by tracing the signal left to right and noting that the functions performed are the same for both the signal and its reference up to the DELTICs. Only the signal plus noise y(t) is traced.

The first operation is bandpass filtering (BPF) which rejects out of band noise and reproduces the signal plus band limited noise. This

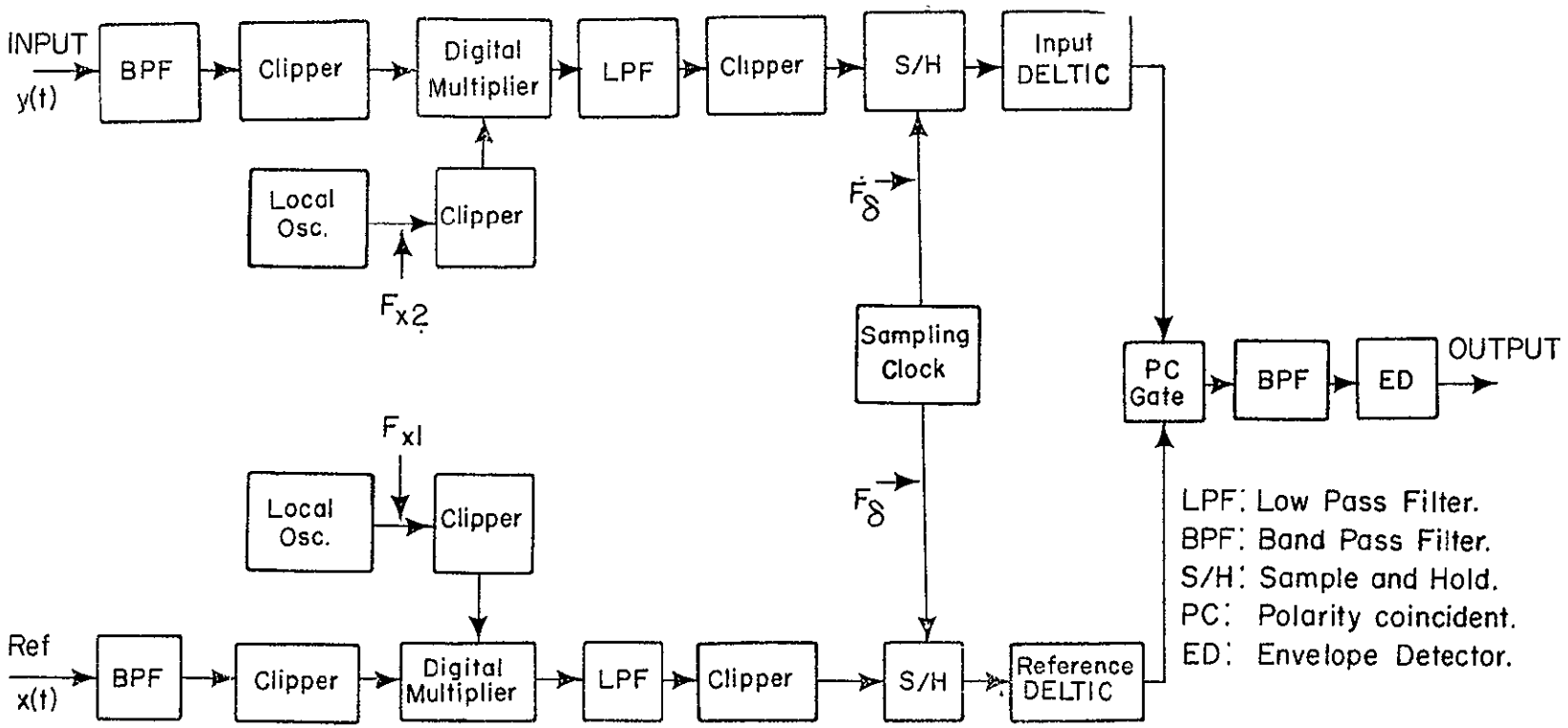


Figure 2.1 Block Diagram of DELTIC DFPCC Signal Processor.

composite of signal plus noise is infinitely clipped producing a binary level signal and redistributing the energy in the frequency spectrum. For a pure sinusoid clipping introduces odd harmonics and for a more complicated signal plus noise spectrum the action produces the spectrum of the angle modulated portion of the input and satellite spectra which generally have a broader bandwidths (i.e. analogous to frequency multiplication for FM transmitters). The clipped signal is mixed with a square wave local oscillator (LO) with fundamental frequency F_{x2}. This shifts the original spectrum to several locations corresponding to difference and sum frequencies of F_{x2} and its odd harmonics with the original carrier F_c. Mixing also shifts the harmonic distortion components to different intermediate frequencies (IF). Out of all the multitude of spectra present, only the band with an IF of $|F_{x2} - F_c|$ is of interest. This is the lowest frequency band and can be preserved by passing the mixer output through a low pass filter (LPF) which rejects the distortion components at higher frequencies.

The output of the LPF is clipped so that the output of the clipper corresponds with the output of the original clipper except that the spectrum is now shifted to an IF of $|F_{x2} - F_c|$. In the reference channel all of the preceding operations are performed; however, the LO has a fundamental frequency F_{x1}, and the IFout of the last clipper is $|F_{x1} - F_c|$. In each channel the LO frequency is chosen so that the IF results in the lower edge of the desired band being significantly lower than the bandwidth W. Therefore, the output of the clippers can be sampled at a frequency of approximately 2W, ignoring the distortion components due to the clipping action of the last clipper.

The DELTIC action accomplishes serial reproduction of gated segments of the sampled signal and reference waveforms during a sampling interval. The difference in the two DELTICs is the gating action. On the reference DELTIC, the gating action is a one-shot phenomena. Only one segment of time length T from the reference waveform is gated in. This waveform is serially reproduced during each sampling interval and is saved in memory by the recirculation principle described in Figure 1.4. The output of the reference DELTIC is the periodic with period R = T/N. The gating action on the signal DELTIC slides along the time axis, shifting by one sampling interval at the end of each sampling period. The serial reproduction is carried out during the succeeding sampling interval and the desired portion of the signal frame is saved by recirculation as shown in Figure 1.4. At the next sampling instant, a new sample is loaded with the remaining old samples shifted by one sampling period in the time slots. Figure 2.2 illustrates the gating action of the two DELTICS.

The polarity coincident (PC) gate accomplishes the required multiplicative action for correlation. At the end of the interval in which the DELTIC contents are serially multiplied, the sum of the samples from the PC gate contains the information for constructing one sample point on the correlation function for the frequency shifted, clipped versions of y and x. In addition to this desired information are many distortion components. The purpose of the bandpass filter (BPF) at the output is to reject all distortion components which do not overlap into the frequency band of the desired correlation function output signal. The BPF also acts as an interpolation filter for reconstructing the correlation function from its sampled values.

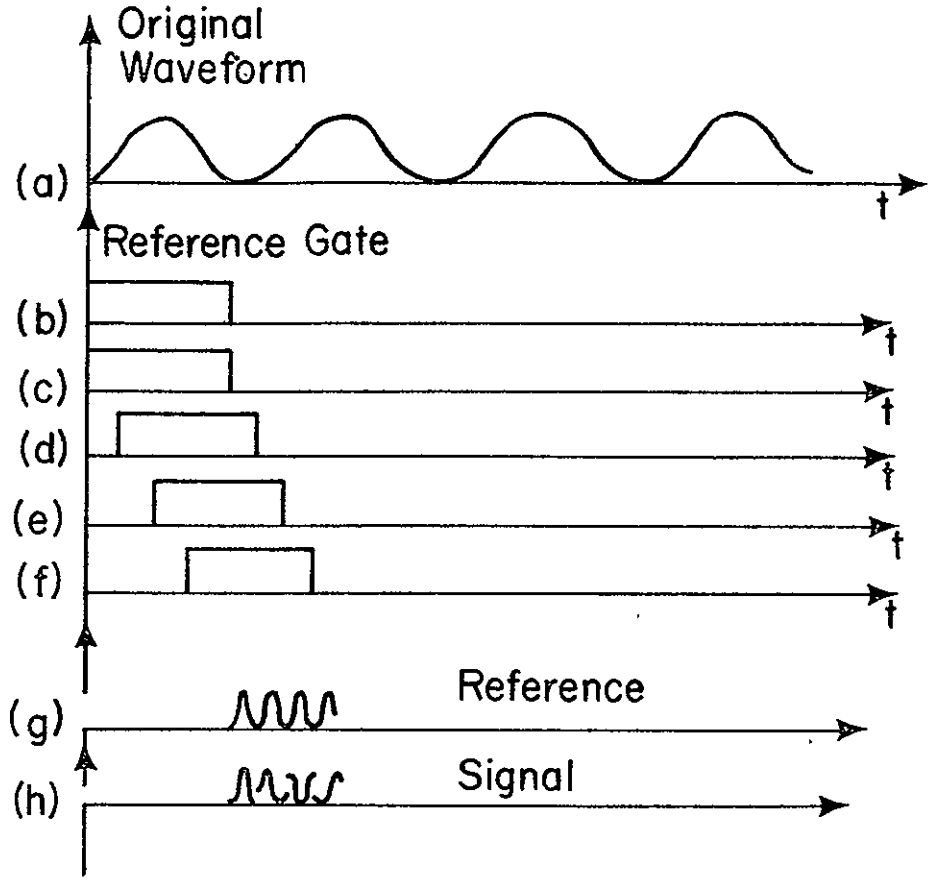


Figure 2.2 Waveforms Illustrating Gate Action and Serial Reproduction by DELTICS: (c) - (d) illustrate sliding gate of signal DELTIC. (g) and (h) represent serial reproductions of waveforms gated in intervals (c) - (d) with same time scale as for (a).

The output of the BPF is, ideally, the correlation function of clipped and filtered versions of y and x with a carrier frequency modulation. This carrier frequency is the difference between the LO's, $|F_{x2} - F_{x1}|$, multiplied by the time compression factor, $N = T/T_s$. Finally, the average value is obtained with an average value envelope detector. A theoretical analysis of the DELTIC DFPCC must consider the various sources of distortion which arise in the approximate correlation technique. The next section discusses these effects in a semi-quantitative manner.

2.2 Distortion Effects[9]

The distortion effects introduced before the low pass filter are essentially removed by the filtering action. New distortion components are introduced by the second clipping action. This effect is illustrated in Figure 2.3 which shows the distortion bands beginning at odd harmonics of the lower band edge (the IF) of the desired band. The energy is spread out over multiples of 3, 5, 7, ..., etc. times the original bandwidth and are also attenuated by factors of 1/3, 1/5, 1/7, etc. corresponding to the harmonic structure of an infinitely clipped sinusoid (square wave). Therefore, the distortion components in the band from F_I to $F_I + W$ are highly attenuated.

The sampling rate is chosen as $F_s \geq 2(F_I + W)$, which would be the Nyquist rate for the band of interest. Since the total spectra including the distortion components extends beyond $F_I + W$, some distortion due to aliasing, or foldover, in sampling is expected. However, the output of the clipper is not to be reconstructed but is correlated with the output in the reference channel. The mixing of frequencies in this operation

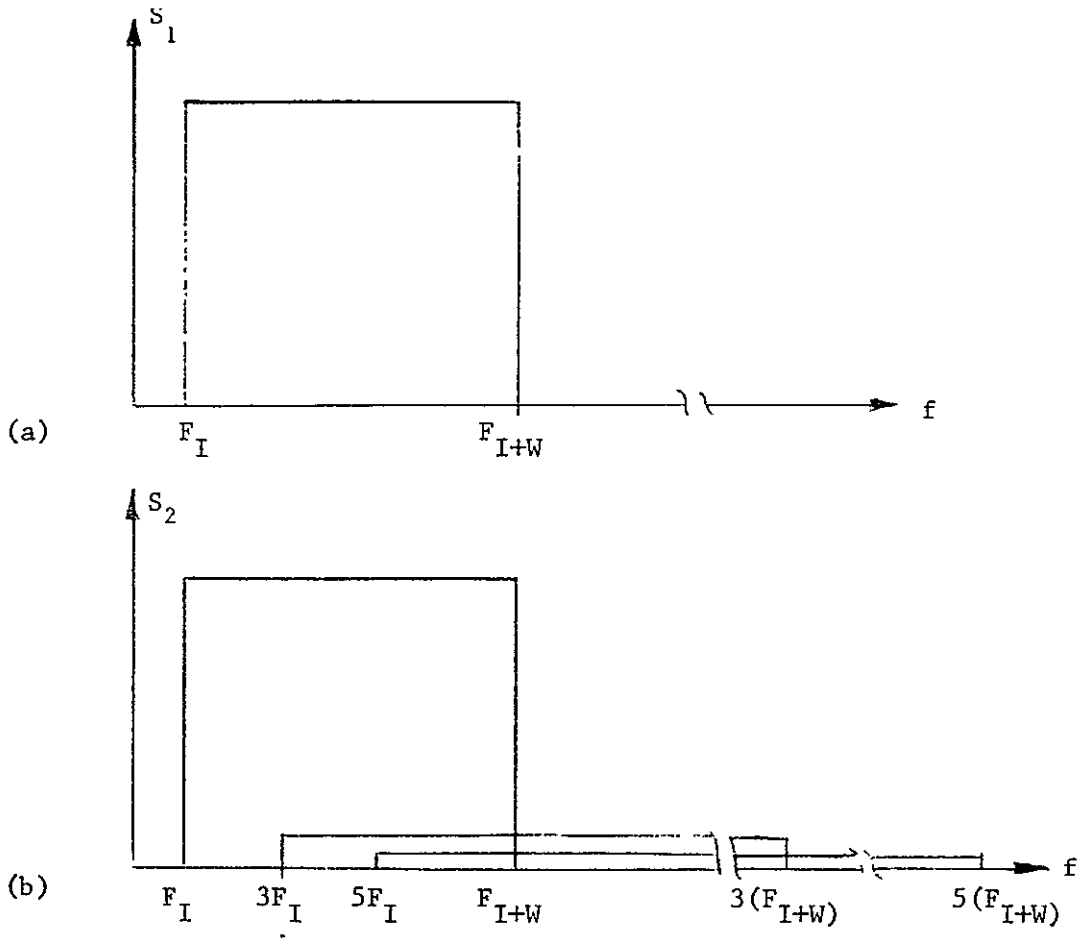


Figure 2.3 (a) Spectral distribution of LPF output.
(b) Spectral distribution after clipping.

reduces the foldover into the band of interest so that the output BPF is more effective in reducing the sampling distortion components than would be a reconstruction filter directly after the sampled limiter output.

Finally, there is the distortion due to the operation of the DELTIC correlator. Whelchel[9] has applied Fourier analysis to operation of the DELTIC correlator for aperiodic signals and signals with periodic modulation. In the case of the aperiodic pulse, he found that the

distortion was negligible if the DELTIC memory length were long enough to accommodate the pulse. For signals with periodic modulation, he found that the power spectral density (PSD) of the multiplier output contained the PSD of the desired correlation function but that distortion components overlapped into the desired band. Since the DELTIC correlator is a sampled data system, one expects sampling type distortion which ideally could be eliminated with a reconstruction filter. No simple intuitive explanation has been found for the non-removable distortion components; therefore, some results from Whelchel's[9] analysis are presented here.

One type of modulating signal considered was the complex periodic modulation:

$$S(t) = e^{j2\pi F_c t} \sum_{s=0}^{M} C_s \, e^{j2\pi s F_o t} \tag{2.1}$$

Whelchel found the output of the multiplier as:

$$Z(f) = \sum_s \sum_n X_s {}^{*} Y_n \, \mathrm{sinc}[R(f - (n-s)f_o - f_\delta)] \cdot \sum_r \delta(f - \frac{r}{R} - (nF_o + F_2)) \tag{2.2}$$

In this expression X_s and Y_n are the original fourier coefficients multiplied by phase factors corresponding to various channel delays, $R = T/N$ is the compressed time length of the memory, $f_\delta = N(F_{x_2} - F_{x_1})$, $f_o = NF_o$, the "sinc" notation is for $\sin\pi x/\pi x$, and the delta notation is for the Dirac delta function. Whelchel has separated this expression into a principal part with $s = n$ and terms contributing to distortion, $s \neq n$.

The principal part contains the PSD of the desired correlation function. Figure 2.4 (a) shows the general result and 2.4 (b) shows the spectra when the following frequency relation is used:

$$f_\delta = \frac{r_m}{R} + F_2 + \frac{W}{2} \tag{2.3}$$

In this case the PSD components are centered at $f = f_\delta$. For a real signal this would correspond to a correlation function envelope with a carrier frequency of f_δ. One may note that in satisfying (2.3) the distortion of the sinc envelope is minimized and also that the satellite spectra lie centered on the nulls of the sinc function. A band pass filter can therefore be used to select the modulated correlation function from the principal spectra.

The distortion components which may overlap into the desired band come from the terms $s \neq n$. If one considers the terms for which $n - s = \alpha = 1, 2, \ldots$, then from (2.2):

$$Z_\alpha(f) = \sum_\alpha \sum_n X^*_{n-\alpha} Y_n \operatorname{sinc}[R(f - \alpha f_o - f_\delta)] \cdot \sum_r \delta(f - \frac{r}{R} - (nF_o + F_2)) \tag{2.4}$$

For each value of α, the sinc envelope for the spectra peaks at $f = \alpha f_o + f_\delta = \alpha N F_o + f_\delta$. Figure 2.5 shows the sinc envelope for $\alpha = 1$ when $f_o = NF_o = 1/R$. Note that the null of the sinc function lies in the middle of the desired band. This means that the distortion components which fall within the desired band will be highly attenuated. It should be noted that this choice of $R = 1/NF_o$ corresponds to $T = 1/F_o$, which agrees with the intuitive idea that the correlation period T should agree with the period of the modulation signal. Thus the memory length should be matched to the modulation signal.

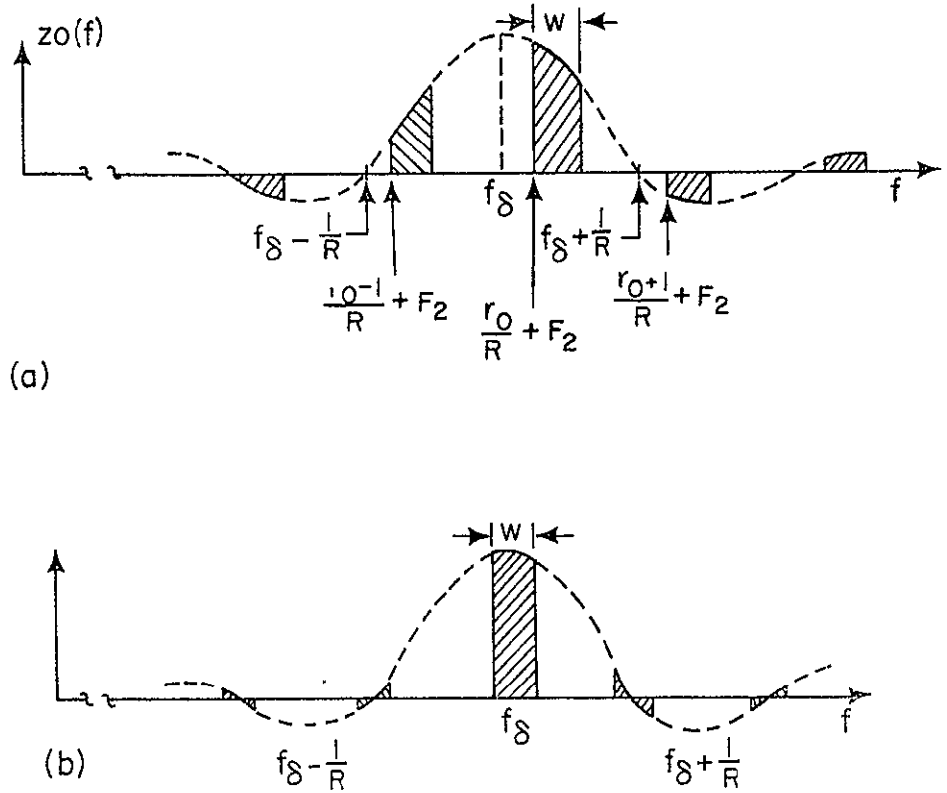


Figure 2.4 (a) Spectral Distribution of Principal Components out of Multiplier.[9]
(b) Distribution when (2.3) is satisfied.
$W \cong M F_o$, the bandwidth of the modulation signal.

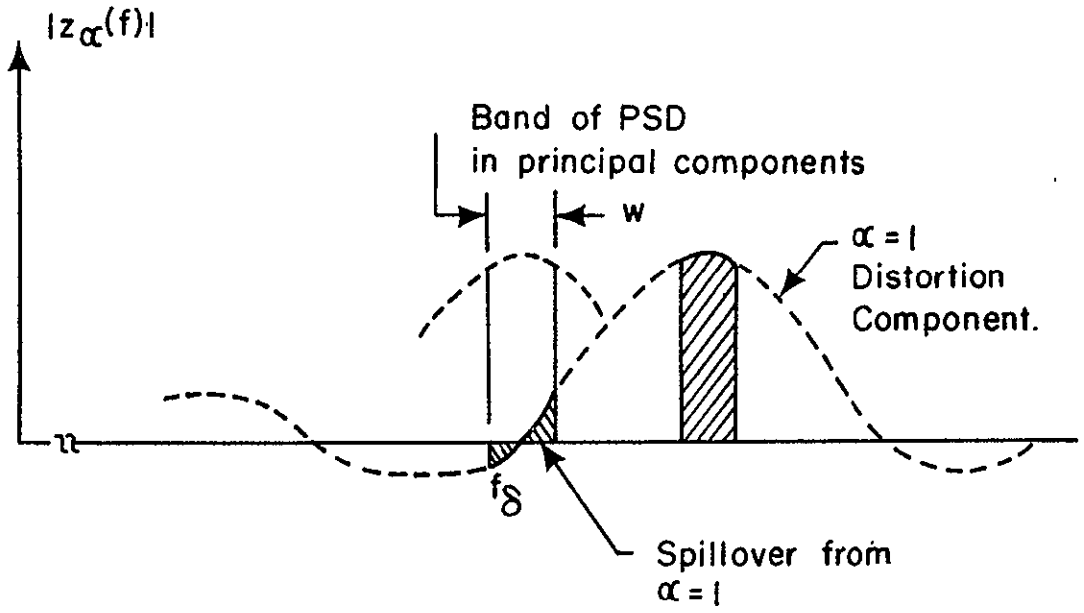


Figure 2.5 Distortion Components Spillover into Desired Output Band.

It is clear from Figure 2.5 that distortion components may spill over into the desired output band so that they cannot be removed by filtering. Whelchel has analyzed this spillover and found two types of behavior. In one case, there is the incoherent, noise like addition of many α values, and in the other case the spillover causes a coherent "glitch" in the correlation spike. This latter phenomena was analyzed by Whelchel in terms of ambiguity functions.

In summary there are many non-linear and time varying operations in the processor which cause distortion components in the output. The proper choice of frequencies, of filter characteristics, of memory length, etc. can minimize the distortion. Practically the processor may be viewed as a correlator in which correlation spikes may be observed; however, there will be a self-noise background which appears between correlation spikes, and there will be a fluctuation of the spike amplitude due to the distortion.

2.3 Theoretical Model of the DELTIC DFPCC[9]

From his analysis of the system operation, Whelchel concluded that the DELTIC DFPCC operated as an ideal correlator for bandpass limited signal plus noise and reference waveforms. Figure 2.6 shows a block diagram of the system concept. Self noise is shown as additive noise in the output. This concept of self noise is convenient for implying a sensitivity limitation; however, the actual structure of the self noise is quite complex. Correlation of signal on signal and of noise on signal both give rise to extraneous output not present in the ideal correlator without self-noise. Quantitative evaluation of the self noise is very difficult and has not been done at this time. However, the

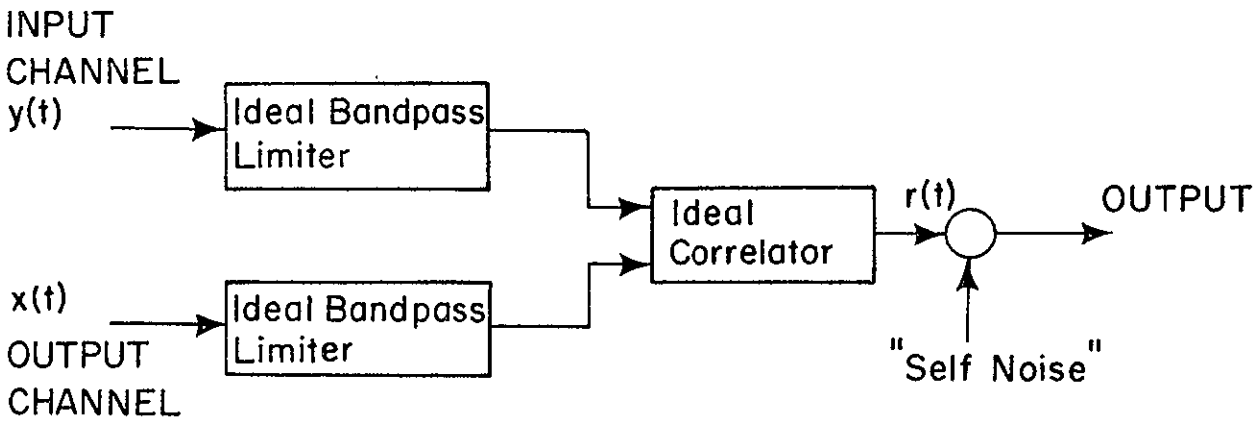


Figure 2.6 Theoretical Performance Model of DELTIC DFPCC.[9]

expected value of the correlation spike in the presence of input noise and the mean square output noise for noise only at the signal channel input have been found by Whelchel.

The expected value (first moment) for the output of the system with signal plus noise at the input to the signal channel is:

$$r_o(t) = W_s(\lambda)\, R_x(t) \tag{2.5}$$

where $R_x(t)$ is the correlation function for the signal without noise with the reference signal and $W_s(\lambda)$ is a weighting factor depending upon the input signal to noise ratio, λ.

$$W_s(\lambda) = \int \Gamma(\tfrac{3}{2}) \cdot a_o e^{-\frac{a_o^2}{2}} \cdot [I_o(\tfrac{a_o^2}{2}) + I_1(\tfrac{a_o^2}{2})] \cdot p(A)dA \tag{2.6}$$

Here,

$$a_o^2 = \frac{A^2}{2\,\sigma_N^2} \quad , \tag{2.7}$$

where A is the envelope of a narrowband signal function, σ_N^2 is the mean square value of the band limited input noise, P(A) is the amplitude probability density function, and I_o and I_1 are modified Bessel functions of the first kind.

The mean square output noise of the system with noise only at the input channel was shown to be given by:

$$\sigma_o^2(N) = \frac{1}{T}\int_{-\infty}^{\infty} R_n(\beta)R_x(\beta)d\beta \tag{2.8}$$

where R_n and R_x are the autocorrelation functions for the bandpass limited noise and signal respectively. Because of the bandpass limited

characteristics, both R_n and R_x are independent of the actual signal and noise amplitudes; therefore, the output noise power dependent depends only on the spectral characteristics (i.e. bandwidth, etc.) of the reference signal and noise.

Applying the results of (2.5) - (2.8), Whelchel calculated the expected value of the correlation spike height as a function of the input SNR for constant envelope and pseudorandom noise (PRN) signals, with the results shown in Figure (2.7). He defined a figure of merit as:

$$\lambda_o \triangleq \frac{[r_o(0)]^2}{\sigma^2(N)} \tag{2.9}$$

which is the ratio of the peak signal power to the mean noise power without the signal. Since this is a measure of the increase in the spike height above the pre-spike noise background, it is a useful figure of merit. It should not of course be treated as a true SNR value at the output, because the noise is modified by the presence of the signal due to direct and distortion effects. For narrow band signals, $\sigma_o^2(N)$ is inversely proportional to the TW product of the signal. The figure of merit for this type of signal is:

$$\lambda_o = 2TW[W_s(\lambda)]^2 \tag{2.10}$$

Figure (2.8) shows λ_o as a function of λ_i, the input SNR, and the obvious limiting value is 2TW.

2.4 Summary

The DELTIC DFPCC acts as a correlator of bandpass limited signal plus noise with the signal, independent of the random carrier phase. The

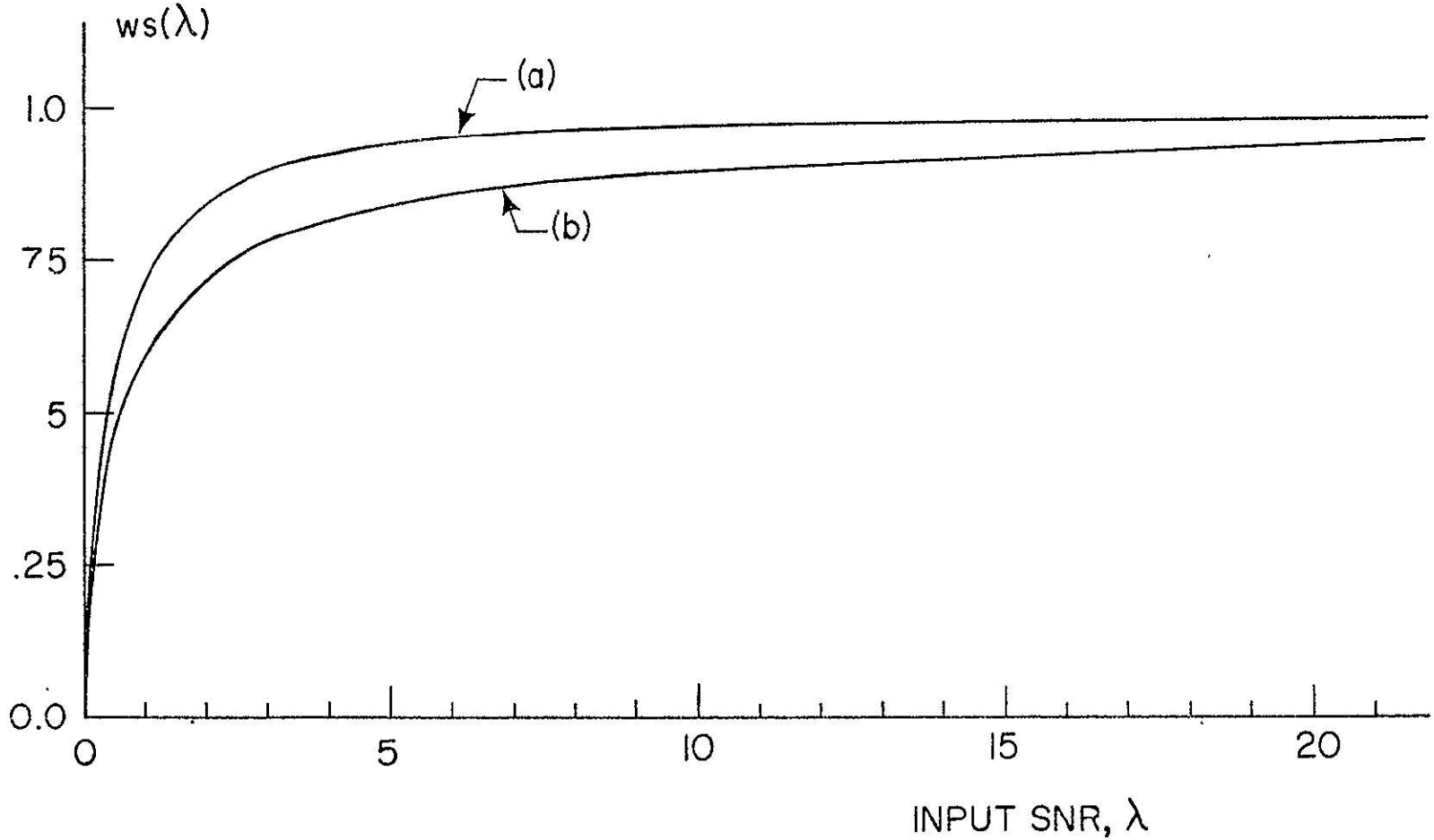


Figure 2.7 Ratio of Correlation Spike Height to Maximum Value as a Function of Input SNR.[9]
(a) Constant Envelope Signal
(b) Pseudo-random Noise

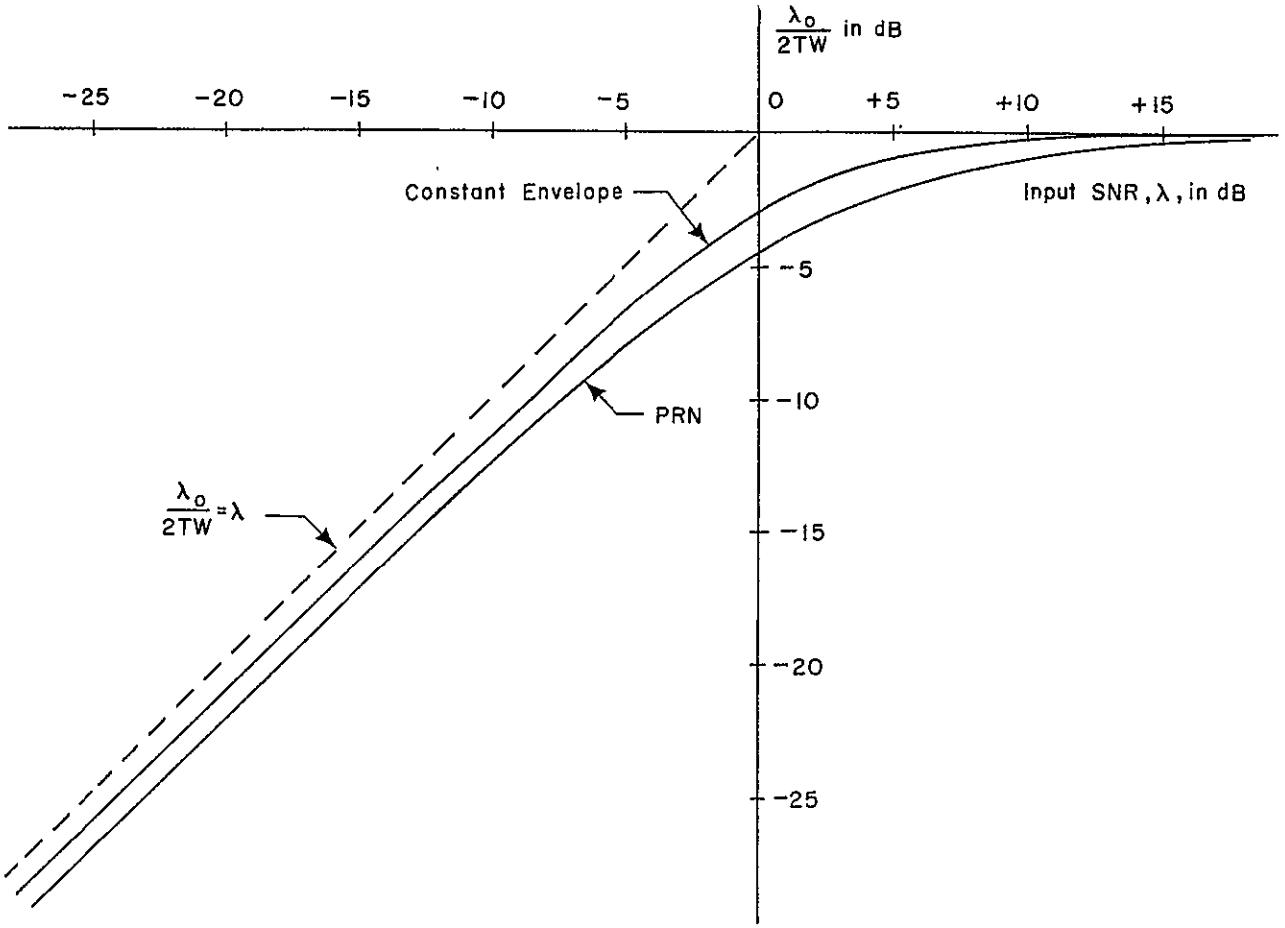


Figure 2.8 Figure of Merit for DELTIC DFPCC vs. Input SNR[9] for Constant Envelope and for Pseudo-random Noise type Signals.

correlation spike height depends only upon the spectral characteristics of the signal and noise and the input SNR. The output noise due to input noise only is independent of the input noise amplitude and generally decreases with the noise bandwidth. The nonlinear and time varying nature of the processor operation results in many distortion terms in addition to the desired correlation function and inevitable noise. Many of these distortion components are removable by filtering; however, some appear in the passband of the correlation function itself and cannot be removed. These components appear as incoherent fluctuations resembling background noise in the absence of the spike and as a variation in the amplitude of the correlation spike waveform which are greater than that due to the input noise alone.

3. DESIGN IMPLEMENTATION

The first requirement in designing the DELTIC DFPCC is to select the system frequencies so that the distortion components in the output can be minimized. The second requirement in this work is to choose implementation schemes compatible with LSI technology. This generally means realizing as many functions as possible by digital circuitry. A third requirement for the prototype system was to design input and output circuits which allowed a quantitative evaluation of the theoretical performance model developed in the course of this work. This resulted in a more complex system than is required to demonstrate system feasibility. The methods used for realizing these requirements are discussed in this chapter. Block diagrams for systems functions are shown here with detailed circuit diagrams given in the appendices.

3.1 Frequency Requirements

The frequency requirements are set to minimize the distortion effects introduced by sinc envelope distortion, foldover of secondary spectra into the output band, and sampling effects. Table 3.1 defines the frequency parameters and Tables 3.2 and 3.3 give the necessary relations for periodic modulation signals and finite time length aperiodic signals.

The specific design parameters for the prototype system are given in Table 3.4. These parameters were chosen in the following manner. First, it was decided that a DELTIC compression ratio of N = 200 and a DELTIC clock rate of $f_s \doteq 100$ KHz would be used. The value for N gives a large enough SNR improvement factor to dramatically illustrate the utility of the system. Choice of this frequency allows system development without

Table 3.1 Glossary of Terms

Precompression parameters:

T = Effective time storage length(gate) of DELTIC.

T_o = Period of periodic modulation signal

$F_o = 1/T_o$ = Fundamental frequency of periodic modulation.

τ_o = Time duration of aperiodic signal.

F_c = Signal carrier frequency.

F_1 = IF on reference channel.

F_{x1} = LO frequency on reference channel.

$(F_1 = |F_c - F_{x1}|)$

F_2 = IF on signal channel, assumed $F_2 > F_1$.

$(F_2 = |F_c - F_{x2}|)$

F_{x2} = LO frequency on signal channel.

$F_\delta = F_2 - F_1 = F_{x1} - F_{x2}$ = Difference frequency

$F_\sigma = F_2 + F_1$ = sum frequency

W = Signal bandwidth (total width of carrier).

T_s = Time between samples.

R = DELTIC recirculation (serial readout) time.

$(R = T_s)$

$F_s = 1/T_s$ = Sampling rate.

N = DELTIC time compression factor, $N = T/R = TF_s$.

Post compression parameters:

S = Sampling period of DELTIC output, $S = R/N$.

$f_0 = NF_0$

$f_1 = NF_1$

$f_2 = NF_2$

$f_\delta = f_2 - f_1 = N(F_2 - F_1) = N(F_{x1} - F_{x2}) = NF_\delta$

$f_\sigma = f_2 + f_1 = N(F_2 + F_1) = NF_\sigma$

Table 3.2 Necessary Frequency Relationships for Periodic Modulating Signal.[9]

1. $f_\delta = \frac{r_m}{R} + F + \frac{W}{2}$ r_m is an integer	Minimizes sinc envelope distortion and reduces extraneous primary spectral components.
2. $f_\delta > \frac{N}{2} W + \frac{5}{R}$ * or $F_\delta > \frac{W}{2} + \frac{5}{NR}$	Precludes foldover of positive secondary frequency components into band of interest.
3. $F_s > 2(F_2 + W)$	Sets minimum sampling rate.
4. $F_1 > \frac{W}{4N} + \frac{5}{NR}$	Sets minimum IF.
5. $F_s >> F_\delta$	Prevents zero-order hold distortion.

Note: It is assumed here that F_0, F_1, and F_2 are located at the left edge of the passband for the positive frequency portion of the spectrum.

*Careful design, i.e. choice of frequencies and the output BPF, can relieve this restriction.

Table 3.3 Necessary Frequency Relationships for Aperiodic, Finite-Duration Signal.[9]

1. $f_\delta = \frac{n_m}{R} + F_2$ n_m is integer.	Minimizes sinc envelope distortion.
2. $f_\delta > \frac{N}{2} W$ $F_\delta > \frac{W}{2}$	Precludes foldover of secondary components into output band.
3. $F_s > 2(F_2 + \frac{W}{2})$	Sets minimum sampling rate.
4. $F_1 > \frac{W}{2}$	Maintains the narrowband nature of the IF signals
5. $F_s >> F_\delta$	Prevents zero-order hold distortion. Not a rigorous requirement and can be compensated with more complex output BPF.

Note: It is assumed that the memory length matches the signal duration, $T = \tau_o$, and that F_c, F_1, and F_2 are located at the center of the signal passband.

Table 3.4 Summary of Digital System Design Parameters.[9]

Item	Values of Clock Divide Ratio and Frequency
System Clock	$F_x = 4.88772$ MHz
Reference LO	$N_1 = 2000$ $F_{x1} = F_x/N_1 = 2443.86$ Hz
Input LO	$N_2 = 2008$ $F_{x2} = F_x/N_2 = 2434.12$ Hz
Deltic Clock	$N_3 = 54$ $f_s = \frac{1}{S} = F_x/N_3 = 90.513$ KHz
System Sampling Rate	$N = 200$ $F_s = \frac{1}{R} = \frac{f_s}{N} = 452.57$ Hz
Digital Filter Sampling Rate	$\frac{1}{T_1} = \frac{f_s}{2} = 100\ F_s = 45.257$ kHz

Resultant System Parameters:

Center of input signal band	$F_c + \frac{W}{2} = 2573.35$ Hz
Difference Frequencies	$F_\delta = F_{x1} - F_{x2} = 9.74$ Hz $F_\delta = NF_\delta = 1948$Hz
Equivalent DELTIC Memory Length	$T = NR = \frac{N}{F_\delta} = 0.442$ sec

confrontation with serious circuit design problems which would dilute the efforts in the main scope of work for the first development phase. Final choices of frequencies were tailored to use a specific system clock crystal (4.88772 MHz) with convenient divide ratios for the down counters and to meet the criteria set in Table 3.2. The use of a single system clock may be unnecessarily restrictive for the most compact timing circuit implementation.

3.2 Partitioning of Prototype System

After preliminary investigations, it was decided to partition the prototype into analog and digital subsystems as illustrated in Figure 3.1. In order to test the theoretical performance model with respect to output noise behavior, three different input BPF's are used to shape the input noise spectral characteristic and two output BPF's are used. Only one input into the digital subsystem is required since the test signal is steered to the signal or reference DELTIC internally. The input and output BPFs, the input summer and clipper, and the output envelope detector are analog circuits. The remainder of the DELTIC DFPCC system consists of digital circuits. A special test signal generator was also designed and constructed, and this is a hybrid digital-analog subsystem.

3.3 Analog Subsystems

The analog subsystems are described in more detail in the block diagram of Figure 3.2 and the circuit diagrams in Appendix A. The input control switch allows the choice of either no noise or filtered noise from one of three input BPFs. When the signal is to be loaded into the reference DELTIC, no noise is desired; otherwise, the filtered noise is added to the signal, clipped and loaded into the system. The noise

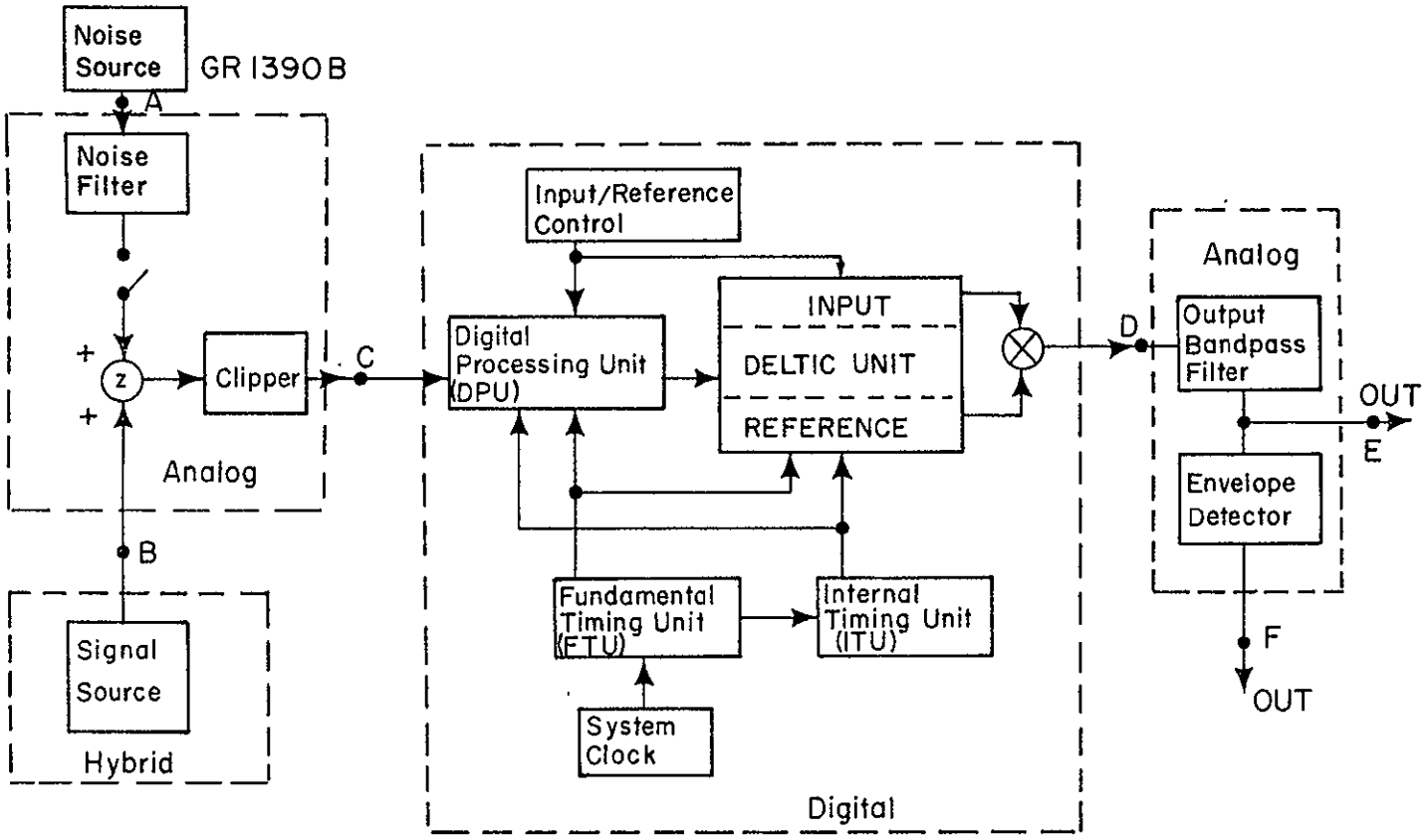


Figure 3.1 Partitioning of Prototype System into Analog and Digital Subsystems.

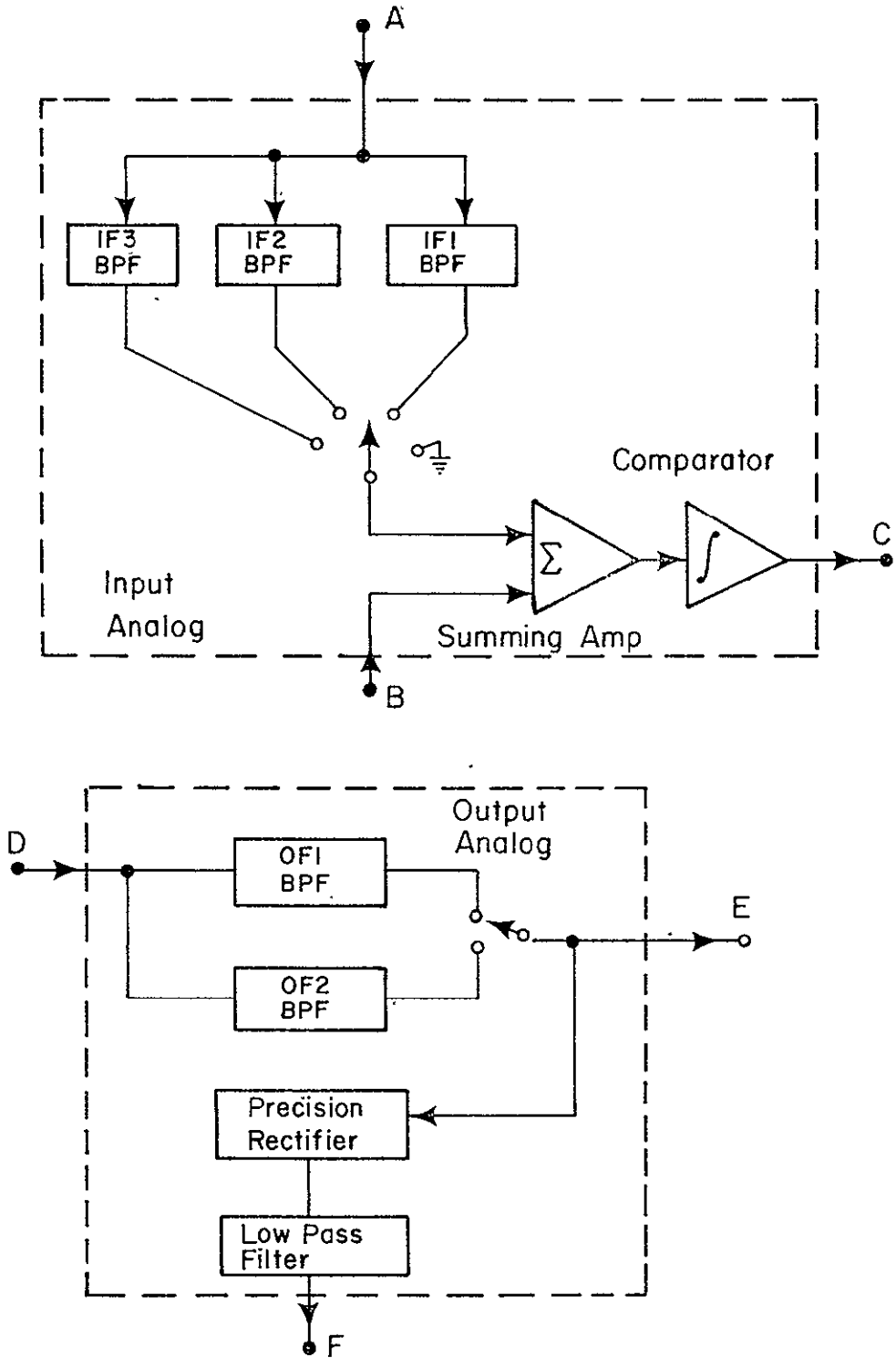


Figure 3.2 Block Diagram of Input and Output Analog Subsystems.

source was a GR 1390-B random noise generator. Table 3.5 describes the characteristics of all the BPF's as well as the envelope detector filter. The input BPF's have relatively simple characteristics while the output BPF's are more complex, since each must reject the distortion components introduced in the DELTIC operations.

The input clipper is an analog comparator, and the output detector utilizes a precision rectifier followed by a low pass averaging filter. The broad band nature ($Q \cong 10$) of the output spectra precludes the use of a simpler detector, such as the linear envelope detector. Inspection of the characteristics in Table 3.5 shows that the low pass filter requirements are rather severe in order to recover the modulation signal.

All of the filters are realized with active RC network techniques utilizing IC op amps. These circuits can be microminiaturized using hybrid technology so that the size of the analog circuitry is more compatible with that for a LSI implementation of the digital circuitry.

3.4 Digital Subsystems

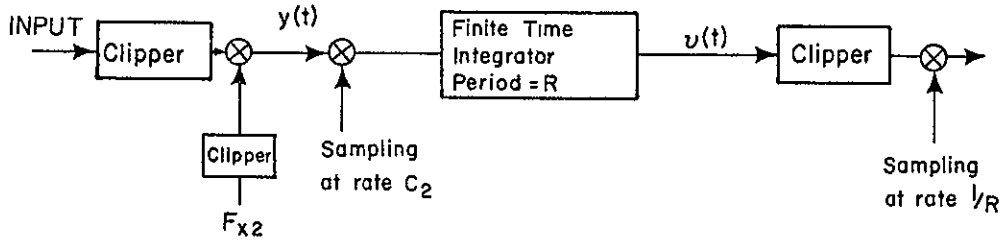
The digital subsystems consist of three major parts: (A) the digital processing unit (DPU), (B) the DELTIC memories with input gating and recirculation control, and (C) the timing unit which generates the required waveforms for (A) and (B). These subsystems are discussed in the following and complete logic diagrams for each unit are given in Appendix B.

A. The DPU (Figure 3.3)

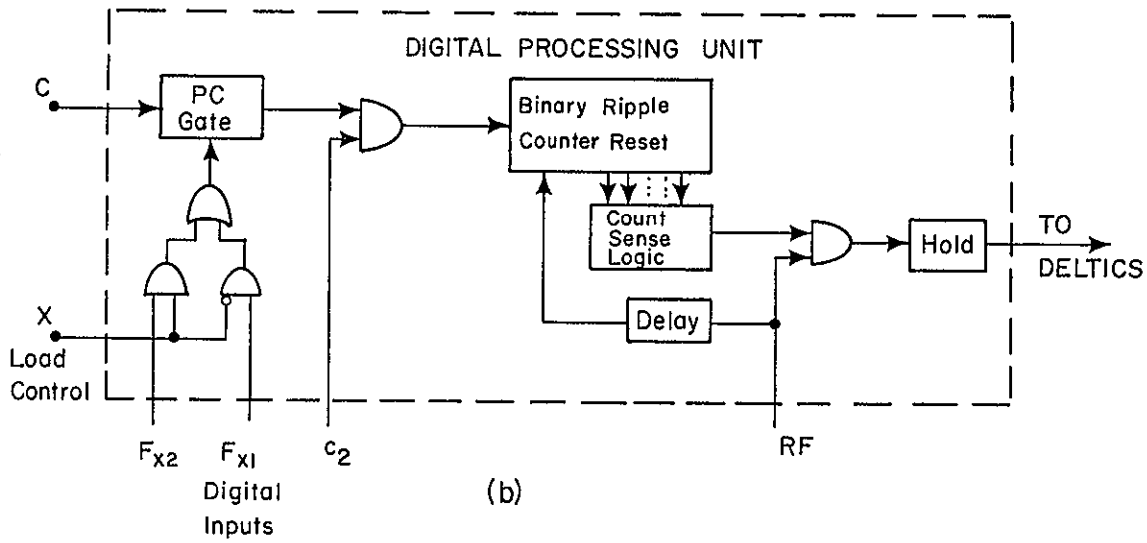
This subsystem represents a significant contribution to the realization of an LSI implementation of the DELTIC DFPCC. It replaces the action of mixing, low pass filtering, and clipping shown in Figure 2.1. Normally

Table 3.5 Analog Filter Specifications for Prototype System.[9]

Filter	Center Frequency Hz	Bandwidth Hz	Comments
IF1	2573	100	Single tuned stage
IF2	2573	64	Two-stage synchronously tuned
IF3	2573	500	Two-stage stagger tuned Butterworth
OF1	1948	100	Chebyshev, .3 dB ripple (4 pole BPF) -30 dB at $\Delta f = \pm 450$ Hz
OF2	1948	250	Equal (.3 dB) ripple (6 pole BPF) -30 dB at $\Delta f = \pm 350$ Hz Nulls at $\Delta f = \pm 450$ Hz
LPF for Envelope Detector		500	4 pole Chebyshev with 1/2 dB ripple. -44 dB at 1500 Hz



(a)



(b)

Figure 3.3 (a) Equivalent Operation of DPU.
(b) Equivalent Digital Implementation.

these operations would require a multiplier, an analog low pass filter, and an analog clipper. The equivalent action required is as follows: A "square wave" from the first clipper is mixed with a square wave LO, and the resultant is LP filtered to preserve only the difference frequency band. This is again clipped so that the output is again a "square wave" with the frequency shifted. The action of the DPU can be understood from the following argument.

It is helpful to consider a hypothetical sampled data implementation of the desired function which is illustrated in Figure 3.3(a). Because of the operational complexity, only square wave inputs to the mixer are considered. The first sampler operates at a rate $C_2 = N_o/R$ ($N_o = 100$), and the finite time integrator, with integrating time R, will smooth the sampling and eliminate most of the components from the mixer except for the difference frequency $F_c - F_{x2}$ and odd harmonics thereof. Whelchel[9] has shown that the output of the integrator would be a parabolic shaped waveform with fundamental frequency $F_c - F_{x2}$. This waveform is then clipped and sampled at the rate 1/R to obtain the desired DELTIC input.

The mathematical form for v(t) at sampling time $t_m = mR$ is:

$$v(mR) = \frac{1}{R} \sum_{n=(m-1)N_o+1}^{mN_o} y(nT_1) \qquad (3.1)$$

where $N_o = R/T_1 = C_2R$. This sum accounts for the finite time integrator operation on the samples of y(t). These samples have binary values so that summing of positive and negative samples is equivalent to counting positives (binary "1's") and subtracting a bias. If N_p is the number of positives and N_n the number of negatives, then $N_p + N_n = N_o$. Therefore, $N_p - N_n = 2N_p - N_o$, and, when $N_p = N_n$, both are equal to $N_o/2$. It then

that the sign of v(t) is positive when $N_p > N_o/2$ and negative when $N_p < N_o/2$. Thus counting the pulses and comparing to the reference count $N_o/2$ is equivalent to determining the polarity of v(t). One final point is that the sum in the finite time integrator extends over only one period of R. Thus the integrator contents at time mR is a completely new set of samples from those at (m-1)R. It then follows that counting the pulses as they occur over the interval of length R and then resetting the counter is equivalent to summing samples at the end of the interval. Figure 3.3(b) shows the block diagram of the counter and the threshold count logic for determining the corresponding polarity of v(t).

The analysis of the DPU action for a complex signal is intractable; however, Whelchel used a digital computer simulation for a linear FM waveform to show that the scheme would work before the system was designed.

B. The DELTIC Unit (Figure 3.4)

The output of the DPU is fed to the DELTIC unit where, according to the load control variable x, it is loaded either into the signal channel or reference DELTIC. When the sampling pulse $\overline{R}$ appears, loading is from the DPU and a sample is gated into the SR. During the next sampling interval the register contents are recirculated from either the last or next to last tap. The reference unit is loaded one time, and thereafter it continues to recirculate while the signal unit is loaded every sample period.

C. The Timing Unit (Figure 3.5)

This unit supplies the digital waveforms required in the DPU and DELTIC unit. All waveforms are derived from a single system clock as indicated by divide counters and logic gating.

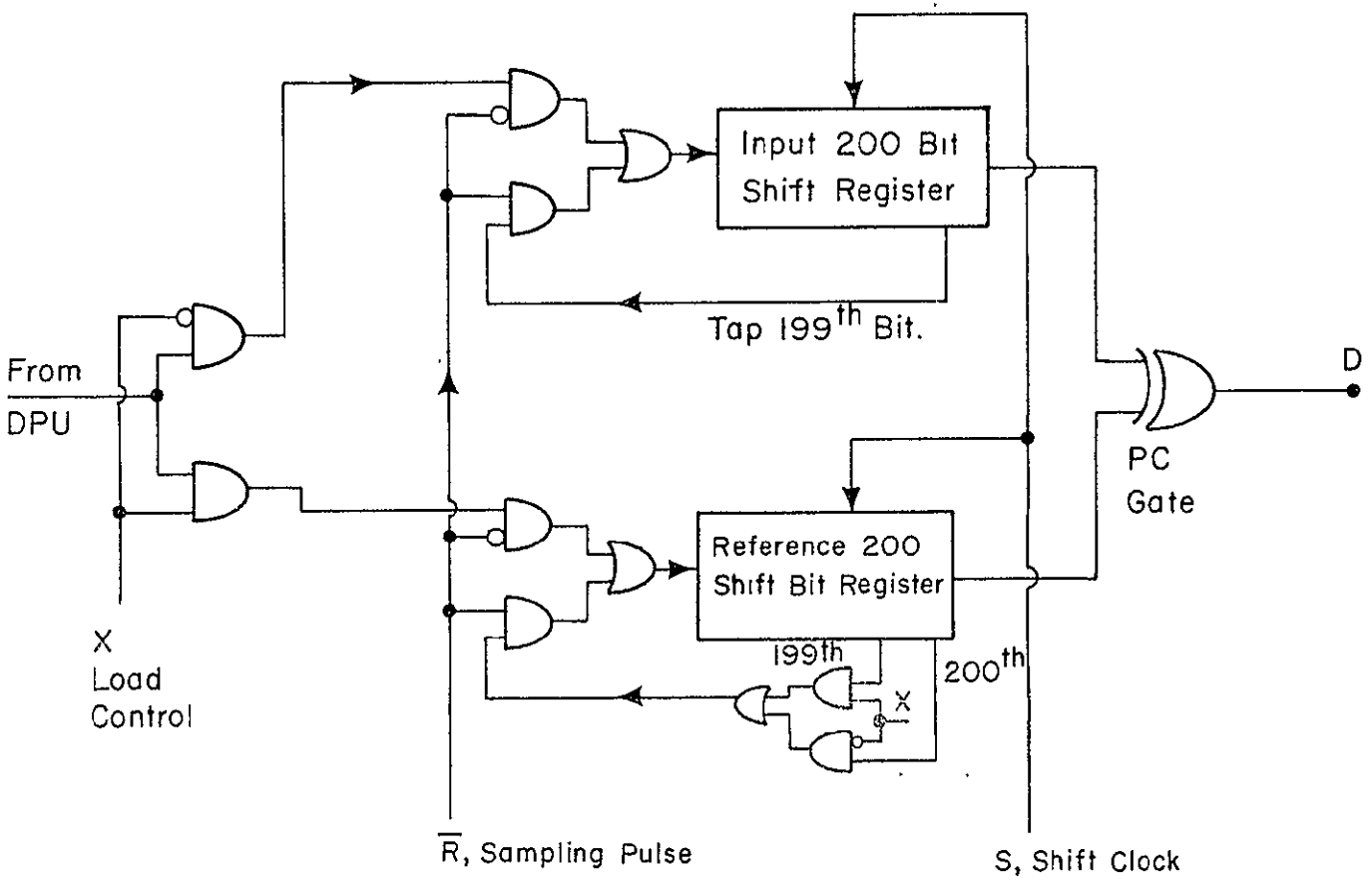


Figure 3.4 Equivalent Logic of DELTIC Memory, Load Control, Sampling, and Serial Output.

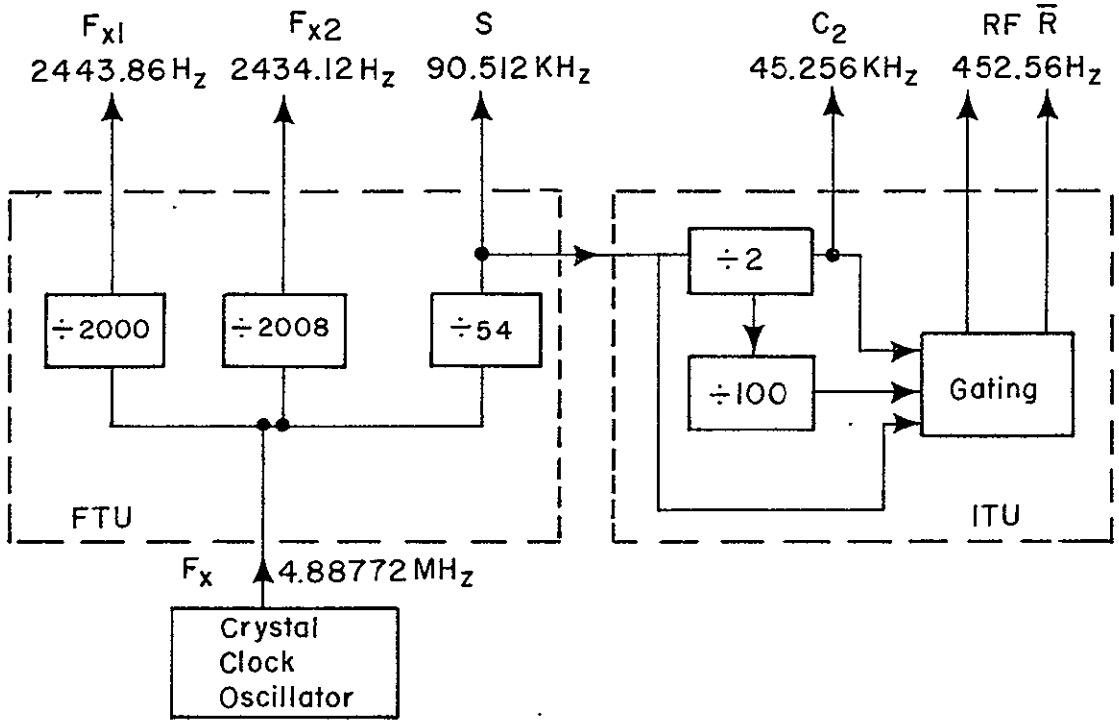


Figure 3.5 Block Diagram of Timing Units.

F_{x1} - Reference channel LO

F_{x2} - Signal Channel LO

S. - DELTIC shift register clock

C_2 - Sampler gate frequency for DPU

RF - DPU reset signal.

$\bar{R}$ - Recirculation and input sampling control for DELTIC

The digital subsystems were all designed using CMOS digital circuits. The DELTIC shift registers were constructed with 64 and 4 bit registers and D-type flip-flops. Special DELTIC shift registers, including the gating, were also constructed in LSI using PMOS logic cells but have not been tested in the prototype at this time.

3.5 The Test Signal Source

A linear FM sweep signal was chosen for the test signal mainly because it was believed that this represented an opportunity to obtain new results.* Other researchers had published data on pseudo random noise signals and it was known that the performance model agree well with that data.

The original intent was to use a commercial sweep generator; however, the frequency stability was inadequate for the requirements of this work. Attempts to stabilize the generator using usual methods were unsuccessful so that a generator was designed and constructed using the following scheme.

The procedure was to design a step-wise linear FM sweep. In principle, the sweep interval is divided into 8 equal parts, and during each subinterval the instantaneous frequency is the value which would fall on a linear sweep during the interval. This is implemented by dividing the system clock with a programmable counter. During each subinterval the counter is programmed to divide by the proper ratio. In fact the intervals are chosen to correspond to the complete number of cycles which is nearest to the desired interval division. This does not cause any great difficulty with respect to linearity of the sweep, and it does preclude phase discontinuities in the waveform. If phase discontinuities were

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*Recently, results were transmitted to us which were obtained by others for the LFM case.

allowed then the waveform after filtering would contain "glitches" where the amplitude drops out. Therefore this was to be avoided. Finally the digital waveform is filtered in a bandpass filter to obtain a smooth signal nearly sinusoidal in waveform.

The hybrid analog-digital test generator is described in more detail by the diagrams in Appendix C.

3.6 Summary

The necessary frequency relationships for the DELTIC PCC were given in Tables 3.2 and 3.3. Requirements for the analog filters were given in Table 3.5. Digital implementation of the prototype system was accomplished with CMOS SSI, MSI, and LSI circuits as described in this chapter. Appendices A, B, and C give the circuit diagrams for the analog and digital circuitry for the DELTIC DFPCC prototype and the stepwise Linear FM sweep generator constructed for testing the system.

It should be noted that the design and implementation effort for this system ran parallel with the theoretical work, with some lead time for the latter. Consequently all the theoretical results were not available when many decisions for implementation were required. In particular, the requirement of condition 2 in Table 3.2 was not known until the configuration was fixed for this effort. It will be observed that the DELTIC difference frequency should have been approximately 5 times higher than the value used in order to prevent distortion components of the positive secondary frequency terms from folding into the output band. This caused more self noise than could have been achieved with condition 2 met.

4. EXPERIMENTAL RESULTS

The objectives of the experimental program were two-fold. First, it was obviously desirable to experimentally verify the implementation concepts for the system and determine the significance of assumed second order effects which could not always be acounted for in analysis. Second, since analysis of the system for design purposes had resulted in a new model for predicting system performance, it was desirable to determine the validity of the model. The experimental test program was designed to first check the theory for the mean correlation spike height as a function of input SNR for both sinewave and LFM inputs. The second feature was the measurement of output noise with only noise present at the input. The results are given in the following sections. Figure 4.1 shows photographs of the experimental set up and the breadboard.

4.1 Qualitative Behavior.

Figure 4.2 shows the DFPCC output for a sine wave input. The output is sinusoidal as predicted by the theory. Figure 4.3 shows the output of the system when it is modified to operate as a true polarity coincident correlator (true PCC).* The output of the true PCC for a sinewave in is a triangular waveform as predicted by theory. Figure 4.4 shows the DFPCC output for the LFM input with no noise at the input. The correlation spike is present in a background of self-noise for the system. The smaller pre-spike is associated with the spill-over of secondary frequency components into the output band which Whelchel has analyzed in terms of ambiguity functions.[9]

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*Reference 9 may be consulted for more details. Whelchel has shown that the system constructed can be easily modified to operate as a true PCC.

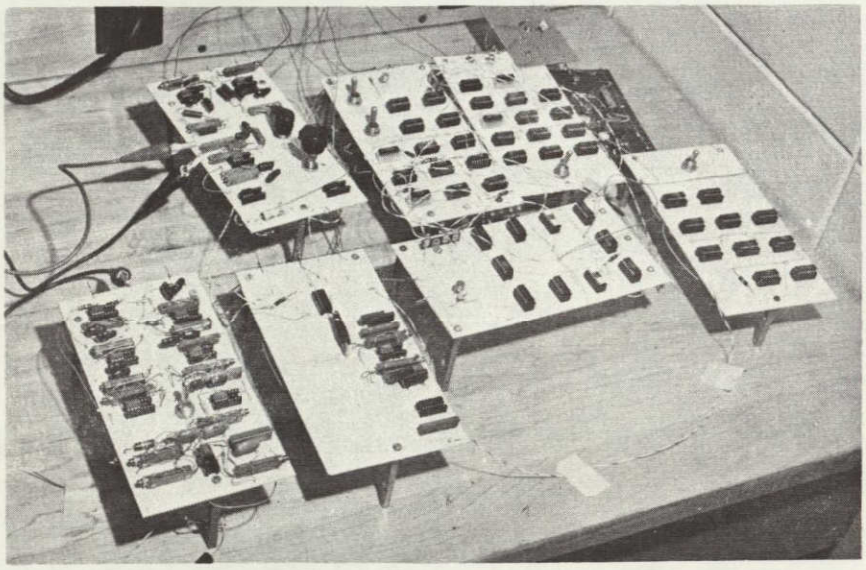


Figure 4.1 (a) Experimental Setup
(b) Breadboards.

Vertical: 2v/div.

Horizontal: 0.2 msec/div.

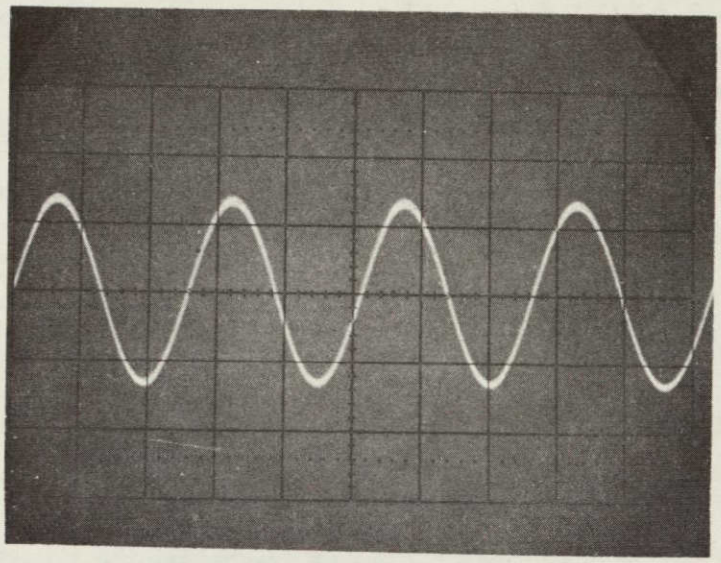


Figure 4.2 Output of DELTIC DFPCC with sinewave input.

Vertical: 1v/div.

Horizontal: 10msec./div

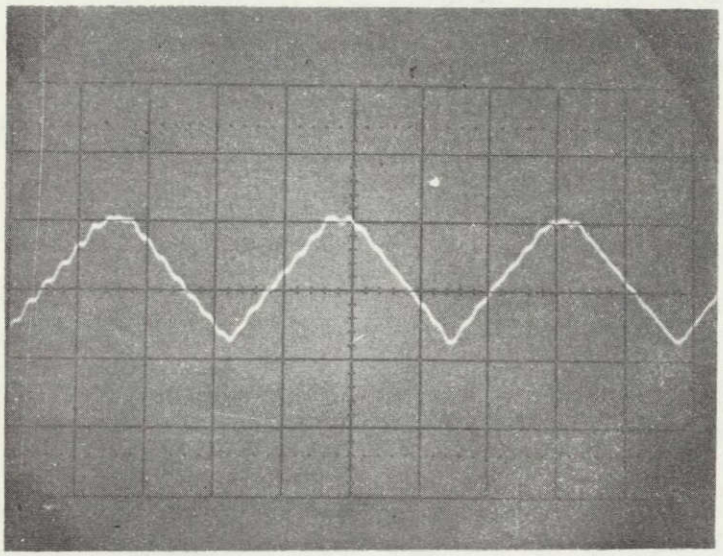


Figure 4.3 Output of System with Sinewave Input when Connected as a True Polarity Coincident Correlator. F_{x1} = 2443.86 Hz. Input from Wavetek 136, f ≐ 2475 Hz.

Vertical: 1 v/div.

Horizontal: 50 msec/div.

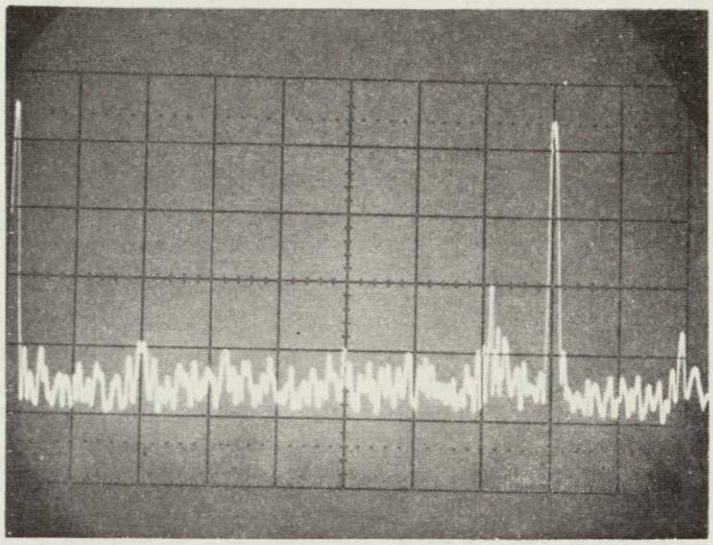


Figure 4.4 Output of DELTIC DFPCC with Stepwise Linear FM Input and Zero Noise.

Figure 4.5 shows a series of traces for the input signal plus noise for different input SNR's. This gives an indication of how the processor input appears in practice after the signal has been bandpass filtered to remove out of band noise of the receiver. Of course before this filtering operation the signal structure is completely buried in the noise background in a practical situation.

The sequence of photographs in Figure 4.6 shows the system output waveforms for an LFM input signal with various input SNRs. These traces show that the background noise level remains relatively constant while the correlation spike height decreases as the input SNR is decreased. Figure 4.7 shows the output waveform with noise only present at the input, and Figure 4.8 compares the output for noise only and signal plus noise at the input. Figure 4.9 shows the system output when operated with zero difference frequency as in the true PCC mode. The results in Figure 4.9 show a cluster of spikes which were of interest for establishing the validity of the ambiguity function theory for analyzing the effects of secondary frequency components.

4.2 Mean Correlation Spike Height.

The theory of operation developed by Whelchel predicted the ratio of the spike height, d, to the maximum value, d_{max}, observed with no input noise, i.e., $W_s(\lambda) = d/d_{max}$ where λ is the input SNR. Figure 4.10 shows the experimental dependence as compared with theory for all of the constant envelope data. Data for each individual experiment consisted of approximately 100 measurements taken from a memory scope and averaged. The second set of data was obtained by Navy Underseas Center[10] and we are grateful to Dr. C. E. Persons for permission to include the results. It

For all traces (multiple exposure):

Vertical: 2v/div

Horizontal: 10 msec./div

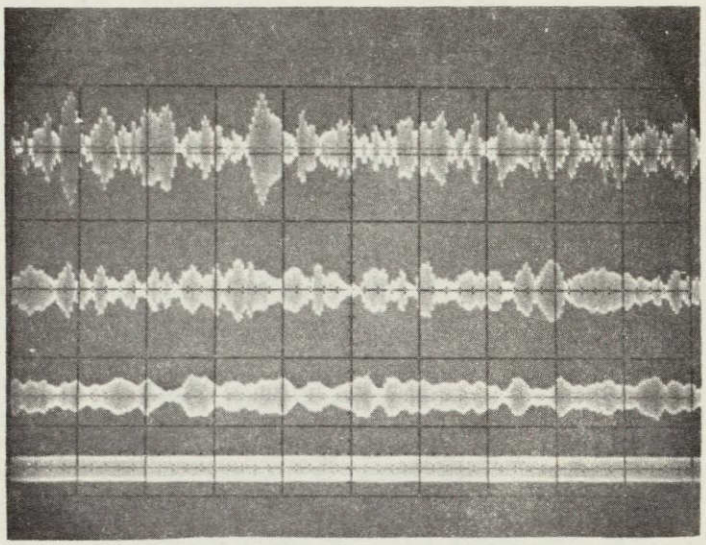
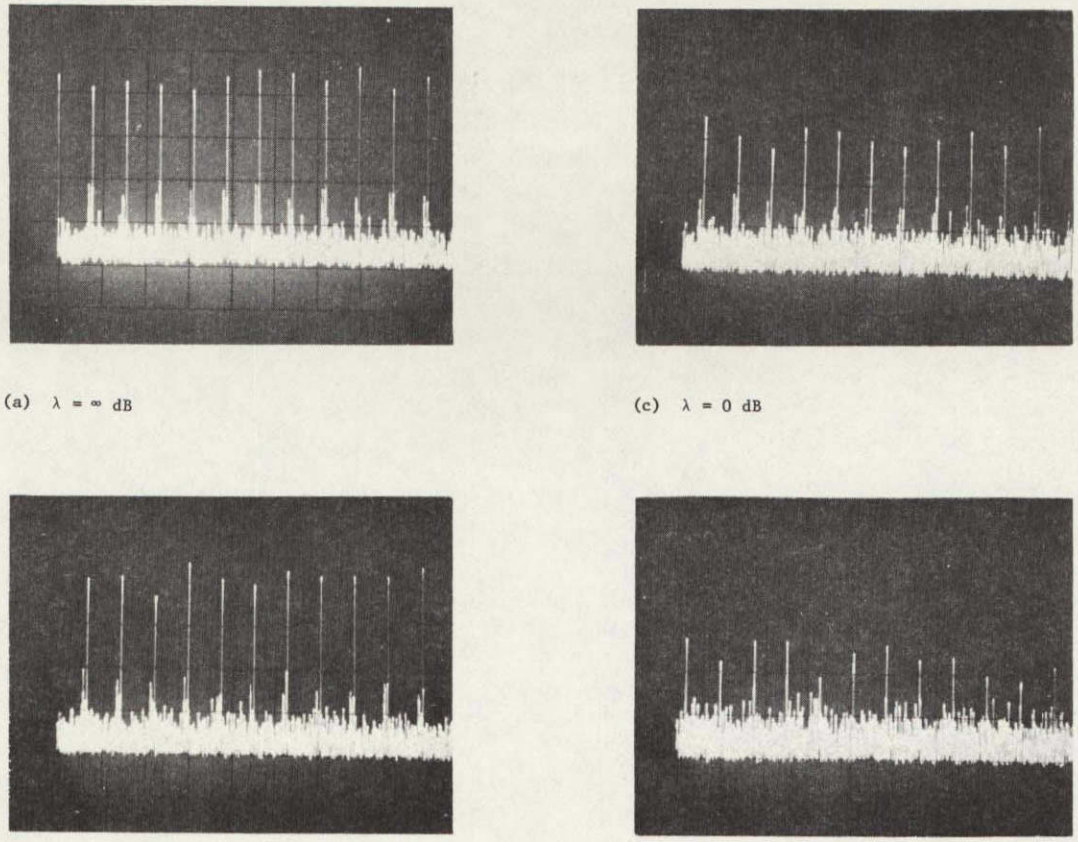


Figure 4.5 Waveforms for input Signal Plus Noise with Filter IF3 Taken at Output of Summer Before Clipping. Top to Bottom, the Input SNRS are - 6 dB, 0 dB, + 6 dB, ∞ dB.

Vertical: 1 volt/div. Horizontal: 0.5 sec/div.



(a) $\lambda = \infty$ dB

(c) $\lambda = 0$ dB

(b) $\lambda = +6$ dB

(d) $\lambda = -6$ dB

Figure 4.6 Output Waveforms from Detector with LFM Input.

Vertical: 1 v/div.

Horizontal: 20 msec/div.

(Multiple exposure)

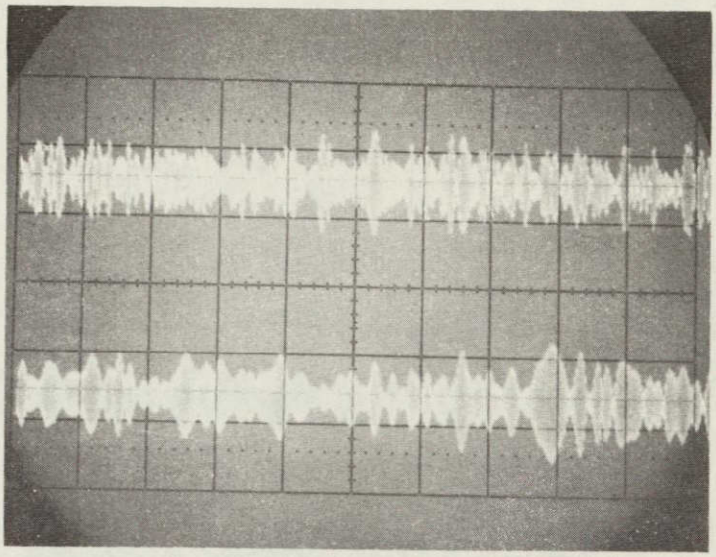


Figure 4.7 Noise only waveform for DELTIC DFPCC with Stepwise Linear FM Store in the Reference DELTIC. Top trace: system input noise from filter IF 3 at comparator input. Bottom trace: system output noise from OF2 output before detection.

Vertical: 1 v/div.

Horizontal: 0.2 sec/div

(Multiple exposure)

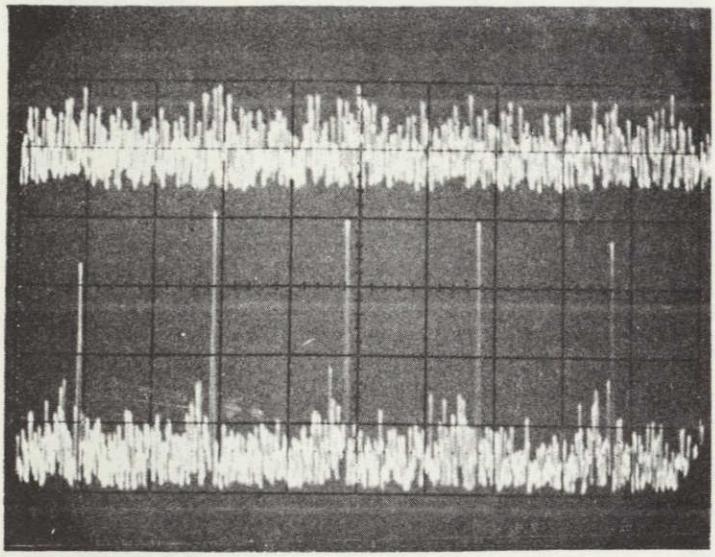


Figure 4.8 Waveforms at DELTIC DFPCC Output. Input Noise from IF3, Input signal is stepwise linear FM. Top trace: noise only at input, Bottom trace: signal plus noise, SNR = 0 dB.

Vertical: 1 v/div

Horizontal: 0.5 sec/div

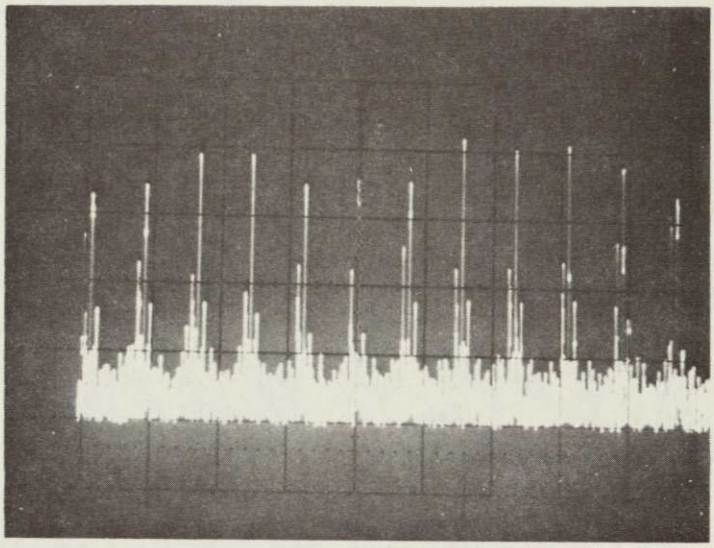


Figure 4.9 Envelope detector output of DELTIC system with $f_\delta = 0$ and signal only on input. Signal is stepwise linear FM. For this case, $c_1 = F_{x1} = 2443.86$ for both input and reference channels. The larger spike corresponds to the ambiguity function $x(\tau,4)$. The spike at the center of the screen is obscured by a vertical graticleline.

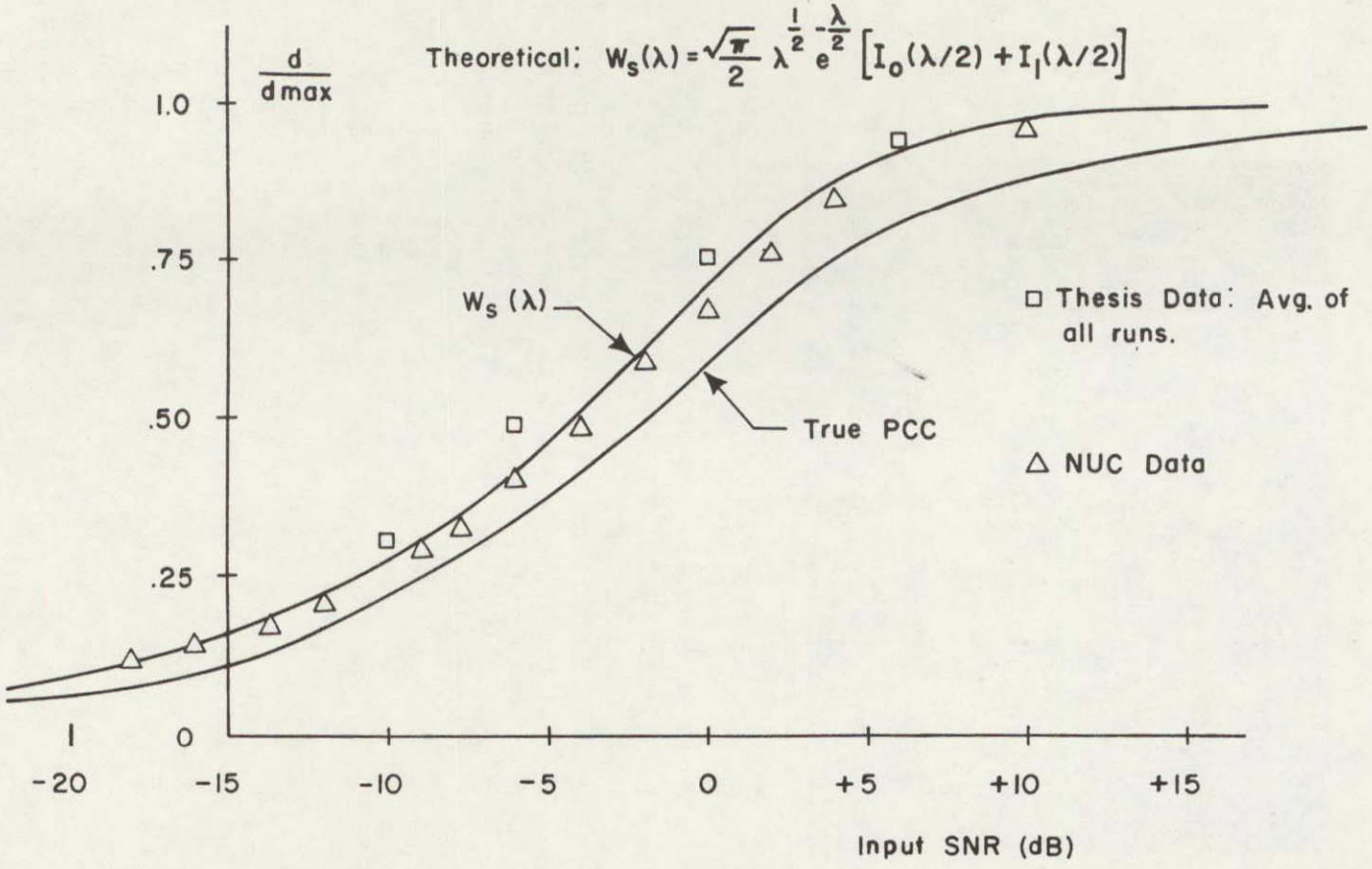


Figure 4.10 Experimental data for dependence of correlation spike height on input SNR for constant envelope signals. I_0 and I_1 are modified Bessel functions of the first kind.

should be noted that the NUC results are probably from a much larger data base than those obtained in this work.

Figure 4.11 shows curves for two different input filters. These results verify that performance depends upon the input SNR and not the details of the spectral structure for the noise not accounted for in the SNR determination.

Figure 4.12 shows d/d_{max} for pseudo-random noise (PRN) obtained by others, and Figure 4.13 shows the results for constant envelope signals plotted in the same format as Figure 4.12.

4.3 Noise Measurements

Attempts to read the noise at the output bandpass filter before the detector with a "true" rms meter were unsuccessful because of the random fluctuations were not smoothed sufficiently by the instrument available. This was particularly true for a sinusoidal reference signal. Consequently, the output of the envelope detector was filtered with a 10 second time constant filter to obtain rectified averaged noise measurements, $\bar{y}$. Figure 4.14 shows $\bar{y}$ vs. the input SNR for a sinusoidal signal in the reference channel.

The experimental results show that the output level is independent of the input level as predicted by theory. There is approximately 1.5 dB discrepancy between theoretical and observed values for filters IF1 and IF2.

The results for IF3 were worse, and the observations made here verified the necessity of checking out the theory by experiment. After observation of a discrepancy of several dB, an investigation was made for possible causes. It was found that the attenuation rate for filter

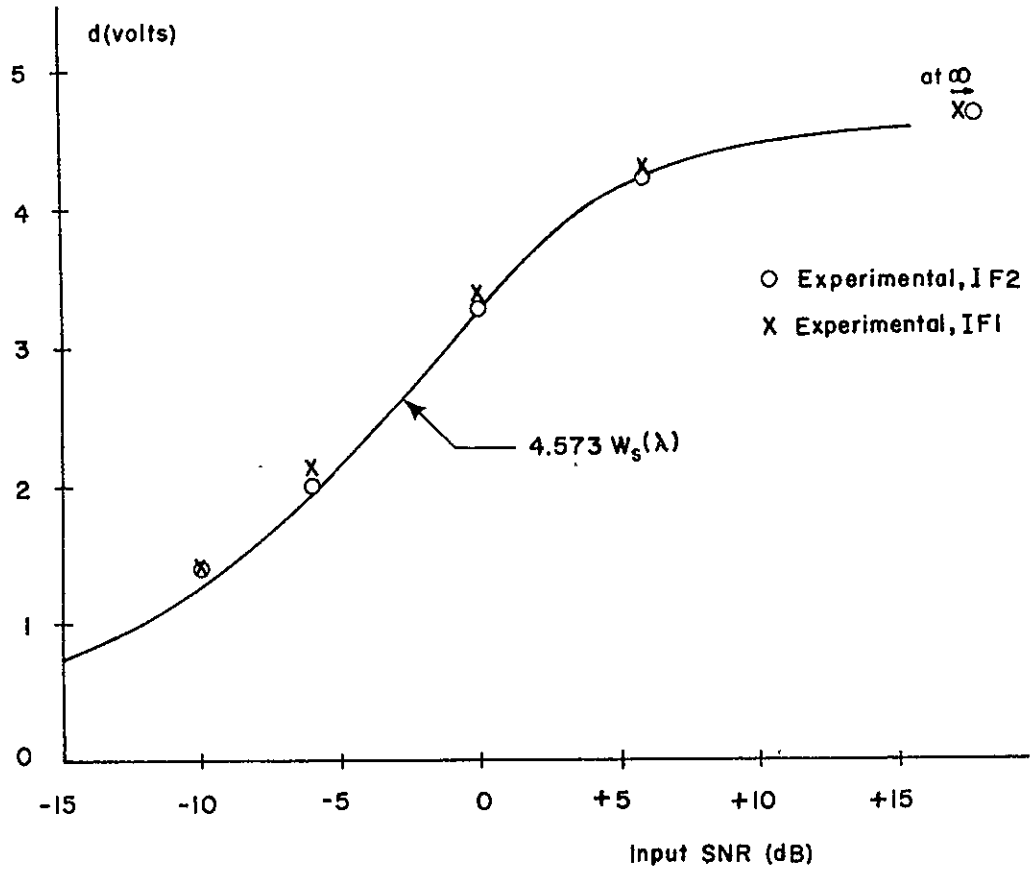


Figure 4.11 Unnormalized correlation spike height dependence on input SNR. Sinusoidal input and output filter is OF1. An offset correction of 0.087 Volts was applied.

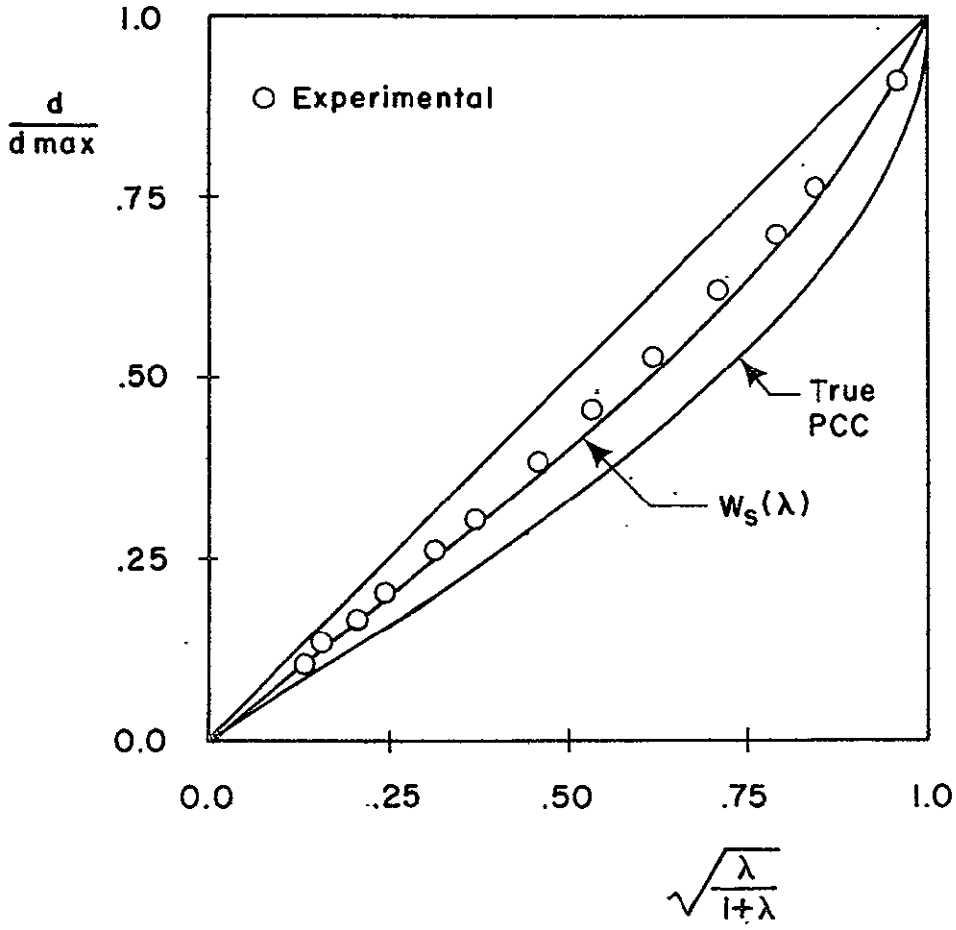


Figure 4.12 d/d_{max} dependence for PRN signals. Experimental data from Naval Underseas Center, San Diego. Theoretical curves:

$W_S(\lambda) = x^{\frac{1}{2}}[E(x^{\frac{1}{2}}) - (1 - x)\, K(x^{\frac{1}{2}})]$

$x = \lambda/(1+\lambda)$ and K and E are complete elliptic integrals of the first and second kind respectively.

True PCC: $d/d_{max} = \frac{2}{\lambda} \sin^{-1}\left(\frac{\lambda}{1+\lambda}\right)$

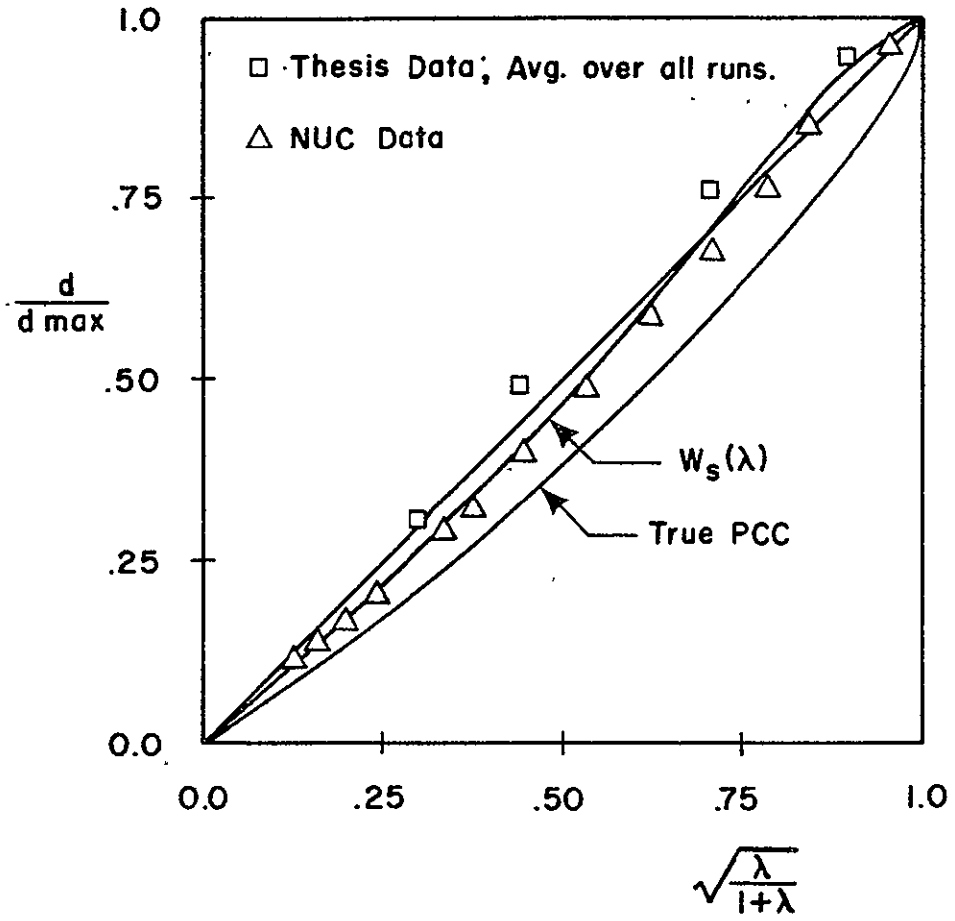


Figure 4.13 d/d_{max} dependence for constant envelope signals using same format as in Figure 4.12. See Figure 4.10 for theoretical curves.

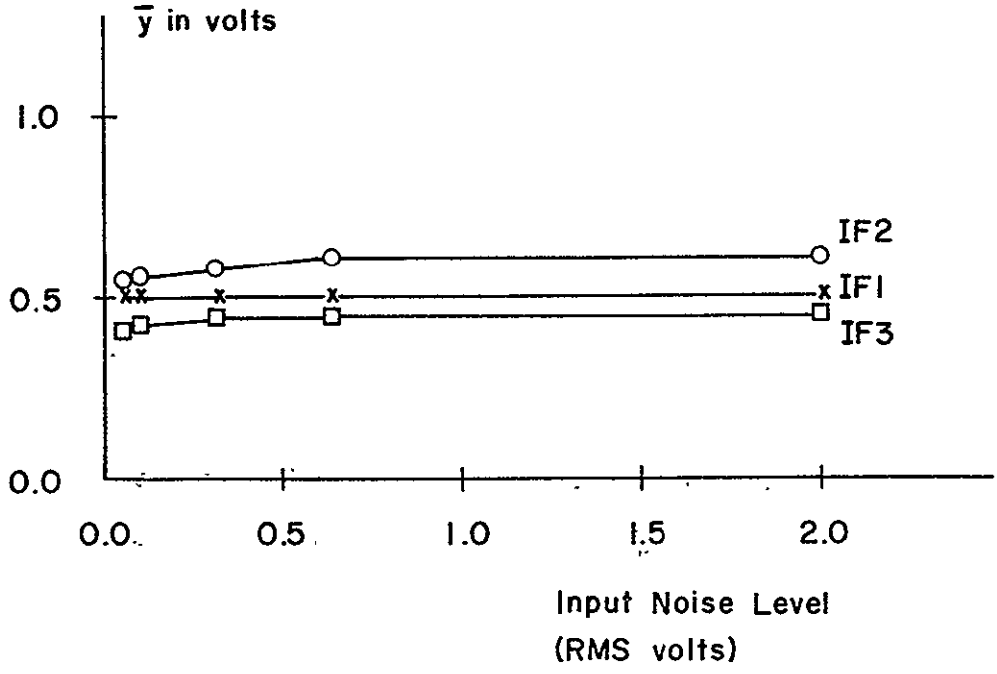


Figure 4.14 Output noise as function of input noise level with sinusoidal signal in reference channel. $\bar{y}$ adjusted by 0.087v offset of the envelope detector.

IF3 was insufficient to preclude a significant spill over of noise into the "negative frequency" region when the noise was heterodyned down to a lower IF; i.e., it did not preserve the narrow band characteristic necessary for a single sideband spectrum. Consequently, the negative frequency components "fold back" into the positive frequency region, and substantially, in this case, increase the noise in the system. This observation pointed out the need for considerable care in choosing the IF and designing the input bandpass filter characteristic. From the standpoint of practical design, this experimental observation made the experimentation very worthwhile.

4.4 Figure of Merit, λ_o

It was possible to estimate the noise output from the bandpass filter before the detector using a true rms meter when the stepped LFM was used in the reference channel. This allowed estimates of λ_o as follows. For a given input SNR, the rms voltage reading was taken without the signal present and then the spike height measured at the envelope detector output. Using the measured response function for the detector, the peak voltage value, corresponding to the spike height, at the bandpass filter output could be computed. From these two values the ratio d^2/σ_o^2 could then be computed. Figure 4.15 shows the experimental results obtained in this manner compared with the theoretically predicted value of λ_o, the figure of merit.

4.5 Conclusions

The experimentation confirmed that the basic implementation concept was sound and that the system was capable of dramatically improving the signal to noise ratio. Experimental results obtained in this work and

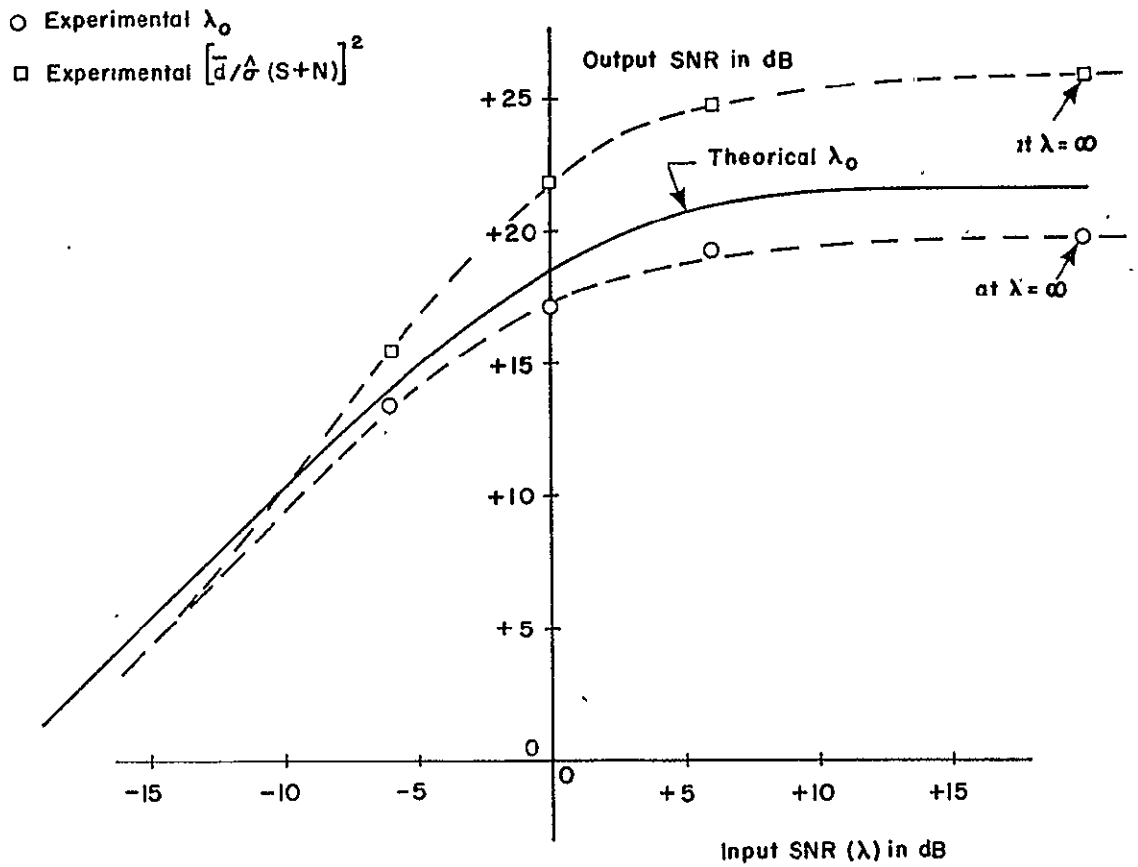


Figure 4.15 Comparison of theoretical and experimental output SNR, λ_0, for stepwise linear FM signal and input noise filter IF2. Experimental variance of correlation spike is also shown.

by others show that the theory of performance developed in the course of this work gives a good prediction of the expected value of the correlation spike as a function of the input SNR. The theory is experimentally valid for both constant envelope and PRN signals. The theory for the expected noise value was less successful; however, the figure of merit was still predicted to within 2 dB.

From a practical standpoint, the experimental observations were useful in establishing the importance of the frequency relationships and the input bandpass filter design in minimizing the output noise, which in some cases is the "self-noise" referred to earlier. The experimental results also helped to refocus theoretical attention on some of the second order effects. Future designs based upon the criteria established here will give better performance than observed in this work.

5. SUMMARY AND CONCLUSIONS

In this chapter the results obtained in this work are summarized and some conclusions are given with respect to the significance of the findings.

5.1 Summary of Results

The operation of a DELTIC DFPCC was analyzed theoretically, and it was found that the processor acts as an ideal correlator for a bandpass limited signal plus noise with a band pass limited reference signal. The output of the ideal correlator is contaminated with self noise due mainly to nonlinear distortion effects. Relationships for the system frequencies were given in Table 3.2 for minimizing the self noise. No quantitative theory of self noise is presently available.

Theoretical results were obtained for the expected value of the correlation spike and for a figure of merit involving an output SNR. A prototype system was designed, built using SSI, MSI, and LSI components, and tested. It was found that the theoretical model agreed very well with experimental results. It was also found that for the prototype system, the rms self noise was roughly 60% of the noise introduced directly from the input by correlator type action. This result was due to system design parameters which had to be fixed before all of the theoretical results were available. With roughly 2 dB increase in output noise due to this effect, the prototype system still gave an improvement of 20 dB in the output SNR with an input SNR of zero dB.

An important design consideration for the analog circuitry was emphasized by experimental observations. If the IF is chosen to be small in order to maximize the sampling efficiency, then considerable care must be exercised in designing the input filter. It is particularly important that a sharp low frequency roll off be obtained in order to preclude the fold back of negative frequency input noise components if the ultimate capability is desired. Filter characteristics with nulls, such as the output BPF used here, should be satisfactory.

The first steps toward an LSI realization of the system were taken by designing and constructing a PMOS DELTIC unit in conjunction with MSFC personnel.

5.2 Possible System Improvements

The complexity of the system can be reduced by use of two timing crystals with lower frequencies. Choice of one crystal was simply an expedient for this project.

The output noise of the system can be reduced further by increasing the output difference frequency. For a practical system the input BPF should be redesigned for a sharper low frequency roll off to minimize input noise.

5.3 Performance Limitations of the DELTIC DFPCC

There is a tradeoff in systems performance parameters for a given maximum DELTIC clock frequency, f_c. For the most straightforward design procedure that meets the criteria in Table 3.2:

$$W \leq f_c/3N \tag{5.1}$$

With some care W can be increased but cannot be greater than $f_c/2N$ in any case. Figure 5.1 shows the bandwidth achievable with various LSI technologies. Efficiency in utilization of the system requires that the signal time duration, T, match the DELTIC so that the maximum symbol rate, 1/T, is given by:

$$1/T = f_c/N^2 \tag{5.2}$$

For a maximum value of f_c achievable with a particular technology, equations (5.1) and (5.2) specify the tradeoff in speed and available SNR improvement. Determining an optimum tradeoff in a particular application may not be a trivial matter; however, in order to obtain representative numbers, assume $N = 200$ and $f_c = 100$ MHz. The value for f_c is representative for the best results reported for buried channel CCDs.[18] These values give $W \leq 167$kHz and $1/T \leq 2.5$ kHz as an indication of upper limits for this system with a processing gain of 133.

Although the tradeoff analysis may be complex and peculiar to each application, some generalizations are possible. Keeping in mind that the processor is essentially for FM signals, one may note the following. Generally there will be a minimum usable ratio of the bandwidth to carrier frequency because of frequency stability limitations of a given power source. Also for a practical power limited source, there is a minimum integration time at the receiver for a specified SNR attainable with ideal processing. Therefore, in a given application, there is a minimum TW product which can be used.

It is clear from the preceding that the DELTIC DFPCC is not suitable for processing communication signals with microwave frequency carriers. It is suitable for low frequency sonar systems. Between these

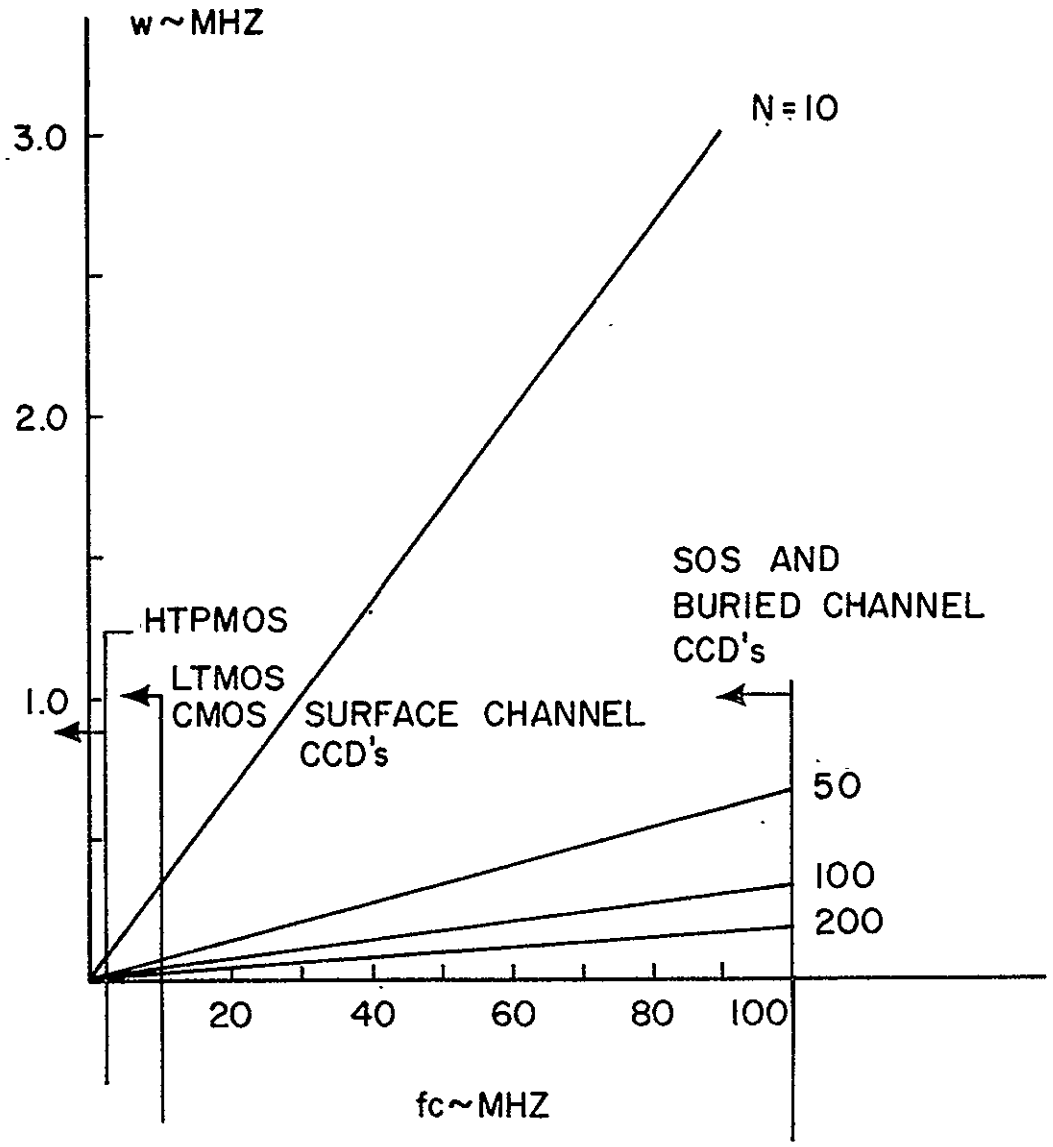


Figure 5.1 Bandwidth Achievable vs. DELTIC Clock Frequency.

Ranges specified represent current technological limits.

obvious cases is a wide frequency range for potential applications that require further consideration.

5.4 Comparison with Other Signal Processors

In this section the DELTIC DFPCC (referred to as DFPCC hereafter) will be compared with (A) CCD transversal filters, (B) parallel mode analog and (C) parallel mode binarycorrelators. Both systems (A) and (B) are capable of true analog processing for signals with information coded into amplitude. When this function is required, the DFPCC cannot be used and the systems cannot be compared. If the analog signals are phase or frequency modulated, the DFPCC can be used with some processing gain loss, approximately 3 dB.

A. The CCD Transversal Filter (CCDTF)

The obvious advantages of the CCDTF over the DFPCC are the relative simplicity of the timing requirements and higher speed capability. Lack of flexibility is a disadvantage.

The CCD requires a multiphase clock but only one clock frequency. The charge transfer clock frequency, f_c, is the sampling frequency; therefore, the maximum bandwidth which can be accommodated is $f_c(\max)/2$. In theory the bandwidth achievable is independent of the TW product with larger TW products achieved by increasing the length of the delay line. If this were true then the CCDTF could handle a bandwidth of $w \leq f_c(\max)/2$ as compared to $w \leq f_c(\max)/3N$ for the DFPCC. In practice the CCDTF will be limited because of the charge transfer efficiency (CTE) of the CCD.[11] When the CCD is used as a DELTIC, the CTE requirement is not so critical because the output pulse can be reshaped. In the CCDTF, the summation is an analog function which requires amplitude and phase fidelity even if the signals are ostensibly binary.[12] For binary signals the CCD can use refresh techniques and serially connected chips; however, simplicity is lost and, in any case, the advantage in speed is not as great as indicated above.

The main disadvantage of the CCDTF when compared to the DELTIC DFPCC is lack of flexibility. Practical implementations require on-chip realization of the tap weights. One practical implementation reported utilizes the charging currents to split transfer electrodes to realize both positive and negative weights.[4] This scheme appears particularly attractive for binary level signals. Once the tap weights are set, there is no simple means for changing them. The clock frequency can be changed to expand or compress the filter impulse response, but this is the extent of the flexibility for application. In the following, two schemes are discussed which could utilize CCD's and provide programmed tap weights. These systems are more properly referred to as correlators.

B. Parallel Mode Analog Correlators (PMAC)

This type of correlator operates in a sampled data mode but with a continuum of signal levels; therefore, analog memories are required for the input and reference signals. Typically a large number of samples are required and each memory cell must be accessible in a parallel mode. This requires that both memories be on the same chip, although a serial connection of chips, each with segments of both memories, is feasible. Since the signal memories do not require long lifetimes, the CCD delay line with taps can serve this purpose. There is no effective means at this time for refreshing the CCD memory with analog contents so that a recirculating CCD memory is not practical for the reference. Efforts have centered on utilizing memory devices with longer lifetimes that do not require constant refreshing.

It should be noted that there is a long history of R & D efforts to produce effective analog memories. Only the magnetic tape recorder and its derivatives have a proven track record. These systems are bulky,

require a considerable expenditure of energy in recording a signal segment, and utilize circuit techniques which are sophisticated when compared with digital circuit methods. Semiconductor devices which exhibit memory effects without a constant expenditure of power include the FAMOS element[13], the MNOS gate[14,3]; and ferroelectric gate field effect transistor.[15]

The FAMOS element has stable characteristics. It utilizes avalanching to raise the carrier energy high enough to go over the barrier of a gate oxide. The oxide is approximately 1000 Å thick and well within the range for which high quality oxides can be reproduceably fabricated. However, a considerable amount of energy (high voltage) is required for writing into the element. This mitigates against its use as an analog memory for reasons which will be apparent.

The MNOS memory element predates the FAMOS and recent developments have improved its stability.[16] However, the device phenomena utilizes tunneling through a thin oxide of approximately 100 Å. It remains to be proved that such oxides can be reliably produced. Furthermore, even with recent improvements, the MNOS device has a time decaying memory function which does not lend itself to simple writing methods. Both temperature and voltage stress still effect the memory element.

Ferroelectric memory elements have a long history of instability and have never shown great promise.

All of the above devices when used in a PMAC should be addressable for writing by a serial technique; otherwise, multiple external taps are required. Such a scheme could be practically implemented using a shift register for writing in digital data; however, the recording of analog levels using the devices above requires pulsing the device with amplitude or time width modulated pulses. This scheme does not appear to be

practical at this time. Therefore, it is concluded that the PMAC will require considerable more developmental effort before it will represent a practical option as a microminiaturized signal processor.

C. Parallel Mode Binary Correlators (PMBC)

The PMBC requires memories with binary valued elements, which moves it into the realm of immediate practicality for LSI. This type of system is not a true digital correlator but can serve as a useful processor for signals with information stored in the zero crossing, i.e., the same as the DELTIC DFPCC does. Binary values are obviously the natural results for semiconductor memories. Dynamic memories can be used with refresh techniques to obtain essentially infinite lifetime.[17] Therefore, charge storage as well as flip-flop techniques are useful.

There are probably several feasible structures for the PMBC. Recently such a system was described using surface charge transistors, SCT, for memory and gating.[2] In the system reported, the SCT could be used as an analog signal memory while the digital reference memory was a shift register. Obviously CCD's could be used in a similar manner. The advantage of retaining the analog character of one signal appears to be dubious according to the results obtained in this work which shows only a small loss in processing gain when both signals have binary levels.

The speed advantage for the PMBC over the DFPCC is not a factor of N as indicated by analysis of an ideal model. The problem of accurate analog summation manifests itself in different ways but will always limit the bandwidth to less than $f_c(\max)/2$, where $f_c(\max)$ is the ultimate sampling rate. For the CCD, the problem is charge transfer efficiency, and for the SCT it is the complexity of clocking the samples into a summation structure.

While the PMBC obviously has a speed advantage with respect to the DFPCC and is equally flexible, it does have a disadvantage. A larger number of components per sample processed must be included on the chip. Two memory functions, one gating function plus an addition per sample processed are required for correlation. It would seem probable that several series connected chips would be required to implement a practical processor. This solution is not without some difficulty. The summing action is a true analog function; therefore, chip matching or external trimming will be required for series connected chips. This does not appear to be a formidable problem, but it may not be trivial. Each serially connected chip would be relatively complex when compared with simple serial memory chips. Therefore it does not appear that production of such chips will be a trivial matter either. Yield problems could be anticipated which would increase the expense of the building block chip for PMBCs.

D Summary

In summary, for angle modulated signals the DELTIC DFPCC and the parallel mode binary correlator, PMBC, appear to be the most attractive alternatives. When bandwidth requirements are not too high, the DFPCC will be the simplest and most economical system for application. It is obviously a practical system which can be realized in LSI. The PMBC will have a higher frequency response capability, will be more complex, and may not yet be ready for extensive LSI manufacturing. It is clear that the PMBC system is practical, and it is simply a matter of resolving the best memory and gating structure for LSI implementation.

5.5 Further Development of the DELTIC DFPCC

A microminaturized version of the prototype system would be of interest for demonstration purposes. In such a system the analog circuitry would be realized using hybrid technology. All of the digital circuitry for the correlator and part, or all, of the timing circuitry would be achieved using LSI. Several MOS technologies are available for implementing the system. Those discussed in the following are: (A) high threshold PMOS, (B) low threshold MOS, (C) CMOS, (D) silicon-on-sapphire, and (E) CCDs.

A. High Threshold PMOS (HTPMOS)

With N = 200, the HTPMOS implementation would yield a system capable of handling a bandwidth of $W \leq 2$ kHz and symbol rates of 25 Hz for a DELTIC clockrate of 800 KHz. With a reduced clock rate, the bandwidth would be reduced and the averaging time increased accordingly. The next phase for development with HTPMOS would be LSI implementation of the DPU and the DELTICs. This would require three LSI chips with two of them identical. The two identical chips would make up the DELTIC unit. Figure 5.2 shows the simplified logic diagram of the DELTIC unit realized by HTPMOS. This circuit was designed and constructed at the MSFC monolithic facility during the summer of 1974. A photomicrograph of the circuit is shown in Figure 1.5. Two of these chips realize the DELTIC unit with all required gates so that an input can be accepted directly from the DPU and an output fed to the output BPF.

The third chip would realize the DPU function. The DPU design would be modified to operate with a 128 bit binary counter so that the threshold count of 64 could be sensed without logic gating. The PC and NAND gating and output buffering could be realized on the same chip as the binary

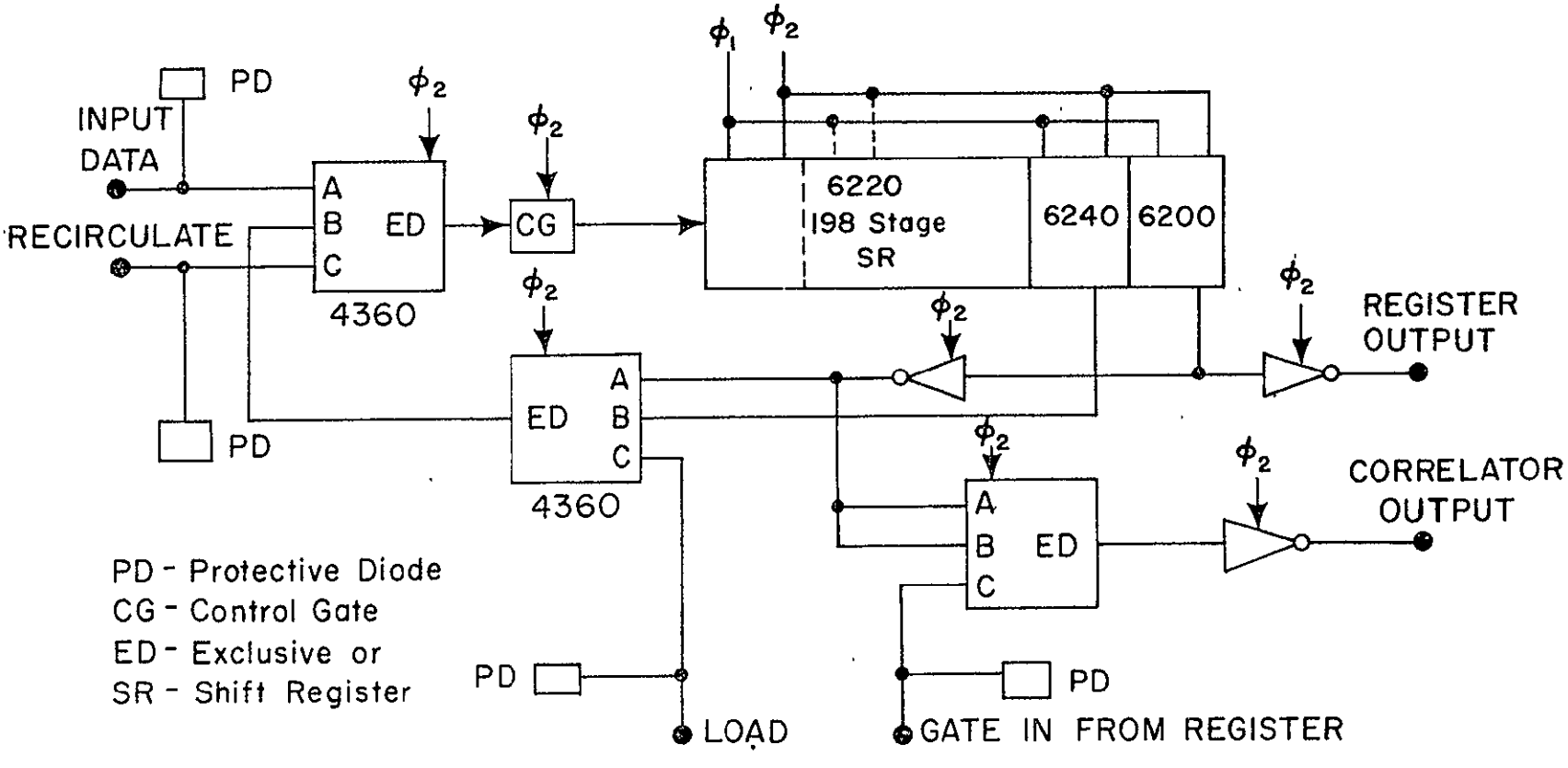


Figure 5.2 Simplified Logic Diagram for PMOS DELTIC.
Numbers are for Banning Cells.

counter. This chip would be roughly the same size and complexity as the DELTIC chips.

Realization of the timing circuitry by the HTPMOS process would apparently be more difficult. A second phase effort should consider the use of hybrid technology with CMOS MSI for realization of the timing circuitry.

B. Low Threshold MOS (LTMOS)

A gain by a factor of 5 or more in speed could be realized using LTMOS. If this project were undertaken, it would probably be done using an N-channel process with similar masks to those used for the HTPMOS. The timing circuitry should be realized with hybrid technology and MSI chips.

C. CMOS

The speed with this technology would be roughly equivalent to LTMOS; however, some added flexibility would be available. The circuit design and masks would of course be different than for LTMOS. All of the digital circuitry could be implemented in LSI. There would be two additional chips for timing circuitry. For convenient implementation, the timing circuitry would be redesigned with either two crystal oscillators or perhaps some analog mixing of the clock and clock derived frequencies.

D. Silicon-on-Sapphire

Using this technology a large increase in speed is possible; however, the circuit design problems would be much more subtle. Using CMOS structures the entire digital portion could again be implemented in LSI. It seems likely that analog buffers would be required for connecting the chips. Operation at the ultimate frequencies with this technology would

also require a redesign of the analog circuitry with particular attention given to the clippers.

E. CCD's

An implementation with CCD's would give performance capabilities in the range available with LTMOS and CMOS with ultimate performance in the range achievable with SOS. The main emphasis with CCD's, however, would be on circuit density.

A first phase effort with CCD's would be the realization of a DELTIC. Conceivably this could be either one or two chips. There is no reason to believe that the 200 bit DELTIC unit cannot be realized on one chip.

An implementation of the DPU using CCD's would be realized in a different manner than for the prototype. Using CCD's if would be simpler to realize the finite time integrator than to use the charge-coupled structure for a counter implementation. For the ultimate performance in speed the CCD finite time integrator would pose some problems; however, for moderate speeds it should be satisfactory..

The finite time integrator can be implemented without taps in the usual sense. Since all tap weights are equal, the charging current in one of the phase lines can be used for summing the delay line contents. However, using this technique, the DPU output would have to be fed to an analog circuit which couples the DPU and DELTIC units.

Ultimately, the DPU and DELTIC unit could be realized as one CCD chip. The DPU output would probably have to come off the chip to an analog circuit and then back to the DELTIC on chip. This scheme would result in an extremely compact signal processor. Timing circuitry could be realized with one or perhaps two LSI CMOS chips. By taking full

advantage of CMOS circuit capabilities, much of the analog circuitry now realized with bipolar IC's could be eliminated or made more compact.

5.6 Recommendations

The CCD technology appears to be the most promising method for fabricating dense signal processing circuits. Construction of a CCD DELTIC would be a first step toward realization of a DELTIC DFPCC. Since the DELTIC requires at least one tap plus some gating, the experience obtained in design and construction would be useful for later work in applications of CCD's to parallel processors, memories, etc. A surface channel CCD would allow DELTIC operation at clock frequencies up to approximately 10 MHz. With N = 100 signals with bandwidths-up to approximately 5 KHz could be handled. Data rates of 100 Hz or more could be accommodated. A state of the art system with this capability would have applications in several area such as:

A. Instrumentation

Low speed systems transmitting binary data with up-chirp and down-chirp linear FM. Two reference memories would be required for detecting both ones and zeros.

B. M-ary Communications Link

An M-ary system would have a greater information rate and would require M reference memories, one for each symbol to be detected. For orthogonal signals with equal bandwidth and time duration, only one input filter and signal DELTIC would be required. Such a system would be applicable in a secure communications link.

C. Data Scanner

This application would probably require operation of the system as a true PCC which is a simple modification. The correlator would be used

to search for coarse features in large blocks of data, such as from a video scene, and to control buffer memories from which data of interest would be transferred to other processors for more detailed processing. Such a system may also be of use for scanning physiological signals with frequency modulated characteristics.

D. Ranging Systems

The DELTIC DFPCC would be particularly applicable to the detection of return signals for either sonic or ultra-sonic systems. In most applications banks of output filters would be required for recovering doppler information.

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APPENDIX A

ANALOG IMPLEMENTATION

This appendix contains the circuit diagrams for the analog circuitry:

A1. Power supplies.

A2. Input filters IF1 and IF2.

A3. Input filter IF3.

A4. Input summer and clipper.

A5. Digital to analog output buffer.

A6. Output filter OF1

A7. Output filter OF2

A8. Detector and lowpass filter.

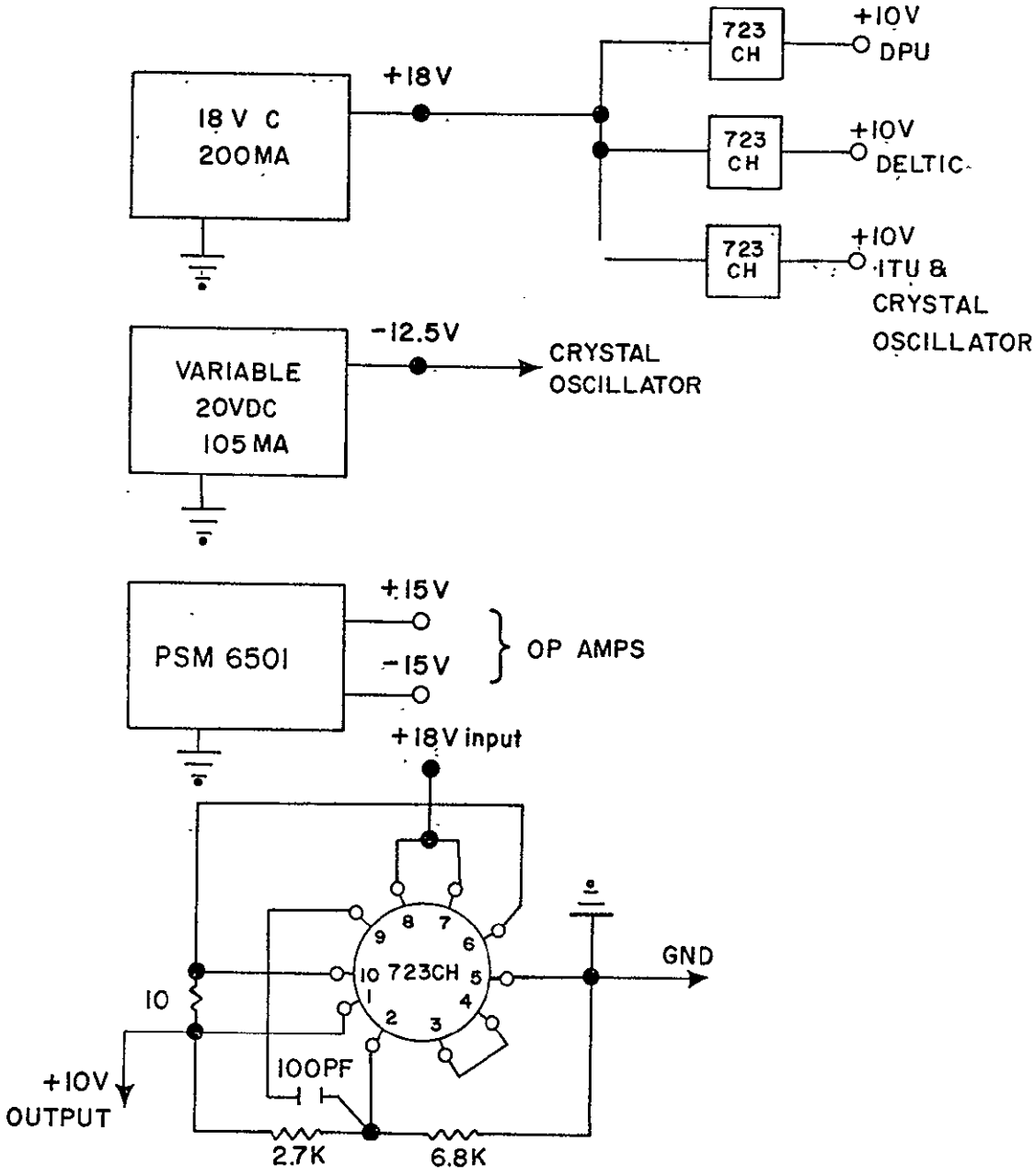


Figure A1. Power Supplies for Breadboard. Regulators are Mounted on Board with unit to be supplied.

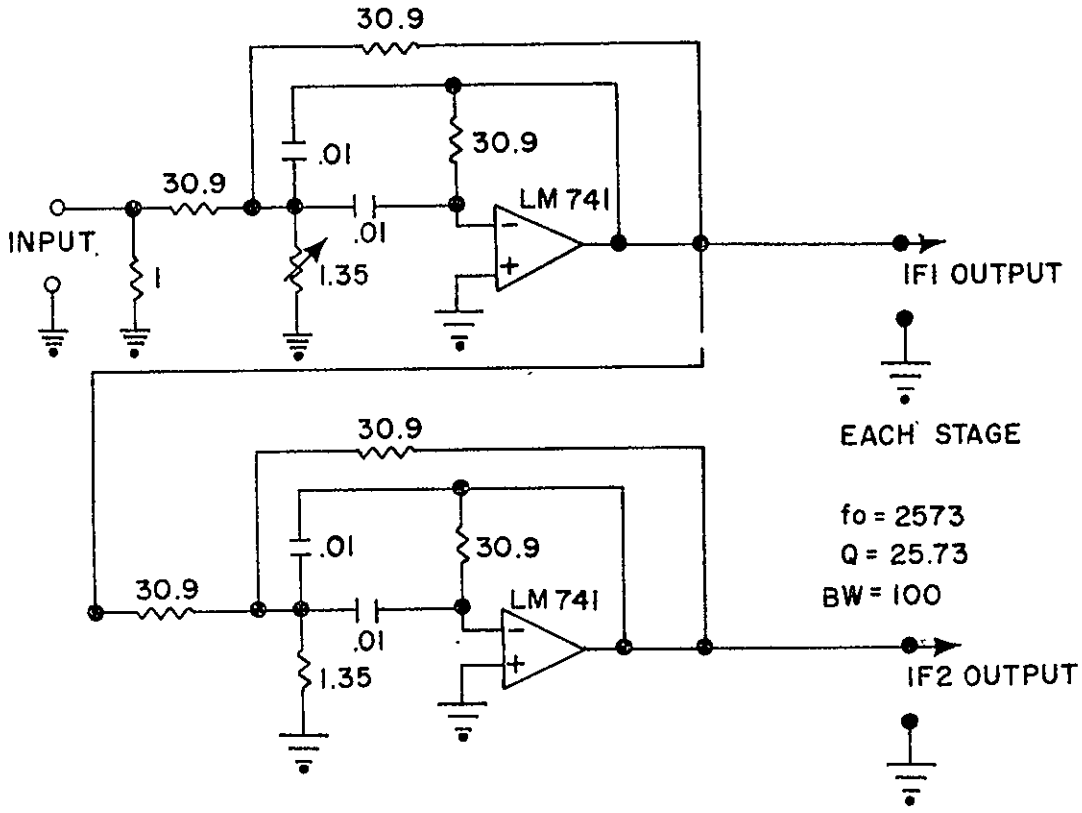
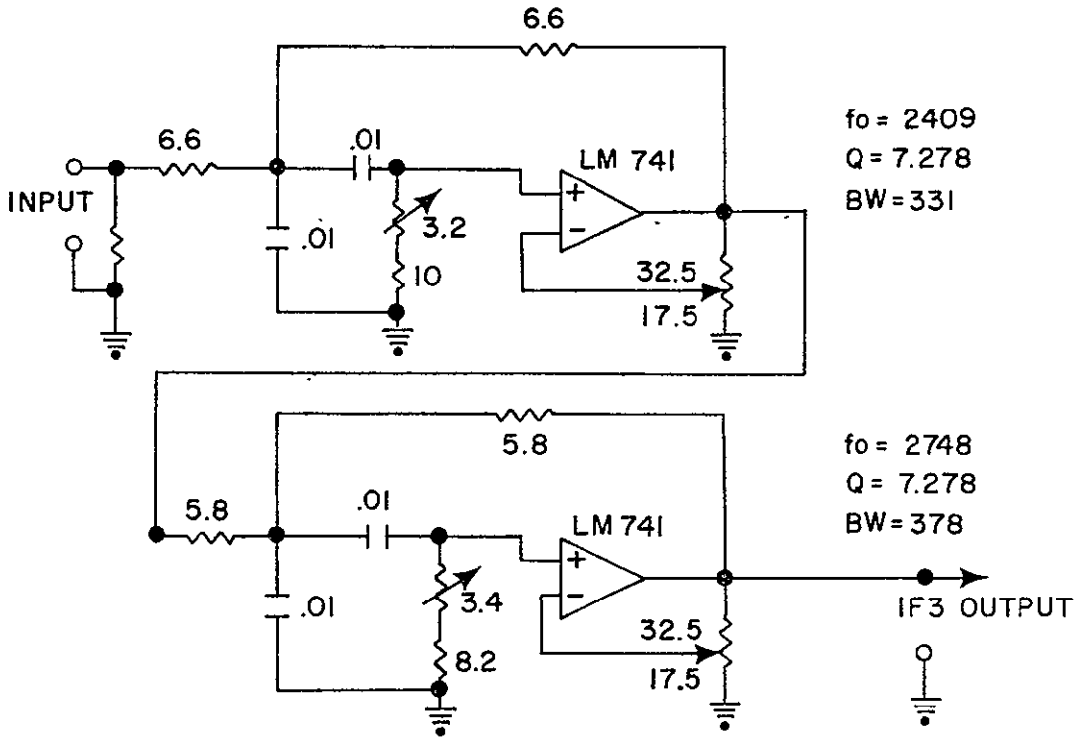


Figure A2 Circuit Diagram for Input Filters IF1 and IF2.



Resistance in Kilohms.
Capacitance in microfarads.
Opamps are 741 type.
1K required for stability when input is open-circuited.

Figure A3 Circuit Diagram for Input Filter IF3.
Butterworth response, f_o = 2573 Hz, BW = 500 Hz.

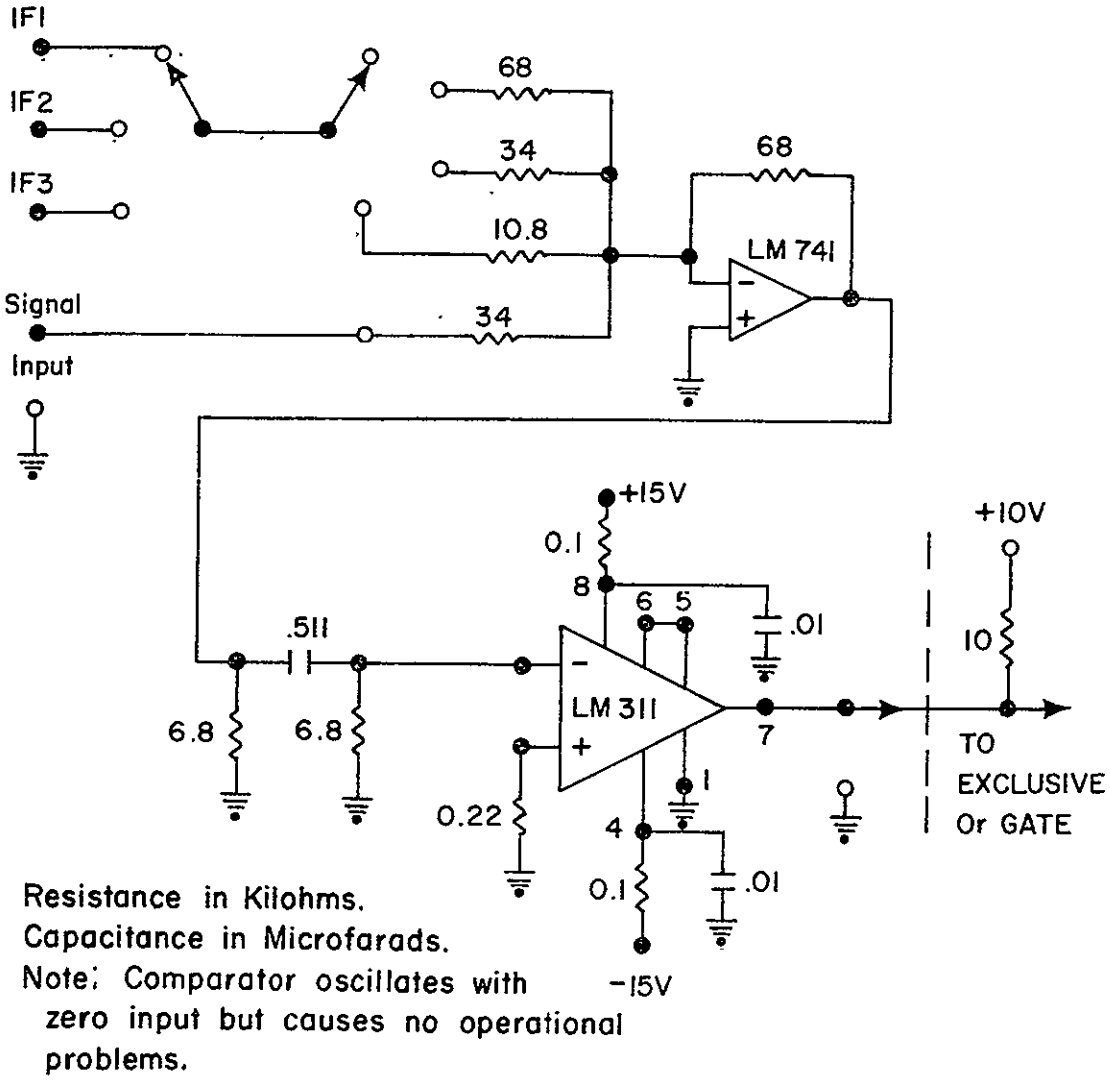


Figure A4 Circuit Diagram for Input Summer and Clipper.

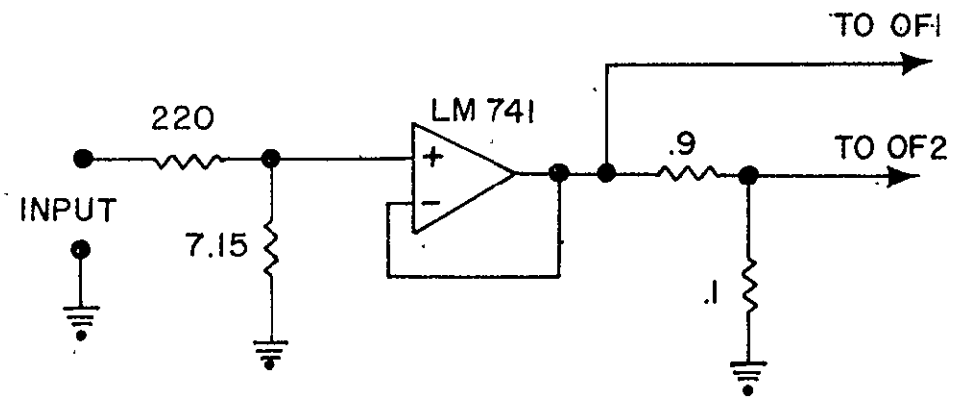


Figure A5 Buffer between CMOS Exclusive- OR Gate and Output Bandpass Filters.

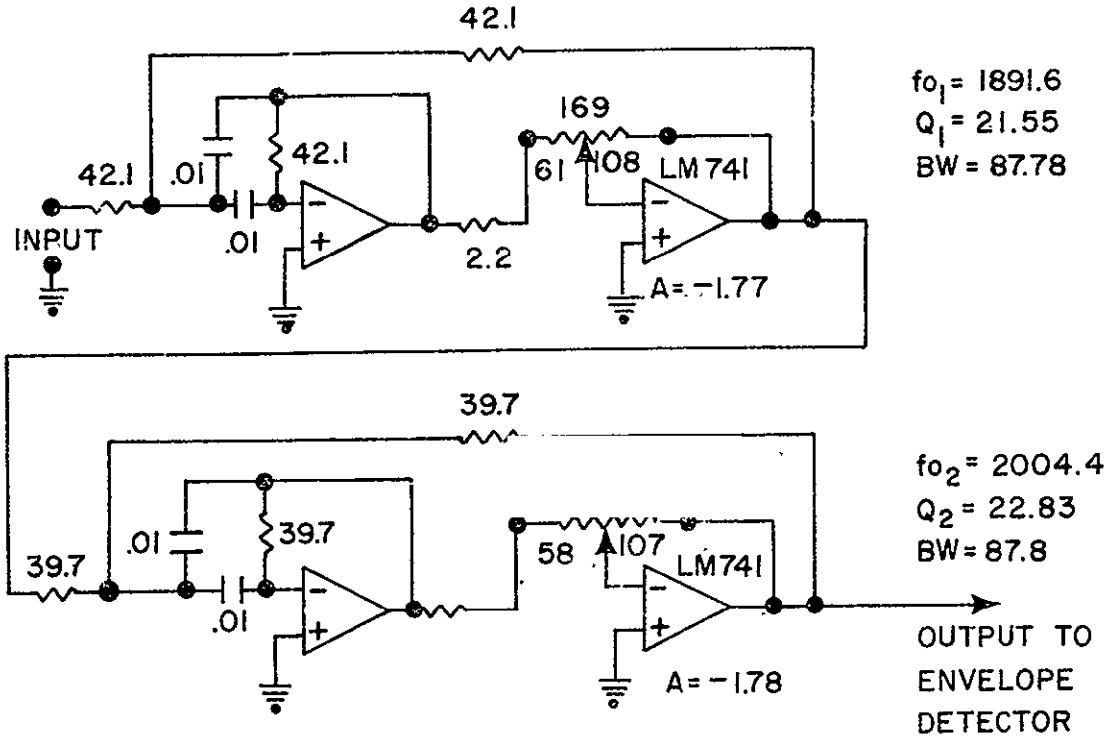


Figure A6 Circuit Diagram for Output Bandpass Filter OF1. Two-pole, 0.3 dB ripple Chebyshev, f_o = 1948 Hz, BW = 100 Hz.

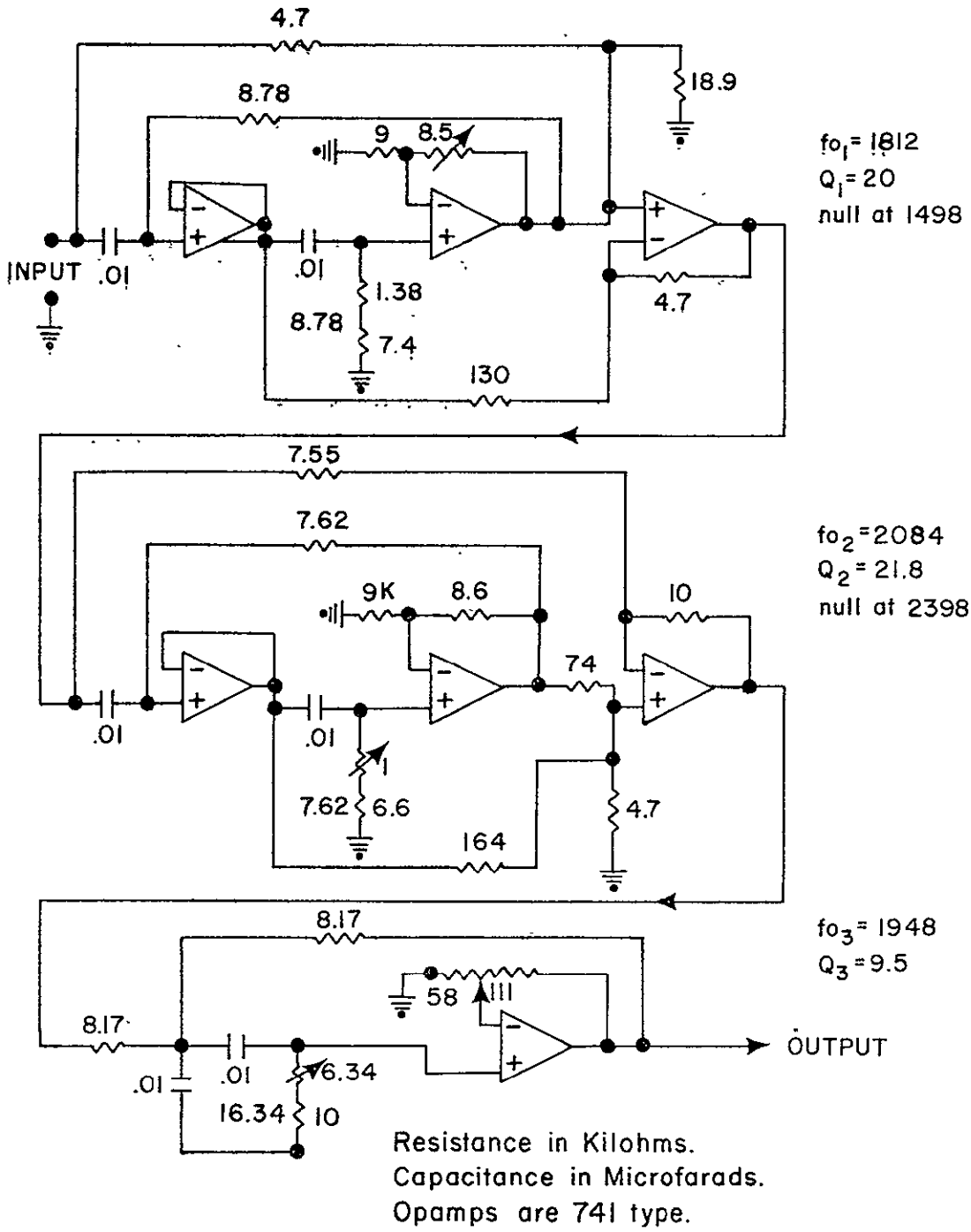


Figure A7 Circuit Diagram for Output Bandpass Filter OF2.
See Table 3.5 for Characteristics.

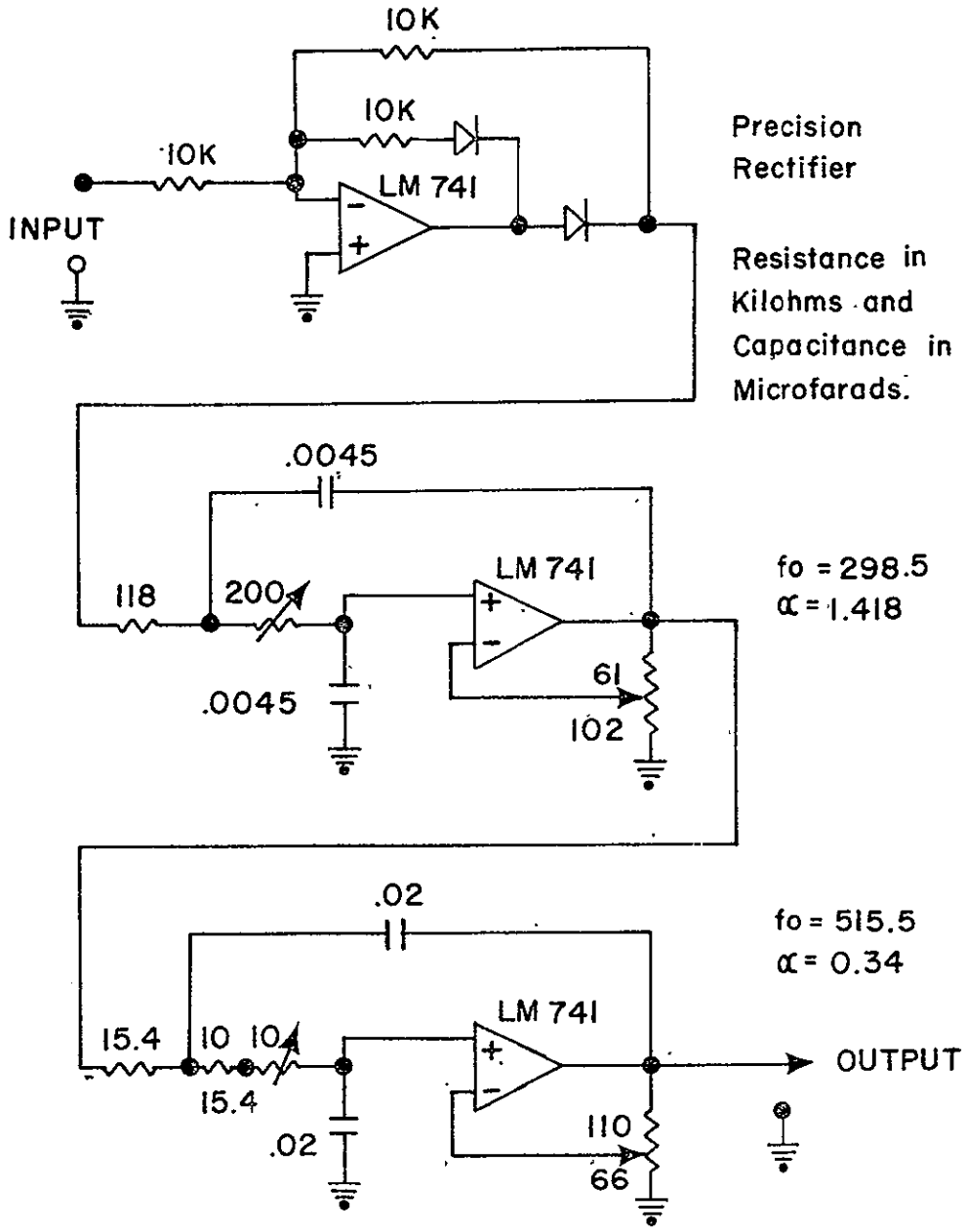


Figure A8 Circuit Diagram for Average Detector Using Precision Rectifier and Low Pass Filter.

4-pole chebyshev, 0.5 db ripple with BW = 500 Hz.

APPENDIX B

DIGITAL IMPLEMENTATION

This appendix contains the detailed logic diagrams for all of the digital circuitry used in the DELTIC DFPCC. Logic components are RCA COS/MOS 4000 series IC's and part numbers are given. Timing waveforms for the timing units are also given.

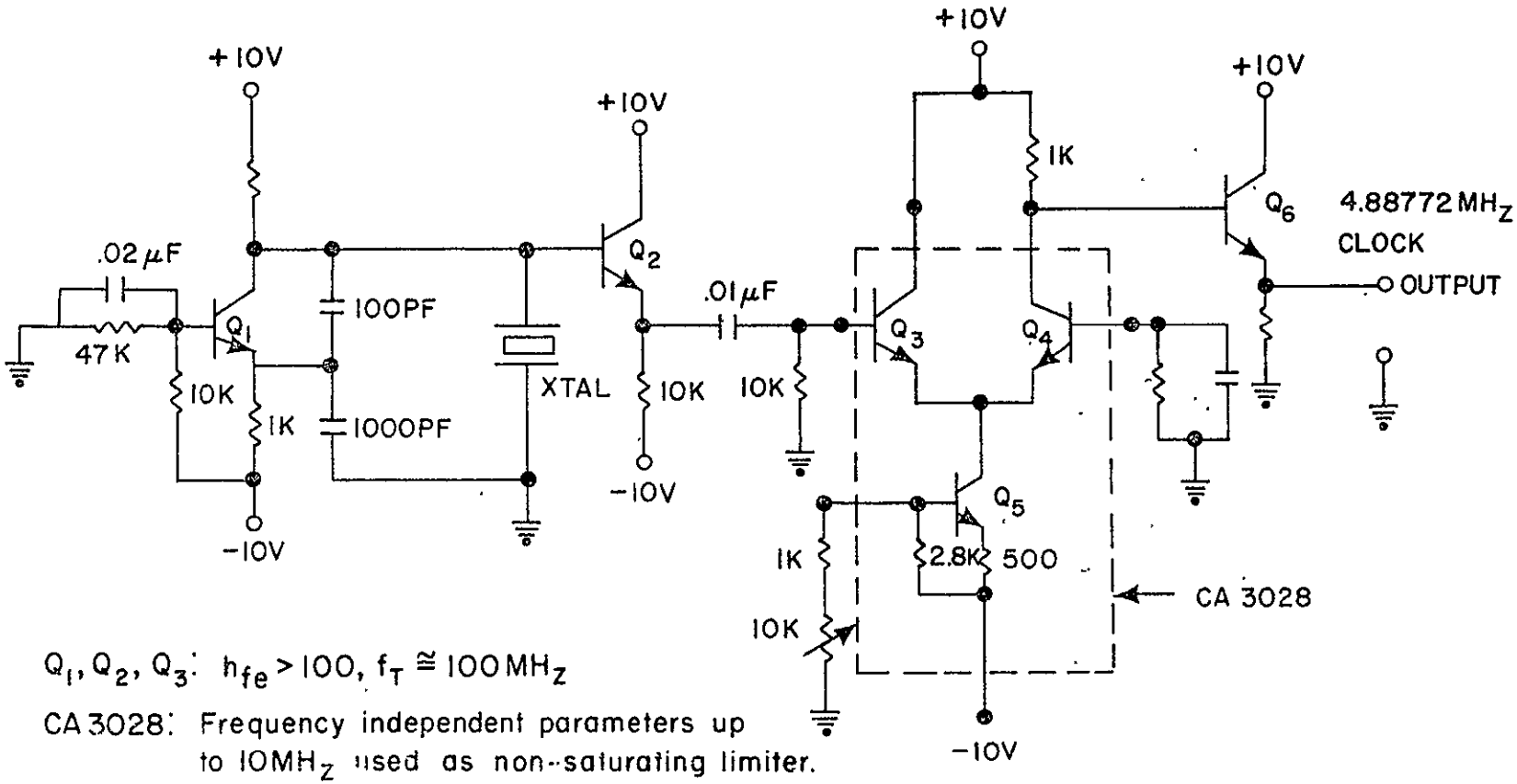
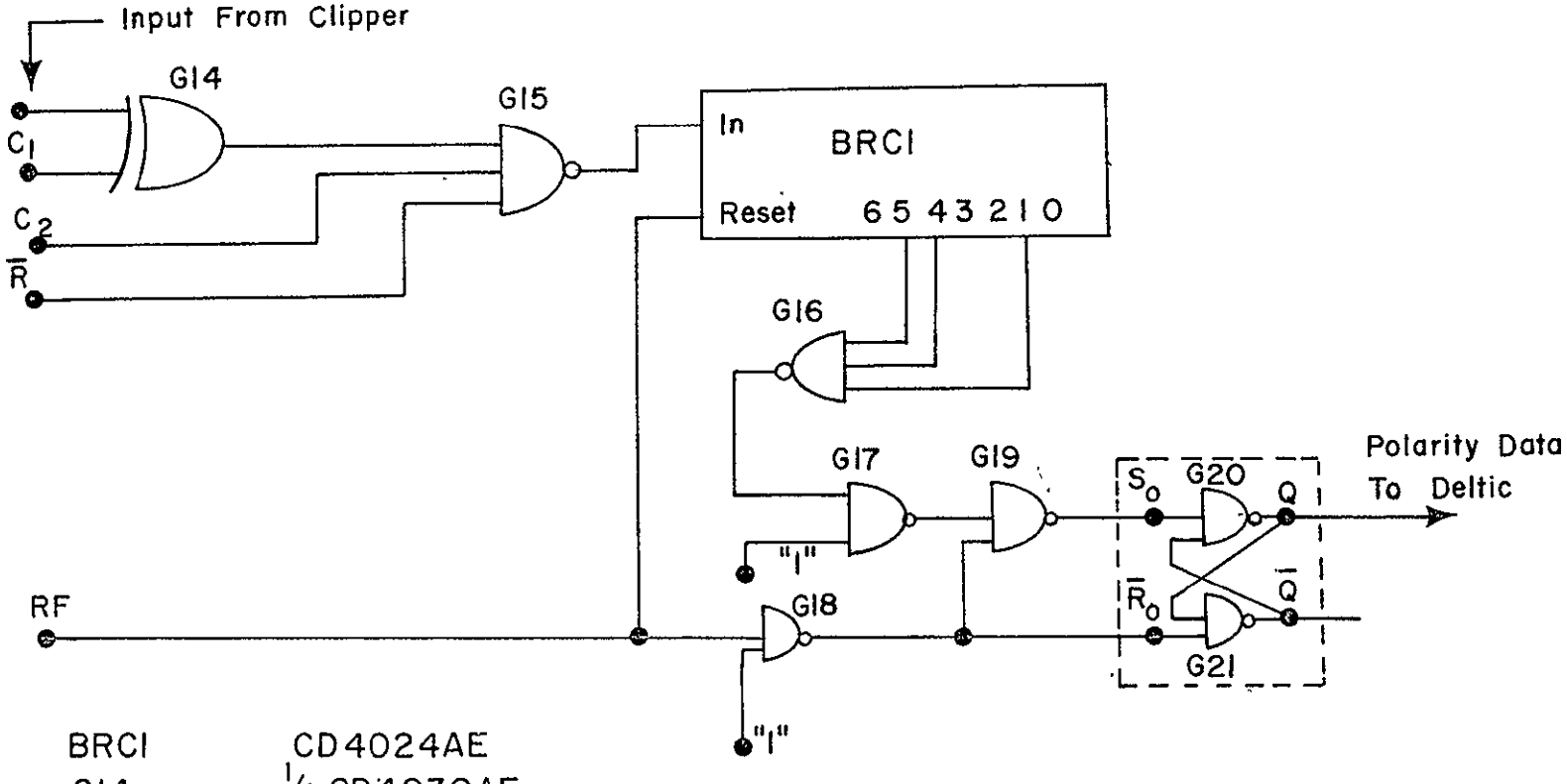


Figure B1 System Master Digital Clock



BRCI	CD4024AE
G14	1/4 CD4030AE
G15, G16	1/3 CD4023AE
G17-G21	1/4 CD4011AE

Figure B2 Logic Diagram for DPU

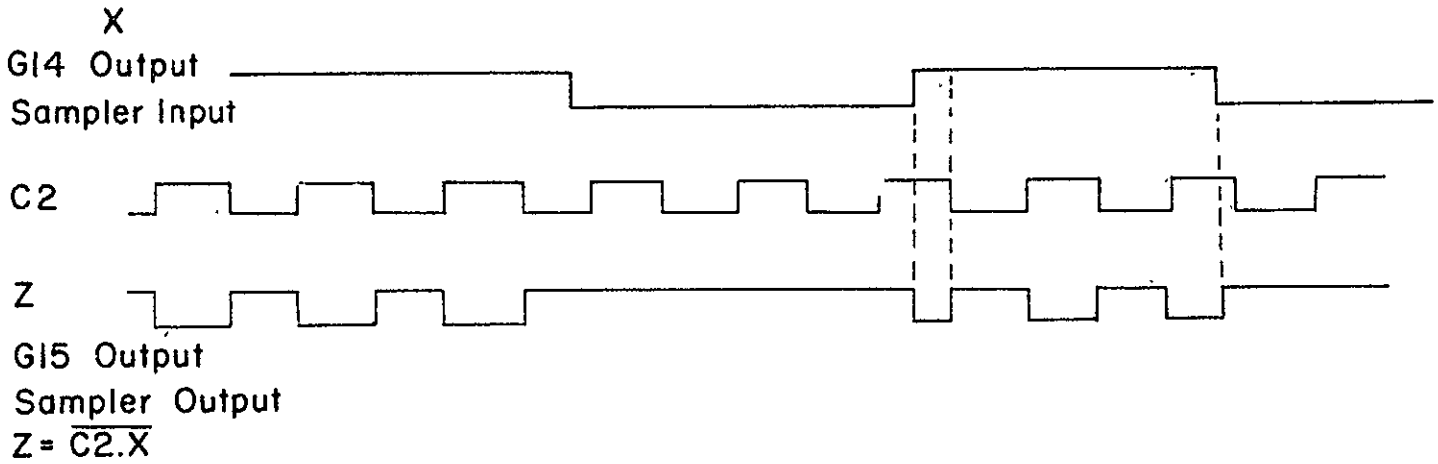


Figure B3 Operation of Asynchronous Sampler in DPU.

Note: A "1" is a negative going transition on Z. If x is "1" during first half of sampling period, then a "1" output is obtained.

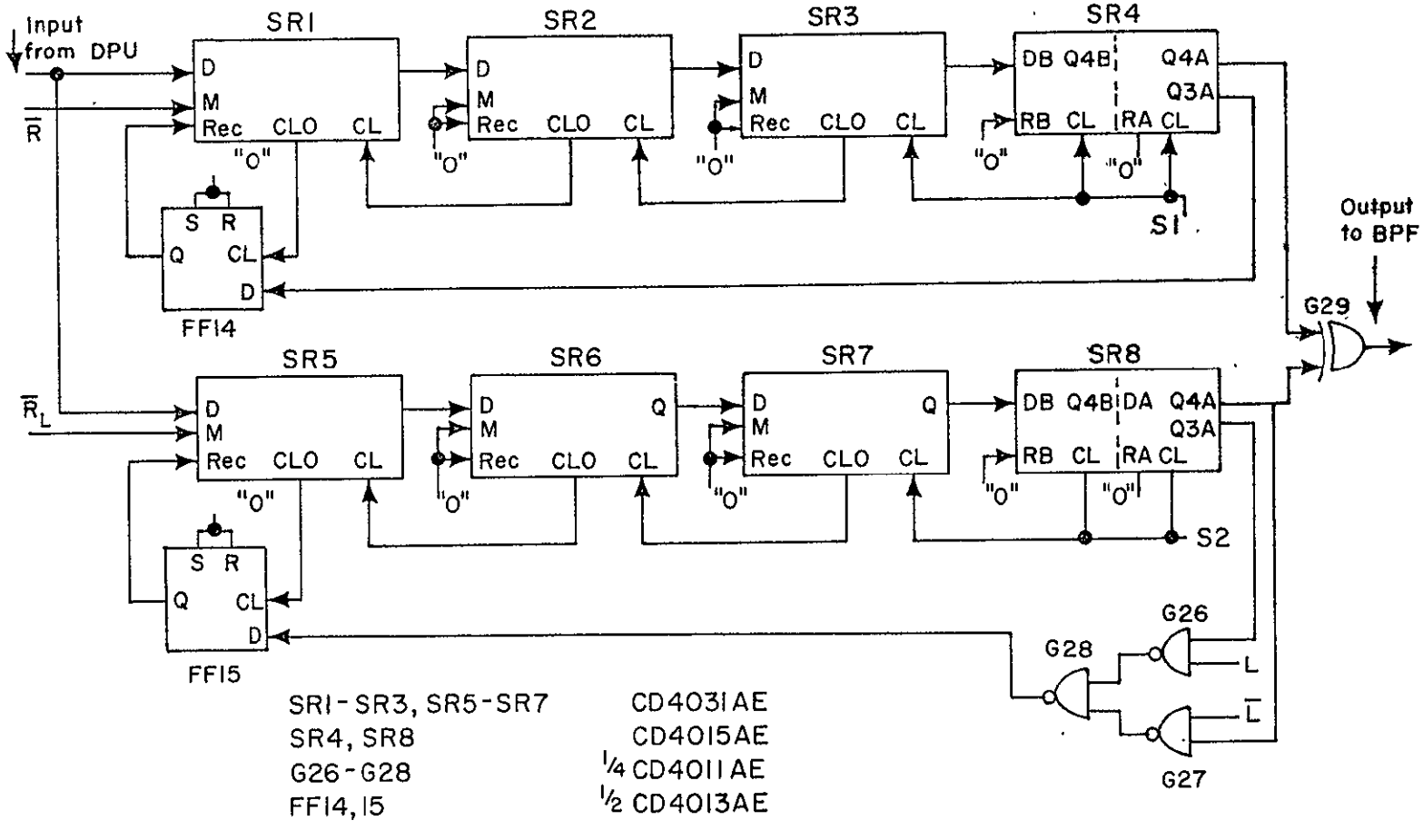


Figure B4 Logic Diagram for DELTIC Unit.

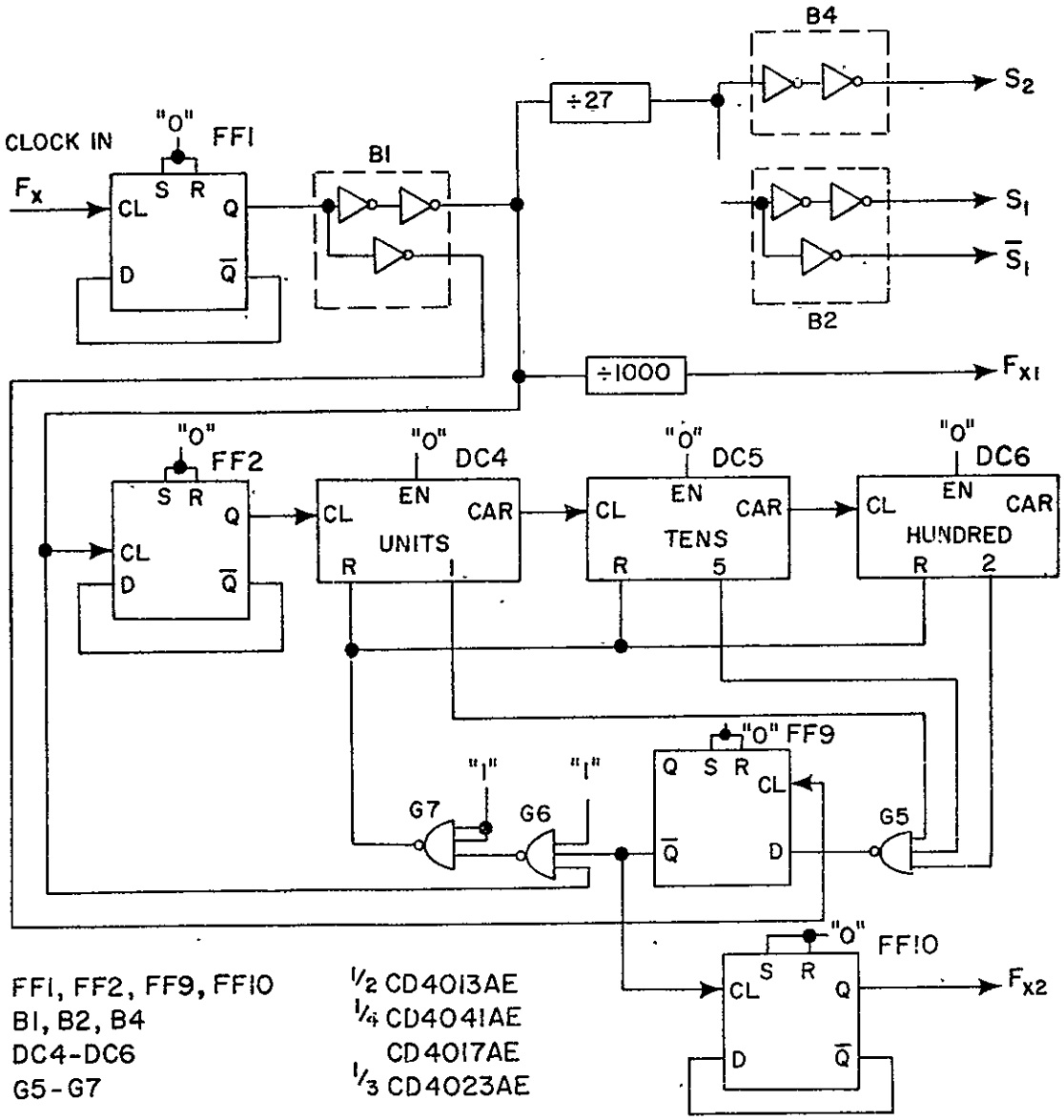
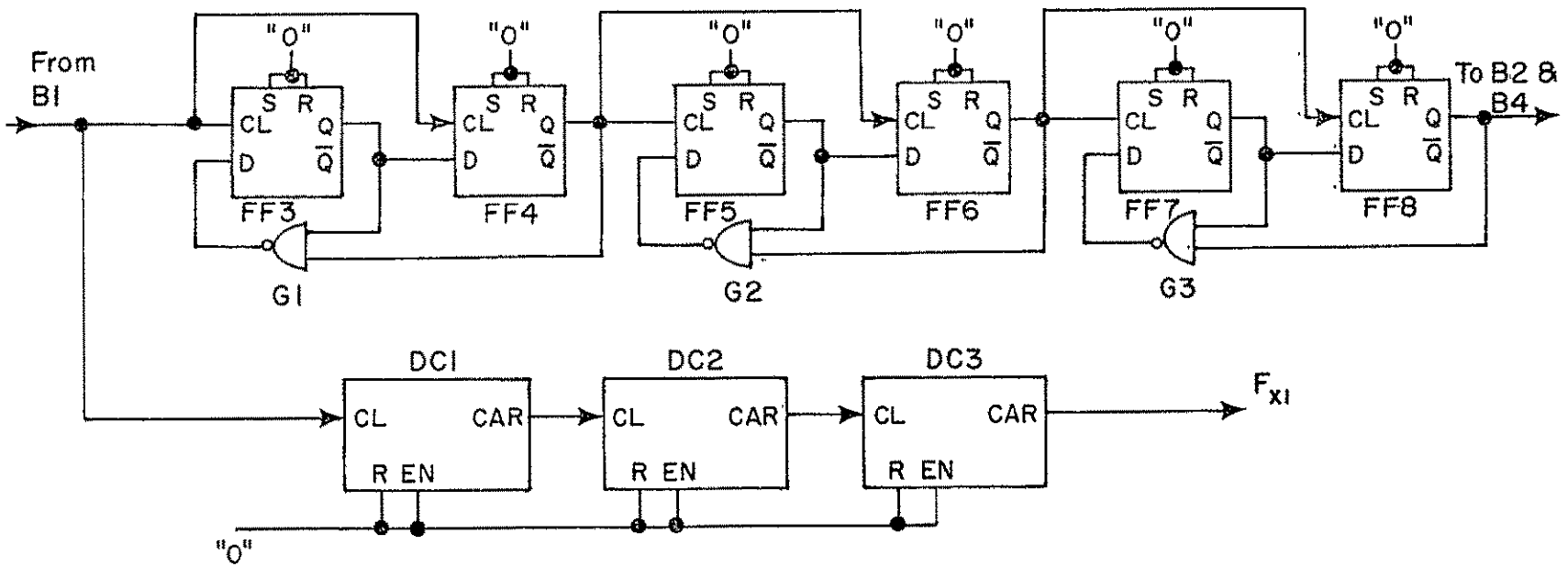


Figure B5 Logic Diagram for FTU.



FF3 - FF8	1/2 CD4013AE
G1 - G3	1/4 CD4011AE
DC1 - DC3	CD4017AE

Figure B6 Logic Diagram for Divide by 27 and 1000 Counter Circuits

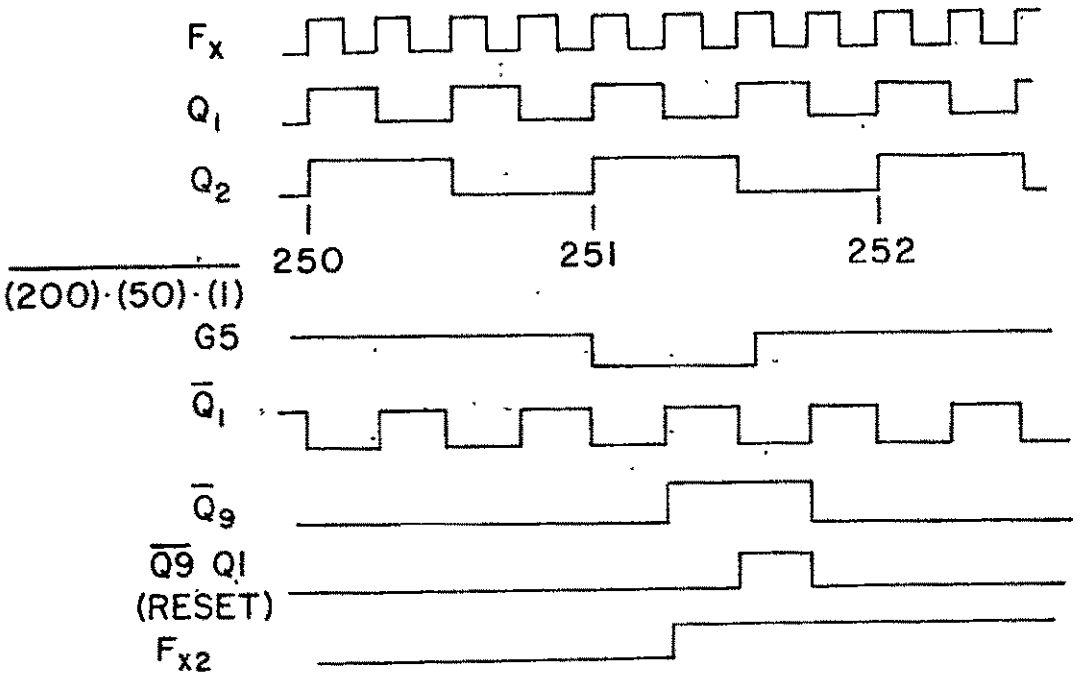


Figure B7 Timing Waveforms for LO with Frequency F_{x2} Implemented with 2008 Frequency Divider.

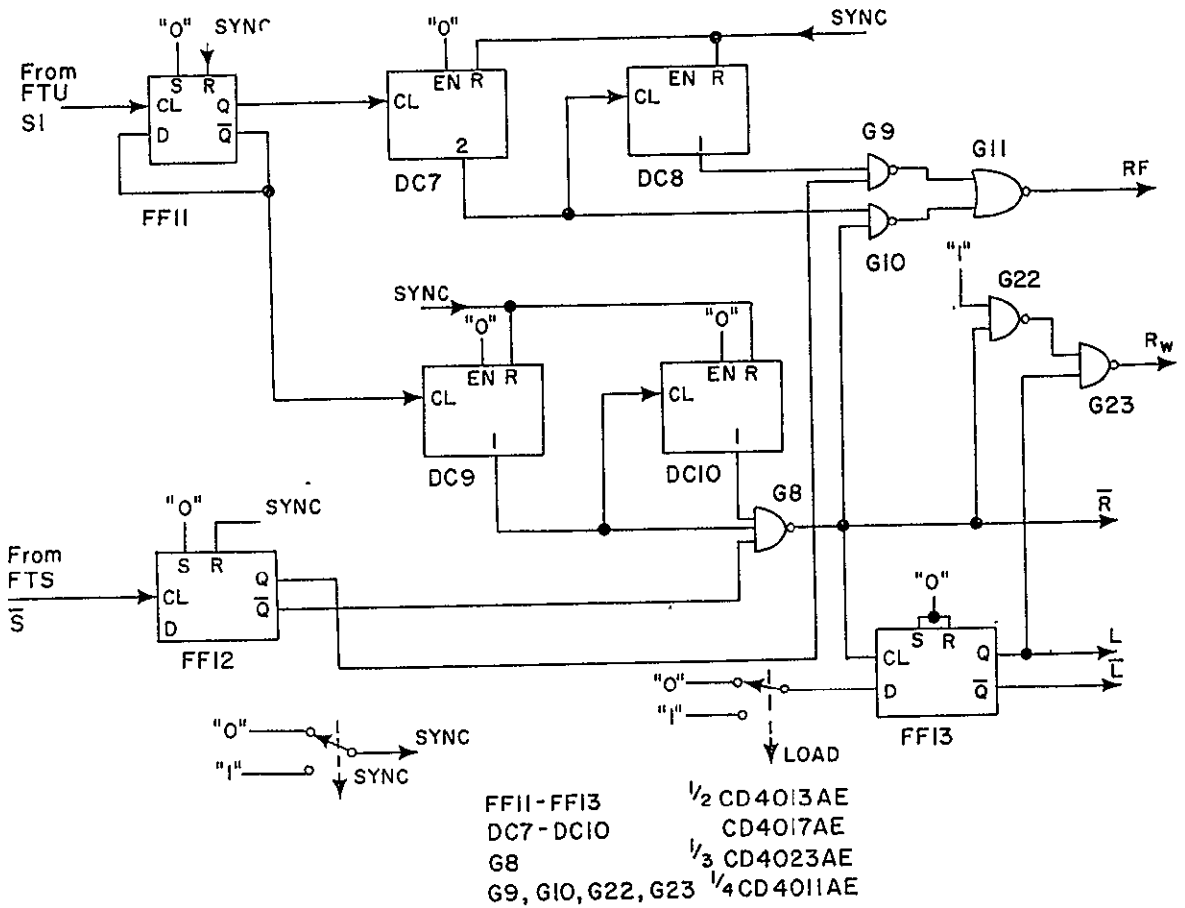


Figure B8 Logic Diagram for ITU.

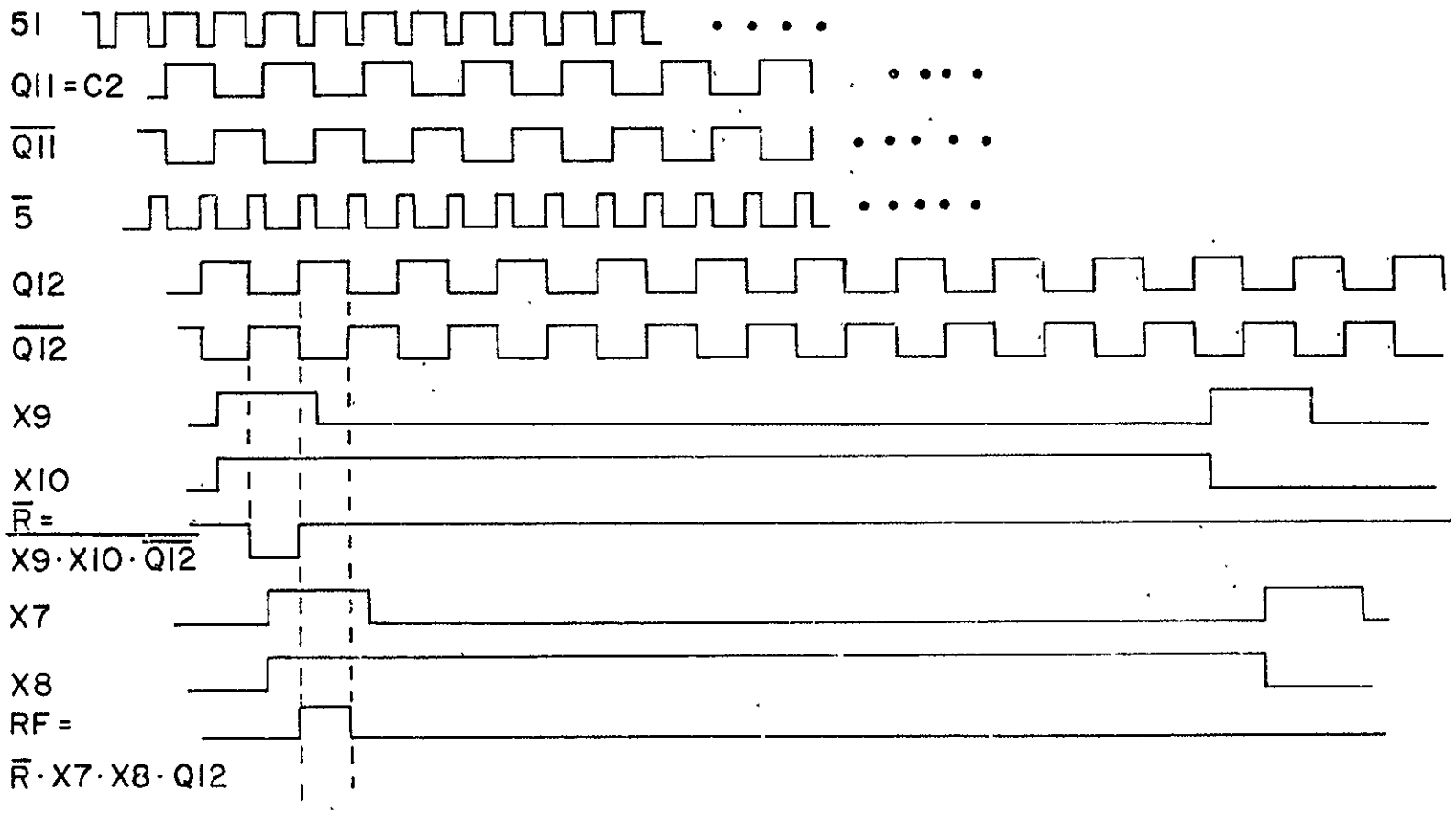


Figure B9 Timing Waveforms for ITU.

APPENDIX C

STEPWISE LINEAR FM SWEEP GENERATOR

This appendix contains logic and circuit diagrams for the test generator which was designed and constructed for this project. The generator consists of a programmable frequency divider, which receives a 1.22193 MHz signal from the fundamental timing unit, and an output bandpass filter.

Digital Parts

PDC1-PDC4	CD3018A
BRC1	CD4024A
FF1-FF4	1/2 CD4013A
G1-G2	1/4 CD4011A
G3-G5	1/3 CD4023A
G6-G8	1/4 CD4001A
G9-G10	1/4 CD4011A

Analog Op-Amps - LM741 equivalent.

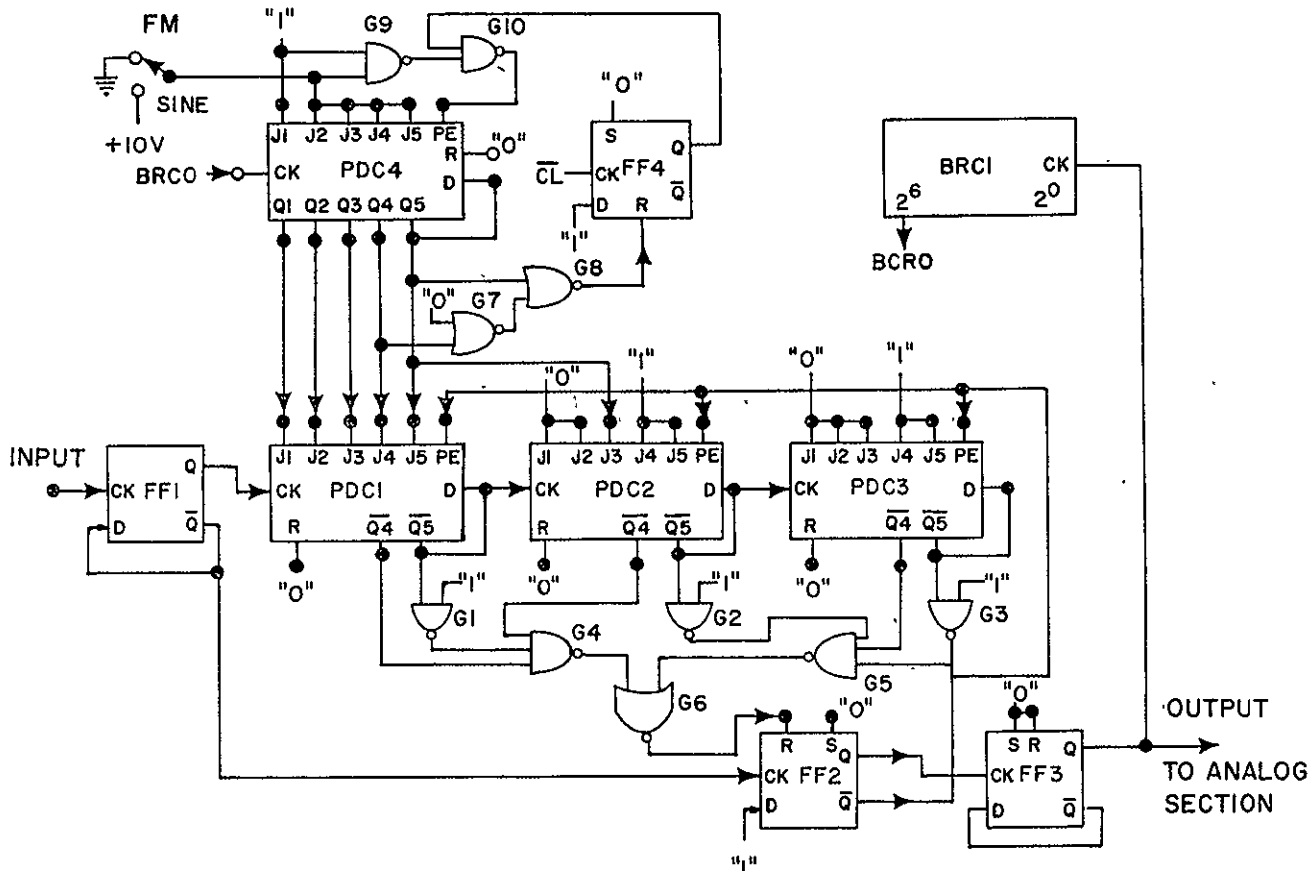


Figure C1 Signal Generator-Digital Section.

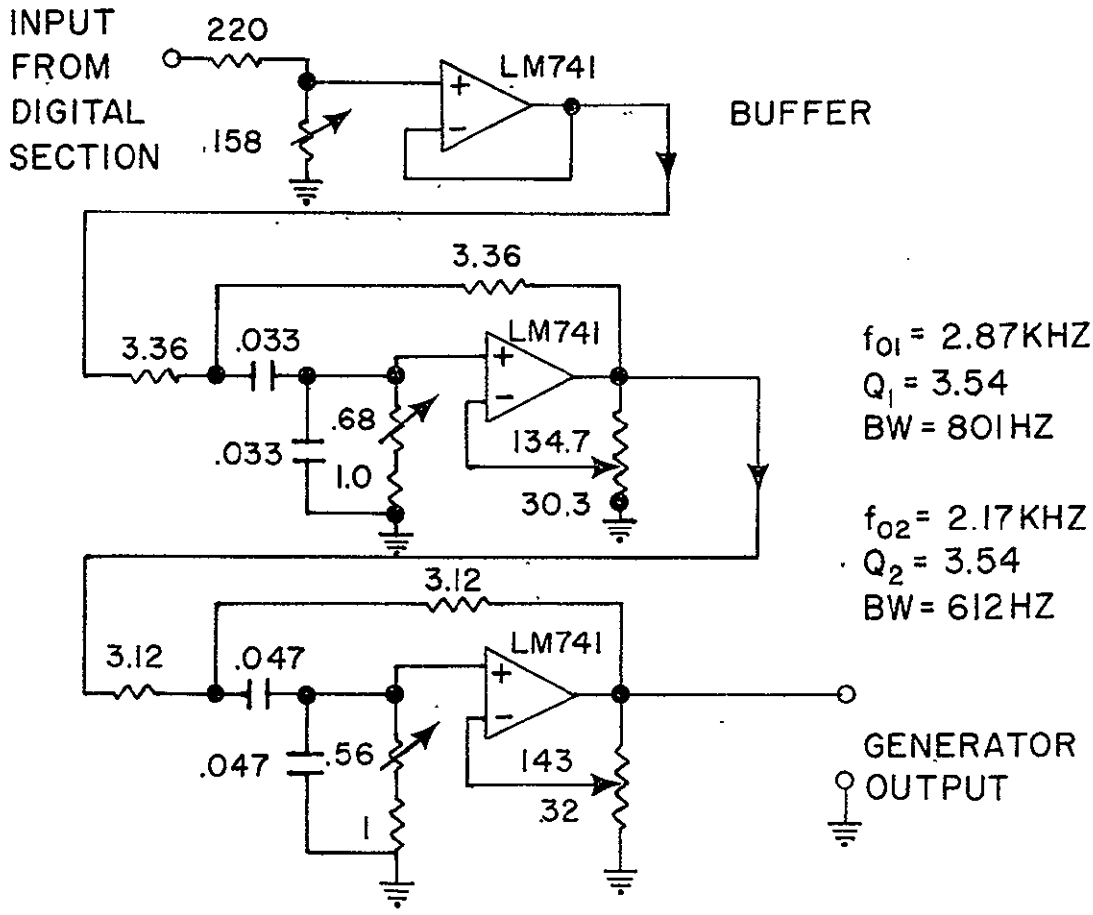


Figure C2 Signal Generator-Analog Section. Buffer is followed by Butterworth Band Pass Filter with BW = 1kHz.

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