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LOW COST SILICON SOLAR CELL ARRAY

by F. T. C. Bartels

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16. Abstract

Final Technical Project Report under Contract NAS3-17361 examining the technological options available for producing low cost silicon solar cell arrays. Based on mass production capacity demand a project value of approximately $\$250/meter^2$ and \$2/watt is projected. Recommendations are included for the most promising cost reduction options.

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I. SUMMARY

The cost of solar cell arrays without concentration can be reduced to approximately $\$250/m^2$ (or \$2/peak watt) through the utilization of known technologies and mass production equipment. A detailed cost analysis showed that this objective could be reached utilizing process technology that is known today and conventional crystal growing and slicing methods. No major technological breakthrough would be required, and the effort would essentially involve production engineering activities rather than a basic research and development effort. There would need to be a growth in production rate to about 2.5 MW per year to justify the mass production equipment.

Additional cost reductions can be projected based on new technologies that are anticipated. Array costs of $\$70/m^2$ (or \$0.50/peak watt) have been projected. There are at least four options that have been identified that appear capable of providing this cost reduction, namely:

1. Ribbon growth of silicon crystal
2. Inexpensive silicon poly raw materials
3. New slicing technology
4. Optical concentration

Again, these objectives require a major expansion in production rate to a level of about 1000 MW per year.

Considering the four options listed, it appears that at least one can be developed within the next five years since both ribbon growth and low cost poly silicon processes are being studied extensively and appear promising.

II. INTRODUCTION

This final report summarizes the work performed under Contract NAS3-17361 directed toward the study of options for lowering the cost of producing solar cells and arrays.

Present methods of producing solar cells and arrays are very expensive because the production rates are small and the processes have not been mechanized. If the costs could be substantially reduced, it would provide the opportunity for considering new missions that utilize large scale solar power systems both for space and terrestrial applications. There are quite a few potential space missions that require large solar cell arrays, that could benefit substantially from lower solar cell array costs. If we consider terrestrial applications, the potential for utilizing solar cell power systems becomes tremendous if the array costs can be reduced enough. Therefore it becomes apparent that the demand for large quantities of solar cell arrays can be anticipated both in space and on the earth's surface, thus we need to assess the potential for developing low cost methods for producing these arrays.

This study is the first step in the process to define the necessary technology, production approaches and methods for substantially reducing solar cell costs. The study reviews and evaluates technology options for lowering cell costs and identifies promising approaches that can be used now in mechanizing and automating production facilities. A detailed cost analysis was made based on this technology and a forecast of the expected cost reductions provides data that can be used as a guide for future systems analysis.

The general approach used in the study was to first make a systematic evaluation of the various technological options available compared to the present manufacturing processes used in producing spacecraft silicon solar cells and arrays. A simplified process flow chart containing all

the basic steps required to make cells and arrays was used as a step-by-step checklist for considering what factors make up the costs and what technological changes could be made. Section III contains detailed discussions of the various technological options that are available. This discussion considers first the options for fabricating the blank and includes an evaluation of the methods of producing and purifying silicon and the methods of growing monocrystals and slicing the blanks. Then the options for fabricating solar cells from the blanks were evaluated and compared to the present fabrication technology. Next, methods of array fabrication were discussed and design criteria evaluated. Also, optical concentration was evaluated and the impact on costs determined.

Section IV contains a detailed cost analysis for producing solar cells and arrays assuming large scale production and an advanced process based on conventional silicon crystal growth and slicing techniques. This provides a realistic near term cost reduction goal that can be used as a guide for future systems analysis.

III. DISCUSSION OF TECHNOLOGICAL OPTIONS

IIIA. BLANK FABRICATION

Material Requirements

The overall process of array fabrication is divided into 3 areas and 14 steps as shown in Figure 1. Area "A", Blank Fabrication, includes six steps in the present process:

1) Reduction of silica to metallurgical silicon
2) Conversion of metallurgical silicon to intermediate compound (e.g., trichlorosilane)
3) Purification of intermediate compound
4) Decomposition of intermediate compound to polycrystalline silicon
5) Growth of silicon monocrystal
6) Slicing into blanks and removal of slicing damage by etching

These steps are grouped into a single technical area because they accomplish the function of preparing the basic raw material for solar cell fabrication (silicon) in a form meeting specified requirements of chemical purity, crystalline perfection, and dimensions. Also, these steps are common to all silicon semiconductor devices.

The important impurities in silicon which must be specified are the group III and group V elements (B, Al, P, As) which produce shallow doping levels, the heavy metals (Fe, Cu, Au) which produce deep levels which act as recombination centers, and the non-metals C and O which produce precipitates.

The tolerable level of group III and V elements depends on the final doping level of the silicon. If the intention is to produce 10 ohm-cm P-type silicon in step 5, boron will be added to the melt in this step to produce

FIGURE 1.

Simplified Process Flow Chart

A. Blank Fabrication

1) Reduction of silica with carbon
2) Conversion of metallurgical silicon to intermediate compound
3) Purification of intermediate compound
4) Decomposition of intermediate compound to polycrystalline silicon
5) Growth of silicon monocrystal
6) Cutting into blanks and removal of cutting damage

----------Finished blank----------

B. Cell Fabrication

7) Junction formation (including removal of back-surface junction if necessary)
8) Contact deposition
9) Anti-reflective coating deposition
10) Cell test and sort

----------Finished cell----------

C. Array Fabrication

11) Cell interconnection into modules
12) Module encapsulation and integration with support structure
13) Module interconnection and integration with concentrator (if used)
14) Installation at site

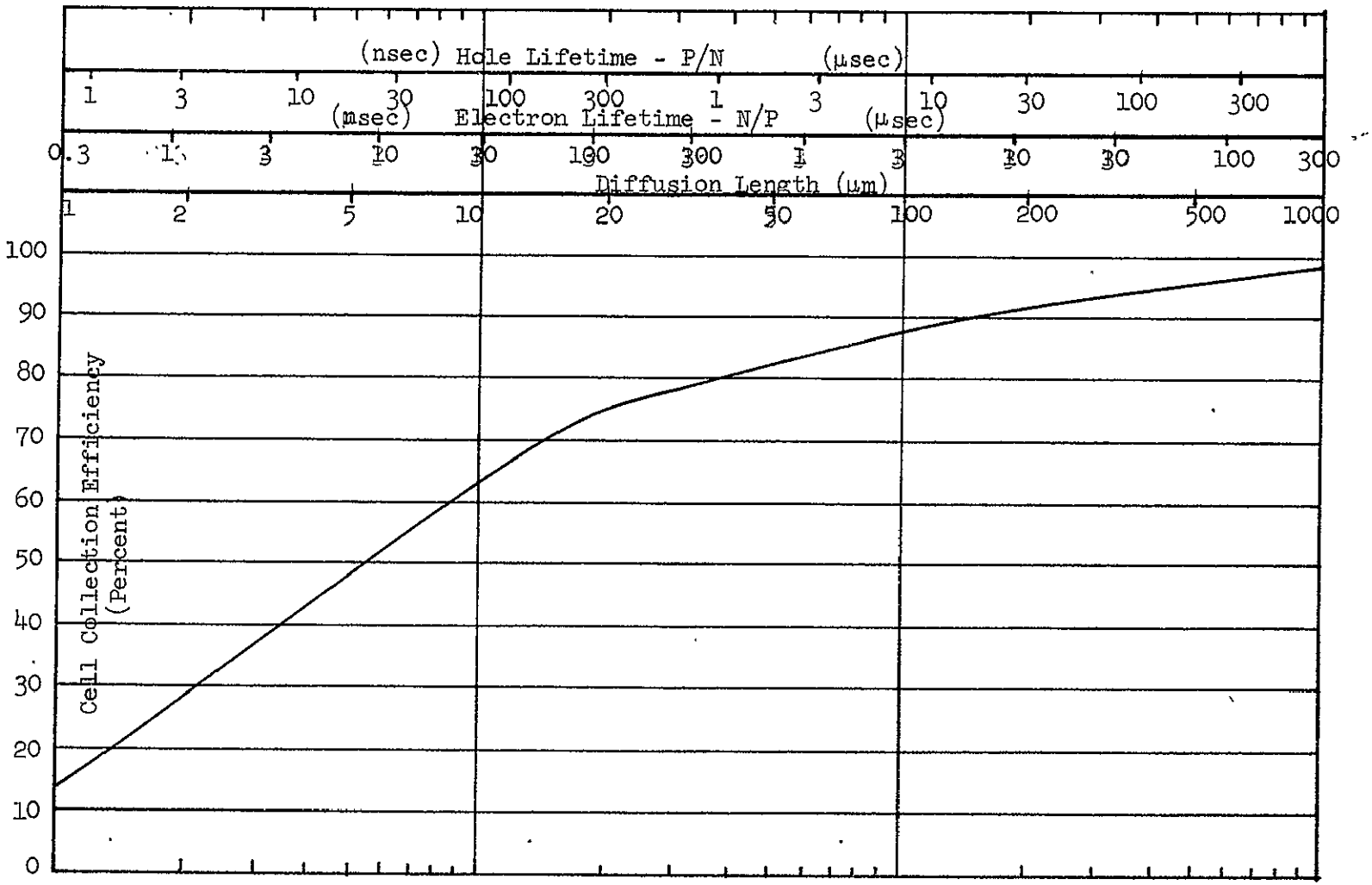
----------Finished array----------

a net acceptor concentration of 1.3×10^{15} cm^{-3}, or 26 ppb (parts per billion). The net concentration of group III-V elements in the poly used will not usually be known prior to crystal growth; it cannot be accurately measured by measuring the resistivity of the poly because free carriers in the poly are trapped by deep levels produced by imperfections. The purification process (step 3) must therefore be thorough enough so that the net concentration in the poly can be assumed to be negligible. In practice, a "negligible" level would be about 2.5 ppb for both donors and acceptors.

Since solar cells for terrestrial applications can be made from more heavily-doped material (as high as 2.5×10^{18} cm^{-3}, or .03 ohm-cm), poly with residual concentrations of group III-V elements as high as 5000 ppb might be usable in this application. However, for general semiconductor device applications such material would be completely unacceptable. The residual level of 2.5 ppb which is acceptable for 10 ohm-cm solar cells is also acceptable for almost all other device uses.

The concentration of deep-level impurities such as Fe, Cu and Au must be kept low in order to obtain adequate current output from the cell. These impurities act as recombination centers, reducing minority carrier lifetime. The relationship between minority carrier lifetime, diffusion length and cell collection efficiency is shown in Figure 2. In order to obtain the high levels of collection efficiency (>90%) presently obtained in space cells, a diffusion length of 200 μm is required, corresponding to a minority carrier lifetime of 10 microseconds for an N/P cell or 30 microseconds for a P/N cell. There is apronounced knee in the efficiency curve at about 20 μm and 75% collection efficiency, corresponding to an electron lifetime of 0.1 microsecond and a hole lifetime of 0.3 microsecond. The rapid decrease in collection efficiency below this point suggests that this is a good estimate of the lower limit for diffusion length in a practical cell. Corresponding values of AMO conversion efficiency would be 10% to 12% for material with a minority carrier diffusion length of 200 μm, decreasing to 6% to 8% at 20 μm. Conversion efficiency in terrestrial sunlight would be somewhat greater.

FIGURE 2: Silicon Solar Cell Collection Efficiency vs. Base Diffusion Length and Minority Carrier Lifetime.



The impurities Fe, Cu and Au produce recombination centers in silicon with a capture cross section of about 5×10^{-15} cm^2. In order for the minority carrier diffusion length to exceed 200 μm, the total electrically active concentration of these elements must be reduced below 1.5×10^{12} cm^{-3} (.03 ppb) for N/P cells or 5×10^{11} cm^{-3} (.01 ppb) for P/N cells. If a minority carrier diffusion length of 20 μm is considered adequate, the allowable concentration of these elements can be 100 times greater.

Discrete crystalline imperfections, such as those produced by electron irradiation, have properties similar to the recombination centers produced by deep-level impurities. Such discrete centers can be eliminated by thermal annealing; the annealed silicon will contain clustered defects (including dislocations and grain boundaries) separated by regions of nearly perfect material. The annealing process results in a very large decrease in defect density; on the other hand, the capture cross section of a defect cluster is much larger than that of a discrete defect. This is the result of the fact that the Fermi level within the cluster is pinned (by the large density of traps within the cluster) near the center of the band-gap, so that the cluster is surrounded by a space-charge region which is a sink for minority carriers. [1,2] This model has been shown to be successful in explaining recombination kinetics in neutron-irradiated silicon [2] and in heteroepitaxial films [3], and has been applied to the study of lithium precipitation in neutron-irradiated silicon [4], and mobility and lifetime [5,6] in polycrystalline films deposited by chemical vapor deposition.

At present, silicon monocrystals for solar cell application are not required to be dislocation-free, but the presence of lineage, slip lines, twins or grain boundaries are cause for rejection. A systematic study of the effects of crystalline imperfections on solar cell performance has not been made, so that a lower limit for material perfection cannot be precisely defined. However, silicon chemically vapor deposited at 1035°C on thermally-grown silica films exhibited a minority-carrier lifetime about 3 orders of magnitude lower than material epitaxially deposited on silicon at the same time [6], and a mobility about 1 order of magnitude lower, indicating a diffusion length of the order of 0.1 μm. Silicon films deposited on

oriented single-crystal spinel were monocrystalline by x-ray diffraction but had a high density of defects in electron micrographic examination; these films also exhibited sub-nanosecond minority-carrier lifetime [3]. On the other hand, Berman and Ralph [7] fabricated solar cells from polycrystalline rods which exhibited efficiencies as high as 11% (AM 1). Their material was Czochralski-grown under conditions (high pull rate) which produced polycrystalline growth with grain size 2mm and larger. Their spectral response curve indicates that the diffusion length in their material was about 20 μm; single-crystal cells fabricated at that time had diffusion lengths of 50-100 μm. The short-circuit current of their poly cells was about 90% of the value for single-crystal cells, and the open-circuit voltage was about 100 mV lower.

If a grain boundary is pictured as a sink for minority carriers, it is reasonable to expect that the short-circuit current will not be seriously affected if the average grain size is much larger than the diffusion length in the interior of the grain. Also, one would expect that the open-circuit voltage will be lowered by a grain boundary intersecting the junction, even if the short-circuit current is only slightly reduced, since under forward bias a large amount of current will flow at the intersection. Therefore, high-efficiency ($>10\%$) cells will probably require perfect material, while low-efficiency (6-8%) cells can be made from poly with grain size greater than ~ 1 mm, and poly material with small grain size will probably not yield acceptable cells.

Figure 2 also provides an estimate of the minimum cell thickness for a given current efficiency. If a back contact which is reflecting for both photons and minority carriers is used (e.g., an aluminum alloyed and diffused contact on an N^+/P cell), the optical thickness of the cell will be twice the physical thickness. Thus, reasonable efficiency can be expected for cells as thin as 10 μm. The maximum area of a single cell is a function of the contact and interconnect design used; since increasing the area increases the current output without changing the voltage, larger cells require proportionately lower-resistance grid lines to carry the larger current without appreciable voltage drop.

Silicon Production

The primary function of steps 1-4 of the simplified process flow in Figure 1 is chemical purification, which in the present process is accomplished in step 3, using an intermediate compound formed in step 2. The major part of this report section is concerned with the choice of the intermediate compound. Before proceeding to discuss the possible choices of intermediate compound, the possibility of dispensing with an intermediate compound will be discussed. If no intermediate compound is used, purification processing must be performed on silica or on metallurgical silicon.

Purification of silica can be accomplished by dissolving silica in a sodium hydroxide solution, followed by fractional precipitation of impurity elements and final precipitation of purified silica, which would then be reduced to silicon by some means which would not re-introduce impurities. Table 1[8] gives a typical analysis of diatomite, a highly pure natural form of silica. From the discussion in the preceeding section, it can be seen that Al and Fe must be reduced in concentration by factors of 10^7 to 10^9, to meet requirements for semiconductor grade silicon. This would seem to exceed the capabilities of chemical technology. The analogous Bayer process for the purification of alumina yields a product containing about 100 ppm Fe.[8]

Purification of metallurgical silicon was attempted during the 1940's; metallurgical silicon was leached with acids to produce material suitable for microwave diodes.[9] Little purification is necessary for this application since extremely low minority-carrier lifetime is required. Other possible approaches involve applying purification processes to molten silicon[10] or to solutions of silicon in metals such as aluminum.[9] Silicon-rich aluminum alloys can be produced by the reduction of clay with carbon in an arc furnace.[11] Table 2 shows a typical analysis of metallurgical silicon of the grade used for trichlorosilane production. It can be seen that the degree of purification required is about the same as for diatomite, and it is difficult to see any technical or cost advantage in working with molten silicon or molten silicon-aluminum alloy over working with an aqueous alkaline solution of silica, particularly in view of the extraordinary corrosivity of molten silicon and aluminum towards all known refractories.

TABLE 1

Typical Analysis of Lompoc Diatomite

SiO_2	88.90%
Na_2O	1.44%
MgO	0.56%
CaO	0.53%
Al_2O_3	3.00%
Fe_2O_3	1.69%
TiO_2	0.14%
V_2O_5	0.11%
Loss on ignition	3.60%

TABLE 2

Typical Analysis of "Metallurgical-Grade" Silicon for Trichlorosilane Production

C	.01 - 1.0%
O	.01 - 1.0%
Fe	0.6%
Al	0.4%
Ca	0.25%
Mg	~.01%
Ti	~.01%
B	~.001%
P	~.001%

It therefore appears that an intermediate compound offers the best route to highly purified silicon, and the remaining options are listed according to the choice of intermediate. An ideal intermediate would be inexpensive to produce, easy to purify, and could be decomposed to purified silicon at low cost and high yield and without producing any unnecessary by-products. All known intermediates fall short of this ideal in some way.

The intermediate compounds which have been used in volume production of semiconductor-grade silicon are silicon tetrachloride ($SiCl_4$), trichlorosilane ($SiHCl_3$) and silane (SiH_4). These are discussed in some detail. $SiCl_4$ and $SiHCl_3$ are produced in large quantities for other purposes.

Silicon tetrachloride is produced by the reaction of silicon or silicon carbide with chlorine at about 500°C. In addition to $SiCl_4$, small quantities of polymeric chlorides of the form Si_nCl_{2n+2} are formed. The $SiCl_4$ vapors emerging from the reactor are led to a distillation column. The purified $SiCl_4$ from the column is sold for about \$0.15/lb,[8] or \$2.00/kg Si content. For semiconductor-grade silicon production, the $SiCl_4$ is further purified by repeated distillation. The major difficulty is the removal of boron trichloride. $SiCl_4$ is reduced to Si by reaction with Zn, Na, or H_2.[9] Zinc reduction was used by DuPont to produce silicon in the 1950's. The product was in the form of needles which required considerable densification before they could be used in a Czochralski crystal grower. Dense rods of polycrystalline silicon can be produced by loading a mixture of $SiCl_4$ vapors and hydrogen into a reactor containing a resistance-heated silicon rod; the silicon deposits on the rod. However, trichlorosilane is preferred in this process because it yields a higher deposition rate and a purer deposit.

Trichlorosilane is produced by the reaction between metallurgical silicon and hydrogen chloride in a fluidized-bed reactor at 300°C:

$$Si + 3\ HCl \longrightarrow SiHCl_3 + H_2$$

The reaction is not quantitative since the competing reaction:

$$Si + 4\ HCl \longrightarrow SiCl_4 + 2\ H_2$$

also occurs, leading to the production of $SiCl_4$ and polymers. To suppress this reaction, excess hydrogen is usually added to the input gas stream. The output gas stream is led to a distillation column from which $SiHCl_3$ is obtained. This grade of $SiHCl_3$ is used in large quantities in the manufacture of silicone plastics; the approximate present price is \$0.80/lb, or \$8.50/kg of Si content.[8] For the production of semiconductor-grade silicon, $SiHCl_3$ is further purified by repeated distillation and finally reduced by hydrogen in a reactor as described above. When $SiHCl_3$ is used, the major residual impurity is phosphorus rather than boron, and phosphorus is much more easily removed by zone refining in vacuum.

Regardless of whether $SiCl_4$ or $SiHCl_3$ is used, the composition of the gas phase in the deposition reactor at the silicon surface is closely approximated by the thermodynamic equilibrium composition. Calculations of this equilibrium for the practical range of input gas compositions and reactor temperatures have been carried out by Lever [12], Sirtl [13], and others. A high yield in the deposition reactor can only be obtained by using a large excess of hydrogen in the input gas stream, which increases the amount of electric power required per kg of poly deposited and reduces the deposition rate. The optimum conditions are thus determined by a complex balance between conversion efficiency and power and capital costs. A typical flow chart for this process is given in Figure 3.

Silane (SiH_4) can be produced by a large number of reactions [14] which can be summarized into two classes:

a) Reaction of metal silicides with acids; for example:

$$Mg_2Si + 4\ HCl \xrightarrow{H_2O} SiH_4 + 2\ MgCl_2$$

TRICHLOROSILANE RAW MATERIALS

120 M Kg/Yr. Polycrystal Silicon Plant
8,000 Hr/Yr. Operation

(All Figures In Pounds/Hour)

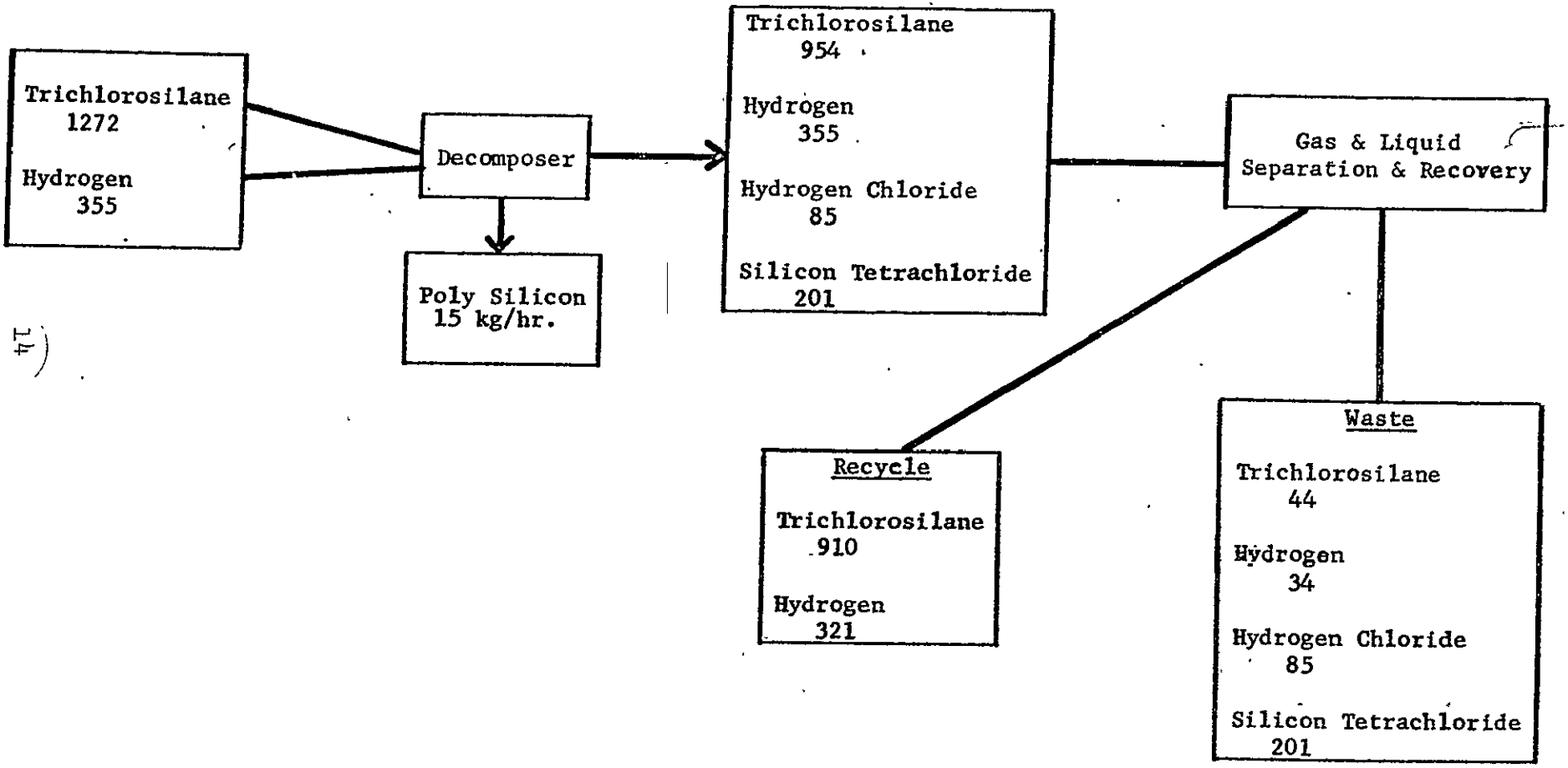


FIGURE 3

This reaction is commonly used in the laboratory; about 25% of the silicon input is converted to silicon hydrides, of which ~40% is SiH_4, ~30% is Si_2H_6, and ~30% consists of higher polymers. The analogous reaction in the liquid ammonia system:

$$Mg_2Si + 4\ NH_4Br \xrightarrow{NH_3} SiH_4 + 2\ MgBr_2 + 4\ NH_3$$

produces a yield of 70-80% of the silicon input, and only silane and disilane are produced. Mg_2Si can be produced at low cost by the reaction between SiO_2 and Mg.

b) Reaction of a suitable silicon compound with a metal hydride; for example:

$$SiCl_4 + LiAlH_4 \xrightarrow{\text{ether}} SiH_4 + LiCl + AlCl_3$$

Although in the laboratory this reaction is most conveniently carried out in a suitable organic medium (e.g., tetrathylene glycol dimethyl ether [15]), in production it is desirable to carry out the reaction in a fused salt bath, so that the hydride formation can occur as part of the overall reaction. Jackson [16] investigated the reaction between Al, H_2 and $SiCl_4$ or SiO_2 in a bath of molten $AlCl_3$/NaCl eutectic (m.p. 108°C, operating temperature 175°C). Very high hydrogen pressures (400 to 900 atm) were required; the reaction mechanism was postulated to involve the formation of $AlH_xCl_{(3-x)}$. At 175°C, 400 atm., the overall reaction:

$$3\ SiO_2 + 4\ Al + 2\ AlCl_3 + 6\ H_2 \longrightarrow 6\ AlOCl + 3\ SiH_4$$

produced silane at a conversion efficiency of ~80%. No information on reaction rates was obtained. Sundermeyer [17] studied the reaction:

$$SiCl_4 + 4\ LiH \longrightarrow SiH_4 + 4\ LiCl$$

in a LiCl/KCl melt at 400°C. The reaction is interesting because the lithium hydride can be produced by electrolysis of the melt to produce lithium metal and chlorine (which can be used for $SiCl_4$ production)

followed by hydrogenation of the lithium metal, using the hydrogen released in the decomposition of the silane. The result is a closed system which converts metallurgical silicon to semiconductor-grade silicon, without any by-products. Union Carbide Corporation obtained patent rights to the Sundermeyer process and developed it into a commercial process for the manufacture of silane.[18] Additional information on this process is contained in the Appendix to this report. Silane is sold for $400/kg, in small quantities, in cylinders. At the present time, one producer of poly (Komatsu Electronic Metals in Japan) uses a proprietary process involving silane. The Komatsu material is more expensive than poly from other producers,[19] but it is preferred by some customers because it does not contain carbon, as does silicon produced from trichlorosilane (10^{18} cm^{-3}).

Although silane is evidently more expensive to produce than other intermediates, it is much easier to purify. The reactions by which silane is produced are advantageous in this respect, since few elements have volatile hydrides (however, among them are B, P and As). Hydrides of B, P and As can be easily removed either by absorption on activated carbon at 0°C or by passing the gas stream over an inert surface at 350°C which will decompose them. Silane is decomposed by pyrolysis in the same type of reactor used for the hydrogen reduction of trichlorosilane.

Dichlorosilane (SiH_2Cl_2) can be produced in relatively low yield (15%) by the reaction of hydrogen chloride and silicon in the presence of excess hydrogen. It is purified by distillation and can be decomposed by pyrolysis, although the yield of poly is better if excess hydrogen is present. Dichlorosilane is currently sold at about $50/kg. The Si-Br-H system has been investigated by Sangster and Sirtl, the Si-I-H system by Sirtl, and the Si-I system by Glang and Wajda. The Si-Br-H system does not seem to be advantageous, since the chemical behavior is very closely similar to the Si-Cl-H system and bromine is much more expensive than chlorine. The Si-I system has some attractive features, despite the high cost of iodine and the relatively low reaction rates attained. Iodide transport (Van Arkel-de Boer process) has been widely studied for the production of pure crystals of refractory metals. The iodide disproportionation reaction:

$$2\ SiI_2 \longrightarrow Si + SiI_4$$

can be used to transport silicon at considerably lower temperatures (925°C) than are needed for the hydrogen reduction of trichlorosilane. If it were not for the fact that many undesirable impurities are also readily transported under the same conditions, a simple reactor of the Van Arkel-de Boer type could be used to convert metallurgical silicon to semiconductor-grade poly or even to single-crystal material. As it is, it is necessary to prepare silicon tetraiodide and purify it in a manner similar to the chlorosilanes, although the purification task appears to be somewhat simpler.

Monocrystal Growth, Slicing and Etching

During the early years of silicon device development, a large number of processes for silicon crystal growth were conceived and evaluated. References to this work (prior to 1965) can be found in the references by Runyan [19] and Crossley et al [20]. After 1965, many of the publications on crystal growth of silicon were related to epitaxial growth processes, which have not been of direct interest in the production of solar cells. Silicon for solar cells has been grown by the standard Czochralski process or its variants, the float-zone and pedestal processes. Although there has been no radical change in the crystal growth technology applicable to solar cells in the preceding decade, costs associated with crystal growth, slicing and etching have been steadily reduced by the introduction of new and better equipment. Czochralski crystal growers have grown larger -- the charge capacity has increased from 1 kg to 16 kg or more during this period -- and automatic control systems have eliminated the need for constant operator attention during most of the growth cycle. Slicers also have been improved to reduce kerf loss and increase cutting speed, and have been fitted with controls for semi-automatic operation. The result has been very substantial cost reductions, primarily in labor costs per unit output, provided that the installation is sufficiently large to take advantage of these new machines. Unfortunately, the lack of gorwth in the solar cell market has not permitted solar cell manufacturers to take the lead in the exploitation of new equipment.

The recent interest in obtaining dramatic cost reductions in silicon solar cells, assuming dramatic production volume increases resulting from widespread application of silicon solar cells for terrestrial power generation, has resulted in renewed activity in the development of new technology for silicon crystal growth and blank fabrication. Some of the approaches aim at elimination of step 6 of blank fabrication (slicing and etching) through the development of techniques for growing silicon crystal in ribbon form. The others aim to replace steps 4, 5 and 6 by the deposition of silicon in thin film form directly from a purified intermediate compound upon a suitable substrate.

Either of these approaches could ultimately lead to a process for continuous fabrication of solar cells, replacing the present wafer-oriented process. This could lead to drastic reductions in processing costs, but would require considerable development work on cell fabrication processes. Initially, the development of ribbon or thin-film silicon is expected to reduce cell costs primarily by eliminating the costs incurred in the present slicing and etching operations. A major part of these costs are the result of the large amount of monocrystalline silicon consumed in these operations.

In principle, the most attractive approach is the deposition of a thin film of silicon from the purified intermediate compound upon an inexpensive substrate. At present, cells fabricated from such material exhibit very low efficiency (<2%); unless their efficiency can be increased substantially their economic potential is not great. Since it is not yet known what changes in deposition process and substrate material will improve efficiency, an economic analysis of thin film silicon cells is premature.

Growth of silicon crystral in ribbon or sheet form, eliminating slicing and etching, has been developed to the point of providing material of satisfactory quality for solar cell fabrication and this option will be discussed in this section. The two processes considered are edge-defined film-fed crystal growth (EFG) and web-dendrite crystal growth. Detailed cost projections for these processes are speculative because these processes have not been developed to the point of production use.

A third option is the further development of the wafer-oriented technology used in production today. For this option, the technology is well understood and detailed cost projections can be made; therefore this option is discussed in Section IV: Cost Analysis.

Ribbon Growth

Both the EFG and web-dendrite processes can be considered as variants of Czochralski growth. In the standard Czochralski technique, a single-crystal seed is dipped into the melt, which is maintained at a temperature a few degrees above the melting point. Since heat can flow from the melt through the seed crystal and pulling spindle, the crystal begins to grow. The diameter of the crystal is controlled during growth by controlling the rate at which the crystal is withdrawn from the melt, balancing this rate against the rate at wich the melt in contact with the crystal solidifies, which depends on the rate of heat flow across the interface. Heat is removed by conduction into the growing crystal and then primarily by radiation from the crystal surface to the walls of the crystal puller. In order to grow a uniform crystal, the thermal environment is designed to have axial symmetry, and both the crucible and the crystal are rotated to average out any residual assymetries. The result is a cylindrical crystal of uniform diameter.

While in principal crystals of different shapes could be grown by modifying the thermal environment only, in practice ribbon crystal growth requires further modifications of the standard Czochralski process. In the EFG process (21), the crystal is grown from the top of a die. A layer of melt is maintained on the top surface of the die by a capillary flow from a reservoir below, and the dimensions of the melt layer are defined by the edges of the die. The growing crystal therefore tends to have the same cross-section as the top surface of the die. In the web-dendrite process (22), the thermal environment of the melt is adjusted so that the top surface of the melt is slightly below the freezing point, although the melt at the crucible walls is above the freezing point. A special seed is used, which under the proper conditions will nucleate two dendrites. Between these dendrites a web is formed.

In ribbon growth, the linear growth rate is much larger than in the standard Czochralski process, because of the much larger surface to volume ratio of the ribbon which increases the rate at which heat flows from the freezing interface. In both processes the ribbon width is limited by the difficulty in maintaining a uniform thermal environment over the width. Consequently, the cross-sectional area of the ribbon is very small compared to the cylindrical crystal grown by the standard process, and the productivity of the crystal furnace is low, unless multiple ribbons can be grown simultaneously. The standard Czochralski crystal grower described in Section IV grows 3" diameter crystal at 1.7 mm/min., or about 8 cm^3/min. To maintain the same productivity, growing 0.2 mm ribbon at 5 cm/min., would require the simultaneous growth of 20 ribbons, each 4 cm wide.

We have not yet taken account of the fact that 50% to 70% of the crystal grown in the standard Czochralski process is consumed in the slicing and etching operations. If 100% of the ribbon material was good, a ribbon process might compete in productivity if only six ribbons could be grown simultaneously. However, even the most enthusiastic proponents of ribbon growth do not project a 100% yield. They usually do assume that substandard ribbon can be remelted; this remains to be demonstrated. In standard Czochralski crystal growth large chunks of substandard material are remelted, but wafers are not remelted.

The inherent advantage of a ribbon growth process arises from the possibility of eliminating the loss of silicon in slicing and etching. The problems which must be overcome in order to make ribbon growth a practical production process arise from the complexities introduced in forcing the crystal to grow in a highly assymmetric shape. To achieve any saving, all of the following technical objectives must be reached:

Crystal quality: The crystal quality (lifetime, etc.) must be as good as the quality of present Czochralski material. Any loss of quality which produces lower efficiency in the cell will be reflected as a severe cost penalty on the ribbon process, since the penalty must include not only the cost of manufacturing additional material but also the costs associated with cell manufacture, array manufacture and land costs resulting from the larger area of converter surface required to supply a given load.

In the early 1960's, a solar cell pilot line was operated by Westinghouse using web-dendrite material, and a median efficiency of about 10% (AM1) was achieved (23). This efficiency was slightly lower than the efficiency of conventional cells produced at that time. The web-dendrite process has also demonstrated the ability to produce dislocation-free crystal (24) in thicknesses less than 25 μm.

The present quality of EFG ribbon is not as good as the Westinghouse web-dendrite material. Tyco data on solar cells has shown there are problems. Some of the earlier cells made from a baked die had an efficiency of about 5%, which would be expected to increase to about 7% after anti-reflection coating. The lower efficiency of EFG ribbon material results from relatively poor crystallinity and also from contamination of the silicon crystal with lifetime-killing impurities from the die material. Some more recent cells are claimed to be over 10% efficiency.

Multiple ribbon growth: If multiple ribbons cannot be grown simultaneously, it is difficult to see how ribbon growth costs can approach the costs of the conventional process. The costs associated with conventional Czochralski growth, per machine-hour of operation, have changed very little with time; the cost reductions per kg of product which have been obtained over the last decade have resulted from increased machine productivity.

Both the web-dendrite process and the EFG process place much more stringent requirements on the crystal furnace. Because the top surface of the melt must be undercooled in the web-dendrite process, temperature control of the melt is very critical. In both accuracy and speed of response, the web-dendrite process is one to two orders of magnitude more critical than the conventional process. These problems are sufficiently severe so that multiple ribbon growth does not seem to have been attempted with the web-dendrite process.

The EFG process does not require better temperature control, but it does have stringent requirements on the die, which must be wet by the molten silicon (to permit the capillary flow which replenishes the liquid film on the top surface of the die) but the die must not be chemically attacked by molten silicon. No material which has been tried appears to fully meet these requirements.

Dimensional control of the growing crystal is clearly more difficult with ribbon growth. In conventional cylindrical crystal growing, crystal diameter is optically sensed and maintained constant by varying the pull rate. In the Westinghouse web-dendrite work, the larger dimension (width) of the ribbon was sensed optically and the smaller dimension (thickness) was sensed by mechanical fingers riding on the ribbon some distance above the freezing interface. Dimensional control was by variation of pull rate, and large differences in pull rate as growth progressed had to be accommodated by the control system. The separation between the point at which ribbon thickness is sensed and the freezing interface introduces a time lag into the control loop, a lag which varies with pull rate. Considerable difficulty was encountered in maintaining constant dimensions, but by the end of the program width was controlled to 9.75 ± 0.12 mm and thickness to $0.4 \pm .06$ mm (23).

In principle, dimensional control of EFG crystal growth should be much simpler, because crystal dimensions are stabilized by the growth process to closely approximate the dimensions of the die. In practice, EFG silicon crystals do not exhibit close dimensional control at present.

Dimensional control is discussed here because it is obvious that multiple ribbon growth will be very difficult, and probably totally impractical, if the dimensions of each ribbon must be independently sensed and the pull rate of each ribbon independently controlled in order to achieve satisfactory uniformity. The EFG process appears to have a clear advantage over the web-dendrite process in this respect, at least in principle. The fact that EFG growth of multiple sapphire ribbons has been demonstrated without independent control does not necessarily imply that independent control will not be required for the EFG growth of multiple silicon ribbons, however. Heat flow from the freezing interface in sapphire is primarily by optical radiation through the transparent crystal. This mechanism provides much more stable growth in the presence of fluctuations in the thermal environment.

Silicon utilization: As discussed above, the standard process appears capable of utilizing no more than about 40% of the input polycrystalline silicon (for a final blank thickness of 0.15 mm). The silicon utilization for ribbon processes can, in principle, be much higher, but further development is required to achieve high utilization factors. In the web-dendrite process, the dendrites contain many dislocations. Trimming off the dendrites improves the efficiency of the final cell but reduces silicon utilization, as well as adding another operation. In the EFG process, a means for continuously replenishing the melt is required in order to maintain the proper level for capillary flow in the die. The use of a floating die is an alternative, but there are also problems to be solved with this approach.

It is also important to realize that growth of unnecessarily thick ribbon reduces the effective utilization fraction. With a proper back contact, cell output falls off very little with decreasing thickness and the minimum practical thickness is determined by yield loss from breakage during cell fabrication. While the web-dendrite process has produced web as thin as 15 μm, the EFG process is having some difficulty in producing ribbon as thin as 200 μm. To produce thin ribbon, a narrow die containing a still narrower slot must be used. This makes the die more expensive and more quickly affected by reactions between the die material and the silicon melt.

At the present time, it does not appear from the literature studied that either the web-dendrite or the EFG process has consistently demonstrated significantly higher silicon utilization than the standard process can attain. During the Westinghouse program in 1963-65, silicon utilization of 55% was reached towards the end of the program, before allowance for the further loss of silicon during dendrite removal. No data is available on silicon utilization in the EFG process.

IIIB. CELL FABRICATION

This report section will begin by reviewing the present solar cell and array fabrication processes to determine the parameters which have a major effect on cost. Those technological options presently available for a large-volume, low-cost manufacturing process will be considered first and finally some options which might become available as a result of future development will be discussed.

In the area of cell fabrication, the number of options which could be considered is very large. To evaluate the technical merits and cost advantages of each option in detail would be laborious, and also of little value in the ultimate analysis. In most cases the cost difference between competing options will be found to be small, considerably smaller than the uncertainties involved in projecting costs to production levels up to one million times present levels. Therefore, we have chosen to discuss the process options in terms of the generalized process flow chart (Figure 1) and the various approaches available for cost minimization. A detailed cost estimate for one particular set of process options is given in Section IV: Cost Analysis.

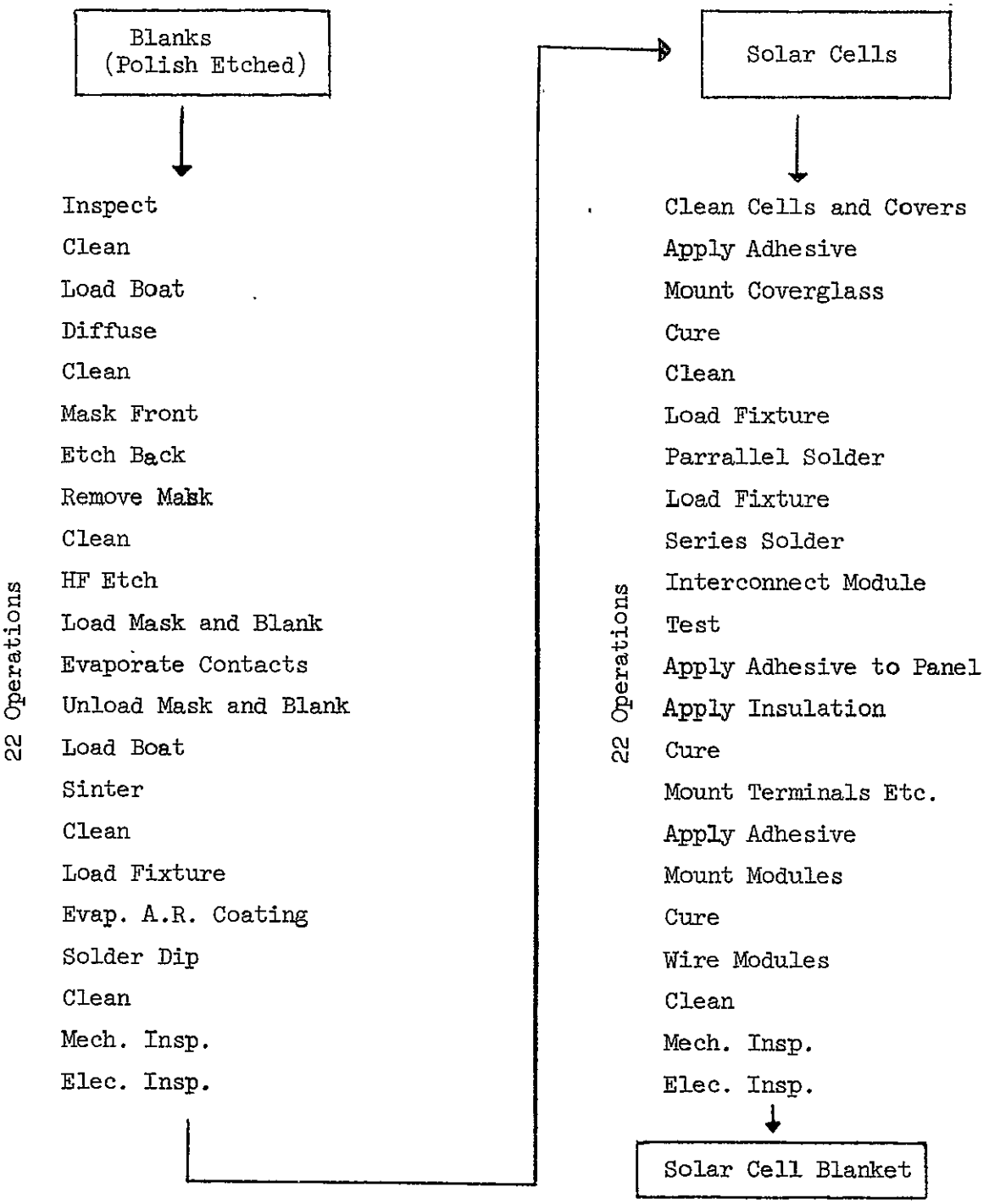
Present Cell Fabrication Technology

A flow chart for present cell and array fabrication for space purposes is given in Figure 4. Forty-four separate operations are shown as being required to complete steps 7-11, of the simplified process flow chart (Figure 1), which carries the array through module interconnection. Not shown in Figure 4 are many other operations which are not in the direct process flow but are nevertheless essential; for example, periodic cleaning of diffusion tubes, boats and evaporation masks.

Most of of the cell fabrication operations listed in Figure 4 involve manual handling of individual blanks, and in most operations the production rate

FIGURE 4

Present Cell and Array Fabrication



per operator is determined by the speed with which blanks can be manually handled. Typically, an operator with average dexterity will achieve a rate of about 250 blanks/hour throughput in such an operation. Thus one might estimate that 22 opeators could process 2000 blanks/day, or 500,000/year. However, because of the incidental operations not shown in Figure 4, and because allowance must be made for absenteeism, training, machine down-time, etc., this estimate would be about a factor of two too low. Even so, since total solar cell production at present is of the order of 1,500,000 cells/year for the entire industry, it can be seen that the total number of operators involved is quite small.

Production costs for solar cells at present are made up of the following components:

Direct production labor	25%
Indirect production labor (Supervision, maintenance, QC, etc.)	25%
Materials	21%
Other overhead (facilities and equipment costs, etc.)	18%
General and administrative costs	11%
	100%

About one-half of the materials cost is silicon; other important materials are acids, gases, solvents and silver.

For the semiconductor industry as a whole, the amount of capital required per dollar of net sales ranges from $0.50 to over $1.00. Solar cell manufacturing is at the bottom end of this range, primarily because the processing operations are labor-intensive and therefore the capital investment required for plant facilities and equipment is unusually low.

For steps 11-12 (array fabrication up to system integration) the break-down of productions costs and capital requirements is not substantially different than for cell manufacture on the whole, although spacecraft arrays are much less standardized than cells and so the cost distribution varies more widely from job to job. In general, the cost of a completed array will be three to four times the cost of the cells contained in it. In addition to cells and coverglasses, the substrate

material itself is a major cost item.

Since each operation requires only a few minutes at most, it is technically possible to process a cell from a sliced blank through to its place in the final array in a single day. In fact, this is not done. Partially processed cells are held at various points in the process for considerable periods of time. While this adds somewhat to cost, it also provides time for in-process inspection and correction of processing difficulties.

Current Technology Cost Reduction Options

In terms of annual volume, the silicon solar cell is a very low volume semiconductor device. If one assumes that in the near future production volume will begin to increase rapidly, a natural approach is to utilize machinery and techniques already in use in the production of high-volume semiconductor devices and other high-volume electronic components. While considerable technology is available at present which could greatly reduce production costs, this technology must be adapted to the specific requirements of solar cell manufacture, and in most cases this will require modifications to the production process.

Cost reduction can be accomplished by eliminating some of the process operations, developing new processes that combine steps, by simplifying the step and making it less critical, by designing machines to speed up the process, by minimizing the number of handling operations, and by using inexpensive materials. A detailed list of cost reduction options are summarized in Table 3. All options will probably not be able to be utilized with every new process developed but an attempt must be made to utilize as many as possible. For instance, a high-speed process is highly desirable but not a necessity for a lowcost process. If a large batch is to be placed in an oven for sintering or a heat treatment, this may require a long time, but because a large quantity is processed at once, it can be inexpensive. Therefore, each process operation must be analyzed on a cost per unit processed basis before it is clear that cost improvement is available.

TABLE 3

COST REDUCTION OPTIONS

1. Reduce number of steps
2. Mechanize handling operations
3. Increase cell area
4. Use continuous flow process
5. Increase process throughput
6. Simplify process
   - Eliminate masking and evaporation
   - Eliminate wet processing
   - Eliminate critical tolerances
7. Reduce indirect material usage
8. Select processes with high controllability (high yield)
9. Integrate operations (assembly)
10. Reduce energy usage

Junction Formation

Junction formation is typically accomplished by the open tube gaseous diffusion process. In this process the silicon blanks are loaded onto a fused silica boat which is placed in a tube furnace. The material is allowed to heat up for several minutes, then a gaseous compound of the desired impurity type (either N or P type) is passed through the tube. Some of the impurity deposits on the silicon and is diffused the proper depth into the bulk material. The boat is then removed from the furnace to cool the material.

The complete process typically requires about 20 to 30 minutes and about 800 cm^2 of material is diffused. Modifications of this process that are likely to result in cost reductions are: the batch size could be increased, the diffusion time can be reduced by increasing the furnace temperature, or the operation could be mechanized to have continuous processing with preloaded boats continuously fed in on a belt system.

Another diffusion method that has been developed and proven satisfactory for solar cells is the paint-on source technique. In this process a dopant compound is simply coated on the silicon, dried, and the silicon placed in a furnace to accomplish the diffusion. At first glance, this looks as if more costs are added since an additional coating step precedes diffusion. The interesting aspect, however, comes from some of the options that result. One important factor is that since the dopant source is directly applied to the silicon surface, the material can be stacked in a boat much more closely than material going into a gaseous diffusion furnace where space for uniform mixing of the gas must be provided. Therefore, a higher packing density and throughput rate can be achieved with equivalent tube furnace facilities. The process is very well suited for a continuous belt furnace operation. The problems of controlling various gaseous atmospheres in different zones is eliminated thus making the gas system simple. There is no operator required except to load and unload boats.

Many other diffusion processes have been used in the semiconductor industry in addition to the two mentioned above (25). Instead of an open

tube, a sealed capsule or partially sealed box can be used. Instead of introducing the diffusant in the gas stream or painting it on, the diffusant can be deposited on the wafer surface by chemical vapor deposition, or generated in the tube by a suitable chemical reaction: for example, oxidized boron nitride wafers can be placed between the silicon wafers in the diffusion boat; boron oxide volatilizes, deposits on the adjacent silicon surfaces and acts as a source for boron diffusion. These variants of the basic diffusion process each have their advantages and disadvantages, but it does not appear that any particular choice would have a large cost impact.

Junction formation can be accomplished by other means than diffusion. Ion implantation is one such technique. In this approach, a suitable compound containing the desired dopant is introduced into an ion source, in which a plasma is formed. Ions are extracted from the plasma by an electric field. A crossed magnetic field may be used to separate the desired ionic species from others. The ion beam then bombards the silicon wafer. The depth of penetration of the ions can be very accurately controlled by controlling the accelerating voltage, while the number of ions per unit area can be accurately controlled by controlling the ion current and bombardment time.

Ion implantation requires equipment which is more complex and expensive than diffusion equipment, but this need not produce a substantial increase in cost per unit processed, if the equipment throughput is high enough. Ion sources for boron, phosphorus and arsenic are available (26,27) which produce 1 to 4mA of ion current, which is sufficient to dope silicon at the rate of about 1 cm^2 cell area per second. This compares quite well with the present throughput of a diffusion furnace. Ion sources have been built for hydrogen ions which produce several amperes of ion current. (28) Since the output of an ion source is expected from theory to vary as $1/\sqrt{M}$, where M is the ion mass number, ion currents of several hundred milliamperes should be attainable for common dopant ions. Mass separation is not required for the solar cell application; and accelerating voltages are low (of the order of 40 KV) because the junction is shallow. Annealing is required to eliminate radiation damage produced by the implantation process, but the energy input to raise the silicon to the annealing temperature can be supplied, at least in part, by the ion beam itself.

Another approach to junction formation is to use a Schottky barrier rather than a P-N junction. Metal films with sheet resistances comparable to the sheet resistance of the diffused layer in P-N junction cells can have values of light transmission as high as 90%, with a suitable AR coating.(29,30) Since the height of Schottky barrier in silicon is always considerably less than the band gap, Schottky barriers are probably better suited for use with larger band gap materials than silicon. However, this may be the best approach to the fabrication of solar cells in polycrystalline silicon, if low conversion efficiency does not rule out polycrystalline silicon entirely.

Whichever approach to junction formation is selected, consideration must be given to the region in which the junction intersects the surface in order to avoid large leakage currents. In present processing, using gas-phase diffusion sources, impurity diffusion occurs at both surfaces of the blank. The junction at the back surface is removed by etching after diffusion. An alternate approach applicable to N+/P cells is to use an aluminum-alloyed back contact.(31) The N+ layer at the back surface is dissolved during the alloying process and an N+/P/P+ structure is produced. An edge etch is required to avoid formation of an N+/P+ junction at the cell edge.

Contact Deposition

Contacts are typically deposited by evaporating suitable contact metals on the silicon wafer through a mask etched to the desired grid pattern. The vacuum evaporated system is usually set up with dual top and bottom evaporation sources so that both sides of the cell is coated at the same time. Some installations use one evaporation source with a rotisserie type fixture to provide metal deposition on both sides of the cell. In general fairly small evaporators are used since the production rates are small. Typically, 0.1 to 0.2 m^2 of cell surface are coated in one operation.

Cost reductions could be realized by going to still larger walk-in type evaporators that have continuous feed wire sources. This type system would increase the throughput rate from about 0.3 m^2 of cell area per hour to over 2 m^2 per hour. Mask loading and cell handling could be completely mechanized so that labor would be minimized.

Another evaporation system technique that could be used is a ferris wheel arrangement within the vacuum chamber which mechanically brings the blanks over a fixed evaporation source and mask. The major advantage of this technique is that a minimum amount of metal is wasted.

Plating has been used for metal contact deposition in past years. This requires some sort of masking material placed on the cell in the proper pattern to prevent the metal from plating where not wanted. This masking can be performed by a photoresist operation or by a screen printing operation. Screen printing is less expensive but cannot produce grid lines as narrow as photoresist. In either case the masking material must be removed after plating; thus two additional operations are introduced. Plating has the advantages that metal is deposited only where needed, reducing metal costs; also, copper or nickel can be used rather than silver, and the thickness of the plating can be greater than can be conveniently deposited by evaporation. Despite these advantages, the replacement of plated electroless nickel contacts by evaporated titanium-silver contacts led to lower costs, because the evaporated contacts led to higher yields. It was found to be very difficult to produce consistently adherent, low-resistance contacts by plating.

A very fast contact deposition method is the screen printing technique whereby a metal paste is simply printed onto the surface in the pattern desired. The printed metal paste is then heated in a furnace to volatilize the binder, sinter the metal particles and make an ohmic contact to the silicon. Although this type contact has not yet been fully developed, it would be a very attractive approach since

completely automatic printing machines capable of handling 20 cells per minute are available. Also there is essentially no waste of material and low-resistance grid lines can be formed. However, as with the plating technique, there appears to be a difficult problem in achieving consistently good adherence and ohmic contact.

Antireflection Coating

Antireflection coatings are presently deposited by vacuum evaporation. Since the AR coating is deposited on only one surface of the cell and the coating is very thin, the production rate can be two or three times the rate of metal contact evaporation. This process can be easily scaled up to larger vacuum chambers to increase throughput. Either masking must be used to prevent deposition of the coating material on the contact bar, or the contact bar must be cleaned (chemically or mechanically) to remove the coating material prior to soldering or welding the interconnector to the cell.

When boron trichloride is used without oxygen to produce a P^+/N cell with a very heavily doped surface, a surface layer of a silicon-boron compound is formed which is an effective antireflection coating. The coating does not interfere with electrical contact to the cell. The surface layer does have some optical absorption and the very high surface concentration of boron does lead to the introduction of defects into the surface region of the cell; for these reasons, P^+/N cells made in this way have slightly lower short-circuit current output than cells diffused in an oxidizing atmosphere, which avoids formation of the silicon-boron compound. Cell conversion efficiency is still quite acceptable, however. No similar technique is known for forming an antireflection coating on N^+/P cells during diffusion.

Although an optimum antireflection coating is very thin (one-quarter wavelength at 600-650 nm), thicker coatings are almost as good if they have the proper index of refraction and low optical absorption. Consideration has been given to a coating applied by spraying or spinning, in the same manner as a diffusion source. The desired index of refraction is 1.95, if the outer surface of the coating is in

contact with air, or about 2.35 if the outer surface of the coating is in contact with a protective layer of glass or plastic. The highest refractive index obtainable for a plastic coating is about 1.6 (polycarbonate lacquer); spin-on glass coatings can be formulated with indices of 1.95. Both coatings have adequate durability. Thick coatings of either material will have a reflection loss of about 21%, compared to 35% for bare silicon and about 6% for silicon coated with an optimized antireflection coating. If a suitable coating could be found with an index of refraction of 2.5, a two-layer thick coating (indices of 1.6 and 2.5) would have a reflection loss of 14%. Unfortunately, neither plastics or glasses appear to be available for the higher-index coating.

The figures given above are computed for light at normal incidence. In typical solar photovoltaic system designs for terrestrial applications, the cells are illuminated over a wide range of angle of incidence; this is true both of flat-panel, fixed-position arrays and tracking arrays using optical concentration. The effect of non-normal incidence is to increase reflection losses for all types of coatings, and to somewhat reduce the relative advantage of quarter-wave coatings over thick coatings.

Cell Testing

Testing of cells prior to assembly of the array is required to:

1) Eliminate low-output cells;
2) Sort acceptable cells into output classes, so that the cells making up a module have matched characteristics, otherwise the curve factor of the module will be seriously degraded;
3) Provide feedback for process control.

Although cells for space applications undergo stringent visual and mechanical inspection as well as electrical tests, the performance of arrays assembled from reject space cells in terrestrial applications strongly suggests that electrical tests are sufficient. The electrical tests consist of illuminating the cell and measuring the electrical output (current as a function of voltage). The illumination intensity, spectral distribution, and cell temperature must be known and maintained

constant. Limiting the testing to electrical measurements is highly desirable because such measurements can be taken rapidly, and the test equipment is readily adapted to computer control to eliminate human error and to provide for data analysis. This feature is important to provide rapid feedback for control of a high-speed fabrication process.

Evaluation of Cell Fabrication Options

Instead of evaluating options one by one, it is more informative to consider the overall process, and to attempt to define the requirements for minimizing production cost in terms of a consistent philosophy which can then be applied to each process operation. For the present process, the dominant cost factor is labor, and one obvious requirement for cost reduction is increased throughput per operator. The first six approaches in the list in Table 3 provide ways of satisfying this requirement. Mechanical wafer handling equipment can process at least 10,000 blanks per shift (assuming the rate of throughput is determined by handling time) even if blanks are handled one at a time. This is five times the rate attainable with manual handling. Increasing the size of the blank from 2 cm square to 7.5 cm diameter increases the area processed per blank by a factor of 11, thus these two changes alone, without any changes in the basic process operations, can increase throughput by a factor of 55. It is reasonable to expect that mechanical handling in properly designed machinery will reduce the possible sources of contamination and permit elimination of most of the in-process cleaning operations. Computer control of the machinery should eliminate much of the direct and indirect labor now required to keep track of the progress of blanks through the fabrication operations, as well as providing prompt feedback to maintain high yield.

Overall, it appears to be possible to reduce direct labor unit costs by as much as a factor of 100 by mechanization. The saving in indirect labor costs and other overhead costs will be less, because the more complex machinery will no doubt increase the percentage of cost associated with equipment maintenance and depreciation. However,

substantial cost savings when costs are expressed in dollars/watt should be attainable in these areas also.

It would therefore appear that the most important criterion to be applied in evaluating the options for each process operation is that the option should be compatible with mechanization. While some type of mechanization can be applied to almost any conceivable type of production operation, the combination of options finally selected for a particular process should all be compatible with the same type of mechanization, in order to provide maximum efficiency.

A major difficulty in selecting one mechanization approach is that some operations require high temperature, others require exposure to strong acids, and still others require process operations to be performed under high vacuum conditions. Sequences of production operations have been conceived (32) which might permit all required operations to be performed on a continuous basis; however, the necessary changes in individual operations are drastic and the development work is not far along. Even if a completely continuous process were technically feasible, the difficulty of introducing further changes would be a serious disadvantage in a field in which rapid technological progress is expected..

It appears that the best approach for the near future is to concentrate on mechanizing the transfer of blanks between operations, leaving the operations themselves to be performed on a batch basis as at present. This may also be the best approach for the long run, particularly if long ribbons of silicon cannot be provided at low cost.

Even though the specific process operations for solar cells differ considerably from those used for fabricating other semiconductor devices, the transfer operation is identical if round blanks rather than square blanks are used. Mechanical equipment for handling round wafers has been developed by several firms for the semiconductor integrated circuits industry, and this equipment is coming into widespread use. A discussion of the principles employed by one firm in the design of its equipment is given in reference (33) and is reproduced in the appendix.

Other firms use slightly different principles, but all firms agree on standardization of two items:

a) The wafer must be round, and all wafers must be the same diameter ($\pm$ 3mm)

b) Wafers are handled in carriers, which contain 25 wafers held in slots with a spacing of 1/8" or 3/16".

The first item permits standardization of wafer tracks and handling fixtures within the machinery, and the second permits transfer of wafers from one carrier to another by placing an empty carrier over a full one and inverting. Carriers are provided in aluminum (for routine processing), fluorocarbon or polypropylene plastic (for wet chemical processing), and quartz (for high-temperature processes).

The major problem in applying this type of machinery to a solar cell production process is in adapting it to high-vacuum operations. Existing equipment is not designed for operation in vacuum, and in some cases the design principles are not compatible with vacuum operation. Either the equipment must be redesigned, or the process operations must be altered to replace vacuum operations with others. As discussed in the previous section, there are alternatives available for all vacuum operations.

As long as cell fabrication is wafer-oriented, the use of wafer-handling equipment provides a satisfactory solution to the cell fabrication problem, in that the combination of mechanized handling and compatible processing operations can reduce cell costs (including the blank) to less than twice the cost of the blank itself. If the cost of the blank were reduced far below the cost of $\$75/m^2$ given in Section IV, cell processing costs would require further reduction if they were not to be again the dominant cost item. While the same basic principle of concentrating on increasing throughput per operator would still be applicable, the specific methods to be employed would depend on whether the silicon input to the cell fabrication operations was in the form of wafers, ribbons, or something else. Until this parameter can better defined, a choice between options for the fardistant future cannot be made.

There are important differences between the space and terrestrial environments which require a completely different approach to array design. Radiation resistance need not be considered in a terrestrial system, and ultraviolet light intensity is much lower. The range of thermal cycling is typically smaller and the rate of change of temperature smaller also. On the other hand, the designer must consider the effects of rain, dust, snow and ice build-up, hail, corrosion from seashore and industrial atmospheres, wind forces, bird fouling, human vandalism, etc. The severity of these conditions varies from one installation to another and typically is not well defined, and available information on the endurance of various materials in terrestrial environments is usually of a general comparative nature. Nevertheless, the high capital cost of solar power systems compared to alternatives requires the designer to design for a long life expectancy with minimum maintenance, and in this respect the design requirements are not less severe than for space systems. To meet these requirements, the designer cannot rely either on extensive testing and qualification of units, as is done for space systems, or on large safety factors and redundant elements, as is commonly done for terrestrial structures, since either approach would produce an unacceptable cost penalty.

In space systems, power output per unit mass and per unit surface area are extremely important parameters. In terrestrial systems they are less important, but not negligible. Many present-day applications of terrestrial solar photovoltaic systems are in remote areas, and the cost and difficulty of transportation must be considered. The cost and difficulty of erecting the system is also very important, and the design should be engineered so that the system can be installed with a minimum of skill and equipment.

Even at present, applications for terrestrial photovoltaic systems range from a fraction of a watt to several kilowatts output (peak). Within the next decade it is hoped that cost reductions will permit extending this range upward into the megawatt range, and by the end of the century, into the gigawatt range.

Given this extremely wide range of applications, it would be indeed remarkable if any one type of array design were to be found to be optimal over the entire range. Given the present very limited experience with terrestrial photovoltaic systems, it is difficult to specify even one type of design which is known to be adequate, let alone optimum, for any application. In the area of array design and fabrication, the gap between our present knowledge and what we need to know is much larger than in the other technical areas previously considered, because we cannot draw to a great extent on the experience gained over the last 15 years on space programs to define a baseline from which to project future costs and technological requirements.

Design Requirements

a. Structural: The array as a whole, and its components, will be subject to mechanical forces arising from wind, thermal expansion, and possibly other forces. Failure can occur by catastrophic mechanical failure, and also by fatigue failure due to cyclic stressing. The designer must not only provide load-bearing members of proper material and cross-section to carry such loads, but must also consider the distribution of internal forces to avoid stress concentrations. A particularly weak point is at the connection of the electrical leads to the cell. Because of the low thermal expansion of silicon compared to common metals and plastics, and the brittleness of silicon, this point is inevitably stressed by thermal forces. In addition to designing this connection to resist cyclic stressing, suitable provisions for stress relief should be provided to avoid the transmission of gross structural forces to the connection.

b. Electrical: A silicon solar cell is a high-current, low-voltage generator, and considerable care is required in designing electrical connections for minimum series resistance.

c. Thermal: Array output voltage decreases with increasing temperature. When the load is essentially a voltage source (e.g., a storage battery), the useful output of the array is zero if the output voltage does not

exceed the battery voltage. It is therefore important to minimize the thermal impedance between the cells and the ambient, since this parameter has a large effect on the number of series cells required to supply a given load under worst-case conditions. Heat transfer from the cell to the ambient atmosphere is primarily by conduction and convection, rather than by radiation as in space.

d. Weatherability: In addition to the gross mechanical and thermal forces imposed on the array by the terrestrial environment, there are many aspects of the environment which can lead to failure due to corrosion or obscuration. In particular, transparent materials used to cover the cells (to protect them from humidity, etc.) are likely to degrade due to yellowing (from ultraviolet absorption), abrasion from dust, water absorption, crazing, etc. In plastics, these effects are accelerated by mechanical stresses (internal stresses built-in by molding operations, and externally applied stresses). If possible, the use of a transparent plastic part as a load-bearing member should be avoided for this reason.

e. Manufacturability: Fabrication costs can be minimized by:

1) choosing low cost materials and using them efficiently;
2) designing around standardized modules which can easily be assembled into a range of array sizes;
3) applying the mechanization concepts discussed under cell fabrication, and integrating module fabrication and cell fabrication to the maximum possible extent.

The above requirements are more easily stated than satisfied. The trade-offs involved in practice can be illustrated by considering a simple conceptual design. Consider a module consisting of an assymmetrical I-beam section of extruded aluminum, with a single series string of cells adhesively bonded to the top surface and coated with a conformal silicone coating for environmental protection. An array is assembled by connecting modules together mechanically by end rails, and paralleling modules electrically.

Design Characteristics

a. Structural: Structural requirements are satisfied primarily by the aluminum member, which is light in weight and relatively inexpensive

($ 0.50/lb. for aluminum extrusion in quantity). The I-beam section uses material efficiently, and the mechanical joints at the ends of the module can be made by simple means in the field. The durability of extruded aluminum is generally adequate if the aluminum is properly protected by anodizing or painting. Since the entire structure can be made of aluminum, thermal forces between structural members are minimized. The length of the module is an important design parameter, since longer modules require a deeper section.

b. Electrical: Electrical requirements also affect module length. For simplicity, a module output voltage equal to the desired array output voltage is desirable, but this may result in a module length which is undesirable structurally. A simple series string makes interconnection simple, but is vulnerable to opens and to shadowing. Since in a series string the current in each cell is constant, cell testing and sorting should preferably be at constant current rather than constant voltage.

c. Thermal: Thermal requirements are met very well by this design if the thickness of the adhesive layer under the cell and the conformal coating over the cell is kept to a minimum. This is best done if these layers are applied in the form of films and laminated to the cells and aluminum I-beam, perhaps in the manner developed at NASA-Lewis (34, 35, 36). The lamination process would need considerable development for this application. Silicone resins applied as liquids can also be used. For applications involving optical concentration, the thermal impedance can be reduced by changing the aluminum extrusion die to add fins to the aluminum beam; this can be done without otherwise affecting the array fabrication process.

d. Weatherability: Weatherability factors are the weakest point of the design. The conformal coating provides environmental protection; it must be flexible to prevent cracking under thermal cycling, but this conflicts with the desire for a hard abrasion-resistant surface. Extremely good adhesion to aluminum, silicon, and the electrical interconnector is necessary to prevent moisture entry and delamination at mating surfaces; plastics which have high bond strengths are not

especially good in chemical stability or ultraviolet resistance. One way of avoiding these conflicts is to use an outer window of glass with a resilient plastic filling the gap between the glass and the aluminum; this adds another layer of material, increasing cost and thermal impedance, and the requirements on the plastic are reduced only slightly. The resilient plastic layer is now sandwiched between two rigid materials with different thermal expansion coefficients, which further aggravates the problem of maintaining good adhesion during service life.

e. Manufacturability: Manufacturability of the basic design is excellent, but the variations which may be required to meet performance requirements complicate processing and increase cost. It is clear that some economic balance must be sought between fabrication cost and service life, but the proper economic balance will differ substantially for different users and in any case the necessary data for the computation are not available.

While the specifics of the above discussion apply to one particular design, the general problem of defining and improving cost-effectiveness in array design and manufacture apply to any design. Figures of merit such as dollars per watt are not really the best choice for comparing array designs, since they do not include the important parameter of expected service life. Fortunately, if a simple array design is chosen, the additional cost associated with the array manufacturing operations can be reduced to a fraction of the cost of the cells, at least until cell costs decline substantially below the costs projected for the 1980-85 time period. During the next decade, one can hope that experience will provide more data on materials properties and service performance so that array fabrication costs can be reduced in parallel with cell costs without impairing service life.

IIID. OPTICAL CONCENTRATION

Optical concentration is an available technological option which can be exploited to increase cell output. System cost in dollars per watt will be reduced as long as the added costs for the optical elements, additional structure and cooling, and the costs of sun tracking, if used, are less than the saving produced by reducing the number of cells required to power a given load. The system net energy cost (energy consumed in fabricating the system) and the energy payback period can also be substantially reduced by optical concentration if the energy cost of the additional optical elements is less than the energy cost of the solar cells they replace. This will usually be the case.

As the optical concentration ratio "m" is increased, cell current output increases proportionally but cell power output increases more slowly because cell temperature increases and the power dissipated in the internal resistance of the cell also increases. As m increases, the cost of the optical elements, structure, cooling and tracking also increase. Higher concentration ratios require more perfect optical elements, more accurate alignment and tracking, and more complex cooling systems. Also, as m increases, the field of view of the system is reduced and some part of the diffuse sky radiation is lost.

The optimum value of m is thus determined by a complex balance between many factors. This problem is presently being investigated by Arizona State University and Spectrolab under NSF and ERDA sponsorship. However, the following general conclusions can be drawn from the report on the first year of this study (37):

a) The optimum concentration ratio depends on cell cost, and goes down as cell costs decline relative to the costs of other elements.

b) The optimum concentration ratio also depends on the value of the thermal output from the array. If only electrical output is of interest, the value of the thermal output is negative (since costs are incurred in dissipating the heat). If the thermal output is useful, a higher concentration ratio is optimum to raise the temperature of the thermal output. Pushed to the limit, the system becomes a solar thermal system with electrical output as a by-product. In this connection, it is interesting that a silicon solar cell is a near-optimum selective absorber; indeed, silicon thin films are being used in one experimental study of solar thermal power systems at the University of Arizona.

c) Large reductions in silicon solar cell series resistance can be achieved by improved designs, without sacrificing efficiency or cost. The most effective design change is the use of ribbon conductors bonded to the front of the cell to minimize the length of the current path in the contact metallization. With optimum cell design, high efficiency can be achieved in low cost cells up to illumination levels of at least 10 watts/cm^2 (100 suns terrestrial).

d) Significant improvements in thermal resistance (cell to ambient) can be achieved with optimum choices of cell mounting methods and heat transfer surface configuration.

e) Optimum values of concentration ratio are typically in the range of 10 to 40. Because these values are fairly low, there is a wide range of choice for the optical elements, and the accuracy with which the optical surfaces must be fabricated is low. Additional work is needed to determine the lowest cost optical concentrator in this range; also, attention should be paid to achieving as nearly uniform flux distribution in the exit plane as possible.

f) For favorable locations, it is possible to reduce energy costs by more than a factor of 3 through optical concentration, assuming unconcentrated array costs of about $\$250/m^2$ as projected in Section IV for the early 1980's. In other words, the proper use of optical concentration would reduce the manufacturing cost of arrays from the figure of \$2.15/watt projected in Section IV to the equivalent of \$0.70/watt. As array costs decrease further, the savings from optical concentration also decrease but remain appreciable even at array cost levels of $\$50/m^2$ (under \$0.50/watt) for unconcentrated arrays.

From these results, it appears that the use of optical concentration is a very powerful approach to achieving large reductions in the cost of photovoltaic solar energy in the near future, in favorable locations and applications. However, optical concentration increases system complexity and therefore is most likely to be applied to large systems for which the increased engineering design and installation costs will not constitute a severe cost penalty. Optical concentration can be applied to space systems as well as terrestrial systems, although the degree of optical concentration which is practical for space systems is lower because of the increased difficulty of heat rejection. For the low concentration ratios found to be optimum in the ASU-Spectrolab study, the additional costs involved in fabricating cells and arrays designed for use with optical concentration were found to be small.

IV. COST ANALYSIS

General

In this section, we will make the cost analysis by presenting cost estimates for cell and array fabrication based on similar assumptions. In general, our assumptions are that we will be using the best currently available technology, with reasonable engineering extensions to fit this technology to our needs. We are not assuming any major changes in process technology, but we are assuming certain improvements in process technology which we regard as reasonable, low-risk assumptions. In the blank fabrication area, we assumed that:

a) the cost of poly would be $35/kg; and
b) kerf loss in cutting could be reduced to 0.15 mm and etching loss to 0.05 mm.

We have experimentally verified that good solar cells can be produced from off-grade material which can be purchased for about the assumed price, and that removal of 0.03 mm/face from saw-cut slices, in sodium hydroxide etchant, produces and adequately damage-free surface. We have not experimentally verified the assumed reduction in kerf loss from 0.30 to 0.15 mm, but manufacturers of blades and slicing equipment have stated that they believe this goal is attainable within current technology.

There are many options available in the cell fabrication area which would produce cells of very similar characteristics and cost. We have chosen a process involving the use of conventional thermal diffusion for the junction formation step, with spin-on diffusants applied to both surfaces of the blank (a phosphorus-containing diffusant on one side, a boron-containing diffusant on the other). Two diffusants are not strictly necessary, particularly if low-resistivity silicon material is used, but will produce a better cell. Contacts are applied by screen printing; we have verified that contacts

of acceptable electrical and physical characteristics can be made in this way. The anti-reflection coating is assumed to be applied by a spin-on technique; we have received samples of an AR coating material for spin application but have not verified its performance as yet. The final processing step is an operation to remove the P+/N+ junction at the edge of the cell; this can be done by stack etching if round cells are to be produced, or by diamond sawing if another shape is to be cut from the round blank. If maximum packing factor is desired, the best choice is a hexagon, which can be produced by three passes through a double-bladed saw. The hexagonal cell has 82.7% of the area of the round blank from which it is cut, while a square contains only 63.7% of the area of the round blank.

After testing and sorting by automatic machinery, cells are interconnected by soldering, using automatic machinery to cut and form the mesh interconnectors and to solder the interconnectors to the cell. Although no machinery exists which performs these operations in precisely the required way, similar machinery has been built to automatically test, sort and interconnect the 2 x 2 cm cells used in space applications. The basic technology is well known and we see no reason why such machines cannot be built, although the development of a completely satisfactory machine is not a trivial engineering project.

Interconnected strings are laid down on anodized aluminum extrusions (for mechanical support and thermal control) and coated with a silicone conformal coating.

The cell and array design and processes which we have chosen for analysis are reasonable choices for the near future. The fact that considerable technological developments will occur which will provide new options for further cost reductions. At the time at which these options become technologically feasible, their economics will be evaluated against the costs of the conventional technology at that time period. In the next

section, we present cost estimates for the baseline process as it might be carried out in a minimum-sized plant in the near future. In subsequent sections, we attempt to project unit costs at higher production rates, for this same process and design. These estimates are quite rough, but are intended to provide some idea of the unit costs attainable with conventional technology as a function of production rate and time, and therefore to define the economic environment in which the evaluation of future technological developments will be carried out.

Detailed Cost Analysis

It was assumed that the crystal growing operation employed five large-capacity crystal growers operating 24 hours per day, 7 days per week, 49 weeks per year. It was also assumed that the machine availability was 80% (i.e., that the total amount of material processed was 80% of the amount that could be processed if there were no machine down-time or other interruption of production) and that 80% of the crystal grown was within specifications. With these assumptions, five crystal growers would produce 23,000 kg of good 78 mm (3") diameter crystal per year. The detailed cost analysis of the crystal growing operation is shown in Table 4 and is representative of data supplied by Leybold-Heraeus[38] on one of the largest crystal furnaces available. The totals shown are the total manufacturing costs to which the cost of polycrystalline silicon must be added to obtain single crystal costs. Using the $35/kg poly crystal cost assumptions this results in a single crystal silicon cost of $62.03/kg for 3 inch diameter crystals.

To process this material into blanks, 18 slicers would be required. With a slicing yield of 95%, they would produce 5.6 million good slices per year from the 23,000 kg of crystal, operating 24 hours per day, 7 days per week, 49 weeks per year. The slicing cost analysis is summarized in Table 5.

On the same basis, the subsequent processing line must accept 681 slices per hour. Assuming 80% machine availability on the cell processing line, the line must process 851 slices per hour when operating. A design

TABLE 4

PRODUCTIVITY OF EKZ 1600/6000 CRYSTAL GROWING MACHINE FOR SILICON

	Maximum Pulling Length		1600 mm (62.9")	1600 mm (62.9")	
	Crystal Diameter	52.5 mm (2.06")		78 mm (3.07")	
	Orientation	1-1-1	1-0-0	1-1-1	1-0-0
	Cyl. crystal length mm	1400 (55.1")	1450 (57")	1350 (53")	1400 (55.1")
	Cyl. crystal weight Kg	7.100	7.4	15	15
	Remaining Si in crucible and tapered ends Kg	0.4	0.3	0.85	0.55
	Crucible charge Kg	7.5	7.7	16	16.3
	Theoretical yield	94.6	96.1	93.75	96.3
1.0	Charging time				
1.1	Loadming min	10		10	
1.2	Melting min	60		80	
1.3	Balance Temp. min	5		5	
1.4	Pulling time min	740		795	
1.5	Cooling time min	90		120	
1.6	Remove crystal min	15		15	
1.7	Cleaning after 5 charges (100 min total) min	20		20	
1.8	Total 1.1-1.7 min	940		1045	
1.9	Service and repair 4% of 1.8	40		40	
1.10	Total time/charge	980		1085	
	Pulling time is estimated at mm/min	1.9 mm/min		1.7 mm/min	

			52.5 mm (2.02") 1-1-1	78 mm (3.07")
2.0	Productivity/Year			
2.1	Available hours (49 wks x 7 days x 24 hrs)	hrs.	8,200	8,200
2.2	Theoretical no. of charges		500	450
2.3	Assumed 80% yield		400	360
2.4	Silicon requirement/yr	Kg.	3,000	5,760
2.5	Assumed 80% yield of cylinder crystal	Kg.	2,400	4,600
3.0	Power requirements and operational supplies			
3.1	Power consumption/charge			
3.11	Melting	KWh	50	80
3.12	Pulling	KWh	435	530
3.13	Total	KWh	485	610
3.2	Cooling water/charge	gal.	15,508	17,173
3.3	Argon/charge	$ft.^3$	98.9	106
3.4	Crucible diameter	mm	200	240
4.0	Productionccosts/year			
4.1	Direct labor, 1 man, 5 machines (20% of $9/hr. x 8200)		$14,760	$14,760
4.2	Power ($.03/KWh)		7,275	8,235
4.3	Argon ($0.10/ft3)		4,945	5,300
4.4	Quartz crucibles ($50 each)		25,000	27,500
4.5	Spare parts and wear parts		20,000	20,000
4.6	Total 4.1 - 4.5		$71,980	$75,795

4.7	Production costs/Kg mono crystal	$29.99	$16.48

These figures are only meant to be representative. Each user must adjust the above to suit their particular cost structure.

5.0	Fixed costs		
5.1	Machine price based on a purchase of 5 units	$170,000	$170,000
5.2	Transportation, installation (estimate)	15,000	15,000
5.3	Building costs - $\$40/ft^2$ 180 Ft^2 required	7,200	7,200
5.4	Investment 5.1 - 5.3	$192,200	$192,200
5.5	Crystal costs, depreciation - 5 years	38,440	38,440
5.6	Fixed costs/Kg crystal of 3.07" ϕ (pt. 5.5/2.5 = $/Kg)	8.35/Kg	8.35/Kg

6.0	Manufacturing costs/Kg Si		
6.1	Production costs/year	$ 29.99	$ 16.48
6.2	Fixed costs/year	8.35	8.35
6.3	Total costs/Kg Si	$ 38.34	$ 24.83
6.4	Allowance for silicon wasted	2.20	2.20
6.5	Total manuf. costs/Kg Si	$ 40.54	$ 27.03

Table 5

Cost Analysis -- Slicing and Etching
Projected 1977 Costs (revised)

Basis: Cost/kg of 3" diameter blanks
Final blank thickness 0.15 mm

Silicon Cost			
Kerf loss: 0.15 mm			
Etching loss: 0.05 mm			
Yield loss: 0.02 mm (95% slicing yield)			
Material utilization: 0.15/0.37 = 41%			
Cost of silicon consumed in process at $62.03/kg crystal cost			$ 90.97
Slices/kg product: 599			
Other Material			
Blades: $80/blade, 2000 slices/blade			23.96
Etchant: sodium hydroxide			4.10
Other chemicals and solvents			4.50
Labor			
Feed rate: $2\frac{1}{4}$"/minute, 40 slices/hour			
Machine hours/kg product: cutting—	14.98		
Machine set-up and adjustment	2.25		
	17.23		
Labor hours/kg product: slicing (1 operator per 5 machines)	3.45		
Etching	0.50		
	3.95	x $7.50/hr.	29.63
Totals			
Total conversion cost per kg of product			$153.16
Cost of silicon crystal in product			62.03
Value of product per kg			$215.19
Cost per completed blank			$ 0.36
Cost per square meter (2.86 m^2/kg)			$ 75.21

operating rate of 900 slices/hour has been used in the following discussion.

The cell processing operations are listed in Table 6. Steps 1, 2 and 8 are carried out using equipment of the type developed for automatic application of photoresist. A typical example is the GCA 6605/4122 automatic coater with mated bake oven. Using a 12 second spin cycle, which is adequate for the application of spin-on diffusants, the four tracks of this machine will process 900 slices per hour. Three machines would be required in a minimum-size facility, one for each of the three steps. The GCA 6605/4122 coater costs about $40,000 with programmable controller which can interface directly with a process control computer.

Steps 3 and 7 can most advantageously be performed in belt furnaces. The use of spin-on diffusants eliminates the need for careful control of furnace atmosphere during diffusion, and even the smallest belt furnace can process far more than 900 slices per hour if the slices are in wafer carriers, 25 wafers per carrier, and the wafers will then be transferred to mating quartz boats by dump transfer. Suitable belt furnaces are priced at from $5,000 to $15,000 depending on size and features.

At the exit end of the diffusion furnace, wafers would be dump-transferred from quartz boats to Teflon carriers, and step 4 would be carried out in a spin rinser-drier, 4 boats (100 wafers) per load. One machine would be required, costing about $2,500.

Steps 5 and 6 are performed using automatic screen printers with cartridge feed and automatic paste dispensers. Such machines are available from several manufacturers at a price of about $15,000. Since screen printing is generally done on square ceramic substrates, the cartridges and feed mechanisms used on presently available printers are not directly compatible with the wafer carriers used elsewhere in the processing. However, it appears that compatibility could be achieved with minor mechanical modifications. Each printer should be provided with a small oven to

Table 6

Baseline Process Operations

Starting material: Etched silicon blanks, 78 mm diameter, .0±5 mm thickness, resistivity and conductivity type optional.

1) Spin on P-type diffusant and bake.
2) Spin on N-type diffusant on other surface and bake.
3) Diffuse in belt furnace.
4) Remove diffusion oxides in HF, rinse and dry.
5) Screen print back contact and bake.
6) Screen print front contact and bake.
7) Fire contacts in belt furance.
8) Spin on AR coating and bake.
9) Cut to final size and shape.
10) Test and sort.
11) Interconnect into series strings.
12) Apply first layer of encapsulant to aluminum extrusion and lay down cell strings.
13) Apply second layer of encapsulant and cure.
14) Install end connection blocks and caps.
15) Final test.

dry the paste.

The screen printed contact is the first departure in this process from the conventional technology employed in space solar cells. The major advantage of the screen printing over vacuum evaporation is the extremely high throughput. Typical cycle times for screen printers are 2 to 4 seconds per print. Thus two machines costing about $30,000 with one operator per machine, are sufficient to handle the two screening operations at a rate of 900 wafers/hour. A vacuum process would require a bank of equipment costing an order of magnitude more, plus a much larger staff to handle not only the deposition itself but also the ancillary duties such as mask cleaning and maintenance. Screen printing is also more economical of contact metal since metal is deposited only where required. The major drawback to the screen printed contact is the higher contact resistance between the contact metal and the silicon. Adequately low contact resistance can be obtained for cells designed to operate at 100 mW/cm^2 illumination. If optical concentration is used, the screen printed contact may not be satisfactory at present. There are several possible ways of improving the contact resistance, so that further development should result in contacts which are satisfactory for moderate concentration factors.

The second departure from conventional processing is the use of a spin-on AR coating. The coating material is a solution of organometallic compounds which form a glass layer of the proper refractive index after firing. The coating thickness is controlled by the solution viscosity and the spin speed. The economic advantage of this process over vacuum deposition is not as large as for contacts, because the vacuum deposition of the AR coating does not require masks and the deposited layer is much thinner than the contact metallization. The drawback of the spin-on process is that precise control of thickness and refractive index is more difficult to achieve.

The spin-on AR coating has not been thoroughly evaluated; however, for purposes of cost analysis the total processing cost would be little affected by the substitution of a process involving vacuum evaporation, sputtering,

or chemical vapor deposition, provided the apparatus used could accept wafers in carriers at a steady throughput of 900 wafers/hour. In principle there appears to be no reason why equipment could not be built to carry out any of the above processes. Since such equipment would have to be custom designed and developed, we have assumed the spin-on process because the equipment cost is known.

Step 9 would require a simple modification to an existing dicing saw, such as the Tempress 602 ($12,000), to mount two blades on the mandrel, and to rotate the table 60° between cuts. However, it would be much less expensive to build a saw specifically for this operation, since most of the cost of the Tempress saw is accounted for in the step-and-repeat mechanism.

The remaining operations require specialized equipment which must be designed and built for the operations. In particular, handling mechanisms will be different than those used in cell processing if the cell is cut to a non-circular shape. Estimated costs (not including development) are given for the remaining equipment. Optical elements for concentration are not included in these estimates.

In summary Table 5 gives the cost of an etched blank ready for diffusion. Table 7 provides cost data for steps 1 through 10 of Table 6, giving the cost of a completed cell, tested and sorted. Table 8 provides cost data for steps 11 through 15 of Table 6, giving the manufacturing cost of a completed module. Table 9 summarizes the equipment and space requirements. Table 10 provides a summary of the costs for the entire process.

It is difficult to estimate just how much optimism is built into these figures. Perhaps the most questionable assumption is that consistant round-the-clock capacity operation could be achieved. While an adequate allowance for equipment maintenance has been provided (both scheduled and unscheduled) it is difficult to imagine economic conditions which would

Table 7

Cost Analysis -- Cell Fabrication
Projected 1977 Costs

Basis: Cost/year of operation of one production line, 900 cells/hr design capacity, 8232 hrs/yr operation.

		K$
Material		
Silicon slices, 78 x 0.15 mm 5,585,000/yr x $0.36/slice		2,006.5
Contact paste, diffusants and AR coating		194.1
Miscellaneous material		100.0
	Total Material	2,300.6
Labor		
20 operators x $7.50/hr x 8232 hours		1,234.8
	Total Cost	3,535.4

Acceptable cells: 5,585,000 starts/yr x 0.85 yield	4,747,250
Cost per acceptable cell	$0.745
Area produced: 4,747,250 cells x 39.5 cm^2/cell (hexagonal)	18,760 m^2/yr
Cost per square meter	$188.46
Output power at 1 kw/m^2 insolation, 25°C, 14% efficiency	2,626 kw
Cost per watt	$1.35

Table 8

Cost Analysis -- Module Fabrication
Projected 1977 Costs

Basis: Cost/year of operation of one production line, 900 cells/hr design capacity, 8232 hrs/yr operation.

		K$
Material		
Solar cells, hexagonal, 67.55 mm		3,535.4
Aluminum extrusion, assym. I-beam 11" wide 263,000 ft/yr x 1.576 lb/ft x $0.64/lb		265.3
Silicone encapsulant, .02" thickness over cell 74,832 lb/yr x $2.50/lb		187.1
Miscellaneous materials		150.0
	Total Material	4,137.8
Labor		
20 operators x $7.50/hr x 8232 hours		1,234.8
	Total Cost	5,372.6
Area produced: 18,760 m^2 cells x 0.95 yield x 1/0.85 packing factor:		20,967 m^2
Cost per square meter		$256.25
Output power at 1 kw/m^2 insolation, 25°C, 14% cell efficiency (11.9% array efficiency)		2495 kw
Cost per watt		$2.15

Table 9

Summary of Equipment and Space Requirements

Equipment

*5 crystal growers at $170K		$ 850K
18 slicers at $24K		432
1 etching station		25
3 coaters at $38K (with bake oven)		114
2 belt furnaces at $12K		24
2 screen printers at $15K (with dryers)		30
3 dicing saws at $12K		36
1 automatic cell tester/sorter		45
1 automatic interconnect soldering machine		90
1 vacuum encapsulation machine		15
Miscellaneous equipment		400
		$2061K
	Installation	309
		$2470K

Space

*Crystal growing	900 ft^2		
Slicing and etching	1500		
Cell fabrication	3000		
	5400 ft^2	at $40/$ft^2$	$ 216K
Module fabrication	3000 ft^2		
Office and laboratory	3000		
	6000 ft^2	at $30/$ft^2$	180
Storage:	10000 ft^2	at $20/$ft^2$	200
	21400 ft^2		$ 596K

*Costs associated with these items are already included in the crystal cost analysis.

Table 10

Cost Summary

Basis: Annual costs as estimated in previous tables.

	K$	%
Material		
Polycrystalline silicon ($35/kg)	997.3	19
Other materials	1,505.3	28
Direct Labor		
45 operators/shift at $3/hr	1,111.3	21
Overhead		
Indirect labor	670.0	12
Fringe benefits	356.3	7
Rent and facilities maintenance	85.8	2
Depreciation of equipment	494.0	9
Miscellaneous manufacturing overhead	152.6	3
	5,372.6	

provide a sufficiently high level of demand so that production cut-backs due to lack of orders were never encountered. Also, no allowance has been made for production shut-downs due to changes in product design. Costs would be substantially higher if the more probable assumptions of fluctuations in production rate and product mix were made. It should be borne in mind that a very large percentage of the costs are fixed costs, at least in the short run. This is true even for materials, since the continuous operation of such a plant would involve careful scheduling of deliveries from vendors to minimize inventory requirements, and these schedules could not be changed at a moment's notice. Nevertheless, since the assumption of steady continuous operation is always made in other cost analyses of this type, the same assumption is made here.

On the other hand, the direct labor costs are probably higher (by as much as a factor of two) than the minimum requirement. Because off-the-shelf equipment has been used in the estimates, each piece of equipment is assumed to be self-contained and transfer of product from one operation to other is assumed to be done manually. If such a production line were to be actually built today, it is clear that the expenditure of engineering effort to provide more integration of equipment would be worthwhile in reducing labor requirements.

Ultimate Cost Analysis

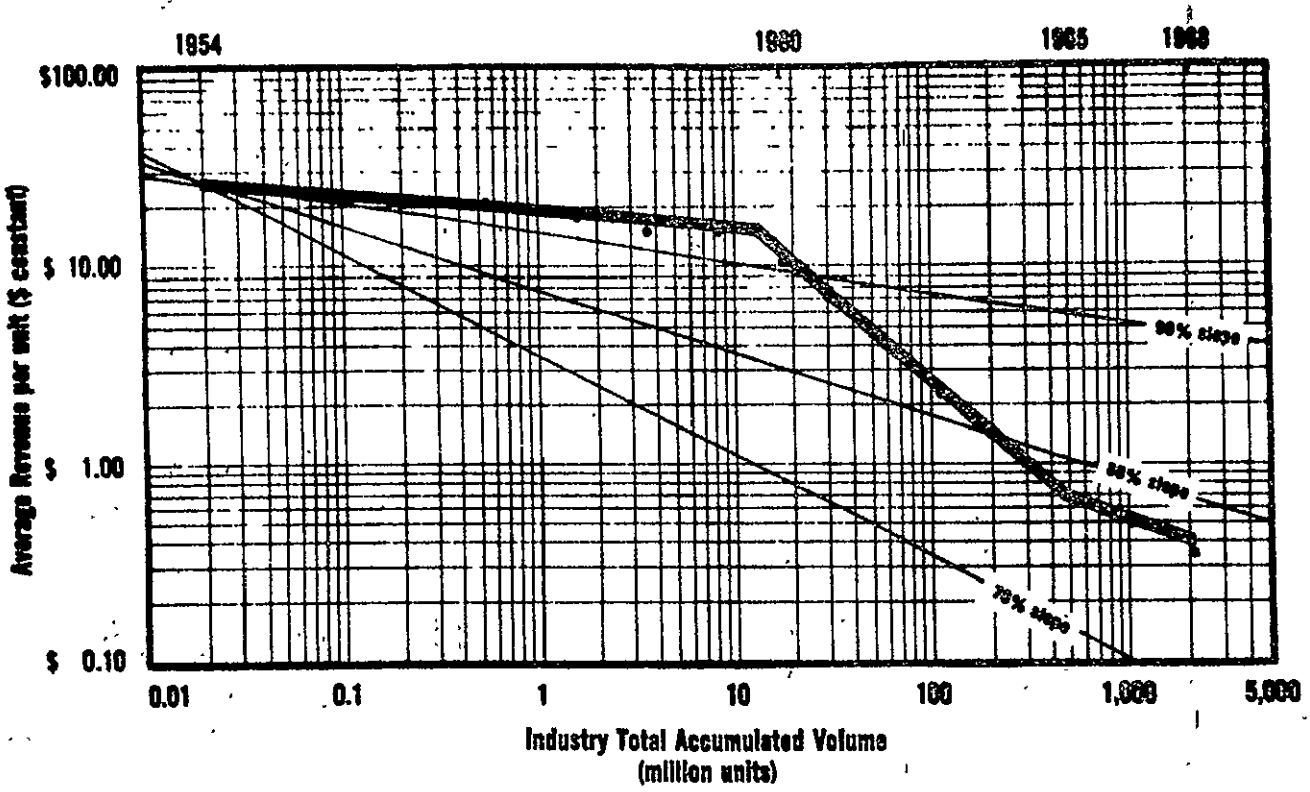
The cost estimates in the previous section are estimates of manufacturing cost. At least two other cost figures are of interest in assessing the competitive position of photovoltaic solar power systems. Selling price includes manufacturing costs plus engineering design and marketing costs, general and administrative expenses (including the costs of working capital), and profit. Installed cost includes selling price plus other costs incurred by the purchaser, such as system engineering, specification and procurement costs, transportation and erection of the system at the site, site acquisition and preparation expenses, etc. Installed cost is obviously the most meaningful cost parameter to use in comparing solar power to other power sources. However, it includes

many cost items which would differ considerably between different installations and which in any case are outside the scope of this study. Manufacturing cost is the best parameter to use in comparing array processes and design concepts and therefore is most appropriate for use in this study.

In previous sections, estimates of manufacturing costs for cells and modules have been generated. For the purpose of comparing solar power to other power sources, system costs are most meaningful. A solar power system consists of a number of modules making up the array, plus additional elements such as energy storage components, regulation and control electronics, and power conditioning and conversion equipment to match array output to the requirements of the load. Again, the estimation of system costs involve factors which are application-dependent and which are outside the scope of this study.

It is not uncommon in the literature to find estimated manufacturing costs for solar cells being used for comparison purposes as if they were equivalent to installed costs for photovoltaic solar power systems, or to encounter cost estimates which are not sufficiently well defined to be placed in the appropriate category. This presents some problems in comparing the cost estimates developed during this project with others in the literature.

In order to project the behavior of costs over time, the "experience curve" concept developed by the Boston Consulting Group will be used. This projection shows that if unit cost (in constant dollars) is plotted against total accumulated unit volume (both variables on logarithmic scales) regular curves result which can be interpreted in terms of the economic environment of the industry and from which conclusions can be drawn as to the optimum business strategy for a producer. Examples of these plots are given in Figure 5. A straight line on these plots implies a constant fractional change in cost or price for a given factor of increase in total accumulated volume. The straight lines marked "90% slope", "80% slope", and "70% slope" refer to price decreases of 10%, 20% and 30% for each doubling of accumulated volume.



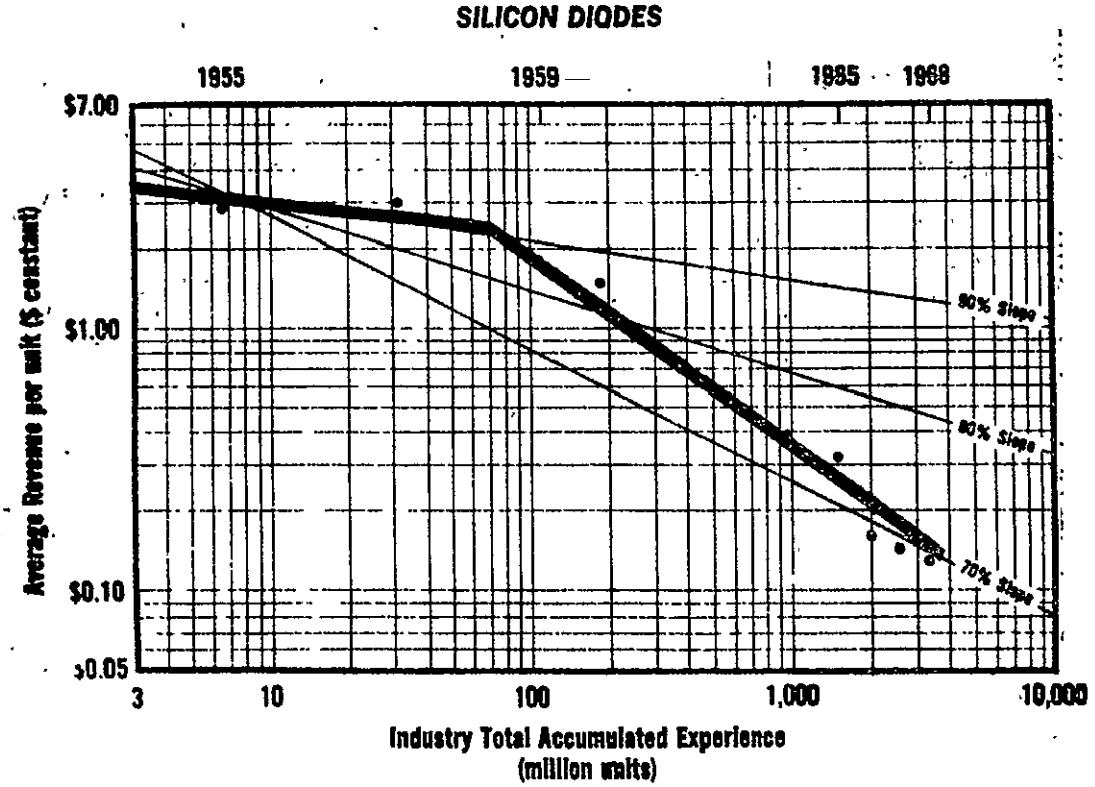


Figure 5 . - Experience Projections

For most industries, price/volume plots display a slope between 90% and 70%, with a 90% slope characteristic of mature industries (and also of the start-up phase of new products or industries) and a 70% slope characteristic of periods of rapid technological change and market expansion within an industry.

If the production rate increases exponentially with time, the ratio of the total cumulative volume produced at the end of a given year to the production during that year will be a constant. For a production rate which doubles every two years the constant factor is 3.4. Also, it would be unrealistic to assume that the single production line analyzed in the preceding section would account for a major fraction of industry production. If an assumption is made that it accounts for one-third of total industry production at the time the estimated costs are realized, the industry production rate at that point would be about 60,000 m^2/year and the accumulated production 200,000 m^2.

In Figure 6 we have plotted the blank, cell and array cost figures on a plot of silicon solar cell cost projections taken from the Satellite Solar Power Station Feasibility Study (NASA CR-2357). The points for the blank and cell are connected to the 1971 points for a 2" diameter wafer and cell. It can be seen that the connecting lines have a 70% slope. While this doen't prove anything, it is consistent with the experience of other industries under similar conditions and therefore tends to support the reasonableness of the cost estimates previously derived.

Also shown on Figure 6 are lines extrapolating costs to a total cumulative production volume of 20 million square meters. The line for the blank cost is drawn with a slope of 90%, and this results in a prediction of a factor of 2 decrease in cost for a factor of 100 increase in accumulated volume, to about \$37/m^2. The point labeled "Cost Projection for EFG Ribbon-Grown Solar Cell" is plotted at \$25/m^2, the cost estimates for EFG ribbon adopted in NASA CR-2357. The Phase II cost estimate by Tyco, is \$8.75/m^2. As indicated, the Tyco estimate appears to be too low but the NASA CR-2357 estimate appears reasonable.

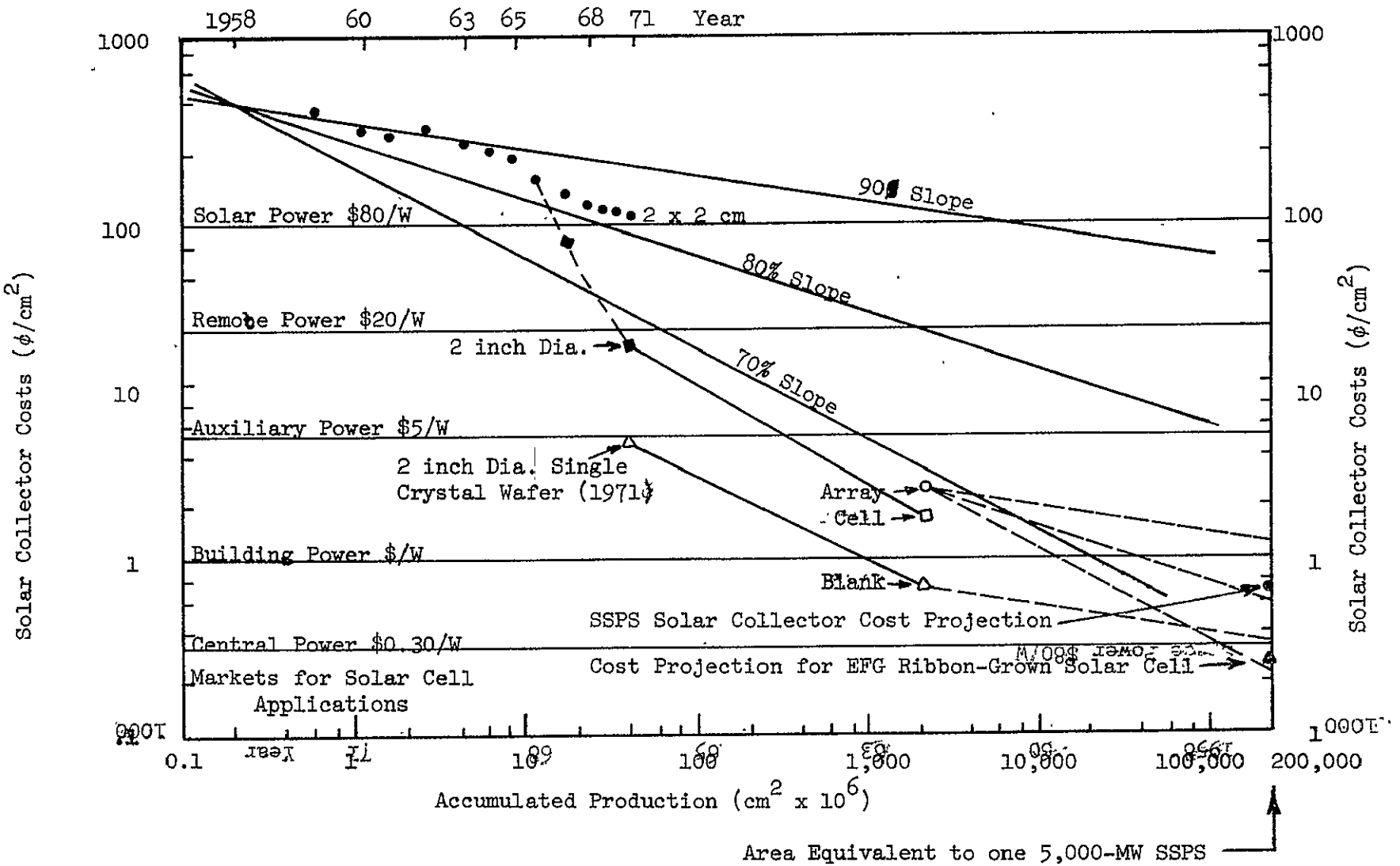


FIGURE 6. SILICON SOLAR CELL COST PROJECTIONS

From the point representing the array cost estimate derived in this report, lines with slopes of 90%, 80% and 70% are drawn. A 90% slope for the blank cost was considered reasonable on the assumption that the blank fabrication processes are already highly mechanized and rapid cost reduction is not likely without substantial technological change. On the other hand, the level of mechanization described in the preceding section for cell and array fabrication is clearly only a first step, and the cost elements associated with direct labor and structural materials could clearly be reduced considerably by greater mechanization and more thorough design. A 70% slope is obviously impossible since the array cost would then be less than the blank cost, but 80% is not unreasonable and would result in an array cost slightly lower than the SSPS Solar Collector Cost Projection of $\$68/m^2$. This would imply that the additional costs of cell and array fabrication could be reduced from the level of about $\$180/m^2$ estimated in the previous section to about $\$30/m^2$, or a factor of 6. While this is clearly a challenging task, it should be borne in mind that the 100-fold volume increase itself would be expected to provide a cost reduction of a factor of 2 (90% slope).

Prospects for achieving these cost reductions will be discussed in the next section of this report. The remaining portion of this section will attempt to forecast the time at which these costs and production volumes will be reached.

Industrial Growth Forecast

For purposes of analysis it was assumed that we would start by building a plant with a production level of 1.5 MW/yr in 1978, then double production capacity every two years thereafter. The 1978 level was the most optimistic forecast which could be justified based on marketing studies. It corresponds to almost 100% saturation of the remote power market which is presently the only commercial application for photovoltaic terrestrial systems. A doubling time of 2 years was the most optimistic forecast we could justify based on studies of production increases in other industries.

The industrial growth forecast was thus based to a great extent on considerations of demand, rather than on the production factors. It has been apparent that the

doubling of demand every two years would require a massive and continuing effort to develop new applications and markets for photovoltaic systems, and that government assistance in this effort would be even more critical than in technology. No attempt has been made to define the specific approaches to this problem which should be considered by the government. Historically it is apparent that much less attention has been paid to stimulating demand than to improving technology, although the results of this study appear to us to make a strong case for the position that, because of inadequate demand, industry is presently unable to take advantage of existing low-cost production technology to make immediate cost reductions.

If production rate was limited only by technological considerations, a production level of about 60,000 m^2/year (about 7 MW/year at the array level) could be reached by 1977, as estimated in the preceding section, and thereafter production could be doubled each year to reach 6 million m^2/year (700 MW/year) in 6.5 years.

Figure 7 shows several production rate estimates. Line "A" is the working estimate, with a 2-year doubling time. Line "B", with a 5-year doubling time, is a reasonable estimate of the rate at which demand might be expected to increase without governmental stimulation, based on the experience of similar industries. Line "C", with a 1-year doubling time, represents our estimate of the maximum rate at which production could increase if limited only by technological factors. Finally, line "D" is the production rate forecasted by the National Science Foundation (H. R. Blieden: A National Plan for Photovoltaic Conversion of Solar Energy; Proc. Workshop on Photovoltaic Conversion of Solar Energy for Terrestrial Applications (Cherry Hill, 1973); NSF-RA-N-74-013). The approximate doubling times for line "D" are 20 weeks up to 1000 MW/year increasing to 5 years beyond 5000 MW/year.

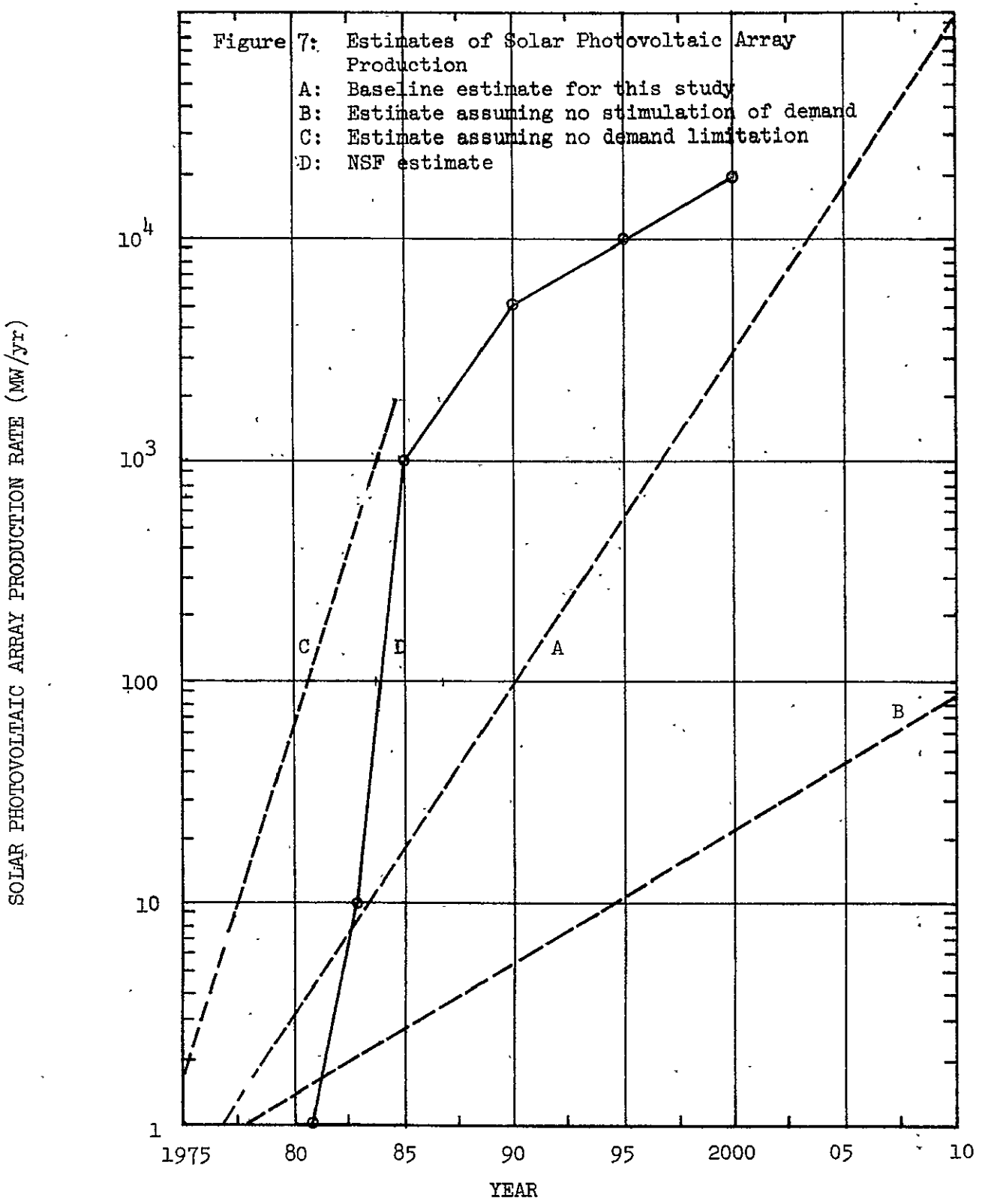


Figure 7: Estimates of Solar Photovoltaic Array Production
A: Baseline estimate for this study
B: Estimate assuming no stimulation of demand
C: Estimate assuming no demand limitation
D: NSF estimate
SOLAR PHOTOVOLTAIC ARRAY PRODUCTION RATE (MW/yr)
10^4
10^3
100
10
1
1975
80
85
90
95
2000
05
10
YEAR
A
B
C
D

V. CONCLUSIONS

Manufacturing costs of solar photovoltaic arrays, without optical concentration, can be reduced to approximately $\$250/m^2$ through the utilization of existing mass production equipment and processes. The only critical requirement is the growth of demand to the point at which mass production is economically feasible. During this period, engineering effort will need to be expended to plan, construct and debug the production lines. This effort is essentially of a production engineering rather than an R & D nature, and can most effectively be carried out in a pilot line operation.

To reduce manufacturing costs to $\$70/m^2$ and \$0.50/watt, the major technical problems to be addressed are lowering the blank cost by at least a factor of 2, to the level of \$25 to $\$35/m^2$, and lowering the cell and array fabrication costs by a factor of 4 to 6. Again, these objectives require a major expansion of production volume as well as technological development.

There are at least four options which appear to be capable of reducing blank cost by the required amount:

1) Ribbon growth of silicon crystal
2) Inexpensive silicon poly from silane
3) New slicing technology
4) Optical concentration

Research on ribbon growth is being supported by ERDA and NASA, concentrating on the EFG process and the web-dendritic process. In order to provide the required cost, improvements are needed in all of the following areas:

a) crystal structural perfection and lifetime must be improved to closely approach present crystal growing techniques;
b) ribbon width should be increased and thickness reduced, and dimensional control greatly improved;
c) means for continuously replenishing the melt should be developed;

d) growth techniques should be developed for growth of multiple ribbons;

e) all of the above developments should be incorporated into the design of reliable equipment, suitable for production-line operation.

Very inexpensive poly, of the order of $6/kg, could provide the required cost reduction without major changes in the crystal growth or slicing processes. The approach utilizing silane is preferred because:

a) silane pyrolysis to silicon will consume much less electrical power than the present process, reducing the payback period from years to months;

b) it is likely that good quality hexagonal single crystal material can be deposited directly from silane in the poly reactor at a small additional cost, eliminating the crystal growing step and reducing the loss of silicon incurred in shaping cells to produce high packing factor;

c) silane is inherently more suitable for the production of thin films because deposition occurs at much lower temperatures and reaction products are non-corrosive to substrate materials.

A slicing process which substantially eliminated the loss of silicon in the cutting and etching steps would also provide the required cost reduction independently of other technological improvements. A non-abrasive cutting process is required to prevent the introduction of damage which must be etched away. No potentially suitable process was uncovered in this study, but some form of electrochemical machining, possibly using very thin wires as electrodes, might be feasible.

Optical concentration reduces the effective blank cost per watt by increasing output per cell at the expense of increased array cost. Based on current research results, it appears that concentration factors (including optical losses) of about 4 in non-tracking collectors and about 15 in tracking collectors, are feasible with low-cost optical

elements. These concentration factors appear to be compatible with low-cost cell designs and processes. While the use of concentration does involve some additional constraints on array location and increases the cost of the array fabrication steps, it is felt that the array target cost of $0.50/watt is well within reach, independent of other technological advances.

In addition to these four options, thin film polycrystalline cells could provide costs much lower than $0.50/watt. The technical problems which must be solved in order to accomplish this are very basic in nature, and it is difficult to evaluate this option on a basis comparable to the other four options.

Considering the four listed options, it would appear that at least one can be confidently expected to be developed within the next five years. In particular, optical concentration involves only the solution of engineering design problems, without the need for any research effort to remove underlying technical limitations, and ribbon crystal growth and inexpensive poly from silane appear to be not very far from reality.

Reduction of cell and array fabrication costs require mainly increased mechanization of fabrication operations and material cost reduction. Mechanization, as before, can be expected to occur as a result of increased production volume. Material cost reduction is largely a matter of design refinement involving minimization of the amount of structural and protective materials used, and substitution of lower-cost materials. The major technical need is for more information relevant to reliability of arrays in various terrestrial environments, since manufacturing cost reductions cannot be obtained at the expense of service life if solar photovoltaic power generation is to be economically advantageous.

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APPENDIX I

APPENDIX I

THE ELECTROCHEMICAL PRODUCTION OF HYDRIDES IN MOLTEN SALTS

Dr. W. Sundermeyer *
Organic Chemistry Institute of the
University of Goettingen

and

Dr. L. M. Litz
Union Carbide Corporation
Research Laboratory, Parma, Ohio

ABSTRACT

The development of an electrochemical process for hydrogenation of halogen compounds of boron, silicon, germanium and phosphorus is described. The production of hydrogen compounds is possible with this process. An experimental facility for the manufacture of silane was built, which could produce sufficient inexpensive silicon to meet the requirements of the entire U. S. A. for pure silicon (for transistors, etc.).

Possibilities and problems of applied electrochemistry have been thoroughly discussed in this journal recently, in which reactions in aqueous or organic solutions have been emphasized.[1] Following the historical development still further, one sees on the other hand, that the production of molten salts is still considered as electrometallurgy even though considerable contributions have been made toward a general utilization of molten salts as a reaction medium.[2] The specific advantage of the application of ionic liquids lies in the fact that one could use the electrochemical or metallurgical process as a step in a continuous or semi-continuous recycling process, usually to reestablish the initial state again. An especially typical example occurs here in Germany in which a well established process for the hydrogenation of halogen compounds

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* Presented to the GDCH-Technical Group (Applied Electrochemistry, Oct. 22 & 23, 1964 in Ludwigshofen/Rh)

of groups III, IV and V of the Periodic Table[3] operates. The process was further expanded in the U.S.A. for the manufacture of silane.

With the increasing need for pure silicon for semiconductor devices, an inexpensive process for the production of silane (SiH_4) seemed desirable, since as is well known, it can be thermally decomposed to very pure silicon. Older methods, especially the use of silicides and acids in aqueous or non-aqueous systems (liquid ammonia/ammonium bromide) or the hydrogenation of silicon tetrachloride with the well known but very complex hydrides of boron and aluminum (boronates, alanates), although still very useful for laboratory use, are not practical for commercial synthesis. No solvent of the usual sort could be found for the well-ordered salt-like hydride of alkali and alkali earth metals. A big step forward was a process[4] in which silicon tetrachloride or other halogen compounds were converted in a suspension of sodium hydride in mineral oil at an elevated temperature; aluminum must be present as an "activator" (or catalyst).

A steady new formation of complex compounds between these activators and the sodium hydride, and their solubility in the above solvents allows a smooth running reaction.

Reduction of $SiCl_4$ in a Melt

Even though there are no conventional solvents for salt-like hydrides, they do dissolve well in molten salts, e. g., in a lithium chloride/potassium chloride melt (at 400°C), and are then able to undergo the desired reaction. If silicon or boron halogenides are passed through the above solution, then immediately the halogenide is exchanged for hydrogen.

$$4\ LiH + Si\ Cl_4 \rightarrow SiH_4 + 4\ LiCl \quad (1)$$

If simultaneously one sets into action the usual fusion electrolysis with a hydrogen-bathed cathode, there will be formed new alkalihydrides continuously over the precipitated alkalimetal (Li). This corresponds to the initial state, without changing the salt melt or producing useless by-products.

$$4\ LiCl \rightarrow 4\ Li + 2\ Cl_2 \quad (2)$$

$$4\ Li + 2\ H_2 \rightarrow 4\ LiH \quad (3)$$

the results of the balanced reaction is

$$Si\ Cl_4 + 2\ H_2 \rightarrow Si\ H_4 + 2Cl_2 \quad (4)$$

or if one uses the chlorine made directly again to produce silicon tetrachloride,

$$Si + 2\ Cl_2 \rightarrow Si\ Cl_4 \quad (5)$$

For the elements boron, germanium and phosphorus the same formulas can be used.

Methods for the Technical Realization of This Reaction

There have already been reports concerning the choice of melts and the different possible end-products, and also concerning the reaction results[3,5]. In the following, the specific requirements which the apparatus must fulfill to have the desired reaction, or rather how to overcome the significant corrosion problem, shall be discussed. The presence of hydride ions seems to be a prerequisite for the process, but under no circumstances should the hydrogenated halogen, e.g., silicon tetrachloride, be allowed contact with the alkalimetal in the cathode area, for

elemental silicon instead of silane would be formed. Both the free lithium and the alkali-hydride show a strong corrosive action toward all ceramic materials and graphite. A reaction chamber made of carbon-free steel (and under certain circumstances protected by a layer of solidified melt) is the most suitable because in the usual electrolysis cell an isolation problem exists.

Both possibilities, the semi- and completely continuous process were demonstrated by a simple set-up, on which all subsequent systems were based.[3]

If for instance one electrolyzes a lithium chloride/potassium chloride melt at 400°C in a simple U-tube (Fig. 1) and the cathode and anode area are separated either through mechanical means or by "freezing" the melt, in the lower area, then the lithium is completely reacted with hydrogen to lithium hydride, and if one then injects silicon tetrachloride a semi-continuous process results which can be recycled by opening the closure.

In a larger cell, which has the advantage of a closer electrode spacing, one uses a double wall spacer, whose holes can be shielded by misalignment.[6] By doing this one can shield the anode area with its unstable graphite anode against the lithium hydride. Only after more recent experiments was it possible, by incorporation of a tungsten anode, to use again the simple principle of the U-tube in a semi-continuous process, without the necessity of the periodic separation of the electrode areas.

Continuous Operation Technique

Naturally the continuous process is the most interesting. It can be demonstrated in a double U-tube[3] (see Figure 2). Between the two sections of the anode and cathode area, there is a third reaction zone, into which the silicon tetrachloride vapor, possibly with hydrogen as a carrier

gas, is injected. During the electrolysis, hydrogen is fed into the cathode area which is heated to 150-200°C higher than the rest of the apparatus. By this means the formation of lithium hydride is greatly enhanced. By convection, the agitation produced by the injected gases, and the rapid transport in the electric field toward the anode, the hydride ions end up in the middle reaction zone, where they react with the silicon-tetrachloride to produce silane. For this process too, cylindrically symmetric cells with cylindrical separators were developed. A further interesting variation is that, instead of the previously used graphite anode material, coarse silicon or boron granules are loosely packed in contact with a graphite conductor, which react directly with the anodically formed chlorine to form the halogenides ($SiCl_4$, BCl_3),[9]. This cell allows the formation of silane.[10] However, contact of the rising concentration of silicon tetrachloride with free lithium metal, which reacts slowly to hydride at the operating temperature off 350°C, is unavoidable, since the hydrogen-bathed cathode is directly connected to the anode delivering silicon tetrachloride. The electrolytic efficiency is also greatly decreased from the free chlorine which may be formed. The free chlorine oxidizer attacks the silicon and causes it to precipitat throughout the melt, and increases the resistance of the cell. Then the silicon granules fise to the surface and produce a unique surface appearance.

The anodically introduced boron or silicon must naturally be very pure to avoid contamination of the melting bath and the disassociation of metals other than lithium (e.g. iron out of ferro-silicon).

The automatic dissolving anode leads to a further simplification of the apparatus, shown in Fig. 2, which resembles the simple U-tube. In one leg of the tube the silicon anode forms silicon tetrachloride at 400°C while at the same time in the second leg a hydrogen-bathed iron cathode at 600°C produces lithium hydride[11] (see Fig. 3). The hydride ions arrive in the anode area by means of the stirring effect of hydrogen but especially through the convection of the melt between the two legs which are at different temperatures. In order that the hydride ions do not get to the anode itself, where there would be a discharge, the connecting piece between the two legs is set at an angle to the top of the anode area. By this means the transport by convection is improved, as well as guranteeing that the hydride ions will only come in contact with the rising silicon tetrachloride. The most unsatisfactory feature of this cell is the electrode spacing.

An essential principal step to a continuous process for commercial use is represented by the apparatus depicted in Fig. 4. In a cell, fitted with a diaphragm or baffle with a silicon granular anode and an iron cathode, lithium and silicon tetrachloride are produced. Since the rising lithium is caught immediately in a steel funnel, the whole cell can be made of a ceramic material. i.e. an insulating mass. The lithium rises to a reaction chamber, heated to 600°C, which is over the cathode area, where it converts to a hydride with injected hydrogen. By convection, the hydride solution arrives, as described in Figure 3, at a second part of the apparatus above the anode area in which the anodally produced silicon tetrachloride rises and is converted to silane.

This reactor, because of the decomposability of the end product,

runs at 400°C. Because of this, a strong convection current for the transport of the hydride in the upper chamber occurs in the melt via a second connecting tube to the first reaction chamber. Only the gradual depletion of the lithium chloride in the electrolysis cells and the precipitation of potassium chloride associated therewith is disadvantageous, since the necessary convection of the melt which is rich in lithium chloride by virtue of the reaction, (Eq.1), is not easily achieved.

Technical Experimental Installation

All the variations of the process described up until now finally led to a mature "pilot plant" which has worked for years, trouble-free (Fig. 5) with over a 90% reaction and a significant yield and delivers very pure silane. Unlike the first-mentioned process in mineral oil, this process is free of boron, aluminum and carbon contamination.** No self-dissolving silicon anode is used because of the aforementioned disadvantage, but instead the silicon tetrachloride is produced externally to the electrolytic cell using the chlorine recovered. Simultaneously a more compact construction method which has a smaller electrode spacing is achieved, in which the container wall serves as cathode. A bell jar gathers the rising lithium which, because of its low specific gravity flows on its own to the hydride producer.

**The present plant could fill the complete demand for silicon in the entire U.S.A. The crystallized product with a specific resistance of at least 1000 ohm-cm can be produced at a third of the price of similar material made by the trichlorosilane process.

Lithium hydride is again formed here at 600°C, which arrives in the already-mentioned fashion, by convection into the actual reactor (400°C). The descending lithium chloride-rich melt returns to the hydride producer and in part from there to the electrocell.

Once again the return to the electrolysis area would not be sufficient, if artificial circulation were used without the use of a pump or the equivalent. For this reason, a gas is introduced into a vertical portion of one of the connecting tubes of the reactors and the cell. The rising gas bubbles push (if the outer tube is close enough to the inner tube) the liquid up before it and pulls the potassium chloride-rich melt out of the cell, and thereby the lithium chloride-rich melt is brought into the cell via a second connecting tube.

As easily seen in Fig. 5, silicon tetrachloride (which has to be introduced anyway) is appropriately used as the carrier gas, so that the silane produced is not mixed with foreign gas which would make the condensation more difficult.

In order to give satisfactory results the apparatus must be of a size which would allow 6-10 kilograms of lithium to be electrolyzed and further processed in a period of 8 hrs.

In addition, a sufficient convection of the melt is possible in the diagonal pipe only if it has an ample cross-sectional area. Return to the principle of the separation of the three reaction components, initially introduced in the three-pipe apparatus (instead of use of a single reaction chamber[3,5]) permits the process to proceed simply and without reagent starvation. An unexpected advantage is that the plant can be turned off at any time and after it has been reheated can again be turned on.

The Laboratory Process

In closing, a process should be mentioned, which is an interesting variation that allows working on a smaller scale and yet returns one to a semi-continuous process and the continuous production of silane. The lithium is electrolyzed in a double cell, Fig. 6, and then transferred to a similar double cell which serves as a hydride-producing reaction unit. If the lithium chloride is sufficiently depleted in the electrolytic double cell calcium chloride precipitates at the operating temperature, and if a large lithium chloride excess exists in the second double cell, by virtue of the reactions of Eqs. (3) and (1), then the electrolysis will be performed in the latter and the lithium will be introduced into the first double cell and there turned to hydride and reacted with silicon tetrachloride. Since the chamber used at any particular time as the hydride producer is heated to 600°C at the surface of the melt and only to 500-550°C, at the bottom, there is sufficient convection within each double cell for the transport of the lithium-rich melt. The transport of the lithium or potassium chloride is completely avoided here, since the relatively simple alternating transport of the separating lithium metal takes place. Such a set-up could find use even on a laboratory scale foresubstantial requirement of hydrogenated products.

Use of Silanes

Silane has the following advantages as a compound for the production of transistor silicon, as compared with the presently widely-used technique of converting trichlorosilane, $SiHCl_3$: the silane obtained by this new process which is already very pure, may be further purified more easily than trichlorosilane by a simple absorption process.

The boron content is extraordinarily low, so therefore a product with a greater than 500 ohm-cm specific resistance can be directly produced. The energy costs for heating the silicon rods on which the pure metal is separated are considerably lower than in the trichlorosilane process because of the low decomposition temperature of the silane. Finally the yield of silicon metal, referring to the silicon present in the trichlorosilane, is limited by the restriction of chemical balance to 20%, and there is no use for the silicon tetrachloride which is produced at the same time. A similar limitation is not present with silane, so that more than a 96% silicon separation can be attained by the thermal decomposition.

In closing reference should be made to the production of the technically interesting chlorosilane and hydrogen-containing organosilanes through co-proportioning with silane as the final product.

Submitted Sept. 28, 1964 (B1838)

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6. Compare Fig. 2 reference #3. Because of the very complicated built-in metal parts inside of the melt this finds no technical application.
7. The reaction of the lithium with hydrogen is slow at temperatures lower than 450°C.

8. Compare Fig. 4 & 5 of reference 3

9. E. Enk & J. Nicki, DAS 1092 890 (July 7, 1959; Nov. 17, 1960)

10. Data on test duration, depletion, transformation were not revealed.

11. L. M. Litz & S. A. Ring, U.S. patent April 27, 1961; French patent 1 323 193 (April 25, 1962 and Feb. 25, 1963)

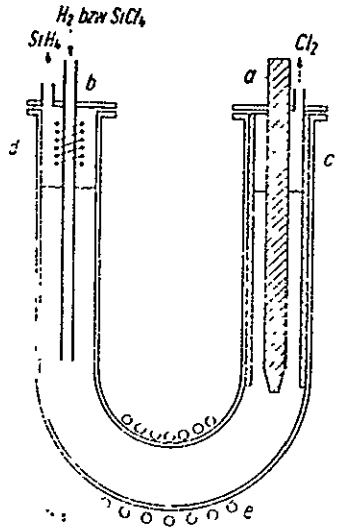

Fig. 1 Simple U-Tube apparatus for producing silane a. anode b. cathode c. ceramic d. additional heating e. cooling coil.

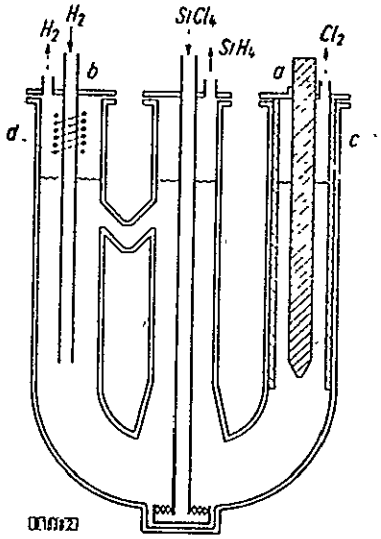

Fig. 2 Double-U-tube for a continuous process (designation same as in Fig. 1.)

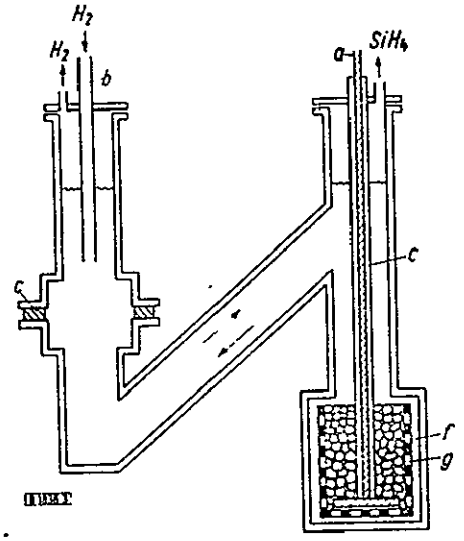

Fig. 3 Continuous process with self-dissolving anode (designations same as Fig. 1 f. silicon granules g. diaphragm.)

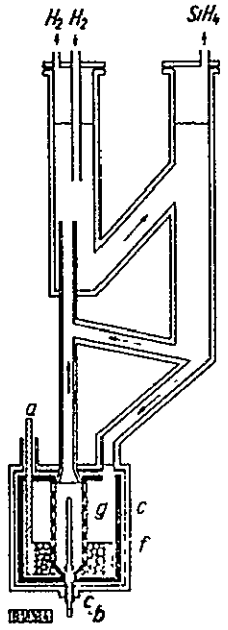

Fig. 4 Continuous process with self-dissolving anode with narrower electrode spacing (designation same as Fig. 1 & 3)

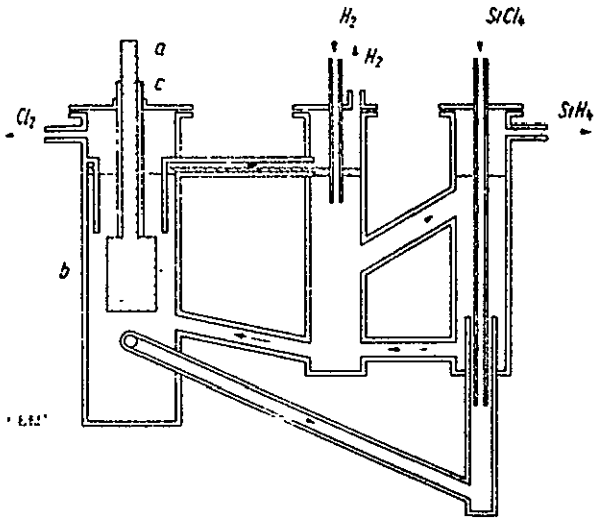

Fig. 5 Technical experimental plant. (designation same as Fig. 1)

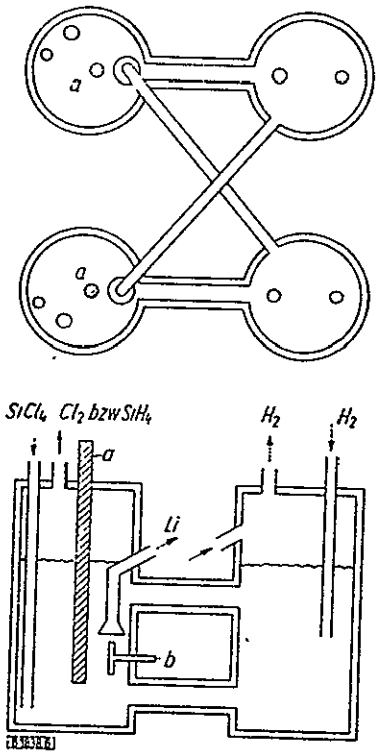

Fig. 6 Laboratory system (Top view & side view) (designation same as Fig. 1)

APPENDIX II

Touchless Wafer Handling

Donald P. Baumann
GCA Industrial Modular Systems
Santa Clara, California

Semiconductor wafer processing is discussed with emphasis on wafer handling methods. it is suggested that the increasing high damage rate (and its critical cost) due to "man-handling" of wafers can be reversed by moving them on a linear dynamic air bearing. This appears to be the next step after flip-transferrable carriers. The technique has been applied successfully to at least half a dozen common processing operations by both large and small manufacturers. The system is discussed in detail including comparisons and compatibility with other handling methods, costs, conversion from hand processing, and impact on the industry.

IN MANUFACTURING SEMICONDUCTORS the most insecure and unpredictable element has been warer processing. Wafers moving through the production process travel from tweezer-tips to finger-tips, back and forth from station to station. They are moved and manipulated one at a time by various personnel, who may drop, break, scratch, chip or otherwise damage as many as not. Damage and breakage rates, speed of production, and wafer uniformity (all still in primitive stages in many plants) are major cost considerations throughout the industry. These costs become more critical as the sophistication of electronic units expands. The dramatic increase in complexity is seen in comparing a small signal transistor to an LSI computer module.

Of course, every manufacturer in the semiconductor industry wants to produce a better, more reliable product in the shortest time and at the lowest cost. Time goals would seem to point to some kind of batch processing, but significantly reducing costs complicates the picture. Deciding how to approach the task requires careful analysis.

Quality *Is* Quantity

The term "yield" is bandied about in discussions of how to make semiconductors more efficiently, and therefore merits some discussion. Consider transistors approximately 10 mils by 15 mils square, with 15,000 to 30,000 per wafer. If the *yield per wafer* is sufficient, whether it costs $10 or $20 to process one wafer matters little. What matters is whether you get 10,000 or 15,000 *good* dies on the wafer. In this situation wafer *quality* is measured by die *quantity*. And with that many dice on one wafer, you really are batch processing; the batch is on each wafer, not in groups of wafers processed in different labs. These transistors are small signal transistors, which represent about 80% of the market. Here the cost of getting a single die through wafer processing is negligible compared to costs of packaging, wire bonding, testing, etc. after wafer processing (see Table 1).

The next rung in the complexity ladder is the basic integrated circuit (IC) In this case the average wafer has a maximum of only 1000 to 1500 dice. Also, there are more steps in the processing, such as isolation diffusion, an extra layer of metal, or passivation layer (mostly in the photo-resist area). A finished wafer costs $15 to $30, still not much compared to the cost of the remaining processing operations. For example, packaging alone for one die runs 25¢-$2.00, while the wafer processing cost for that die is about 2-3¢ (see Table I).

The cost picture is quite different with a more sophisticated unit, such as a beam-lead CMOS memory. There may be 25 or more major wafer processing steps (e.g., 9 or 10 masking steps); dice are ¼" by ¼", and the yield is usually 10-20 per wafer. Here the individual wafer cost is $50 to $150. Now the processing cost per die is in the same ballpark as that of packaging and other operations.

Even if a company is just in transistors, automation in today's market is becoming a matter of survival. The number of devices sold each year has tripled in the past five or six years, while the market's gross sales have remained unchanged or declined somewhat So, a unit that used to sell for $1.00 now costs about 30 cents.

If IC's are the product, the point appears moot. It

Table I—Cost Analysis

	Dice/Wafer	Process Cost/Wafer	Yield/Wafer	Process Cost/Die
Small Signal Transistors	15-30,000	$10-20	10-15,000	≈ 0.1¢
Average IC	1000-1500	$15-30	500-800	≈ 3.0¢
Beam-Lead CMOS (LSI)	15-25	$50-150	10-20	≈ $10

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is worth studying, as mentioned, costs of packaging and testing can be considerable. An MOS device, for example, that requires special testing, may call for an additional half million dollars in equipment. When such testing is required, it is often due to minor imperfections caused by *unreliable wafer handling*. A company that is selling to the military as well as to the commercial market can have a significant sorting problem when trying to meet stringent specifications.

Testing and sorting are interdependent. The devices are sorted into quality categories through a succession of *decreasingly* difficult tests (see Table II). The culls from the more severe tests can only be used in unsophisticated equipment like pocket transistor radios. Here, a reliable automatic handling system can reduce the need for testing and sorting, because 90% of the devices on such carefully handled wafers usually pass the first test.

If one gets into MSI, LSI, and beyond, the choice is obvious. He must be concerned with wafer processing costs first. Here, management thinks early about mechanization and automation.

50% Damage and "Nobody Wanted to Admit it"

With wafer processing under scrutiny, where should the money be spent? Should it go into wafer handling, process control, reducing materials costs, or eliminating labor? In a recent presentation, Mike Clayton, Manager of Process Engineering at Motorola's Semiconductor Products Division, said, "Wafer handling is usually the major factor because half the wafers that started in a manual processing system didn't reach the end. (This is why Motorola made the move toward automation more than four years ago) I mean there was about 50% damage, although nobody wanted to admit it."

It becomes a very vicious cycle; once a lot of money has been invested in these wafers, and half the work is in broken pieces, the manufacturer cannot afford to discard the pieces. So he processes them and; thereby, is locked into a manual handling system because most mechanized equipment and systems won't handle broken pieces. In other words, if automation is to be achieved, the breakage must be largely eliminated or the system must handle broken pieces. Consequently, many companies have been afraid to automate handling.

Stop "Man-Handling"

Most of the numerous approaches to this dilemma tried to reduce man/wafer contact. Primarily, such solutions placed an intermediary tool or surface mechanically between human hands and wafers. Thus the first "carrier" (a vertically slotted holder) replaced the tray, where wafers lie flat and exposed to impurities and damage.

A few work stations were mechanized with new apparatus. Mechanically they run the gamut from steel wires and conveyor belts to rubber bands, but their uses are limited and most are bulky; but, more important, they use trays or other means of transport that are incompatible with carriers. In addition wafer loading/unloading, a primary scene of damage, is a critical factor.

Table II—Testing and Sorting
(100 MOS devices/wafer)

	Number of Devices Passing Test	
	Manually Handled Wafers	Air Transported Wafers
1 Stringent Test	10	90
2 Medium Test	10	10
3. Minimal Test	30	—

Flip-transferrable carriers made possible the first step in taking wafers from manual handling (see Fig. 1). Wafers can move from one station to the next without manual contact, because the wafers slide from one carrier directly into another.

A new development programs wafers to move in and out of carriers without touching *any* surface enroute. Carefully combined streams of air act as invisible hands in manipulating and transporting wafers automatically, yet they avoid solid contact much of the time. This "air bearing system" handles wafers with unprecedented care, helps produce uniform wafers more consistently, and may require less floor space than most mechanized equipment, depending upon the application.

"Reject rates are reduced by 10-20% where the air bearing system is used," said Don McDonald, Product Manager at Advanced Memory Systems, Inc., "but this is only one of the advantages." He then spoke of gains in speed, uniformity, consistency, repeatability, definition, and an overall improvement in semiconductor quality and yield.

"You can probably increase throughput by 30%," said McDonald, "if that's what you are looking for. But we're more concerned with the consistency of fine geometry definition. With this new equipment, definition and consistency are improved by at least 50%." The micron lines—lines between the paths and circuits on the wafer —are more precisely repeated, because wafers are han-

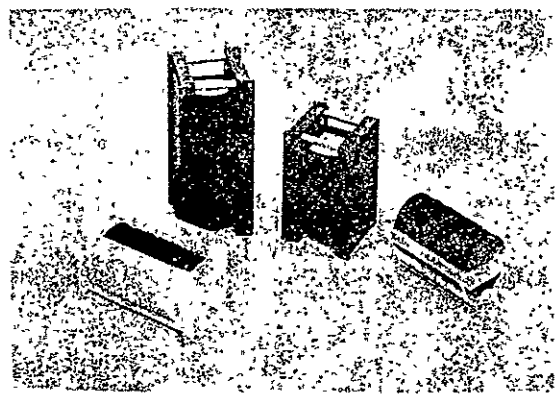

Fig. 1—Wafer Carriers. Carriers come in several types and sizes, but all hold the standard 25 wafers. The white and clear carriers are of quartz and silicon respectively for high temperature operations.

dled with more care and consistency. There is actually cleaner development of the film on the wafer due to the automatic non-contact technique. There is much greater consistency in the application and spraying of the photo-resist, and the line areas are etched without undercutting the lines themselves. The result can be likened to the difference between a good and bad photograph

The Coanda Effect

This air transport system is based on a device called the "Linear Directional Air Bearing." The patent holder, C. Arthur Lasch, co-founder and president of GCA/Industrial Modular Systems Corp., used a principle known as the "Coanda Effect", namely, that when high velocity, low pressure air is directed onto a track through tangential jets, the flow acts as a pump that entrains air from the atmosphere. Differential pressures from above and below result in a vector forcing air down along the track's surface. Any regularly shaped object will reach equilibrium in the stream above the track and move as directed by the jet's flow. This also may be called *pressure gradient bending*, a pressure gradient is produced which bends the jets' flow toward the track's surface. See Fig. 2.

The resulting air bearing system moves wafers on a .008 to .015 inch air cushion within a processing station or in entering/departing stations.

An example of wafer processing improvement with this equipment is seen in photo-resist coating. Production rates are reported to have jumped as high as 1200 wafers per hour (depending upon spin cycle duration). However, this is only part of the function of the air bearing system. Wafers are not only moved on a cushion of air through developing, etching, photo-resist coating, and high-temperature processing, but they can be moved into and out of the work stations with the new technique.

A Smooth Transition

A noteworthy feature of the units in the air bearing system is that they *are* units; that is, separate independent modules. As AMS's McDonald points out, "You don't have to have the whole line to make each piece worthwhile. Each is valuable on its own merits. You can adapt your initial capital investment to your budget as well as your needs."

One mechanical apparatus, designed to do a similar job, functions well and is, perhaps, easier to set up. Here, however, the wafers are carried in flat trays five at a time and are exposed to possible damage. In addition, the trays are incompatible with flip-transferrable carriers. Again, loading/unloading becomes a sticky situation that requires man-handling. There is another mechanical system that utilizes flip-transferrable carriers, but the company is just starting to release its equipment, and it is premature to evaluate it at this point.

The early air bearing systems, installed three to four years ago, were each custom designed. It was difficult to see how each would work in other situations. A little more than a year ago an off-the-shelf product line

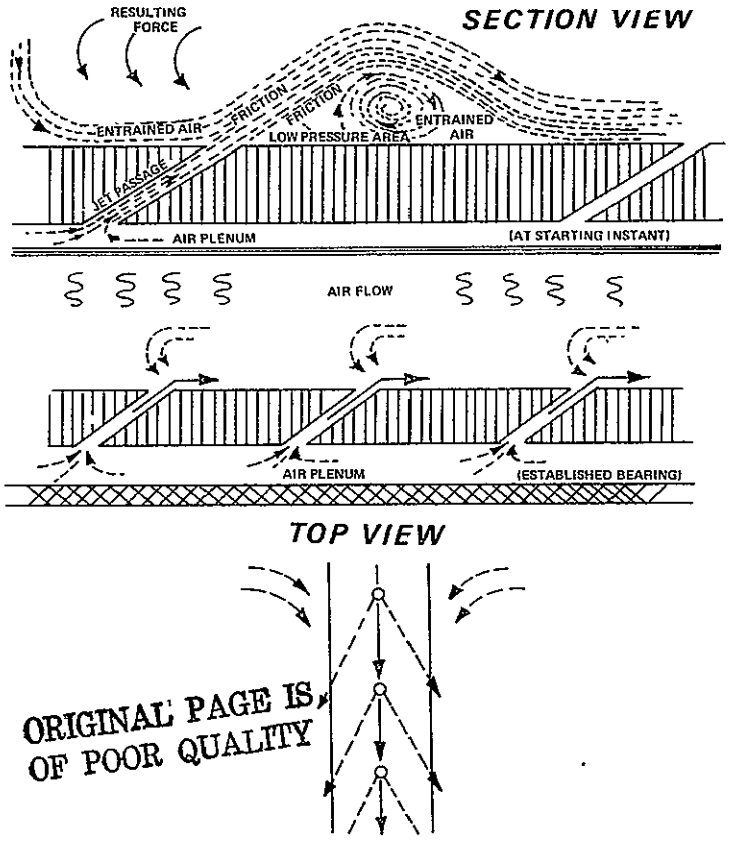

Fig. 2—Coanda Effect (pressure gradient bending).

began appearing, module by module. General application proved successful and the line is still growing. Currently available are. a loader/unloader, a wafer feed system (used in mask alignment), an automatic developer system, a rapid-quench furnace transport, and of course, the flip-transferrable carriers.

Although this is still the only air bearing system of its kind on the market (a related technique has been used to move bulk grains, tin cans, and various lightweight objects in packaging operations) several manufacturers are into the carrier business. The largest semiconductor manufacturers were making their own flip-transferrable carriers in-house several years ago. According to GCA/Industrial Modular Systems Corp., the system's manufacturer, they have cooperated with other companies like Emerson Plastronics, Fluoroware, Fluorocarbon, and others to allow them to begin manufacturing similar carriers. For high temperature operations, companies like Berkeley Glass, International Quartz and Quar-Tronics are making quartz and silicon carriers. All hold 25 wafers each, and are compatible for flip-transferring.

The starting point for air bearing operations is the transition from single, manual transport of wafers to mass air transport. An operator selects wafers individually to enter the loader/unloader. The carrier is then indexed up to present its next empty slot (see Fig. 4). Conversely, the machine can unload wafers automatically and feed them into any sort of connecting equipment. A prime feature here is speed. Hand-loading requires 5-10 seconds per wafer; with the air bearing

unit, throughput is at one wafer per second. Typical cost for the unit and a laminar flow work station is $4500.

Mask Alignment

A variation of the loader/unloader is the air bearing wafer feed system. This unit automatically unloads wafers from a standard carrier, orients them, carries them into a mask aligner for fine alignment and exposure, then transfers them to a carrier at the other end of the station (see Fig. 5). This module is directly compatible with the mask aligner made by K&S. Kasper makes an aligner that incorporates the air bearing feed system within the unit. Such companies operate under a licensing agreement with the air bearing manufacturer. This includes other approaches to the task. Mask aligner makers, like Co-Bilt, offer handling systems that accept the wafer carrier, but move the wafers mechanically. The air bearing wafer feed system is connected to the mask aligner so that each step of the operation is cued by the corresponding action of the aligner. Therefore, the system loads and unloads the wafers without any direct command from the operator, who is free to keep his mind on running the mask aligner (a precision task that truly requires all of his attention).

A wafer in the above operation goes through four steps:

1. The wafer is removed from its input carrier and transported on an air bearing to a buffer position where it waits until the pre-alignment chuck is clear.
2. The wafer moves to the pre-alignment fixture. It is rotated on air jets until the flat or notch is centered on an optical sensor. This position is maintained by vacuum.
3. The wafer is moved into the mask aligner for fine alignment and exposure.
4. The wafer is moved out of the aligner and into the output carrier, again, on an air bearing.

A typical cost for an entire installation, including the work station, mask aligner, and feed system is $41,500.

Programmed Coating and Developing

The automatic photoresist coater can be programmed as desired. Again, the linear air bearing system, without human or mechanical contact, gently unloads wafers from the input carriers, transports them to and from spin chucks, and loads them onto output carriers for baking (see Fig. 6). The entire coating cycle is governed by pre-set programs dictated by plug-in cards that control time, acceleration, ramp, and spin speed. Process functions may include: spray washing with a cleaning solvent and spin drying, pre-coating with materials such as silane-zylene and spin drying, and coating with photo-resist and spin drying. Compared to other methods, only a fourth to a third the amount of photoresist is required. Coating thickness variations of less than 100Å across the wafer surface are reported as typical.

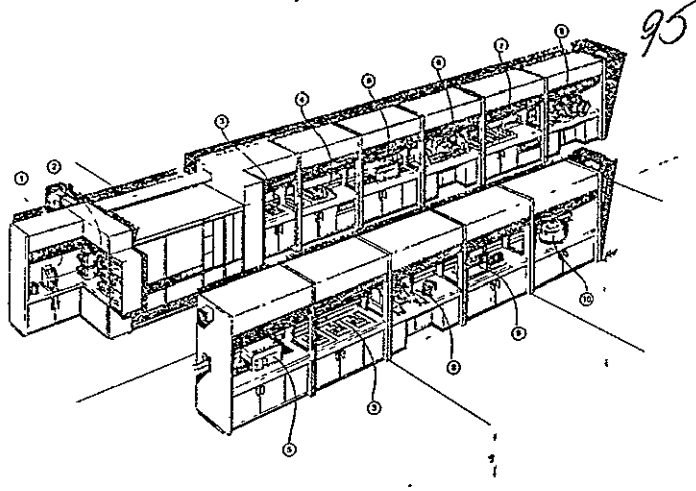

Fig. 3—Partial Production Line—(1) Loader/Unloader, (2) Continuous Diffusion Station, (3) Etching/Cleaning Area, (4) Automatic Photo-Resist Coater, (5) IR Bake Oven, (6) Automatic Mask Aligner, (7) Automatic spin/Spray Developer, (8) Inspection station.

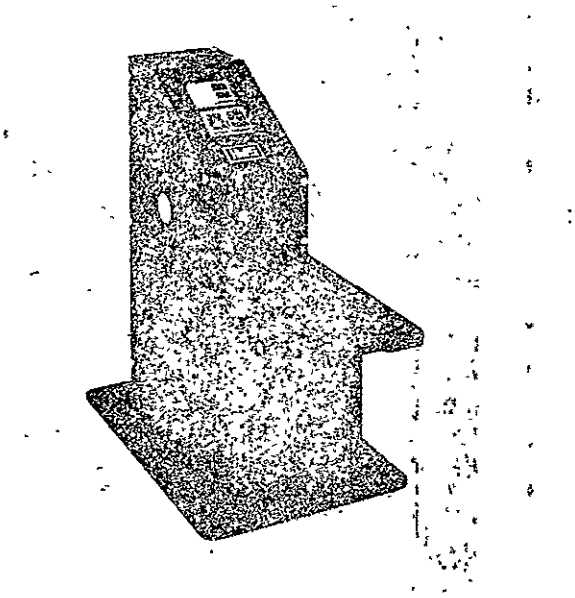

Fig. 4—Loader/Unloader. A carrier rises step by step from the I-shaped cavity, and with each step a wafer moves out of or into the slot that is on the level of the air bearing track.

The photo-resist spray developers appear very similar to the coaters. Four standard carriers are loaded into the input side. A start button is pressed and wafers are carried through the spray development cycle four at a time, then reloaded into output carriers, all by air bearing. Of course, the plug-in programs are unique for each operation. A typical program for developing a KTFR film of one micron thickness is:

1. Developer is sprayed on for five seconds at 800 rpm.
2. For the next two seconds developer and rinser are sprayed simultaneously.
3. A five-second rinse during which spin speed is accelerated to 4000 rpm.

4. A five-second spin-dry completes the 17-second process.

Such a cycle gives a throughput rate of 650-700 wafers per hour. One-micron lines with one-micron spacing are produced, with a reported edge definition of better than 0.1 micron. The typical cost of a coater or developer with laminar flow work station is $27,000.

The air bearing principle also has invaded high temperature processing. However, the system doesn't use air; instead it employs another gas mixture less sensitive to heat. The rapid quench furnace transport system automatically transfers wafers individually from a carrier into a soak position in a furnace via a quartz gas bearing track. After the specified soak time, the track is pulsed with high-velocity gas, which couples to the wafer and accelerates it from the furnace tube (in 0.2 seconds) to a water-cooled vacuum plate. While this wafer is cooled, the next wafer is carried into the tube. The "quenched" wafer is transported from the chill plate to a carrier. The sequence is repeated automatically until all the waiting wafers have been cycled. This module is said to be most useful in gold diffusion and aluminum and gold spike alloying. System cost varies greatly with numbers and types of furnaces and other individual requirements.

Some firms are reluctant to automate because of the assumed difficulty in adapting to the variety of wafer sizes. However, all modules of the air bearing system accommodate wafers ranging in diameter from 0.875 to 3.50 inches, which includes all wafer sizes currently used in the semiconductor industry. Most standard carriers are compatible also.

Conclusion

The need to reckon with the costs of wafer processing has increased over the past five to eight years, especially since sophisticated MSI and LSI circuitry have begun to dominate electronic component production. Manual wafer handling and its attendant high damage rate, slow production speeds, low yield, and lack of consistency comprise the primary arena of loss. The use of flip-transferrable carriers was the first step in attacking the problem, and they are being widely and rapidly accepted. Now the linear directional air bearing system seems to be emerging as the next step. The technique has been applied successfully to at least half a dozen common processing operations. Noteworthy increases in yield, production speed, and wafer uniformity, as well as reductions in reject rates have been achieved. Still, hand processing is not entirely obsolete, since the air bearing system is compatible with hand operations during probation and conversion. It is still speculation, but the industry dream of fully automated "no-touch" wafer processing may be around the corner.

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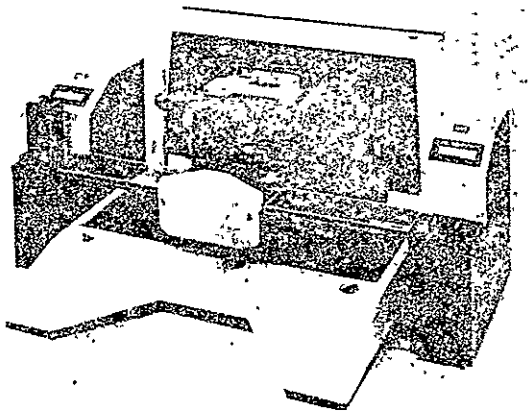

Fig. 5—Wafer Feed System. Wafers are automatically unloaded from the carrier, oriented, air-lifted into the mask aligner, and in proper continuing sequence, transferred to a receiving carrier.

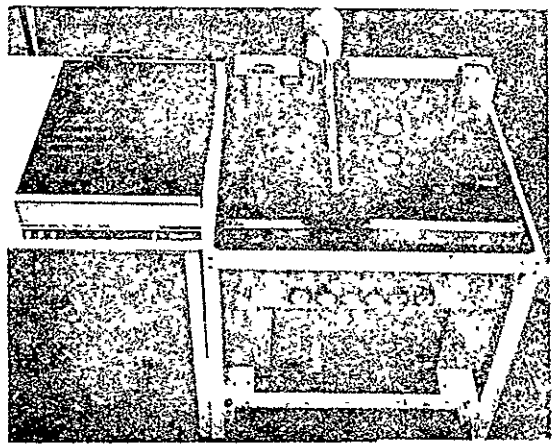

Fig. 6—Automatic Photoresist Coater. Airborne wafers can be unloaded four at a time from input carriers to spin chucks; then from the chucks to waiting output carriers; all programmed and all without human contact.

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